W681307 Product Datasheet

USB1.1 CODEC Microprocessor
Control Unit with 32KB Mask ROM
and 4KB RAM.

Publication Release Date: May, 2007
Revision 1.3

AMENDMENT HISTORY

Ver	Date	Filename	Author	Changes (•: modified, √: added, ×: removed)	Reference
1.0	2006/11/22	W681307_Data Sheet_V1.0	MCSu		
1.1	2006/12/02	W681307_Data Sheet_V1.1	MCSu	• Modify register 0x14C4. • Modify Figure 14-2.	W681307_Data Sheet_V1.0
1.2	2006/12/28	W681307_Data Sheet_V1.2	MCSu	• Modify register 0x14E5.	W681307_Data Sheet_V1.1
1.3	2007/07/23	W681307_Data Sheet_V1.3	TYChiu	• Modify endpoint table 18.2.1.	W681307_Data Sheet_V1.2

CONTENTS

1. GENERAL DESCRIPTION ..... - 9 -
2. FEATURES ..... - 10 -
3. PIN CONFIGURATION ..... - 11 -
4. PINS DESCRIPTION ..... - 12 -
5. SYSTEM DIAGRAM ..... - 17 -
5.1 Function Block Diagram ..... - 17 -
5.2 I/O Cells in Winbond MCU Chip ..... - 18 -
6. ELECTRICAL CHARACTERISTICS ..... - 20 -
6.1 Absolute Maximum Ratings ..... - 20 -
6.2 DC Characteristics ..... - 20 -
6.3 Analog Transmission Characteristics ..... - 21 -
6.3.1 Amplitude Response for Analog Transmission Performance ..... - 21 -
6.3.2 Distortion Characteristics for Analog Transmission Performance ..... - 21 -
6.4 Analog Electrical Characteristics ..... - 22 -
6.5 Power Drivers – PO1, 2 ..... - 22 -
6.6 Programmable Output Linear Regulator ..... - 23 -
6.7 USB PHY Electronic Characteristics (25°C, VDD_USB = 3.3V, DVDD1, 3 =1.9V) ..... - 23 -
6.8 USB PLL Electronic Characteristics (25°C, AVDD = 3.3V, DVDD1, 3 =1.9V) ..... - 24 -
6.9 The Crystal Specification Requirement ..... - 24 -
6.10 Recommended Crystal Specification ..... - 25 -
7. MEMORY AND REGISTER MAP ..... - 26 -
7.1 Program Memory Map ..... - 26 -
7.2 Data Memory Map ..... - 26 -
7.3 Register Map ..... - 27 -
7.3.1 Mixer and Speech Logic Registers Overview ..... - 27 -
7.3.2 Support Logic Registers Overview ..... - 27 -
7.3.3 Interface Logic Registers Overview ..... - 28 -
7.3.4 Speech Interface Registers Overview ..... - 28 -
7.3.5 Processor Interface Registers Overview ..... - 29 -
7.3.6 Transcoder DSP Registers Overview ..... - 29 -
7.3.7 Echo Canceller Registers Overview ..... - 30 -
7.3.8 Soft Clip Registers Overview ..... - 31 -
7.3.9 CODEC Digital Part ..... - 31 -
7.3.10 Sounder Path Select ..... - 31 -
7.3.11 Frequency Adjustment of Crystal Oscillator ..... - 31 -
7.3.12 Specific Register ..... - 31 -
7.3.13 VAG Selection ..... - 32 -
7.3.14 CODEC Control Register Overview ..... - 32 -
7.3.15 Specific Registers ..... - 32 -
7.3.16 Test Cases and Debugging Registers Overview ..... - 32 -
7.3.17 Charge Park Detection ..... - 32 -
7.3.18 DA High Pass Filter Selection ..... - 33 -
7.3.19 TI PATH Selection ..... - 34 -
7.3.20 Network side / Acoustic side Power Measurement ..... - 34 -
7.3.21 PCM Highway Channel Registers Overview ..... - 35 -
7.3.22 SPI Interface Registers Overview ..... - 35 -
7.3.23 Data Flash SPI Interface Registers Overview ..... - 36 -

7.3.24 W2S Interface Registers Overview ..... - 36 -
7.3.25 USB Control Registers Overview ..... - 37 -
7.3.26 ISP Mode ..... - 38 -
8. SUPPORT LOGIC ..... - 39 -
8.1 Clock Control & Reset 32K ..... - 40 -
8.1.1 Overview ..... - 40 -
8.1.2 Functionality ..... - 40 -
8.1.3 Clock Enable Register ..... - 40 -
8.2 Interrupt Control ..... - 41 -
8.2.1 Overview ..... - 41 -
8.2.2 Functionality ..... - 41 -
8.2.3 Interrupt Registers ..... - 43 -
8.2.4 Extends of interrupt ..... - 44 -
8.3 Ringer Tone Generator ..... - 45 -
8.3.1 Overview ..... - 45 -
8.3.2 Functionality ..... - 45 -
8.3.3 Sounder Tone Register Definition ..... - 46 -
8.3.4 Sounder Volume Register Definition ..... - 46 -
8.3.5 Example of use ..... - 46 -
8.3.6 Sounder Registers ..... - 47 -
8.4 PIEZO Tone Generator ..... - 48 -
8.4.1 Overview ..... - 48 -
8.4.2 Functionality ..... - 48 -
9. INTERFACE LOGIC ..... - 49 -
9.1 Keypad Scanner ..... - 49 -
9.1.1 Overview ..... - 49 -
9.1.2 Use of the Keypad Scanner ..... - 50 -
9.1.3 Use of a Software Keypad Scanner ..... - 50 -
9.2 I/O Ports ..... - 50 -
9.3 Keypad Control Registers ..... - 51 -
9.3.1 Key Location and Size Programming ..... - 53 -
9.4 Timers ..... - 53 -
9.4.1 Watch Dog Control ..... - 54 -
9.4.2 Timer 1ms Control1 ..... - 54 -
9.4.3 Timer Control ..... - 54 -
9.4.4 1S Counter ..... - 55 -
9.4.5 Watch Dog Kick ..... - 55 -
9.4.6 1ms Counter ..... - 55 -
10. SPEECH INTERFACE ..... - 56 -
10.1 Overview ..... - 56 -
10.2 Functionality ..... - 56 -
10.3 PCM Serial Interface ..... - 57 -
10.3.1 Use with Additional External Lines ..... - 57 -
10.3.2 I/O Ports ..... - 57 -
10.3.3 Status of Speech Interface When Reset ..... - 58 -
10.4 Internal CODEC Control ..... - 58 -
10.5 PCM Interface Registers ..... - 58 -
10.5.1 Speech Control 0 ..... - 58 -

10.5.2 Specific Register ..... - 58 -
10.5.3 Speech IO Direction ..... - 59 -
10.5.4 Speech IO Input Data ..... - 59 -
10.5.5 Speech IO Output Data ..... - 59 -
10.5.6 Speech IO Mask ..... - 60 -
10.5.7 Fsync Counter ..... - 60 -
10.6 The multiplexer to connect 5 PCM channels to 4 processor channels ..... - 60 -
10.6.1 Multiplexer control register ..... - 60 -
10.7 PCM Highway Interface ..... - 61 -
10.7.1 The Introduction of PCM Modes ..... - 61 -
10.7.2 The Description of PCM Highway Interface Registers ..... - 63 -
10.8 Digital Gain Multiplexer ..... - 66 -
10.8.1 Fine-Tuning Gain Stage Registers ..... - 66 -
11. PROCESSOR INTERFACE ..... - 70 -
11.1 Overview ..... - 70 -
11.2 Functionality ..... - 70 -
11.3 Processor Access Sequencer ..... - 70 -
11.4 Read Multiplexer ..... - 73 -
11.5 Processor Interface Control Registers ..... - 73 -
11.5.1 AuxOpPort ..... - 73 -
11.5.2 DiagSel ..... - 74 -
11.5.3 Diag_CS ..... - 75 -
11.5.4 Diag_CS3 ..... - 76 -
11.5.5 Multiplier_Enable ..... - 77 -
11.6 In System Programming Mode ..... - 77 -
11.6.1 Hardware Setting Usage ..... - 77 -
11.6.2 Software Command Usage ..... - 77 -
11.6.3 ISP_CTRL (Hardware & Watchdog Reset Control Register) ..... - 78 -
11.6.4 Specific Register ..... - 78 -
11.7 MASK ROM Mode ..... - 79 -
11.7.1 Usage ..... - 79 -
12. SPEECH PROCESSOR ..... - 80 -
12.1 Transcoder DSP ..... - 80 -
12.2 The Description of the Activation Registers ..... - 81 -
12.2.1 MIXER_EN ..... - 81 -
12.2.2 SPEECH LOGIC_EN ..... - 81 -
12.3 The Description of Transcoder DSP Registers ..... - 81 -
12.3.1 Connect0 ..... - 82 -
12.3.2 Specified Register ..... - 82 -
12.3.3 Specified Register ..... - 82 -
12.3.4 Specified Register ..... - 82 -
12.3.5 PCMmode0 ..... - 83 -
12.3.6 InputGain0 ..... - 83 -
12.3.7 OutputGain0 ..... - 83 -
12.3.8 ToneFreqA0 ..... - 83 -
12.3.9 ToneFreqB0 ..... - 84 -
12.3.10 ToneVolA0 ..... - 84 -
12.3.11 ToneVolB0 ..... - 84 -

12.3.12 ToneEna0 ..... - 84 -
12.3.13 SideTone ..... - 85 -
12.3.14 Loopback_EN ..... - 85 -
12.3.15 Specified Register ..... - 85 -
12.3.16 Connect1 ~ ToneEna1 ..... - 85 -
12.3.17 Connect2 ~ ToneEna2 ..... - 85 -
12.3.18 SideToneChannel_Ena ..... - 86 -
12.3.19 Connect3 ~ ToneEna3 ..... - 86 -
12.4 PCM Mixer Matrix ..... - 86 -
12.5 Gain Tables ..... - 86 -
13. ECHO CANCELLER ..... - 89 -
13.1 Half AEC Block Diagram ..... - 89 -
13.1.1 Acoustics Suppression ..... - 89 -
13.1.2 Network Power Estimation ..... - 90 -
13.1.3 Acoustic Power Estimation ..... - 90 -
13.1.4 Auto Gain Control ..... - 91 -
13.2 The Software Interface of Speech Processor ..... - 91 -
13.3 Activation Registers ..... - 91 -
13.3.1 UP_CONFIG ..... - 91 -
13.3.2 UP_RESET ..... - 92 -
13.3.3 EC_BELTA ..... - 92 -
13.3.4 Specific Register ..... - 92 -
13.4 Performance Adjustment Registers ..... - 92 -
13.4.1 Acoustic Suppressor Register ..... - 92 -
13.4.2 Acoustic Side Control Registers ..... - 93 -
13.4.3 Network Side Control Registers ..... - 95 -
13.4.4 ACOUSTIC / NETWORK Active Status ..... - 98 -
13.4.5 AGC Control Registers ..... - 98 -
13.4.6 Noise Suppressor Registers ..... - 100 -
13.4.7 AEC Soft Clip ..... - 101 -
13.5 Acoustic Side / Network Side Power Measurement ..... - 106 -
13.5.1 ACOUSTIC_SHORT_TERM_POWER ..... - 106 -
13.5.2 ACOUSTIC_LONG_TERM_POWER ..... - 106 -
13.5.3 ACOUSTIC_POWER_DEVIATION ..... - 107 -
13.5.4 ACOUSTIC / NETWORK Active Status ..... - 107 -
13.5.5 NETWORK_SHORT_TERM_POWER ..... - 107 -
13.5.6 NETWORK_LONG_TERM_POWER ..... - 108 -
13.5.7 NETWORK_POWER_DEVIATION ..... - 108 -
13.5.8 ACOUSTIC / NETWORK Active Status ..... - 108 -
14. SYSTEM FUNCTION ..... - 109 -
14.1 Power On Reset ..... - 109 -
14.1.1 CODEC On/Off Scheme ..... - 109 -
14.1.2 CODEC Digital Part ..... - 110 -

14.2 ADC Adaptive Bit Flip Probability ..... - 110 -
14.3 Sounder Signal Selection ..... - 111 -
14.4 Frequency Adjustment of Crystal Oscillator ..... - 112 -
14.5 Specific Register ..... - 113 -
14.6 VAG Selection ..... - 113 -
14.7 TG Gain Register ..... - 114 -
14.8 PO Gain Register ..... - 115 -
14.9 The PCM CODEC ..... - 117 -
14.9.1 Block Diagram ..... - 117 -
14.9.2 Analog Interface and Signal Path ..... - 117 -
14.9.3 Control Register: CODEC_CTRL ..... - 118 -
14.9.4 Specific Register ..... - 119 -
14.9.5 Specific Register ..... - 119 -
14.10 RECEIVE_DIAG ..... - 119 -
14.11 Specific Register ..... - 121 -
14.12 EnAllClock ..... - 121 -
14.13 CODEC_Test_Sel ..... - 121 -
14.14 Test_SYSCLKOUT ..... - 122 -
14.15 BGP_LPF_EN ..... - 122 -
14.16 CODEC Status Indicator ..... - 122 -
14.17 BandGap Voltage Adjustment ..... - 123 -
14.18 Specific Register ..... - 123 -
14.19 Linear Regulator Voltage Controller Register ..... - 123 -
14.20 Core PWR_Det ..... - 124 -
14.21 DA High Pass Filter Selection ..... - 124 -
14.22 TI Path Selection ..... - 125 -
15. SERIAL PERIPHERAL INTERFACE ..... - 127 -
15.1 Serial Peripheral Interface – SPI signals ..... - 127 -
15.1.1 SPI_Control 0 ..... - 128 -
15.1.2 SPI_Control 1 ..... - 128 -
15.1.3 SPI Status ..... - 129 -
15.1.4 SPI Interrupt Enable ..... - 129 -
15.1.5 DumpByte ..... - 129 -
15.1.6 Write TX FIFO ..... - 129 -
15.1.7 Read RX FIFO ..... - 130 -
15.1.8 SPI_Transfer_Size ..... - 130 -
15.1.9 SPI_Start_rtx ..... - 130 -
16. SPI FOR SERIAL DATA FLASH ..... - 131 -
16.1 Introduction to SPI of Serial Data Flash ..... - 131 -
16.2 Block Diagram ..... - 131 -
16.3 Data Format ..... - 132 -
16.4 FSM ..... - 134 -
16.5 FIFO/RAM ..... - 134 -
16.6 Interrupt ..... - 134 -
16.7 DF_SPI Register Group ..... - 134 -
16.7.1 DF_CLK ..... - 134 -
16.7.2 DF_CMD_LEN ..... - 135 -
16.7.3 DF_DATA_LEN ..... - 135 -

16.7.4 DF_INTR_REG ..... - 135 -
16.7.5 DF_CMD_B1 ~ DF_CMD B5 ..... - 136 -
16.7.6 DF_CLK_FORMAT ..... - 137 -
16.7.7 DF_FIFO_DATA ..... - 138 -
16.7.8 DF_CNT ..... - 138 -
16.7.9 DF_WR_CNT ..... - 139 -
16.7.10 DF_RD_CNT ..... - 139 -
16.8 Example of W25X20/40/80 Serial Flash ..... - 139 -
17. WINBOND 2-WIRE SERIAL BUS ..... - 141 -
17.1 Introduction to Winbond 2-Wire Serial bus ..... - 141 -
17.2 The Description of W2S Register ..... - 141 -
17.2.1 W2S_Enable ..... - 141 -
17.2.2 EEPROM_Config ..... - 142 -
17.2.3 Prescale_Lo ..... - 142 -
17.2.4 Prescale_Hi ..... - 142 -
17.2.5 RdWrFIFO ..... - 143 -
17.2.6 Force_Activity ..... - 143 -
17.2.7 W2S_Status ..... - 143 -
17.2.8 FIFORdPtr ..... - 144 -
17.2.9 FIFOWrPtr ..... - 144 -
17.2.10 ForceAckFail ..... - 144 -
17.2.11 W2S_Misc ..... - 144 -
18. USB DEVICE CONTROLLER AND TRANSCEIVER ..... - 145 -
18.1 Overview ..... - 145 -
18.2 Functionality ..... - 145 -
18.2.1 Endpoints ..... - 146 -
18.2.2 Descriptor Rom ..... - 146 -
18.2.3 Configurations and Interfaces ..... - 147 -
18.2.4 Audio Class ..... - 148 -
18.2.5 HID Class ..... - 149 -
18.2.6 USB ISP mode ..... - 150 -
18.2.7 Vendor Command ..... - 150 -
18.3 USB Registers ..... - 150 -
18.3.1 USB Enable Register ..... - 150 -
18.3.2 USB Interrupt Register A ..... - 150 -
18.3.3 USB Interrupt Register B ..... - 151 -
18.3.4 EndPoint 0 – Control In/Out Registers ..... - 152 -
18.3.5 EndPoint 1 and 2 – ISO In/Out Registers ..... - 153 -
18.3.6 EndPoint 3 – Bulk In Registers ..... - 155 -
18.3.7 EndPoint 4 – Bulk Out Registers ..... - 156 -
18.3.8 EndPoint 5 – Interrupt In Registers ..... - 157 -
18.3.9 Specific Register ..... - 158 -
18.3.10 Specific Register ..... - 158 -
18.3.11 Specific Register ..... - 158 -
19. PACKAGE DIMENSIONS ..... - 159 -

1. GENERAL DESCRIPTION

The main product targets for the USB CODEC MCU chip are：

- 27.648MHz four cycle 8032 MCU
- Support external Flash and easy transfer to low cost Mask ROM production
- Universal Serial Bus (USB) v1.1 compliant device controller and PHY, capable of full speed communication (12MHz) with up to 5 configuration end –points
- 8KHz voice sampling rate and 16bits of ADC/DAC
- Support AEC/AGC for on-chip speaker phone support
- Support Keypad function

Winbond MCU chip will be available in the following package

Device	Package	Description
W681307D xxxx	100 pin LQFP	Normal mode, Mask ROM 32K, x2 CLK

2. FEATURES

Micro controller

- Embedded 27.648MHz WINBOND® Turbo 8032 Micro-Controller with 4 Clocks per Machine Cycle
- 4K system RAM, 32K MASK ROM
- Core 1.9V, I/O 3.3V
- Power on Reset circuit
- Software Power Down mode
- In system Programming (ISP) for 29/39/49 series flash ROM
- Built-in Keypad Scan, Watchdog, Wait State

Speech Processor/Interface

- 4 Processor Channels
- Programmable input/output gain stage
- Programmable Auto Gain Control (AGC) stage
- Programmable Soft Clip gain stage
- Acoustic Echo Cancellation (AEC) with half duplex, absolute/relative mode
- PCM interface for External CODEC or PCM interface
- SNDR output
- Built in DTMF tone generator

PCM CODEC

- One Built-in PCM CODEC
- Analogue input amplifier with Internal programmable gain stage
- Analog output amplifier: Push pull drive, Internal programmable gain stage

USB 1.1

- Universal Serial Bus USB v1.1 compliant device controller and PHY, capable of full speed communication (12MHz) with up to 5 configuration end –points.

UART

- T8032 UART for data transmit application.

PCM Highway

- The 1st PCM Highway has four channels..
- All channels support 8/16 bits pcm format, and IOM2 mode.
- Works in master or slave modes with external CODEC.

W2S

- Support three EEPROM format page modes.
- Support six kinds of W2S bus clocks.

SPI interface

- Works in master or slave modes.

SPI Flash interface

- Works in master with the Winbond SPI interface of series flash.

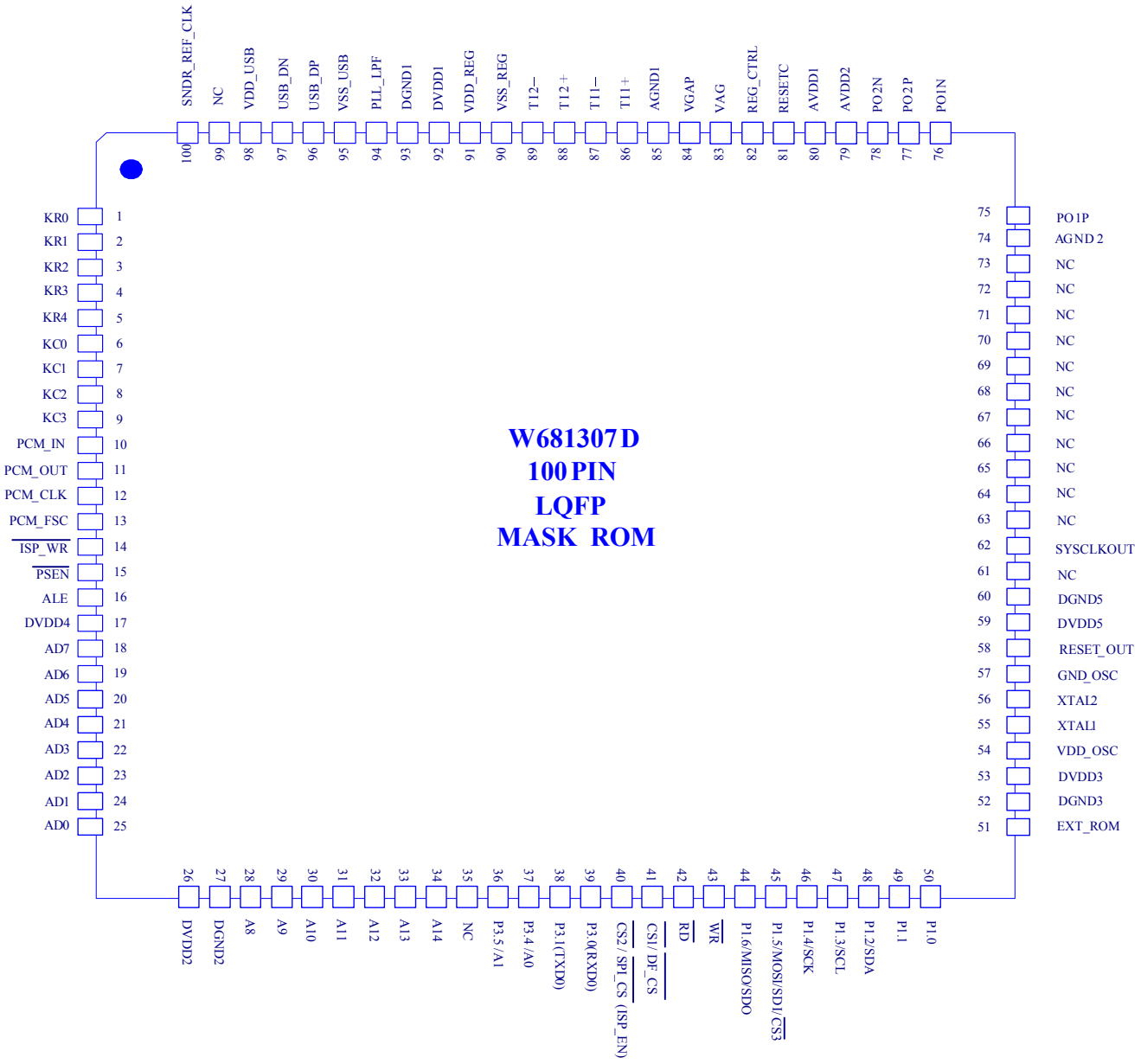
ISP

- In-system-Programming capability with software command via UART or USB interface.

Package

- 100 pin LQFP package

3. PIN CONFIGURATION



4. PINS DESCRIPTION

Pin no.	Pin name	I/O	State during Reset	State after Reset	Pin type section	Function Description	Alternative Function
1	KR0	I/O	Input H	Input H	PC3B01U	Keypad Scan row output	GPIO
2	KR1	I/O	Input H	Input H	PC3B01U	Keypad Scan row output	GPIO
3	KR2	I/O	Input H	Input H	PC3B01U	Keypad Scan row output	GPIO
4	KR3	I/O	Input H	Input H	PC3B01U	Keypad Scan row output	GPIO
5	KR4	I/O	Input H	Input H	PC3B01U	Keypad Scan row output	GPIO
6	KC0	I/O	Input L	Input L	PC3B01D	Keypad Scan column input	GPIO
7	KC1	I/O	Input L	Input L	PC3B01D	Keypad Scan column input	GPIO
8	KC2	I/O	Input L	Input L	PC3B01D	Keypad Scan column input	GPIO
9	KC3	I/O	Input L	Input L	PC3B01D	Keypad Scan column input	GPIO
10	PCM_IN	I/O	**Input H**	**Input H**	**PC3B02U**	PCM high way, Data input	GPIO
11	PCM_OUT	I/O	**Input H**	**Input H**	**PC3B02U**	PCM high way, Data output	GPIO
12	PCM_CLK	I/O	Input L	Input L	**PC3B02D**	PCM high way, Clock In/Output	GPIO
13	PCM_FSC	I/O	Input L	Input L	**PC3B02D**	PCM high way, Frame pluse In/Output	GPIO
14	**$\overline{\text{ISP_ WR}}$**	O	Input H	Input H	PC3B02U	In the normal mode operation, this pin is high. In the in-system-programming (PROG) state, this pin is used for $\overline{\text{WR}}$ function for writing flash memory program.	
15	$\overline{\text{PSEN}}$	O	Input H	Output H	PC3B02U	8032T for Program Memory Strobe Enable	
16	ALE	I/O	Input **H**	Output H	PC3B02U	Output address latch enable (ALE) function	
17	DVDD4	PWR	-	-	PVDDC	Digital supply voltage 4 (for digital I/O pads power)	
18	AD7	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 7	
19	AD6	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 6	
20	AD5	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 5	
21	AD4	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 4	
22	AD3	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 3	
23	AD2	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 2	
24	AD1	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 1	
25	AD0	I/O	Input H	Input H	PC3B02U	8032T Multiplexed Address/Data pin 0	
26	DVDD2	PWR	-	-	PVDDR	Digital supply voltage 2 (for digital I/O pads power)	
27	DGND2	PWR	-	-	PVSSR	Digital ground 2 (I/O ground)	

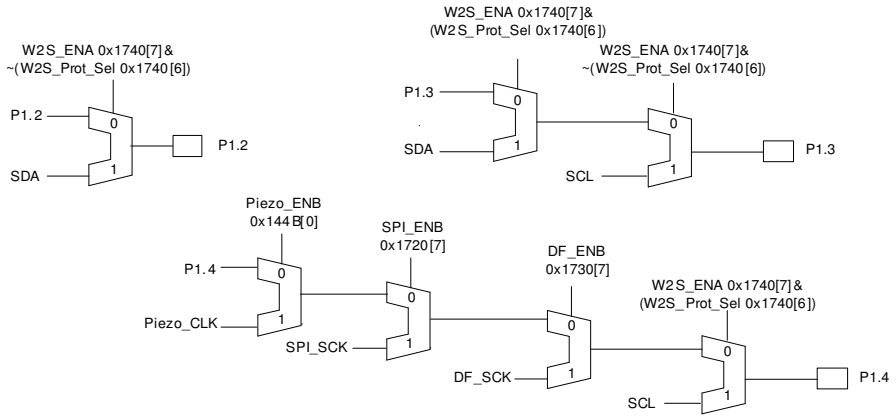
29	A9	I/O	Input H	Output H	PC3B02U	8032T Address Line 9	
30	A10	I/O	Input H	Output H	PC3B02U	8032T Address Line 10	
31	A11	I/O	Input H	Output H	PC3B02U	8032T Address Line 11	
32	A12	I/O	Input H	Output H	PC3B02U	8032T Address Line 12	
33	A13	I/O	Input H	Output H	PC3B02U	8032T Address Line 13	
34	A14	I/O	Input H	Output H	PC3B02U	8032T Address Line 14	
35	NC	I/O	Input H	Output H	PC3B02U	No connection	
36	P3.5 /A1	I/O	Input H	Input H	PC3B02U	Port3 Bit 5 of 8032T	
37	P3.4 /A0	I/O	Input H	Input H	PC3B02U	Port3 Bit 4 of 8032T	
38	P3.1 /TXD0	I/O	Input H	Input H	PC3B02U	Port 3 Bit 1 or TXD serial transmit data port of internal 8032 Turbo	
39	P3.0 /RXD0	I/O	Input H	Input H	PC3B02U	Port 3 Bit 0 or RXD serial receive data port of internal 8032 Turbo	
40	$\overline{CS2}$ / $\overline{SPI_CS}$	**I/O**	**Input H**	**Output H**	**PC3T02**	**External Chip Select**	**General Purpose Output**
41	$\overline{CS1}$ / $\overline{DF_CS}$	**I/O**	**Input H**	**Output H**	**PC3T02**	**External Chip Select**	**General Purpose Output**
42	$\overline{RD}$ /P3.7	I/O	Input H	Input H	PC3B02U	8032T Read Strobe	P3.7 is 8032 I/O
43	$\overline{WR}$ / P3.6	I/O	Input H	Input H	PC3B02U	8032T Write Strobe	P3.6 is 8032 I/O
44	P1.6 /MISO/SDI	I/O	Input H	Input H	PC3B02U	Port 1 Bit 6	SPI function
45	P1.5 /MOSI/SDO / $\overline{CS3}$	I/O	Input H	Input H	PC3B02U	Port 1 Bit 5	SPI function or External Chip Select
46	P1.4 /SCK	I/O	Input H	Input H	PC3B02U	Port 1 Bit 4 or SPI interface clock output	This pin also supports wait state function.
47	P1.3 /SCL	I/O	Input H	Input H	PC3B02U	Port 1 Bit 3 or W2S interface clock output of programming EEPROM.	
48	P1.2 /SDA	I/O	Input H	Input H	PC3B02U	Port 1 Bit 2 or W2S interface serial data of programming EEPROM.	
49	P1.1	I/O	Input H	Input H	PC3B02U	Port 1 Bit 1	
50	P1.0	I/O	Input H	Input H	PC3B02U	Port 1 Bit 0	
51	EXT_ROM	I	Input H	Input	PC3D01U	When set this pin to high then the chip goes into external ROM mode.	
52	DGND3	PWR	-	-	PVSSC	Digital ground 3 (core power ground)	
53	DVDD3	PWR	-	-	PVDDC	Digital supply voltage 3 for core power, which should connect to DVDD1.	
54	VDD_OSC	PWR	-	-	PVDDC	Oscillation circuits supply voltage.	
55	XTAL1	I	Active	Active	PAnalog	13.824Mhz Crystal oscillator output	
56	XTAL2	O	Active	Active	PAnalog	13.824Mhz Crystal oscillator input	
57	GND_OSC	PWR	-	-	PVSSC	Oscillation circuits ground	

58	RESETOUT	O	L	H	PC3o01	Chip reset indication output. Active high after the reset state.
59	DVDD5	PWR	-	-	PVDDC	Digital supply voltage 5 (for digital I/O pads power)
60	DGND5	PWR	-	-	PVSSC	Digital ground 5 (I/O ground)
61	NC	O	Tristate	Tristate	PC3T02	No connection
62	SYSCLKOUT	O	Tristate	L	PC3T02	13.824 MHz system clock output
63	NC	O	Tristate	Tristate	PC3T02	No connection
64	NC	O	Tristate	Tristate	PC3T01	No connection
65	NC	O	Tristate	Tristate	PC3B01	No connection
66	NC	O	Tristate	Tristate	PC3T01	No connection
67	NC	O	Tristate	Tristate	PC3T01	No connection
68	NC	O	Tristate	Tristate	PC3T02	No connection
69	NC	O	Tristate	Tristate	PC3T02	No connection
70	NC	O	Tristate	Tristate	PC3T02	No connection
71	NC	O	Tristate	Tristate	PC3T01	No connection
72	NC	O	Tristate	Tristate	Analog	No connection
73	NC	I	Hi-Z	Hi-Z	Analog	No connection
74	AGND2	PWR	-	-	PVSSC	Analog ground for OP2 output amplifier
75	PO1P	O	Tristate	Tristate	PAnalog	Power amplifier output (non-inverting) - This pin is the non-inverting power amplifier output, which is an inverted version of the signal at PO1N. This pin is capable of driving a 120 Ω load to PO1N at 3V supply power. This pin is D.C. referred to the VAG pin. This pin is tri-state when the chip is in analog CODEC power down mode.
76	PO1N	O	Tristate	Tristate	PAnalog	Power amplifier output (inverting) - This pin is the inverting power amplifier output. This pin is capable of driving a 120 Ω load to PO1P at 3V supply voltage. This pin is D.C. referenced to the VAG pin. The PO1P and PO1N outputs are differential. This pin is tri-state when the chip is in analog CODEC power down mode.
77	PO2P	O	Tristate	Tristate	PAnalog	Power amplifier output (non-inverting) - This pin is the non-inverting power amplifier output, which is an inverted version of the signal at PO2N. This pin is capable of driving a 16 Ω load to PO2N at 3V supply power. This pin is D.C. referred to the VAG pin. This pin is tri-state when the chip is in analog CODEC power down mode.
78	PO2N	O	Tristate	Tristate	PAnalog	Power amplifier output (inverting) - This pin is the inverting power amplifier output. This pin is capable of driving a 16 Ω load to PO2P at 3V supply voltage. This pin is D.C. referenced to the VAG pin. The PO2P and PO2N outputs are differential. This pin is tri-state when the chip is in analog CODEC power down mode.
79	AVDD2	PWR	-	-	PVDDC	Analog supply voltage for OP2 amplifier
80	AVDD1	PWR	-	-	PVDDC	Analog supply voltage
81	RESETC	O	Tristate	Tristate	PAnalog	It should connect a capacitor for internal power on reset circuit.
82	REG_CTRL	O	Active	Active	PAnalog	Output signal of 3V linear regulator to drive the PNP transistor.
83	VAG	O	Tristate	1.5V	PAnalog	Analog reference voltage. This pin possesses the analog virtual ground of internal CODEC circuits.
84	VBGP	O	1. 0V	1.0V	Panalog	The Band gap output voltage. It is 1.0V volt typically.
85	AGND1	PWR	-	-	PVSSC	Analog ground
86	TI1+	I	Hi-Z	Hi-Z	PAnalog	This is the non-inverting input of the transmission operational amplifier TG1.
87	TI1-	I	Hi-Z	Hi-Z	PAnalog	This is the inverting input of the transmission operational amplifier TG1.
88	TI2+	I	Hi-Z	Hi-Z	PAnalog	This is the non-inverting input of the transmission operational amplifier TG2.
89	TI2-	I	Hi-Z	Hi-Z	PAnalog	This is the non-inverting input of the transmission operational amplifier TG2.

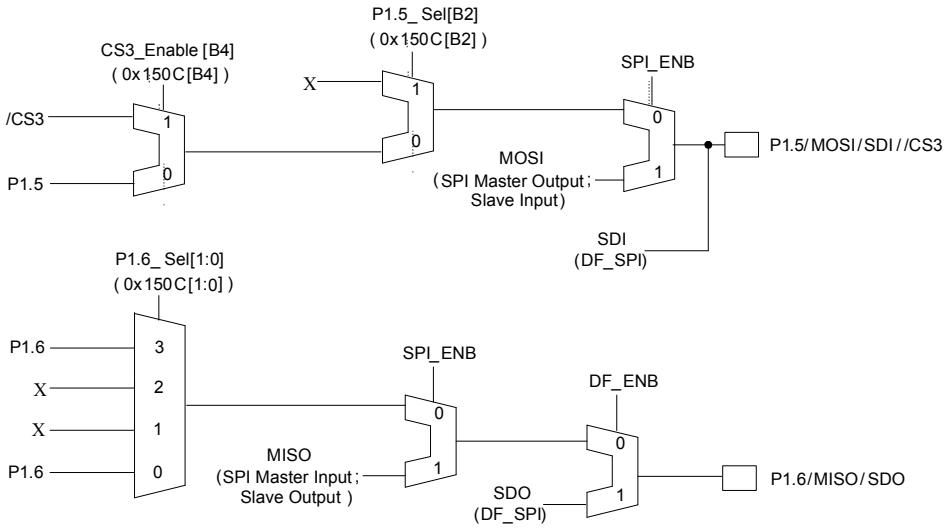
90	VSS_REG	PWR	-	-	PVSSC	Ground of 3.0V linear regulator.
91	VDD_REG	PWR	-	-	PVDDC	3.3V input of 3.0V linear regulator.
92	DVDD1	PWR	-	-	PVDDC	1.9V linear regulator output for internal digital core power supply. Connect a large capacitor (>10uF) for output regulation.
93	DGND1	PWR	-	-	PVSSC	Digital ground 1 (core power ground)
94	PLL_LPF	O	Tristate	Tristate	Panalog	Internal 48MHz PLL charge pump output. Put a passive LPF filter in the pin to ground.
95	VSS_USB	PWR	-	-	PVSSC	USB analog front end ground.
96	USB_DP	Analog I/O	Hi-Z	Hi-Z	PAnalog	USB D+ connection. Series termination resistors (22Ω±1%) are required for impedance of USB bus. The USB Spec1.1 states that the impedance of each driver is required to be between 28 and 44Ω. This chip drive output resistance is 8 to 10Ω. Therefore, the 22Ω±1% series resistors are used.
97	USB_DN	Analog I/O	Hi-Z	Hi-Z	PAnalog	USB D- connection. Series termination resistors (22Ω±1%) are required for impedance of USB bus. The USB Spec1.1 states that the impedance of each driver is required to be between 28 and 44Ω. This chip drive output resistance is 8 to 10Ω. Therefore, the 22Ω±1% series resistors are used.
98	VDD_USB	PWR	-	-	PVDDC	USB analog front end supply power. Full speed devices are identified by pulling D+ to 3.3V±0.3 Volts via a 1.5kΩ±5 % resistor. The baseband chip inside has been built in the 1.5kΩ±20% resistor and the default is disconnected to VDD_USB. The
99	NC	I	Input	Input	PC3D21	No connection
100	SNDR	O	Output L	Output L	PC3B02U	Sounder output - This is a control pin to turn on/off the external transistor, which is used to supply the high peak currents that magnetic sounders typically require.

*** When /CS2 is pull low in the initial power on state. Then the chip will enter into the hardware ISP mode to download the system program code via UART or USB ports.**

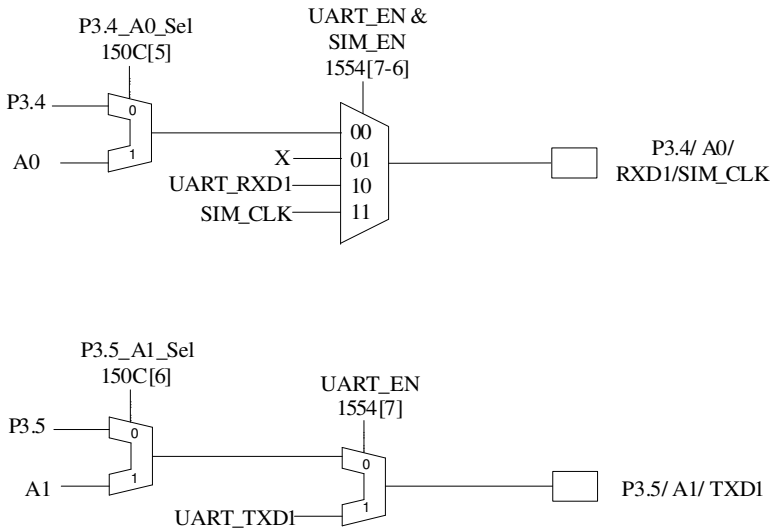
* P1.2;、P1.3 and P1.4 multiple functions：



* P1.5 and P1.6 multiple functions：



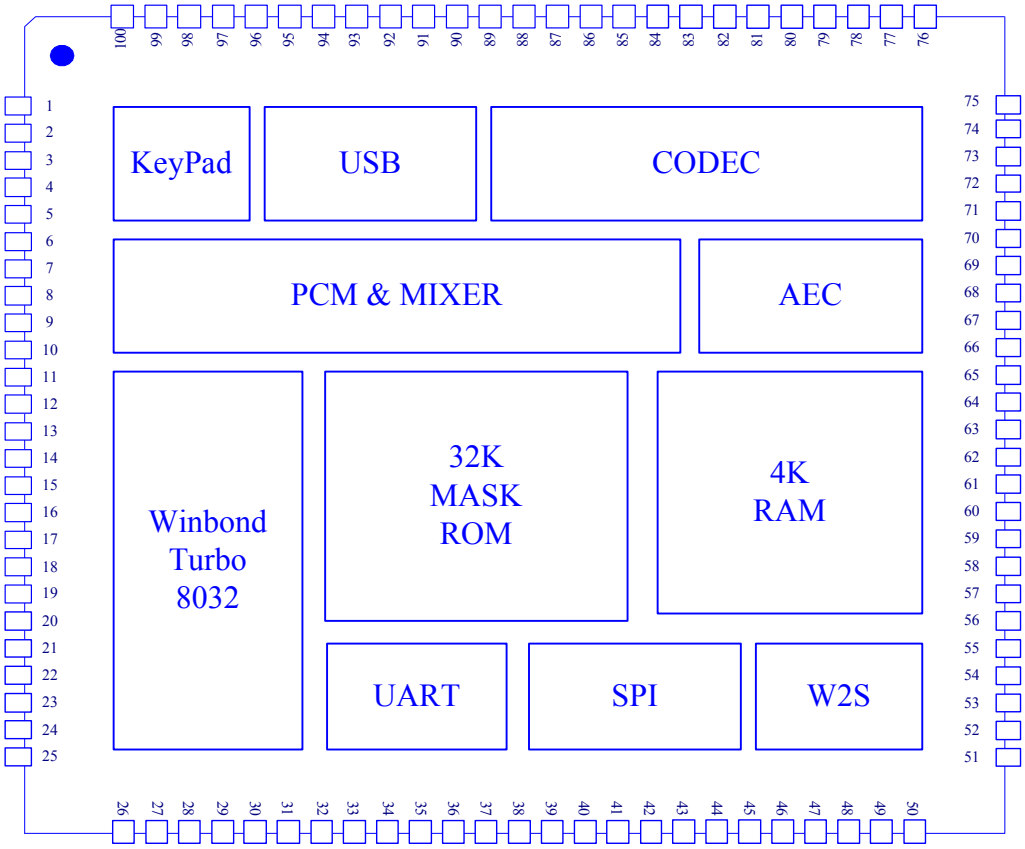
* P3.4 and P3.5 multiple functions：

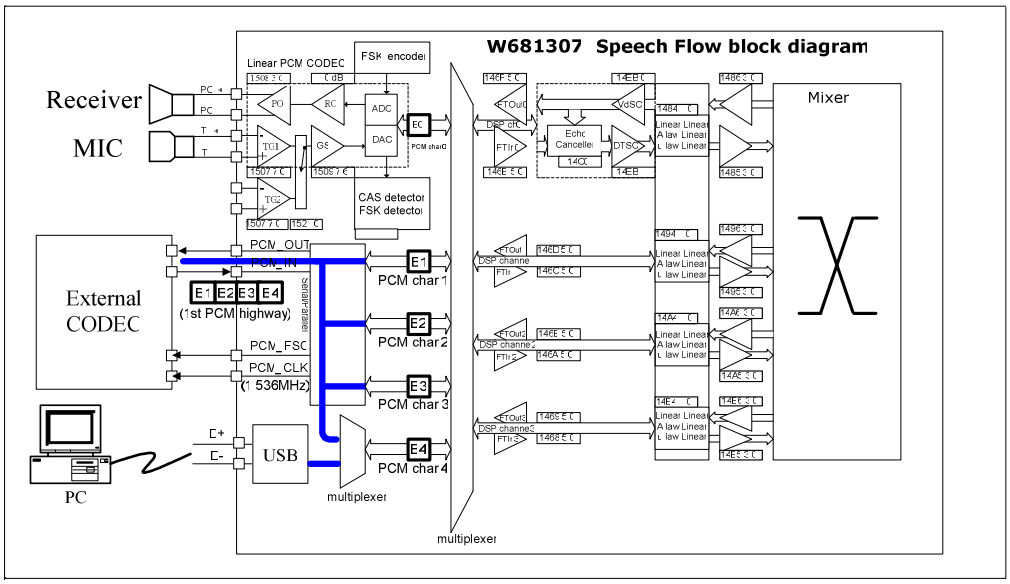


5. SYSTEM DIAGRAM

5.1 Function Block Diagram

The function block diagrams of the MCU chip and speech interface are shown below：





5.2 I/O Cells in Winbond MCU Chip

Chartered Semiconductor (Artisan) 0.25um Integral I/O cell library

PC3B02U
3V CMOS 3-State I/O Pad with Pull-up Resistor, 2mA

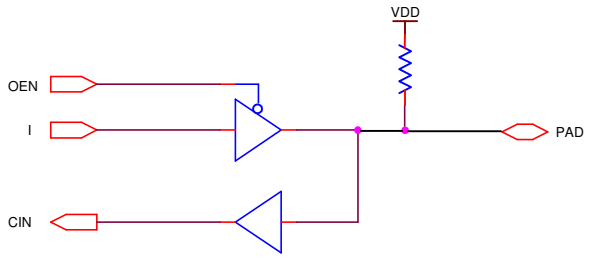


Figure 5-1: PC3B02U pad

PC3B02D
3V CMOS 3-State I/O Pad with Pull-down Resistor, 2mA

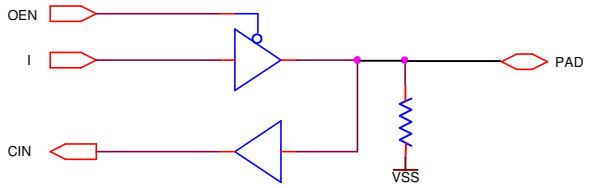


Figure 5-2: PC3B02D pad

PC3o02
3V CMOS Output Pad, 2mA

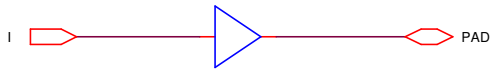


Figure 5-3: PC3o02 pad

PC3D01D
3V CMOS Input only Pad with Pull-down Resistor

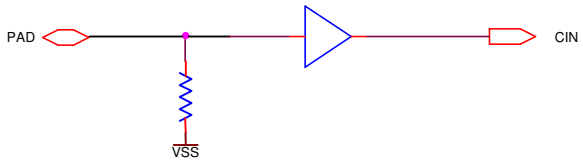


Figure 5-4: PC3D01D pad

PC3D01U
3V CMOS Input only Pad with Pull-up Resistor

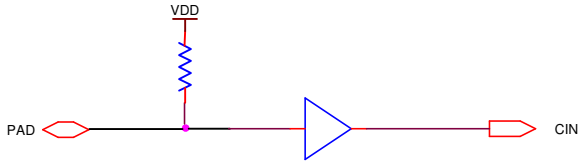


Figure 5-5: PC3D01U pad

PC3D21U
3V CMOS Schmitt non inverting Input only Pad with Pull-up Resistor

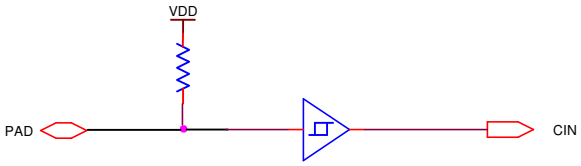


Figure 5-6: PC3D01D pad

PC3T01/02
3V CMOS 3-State Output Pad, 1mA/2mA

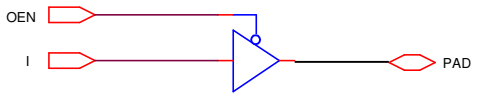


Figure 5-7: PC3T01 pad

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

(Voltage Referenced to AGND pin)

PARAMETER	SYMBOL	RATING	UNIT
Core Power Supply Voltage, pin 53, 92	DVDD	1.9	V
I/O Power Supply Voltage, pin 17, 26, 59	IOVDD	2.7 ~ 3.6	V
Power Supply Voltage , pin 80	AVDD	3.0 ~ 3.6	V
DC Supply Voltage for USB Ouput Stage	VDD_USB	3.0 ~ 3.6	V
Operating Temperature	TOP	-10 to +55	℃
Storage Temperature	TSTG	-85 to +85	℃

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

6.2 DC Characteristics

(AGND = 0 volt TOP = -10 to +55 ℃)

PARAMETER	SYM.	CONDITION	MIN.	TYP.	MAX.	UNIT
Core Operating Current	Icore		-	6	-	mA
I/O Operating Current	II/O		-	6	-	mA
Analog Operating Current	IANA			5		mA
Input High Voltage	VIH	All digital input pins	VDD ×0.7	-	-	V
Input Low Voltage	VIL	All digital input pins	0	-	VDD ×0.3	V
Output High Voltage	VOH	DT, SSP Tx	VDD× 0.75	-	-	V
Output Low Voltage	VOL	DT, SSP Tx	0	-	VDD× 0.25	V
Input High Current	IIL	AGND ≤ Vin ≤ AVDD	-10	-	+10	µA
Input Low Current	IIH	AGND ≤ Vin ≤ AVDD	-10	-	+10	µA
Input Capacitance	CIN	All digital input pins to AGND	-	-	10	pF

6.3 Analog Transmission Characteristics

(AVDD =+3.0V ±5%, AGND = 0 volt , Top = -10 to +55° C ; all analog signal referenced to VAG; 64 Kbps PCM; FST = FSR = 8 KHz; BCLKT = BCLKR = 1.536 MHz; MCLK = 13.824 MHz ; Unless otherwise noted)

6.3.1 Amplitude Response for Analog Transmission Performance

PARAMETER	SYM.	CONDITION	TYP.	A/D		D/A		UNIT
				MIN.	MAX.	MIN.	MAX.	
Absolute Level *	LABS	0 dBm0 = -3.0 dBm @ 600	0.549	---	---	---	---	Vrms
Max. Transmit Level	TXMAX	---	VAG - 1dB	---	---	---	---	Vpk
Frequency Response, Relative to 0 dbm0 @ 1020Hz	GRTV	15 Hz	---	---	---	-60	-0.5	dB
		50 Hz	---	---	---	-40	-0.5	
		100 Hz	---	---	---	-20	-0.5	
		200 Hz	---	---	-3	-5	-0.5	
		300 to 3000 Hz	---	---	-0.20	+0.15	-0.20	
		3300 Hz	---	---	-0.35	+0.15	-0.35	
		3400 Hz	---	---	-0.5	0	-0.5	
		4000 Hz	---	---	---	-12	---	
		4600 to 7000 Hz	---	---	---	-40	---	
Gain Variation vs Level Tone (1020 Hz relative to -10 dBm0)	GLT	+3 to -40 dBm0	---	-0.3	+0.3	-0.2	+0.2	dB
		-40 to -50 dBm0	---	-1.0	+1.0	-0.4	+0.4	
		-50 to -55 dBm0	---	-1.6	+1.6	-0.8	+0.8	

6.3.2 Distortion Characteristics for Analog Transmission Performance

PARAMETER	SYM.	CONDITION	TYP.	TRANSMIT		RECEIVE		UNIT
				MIN.	MAX.	MIN.	MAX.	
Absolute Group Delay	DABS	1600 Hz	---	---	250	---	200	µS
Group Delay Referenced to 1600 Hz	DRTV	500 to 600 Hz	---	---	250	---	30	µS
		600 to 1000 Hz	---	---	200	---	20	
		1000 to 2600 Hz	---	---	70	---	70	
		2600 to 2800 Hz	---	---	100	---	120	
		2800 to 3000 Hz	---	---	145	---	200	
Total Distortion vs. Level Tone (1020 Hz, Mu-Law, C-Message)	DLT	+3 dBm0	---	36	---	34	---	dBC
		0 to -30 dBm0	---	36	---	36	---	
		-40 dBm0	---	29	---	30	---	
		-45 dBm0	---	25	---	25	---	

6.4 Analog Electrical Characteristics

(OP Amplifer TG and VAG; AVDD = +3.0V ±5%, AGND = 0V; Top = -10 to +55° C)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Current of TG		TI1+, TI1- TI2+, TI2-	---	±0.01	±1.0	µA
AC Input Impedance to VAG for TG (1 kHz)	R_{TIIN}	TI1+, TI1- TI2+, TI2-	---	1.0		M
Input Capacitance of TG	C_{TIIN}	TI1+, TI1- TI2+, TI2-	---	---		pF
Input Offset voltage of TG	V_{OFIN}	TI1+, TI1- TI2+, TI2-	---	---	25	mV
Input Common Mode Voltage of TG	V_{CMV}	TI1+, TI1- TI2+, TI2-	0.5	---	AVDD–0.8	V
Input Common Mode Rejection Ratio of TG		TI1+, TI1- TI2+, TI2-		60	100	dB
Gain Bandwidth Product of (10kHz) $R_{load} \geq 10$ K		TI1+, TI1- TI2+, TI2-		975		KHz
DC Open Loop Gain of TG $R_{load} \geq 10$ K		TI1+, TI1- TI2+, TI2-	80	95		dB
Bandgap voltage	V_{BGAP}	Ref to AGND		1.0		V
VAG Output Voltage	V_{VAG}	Ref to AGND		1.5		V
VAG Output Current with less than 50 mV change in output voltage	I_{VAG}	V_{VAG} . 50mV		1		mA
Power Supply Rejection Ratio	PSRR	TG	---	55	---	dB

6.5 Power Drivers – PO1, 2

(AVDD = +3.0V ±5%, AGND = 0V; Top = -10 to +55° C)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Offset Voltage of PO1+ (PO2+) relative to PO1-(PO2-)		Inverted Unity Gain for PO-			30	mV
PO1+(PO2+), PO1-(PO2-) Output Current @ VAG=1.5V, R_L=120, THD<1%		VAG-0.7 V ≤ PO+ ,PO- ≤ VAG+0.7 V		6		mA
PO1+(PO2+), PO1-(PO2-) Output Resistance		Inverted Unity Gain for PO-		10		Ω
Gain Bandwidth Product @ 10 kHz		Open Loop for PO-		433		kHz
Load Capacitance for PO	C_{LAP}	PO- to PO+	---	---	300	pF
Gain of PO1+(PO2+) relative to PO1-(PO2-)				0	0.2	dB
Load Resistance differentially for PO1	R_{LDAP}	PO1- to PO1+	---	120	---	Ω
Load Resistance differentially for PO2	R_{LDAP}	PO2- to PO2+	---	16	---	Ω

6.6 Programmable Output Linear Regulator

Linear Regulator 1 (REG1) T = 25°C, External Transistor PNP: BC807-25

PARAMETERS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current Consumption during Operation	Idle,		50		uA
Current Consumption during Power off			1		nA
Drop Out Voltage	Iout= 100mA		0.3		V
Input Voltage		3.3		3.6	V
Programmable Output Voltage Range	Iout= 100mA	3.0		3.3	V
Maximum Output Current (PNP)	The characteristics vary with the associated external components (PNP).		250		mA
Load Regulation (PNP)	Vin= 3.3V, Vout=3.0V, Iout= 100mA		50		mV
Line Regulation (PNP)	Vin=3.3V...3.6V, Vout=3.0V, Iout= 100mA		50		dB
REG_CTRL Sink Current	Vin=3.3V, Vout=3.0V*0.95		Tbf		mA
REG_CTRL leakage Current during Power Off	Vin= 3.3V, Vout= tristate			0.1	uA

6.7 USB PHY Electronic Characteristics (25°C, VDD_USB = 3.3V, DVDD1, 3 =1.9V)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage for USB Ouput Stage	VDD_USB		3.0	3.3	3.6	V
Input Voltage Range for USB_DP/DN	USB_DP USB_DN		0	VDD_USB	3.6	V
Input High	V_{IH}		2.0			V
Input Low	V_{IL}				0.8	V
Differential Input Sensitivity	V_{DI}		0.2			V
Differential Common-mode Range	V_{CM}		0.8	---	2.5	V
Single-end Receiver threshold	V_{SE}		0.8		2.0	V
Output Low	V_{OL}				0.3	V
Output High	V_{OH}		2.8			V
Output signal cross Voltage	V_{CRV}		1.3		2.0	V
Pull-up Resistor	R_{UP}		1.2	1.5	1.8	KΩ
Driver Output Resistance	Z_{DRV}		8		12	Ω
Transceiver Capacitance	C_{IN}				20	pF
Driver Rise Time	T_R	C_L = 50pF	4	8	15	ns

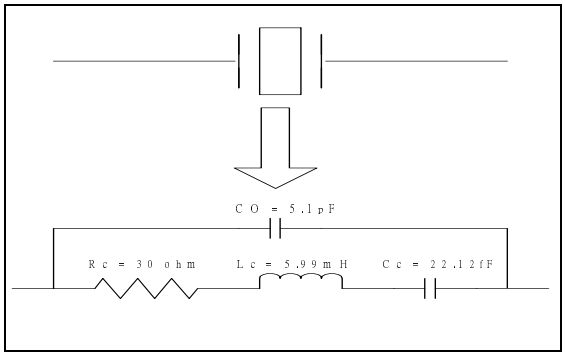
Driver Fall Time	T_F		4	8	15	ns
Rise and Fall Time Matching	T_{LRLF}	$T_{LRLF} = T_{LR}/ T_{LF}$	90	100	111	%
VDD_USB Supply Current * (exclude internal pull high resistor)	I_{USB}	Standby			10	nA
		Input Mode			2	mA
		Output Mode			2	mA

6.8 USB PLL Electronic Characteristics (25°C, AVDD = 3.3V, DVDD1, 3 =1.9V)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operation Current	I_{PLL}	VCO_{FREQ} = 96MHz, $FOUT_{FREQ}$ = 48MHz				mA
PLL Shut-Down Current	I_{PLL_DN}					uA
Operation Voltage	V_{PLL}		3.0	3.3	3.6	V
Input Clock Frequency Range	F_{IN}			13.824		MHz
Comparison Frequency	F_{REF}			768		KHz
PLL Output Frequency	F_{OUT}			48		MHz
VCO Frequency	F_{VCO}		---	96	---	MHz
Ouput Duty Cycle			40	50	60	%
PLL Short-Term Peak To Peak Output Jitter	T_{JITTER}					ps
PLL Lock In Time	T_{READY}					ms

6.9 The Crystal Specification Requirement

The below figure is shown the electrical equivalent circuit for a crystal and the parameters are used for the crystal circuit.



6.10 Recommended Crystal Specification

The following crystal specifications are recommended for a proper cooperation between the crystal and baseband crystal oscillator. Correct coordination guarantees great reliability and low failure rates in production.

Parameter	Limit values			Unit	Condition
	Min.	Type.	Max.		
Frequency		13.824		MHz	Fundamental mode
Tolerance of center frequency	-10		+10	ppm	25°C ±3°C
Tolerance over operation range	-5		+5	ppm	0°C to 55°C
Crystal current					
Load capacitance		18		pF	
Dynamic capacitance Cc		22.12		fF	
Resonance resistance Rc		40		Ω	
Electrostatic capacitance		5.1		pF	
Aging			±3	ppm/year	

7. MEMORY AND REGISTER MAP

7.1 Program Memory Map

Program area memory is mapped from 0x0000 to 0xFFFF, this can be used by external ROM.

7.2 Data Memory Map

Data memory address	Size	Function	Comment
0x0000 - 0x0FFF	(4KB)	Not allocated	
0x1000 - 0x143F (except for 0x1401 and 0x1420)	(1KB)	Blocked for test modes (0x1401 and 0x1420 are activation registers)	
0x1440 - 0x144F	(16B)	Support Logic	
0x1450 - 0x145F	(16B)	Interface Logic	
0x1460 - 0x1466	(07B)	Speech interface	
0x1467	(01B)	Multiplexer to connect 5 PCM channels to 4 DSP channels	
0x1468 - 0x146F	(15B)	Fine tune gain	
0x1470 - 0x1474, 0x150C (0x1475 ~ 0x147F: To Be Defined)	(06B)	Processor Interface (AuxOpPort,DiagSel,Diag_CS,Diag_CS3,Multiplier_enable)	
0x1480 - 0x14BF (0x1487, 0x1497, 0x149D ~ 0x149F, 0x14A7, 0x14AD ~ 0x14AE, 0x14B7, 0x14BD ~ 0x14BF: To Be Defined)	(52B)	Transcoder DSP Registers	
0x14C0 - 0x14FF (0x14FA~ 0x14FF: To Be Defined)	(58B)	Half Acoustic Echo Canceller Registers	
0x1500 - 0x151F (0x1516 ~ 0x1517, 0x1519, 0x151B ~ 0x151F: To Be Defined)	(24B)	MCU System Register	
0x1520 - 0x157F (except for 0x1521)	(96B)	Blocked for test modes (0x1521 is TI path selection register)	
0x1580 - 0x15BF	(64B)	(Reserved)	
0x15C0 - 0x15CF (0x15C7, 0x15CF: To Be Defined)	(14B)	Acoustic side / Network side Power Measurement	
0x15D0 - 0x16FF	(304B)	(Reserved)	
0x1700 – 0x171F (0x1705 ~ 0x1707, 0x170D ~ 0x170F, 0x1711 ~ 0x171F: To Be Defined)	(11B)	PCM highway	
0x1720 – 0x1728 0x1729 ~ 0x172F: To Be Defined)	(9B)	Master or slave SPI interface	
0x1730 ~ 0x173F	(16B)	Data Flash SPI interface	
0x1740 – 0x175F (0x174B ~ 0x175F: To Be Defined)	(11B)	W2S interface	
0x1760 – 0x177B (0x1764: To Be Defined)	(27B)	Blocked for test modes	
0x1800 ~ 0x187F	(127)	USB control registers	
0x1900 ~ 0x1901	(2B)	ISP mode control register	
0x5000 - 0x6FFF	(8KB)	Reserved for On-chip Expansion	
0x7000 - 0x7FFF	(4KB)	On chip data RAM	*4
0x8000 - 0xEFFF	(4-28KB)	External data RAM programmable selected by CS1	*2
0xF000 - 0xFFFF	(4KB)	External data RAM selected by CS2	*3

*1. Specific registers are blocked for test modes of hardware logic functions.
*2. The On-chip RAM is contiguous with CS1, which is used for off chip RAM.CS2 is the same.
*3. CS1 is a programmable address range, CS1 can be programmable range starting at 0x8000 and ending at 0xEFFF, with step 4K. CS2 is the same.
*4. In the event of further on chip RAM being required this can be put in this reserved location, hence on-chip and off chip RAM will remain contiguous. The address decoding logic in this chip will not decode this area.

7.3 Register Map

7.3.1 Mixer and Speech Logic Registers Overview

Address	Name	Mode	Value At Reset	Function
0x1401	Mixer_En	R/W	0x00	Enable the mixer block.
0x1420	SPEECH LOGIC_EN	R/W	0x04	Enable the four channels of speech logic interface (which is not needed by the CODEC).

(0x1000 ~ 0x143F are blocked for test modes except for 0x1401 and 0x1420)

7.3.2 Support Logic Registers Overview

Address	Name	Mode	Value At Reset	Function
0x1440	ClockEnable	R/W	0x78	Clock 3, 4 & 5 Enable Bits and Reset 32K logic
0x1441	IntrptSource0	R/W	0x00	Interrupt source register 0
0x1442	IntrptSource1	R/W	0x00	Interrupt source register 1
0x1443	IntrptEnable0	R/W	0x00	Interrupt enable register 0
0x1444	IntrptEnable1	R/W	0x00	Interrupt enable register 1
0x1445	IntrptPriority0	R/W	0x00	Interrupt priority register 0
0x1446	IntrptPriority1	R/W	0x00	Interrupt priority register 1
0x1447	SounderTone1	R/W	0x00	Sounder frequency control register 1
0x1448	SounderTone2	R/W	0x00	Sounder frequency control register 2
0x1449	SounderVol1	R/W	0x00	Sounder volume control register 1
0x144A	SounderVol2	R/W	0x00	Sounder volume control register 2
0x144B	PIEZO Function	R/W	0x00	PIEZO Enable and frequency select
0x144C	PIEZO Clock output	R/W	0x00	Output the PIEZO driving clock
0x144D	IntrptSource2	R/W	0x00	Interrupt source register 2
0x144E	IntrptEnable2	R/W	0x00	Interrupt enable register 2
0x144F	IntrptPriority2	R/W	0x00	Interrupt priority register 2

7.3.3 Interface Logic Registers Overview

Address	Name	Mode	Value At Reset	Function
0x1450	KeyIoDR	R/W	0x1F	- Row Keys IO Port Direction Control & Wake up enable
0x1451	KeyIoDC	R/W	0x1F	Col Keys IO Port Direction Control
0x1452	KeyIoIpR		Undefined	Row Keys IO Port Input Data Register
0x1453	KeyIoIpC		Undefined	Col Keys IO Port Input Data Register
0x1454	KeyIoOpR		Undefined	Row Keys IO Port Output Data Register
0x1455	KeyIoOpC		Undefined	Col Keys IO Port Output Data Register
0x1456	KeyIoMskR	R/W	0x00	Row keys IO Port Control Register for Mask
0x1457	KeyIoMskC	R/W	0x00	Col keys IO Port Control Register for Mask
0x1458	KeyLocation	R	0x00	Gives the Row and Column numbers of the last detected key press
0x1459	KeyPadSize	R/W	0x00	Sets the size of the Keypad scanned by the Keypad Scanner function
0x145A	Watch Dog Control	R/W	0x00	Control watchdog and keypad bounce
0x145B	Timer 1ms Control1	R/W	0x00	Control the 1ms Timer
0x145C	Timer Control	R/W	0x00	Reset the 1ms, 1S, 1min Timer
0x145D	1S Counter	R/W	0x00	Second counter 0-59
0x145E	Watch Dog Kick	R/W	0x00	Reset the watchdog
0x145F	1mS Counter	R	0x00	1ms counter, reset, enable bit and counter value

7.3.4 Speech Interface Registers Overview

Address	Name	Mode	Value At Reset	Function
0x1460	Speech Control 0	R/W	0x00	Configuration Register for PCM interface
0x1461	Specific Register	R/W	0x00	Blocked for test modes
0x1462	Speech IO Direction	R/W	0x00	Speech I/O interface direction control
0x1463	Speech IO Input Data	R/W	0x00	Speech I/O port input data
0x1464	Speech IO Output Data	R/W	0x00	Speech I/O port Output data
0x1465	Speech IO Mask	R/W	0x00	Speech I/O port control register for mask
0x1466	Fsync counter	R/W	0x00	Frame sync counter within the speech interface
0x1467	Multiplexer control register	R/W	0x00	Multiplexer to connect 5 PCM channels to 4 DSP channels
0x1468	FTInGain3	R/W	0x00	Fine tune gain input stage
0x1469	FTOutGain3	R/W	0x00	Fine tune gain output stage
0x146A	FTInGain2	R/W	0x00	Fine tune gain input stage
0x146B	FTOutGain2	R/W	0x00	Fine tune gain output stage
0x146C	FTInGain1	R/W	0x00	Fine tune gain input stage
0x146D	FTOutGain1	R/W	0x00	Fine tune gain output stage
0x146E	FTInGain0	R/W	0x00	Fine tune gain input stage
0x146F	FTOutGain0	R/W	0x00	Fine tune gain output stage

7.3.5 Processor Interface Registers Overview

Address	Name	Mode	Value At Reset	Function
0x1470	AuxOpPort	R/W	0x00	Chip selects or output ports
0x1471	Reserved			
0x1472	Diag_CS	R/W	0x00	Chip selects or output ports
0x1473	Diag_CS3	R/W	0x00	Chip selects or output ports
0x1474	Mutiplier_enable	R/W	0x00	Fast 8x8 multiplier in T8032
0x1475-0x147F	Reserved			

7.3.6 Transcoder DSP Registers Overview

Address	Name	Mode	Value At Reset	Function
0x1480	Connect0	R/W	0x00	Specify mixing among four PCM channels
0x1481-0x1483	Specified Register	R/W	0x00	Blocked for test modes
0x1484	PCMmode0	R/W	0x00	Select between 14-bit linear, A-law and µ-law mode
0x1485	InputGain0	R/W	0x00	PCM input gain
0x1486	OutputGain0	R/W	0x00	PCM output gain
0x1487	RESERVED			
0x1488	ToneFreqA0	R/W	0x00	Set frequency of tone A
0x1489	ToneFreqB0	R/W	0x00	Set frequency of tone B
0x148A	ToneVolA0	R/W	0x00	Set level of tone A
0x148B	ToneVolB0	R/W	0x00	Set level of tone B
0x148C	ToneEna0	R/W	0x00	Enable addition of tones
0x148D	SideTone	R/W	0x00	Set sidetone gain
0x148E	Lookback_EN	R/W	0x00	Test facilities for Transcoder DSP
0x148F	Specified Register	R/W	0x00	Blocked for test modes
0x1490-0x149C	Connect1 ~ ToneEna1	R/W	0x00	The functions are the same as channel 0
0x149D–0x149F	RESERVED			
0x14A0-0x14AC	Connect2 ~ ToneEna2	R/W	0x00	The functions are the same as channel 0
0x14AD–0x14AE	RESERVED			
0x14AF	SideToneChannel_Ena	R/W	0x01	Side tone enables for each active PCM channel
0x14B0-0x14BC	Connect3 ~ ToneEna3	R/W	0x00	The functions are the same as channel 0
0x14BD–0x14BF	RESERVED			

7.3.7 Echo Canceller Registers Overview

Address	Name	Mode	Value At Reset	Function
0x14C0	UP_CONFIG	R/W	0x00	Configuration for the echo cancellation unit
0x14C1	UP_RESET	R/W	0x08	Enables the three buffers used by the echo cancellation FIR filter
0x14C2	EC_BELTA	R/W	0x03	The echo cancellation update gain
0x14C3	Specific Register	R/W	0x03	Blocked for test modes
0x14C4	LS_BUILD_UP_TIME	R/W	0x07	Controls acoustic suppression factor convergence towards target
0x14C5-0x14C6	LS_MAX_ATTEN	R/W	0x1CA8	Maximum attenuation value that will be utilised by the acoustic suppression algorithm
0x14C7-0x14C8	LS_MIN_ATTEN	R/W	0xFFFF	Minimum attenuation value that will be utilised by the acoustic suppression algorithm
0x14C9	DT_LONG_ACOUSTIC_ATTACK_TC	R/W	0x09	Attack time for long term acoustic power estimation
0x14CA	DT_SHORT_ACOUSTIC_ATTACK_TC	R/W	0x0B	Attack time for short term acoustic power estimation
0x14CB-0x14CC	DT_ACOUSTIC_HANGOVER_TIME	R/W	0x0020	Define the inertial delay of the double talk detection algorithm for acoustic side
0x14CD-0x14CE	DT_ACOUSTIC_DEV_THRESHOLD	R/W	0x0666	Define the instantaneous acoustic power change
0x14CF-0x14D0	DT_SHORT_ACOUSTIC_THRESHOLD	R/W	0x0404	Define the power threshold
0x14D1	VD_LONG_NETWORK_ATTACK_TC	R/W	0x09	Attack time for long term network power estimation
0x14D2	VD_SHORT_NETWORK_ATTACK_TC	R/W	0x0B	Attack time for short term network power estimation
0x14D3-0x14D4	VD_NETWORK_HANGOVER_TIME	R/W	0x0009	Define the inertial delay of the voice detection algorithm for the network side
0x14D5-0x14D6	VD_NETWORK_DEV_THRESHOLD	R/W	0x0666	Define the instantaneous network power change
0x14D7-0x14D8	VD_LONG_NETWORK_THRESHOLD	R/W	0x0666	Minimum power level that constitutes speech over the network interface, as measured by the long term power estimation algorithm
0x14D9-0x14DA	VD_SHORT_NETWORK_THRESHOLD	R/W	0x040E	Minimum power level that constitutes speech over the network interface, as measured by the short term power estimation algorithm
0x14DB-0x14DC	VD_CUT_OFF_NETWORK_POWER	R/W	0x0666	Configurable bias for network power estimation
0x14DD	Specific Register	R/W	0x00	Blocked for test modes
0x14DE	ACOUSTIC / NETWORK Active Status	R	0x00	Acoustic side and Network side active status
0x14DF-0x14E0	AGC_THRESHOLD	R/W	0x0800	The AGC threshold is set the maximum output power from AGC module
0x14E1-0x14E2	AGC_NOISE_THRESHOLD	R/W	0x00C8	The calculated input power is compared with the AGC_NOISE_THRESHOLD
0x14E3	AGC_MAX_SG	R/W	0x02	The AGC module has maximum gain to amplifier the echo cancelled input signal
0x14E4	Specific Register	R/W	0x0F	Blocked for test modes
0x14E5	AGC_LG_ATTACK_TC	R/W	0x0B	The field defines the inertial delay utilized for the long term gain estimation
0x14E6	AGC_ST_ATTACK_TC	R/W	0x09	Attack time for short term AGC power estimation
0x14E7	NS_STTACK_Tcand_GAIN	R/W	0x00	Set Noise_Suppressor_Index and ShortTermPowerTC
0x14E8	NS_ATTEN_DW_UP_TC	R/W	0x00	Set Noise_rise_TC and Noise_fall_TC
0x14E9	NS_Active_Power_MSB	R/W	0x00	Set noise threshold
0x14EA	NS_Active_Power_LSB	R/W	0x00	Set noise threshold

7.3.8 Soft Clip Registers Overview

Address	Name	Mode	Value At Reset	Function
0x14EB	Soft Clip Control	R/W	0x00	Enable the soft clipping function
0x14EC	VD Soft Clip Normal Index	R/W	0x00	Control the gain of VD soft clip module at normal mode
0x14ED	VD Soft Clip Low Index	R/W	0x00	Control the gain of VD soft clip module at low mode
0x14EE 0x14EF	VD SC Threshold	R/W	0x0400	Determine the selection of Soft Clip gain
0x14F0	ShortTermPreNetworkPowerAttackTC	R/W	0x07	Time constant use to calculate the short term network power for VD soft clip
0x14F1	VDSC Attack TC	R/W	0x07	Smooth the gain change
0x14F2	DT Soft Clip Normal Index	R/W	0x00	Control the gain of DT soft clip module at normal mode
0x14F3	DT Soft Clip Low Index	R/W	0x00	Control the gain of DT soft-clip module at low mode
0x14F4 0x14F5	DT SC Threshold	R/W	0x0400	Determine the selection of Soft Clip gain
0x14F6	ShortTermPostAcousticPower AttackTC	R/W	0x07	Time constant use to calculate the short term acoustic power for DT soft clip
0x14F7	DTSC Attack TC	R/W	0x07	Smoothing function, smooth the gain change

7.3.9 CODEC Digital Part

Address	Name	Mode	Value At Reset	Function
0x1500	CODEC_OnOff_Scheme	R/W	0x00	Hardware scheme to arrange the procedure and timing for CODEC_digital_disable and CODEC_analog_disable
0x1501	CODEC Digital Part	R/W	0x80	Reset CODEC FIFO value or reset CODEC FIFO point
0x1502	CODEC ADC ABF PROB	R/W	0xFF	Adaptive bit flip probability of the ADC path in the CODEC modulator

7.3.10 Sounder Path Select

Address	Name	Mode	Value At Reset	Function
0x1503	Sounder path	R/W	0x00	Sounder signal select PDM or PWMnd reference clock generation for external melody chip

7.3.11 Frequency Adjustment of Crystal Oscillator

Address	Name	Mode	Value At Reset	Function
0x1504	FACO	R/W	0x00	Select the on-chip capacitance connected to XTAL1 and XTAL2 respectively

7.3.12 Specific Register

Address	Name	Mode	Value At Reset	Function
0x1505	Specific Register	R/W	0x00	Blocked for test modes

7.3.13 VAG Selection

Address	Name	Mode	Value At Reset	Function
0x1506	VAG Selection	R/W	0x00	Select the reference voltage at pin VAG.

7.3.14 CODEC Control Register Overview

Address	Name	Mode	Value At Reset	Function
0x1507	TG1 Gain Register	R/W	0x00	Set TG1 gain from 0dB, 6dB, 12dB, 18dB to 24dB or bypass and doublt you selected gain. TG2 internal gain.
0x1508	PO Gain Register	R/W	0x00	Set PO gain from -4dB, 2dB, 8dB or bypass
0x1509	CODEC_CTRL	R/W	0x00	OP amp PO power down, CODEC analog loopback, CODEC transmitter gain

7.3.15 Specific Registers

Address	Name	Mode	Value At Reset	Function
0x150A	Specific Register	R/W	0x00	Blocked for test modes
0x150B	Specific Register	R/W	0x00	Blocked for test modes

7.3.16 Test Cases and Debugging Registers Overview

Address	Name	Mode	Value At Reset	Function
0x150C	RECEIVE_DIAG	R/W	0x00	Register for diagnostic and output pins switch
0x150D	Specific Register	R/W	0x00	Blocked for test modes
0x150E	EnAllClock	R/W	0x00	Enable all of test clock
0x150F	CODEC_Test_Sel	R/W	0x00	Digital CODEC part test mode selection
0x1510	RSSI Mode	R/W	0x00	Use for ISP mode protect
0x1511	BGP_LPF_EN	R/W	0x00	Enable the low pass filter at the BGP generator
0x1512	CODEC Status Indicator	R/W	0x00	CODEC DAC ADC FIFO point indicator
0x1513	Bandgap Voltage Adjustment	R/W	0x00	Bandgap Voltage Adjustment
0x1514	Specific Register	R/W	0x00	Blocked for test modes
0x1515	Linear Regulator Voltage Controller Register	R/W	0x00	The adjustment possibilities of output voltage of the linear regulator have been built in to compensate the bandgap variation in process.
0x1516-0x1517	Reserved			

7.3.17 Charge Park Detection

Address	Name	Mode	Value At Reset	Function
0x1518	Core PWR_Det	R	0x00	Monitor core power voltage

7.3.18 DA High Pass Filter Selection

Address	Name	Mode	Value At Reset	Function
0x151A	DA High Pass Filter Selection	R/W	0x00	Codec D/A high pass filter control register

7.3.19 TI PATH Selection

Address	Name	Mode	Value At Reset	Function
0x1521	TI Path Selection	R/W	0x00	Choose the signal to be processed in off-hook or on-hook signalling

(0x1520 ~ 0x157F are bloked for test modes except for 0x1521)

7.3.20 Network side / Acoustic side Power Measurement

Address	Name	Mode	Value At Reset	Function
0x15C0~ 0x15C1	ACOUSTIC_SHORT_TERM_ POWER	R	0x0000	Short Term Acoustic Power calculated by the double talk detector (DT)
0x15C2~ 0x15C3	ACOUSTIC_LONG_TERM_ POWER	R	0x0000	Long Term Power on Acoustic estimated by the double talk detector (DT)
0x15C4~ 0x15C5	ACOUSTIC_POWER_DEVI ATION	R	0x0000	Acoustic Power Deviation estimated by the double talk detector (DT)
0x15C6	ACOUSTIC / NETWORK Active Status	R	0x00	Acoustic and Network active status
0x15C7	Reserved			
0x15C8~ 0x15C9	NETWORK_SHORT_TERM_ POWER	R	0x0000	Short Term Network Power calculated by the voice detector (VD)
0x15CA~ 0x15CB	NETWORK_LONG_TERM_ POWER	R	0x0000	Long Term Power on Network estimated by the voice detector (VD)
0x15CC~ 0x15CD	NETWORK_POWER_DEVI ATION	R	0x0000	Network Power Deviation estimated by the voice detector (VD)
0x15CE	ACOUSTIC / NETWORK Active Status	R	0x00	Acoustic and Network active status

7.3.21 PCM Highway Channel Registers Overview

Address	Name	Mode	Value At Reset	Function
0x1700	PCM channel format and delay control of 1st group	R/W	0x02	PCM channel format and delay control of 1st group in the 1st PCM Highway
0x1701	TX delay1	R/W	0x00	Set the values for delaying the transmitted bits of PCM channel1 after the rising edge of the Fsync.
0x1702	TX delay2	R/W	0x00	Set the values for delaying the transmitted bits of PCM channel2 after the tail bit of PCM channel 1.
0x1703	RX delay1	R/W	0x00	Set the values for delaying the received bits of PCM channel1 after the rising edge of the Fsync.
0x1704	RX delay2	R/W	0x00	Set the values for delaying the received bits of PCM channel2 after the tail bit of RX PCM channel 1.
0x1705~ 0x1707	Reserved			
0x1708	PCM channel format and delay control of 2nd group	R/W	0x02	PCM channel format and delay control of 2nd group in the 1st PCM Highway
0x1709	TX delay3	R/W	0x00	Set the values for delaying the transmitted bits of PCM channel3 after the tail bit of PCM channel 2.
0x170A	TX delay4	R/W	0x00	Set the values for delaying the transmitted bits of PCM channel4 after the tail bit of PCM channel 3.
0x170B	RX delay3	R/W	0x00	Set the values for delaying the received bits of PCM channel3 after the tail bit of RX PCM channel 2.
0x170C	RX delay4	R/W	0x00	Set the values for delaying the received bits of PCM channel4 after the tail bit of RX PCM channel 3.
0x170D~ 0x170F	Reserved			
0x1710	PCM channel format control of 2nd PCM highway	R/W	0x02	PCM channel format control of the 2nd PCM highway.

7.3.22 SPI Interface Registers Overview

Address	Name	Mode	Value At Reset	Function
0x1720	SPI_control0	R/W	0x00	Setting SPI interface control register.
0x1721	SPI_control1	R/W	0x00	Setting SPI interface control register.
0x1722	SPI Status	R	0x00	Read the SPI Status.
0x1723	SPI Interrupt Enable	R/W	0x00	Enable SPI interrupt.
0x1724	DumpByte	R	0x00	Show the received byte when 1720[3] is set.
0x1725	Write TX FIFO	W	0x00	Store data in SPI TX-FIFO when micro controller writes data to this register.
0x1726	Read RX FIFO	R	0x00	Read data from SPI RX-FIFO when micro controller read data from this register.
0x1727	SPI_transfer_size	R/W	0x00	Setting the transfer size when Tx and Rx.
0x1728	SPI_start_rtx	R/W	0x00	Start to transmit at the rate of transfer size when Tx and Rx.

7.3.23 Data Flash SPI Interface Registers Overview

Address	Name	Mode	Value At Reset	Function
0x1730	DF_CLK	R/W	0x00	Setting data flash SPI interface enable and clock rate.
0x1731	DF_CMD_LEN	R/W	0x00	Setting data flash SPI interface command length control register.
0x1732	DF_DATA_LEN	RW	0x00	Setting data flash SPI interface data length control register.
0x1733	DF_INTR_REG	R/W	0x00	Enable data flash SPI interrupt.
0x1734 ~ 0x1738	DF_CMD_B1 ~ DF_CMD B5	RW	0x00	Setting data flash SPI interface command contact register.
0x173B	DF_CLK_FORMAT	RW	0x00	Setting the data flash SPI interface format.
0x173C	DF_FIFO_DATA	RW	0x00	Read/write the data from the data flash SPI interface FIFO.
0x173D	DF_CNT	R	0x00	Current the data flash SPI interface FIFO counter value.
0x173E	DF_WR_CNT	R/W	0x00	CPU current Write-point for the data flash SPI interface FIFO.
0x173F	DF_RD_CNT	R/W	00	CPU current Read-point for the data flash SPI interface FIFO.

7.3.24 W2S Interface Registers Overview

Address	Name	Mode	Value At Reset	Function
0x1740	W2S_Enable	R/W	0x00	Enable W2S interface.
0x1741	EEPROM_Config	R/W	0x00	Setting the page mode of EEPROM.
0x1742	Prescale_Lo	R/W	0x00	Control W2S bus speed.
0x1743	Prescale_Hi	R/W	0x00	Control W2S bus speed.
0x1744	RdWrFIFO	R/W	0x00	Read /Write data into TX FIFO.
0x1745	Force_Activity	R/W	0x00	Force activities of W2S.
0x1746	W2S_Status	R	0x00	Read W2S status.
0x1747	FIFORdPtr	R	0x00	Monitor W2S FIFO read pointer.
0x1748	FIFOWrPtr	R	0x00	Monitor W2S FIFO write pointer.
0x1749	ForceAckFail	R/W	0x00	Enable Ack Fail Event.
0x174A	W2S_Misc	R	0x00	Monitor current finite state and interrupt indication.

7.3.25 USB Control Registers Overview

Address	Name	Mode	Value At Reset	Function
0x1800	USB Enable Register	R/W	00	USB 1.1 function enables control register.
0x1801~ 0x1803	USB Interrupt Register A. Enable, status and clear	R/W	00	USB endpoints interrupt enable, status and clear.
0x1804 ~ 0x1806	USB Interrupt Register B. Enable, status and clear	R/W	00	USB endpoints interrupt enable, status and clear.
0x1810	EndPoint 0 – Control In/Out Registers	R/W	00	Control in/out Endpoint control register.
0x1811	Control In Data	R/W	00	Control in Endpont Data. Internal FIFO has 8 bytes for Control In transmission.
0x1820 ~ 0x1827	Control HID Out Data	R	00	Control HID out receiving data.
0x1828 ~ 0x182F	Control Out Data	R	00	Control Out Endpoint receiving data.
0x1830	EndPoint 1 and 2 – ISO In/Out Registers	R/W	00	ISO In/Out Endpoint control register.
0x1839 ~ 0x1847	ISO SYNC Speed Register	R/W	xx	ISO SYNC fine-tuning speed parameter register.
0x1848	EndPoint 3 – Bulk In Registers-- Control Register	R/W	00	Bulk In Endpoint control register
0x1849	Bulk In Data	W	00	Bulk_In transmission data register except final data.
0x184A	Bulk In Final Data	W	00	Bulk_In transmission final data register.
0x184B	Bulk In FIFO Empty Flag	R	00	Bulk_In transmission FIFO data empty flag.
0x1850	EndPoint 4 – Bulk Out Registers--- Control Register	R/W	00	Bulk Out Endpoint control register
0x1851	Bulk Out FIFO Length	R	00	Shown Bulk Out Endpoint receiving FIFO data length.
0x1852	Bulk Out Data	R	00	Bulk Out Endpoint receiving FIFO data.
0x1858	EndPoint 5 – Interrupt In Registers--- Control Register	R/W	00	Interrupt In Endpoint control register
0x1859	USB Interrupt Data Length	R/W	00	Interrupt In Endpoint transmission data length
0x1860~0x 186F	Interrupt In Data	R/W	00	Total 16 bytes Interrupt In transmission data registers.
0x1870- 0x1874	Specific Register	R/W	00	Blocked for test modes
0x1875	Specific Register	R/W	00	Blocked for test modes

7.3.26 ISP Mode

Address	Name	Mode	Value At Reset	Function
0x1900	ISP control register	R/W	00	ISP mode control and enable register
0x1901	Specific Register	R/W	00	Blocked for test modes

8. SUPPORT LOGIC

The Support Logic provides the following functionality：

- System reset and Clock Control
- Interrupt Processing / Control
- Ringer Tone Generation

Figure 8-1 illustrates the functionality of the MCU Chip Support Logic：

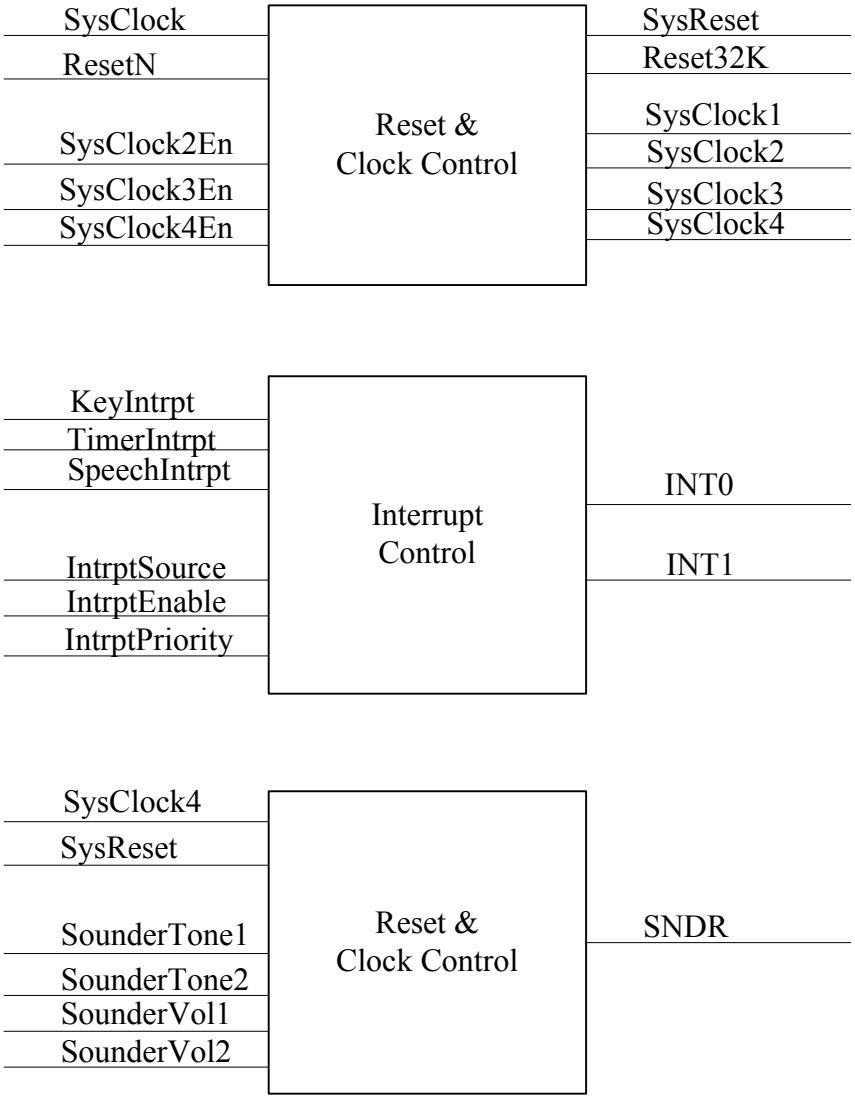


Figure 8-1 Illustration of the MCU Chip Support Logic

8.1 Clock Control & Reset 32K

8.1.1 Overview

Each register in the Speech Processor、Support and Interface Logic is reset synchronously. The Reset & Clock Control function ensures that the system reset signal is correctly generated. The system reset signal is also used to ensure that bi-directional signals are all set to input during initialization. A separate reset signal is provided for registers operating at 32KHz.

The MCU chip has five internal 13.824MHz clocks. The clocks are gated to conserve power. Four clocks are of the same phase and should be balanced during layout to allow data to be handled between the clock domains without additional logic. The clock to the 8032Turbo is of the opposite phase to the other four 13.824MHz clocks. The 32KHz clock is not gated or controlled on-chip.

8.1.2 Functionality

The System Reset signal SysReset is used to synchronously reset all the latches, which run from the 13.824MHz system clock:

- Two asynchronous latches sample the reset input. These are clocked to the non-reset state when the system clock is running and are used to ensure that the device is reset if the system clock is not running when the reset input is released.
- All gated clocks are enabled and the SysReset signal is asserted for 4 system clock cycles after the end of the external reset signal is detected by the asynchronous latches.
- SysReset is asserted from the time the asynchronous latches are reset until the end of the reset sequence to ensure bi-directional signals are forced to safe values during initialization.

A separate latch, controlled by a processor register bit Reset32k holds all 32768Hz logic in reset until set by the processor.

The 8032T is reset by SysReset.

Clock gating is performed with an OR function such that the clock signal is held high when disabled.

The Support and Interface Logic use 6 clocks: -

- SysClock: Non-gated 13.824MHz clock.
- SysClock1: Clock to the 8032Turbo.This clock is inverted relative to the other four SysClocks. Enabled for (clocks_unstable=0).
- SysClock2: Clock to the Processor-Writeable registers. Controlled by the Processor Interface.
- SysClock3: Clock to the Speech Interface Logic (which is not needed by the CODEC). Controlled by Processor-writeable register.
- SysClock4: Clock to the Ringer Tone Generator. Controlled by Processor-writeable register.
- SysClock5:Clock to the Winbond Linear CODEC (and logic in the Speech Interface needed to support operation of the CODEC)

Care will be required in the physical design of the Support Logic to ensure balancing of all clocks.

All outputs from logic in the 32768Hz clock domain are re-timed on entering the 13.824MHz clock domain. This is done using serial pairs of latches to give metastability protection.

Signals in Interface Logic are re-timed: -

- KeyPress interrupt
- WatchDog interrupt
- WatchDog kick
- 1 millisecond timer interrupt
- 1 second timer interrupt

8.1.3 Clock Enable Register

Address	Access Mode	Value At Reset	Nominal Value
0x1440	R/W	0xFD	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset32K	Blocked (for test modes)				SysClock5En	SysClock4En	SysClock3En

Sysclock3En When set, enable system clock 3.

Sysclock4En	When set, enable system clock 4.
Sysclock5En	When set, enable system clock 5.
Reset32K	set low to reset the 32KHz clock source.

8.2 Interrupt Control

8.2.1 Overview

The Support and Interface Logic generate internal events, these interrupt events are conditioned by the Interrupt Control logic before it is issued to the Processor. Figure 8-2 shows the interrupt structure.

8.2.2 Functionality

The Support and Interface Logic generate interrupt events as one-cycle pulses. The Support and Interface Logic generate the following interrupts:

- Hardware Keypad Scanner Interrupt
- Keypad port input general purpose IO Interrupt
- Timer Interrupt
- Speech Interface Interrupt
- WatchDog Interrupt

The Speech Interface generates the following interrupts: -

- PCM Port Input General Purpose IO Interrupt

Three registers control the generation of interrupts in the MCU chip, the IntrptSource register, the IntrptEnable register and the IntrptPriority register. Each interrupt has a corresponding bit in the IntrptSource, IntrptEnable and IntrptPriority registers.

- The IntrptSource register is set when an interrupt event occurs and is cleared by Processor write.
- When the Processor writes to IntrptSource, any bits that are set to 1 cause the corresponding bit of IntrptSource to be cleared, bits set to 0 are not affected.
- An Interrupt is generated when IntrptSource AND IntrptEnable =1 for any of the interrupt sources.
- For each bit; if IntrptPriority =0, the interrupt is issued to INT0, if IntrptPriority =1, the interrupt is issued to INT1.
- The watchdog interrupt is implemented for debug purposes only. The Watchdog must be kicked before attempting to clear its associated source register.

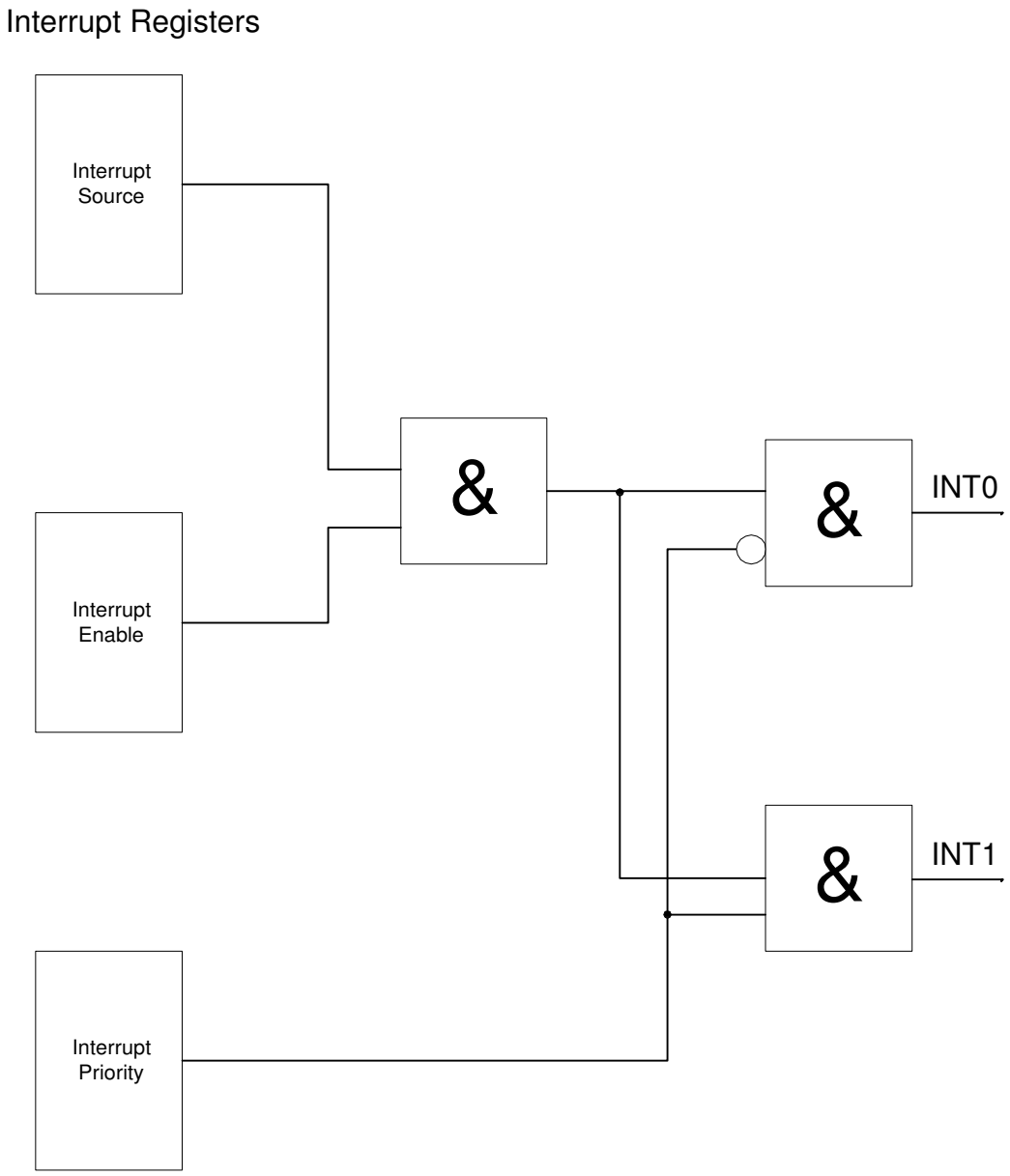


Figure 8-2 Interrupt Structure

8.2.3 Interrupt Registers

Address	Name	Description	Bit	Description	Value At Reset
1441H	IntrptSource0	Interrupt source register 0 Read: 1 = Interrupt 0 = No Interrupt Write: 1 = Clear	0	Blocked(for test modes)	0
			1	Blocked(for test modes)	0
			2	Blocked(for test modes)	0
			3	Blocked(for test modes)	0
			4	Blocked(for test modes)	0
			5	Timer1sIntrpt	0
			6	Timer1msIntrpt	0
			7	KeyPressIntrpt	0
1442H	IntrptSource1	Interrupt source register 1 Read: 1 = Interrupt 0 = No Interrupt Write: 1 = Clear	0	SpeechIOIntrpt	0
			1	WatchdogIntrpt	0
			2	KeyIOIntrpt	0
			3	Blocked(for test modes)	0
			4	Blocked(for test modes)	0
			5	Blocked(for test modes)	0
			6	Blocked(for test modes)	0
			7	Blocked(for test modes)	0
1443H	IntrptEnable0	Interrupt enable register 0 1 = Enabled 0 = Disabled	0	Blocked(for test modes)	0
			1	Blocked(for test modes)	0
			2	Blocked(for test modes)	0
			3	Blocked(for test modes)	0
			4	Blocked(for test modes)	0
			5	Timer1sIntrpt	0
			6	Timer1msIntrpt	0
			7	KeyPressIntrpt	0
1444H	IntrptEnable1	Interrupt enable register 1 1 = Enabled 0 = Disabled	0	SpeechIOIntrpt	0
			1	WatchdogIntrpt	0
			2	KeyIOIntrpt	0
			3	Blocked(for test modes)	0
			4	Blocked(for test modes)	0
			5	Blocked(for test modes)	0
			6	Blocked(for test modes)	0
			7	Blocked(for test modes)	0
1445H	IntrptPriority0	Interrupt priority register 0 0 = INT0 1 = INT1	0	Blocked(for test modes)	0
			1	Blocked(for test modes)	0
			2	Blocked(for test modes)	0
			3	Blocked(for test modes)	0
			4	Blocked(for test modes)	0
			5	Timer1sIntrpt	0
			6	Timer1msIntrpt	0
			7	KeyPressIntrpt	0
1446H	IntrptPriority1	Interrupt priority register 1 0 = INT0 1 = INT1	0	SpeechIOIntrpt	0
			1	WatchdogIntrpt	0
			2	KeyIOIntrpt	0
			3	Blocked(for test modes)	0
			4	Blocked(for test modes)	0
			5	Blocked(for test modes)	0
			6	Blocked(for test modes)	0
			7	Blocked(for test modes)	0

8.2.4 Extends of interrupt

144DH	IntrptSource2	Interrupt source register 2 1 = Interrupt 0 = Cleared	0	Blocked(for test modes)	0
			1	Reserved	0
			2	SPIIntrpt	0
			3	W2SIntrpt	0
			4	Blocked(for test modes)	0
			5	CPWRIntrpt	0
			6	Reserved	0
			7	USBIntrpt	0
144EH	IntrptEnable2	Interrupt enable register 2 1 = Enable 0 = Disable	0	Blocked(for test modes)	0
			1	Reserved	0
			2	SPIIntrpt	0
			3	W2SIntrpt	0
			4	Blocked(for test modes)	0
			5	CPWRIntrpt	0
			6	Reserved	0
			7	USBIntrpt	0
144FH	IntrptPriority2	Interrupt priority register 2 0 = INT0 1 = INT1	0	Blocked(for test modes)	0
			1	Reserved	0
			2	SPIIntrpt	0
			3	W2SIntrpt	0
			4	Blocked(for test modes)	0
			5	CPWRIntrpt	0
			6	Reserved	0
			7	USBIntrpt	0

8.3 Ringer Tone Generator

8.3.1 Overview

The buzzer signal generates tones to signal an incoming call.

There are two buzzer signal can be selected to connect to SNDR pin. This subsection describes the Ringer Tone Generator with the PWM (Pulse Width Modulation) format. The other buzzer signal of PDM (Pulse Density Modulation) format will be described on 1503[1:0].

8.3.2 Functionality

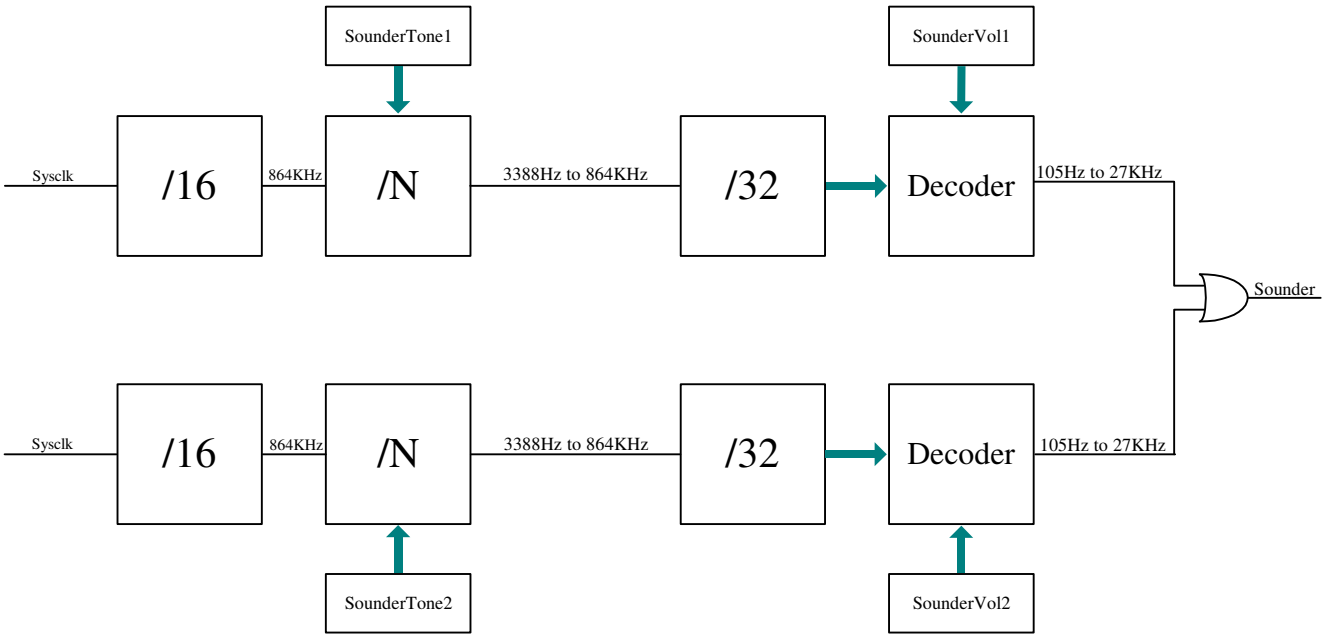


Figure 8-3 The Ringer Tone Generator

The Ringer Tone Generator has two controllable tone sources, shown in Figure 8-3. This each gives a programmable output frequency of between 105Hz and 27KHz. Each tone source has a programmable mark-to-space ratio. By controlling the mark to space ratio the volume of the sounder can be controlled.

- The ÷16 function produces a 864kHz pulse from the 13.824MHz system clock.
- The ÷n function produces a 3388 to 864kHz pulse from its 864kHz input. The output frequency of this function and the corresponding output frequency of the chip is determined by the SounderTone register.
- The ÷ 32 function contains a counter, clocked by the system clock, which increments on each pulse at it input. The Decoder uses the 4-bit output from this counter to produce a 105Hz to 27kHz with a programmable Mark-Space ratio defined by the SounderVol register.
- The tone source always starts in the same way (for a given set of programmed values)
- The tone source stops cleanly, that is it stops in the inactive state (logic 0) without truncation of any ongoing high pulse.
- The results of tone source one and tone source two are logically OR together to produce the output signal Sounder".
- Both tone generators have a common enable signal to allow them to be synchronized together.
-

8.3.3 Sounder Tone Register Definition

The registers SounderTone1 and SounderTone2 set the output frequency of the corresponding tone generator.

Each 8-bit register has a range of 1 to 255 (decimal) corresponding to an output frequency range of 105Hz to 27KHz, with a 10% tolerance.

8.3.4 Sounder Volume Register Definition

The registers SounderVol1 and SounderVol2 set the mark to space register of the corresponding tone generator.

Table 8-1: SounderVol1 and SounderVol2 pulse generation ratio.

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Mark	Space
0	0	0	0	0	No output (permanent low)	
0	0	0	0	1	1	31
0	0	0	1	0	2	30
0	0	0	1	1	3	29
0	0	1	0	0	4	28
0	0	1	0	1	5	27
0	0	1	1	0	6	26
0	0	1	1	1	7	25
……						
1	1	1	1	0	30	2
1	1	1	1	1	31	1

8.3.5 Example of use

In order to generate a 794Hz frequency output from tone source one with a mark to space ratio of 1:1. Program the SounderTone1 register with 00100010 (÷ n = 35) and program the SounderVol1 register with 10000.

To give a 1350Hz frequency output from tone source one with a mark to space ratio of 7:25. Program the SounderTone1 register with 00010100 (÷ n = 21) and program the SounderVol1 register with 00111.

8.3.6 Sounder Registers

Address	Name	Description	Bit	Description	Value at Reset
1447H	SounderTone1	Sounder frequency control	0	Sounder frequency control	0
			1		0
			2		0
			3		0
			4		0
			5		0
			6		0
			7		0
1448H	SounderTone2	Sounder frequency control	0	Sounder frequency control	0
			1		0
			2		0
			3		0
			4		0
			5		0
			6		0
			7		0
1449H	SounderVol1	Sounder volume control	0	Sounder volume control	0
			1		0
			2		0
			3		0
			4		0
			5	Reserved	0
			6	Reserved	0
			7	Tone generators enable = 1	0
144AH	SounderVol2	Sounder volume control	0	Sounder volume control	0
			1		0
			2		0
			3		0
			4		0
			5	Reserved	0
			6	Reserved	0
			7	Tone generators enable = 1	0
144BH	PIEZO Function	Enable PIEZO function Select PIEZO frequency	0	Enable	0
			1	Frequency Select 0: 216KHz, 1: 108KHz	0
			2	Reserved	0
			3	Reserved	0
			4	Reserved	0
			5	Reserved	0
			6	Reserved	0
			7	Reserved	0
144CH	PIEZO Clock output	Output twice clock count of this register value	0	PIEZO driving signal from PCM0	0
			1		0
			2		0
			3		0
			4		0
			5		0
			6		0
			7		0

8.4 PIEZO Tone Generator

8.4.1 Overview

The PIEZO signal can generated by the Ringer Tone generator, this subsection describe the PIEZO-driving clock from the Ringer tone generator, shown in Figure 8-4.

8.4.2 Functionality

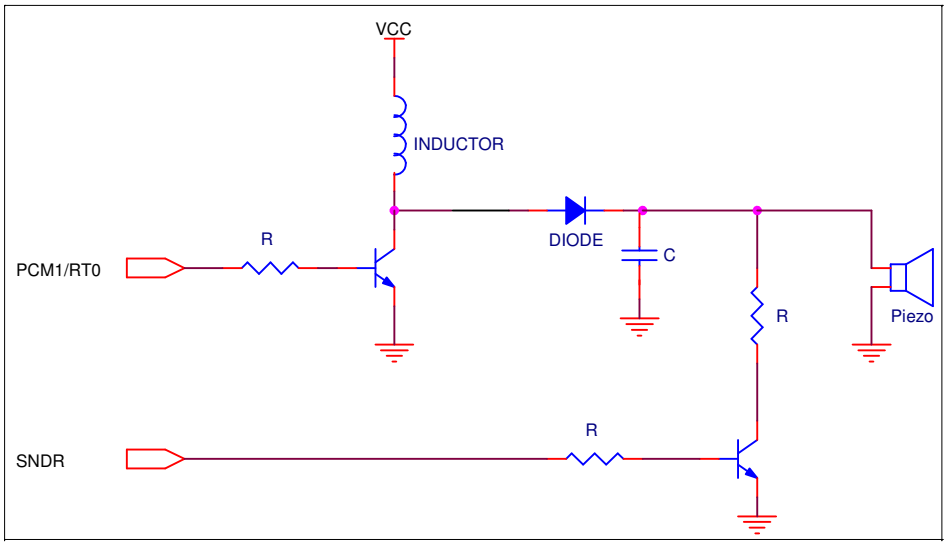


Figure 8-4 Piezo tone circuit

The PCM1/RTO pin generates the driving signal to obtain higher voltage. When set register 0x144B[0], will enable the functionality of Piezo, 0x144B[1] select the frequency of 108KHz or 216KHz for driving signal. The register 0x144C[7:0] output the twice number of clock for up conversion the voltage. The Soundertone and SounderVol register controls the melody of piezo.

9. INTERFACE LOGIC

The Interface logic consists of：

- A Keypad Scanner
- Timers
- Input/Output Ports

Figure 9-1 illustrates the operation of the Interface Logic：

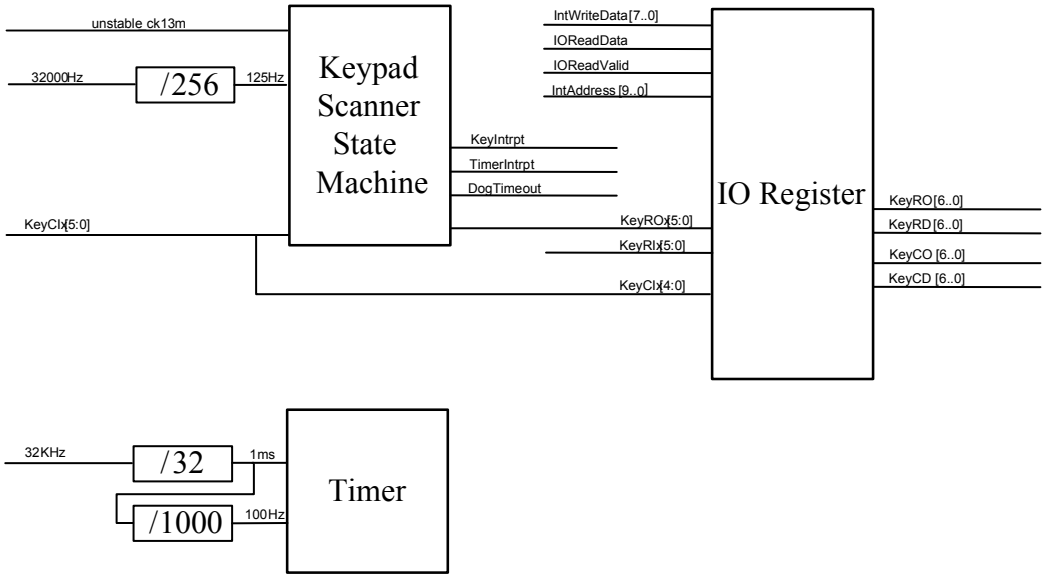


Figure 9-1 The Interface Logic.

9.1 Keypad Scanner

9.1.1 Overview

The Keypad Scanner State Machine operates from the 32000Hz clock. The keypad scanner identifies which key has been pressed and includes de-bouncing logic. Multiple concurrent key presses are not supported. Dividers provide 1Hz and 1ms timing signals. The 1 Hz signal provides timing for keypad de-bouncing and the 1 Hz and 1ms signals are used for the Timer.

The KeySize register sets the size of the keypad, up to 9 of the unused signals can be used as IO Ports.

All active Row outputs are initially set high, each Column input has an external pull-down resistor. When a Key is pressed, the signal from one Column will go high. The Keypad Scanner function operates as follows:

- The State machine waits in a default state until a high is found at one of the Column inputs.
- Each active Row output is set low in turn until a low is detected at the Column input. The Row and Column numbers are stored.
- The State Machine waits for the de-bounce period set in the KeyBounce Register.
- Each Row output is set low in turn until a low is detected at the Column input. The Row and Column numbers are stored.
- The Row and Column numbers stored at 2 and 4 are compared. If these are the same, a valid keystroke has been detected.
- The State Machine waits for unstable_ck13m to go low, asserts KeyIntrpt and returns to 1.

The KeyBounce register sets a de-bounce period of 8mS, 16mS, 24mS or 32mS (times are -0.0 mS +1.5 mS).

9.1.2 Use of the Keypad Scanner

The software should set up the KeyPadSize register so that the keypad can be used. This register sets the keypad size and the de-bounce period.

Once a key has been de-bounced a KeyIntrpt interrupt is generated and the key value is stored in the KeyLocation register. When the key is released a further KeyIntrpt interrupt is generated. (Note that only two interrupts are generated in a key press release sequence and that holding a key down for extended periods does not result in multiple interrupts.)

The KeyPress register bit in the KeyLocation states whether a key is pressed. When a key is pressed the bit is active once the key press has been de-bounced and is removed once the key is released.

Where ports are being used with the hardware keypad scanner, the corresponding data bit in the Key IO port output data register must be set to zero.

9.1.3 Use of a Software Keypad Scanner

If keypad scanning is done in software than the keypad scanner functionality is not used and the pins are treated as general purpose I/O ports KeyC[3:0] and KeyR[4:0].

9.2 I/O Ports

Pins not used by the Keypad scanner are available as standard IO Ports, controlled by KeyIoDR, KeyIoDC, KeyIoIpR, KeyIoIpC, KeyIoOpR and KeyIoOpC. An interrupt event will be generated if there is a change in the value of any one of KeyIoIp and the corresponding bit of KeyIoMsk is set.

Note that the direction of KeyC[3:0] amd KeyR[4:0] are always controlled by the KeyIoDC[3:0], KeyIoDR[4:0] registers.

9.3 Keypad Control Registers

Address	Name	Description	Bit	Description	Value at Reset	Physical Mapping to output ports
1450H	KeyIoDR Sysclock2	Key IO Port Direction Control Register 0 = output 1 = input(Default)	0	KeyIoDR[0]	1	Row[0]
			1	KeyIoDR[1]	1	Row[1]
			2	KeyIoDR[2]	1	Row[2]
			3	KeyIoDR[3]	1	Row[3]
			4	KeyIoDR[4]	1	Row[4]
			5	Reserved	1	
			6	Blocked (for test modes)	0	
			7	Reserved	1	
1451H	KeyIoDC Sysclock2	Key IO Port Direction Control Register 0 = output 1 = input	0	KeyIoDC[0]	1	Col[0]
			1	KeyIoDC[1]	1	Col[1]
			2	KeyIoDC[2]	1	Col[2]
			3	KeyIoDC[3]	1	Col[3]
			4	Reserved	1	
			5	Reserved	1	
			6	Reserved	1	
			7	Reserved	1	
1452H	KeyIoIpR Sysclock2	Key IO Port Input Data Register Value =True	0	KeyIoIR[0]	0	Row[0]
			1	KeyIoIR[1]	0	Row[1]
			2	KeyIoIR[2]	0	Row[2]
			3	KeyIoIR[3]	0	Row[3]
			4	KeyIoIR[4]	0	Row[4]
			5	Reserved	0	
			6	Reserved	0	
			7	Reserved	0	
1453H	KeyIoIpC Sysclock2	Key IO Port Input Data Register Value =True	0	KeyIoIC[0]	0	Col[0]
			1	KeyIoIC[1]	0	Col[1]
			2	KeyIoIC[2]	0	Col[2]
			3	KeyIoIC[3]	0	Col[3]
			4	Reserved	0	
			5	Reserved	0	
			6	Reserved	0	
			7	Reserved	0	
1454H	KeyIoOpR Sysclock2	Key IO Port Output Data Register Value =True	0	KeyIoOR[0]	0	Row[0]
			1	KeyIoOR[1]	0	Row[1]
			2	KeyIoOR[2]	0	Row[2]
			3	KeyIoOR[3]	0	Row[3]
			4	KeyIoOR[4]	0	Row[4]
			5	Reserved	0	
			6	Reserved	0	
			7	Reserved	0	

Address	Name	Description	Bit	Description	Value at Reset	Physical Mapping to output ports
1455H	KeyIoOpC Sysclock2	Key IO Port Output Data Register Value =True	0	KeyIoOC[0]	0	Col[0]
			1	KeyIoOC[1]	0	Col[1]
			2	KeyIoOC[2]	0	Col[2]
			3	KeyIoOC[3]	0	Col[3]
			4	Reserved	0	
			5	Reserved	0	
			6	Reserved	0	
			7	Reserved	0	
1456H	KeyIoMskR Sysclock2	Key IO Port Control Register For Mask 0= off=masked 1= on=unmasked	0	KeyIoM[0]	0	Row[0]
			1	KeyIoM[1]	0	Row[1]
			2	KeyIoM[2]	0	Row[2]
			3	KeyIoM[3]	0	Row[3]
			4	KeyIoM[4]	0	Row[4]
			5	Reserved	0	
			6	Reserved	0	
			7	Reserved	0	
1457H	KeyIoMskC Sysclock2	Key IO Port Control Register For Mask 0=off=masked 1=on=unmasked	0	KeyIoM[0]	0	Col[0]
			1	KeyIoM[1]	0	Col[1]
			2	KeyIoM[2]	0	Col[2]
			3	KeyIoM[3]	0	Col[3]
			4	Reserved	0	
			5	Reserved	0	
			6	Reserved	0	
			7	Reserved	0	
1458H	KeyPress Location Read Only	Gives the Row and column	0	KeyLocR[0]	0	
			1	KeyLocR[1]	0	
			2	KeyLocR[2]	0	
			3	KeyLocC[0]	0	
			4	KeyLocC[1]	0	
			5	KeyLocC[2]	0	
		Shows "1" when KeyPad is pressed	6	KeyPressed	0	
			7	Reserved	0	
1459H	KeyPadSize	Sets the size of the Keypad scanned by the Keypad Scanner function	0	KeyRows[0]	0	
			1	KeyRows[1]	0	
			2	KeyRows[2]	0	
			3	KeyColumn[0]	0	
			4	KeyColumn[1]	0	
			5	KeyColumn[2]	0	
			6	KeyDb[0]	0	
			7	KeyDb[1]	0	

The Timer1sReset bit and watchdog time bits cannot be altered once the watchdog is enabled.

The watchdog is reset every time the location WatchDogKick is written to.

9.3.1 Key Location and Size Programming

Key Location and size registers, KeyLocR[*], KeyLocC[*], KeyRows[*] & KeyColumns[*] are defined as follows:-

Row/Column	[2:0]
Zero (see Note)	0x00
One	0x01
Two	0x02
Three	0x03
Four	0x04
Five	0x05

Note:
that zero is only valid for KeyRows[*] and KeyColumns[*], which means the keypad size=0 and all the keypad pins serve as GPIO. On the other hand, the keyLocR[*] and keyLocR[*] are only checked when KeyPressed bit=1 (0x1458[7]) and meanwhile it should contain non-zero value.

9.4 Timers

There are 3 timers: -

- A programmable 1-millisecond timer
- A 1 second timer
- A programmable 1-second watchdog timer.

The programmable 1-millisecond timer can be enabled, reset and programmed to generate an pulse in the range 1 millisecond to 64 milliseconds (1 millisecond spacing).

The 1-second timer can be enabled, reset and always generates a pulse every 1 second.

The programmable 1 second watchdog timer can be enabled and programmed to generate a pulse in the range 1 second to 8 seconds (1 second spacing). Following reset the watchdog timer is disabled.

In normal operation the watchdog timer should be enabled by writing to the WatchDogEnable bit and the WatchDogResetEn bit. Once written to these bits cannot be cleared except by a system reset, hence the watchdog cannot be disabled. Enabling the Watchdog timer also prevents disabling of the 1-second timer.

The watchdog counts from the output of the 1-second timer. The expiry time is programmable and this value is set in the WatchDogTime[0:2] register field. The software must clear the watchdog counter regularly. If the watchdog counter ever reaches the expiry time, a reset and interrupt will occur.

Note: A write to the WatchDogKick location will not affect the 1-second timer from which the watchdog operates. Therefore if the watchdog is set to 8 seconds, the timeout will occur between 7 to 8 seconds. The WatchDogKick location must be written to before 7 seconds, otherwise a reset and interrupt will occur. It is recommended that a setting of 1 second is not used.
In order to facilitate software debug the device has the Watchdog expiry generated reset disabled from reset. A watchdog interrupt is provided to assist software debugging, this interrupt WatchDogIntrpt is generated by the watchdog timer if it expires. In this case the WatchDogEnable bit would be set, but not the WatchDogResetEn bit.

9.4.1 Watch Dog Control

Address	Access Mode	Value At Reset	Nominal Value
0x145A	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	WatchDog ResetEn	Watch Dog Timer [2:0]			WatchDogEn	KeyBounce[1:0]	

WatchDogEn When set, enable the watchdog, which use system clock source 2.
WatchDogTimer [2:0] Controls the repetition rate of the watchdog timer 1 second to 8 seconds.
WatchDogResetEn When set, it will reset whole baseband chip.
KeyBounce[1:0] Key Debounce Period Selection.

The de-bounce period is defined as follows:

Key-Bounce Period	KeyBounce[1:0]
8 ms	0x00
16 ms	0x01
24 ms	0x02
32 ms	0x03

All times are +/- 0.5ms

9.4.2 Timer 1ms Control1

Address	Access Mode	Value At Reset	Nominal Value
0x145B	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Timer1msLength[5:0]						Timer1msEn	Timer1ms Reset

Timer1msLength[5:0] 1ms timer counter, which controls the repetition rate of the 1ms timer up to 64 ms.
Timer1msEn When set to ‘1’, enable 1ms timer to proceed from it’s previous status. When reset to ‘0’, this just pause the operation but not reset the content.
Timer1msReset When reset to ‘0’, reset the 1ms timer. This timer will operate only when this bit remains ‘1’.

9.4.3 Timer Control

Address	Access Mode	Value At Reset	Nominal Value
0x145C	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reset 1S counter	Reserved	Reserved	Reset 1mS counter	Reset 1S timer

1S timer reset when reset to “0”, reset the 1S timer.
1mS counter reset when reset to “0”, reset the 1mS counter, but this bit does not affect the operation of 1ms timer which is controlled by 0x145B.
1S counter reset when reset to “0”, reset the 1S counter value in 0x145D, but this bit does not affect the operation of 1S timer.

9.4.4 1S Counter

Address	Access Mode	Value At Reset	Nominal Value
0x145D	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	1S Counter					

1-second counter This register records the time in 1 second resolution. Maximum value is 59.

9.4.5 Watch Dog Kick

Address	Access Mode	Value At Reset	Nominal Value
0x145E	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Watch Dog Kick							

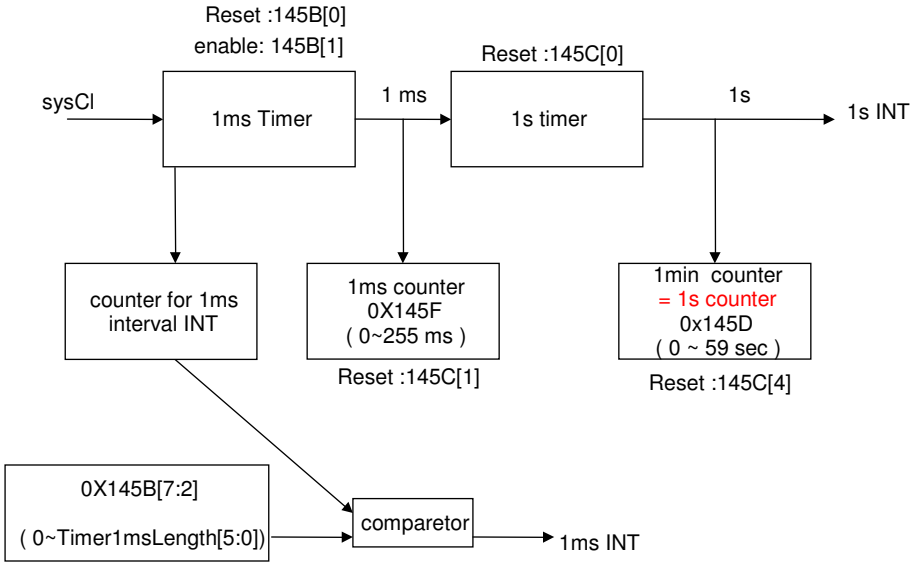
Write to this value will reset the watchdog timer.

9.4.6 1ms Counter

Address	Access Mode	Value At Reset	Nominal Value
0x145F	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Counter value for 1mS timer							

This register records the time in 1 ms resolution. Maximum value is 255.



Note1: ALL THE RESET activities ARE LEVEL_TRIGGERED.
Note2: reset 145C[1] will not effect the waveform of 1ms INT.

10. SPEECH INTERFACE

10.1 Overview

The Speech Interface allows the MCU chip to be connected to one or more of the following:

- External PCM CODEC and Echo Canceller.
- IO Ports which can be used when the external Speech Expansion Interface is not required.
- A test interface to and from the on-chip linear CODEC.

The Speech Interface Block also connects with the on-chip linear CODEC.
The Speech interface also contains three programmable outputs, which are used to control certain pins.

10.2 Functionality

Figure 10-1 shows the speech interface block diagram.

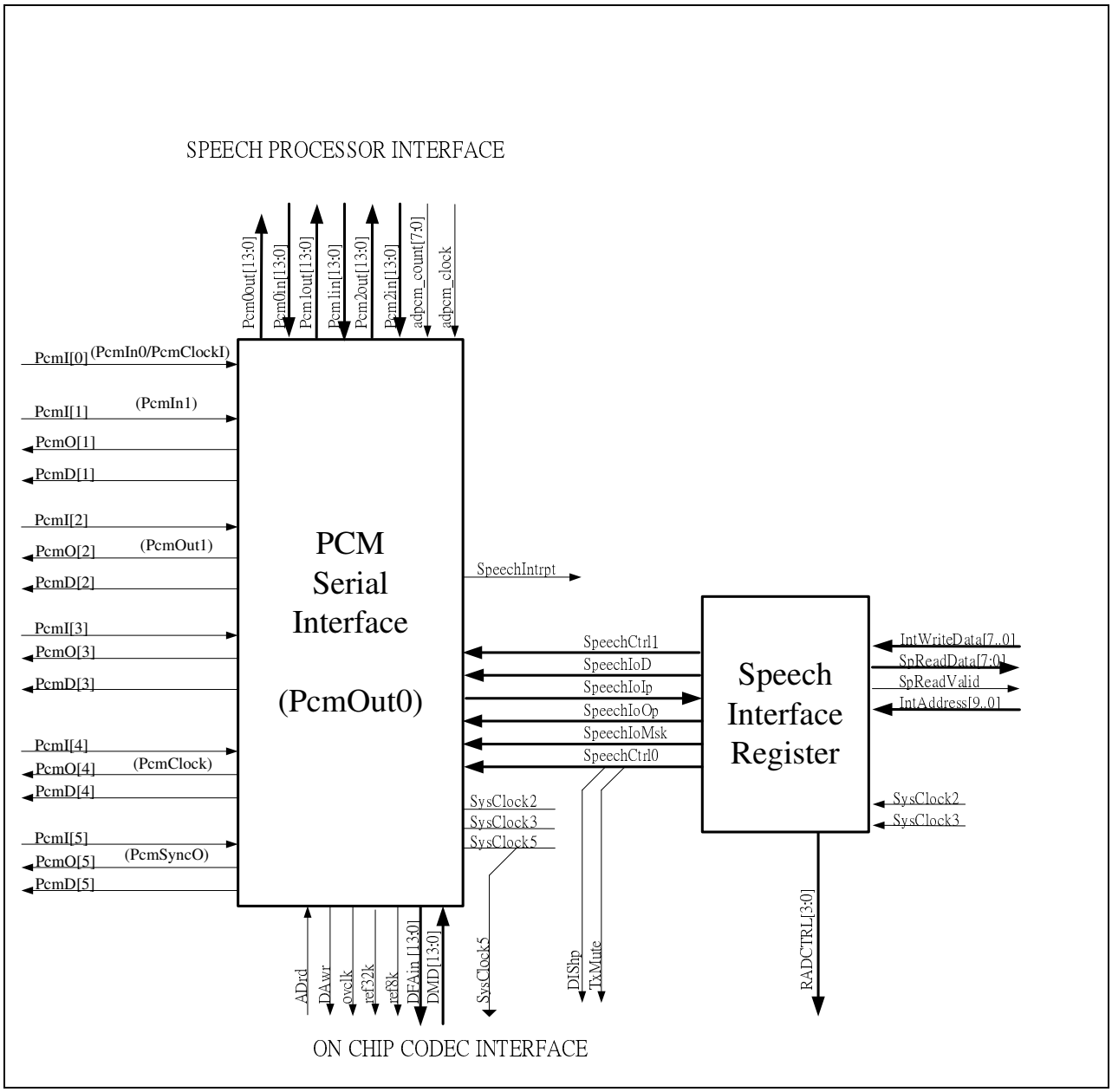


Figure 10-1 Speech Interface Block Diagram

10.3 PCM Serial Interface

The PCM Serial Interface：

- Formats parallel PCM data to/from the Speech Processor for use by external devices
- PCM serial interface supports to convert serial pcm data of external devices to parallel pcm data of Speech Processor. PCM highway supports 4 external devices by 4 slots pcm channels (B1 ~ B4). The internal USB ISO endpoint and the 4th slot of PCM highway are shared with the same PCM channel (B4). When the USB_EN bit is set to high, the internal USB ISO endpoint will be automatically connected to the PCM channel (B4). All channels supports 8/16 bits pcm format, and IOM2 mode.
- PCM highway interface can support maste or slave modes with external devices.
- Implements a 4-bit general purpose IO port when the PCM Serial Interface function is not required

Routing diagram as below Figure 10-2：

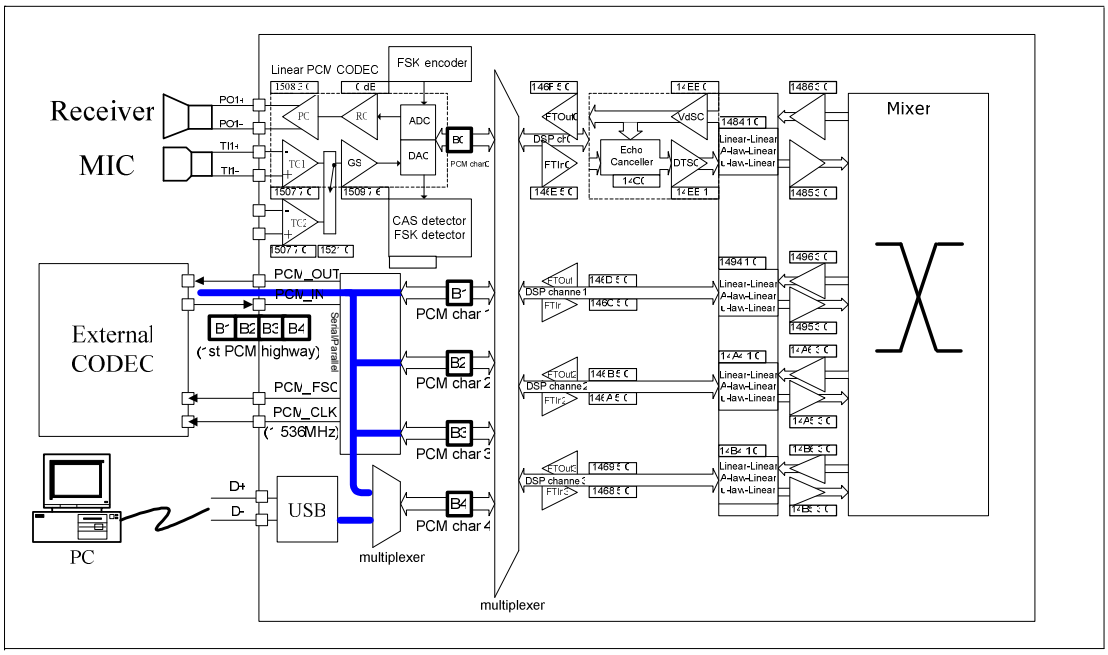


Figure 10-2 W681307 Speech Flow Block Diagram

10.3.1 Use with Additional External Lines

The PCM serial interface block can route channels 1, 2 and 3 from the Speech Processor to PCM highway which can be used to interface to external CODECs to provide connection to two external lines.

For this mode PcmIf enable =1 and Slave Mode =0.
PCM Serial Interface can generate a Long frame sync (for LongSync =1) or a Short frame sync (for LongSync=0).
Timing diagrams for short frame sync and long frame sync modes are given in section 9.7.

10.3.2 I/O Ports

For PCMH1_Dis =1, the Speech Interface is reset and PCM highway (pins name: PCM_OUT, PCM_IN, PCM_FSC, PCM_CLK) operate as standard IO ports, controlled by SpeechIoD, SpeechIoIp and SpeechIoOp registers. An interrupt event will be generated if there is a change in the value of any one of SpeechIoIp and the corresponding bit of SpeechIoMsk is set.

For PCMH1_Dis=0, the direction of PCM highway is always controlled by the PCM highway function setting. In the PCM master mode, the PCM_OUT, PCM_FSC and PCM_CLK pins areoutput, the PCM_IN pin is input. In the PCM slave mode, the PCM_OUT pin is output, the PCM_IN, PCM_FSC and PCM_CLK pins are output.

10.3.3 Status of Speech Interface When Reset

When the device is reset then the speech interface I/O pins will all be set as inputs and the associated interrupts will be masked. Resetting the device will cause the Speech Interface Pins (PCM[0:5] to be (general purpose) I/O ports.

10.4 Internal CODEC Control

The Speech Interface Block provides two control bits to the internal CODEC. The bits are used for TxMute and DisHPF. The signals are output from the speech interface block and go to the internal CODEC. The values output by the speech interface on the two ports equates to the value programmed in DisHPF and TxMute, the bits are reset to 0.

10.5 PCM Interface Registers

This section describes the Speech Interface Register.

10.5.1 Speech Control 0

Address	Access Mode	Value At Reset	Nominal Value
0x1460	R/W	0x03	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Blocked (for test modes)	Fsync Advance	Fsync 16/8bit	Fsync Long/Short	Blocked (for test modes)	Slave Mode	Reserved	PCMH1_Dis

According to the configuration of PCMH1_Dis bit, the PCM highway function and GPIO function can be served at four PCM pins at the same time. On the other hand, four PCM pins can just act for only pure PCM highway function or GPIO function.

B0: PCMH1_Dis	=1	PCM I/O ports are GPIO function.
	=0	PCM I/O ports are serial-parallel converter function.
B2: Slave Mode	=1	Effective PCM highway function will operate at **slave** mode.
	=0	Effective PCM highway function will operate at **master** mode.

B5: Fsync-16/8bit	B4:Fsync Long/Short	
x	0	Short Frame Sync signal is selected. The period of Fsync signal occupies 1 bit clock.
0	1	Long Frame Sync signal is selected. And the period of Fsync signal occupies 8 bits.
1	1	Long Frame Sync signal is selected. And the period of Fsync signal occupies 16 bits.

B6: Fsync advance	=1	The PCM_FSC signal is transmitted in advance of the PCM_CLK by one system clock.
	=0	The PCM_FSC signal is transmitted at the rising edge of the PCM_CLK

10.5.2 Specific Register

Address	Access Mode	Value At Reset	Nominal Value
0x1461	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Blocked (for test modes)	Blocked (for test modes)

10.5.3 Speech IO Direction

Address	Access Mode	Value At Reset	Nominal Value
0x1462	R/W	0x0F	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	SpeechIoD[3]	SpeechIoD[2]	SpeechIoD[1]	SpeechIoD[0]

When set PCM interface as General I/O, this register set the I/O direction.

SpeechIoD[0]	=1:	PCM0 pin will be operated as input port.
	=0:	PCM0 pin operated as output mode.
SpeechIoD[1]	=1:	PCM1 pin will be operated as input port.
	=0:	PCM1 pin operated as output mode.
SpeechIoD[2]	=1:	PCM2 pin will be operated as input port.
	=0:	PCM2 pin operated as output mode.
SpeechIoD[3]	=1:	PCM3 pin will be operated as input port.
	=0:	PCM3 pin operated as output mode.

10.5.4 Speech IO Input Data

Address	Access Mode	Value At Reset	Nominal Value
0x1463	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	SpeechIoI[3]	SpeechIoI[2]	SpeechIoI[1]	SpeechIoI[0]

SpeechIoI When PCM interface is configured as input port, this register reflects the input data.

10.5.5 Speech IO Output Data

Address	Access Mode	Value At Reset	Nominal Value
0x1464	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	SpeechIoO[3]	SpeechIoO[2]	SpeechIoO[1]	SpeechIoO[0]

SpeechIoO When PCM interface is configured as output port, this register set to output data.

10.5.6 Speech IO Mask

Address	Access Mode	Value At Reset	Nominal Value
0x1465	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	SpeechIOM[3]	SpeechIOM[2]	SpeechIOM[1]	SpeechIOM[0]

SpeechIOM[3:0] When PCM interface configured as input port, this register mask the interrupt when PCM interface input port is interrupted.

10.5.7 Fsync Counter

Address	Access Mode	Value At Reset	Nominal Value
0x1466	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Fsync-Counter						

Fsync-Counter Provide the status of the frame sync counter within the speech interface.

10.6 The multiplexer to connect 5 PCM channels to 4 processor channels

10.6.1 Multiplexer control register

Address	Access Mode	Value At Reset	Nominal Value
0x1467	R/W	0x11	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	PCM channel4	PCM channel3	PCM channel2	PCM channel1	PCM channel0

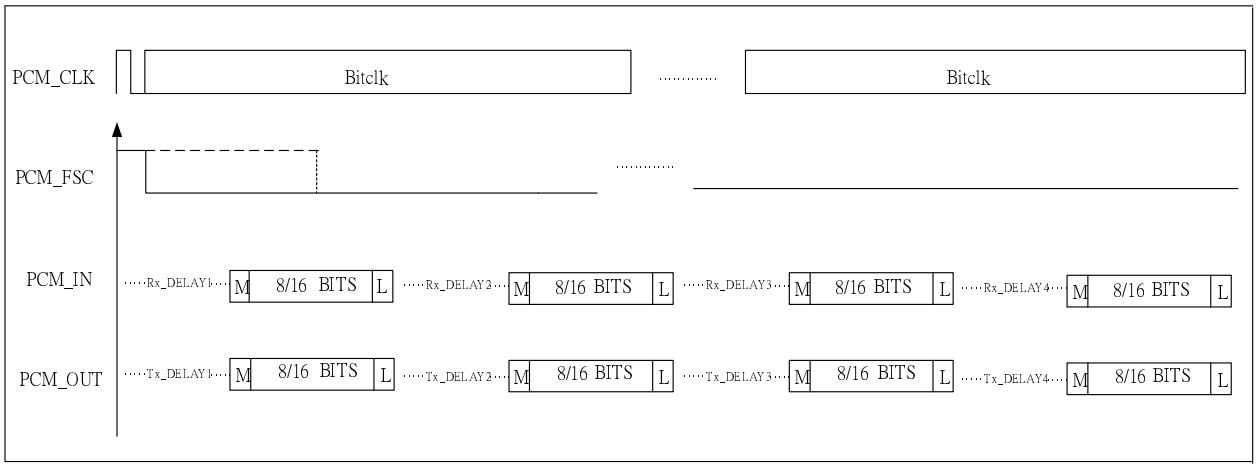
The function of the multiplexer is to choose 4 channels among the 5 PCM channels to be effective which can be connected to 4 processor channels by setting the multiplexer control register 0x1467. And the four processor channels labeled by from C0 to C3 will connect to the effective PCM channels in numerical order of the channel label.The PCM channel4 (B4) have two input source: USB ISO input and external pcm device. It is controlled by USB_EN bit. Setting USB_EN =1, the USB ISO data pass to pcm channel 4 .

10.7 PCM Highway Interface

10.7.1 The Introduction of PCM Modes

10.7.1.1 Master / Slaver mode

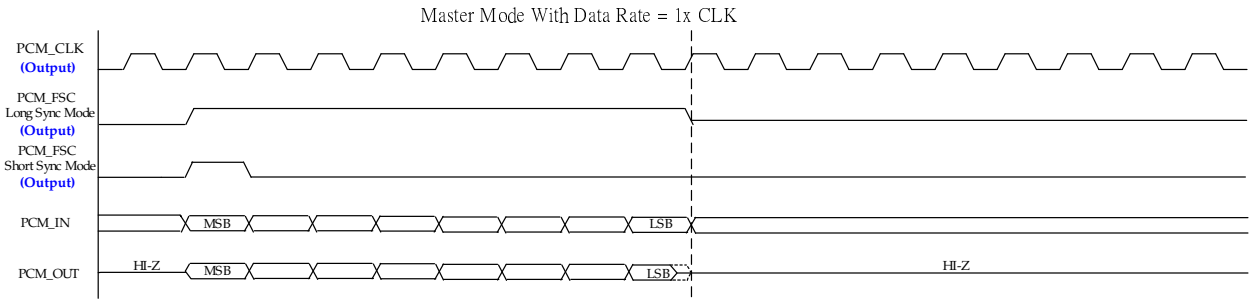
For Master mode, PCM_CLK and PCM_FSC is output port.
For Slaver mode, PCM_CLK and PCM_FSC is input port.

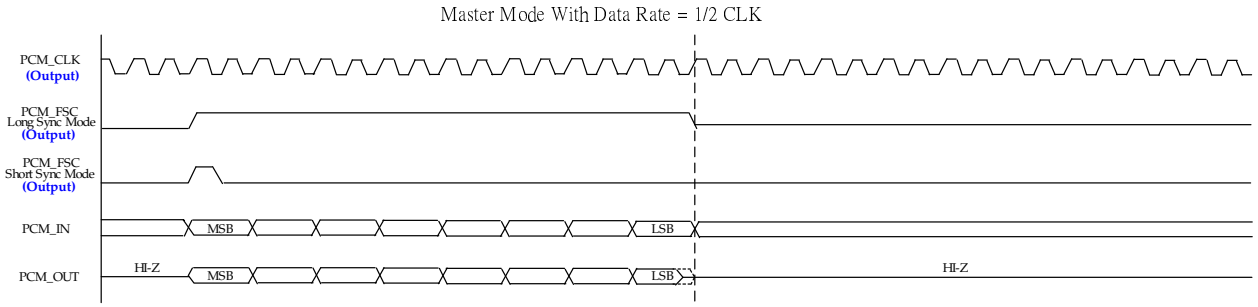


10.7.1.2 Master mode

In master mode, PCM_CLK and PCM_FSC is output port.

PCM_FSC	8K short sync or long sync.
PCM_CLK	1536 KHz
PCM_IN	When sync is coming, it starts to catch MSB in (first sync rising + delay1 bits). LSB is depending 8bits or 16bits for first slot. Data rate is 1x or 1/2 Clk.
PCM_OUT	When sync is coming, it starts to send MSB in (first sync rising + delay1 bits). LSB is depending 8bits or 16bits for first slot. Data rate is 1x or 1/2 Clk.





10.7.1.3 Slave mode

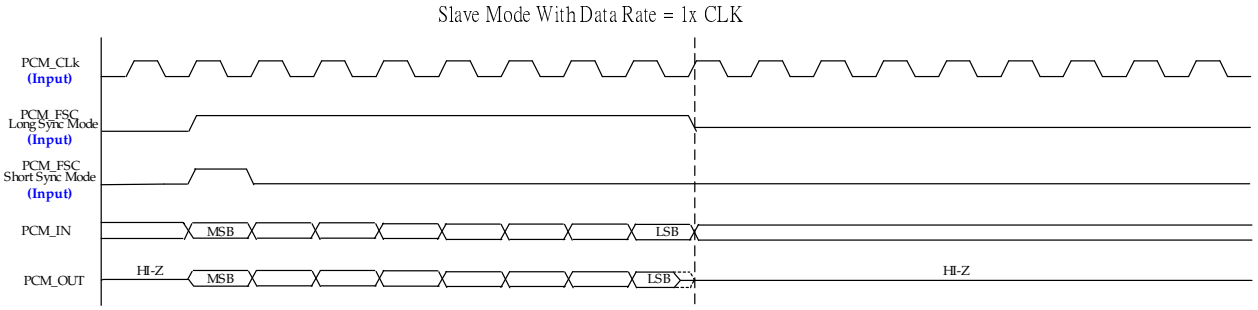
In slave mode, PCM_CLK and PCM_FSC is input port.

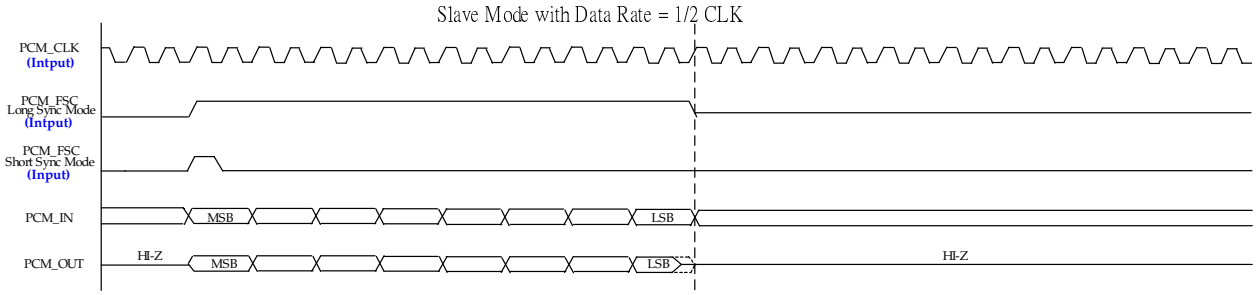
PCM_FSC 8K short sync or long sync.

PCM_CLK 768 KHz ~ 2048 KHz

PCM_IN When sync is coming, it starts to catch MSB in (first sync rising + delay1 bits). LSB is depending 8bits or 16bits for first slot. Data rate is 1x or 1/2 Clk.

PCM_OUT When sync is coming, it starts to send MSB in (first sync rising + delay1 bits). LSB is depending 8bits or 16bits for first slot. Data rate is 1x or 1/2 Clk.





10.7.2 The Description of PCM Highway Interface Registers

10.7.2.1 PCM channel format and delay control of 1st group (PCM B1, PCM B2)

Address	Access Mode	Value At Reset
0x1700h	R/W	0x02

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCMB1_dis	Half rate	PCMB2_dis	RESERVED	Hizen Half/Full	RESERVED	Data 16/8bits	RESERVED

Data 16/8bits	Set the bit to receive/transmit 16 bits; Reset the bit to receive/transmit 8 bits.
Hizen Half/Full	Set the bit to tristate in the end of the bit. Reset the bit to tristate in the falling edge of the end of the bit.
PCMB2_dis	=1: disabling the B2 channel of the PCM Highway. =0: enabling the B2 channel of the PCM Highway.
Half rate	Set the bit for one bit per 2 Bitclk (during data length being 16 bits=>0x1700 [1] =1'b1). Reset the bit for one bit per 1 Bitclk.
PCMB1_dis	=1: disabling the B1 channel of the PCM Highway. =0: enabling the B1 channel of the PCM Highway.

10.7.2.2 TX delay1

Address	Access Mode	Value At Reset
0x1701h	R/W	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX delay1							

Set the values for delaying the transmitted bits of PCM B1 channel after the rising edge of the frame pulse. The resolution is one bitclk in full date rate and two Bitclk in half data rate.

10.7.2.3 TX delay2

Address	Access Mode	Value At Reset
0x1702h	R/W	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX delay2							

Set the values for delaying the transmitted bits of PCM B2 channel after the tail bit of PCM B1 channel. The resolution is one PCM Bitclk in full date rate and two Bitclk in half data rate.

10.7.2.4 RX delay1

Address	Access Mode	Value At Reset
0x1703h	R/W	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX delay1							

Set the values for delaying the received bits of PCM B1 channel after the rising edge of the Fsync. The resolution is one Bitclk in full date rate and two Bitclk in half data rate.

10.7.2.5 RX delay2

Address	Access Mode	Value At Reset
0x1704h	R/W	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX delay2							

Set the values for delaying the received bits of PCM B2 channel after the tail bit of Rx PCM Highway B1 channel. The resolution is one Bitclk in full date rate and two Bitclk in half data rate.

10.7.2.6 PCM channel format and delay control of 2nd group (PCM B3, PCM B4)

Address	Access Mode	Value At Reset
0x1708h	R/W	0x02

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCMB3_dis	Half rate	PCMB4_dis	RESERVED	Hizen Half/Full	RESERVED	Data 16/8bits	RESERVED

Data 16/8bits	Set the bit to receive/transmit 16 bits; Reset the bit to receive/transmit 8 bits.
Hizen Half/Full	Set the bit to tristate in the end of the bit. Reset the bit to tristate in the falling edge of the end of the bit.
PCMB4_dis	=1: disabling the B4 channel of the PCM Highway. =0: enabling the B4 channel of the PCM Highway.
Half rate	Set the bit for one bit per 2 Bitclk (during data length being 16 bits=>0x1708 [1] =1'b1). Reset the bit for one bit per 1 Bitclk.
PCMB3_dis	=1: disabling the B3 channel of the PCM Highway. =0: enabling the B3 channel of the PCM Highway.

10.7.2.7 TX delay3

Address	Access Mode	Value At Reset
0x1709h	R/W	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX delay3							

Set the values for delaying the transmitted bits of PCM Highway B3 channel after the tail bit of TX PCM Highway B2 channel. The resolution is one Bitclk in full date rate and two Bitclk in half data rate.

10.7.2.8 TX delay4

Address	Access Mode	Value At Reset
0x170Ah	R/W	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX delay4							

Set the values for delaying the transmitted bits of PCM Highway B4 channel after the tail bit of TX PCM Highway B3 channel. The resolution is one Bitclk in full date rate and two Bitclk in half data rate.

10.7.2.9 RX delay3

Address	Access Mode	Value At Reset
0x170Bh	R/W	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX delay3							

Set the values for delaying the received bits of PCM Highway B3 channel after the tail bit of RX PCM Highway B2 channel. The resolution is one Bitclk in full date rate and two Bitclk in half data rate.

10.7.2.10 Rx delay4

Address	Access Mode	Value At Reset
0x170Ch	R/W	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX delay4							

Set the values for delaying the received bits of PCM Highway B4 channel after the tail bit of RX PCM Highway B3 channel. The resolution is one Bitclk in full date rate and two Bitclk in half data rate.

10.8 Digital Gain Multiplexer

There are 4 fine-tune on-chip gain stage allocated between multiplexer interface and half acoustic canceller block or behind multiplexer interface. This gain stage is implemented by a digital multiplexer to provide a range of +12 dB to –12 dB with a resolution of 0.5 dB per step. Figure 10-3 is shown the location of this digital gain multiplexer. **The 4 channels FT Gain Stage support gain adjustment for linear PCM signal for each PCM channel. Each channel has its independent gain registers for gain setting.**

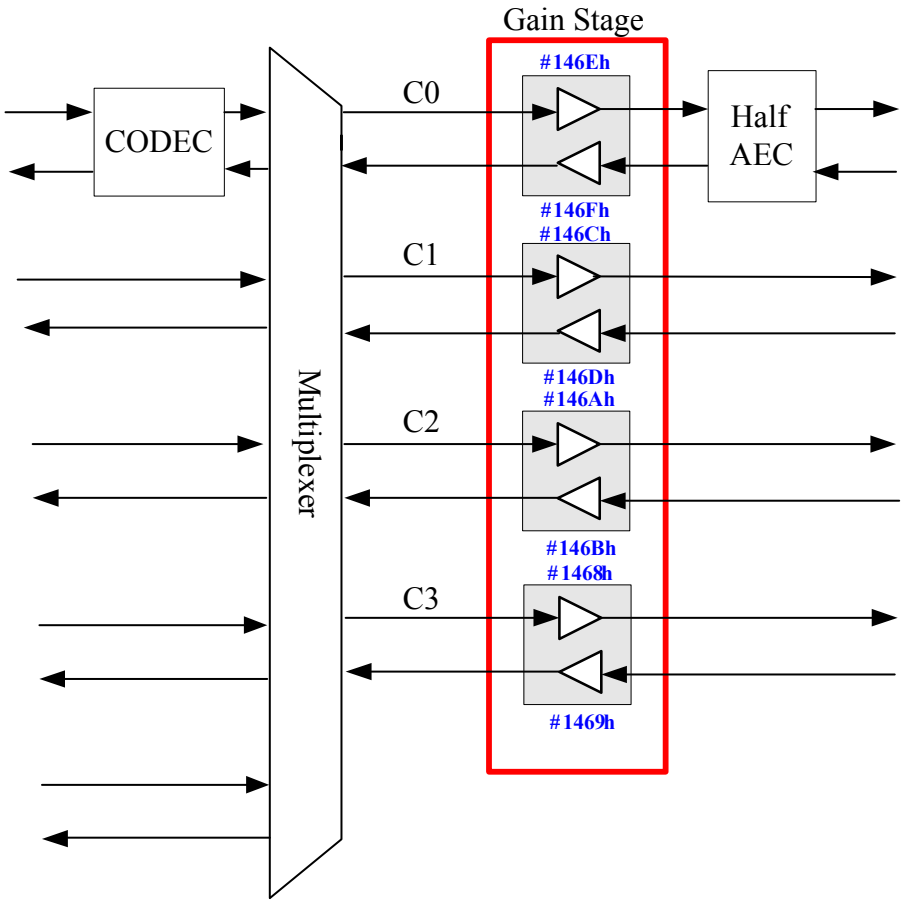


Figure 10-3 The location of digital fine-tuning gain stage

10.8.1 Fine-Tuning Gain Stage Registers

10.8.1.1 FTInGain3

Address	Access Mode	Value At Reset	Nominal Value
0x1468	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	FTInGain[5]	FTInGain[4]	FTInGain[3]	FTInGain[2]	FTInGain[1]	FTInGain[0]

Refer to Table 10-1 for fine tune input gain. This gain is applied to the input data of processor channel C3.

10.8.1.2 FTOutGain3

Address	Access Mode	Value At Reset	Nominal Value
0x1469	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	FTOutGain[5]	FTOutGain[4]	FTIOutGain[3]	FTOutGain[2]	FTOutGain[1]	FTOutGain[0]

Refer to Table 10-1 for fine tune output gain. This gain is applied to the output data of processor channel C3.

10.8.1.3 FTInGain2

Address	Access Mode	Value At Reset	Nominal Value
0x146A	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	FTInGain[5]	FTInGain[4]	FTInGain[3]	FTInGain[2]	FTInGain[1]	FTInGain[0]

Refer to Table 10-1 for fine tune input gain. This gain is applied to the input data of processor channel C2.

10.8.1.4 FTOutGain2

Address	Access Mode	Value At Reset	Nominal Value
0x146B	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	FTOutGain[5]	FTOutGain[4]	FTIOutGain[3]	FTOutGain[2]	FTOutGain[1]	FTOutGain[0]

Refer to Table 10-1 for fine tune output gain. This gain is applied to the output data of processor channel C2.

10.8.1.5 FTInGain1

Address	Access Mode	Value At Reset	Nominal Value
0x146C	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	FTInGain[5]	FTInGain[4]	FTInGain[3]	FTInGain[2]	FTInGain[1]	FTInGain[0]

Refer to Table 10-1 for fine tune input gain. This gain is applied to the input data of processor channel C1.

10.8.1.6 FTOutGain1

Address	Access Mode	Value At Reset	Nominal Value
0x146D	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	FTOutGain[5]	FTOutGain[4]	FTIOutGain[3]	FTOutGain[2]	FTOutGain[1]	FTOutGain[0]

Refer to Table 10-1 for fine tune output gain. This gain is applied to the output data of processor channel C1.

10.8.1.7 FTInGain0

Address	Access Mode	Value At Reset	Nominal Value
0x146E	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	FTInGain[5]	FTInGain[4]	FTInGain[3]	FTInGain[2]	FTInGain[1]	FTInGain[0]

Refer to Table 10-1 for fine tune input gain. This gain is applied to CODEC PCM output data. This gain can be also adjusted to consider the power requirement of the half acoustic echo canceller.

10.8.1.8 FTOutGain0

Address	Access Mode	Value At Reset	Nominal Value
0x146F	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	FTOutGain[5]	FTOutGain[4]	FTIOutGain[3]	FTOutGain[2]	FTOutGain[1]	FTOutGain[0]

Refer to Table 10-1 for fine tune output gain. This gain is applied to CODEC PCM input data. This gain can be also adjusted to consider the power requirement of the half acoustic echo canceller.

Table 10-1： Fine-tuning input, output gain (decimal index). The 5-bit numbers allow +/- 12 dB adjustment in 0.5 dB steps and hard mute.

FT In/out Gain [4:0]	Gain Value	FT In/out Gain [4:0]	Gain Value
0x00	0 dB	**0x19**	-0.5 dB
0x01	0.5 dB	**0x1A**	-1.0 dB
0x02	1.0 dB	**0x1B**	-1.5 dB
0x03	1.5 dB	**0x1C**	-2.0 dB
0x04	2.0 dB	**0x1D**	-2.5 dB
0x05	2.5 dB	**0x1E**	-3.0 dB
0x06	3.0 dB	**0x1F**	-3.5 dB
0x07	3.5 dB	**0x20**	-4.0 dB
0x08	4.0 dB	**0x21**	-4.5 dB
0x09	4.5 dB	**0x22**	-5.0 dB
0x0A	5.0 dB	**0x23**	-5.5 dB
0x0B	5.5 dB	**0x24**	-6.0 dB
0x0C	6.0 dB	**0x25**	-6.5 dB
0x0D	6.5 dB	**0x26**	-7.0 dB
0x0E	7.0 dB	**0x27**	-7.5 dB
0x0F	7.5 dB	**0x28**	-8.0 dB
0x10	8.0 dB	**0x29**	-8.5 dB
0x11	8.5 dB	**0x2A**	-9.0 dB
0x12	9.0 dB	**0x2B**	-9.5 dB
0x13	9.5 dB	**0x2C**	-10.0 dB
0x14	10.0 dB	**0x2D**	-10.5 dB
0x15	10.5 dB	**0x2E**	-11.0 dB
0x16	11.0 dB	**0x2F**	-11.5 dB
0x17	11.5 dB	**0x30**	-12.0 dB
0x18	12.0 dB	**0x3F**	**Mute**

11. PROCESSOR INTERFACE

11.1 Overview

The Processor Interface controls reads and writes made by the Processor to the on-chip RAM and on-chip registers.

11.2 Functionality

Figure 11-1 shows the processor interface block diagram.

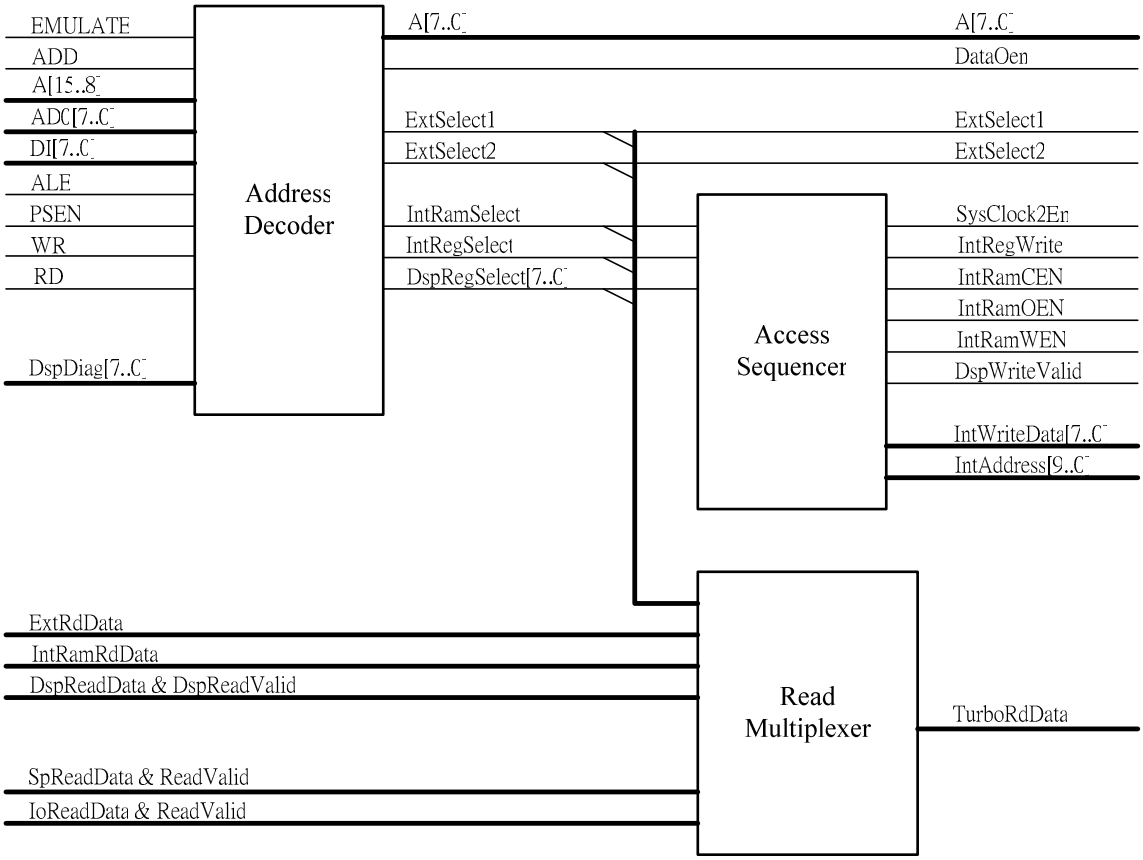


Figure 11-1 Illustration of the Processor Interface

11.3 Processor Access Sequencer

The Processor Access Sequencer has 2 functions：

- Internal Register access sequencing
- On-Chip RAM access sequencing

External RAM accesses, external ROM accesses and internal register reads are performed directly by the 8032Turbo, the Address Decoder and Read Multiplexer. No action is required by the Processor Access Sequencer.

The operation of the Processor Access Sequencer for internal register writes is shown in Figure 11-2.

Note that：

- The sequence of a register write is not affected by the setting of STRECH.
- The Internal Register Clock Enable signal SysClock2En is active for 4 cycles to allow internal events to be scheduled after a

register writes.

- The Internal Address Bus IntAddress is a latched version of the Processor Address bus, updated when an internal accesses is required. This reduces internal transitions on the chip to save power.

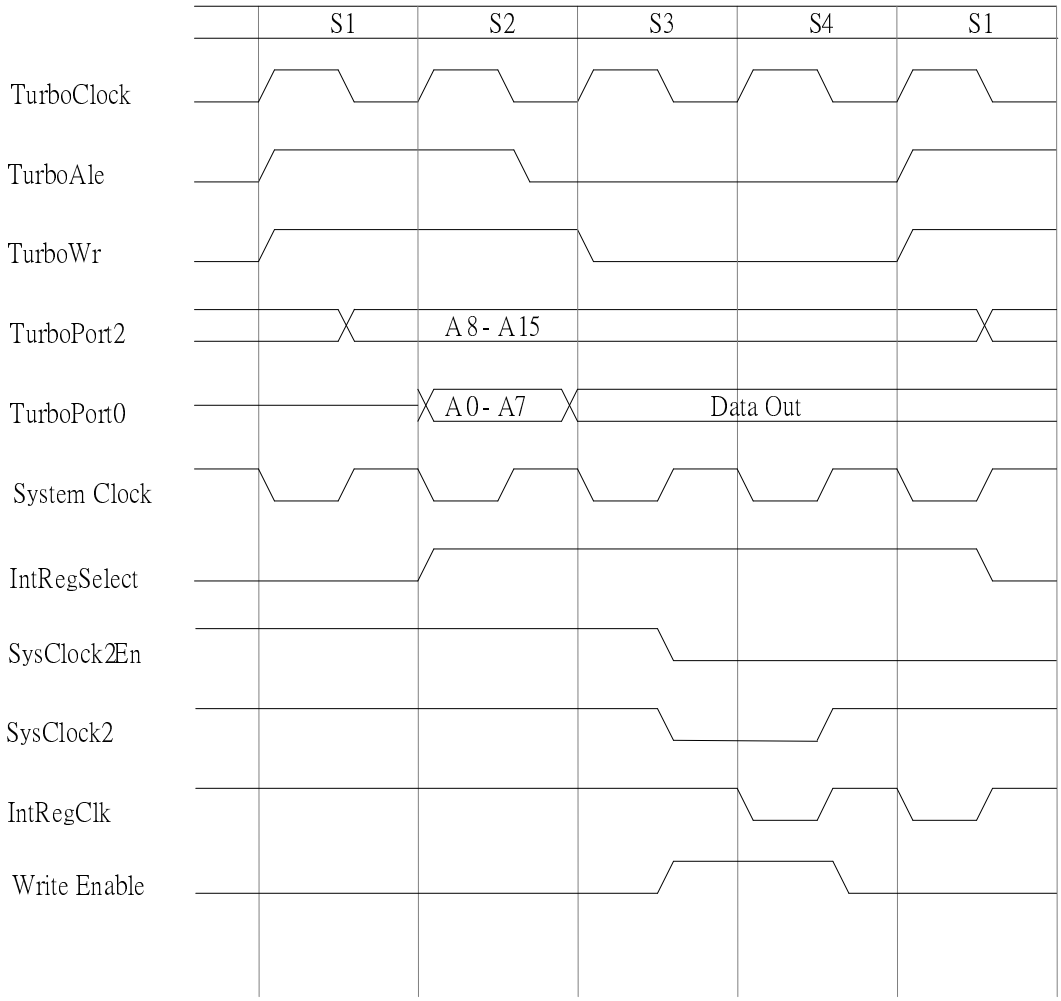


Figure 11-2 Timing of Internal Register Writes

The operation of the Processor Access Sequencer for access to the On-Chip RAM is shown in Figure 11-3.
Note that：

- The On-Chip RAM is a clocked-synchronous RAM.
- The data read out of the On-Chip RAM is latched in the Processor Interface.

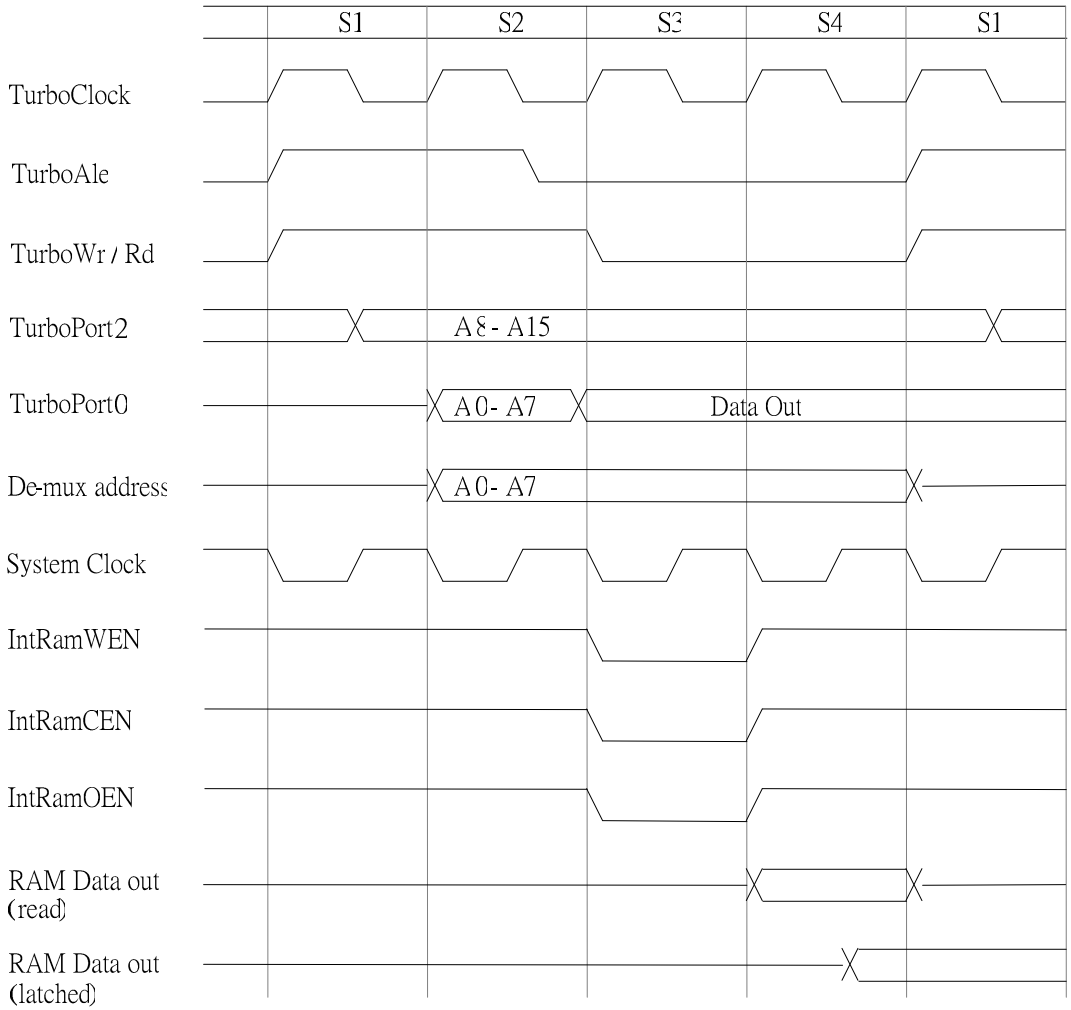


Figure 11-3 Timing of On-Chip RAM Access

11.4 Read Multiplexer

The Read Multiplexer multiplexes the following data onto the internal 8032Turbo data bus:

- On-chip registers
- On-Chip RAM
- Speech Processor Registers
- Off-Chip Bus Interface

Each function performs local address decoding for both Reads and Writes. For register reads, each block multiplexes the addressed register onto a single output bus and asserts a Data Valid signal.

All internal modules present zero on the read data buses when not selected.

In the case of support logic, processor interface, speech interface and interface logic these modules decode a lower part of the address bus, so may present data out at various points in the memory map.

For other blocks all the decoding is done within the processor interface.

A data inputs are qualified with appropriate Address Decoder outputs. This ensures that only the required sub-module data is presented to the 8032Turbo.

11.5 Processor Interface Control Registers

11.5.1 AuxOpPort

Address	Access Mode	Value At Reset	Nominal Value
0x1470	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	CS1R2	CS1R1	CS1R0	AuxOp Port1En	AuxOpPort1	AuxOp Port0En	AuxOpPort0

CS1 and CS2 can be set as general output port, 0x1470 bit1 and bit3 enable this function independently. AuxOpPort0 means CS1 and AuxOpPort1 means CS2. When you enable the general output function, the CS1/CS2 will be not in address decode mode. Figure 11-4 shows /CS1 & /CS2 output multiplexer.

AuxOpPort0 The AuxOpPort data bits contain TRUE data.
AuxOpPort0En When set, enable the AuxOpPort 0.
AuxOpPort1 The AuxOpPort data bits contain TRUE data.

AuxOpPort1En When set, enable the AuxOpPort 1.

The AuxOpPort enables are active high.

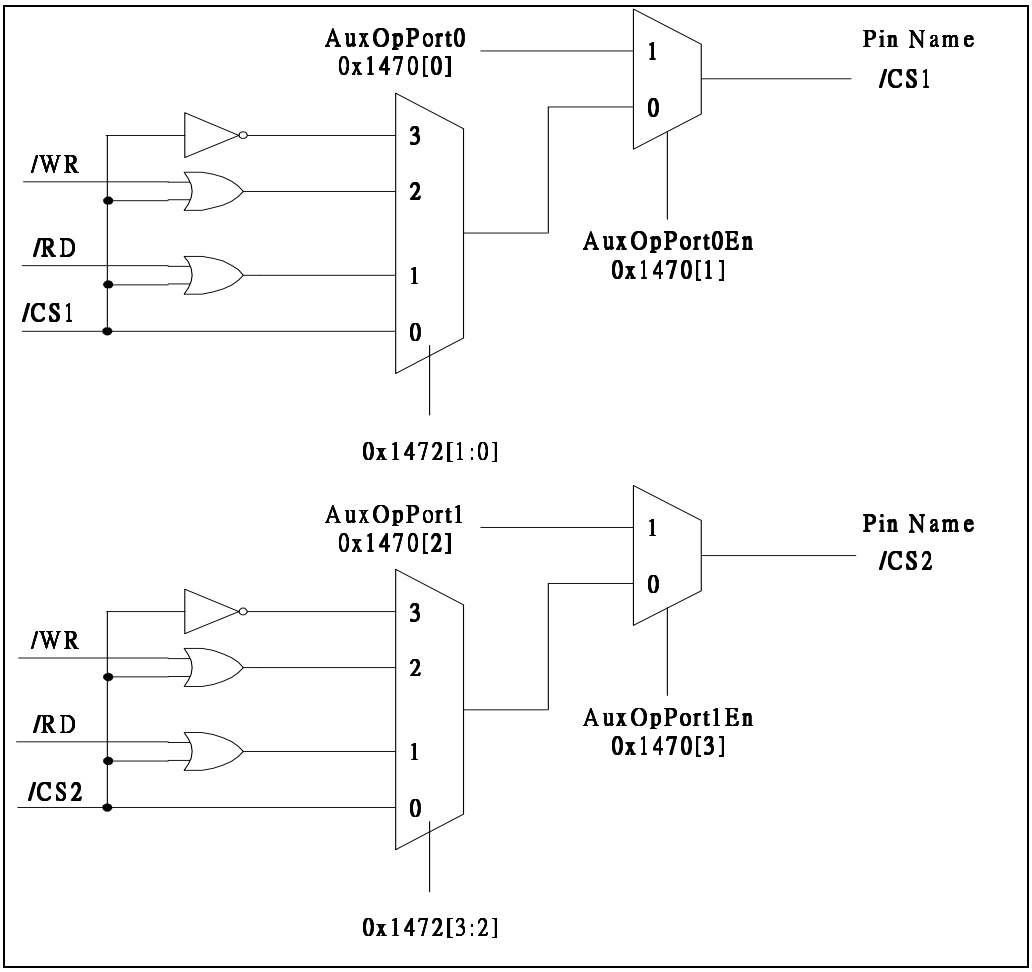


Figure 11-4 /CS1 & /CS2 output multiplexer

The CS1 range is defined as:

CS1R2	CS1R1	CS1R0	Depth	Address Range	
0	0	0	4KB	0x8000	0x8FFF
0	0	1	8KB	0x8000	0x9FFF
0	1	0	12KB	0x8000	0xAFFF
0	1	1	16KB	0x8000	0xBFFF
1	0	0	20KB	0x8000	0xCFFF
1	0	1	24KB	0x8000	0xDFFF
1	1	0	28KB	0x8000	0xEFFF
1	1	1	32KB	0x8000	0xFFFF

11.5.2 DiagSel

Address	Access Mode	Value At Reset	Nominal Value
0x1471	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

11.5.3 Diag_CS

Address	Access Mode	Value At Reset	Nominal Value
0x1472	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	CS2R2	CS2R1	CS2R0	CS2_Sel[1]	CS2_Sel[0]	CS1_Sel[1]	CS1_Sel[0]

CS1 & CS2 can be selected output for setting the bits

CS1 & CS2 output multiplexer (See Figure 11-4)

CS1[1:0] / CS2[3:2]	Output
00	CS1 / CS2
01	CS1|RD / CS2|RD
10	CS1|WD / CS2 |WD
11	~((CS 1 | RD) & (CS1 | WR)) / ~((CS 2 | RD) & (CS2 | WR))

The CS2 range is defined as:

CS2R2	CS2R1	CS2R0	Depth	Address Range	
0	0	0	4KB	0xF000	0xFFFF
0	0	1	8KB	0xE000	0xFFFF
0	1	0	12KB	0xD000	0xFFFF
0	1	1	16KB	0xC000	0xFFFF
1	0	0	20KB	0xB000	0xFFFF
1	0	1	24KB	0xA000	0xFFFF
1	1	0	28KB	0x9000	0xFFFF
1	1	1	32KB	0x8000	0xFFFF

CS1 and CS2 can address 32 K totally. So for example, you set CS2 for addressing 12 KB, then CS1 only address 20KB .
CS1: 0x8000H~ 0xCFFFH ; CS2 : 0xD0000H~0xFFFFH.

11.5.4 Diag_CS3

Address	Access Mode	Value At Reset	Nominal Value
0x1473	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RD_WR_BLK	CS2_WAIT _EN	CS3_SEL[1]	CS3_SEL[0]	PWR_SAVE[1]	PWR_SAVE[0]

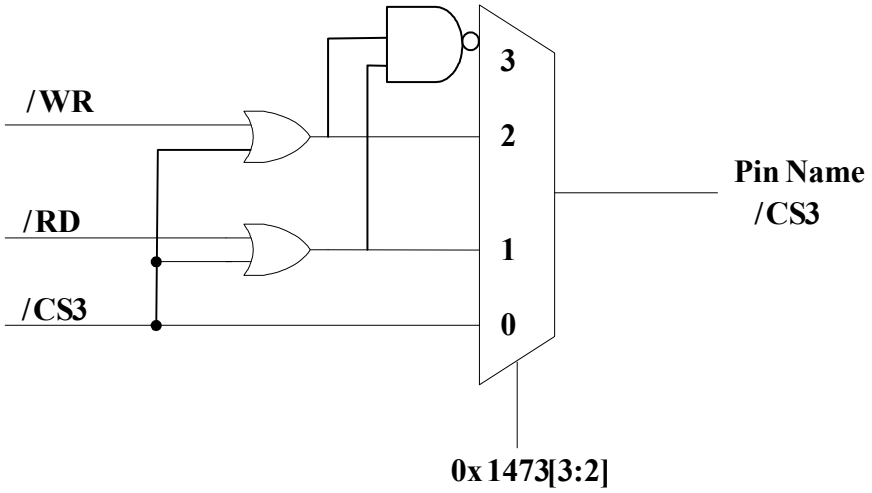


Figure 11-5 CS3 Output multiplexer

CS3 output multiplexer is shown in Figure 11-5. **Address mapping range of CS3 is 0x2000~0x5FFF**

CS3_sel[1:0]	Output
00	CS3
01	CS3 | RD
10	CS3 | WD
11	~((CS 3 | RD) & (CS3 | WR))

CS2_WAIT_EN This is a wait state enable bit for CS2 controlled device. When set this bit, the WR/RD duration to CS2 controlled device will last from 4 clock cycles to 8 clock cycles.

RD_WR_BLK When set this bit, the external RD/WR signal will not active (blocked) when access internal RAM/register (0x0000 to 0x1FFF and 0x6000 to 0x7FFF), the default is not blocked.

PWR_SAVE [1:0] You can set PWR_SAVE [1:0] to control AD/ADDR bus output state for I/O power save purpose.

PWR_SAVE[1:0]	AD/ADDR bus
00	No power save feature.
01	AD/ADDR bus only active when T8032 RD/WR in the Mask ROM mode.
10	AD/ADDR bus only active when T8032 RD/WR external device (0x8000~0xFFFF),in the Mask ROM mode.
11	AD/ADDR bus always inactive.

11.5.5 Multiplier_Enable

Address	Access Mode	Value At Reset	Nominal Value
0x1474	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	Mul8x8_en

Mul8x8_en This is an enable bit of a fast 8x8 multiplier in T8032.When set this bit, a fast T8032 internal 8x8 multiplier will be active otherwise the original T8032 add-shift multiplier is the default choice.

11.6 In System Programming Mode

In System Programming mode is designed for fast program on board flash. Flash type includes 29, 39 and 49 series. The chip is provided two ISP entry modes. One is hardware setting and the other is software command mode.
This function comes with the PC software, which transfer the binary code to internal T8032 to program the external ROM flash. ISP function use internal T8032 UART or USB port to transfer data, the default baud rate of the UART port is 9600bps, which can be set by remote PC program. There are four baud-rates for selection, 9600bps, 19200bps, 28800bps and 57600bps. The double-speed MCU chip (2x), you can select optional 115200bps for flash program.

11.6.1 Hardware Setting Usage

In the initial power-up state, the /CS2 pin will replaced as ISP function hardware setting pin. When /CS2 pin set to low and re-power up the system, the chip will execute the internal ISP code, and wait for PC command and binary data to update the external ROM flash. If the /CS2 is set to output purpose pin (the pin is default pull-up), this chip will in normal mode. The flash needed an external write signal. The ISP_WR pin of the chip needs to connect to the /WR pin of the external Flash and which pin only active in ISP operation.

11.6.2 Software Command Usage

This ISP function can provide the system program update from the internal USB or UART ports with software command and don't need any hardware modification. Therefore the baseband chip doesn't need extra circuit to support this function. Figure 11-6 is shown the function description and specification.

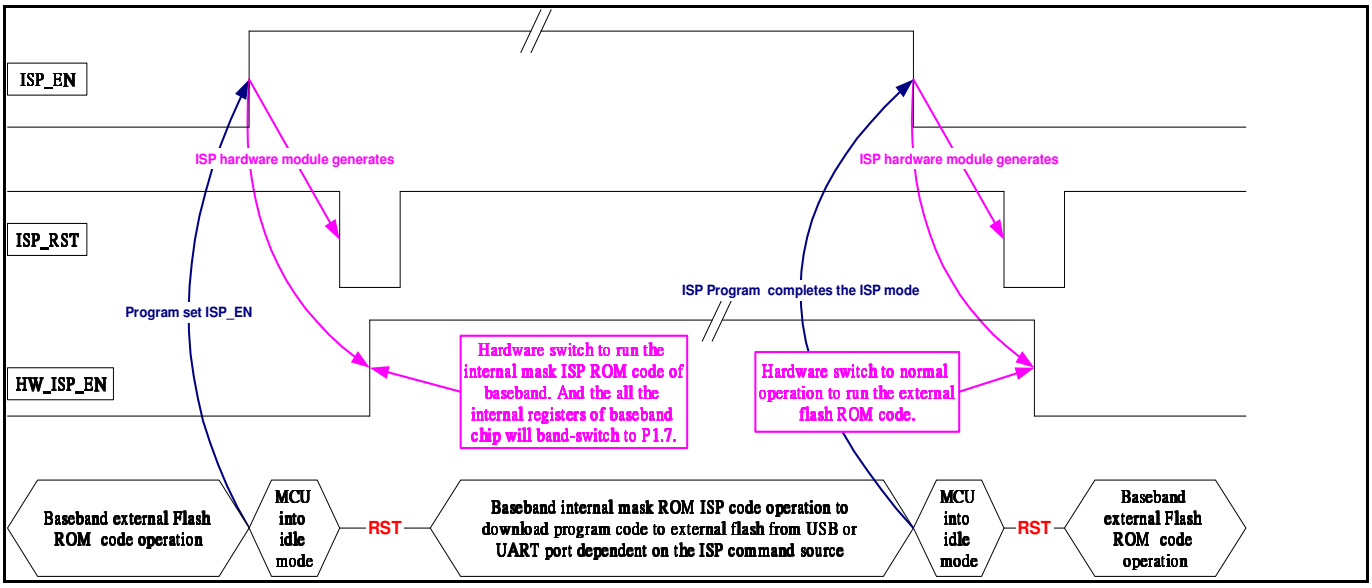


Figure 11-6 The software ISP operation procedure

11.6.3 ISP_CTRL (Hardware & Watchdog Reset Control Register)

Address	Access Mode	Value At Reset	Nominal Value
0x1900	RW	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISP_EN	Reserved	Reserved	Reserved	Reserved	Reserved	USB_ISP	UART_ISP

This ISP control register is provided the In-system-programming function to update the system program code without modification hardware. This function can be enabled by the bit 7 of ISP_CTRL control register. And the enable command which is come from the internal UART port or USB interface.

UART_ISP This bit is reserved for ISP mask rom program recognition which type ISP mode is enabled. When ISP enabled command is come from internal UART port. Then the normal program will set this bit for recognition in ISP mode period before enabled ISP_EN bit. And download program data will come from UART port in the ISP programming period.

USB_ISP The bit function is the same as UART_ISP.

ISP_EN When set this bit will enable ISP mode to program the external flash ROM via the internal USB interface or UART port.

11.6.4 Specific Register

Address	Access Mode	Value At Reset	Nominal Value
0x1901	RW	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Blocked (for test modes)	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

11.7 MASK ROM Mode

Mask ROM Mode is designed to use the internal mask ROM, besides this MCU chip also can disable the internal mask ROM to use external flash ROM. Although MCU chip provide ISP mode and MASK ROM mode but you cannot use it simultaneously. Each function is independent function.

11.7.1 Usage

When set EXT_ROM pin to low, the chip will execute the internal mask ROM code. When set EXT_ROM pin to high, the chip will execute the external flash ROM code.

12. SPEECH PROCESSOR

The Speech Processor provides a complete implementation, including :

- 4 duplex channels
- 1 channel Echo Canceller
- A Mixer Block
- Programmable Tone Generators

The Speech Processor supports A-law, µ-law and 16-bits linear PCM formats. Echo canceller channels support 16 bits linear PCM only.

The Speech Processor is implemented by an optimized micro-coded DSP, an external FIR Filter Engine and one digital gain multiplexer. The architecture of the Speech Processor can be shown in Figure 12-1.

The Microcode DSP Core:

- Performs Tone Generation
- Performs PCM Mixing

The FIR Engine:

- Performs real-time Echo Estimation
- Implements Network Echo Suppression
- Calculates the Echo Cancellation filter coefficients
- Performs intermediate calculations on the Echo Estimation error

12.1 Transcoder DSP

The Transcoder DSP is a low power implementation and has the following features:

- Low power consumption and low gate count
- Group delay under 14 µs / channel
- DTMF and call progress tones
- Sidetone generation and Volume control
- Requires only 4.1 MIPS per channel

The Transcoder DSP supports A-law, µ-law and 16-bits linear PCM formats. Format selection is programmable on a by-channel basis.

The signal flow (per channel) is shown in Figure 12-1 below :

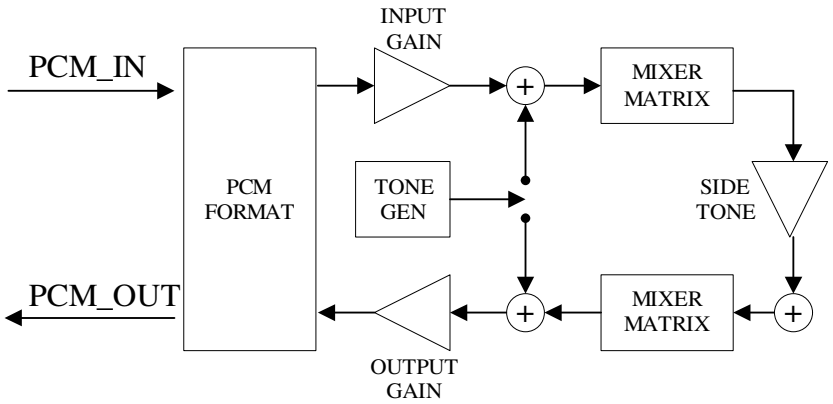


Figure 12-1 Transcoder signal flow

There are dual-tone generators for each PCM channel. These can generate DTMF and common signaling tones, as well as user notification tones. The tones may be added in either direction. A mixer function is enabled by setting 1401[0]. Four full-duplex PCM

channels can be connected / mixed together in any combination. This function is controlled by programmable registers. Moreover, the speech logic interface (which is not needed by the CODEC) of four channels must be enabled.

12.2 The Description of the Activation Registers

12.2.1 MIXER_EN

Address	Access Mode	Value At Reset	Nominal Value
0x1401	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	MIXER_EN

MIXER_EN Set to enable the mixer block.

12.2.2 SPEECH LOGIC_EN

Address	Access Mode	Value At Reset	Nominal Value
0x1420	R/W	0x04	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	SPEECH LOGIC_EN

SPEECH LOGIC_EN Set to enable speech logic interface (which is not needed by the CODEC) of four channels.

12.3 The Description of Transcoder DSP Registers

The transcoder block is programmed via microprocessor accessible programming registers.

All registers allow read/write access and reset to zero except as noted. All bits not specified below are reserved or blocked and should only be written with zeros. Unspecified bits read back zero.

The transcoder registers are divided into `Global registers' and `Channel-specific registers'.

Global registers：

- Consist of SideTone (0x148D) and Lookback_EN (0x148E) registers.

Channel-specific registers：
Channel-specific registers appear in four groups at offsets of sixteen bytes.

- Channel 0 registers appear at addresses 0x1480 -> 0x148C
- Channel 1 registers appear at addresses 0x1490 -> 0x149C
- Channel 2 registers appear at addresses 0x14A0 -> 0x14AC
- Channel 3 registers appear at addresses 0x14B0 -> 0x14BC

12.3.1 Connect0

Address	Access Mode	Value At Reset	Nominal Value
0x1480	R/W	0x01	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCM channel 3	PCM channel 2	PCM channel 1	PCM channel 0	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	* Blocked (for test modes)

Specify mixing among four PCM channels. This register enables the connections of each PCM channels.
Bits [7:4] correspond to PCM channels 3:0.
* Blocked (for test modes) must be set to 1.

When the value of the bit is set to 1, it enables the addition of the corresponding channel in mixing. An additive connection is set up between the specified channels.

12.3.2 Specified Register

Address	Access Mode	Value At Reset	Nominal Value
0x1481	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	Blocked (for test modes)	Blocked (for test modes)

12.3.3 Specified Register

Address	Access Mode	Value At Reset	Nominal Value
0x1482	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	Blocked (for test modes)

12.3.4 Specified Register

Address	Access Mode	Value At Reset	Nominal Value
0x1483	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	Blocked (for test modes)

12.3.5 PCMmode0

Address	Access Mode	Value At Reset	Nominal Value
0x1484	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	COMP_FORMAT	PCM_LINEAR

PCM_LINEAR =1, PCM port 0 operates in 16-bit linear mode.
=0, 8-bit compressed PCM.

COMP_FORMAT If PCM port 0 is in compressed mode,
=1, A-law,
=0, μ -law

12.3.6 InputGain0

Address	Access Mode	Value At Reset	Nominal Value
0x1485	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	InputGain[3]	InputGain[2]	InputGain[1]	InputGain[0]

InputGain[3:0] PCM input gain table is listed as below Table 12-1. This gain is applied directly to the PCM input value.

12.3.7 OutputGain0

Address	Access Mode	Value At Reset	Nominal Value
0x1486	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	OutputGain[3]	OutputGain[2]	OutputGain[1]	OutputGain[0]

OutputGain[3:0] PCM output gain table is listed as below Table 12-2. This gain is applied after the Mixer Matrix and tone generation.

12.3.8 ToneFreqA0

Address	Access Mode	Value At Reset	Nominal Value
0x1488	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ToneFreqA							

Frequency of tone A = ToneFreqA * 15.625 (Hz)

12.3.9 ToneFreqB0

Address	Access Mode	Value At Reset	Nominal Value
0x1489	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ToneFreqB							

Frequency of tone B = ToneFreqB * 15.625 (Hz)

12.3.10 ToneVolA0

Address	Access Mode	Value At Reset	Nominal Value
0x148A	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	ToneVolA[4]	ToneVolA[3]	ToneVolA[2]	ToneVolA[1]	ToneVolA[0]

Tone level is listed as below Table 12-3 for tone generator A.

12.3.11 ToneVolB0

Address	Access Mode	Value At Reset	Nominal Value
0x148B	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	ToneVolB[4]	ToneVolB[3]	ToneVolB[2]	ToneVolB[1]	ToneVolB[0]

Tone level is listed as below Table 12-3 for tone generator B.

12.3.12 ToneEna0

Address	Access Mode	Value At Reset	Nominal Value
0x148C	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	Tx_tone	Rcv_tone

Rcv_tone =1, add tone generators to the receiving (PCM_OUT) path. Receive tones are added just before the PCM output gain stage.

Tx_tone =1, add tone generators to the transmitting (PCM_IN) path. Transmit tones are added just after the PCM input gain stage.

WARNING: enabling tones in both directions at the same time causes the output frequencies to double.

12.3.13 SideTone

Address	Access Mode	Value At Reset	Nominal Value
0x148D	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	SideTone[4]	SideTone[3]	SideTone[2]	SideTone[1]	SideTone[0]

SideTone[4:0] Side tone gain is listed as below Table 12-4. This is applied to all active PCM channels between the Mixer Matrix and PCM formatting. Please refer to 0x14AF to enable the active sidetone channel.
SideTone[4:0] =0, to disable side tone.

12.3.14 Loopback_EN

Address	Access Mode	Value At Reset	Nominal Value
0x148E	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
* Blocked (for test modes)	RESERVED	RESERVED	RESERVED	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Loopback_EN

Loopback_EN =1, loopback behind the side tone function in the transmitting (PCM_IN) path.
* Blocked (for test modes) must be set to 1.

12.3.15 Specified Register

Address	Access Mode	Value At Reset	Nominal Value
0x148F	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Blocked (for test modes)							

12.3.16 Connect1 ~ ToneEna1

Address	Access Mode	Value At Reset	Nominal Value
0x1490 ~ 0x149C	R/W	0x00	

The functions are the same as channel 0.

12.3.17 Connect2 ~ ToneEna2

Address	Access Mode	Value At Reset	Nominal Value
0x14A0 ~ 0x14AC	R/W	0x00	

The functions are the same as channel 0.

12.3.18 SideToneChannel_Ena

Address	Access Mode	Value At Reset	Nominal Value
0x14AF	R/W	0x01	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	SideTone_ch3	SideTone_ch2	SideTone_ch1	SideTone_ch0

The register can enable side tone individually for the each active pcm channel.

12.3.19 Connect3 ~ ToneEna3

Address	Access Mode	Value At Reset	Nominal Value
0x14B0 ~ 0x14BC	R/W	0x00	

The functions are the same as channel 0.

12.4 PCM Mixer Matrix

The registers Connect0-3 specify channels which should be connected together and enable the corresponding PCM channels. The connection registers of each specified PCM channels can be set to the same value simultaneously. The result is the same that one of each registers be set. For example, The PCM0 and PCM1 channels need to be connected. So the 1480 and 1490 can be set to 31. The effect is the same that only 1480 or 1490 is set.

12.5 Gain Tables

There are four gain functions in this block: PCM I/O gain, side tone gain and tone gain (level).

Table 12-1 The PCM Input gain is provided to allow minor corrections for board-level analogue gain problems. The 4-bit numbers allow +/- 10 dB adjustments and hard mute.

InputGain (3:0)	Nominal gain	Actual gain
0x00	0 dB	0 dB
0x01	+1 dB	+1.0
0x02	+2 dB	+2.0
0x03	+3 dB	+2.8
0x04	+4 dB	+4.2
0x05	+6 dB	+6.0
0x06	+8 dB	+8.0
0x07	+10 dB	+9.5
0x08	-∞ (Hard mute)	-∞
0x09	-10 dB	-10.1
0x0A	-8 dB	-8.5
0x0B	-6 dB	-6.0
0x0C	-4 dB	-4.1
0x0D	-3 dB	-3.2
0x0E	-2 dB	-1.8
0x0F	-1 dB	-1.2

Table 12-2 The PCM Output gain is provided to allow minor corrections for board-level analogue gain problems. The 4-bit numbers allow +/- 16 dB adjustments and hard mute.

OutputGain(3:0)	Nominal gain	Actual gain
0x00	0 dB	0 dB
0x01	+1.5 dB	+1.9
0x02	+3 dB	+3.5
0x03	+5 dB	+4.9
0x04	+7 dB	+7.0
0x05	+10 dB	+9.9
0x06	+13 dB	+13.5
0x07	+16 dB	+15.6
0x08	-∞ (Hard mute)	-∞
0x09	-16 dB	-18.1
0x0A	-13 dB	-12.0
0x0B	-10 dB	-8.5
0x0C	-7 dB	-6.0
0x0D	-5 dB	-4.1
0x0E	-3 dB	-2.5
0x0F	-1.5 dB	-1.2

Table 12-3 Tone levels are specified in linear values, referenced to ½ of the max PCM level (+3.17 dBm0). Tone level = -2.85 dBm0 + 20 log10 (TONEVOL / 32). Because there are 32 legal values, the following table contains only example values.

Tone Generator Gain Value					
TONEVOLx(4:0)	**Actual level (dBm0)**	**TONEVOLx(4:0)**	**Actual level (dBm0)**	**TONEVOLx(4:0)**	**Actual level (dBm0)**
0x00	Disable	**0x0B**	-12.1251	**0x16**	-6.1045
0x01	-32.9530	**0x0C**	-11.3694	**0x17**	-5.7184
0x02	-26.9324	**0x0D**	-10.6741	**0x18**	-5.3488
0x03	-23.4106	**0x0E**	-10.0304	**0x19**	-4.9942
0x04	-20.9118	**0x0F**	-9.4312	**0x1A**	-4.6535
0x05	-18.9736	**0x10**	-8.8706	**0x1B**	-4.3257
0x06	-17.3900	**0x11**	-8.3440	**0x1C**	-4.0098
0x07	-16.0510	**0x12**	-7.8475	**0x1D**	-3.7050
0x08	-14.8912	**0x13**	-7.3779	**0x1E**	-3.4106
0x09	-13.8681	**0x14**	-6.9324	**0x1F**	-3.1258
0x0A	-12.9530	**0x15**	-6.5086		

Table 12-4 The side tone gain is adjustable from -32 dB to 0 dB in 1 dB steps. Setting this register to 0 disables side tone.

Side Tone Gain value			
Index	**Value**	**Index**	**Value**
0x00	**Mute**	**0x10**	-15 dB
0x01	0 dB	**0x11**	-16 dB
0x02	-1 dB	**0x12**	-17 dB
0x03	-2 dB	**0x13**	-18 dB
0x04	-3 dB	**0x14**	-19 dB
0x05	-4 dB	**0x15**	-20 dB
0x06	-5 dB	**0x16**	-21 dB
0x07	-6 dB	**0x17**	-22 dB
0x08	-7 dB	**0x18**	-23 dB
0x09	-8 dB	**0x19**	-24 dB
0x0A	-9 dB	**0x1A**	-25 dB
0x0B	-10 dB	**0x1B**	-26 dB
0x0C	-11 dB	**0x1C**	-28 dB
0x0D	-12 dB	**0x1D**	-30 dB
0x0E	-13 dB	**0x1E**	-32 dB
0x0F	-14 dB	**0x1F**	-36 dB

13. ECHO CANCELLER

13.1 Half AEC Block Diagram

The acoustics echo cancellation unit removes the echo signal inserted by the speaker and space.

Figure 13-1 illustrates the block diagram of the Half Acoustics Echo Canceller in the Speech Processor.

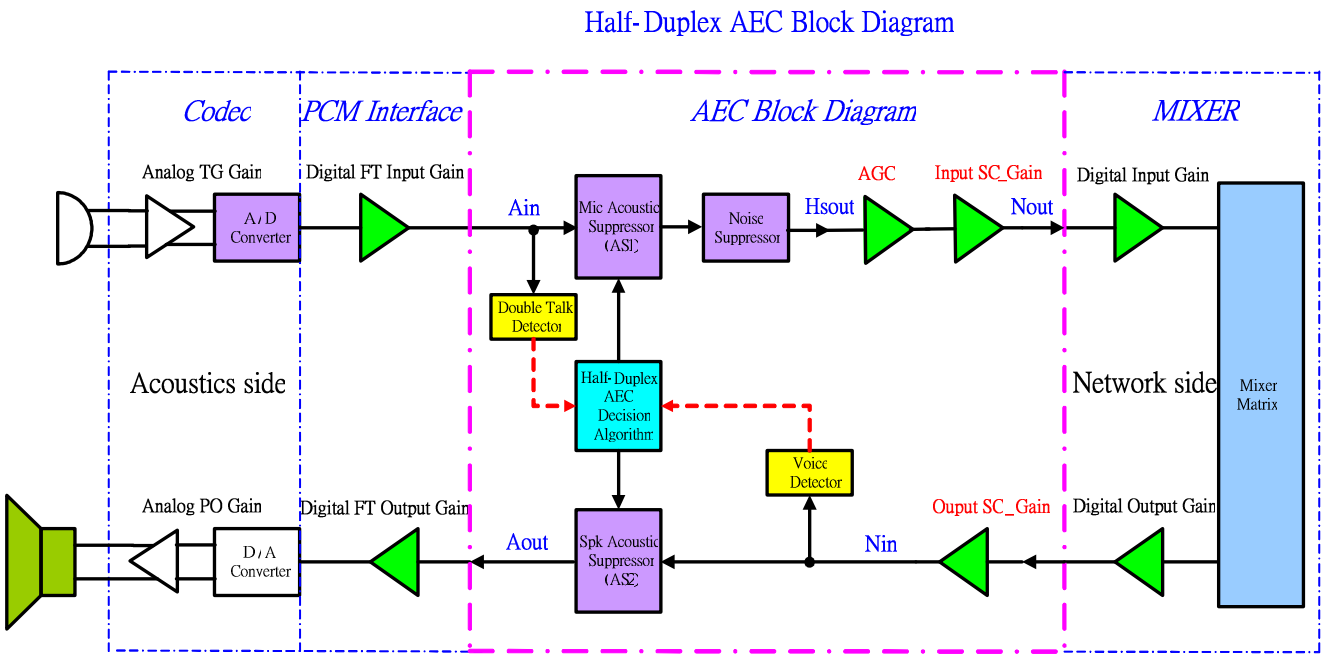


Figure 13-1 The signal flow through the Acoustics Echo Canceller in the Speech Processor

13.1.1 Acoustics Suppression

When enabled (and so, switched into the network output data path) the acoustic suppression unit will insert a configurable attenuation factor into the network output path. The attenuation will switch between a maximum and minimum value depending on the presence or absence of speech on the network output data path. When speech is present the attenuation will converge towards the minimum value. When speech is absent the attenuation will converge towards the maximum value. The attenuation factor will not switch abruptly between these two factors but will exponentially converge from one to the other.

When enabled the network output data path will include the following arithmetic unit：

$$Nout \propto Nout * AS_ATTENUATION$$

13.1.2 Network Power Estimation

To detect the double talk condition an estimate of the long term network power is required.

The long term network power is estimated with the following arithmetic unit：

$$Pnin_n \propto Pnin_{n-1} + \begin{pmatrix} \left(\left|Nin_n\right| * 2^{VD_LONG_NETWORK_ATTACK_TC-16}\right) \\ -\left(Pnin_{n-1} * 2^{VD_LONG_NETWORK_ATTACK_TC-16}\right) \\ +\left(Vd_Long_Network_Threshold * 2^{VD_LONG_NETWORK_ATTACK_TC-17}\right) \end{pmatrix}$$

The short term network power is estimated with the following arithmetic unit：

$$PninShort_n \propto PninShort_{n-1} + \begin{pmatrix} \left(\left|Nin_n\right| * 2^{VD_SHORT_NETWORK_ATTACK_TC-16}\right) \\ -\left(PninShort_{n-1} * 2^{VD_SHORT_NETWORK_ATTACK_TC-16}\right) \end{pmatrix}$$

The deviation term network power is estimated with the following arithmetic unit：

$$PninDev_n \propto \left| \; Pnin_n - Cut_Off_Network_Power - PninShort_n \; \right|$$

13.1.3 Acoustic Power Estimation

This speech will have originated at the near end and does not correspond to a reflected echo signal. Speech is deemed to occur if the long term acoustic power exceeds a predetermined threshold or if the short term acoustic power exhibits sudden variations. If speech is being carried over both the network and acoustic interfaces then the double talk condition occurs.

The long term acoustic power is estimated with the following arithmetic unit：

$$Pain_n \propto Pain_{n-1} + \begin{pmatrix} \left(\left|Ain_n\right| * 2^{DT_LONG_ACOUSTIC_ATTACK_TC-16}\right) \\ -\left(Pain_{n-1} * 2^{DT_LONG_ACOUSTIC_ATTACK_TC-16}\right) \end{pmatrix}$$

The short term acoustic power is estimated with the following arithmetic unit：

$$PainShort_n \propto PainShort_{n-1} + \begin{pmatrix} \left(\left|Ain_n\right| * 2^{DT_SHORT_ACOUSTIC_ATTACK_TC-16}\right) \\ -\left(PainShort_{n-1} * 2^{DT_SHORT_ACOUSTIC_ATTACK_TC-16}\right) \end{pmatrix}$$

13.1.4 Auto Gain Control

The short term cancelled power is estimated with the following arithmetic unit：

$$PgShort_n \propto PgShort_{n-1} + \begin{pmatrix} \left(|Hsout| * 2^{AGC_ST_ATTACK_TC-16}\right) \\ -\left(PgShort_{n-1} * 2^{AGC_ST_ATTACK_TC-16}\right) \end{pmatrix}$$

The AGC module is operated with the following algorithm：

If $\left(|Hsout| > PgShort\right)$
then $PgShort = |Hsout|$

If $PgShort < AGC_NOISE_THRESHOLD$
then $Sg = 1$
Else $Sg = \dfrac{AGC_THRESHOLD}{PgShort}$

If $Sg > AGC_MAX_SG$
then $Sg = AGC_MAX_SG$

The long term AGC module gain is estimated with the following arithmetic unit：

$$Sglong_n \propto Sglong_{n-1} + \begin{pmatrix} \left(Sg * 2^{AGC_LG_ATTACK_TC-16}\right) \\ -\left(Sglong_{n-1} * 2^{AGC_LG_ATTACK_TC-16}\right) \end{pmatrix}$$

If $Sglong > Sg$
then $Sglong = Sg$

13.2 The Software Interface of Speech Processor

The following registers are used to configure the echo canceller. All registers may be both read and written by software. The width of each location will be a byte within the memory map. Some locations may have unused bits which will be returned undefined values on a read cycle. Information in these bit positions will be discarded on write cycles.

The registers within the echo cancellation unit may be segmented into two classes：Activation Registers and Performance Adjustment Registers. An overview of each register class and nominal values to program each register is presented.

13.3 Activation Registers

13.3.1 UP_CONFIG

Address	Access Mode	Value At Reset	Nominal Value
0x14C0	R/W	0x00	0x82

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AGC	RESERVED	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	AS1_ENA	Blocked (for test modes)

AS1_ENA When set, the acoustic suppression (AS1) function will be enabled.
AGC When set, enable AGC function.
* The acoustic suppression (AS2) function is always enabled.

13.3.2 UP_RESET

Address	Access Mode	Value At Reset	Nominal Value
0x14C1	R/W	0x08	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Blocked (for test modes)	RESERVED	RESERVED	AEC_Reset	Power Down	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)

Power Down When set, Power down the AEC unit to save power. Speech signal will bypass AEC module.
AEC_Reset When set, Setting this bit will cause the AEC registers, including the activation registers and performance adjustment registers, to be reseted to their hardware reset values.

13.3.3 EC_BELTA

Address	Access Mode	Value At Reset	Nominal Value
0x14C2	R/W	0x03	0xE0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NS_Enable	NetAcIdle	* Blocked (for test modes)	Absolute	Blocked (for test modes)			

Absolute When set, the double talk detection algorithm is based on absolute value of Acoustic power.
NetAcIdle When set, the double sides don't have any voice; it will mute in Network side.
NS_Enable If this bit is set "0", noise suppressor is by-passed. If this bit is set "1", then noise suppressor is enabled.
* Blocked (for test modes) must be set to 1.

13.3.4 Specific Register

Address	Access Mode	Value At Reset	Nominal Value
0x14C3	R/W	0x03	0x03

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	Blocked (for test modes)			

13.4 Performance Adjustment Registers

13.4.1 Acoustic Suppressor Register

13.4.1.1 AS_BUILD_UP_TIME

Address	Access Mode	Value At Reset	Nominal Value
0x14C4	R/W	0x07	0x55

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AS2_BUILD_UP_TIME				AS1_BUILD_UP_TIME			

Control register for acoustic suppression factor convergence towards target.
Raising (lowering) the value of this field will lower (raise) the inertial delay present when the acoustic suppression unit responds to the presence or absence of speech.

13.4.1.2 AS_MAX_ATTEN

Address	Access Mode	Value At Reset	Nominal Value
0x14C5 - 0x14C6	R/W	0x1CA8	0x0200

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
C5	AS1 & AS2_MAX_ATTEN							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C6	AS1 & AS2_MAX_ATTEN							

Maximum attenuation value will be utilized by the acoustic suppression algorithm.
The maximum value of this field provides an attenuation factor of 1.
The minimum value provides an attenuation factor of 0.

13.4.1.3 AS_MIN_ATTEN

Address	Access Mode	Value At Reset	Nominal Value
0x14C7 - 0x14C8	R/W	0xFFFF	0xFFFF

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
C7	AS1 & AS2_MIN_ATTEN							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C8	AS1 & AS2_MIN_ATTEN							

Minimum attenuation value will be utilized by the acoustic suppression algorithm.
The maximum value of this field provides an attenuation factor of 1.
The minimum value provides an attenuation factor of 0.

13.4.2 Acoustic Side Control Registers

13.4.2.1 DT_LONG_ACOUSTIC_ATTACK_TC

Address	Access Mode	Value At Reset	Nominal Value
0x14C9	R/W	0x09	0x09

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	DT_LONG_ACOUSTIC_ATTACK_TC			

Acoustic long term power estimation's attacking time constant.

This field defines the inertial delay utilized for the long term acoustic power estimation. Raising the value of this field reduces the inertia and will make the estimation more responsive whilst lowering the field will cause the power estimation algorithm to be less responsive to bursts of energy on the acoustic.

13.4.2.2 DT_SHORT_ACOUSTIC_ATTACK_TC

Address	Access Mode	Value At Reset	Nominal Value
0x14CA	R/W	0x0B	0x0B

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	DT_SHORT_ACOUSTIC_ATTACK_TC			

Acoustic short term power estimation's attacking time constant

This field defines the inertial delay utilized for the short term acoustic power estimation. Raising the value of this field reduces the inertia and will make the estimation more responsive whilst lowering the field will cause the power estimation algorithm to be less responsive to bursts of energy on the acoustic side.

13.4.2.3 DT_ACOUSTIC_HANGOVER_TIME

Address	Access Mode	Value At Reset	Nominal Value
0x14CB - 0x14CC	R/W	0x0020	0x0340

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CB	DT_ACOUSTIC_HANGOVER_TIME							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CC	DT_ACOUSTIC_HANGOVER_TIME							

This field defines the inertial delay of the double talk detection algorithm for acoustic side.
Following the detection of the double talk condition there is a programmable inertial delay (in PCM sample periods 125us) following the disappearance of the double talk condition. For the duration of this delay period the double talk condition is assumed to remain. If double talk does not reappear during this window then the echo cancellation unit will revert back to acoustic training mode.

13.4.2.4 DT_ ACOUSTIC _DEV_THRESHOLD

Address	Access Mode	Value At Reset	Nominal Value
0x14CD - 0x14CE	R/W	0x0666	0x0040

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CD	DT_ ACOUSTIC_DEV_THRESHOLD							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CE	DT_ ACOUSTIC_DEV_THRESHOLD							

This field defines the instantaneous acoustic power change that is deemed to correspond to speech and is used to detect short term changes in voice level on the acoustic interface.Raising (lowering) this field will raise (lower) the change in acoustic power required for the detection of speech (and hence the double talk condition).

13.4.2.5 DT_SHORT_ACOUSTIC_THRESHOLD

Address	Access Mode	Value At Reset	Nominal Value
0x14CF - 0x14D0	R/W	0x0404	0x0040

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CF	DT_SHORT_ ACOUSTIC_THRESHOLD							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D0	DT_SHORT_ ACOUSTIC_THRESHOLD							

This field defines the power threshold that is deemed to correspond to speech. Raising(lowering) this field will raise (lower) the acoustic power required for the detection of speech (and hence the double talk condition).

13.4.3 Network Side Control Registers

13.4.3.1 VD_LONG_NETWORK_ATTACK_TC

Address	Access Mode	Value At Reset	Nominal Value
0x14D1	R/W	0x09	0x09

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	VD_LONG_NETWORK_ATTACK_TC			

Network long term power estimation's attacking time constant

This field defines the inertial delay utilized for the long term network power estimation. Raising the value of this field reduces the inertia and will make the estimation more responsive whilst lowering the field will cause the power estimation algorithm to be less responsive to bursts of energy on the network side.

13.4.3.2 VD_SHORT_NETWORK_ATTACK_TC

Address	Access Mode	Value At Reset	Nominal Value
0x14D2	R/W	0x0B	0x0B

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	VD_SHORT_NETWORK_ATTACK_TC			

Network short term power estimation's attacking time constant

This field defines the inertial delay utilized for the short term network power estimation. Raising the value of this field reduces the inertia and will make the estimation more responsive whilst lowering the field will cause the power estimation algorithm to be less responsive to bursts of energy on the network side.

13.4.3.3 VD_NETWORK_HANGOVER_TIME

Address	Access Mode	Value At Reset	Nominal Value
0x14D3 - 0x14D4	R/W	0x0009	0x0340

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
D3	VD_NETWORK_HANGOVER_TIME							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D4	VD_NETWORK_HANGOVER_TIME							

This field defines the inertial delay of the voice detection algorithm for the network side.

Following the detection of the speech on the network interface there is a programmable inertial delay (in PCM sample periods) following the disappearance of the speech signal. For the duration of this delay period the speech is assumed to remain. If speech does not reappear during this window then the echo cancellation unit will revert back to channel training mode.

13.4.3.4 VD_NETWORK_DEV_THRESHOLD

Address	Access Mode	Value At Reset	Nominal Value
0x14D5 - 0x14D6	R/W	0x0666	0x01B0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
D5	VD_NETWORK_DEV_THRESHOLD							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D6	VD_NETWORK_DEV_THRESHOLD							

This field defines the instantaneous network power change that is deemed to correspond to speech and is used to detect short term changes in voice level on the network interface.

Raising (lowering) this field will raise (lower) the change in network power required for the detection of speech.

13.4.3.5 VD_LONG_NETWROK_THRESHOLD

Address	Access Mode	Value At Reset	Nominal Value
0x14D7 - 0x14D8	R/W	0x0666	0x1050

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
D7	VD_LONG_NETWORK_THRESHOLD							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D8	VD_LONG_NETWORK_THRESHOLD							

Minimum power level constitutes speech over the network interface, as measured by the long term power estimation algorithm.

13.4.3.6 VD_SHORT_NETWROK_THRESHOLD

Address	Access Mode	Value At Reset	Nominal Value
0x14D9 - 0x14DA	R/W	0x040E	0x03C0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
D9	VD_SHORT_NETWORK_THRESHOLD							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA	VD_SHORT_NETWORK_THRESHOLD							

Minimum power level constitutes speech over the network interface, as measured by the short term power estimation algorithm.

13.4.3.7 VD_CUT_OFF_NETWORK_POWER

Address	Access Mode	Value At Reset	Nominal Value
0x14DB - 0x14DC	R/W	0x0666	0x08A0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
DB	VD_CUT_OFF_NETWORK_POWER							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DC	VD_CUT_OFF_NETWORK_POWER							

Configurable bias for network power estimation. This field defines the zero reference for the network power estimation algorithm.

13.4.3.8 Specific Register

Address	Access Mode	Value At Reset	Nominal Value
0x14DD	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Blocked (for test modes)

13.4.4 ACOUSTIC / NETWORK Active Status

Address	Access Mode	Value At Reset	Nominal Value
0x14DE	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	AcousticActive	NetworkActive	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)

AcousticActive = 1, reflect the status of acoustic power
NetworkActive = 1, reflect the status of network power.

13.4.5 AGC Control Registers

13.4.5.1 AGC_THRESHOLD

Address	Access Mode	Value At Reset	Nominal Value
0x14DF - 0x14E0	R/W	0x0800	0x1000

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
DF	AGC_THRESHOLD							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E0	AGC_THRESHOLD							

The AGC threshold is set the maximum output power from AGC module. The purpose is set properly gain to prevent voice signal clipping.

13.4.5.2 AGC_NOISE_THRESHOLD

Address	Access Mode	Value At Reset	Nominal Value
0x14E1 - 0x14E2	R/W	0x00C8	0x0100

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
E1	AGC_NOISE_THRESHOLD							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E2	AGC_NOISE_THRESHOLD							

The calculated input power with time constant AGC_ST_ATTACK_TC is less than the AGC_NOISE_THRESHOLD, then AGC gain is set to unit gain. It is assumed that the input power is background signal.

13.4.5.3 AGC_MAX_SG

Address	Access Mode	Value At Reset	Nominal Value
0x14E3	R/W	0x02	0x0A

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	AGC_MAX_SG			

The AGC module has maximum gain to amplifier the echo cancelled input signal.

13.4.5.4 Specific Register

Address	Access Mode	Value At Reset	Nominal Value
0x14E4	R/W	0x0F	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	*Blocked for test modes			

*Blocked for test modes. Set the 4 bits to 1.

13.4.5.5 AGC_LG_ATTACK_TC

Address	Access Mode	Value At Reset	Nominal Value
0x14E5	R/W	0x0B	0x33

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AGC_LG_ATTACK_TC_POS				AGC_LG_ATTACK_TC_NEG			

AGC_LG_ATTACK_TC_NEG The field defines the inertial delay utilized for the long term gain estimation when the AGC gain is increasing. Raising the value of this field reduces the inertial and will make the estimation more responsive while lowering the field will cause the gain estimation algorithm to be less responsive to bursts of gain on the AGC.

AGC_LG_ATTACK_TC_POS The field defines the inertial delay utilized for the long term gain estimation when the AGC gain is decreasing. Raising the value of this field reduces the inertial and will make the estimation more responsive while lowering the field will cause the gain estimation algorithm to be less responsive to bursts of gain on the AGC.

13.4.5.6 AGC_ST_ATTACK_TC

Address	Access Mode	Value At Reset	Nominal Value
0x14E6	R/W	0x09	0x09

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED				AGC_ST_ATTACK_TC			

Attack time for short term AGC power estimation. This field defines the inertial delay utilized for the short term AGC power estimation. Raising the value of this field reduces the inertial and will make the estimation more responsive while lowering the field will cause the power estimation algorithm to be less responsive to bursts of energy on the AGC.

13.4.6 Noise Suppressor Registers

13.4.6.1 NS_STTACK_Tcand_GAIN

Address	Access Mode	Value At Reset	Nominal Value
0x14E7	R/W	0x00	0xB5

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ShortTermNSPowerATTACKTC[7:4]				Noise_Suppressor_Index[3:0]			

Noise_Suppressor_Index：This 4-bit field defines the gain of Noise suppressor

Noise_Suppressor_Index[3:0]	Noise Suppressor Level (dB)	Noise_Suppressor_Index[3:0]	Noise Suppressor Level (dB)
0	-1	9	-10
1	-2	A	-11
2	-3	B	-12
3	-4	C	-13
4	-5	D	-14
5	-6	E	-15
6	-7	F	-16
7	-8		
8	-9		

ShortTermNSPowerATTACKTC：
The 4-bit field defines the "Time Constant" to calculate the power of voice that enters the noise suppressor module.
So "Noise Suppressor" can determine if current power of voice is larger than "Noise threshold" or not.
The operation is just like "Short term acoustic power time constant.

13.4.6.2 NS_ATTEN_DW_UP_TC

Address	Access Mode	Value At Reset	Nominal Value
0x14E8	R/W	0x00	0x55

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Noise_fall_TC[4:7]				Noise_rise_TC[0:3]			

Noise_rise_TC This 4-bit field defines the time constant of Noise suppressor gain from the gain specified by "noise_suppressor_index" to "0dB". Larger value, faster speed.

Noise_fall_TC This 4-bit field defines the time constant of Noise suppressor gain from "0dB" to the gain specified by "noise_suppressor_index". Larger value, faster speed.

13.4.6.3 NS_Active_Power_MSB

Address	Access Mode	Value At Reset	Nominal Value
0x14E9	R/W	0x00	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NS_Active_Power_MSB							

The most significant byte of noise threshold.

13.4.6.4 NS_Active_Power_LSB

Address	Access Mode	Value At Reset	Nominal Value
0x14EA	R/W	0x00	0x40

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NS_Active_Power_LSB							

The most significant byte of noise threshold.
So "noise_threshold" = {NS_Active_Power_MSB,NS_Active_Power_LSB}

13.4.7 AEC Soft Clip

In order to reduce clipping distortion, a soft clipping function has been implemented in GTx1. A second gain (GTx1_SC) and an overload threshold point (TH_SC) is programmable. Gain GTx1 is changed to GTx1_SC if the input signal level of the GTx1 gain state is greater than TH_SC. Note that the input signal power level is estimated in the GTx1 gain stage using the following arithmetic unit：

$$P_{GTx1} = P_{GTx1} \times \left(1 - 2^{GTx1_TC-16}\right) + \left|A_{GTx1}\right| \times 2^{GTx1_TC-16}$$

If ($P_{GTx1} \geq$ TH_SC)

$$GTx1_Factor \Leftarrow GTx1_SC$$

Else $GTx1_Factor \Leftarrow GTx1$

$$GTx1_{avg} \Leftarrow (1 - 2^{(GT_TC-16)}) \times GTx1_{avg} + GTx1_Factor \times 2^{(GT_TC-16)}$$

$$A_{rin} \Leftarrow A_{GTx1} \times GTx1_{avg}$$

P_{GTx1} ： GTx1 input power with time constant GTx1_TC

$GTx1_{avg}$ ： GTx1 average gain with time constant GT_TC

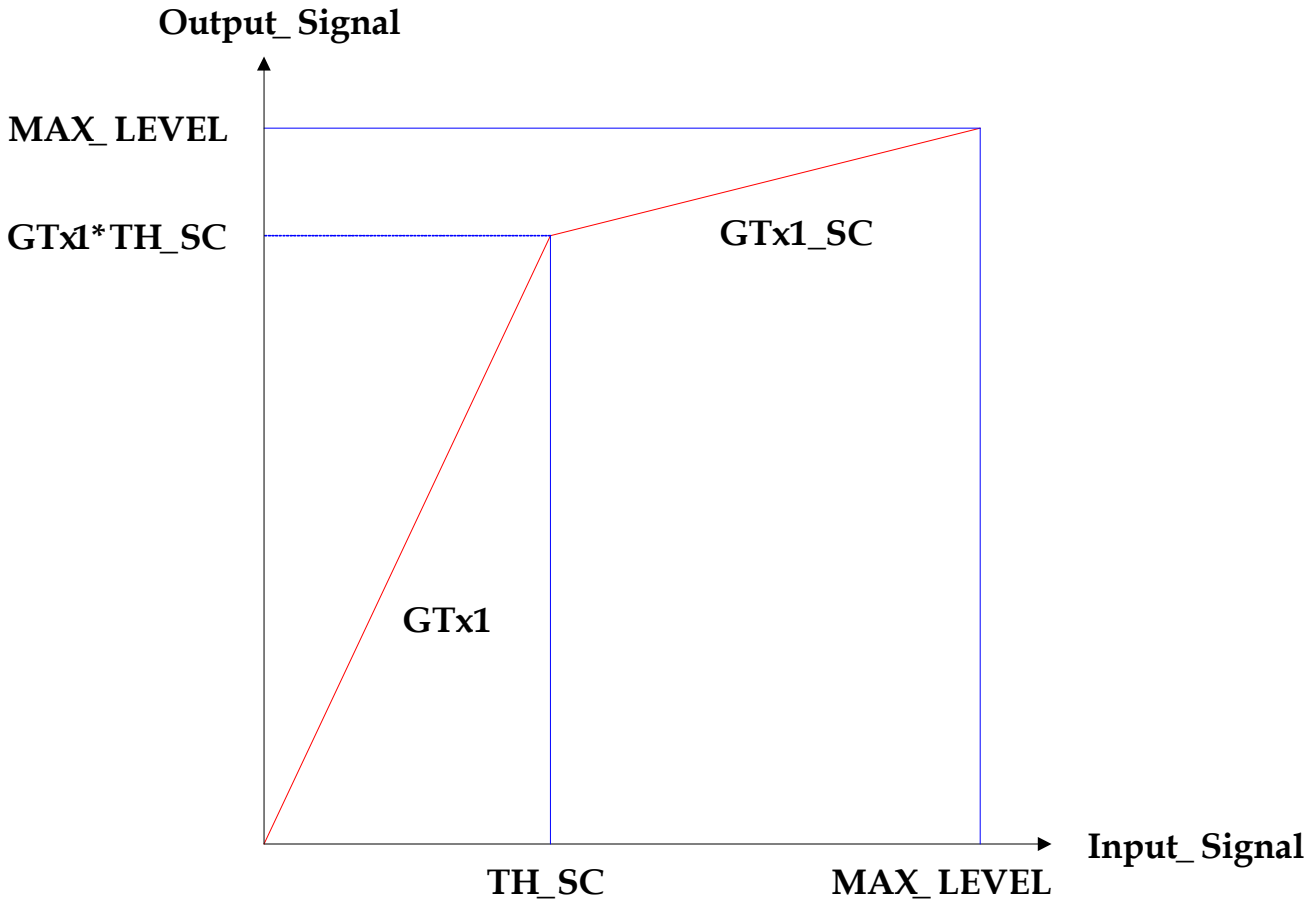


Figure 13-2 Block diagram of the soft clipping function of GTx1

13.4.7.1 Soft Clip Control

Address	Access Mode	Value At Reset	Nominal Value
0x14EB	R/W	0x00	0x03

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	Reserved	Reserved	DTSC_Enable	VDSC_Enable

Soft_clip control register is used to enable the soft clipping function. There are two bits in this register to control two soft clip blocks independently.

VDSC_Enable When set, enable soft clip function for network signal before network signal is sent to AEC module. When reset, disable soft clip function. So network signal is sent to AEC module directly.

DTSC_Enable When set, enable soft clip function for acoustic signal after acoustic signal is sent out from AEC module. When reset, disable soft clip function. So acoustic signal is sent to next stage directly.

13.4.7.2 VD Soft Clip Normal Index

Address	Access Mode	Value At Reset	Nominal Value
0x14EC	R/W	0x00	0x12

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	VDSC_Normal_Index[5:0]					

VDSC_Normal_Index[5:0] is used to control the gain of VD Soft_Clip module at normal mode. The gain selection range is the same as "Digital Gain Multiplexer" and is reproduced below：

VDSC_Normal_Index[5:0] HEX Value	Gain	VDSC_Normal_Index[5:0] HEX Value	Gain
0x00	0 dB (default)	0x19	- 0.5 dB
0x01	0.5 dB	0x1A	- 1.0 dB
0x02	1.0 dB	0x1B	- 1.5 dB
0x03	1.5 dB	0x1C	- 2.0 dB
0x04	2.0 dB	0x1D	- 2.5 dB
0x05	2.5 dB	0x1E	- 3.0 dB
0x06	3.0 dB	0x1F	- 3.5 dB
0x07	3.5 dB	0x20	- 4.0 dB
0x08	4.0 dB	0x21	- 4.5 dB
0x09	4.5 dB	0x22	- 5.0 dB
0x0A	5.0 dB	0x23	- 5.5 dB
0x0B	5.5 dB	0x24	- 6.0 dB
0x0C	6.0 dB	0x25	- 6.5 dB
0x0D	6.5 dB	0x26	- 7.0 dB
0x0E	7.0 dB	0x27	- 7.5 dB
0x0F	7.5 dB	0x28	- 8.0 dB
0x10	8.0 dB	0x29	- 8.5 dB
0x11	8.5 dB	0x2A	- 9.0 dB
0x12	9.0 dB	0x2B	- 9.5 dB
0x13	9.5 dB	0x2C	- 10.0 dB
0x14	10.0 dB	0x2D	- 10.5 dB
0x15	10.5 dB	0x2E	- 11.0 dB
0x16	11.0 dB	0x2F	- 11.5 dB
0x17	11.5 dB	0x30	- 12.0 dB
0x18	12.0 dB	0x3F	Mute

13.4.7.3 VD Soft Clip Low Index

Address	Access Mode	Value At Reset	Nominal Value
0x14ED	R/W	0x00	0x06

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	VDSC_Low_Index[5:0]					

VDSC_Low_Index[5:0] is used to control the gain of vd soft_clip module at low mode. The gain selection range is the same as "VD Soft Clip Normal Index".

13.4.7.4 VD Soft Clip Threshold

Address	Access Mode	Value At Reset	Nominal Value
0x14EE - 0x14EF	R/W	0x0400	0x4000

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
EE	VDSC_Threshold							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EF	VDSC_Threshold							

VDSC_Threshold is used to determine the selection of Soft Clip gain. When the input network power is larger then VDSC_Threshold, VDSC_Low_Index gain is used, otherwise VDSC_Normal_Index gain is used.

13.4.7.5 ShortTermPreNetworkPowerAttackTC

Address	Access Mode	Value At Reset	Nominal Value
0x14F0	R/W	0x07	0x0B

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	ShortTermPreNetworkPowerAttackTC[3:0]			

ShortTermPreNetworkPowerAttackTC[3:0] is the time constant which is used to calculate the short term network power for VD Soft Clip.

13.4.7.6 VDSC Attack TC

Address	Access Mode	Value At Reset	Nominal Value
0x14F1	R/W	0x07	0x05

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	VDSC_AttackTC[3:0]			

When soft clip gain is switched between normal and low, an embedded smoothing function is used to smooth the gain change. VDSC_AttackTC[3:0] is a time constant to control the smoothing speed.

13.4.7.7 DT Soft Clip Normal Index

Address	Access Mode	Value At Reset	Nominal Value
0x14F2	R/W	0x00	0x18

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	DTSC_Normal_Index[5:0]					

DTSC_Normal_Index[5:0] is used to control the gain of DT Soft Clip module at normal mode. The gain selection range is the same as "VDSC_Normal_Index".

13.4.7.8 DT Soft Clip Low Index

Address	Access Mode	Value At Reset	Nominal Value
0x14F3	R/W	0x00	0x0C

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	DTSC_Low_Index[5:0]					

DTSC_Low_Index[5:0] is used to control the gain of DT Soft_Clip module at low mode. The gain selection range is the same as "VDSC_ Normal_Index".

13.4.7.9 DT Soft Clip Threshold

Address	Access Mode	Value At Reset	Nominal Value
0x14F4 - 0x14F5	R/W	0x0400	0x1140

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
F4	DTSC_Threshold							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F5	DT_SC_Threshold							

DTSC_Threshold is used to determine the selection of Soft Clip gain. When the output acoustic power is larger then DTSC_Threshold, DTSC_Low_Index gain is used, otherwise DTSC_Normal_Index gain is used.

13.4.7.10 ShortTermPostAcousticPowerAttackTC

Address	Access Mode	Value At Reset	Nominal Value
0x14F6	R/W	0x07	0x0B

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	ShortTermPostAcousticPowerAttackTC[3:0]			

ShortTermPostAcousticPowerAttackTC[3:0] is the time constant which is used to calculate the short term acoustic power for DT Soft Clip.

13.4.7.11 DTSC Attack TC

Address	Access Mode	Value At Reset	Nominal Value
0x14F7	R/W	0x07	0x05

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	DTSC_AttackTC[3:0]			

When soft clip gain is switched between normal and low, an embedded smoothing function is used to smooth the gain change. DTSC_AttackTC[3:0] is a time constant to control the smoothing speed.

13.5 Acoustic Side / Network Side Power Measurement

13.5.1 ACOUSTIC_SHORT_TERM_POWER

Address	Access Mode	Value At Reset	Nominal Value
0x15C0- 0x15C1	R	0x0000	

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
C0	ACOUSTIC_SHORT_TERM_POWER							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C1	ACOUSTIC__SHORT_TERM_POWER							

Short Term Acoustic Power calculated by the double talk detector (DT).

13.5.2 ACOUSTIC_LONG_TERM_POWER

Address	Access Mode	Value At Reset	Nominal Value
0x15C2- 0x15C3	R	0x0000	

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

C2	ACOUSTIC_LONG_TERM_POWER

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C3	ACOUSTIC_LONG_TERM_POWER							

Long Term Power on acoustic side estimated by the double talk detector (DT).

13.5.3 ACOUSTIC_POWER_DEVIATION

Address	Access Mode	Value At Reset	Nominal Value
0x15C4- 0x15C5	R	0x0000	

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
C4	ACOUSTIC_POWER_DEVIATION							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C5	ACOUSTIC_POWER_DEVIATION							

Acoustic Power Deviation estimated by the double talk detector (DT).

13.5.4 ACOUSTIC / NETWORK Active Status

Address	Access Mode	Value At Reset	Nominal Value
0x15C6	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	AcousticActive	NetworkActive

Bit[1] = 1, reflect the status of acoustic power.
Bit[0] = 1, reflect the status of network power.

13.5.5 NETWORK_SHORT_TERM_POWER

Address	Access Mode	Value At Reset	Nominal Value
0x15C8 - 0x15C9	R	0x0000	

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
C8	NETWORK_SHORT_TERM_POWER							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C9	NETWORK_SHORT_TERM_POWER							

Network Short Term Power calculated by VD modules.

13.5.6 NETWORK_LONG_TERM_POWER

Address	Access Mode	Value At Reset	Nominal Value
0x15CA- 0x15CB	R	0x0000	

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CA	NETWORK_LONG_TERM_POWER							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CB	NETWORK_LONG_TERM_POWER							

Network Long Term Power calculated by VD modules.

13.5.7 NETWORK_POWER_DEVIATION

Address	Access Mode	Value At Reset	Nominal Value
0x15CC- 0x15CD	R	0x0000	

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CC	NETWORK_POWER_DEVIATION							

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CD	NETWORK_POWER_DEVIATION							

Network Power Deviation estimated by the voice detector (VD).

13.5.8 ACOUSTIC / NETWORK Active Status

Address	Access Mode	Value At Reset	Nominal Value
0x15CE	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	AcousticActive	NetworkActive

Bit[1] = 1, reflect the status of acoustic power.
Bit[0] = 1, reflect the status of network power.

14. SYSTEM FUNCTION

14.1 Power On Reset

The power on reset (POR) block generates a internal reset signal to reset the whole chip after connecting the power supply voltage the chip. The power on reset circuit responds to the voltage difference applied between AVDD and AGND. Figure 14-1 shows the power reset circuit.

When AVDD is rising slowly starting from zero to the signal PowerOnResetN will be low until AVDD passed the power-on voltage level Von. After a delay time (about 37ms for 13.824MHz clock) Reset_out goes high and the actual reset sequence starts. If AVDD does not pass Von voltage, then the PowerOnResetN stays low, causing the oscillator to run and having most of the digital logic circuits being in an active reset mode. If AVDD sinks below the power-off voltage level Voff, PowerOnRestN will become low again. The hysteresis voltage between Von and Voff is need to overcome a "reset oscillation" phenomenon that otherwise might occur if AVDD decrease due to the activity during the reset sequence.

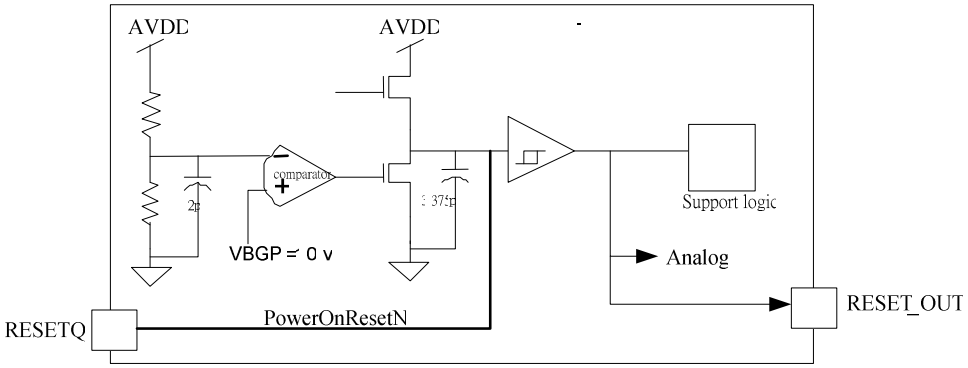


Figure 144-1 Analog part of the power on Reset function.

14.1.1 CODEC On/Off Scheme

Address	Access Mode	Value At Reset
0x1500	R/W	0x00

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	PeriodSelection		Codec on/off	CODECOnOff scheme Enable

CODECOnOff_scheme_Enable — Set "1" to enable hardwired CODEC On/Off scheme.
Set "0" to use independent On/Off control from 0x1509.

CODEC On/Off — Set"1" to turn on CODEC.
Set "0" to turn off CODEC.

PeriodSelection — Set to select the duration length between CODEC_digital_on/off and CODEC_analog_on/off.

Bit[3:2]	Period
2'b00	2 mS
2'b01	4 mS
2'b10	8 mS
2'b11	16 mS

14.1.2 CODEC Digital Part

Address	Access Mode	Value At Reset	Nominal Value
0x1501	R/W	0x80	90

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ABF_MODE	DAC_Dither_Level[1:0]		DAC_Dither _Enable	ADC_ABF_Length[1:0]		CODEC_FIFO_ PTR_Reset	CODEC_FIFO_ Reset

CODEC_FIFO_Reset When set, Clear CODEC FIFO content after each 8K operation.
CODEC_FIFO_PTR_Reset When set, Reset CODEC FIFO pointer after each 8K operation.
ADC_ABF_Length[1:0] Select the limit cycle length to do adaptive bit flipping (ABF) algorithm.

ABF_L[1:0]	Limit cycle Length
0	4
1	6
2	8
3	10

DAC_Dither_Enable When set, enable the dither input in DAC path
DAC_Dither_Level[1:0] Select the dither level in the DAC path.

DA_Dither_Level[1:0]	Dither Level
0	17 bit
1	15 bit
2	16 bit
3	18 bit

ABF_MODE When set, select adaptive bit flipping algorithm (ABF) mode in the analog CODEC modulator.

14.2 ADC Adaptive Bit Flip Probability

Address	Access Mode	Value At Reset	Nominal Value
0x1502	R/W	0xFF	80

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC_ABF_PROB							

This byte set the adaptive bit flip probability of the ADC path in the CODEC modulator. When set ADC_ABF_PROB to 0xFF will disable the adaptive bit-flipping algorithm, and set to 0x00 means always enable the adaptive bit-flipping algorithm if the limit cycle length condition is detected.

14.3 Sounder Signal Selection

Address	Access Mode	Value At Reset	Nominal Value
0x1503	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Blocked (for test modes)	RESERVED	Rclk_SNDR_SEL	RefClkSel		RefClkOn	PDMEN	SNDRSigSel

There are two sounders signal to be selected to connect to SNDR pin. This subsection describes the sounder signal of PDM (Pulse Density Modulation) format. The selection of different sounder signal and the related control bits are shown in 0x1503[1:0].

PDMEN — When set, the TX path of CODEC will be hardware muted, the over sampled DTMF signal is switched to sounder signal path. So except to generate sounder signal, this bit should be reset to 0 while CODEC is active.

SNDRSigSel — When set, the sounder signal comes from the DTMF generator in the speech processor. The DTMF signal will be over sampled to 1 bit signal, which is called Pulse Density Modulation (PDM) format. The PDM format signal then connects to pin SNDR while PDMRingEN=1. The control registers of DTMF generator are allocated from addresses 1488H~148CH
=0, the sounder signal comes from the Ringer Tone Generator with Pulse Width Modulation (PWM) format. The control registers of Ringer Tone Generator are allocated from addresses 1447H~144AH

RefClkOn — When set, enable Reference Clock Generation circuit.

RefClkSel — Reference clock rate selection.

RefClkSel[4:3]	Reference Clk Rate
0	13.824 MHz
1	6.912 MHz
2	3.456 MHz
3	1.728 MHz

Rclk_SNDR_Sel — Switch the function of pin SNDR. Set “1” to configure the SNDR pin as RefClock output.
Set ”0” to configure the SNDR pin as SNDR output.

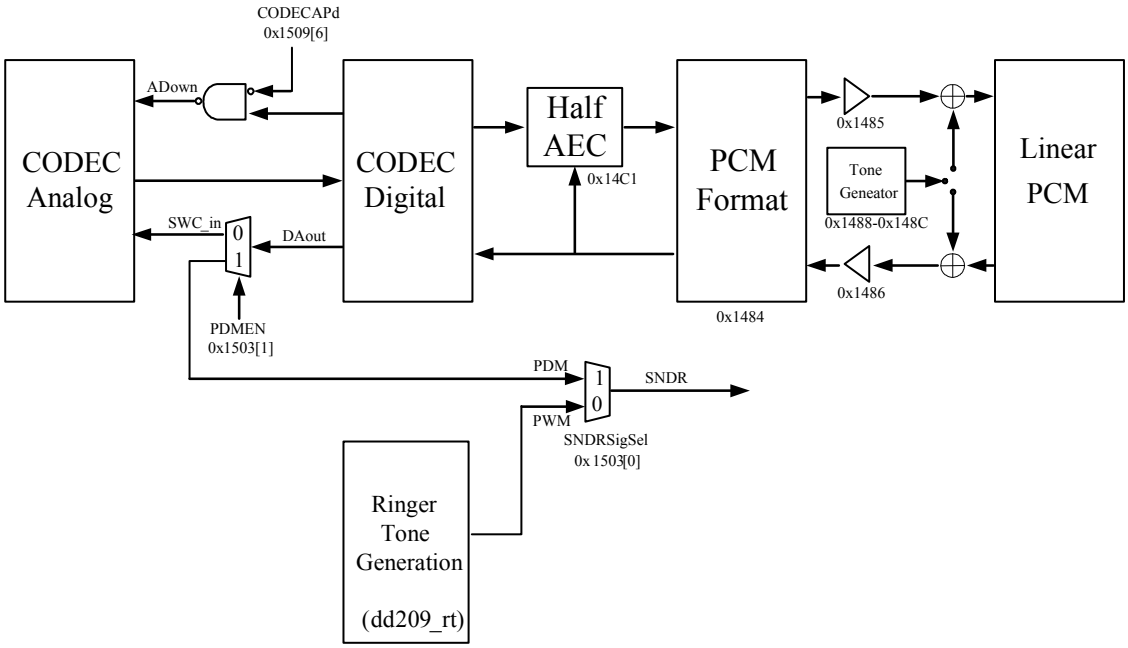


Figure 14-2 Sounder signal selection circuit

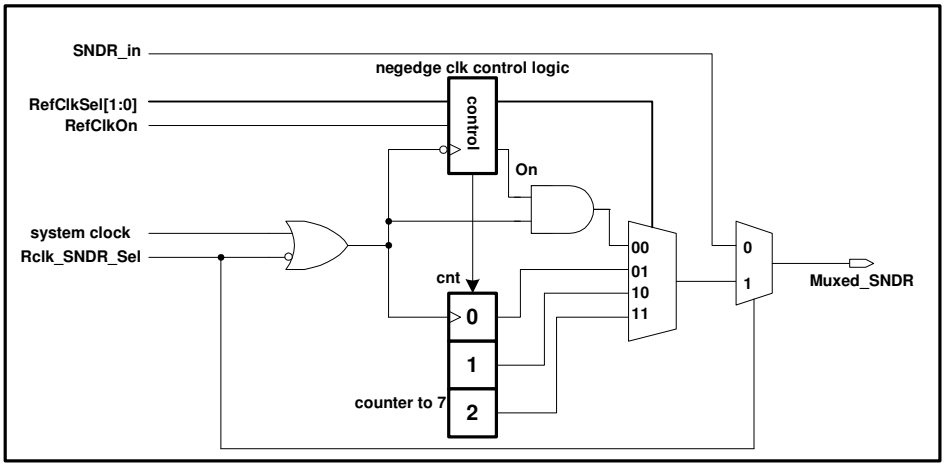


Figure 14-3 Reference clock frequency rate and function selection circuit.

14.4 Frequency Adjustment of Crystal Oscillator

A 13.824 MHz crystal is connected to pin XTAL1 and XTAL2. But the accuracy of the system clock will affect the performance and power saving capability of a handset operating in suspend mode. The frequency deviation resulted from the variation of crystal device and external load capacitances can be adjusted by the on-chip capacitances.

FACO (Frequency Adjustment of Crystal Oscillator) controls the connection of on-chip capacitance Cg and Cd to the crystal oscillator pins XTAL1 and XTAL2 respectively. The total maximum value is 11.9pF per pin. Therefore this register can control the frequency of the crystal oscillator at 13.824 MHz. accurately.

FACO

Address	Access Mode	Value At Reset	Nominal Value
0x1504	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FACO							

FACO[Bit 7] When set, add an 8 pF to Cg and Cd each.
FACO[Bit 6] When set, add an 4 pF to Cg and Cd each.
FACO[Bit 5] When set, add an 2 pF to Cg and Cd each.
FACO[Bit 4] When set, add an 1 pF to Cg and Cd each.
FACO[Bit 3] When set, add an 0.5 pF to Cg and Cd each.
FACO[Bit 2] When set, add an 0.25 pF to Cg and Cd each.
FACO[Bit 1] When set, add an 0.125 pF to Cg and Cd each.
FACO[Bit 0] When set, add an 0.0625 pF to Cg and Cd each.

14.5 Specific Register

Address	Access Mode	Value At Reset	Nominal Value
0x1505	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)

14.6 VAG Selection

Address	Access Mode	Value At Reset	Nominal Value
0x1506	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Vc_vag [2:0]			RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

VAG default voltage is 1.5V. And the VAG level can be programmed by software with following table.

	Vc_vag [2:0]		VAG (V)
	Bin	Hex	
Default	000	0	1.50
	001	1	1.57
	010	2	1.67
	011	3	1.80
	100	4	2.00
	101	5	2.33
	110	6	1.50
	111	7	1.50

14.7 TG Gain Register

Address	Access Mode	Value At Reset	Nominal Value
0x1507	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	TG_A Gain[2]	TG_A Gain[1]	TG_A Gain[0]	Reserved	TG_B Gain[2]	TG_B Gain[1]	TG_B Gain[0]

TG Op amp of the Codec is implemented as a two amplifiers cascade to provide the necessary gain for low signal microphone input. The first stage (TG_A) is designed as a full differential high impendence and low noise amplifier. This amplifier gain can be set as bypass or maximum gain 18dB for microphone input. The second stage (TG_B) is also full differential amplifier and provides maximum gain 24dB for the application requirement. It is according this register to set different gain in the Codec, equivalent architecture is shown in Figure 14-4. The TG amplifier gain table is listed as below：

TG_A Gain[2:0]		Gain [dB]	TG_B Gain[2:0]		Gain [dB]
Bin	Hex		Bin	Hex	
0000	0	0 dB	0000	0	0 dB
0001	1	6 dB	0001	1	6 dB
0010	2	12 dB	0010	2	12 dB
0011	3	18 dB	0011	3	18 dB
0100	4	Bypass	0100	4	24 dB
0101	5	Bypass	0101	5	24 dB
0110	6	Bypass	0110	6	24 dB
0111	7	Bypass	0111	7	24 dB

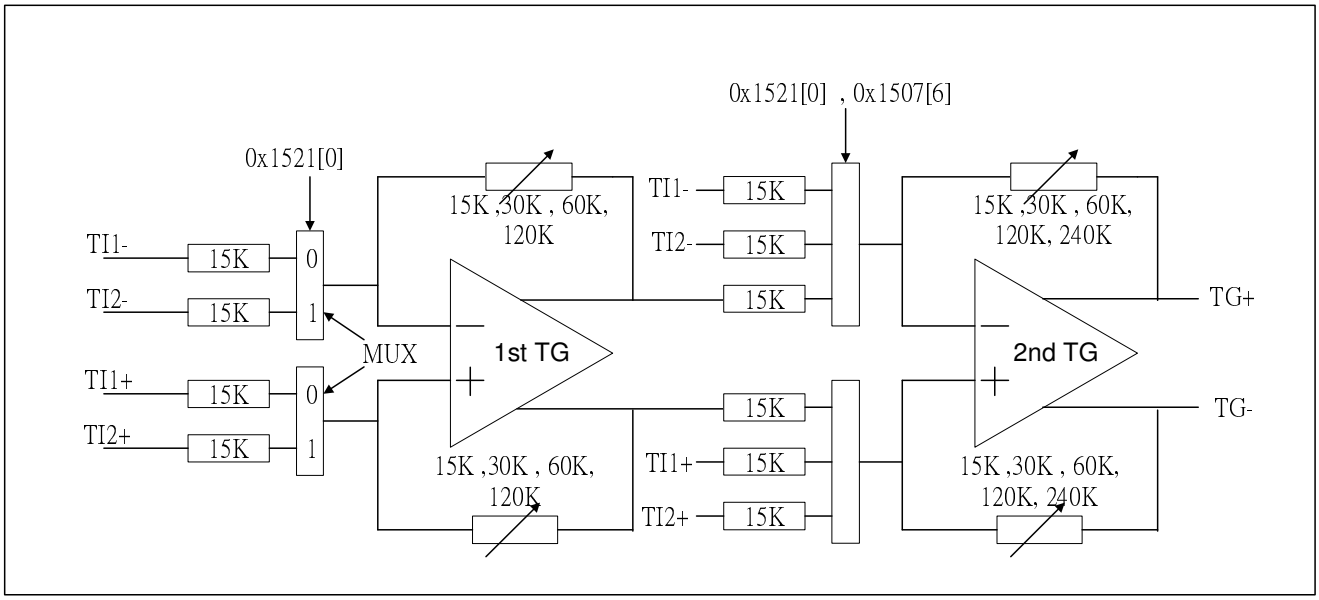


Figure 14-4 Equivalent schematics for TG Op amp.

14.8 PO Gain Register

Address	Access Mode	Value At Reset	Nominal Value
0x1508	R/W	0x88	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PO2_PD	PO2Gain [2]	PO2Gain [1]	PO2Gain [0]	PO1_PD	PO1Gain [2]	PO1Gain [1]	PO1Gain [0]

The gains of PO1 and PO2 op amp are set according to this register value. The maximum driving capability of PO1 is 120Ω and PO2 is 16Ω. The PO1 and PO2 can be power down by the corresponding control bits of PO Gain register.

Note that the PO op amps can be also power down by the CODEC_CTRL register (0x1509).

The PO amplifier gain table is listed as below.

PO1 Gain [3:0]		**Gain [dB]**	**PO2 Gain [7:4]**		**Gain [dB]**
Bin	**Hex**		**Bin**	**Hex**	
0000	0	0 dB	0000	0	0 dB
0001	1	2 dB	0001	1	2 dB
0010	2	4 dB	0010	2	4 dB
0011	3	6 dB	0011	3	6 dB
0100	4	8 dB	0100	4	8 dB
0101	5	10 dB	0101	5	10 dB
0110	6	-2 dB	0110	6	-2 dB
0111	7	-4 dB	0111	7	-4 dB
1xxx		Disable	1xxx		Disable

The equivalent resistance is shown in Figure 14-5.

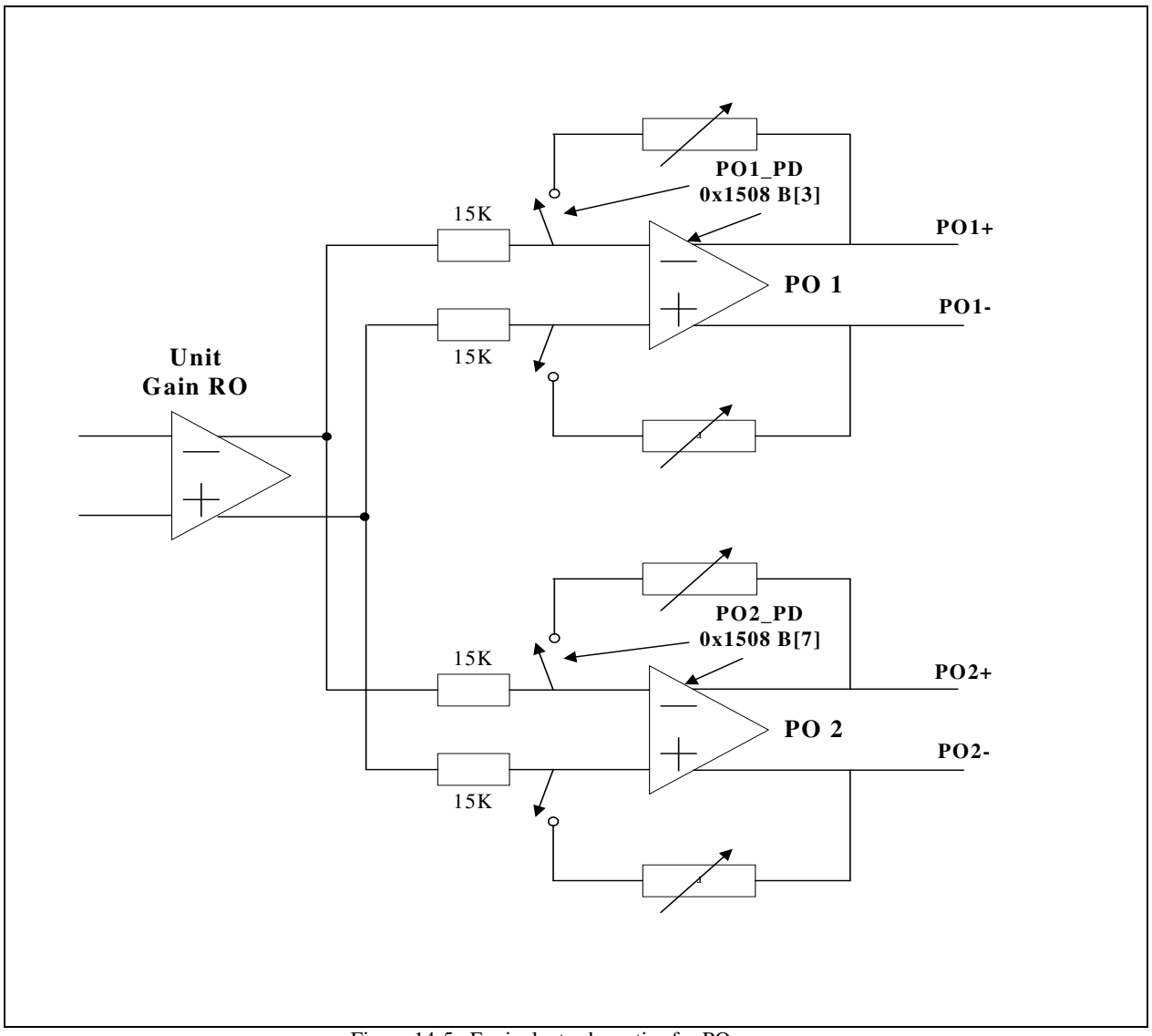


Figure 14-5 Equivalent schematics for PO op amp

14.9 The PCM CODEC

14.9.1 Block Diagram

Figure 14-6 shows the block diagram of the speech CODEC-filter.

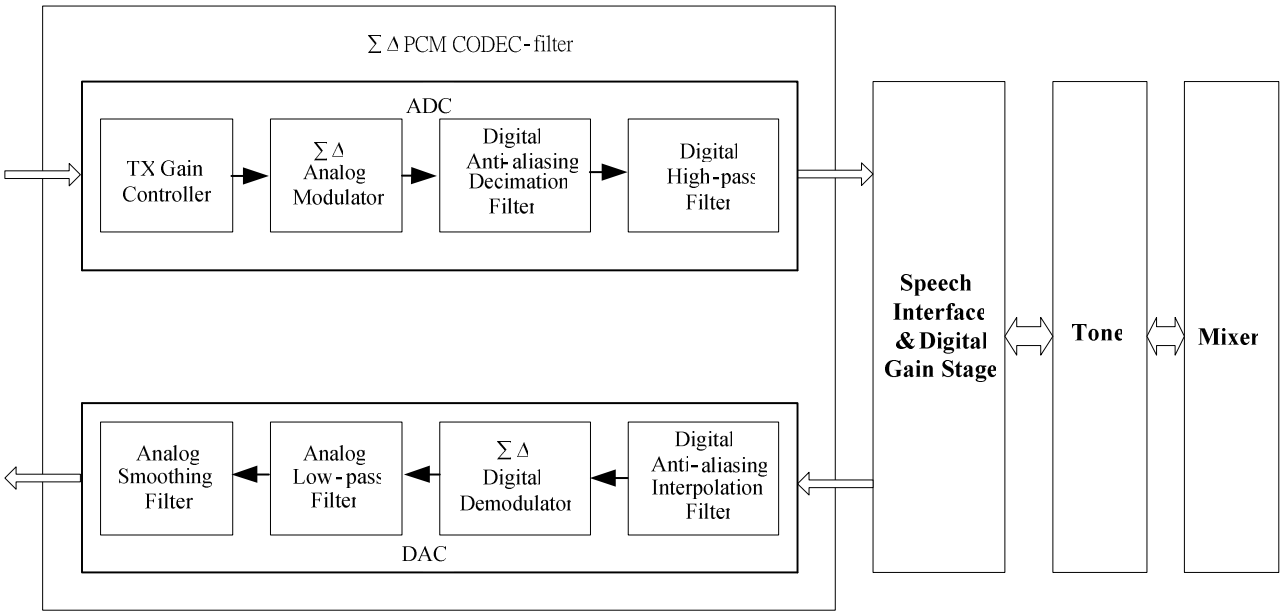


Figure 14-6 The block diagram of the PCM CODEC-Filter

14.9.2 Analog Interface and Signal Path

The built in linear 14-bit PCM CODEC-filter uses ΣΔ technology. There are two paths in the block, a transmit path and a receive path.

14.9.2.1 Transmit Path in ΣΔ CODEC-Filter

An analog signal input, from a microphone interface, is passed to three terminal operational amplifiers (TI+, TI-, TG) driving a typical 2 KΩ load externally to amplify the input analog signal. The modulator block over samples the analog signal at 1.536 MHz with one bit resolution. The next anti-aliasing decimation filter reduces the sampling frequency from 1.536 MHz (1 bit) to 32 KHz (15 bit). Digital bi-quad filters perform the decimation from 32K to 8 KHz and CCITT low-pass filtering at 3400 Hz. The digital HPF block performs the high-pass filtering at 300 Hz. In the final step, the 14 bit A/D conversed data is sent by the transmit path to the DSP engine for further signal processing.

14.9.2.2 Receive Path in ΣΔ CODEC-Filter

A 14-bit linear digital signal from the DSP engine is first passed to the digital anti-aliasing interpolation filter block. The interpolation block performs the reverse operation of the decimation filter (described above in the transmit path) and the sampling rate will be increased from 8 KHz (14 bits) to 1.536 MHz (14 bits). The digital demodulator will then reduce the 14-bit samples (1.024 MHz) to 1 bit (1.536 MHz). The digital output signal will be passed to a 3400 Hz switched capacitor low-pass filter with sin(x)/x correction and an analog smoothing filter to reduce the spectral components of the switched capacitor filter. Finally, the analog output signal is sent to the unit gain power amplifier RO, which is capable of driving a 2 KΩ load connected to the VAG pin.

The last stage of the received path is a pair of power driver PO1- (PO2-) and PO1+ (PO2+) which is connected in a push-pull (differential) configuration. The PO driver can accommodate large gain ranges by adjusting two external resistors for applications such as driving a handset receiver (or a speaker). This differential circuit is capable of driving a 120 Ω (16Ω) load.

14.9.3 Control Register: CODEC_CTRL

The functional description and read/write status of each bit are illustrated in this section. The read or write status of each bit is indicated by the symbol R or W described in Table 14-1.

SYMBOL	TYPE	MEANING
R/W	Read/Write	Data may be read or written by micro-processor.

Table 14-1: Read/Write status description in control register

Address	Access Mode	Value At Reset	Nominal Value
0x1509	R/W	0xC0	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CODEC DigDis	CODECAPd	Reserved	Reserved	Analog Loopback	Reserved	Reserved	Reserved

CODECDigDis [Bit7]: =1, Disable the CODEC digital part,

=0, Enable the CODEC digital part.

CODECAPd [Bit6]: =1, To disabled the CODEC analog part to save power. Especially when using the PDM mode sounder signal, only the CODEC digital filter is necessary.

=0, CODEC analog part enabled.

Analog Loopback [Bit 3]: =1, Setting this bit causes an analog loopback from the receive path to the transmit path. Internally the RO output in the receive path is routed to the transmit gain control in the transmit path; the op-amp TG is bypassed. This feature is useful for self-testing to neglect the external connecting circuit, shown in Figure 14-7.

.

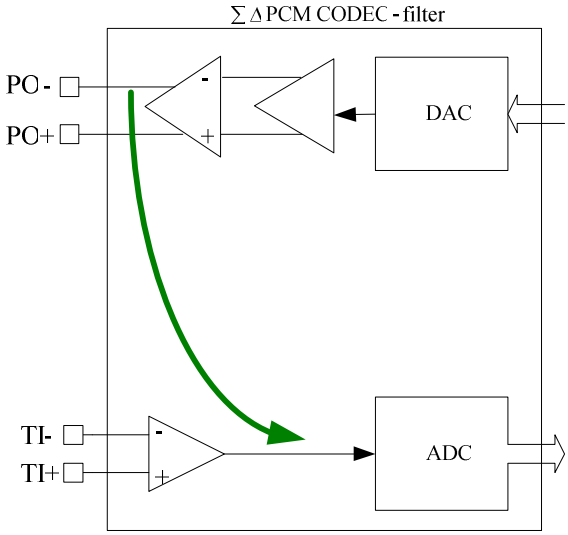


Figure 14-7 The signal flow of Analog Lookback

14.9.4 Specific Register

Address	Access Mode	Value At Reset	Nominal Value
0x150A	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Blocked (for test modes)							

14.9.5 Specific Register

Address	Access Mode	Value At Reset	Nominal Value
0x150B	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Blocked (for test modes)	RESERVED	RESERVED	RESERVED	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)

14.10 RECEIVE_DIAG

Address	Access Mode	Value At Reset	Nominal Value
0x150C	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	P3.5_A1 _Sel	P3.4_A0 _Sel	CS3_Enable	P1.4_WaitState_Sel	P1.5_Sel	P1.6_Sel[1]	P1.6_Sel[0]

B[1:0]	P1.6_Sel[1:0]=	0,	Pin 44= P1.6	Port 1 Bit 6 of embedded T8032.
		1,	Pin 44= X	Undefined. signal.
		2,	Pin 44= X	Undefined. signal.
		3,	Pin 44= P1.6	Port 1 Bit 6 of embedded T8032.
B[2]	P1.5_Sel=	0	Pin 45= P1.5 or /CS3	Port 1 Bit 5 of embedded T8032 or External chip select.
		1	Pin 45= X	Undefined. signal
B[3]	P1.4_waitstate_sel=	0,	Pin 46= P1.4	Port 1 Bit 4 of embedded T8032.
		1,	Pin 46= wait state input	The input pin with pull-high can receive wait signal from external device.
B[4]	CS3_Enable=	0	Pin 45= P1.5	Port 1 Bit 5 of embedded T8032.
		1	Pin 45= /CS3	External chip select.
B[5]	P3.4_A0_Sel=	0,	Pin37= P3.4	Port 3 Bit 4 of embedded T8032.
		1,	Pin37= A0	A0 address of embedded T8032.
B[6]	P3.5_A1_Sel=	0,	Pin36= P3.5	Port 3 Bit 5 of embedded T8032.
		1,	Pin36= A1	A1 address of embedded T8032.

※ If KR is used as GPIO function besides setting SPI_Enable 0x1720 [7] = 0 (disable SPI), 0x150C [7] must be set “0”.

The usages of pin44 and pin45 are illustrated in Figure 14-8.

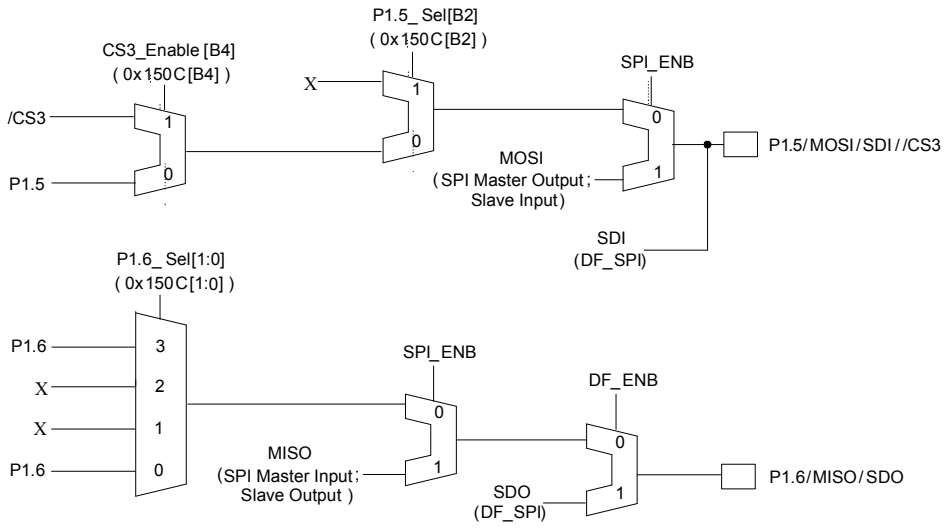


Figure 14-8 The Multiplexers of pin44 and pin45

The usages of pin36 and pin37 are illustrated in Figure 14-9.

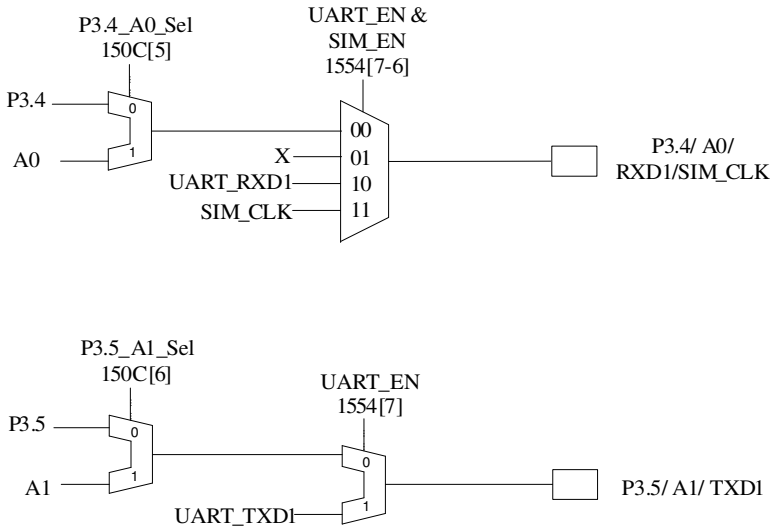


Figure 14-9 The Multiplexers of pin36 and pin37

14.11 Specific Register

Address	Access Mode	Value At Reset	Nominal Value
0x150D	R/W	0x19	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)

14.12 EnAllClock

Address	Access Mode	Value At Reset	Nominal Value
0x150E	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SpeedUp32K	RESERVED	RESERVED	RESERVED	Dump mask Rom	8032 clk output selection	Read MASK ROM Enable	EnAllClock

EnAllClock — when set, most of the clocks will be enabled.
Read Mask ROM Enable — when set, enable read_access for MASK ROM
8032 clk output selection — when set, P1.4 will output system clock used by on chip TB8032. If chip is configured as double system clock speed, it output the x2 system clock.
Dump mask Rom — when set, enable MASK ROM test mode.
SpeedUp32K — when set, 32k clock will replace with 13.824 system clock for speed up testing.

14.13 CODEC_Test_Sel

Address	Access Mode	Value At Reset	Nominal Value
0x150F	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
codec_test _sel[7]	codec_test _sel[6]	codec_test _sel[5]	codec_test _sel[4]	codec_test _sel[3]	codec_test _sel[2]	codec_test _sel[1]	codec_test _sel[0]

Codec_test-sel[3:0]
=0001, loopback DA output.
=0010, loopback AD output.
=0011, assign DA output to “0”.
=0100, loopback DA input.
=0101, test ALU function.
=0110, set value to internal register D2.
=0111, calculate checksum of code ROM.
=1000, calculate checksum of coefficient ROM.
=1001, route external input (pDR) to AD input.
=1010, output code ROM content.
=1011, output coefficient ROM content.

Codec_test-sel[7:4]
=0001, 1-bit AD input.
=0010, ADC FIFO pointer.
=0011, ADC 1st -stage SINC filter output.
=0100, ADC 2nd –stage SINC filter output.
=0101, ADC LPF output.
=0110, ADC HPF output.
=0111, ADC output.
=1000, DAC input.
=1001, DAC 1st –stage SINC filter output.
=1010, DAC LPF output

=1011, DAC 2nd –stage SINC filter output.
=1100, 1-bit DA output.
=1101, DAC FIFO pointer.

14.14 Test_SYSCLKOUT

Address	Access Mode	Value At Reset	Nominal Value
0x1510	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Test_SYSCLKOUT	Blocked (for test modes)

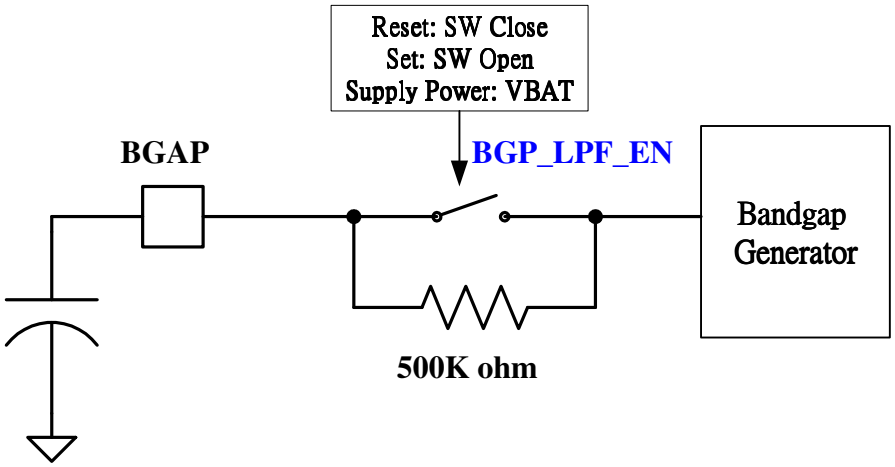
Test_SYSCLKOUT When set, the SYSCLKOUT signal switches to pin RESET_OUT.

14.15 BGP_LPF_EN

Address	Access Mode	Value At Reset	Nominal Value
0x1511	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BGP_LPF_EN	Blocked (for test modes)			Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)

BGP_LPF_EN When set, the switch is open and bandgap low pass filter is enabled.
When reset, the switch is close and bandgap low pass filter is disabled.



14.16 CODEC Status Indicator

Address	Access Mode	Value At Reset	Nominal Value
0x1512	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	ADC_FIFO_Overflow	ADC_FIFO_Underflow	DAC_FIFO_Overflow	DAC_FIFO_Underflow	ADC_SINC_Overflow	ADC_SINC_Underflow

ADC_FIFO_OverflowFIFO pointer overflow in the ADC path.
ADC_FIFO_underflowFIFO pointer underflow in the ADC path.
DAC_FIFO_OverflowFIFO pointer overflow in the DAC path.
DAC_FIFO_underflowFIFO pointer underflow in the DAC path.
ADC_SINC_OverflowOverflow indication for ADC SINC filter.
ADC_SINC_UnderflowUnderflow indication for ADC SINC filter.

14.17 BandGap Voltage Adjustment

Address	Access Mode	Value At Reset	Nominal Value
0x1513	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Vbgp_trimming[5:0]					

Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
±	80mV	40mV	20mV	10mV	5mV

Bandgap voltage is default 1V. You can fine tune bandgap voltage follow below formula.
When set Vbgp_trimming[5] = 1, BandGap Voltage = 1V − 5mV * Vbgp_trimming[4:0]
When set Vbgp_trimming[5] = 0, BandGap Voltage = 1V +5mV * Vbgp_trimming[4:0]
Where Vbgp_trimming [4:0] is a decimal value and ranges from 0 to 31

14.18 Specific Register

Address	Access Mode	Value At Reset	Nominal Value
0x1514	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Blocked (for test modes)	Blocked (for test modes)			Blocked (for test modes)	Blocked (for test modes)		

14.19 Linear Regulator Voltage Controller Register

Address	Access Mode	Value At Reset	Nominal Value
0x1515	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	REG_LV[1]	REG_LV[0]	RESERVED	RESERVED

The output voltage of the embedded linear regulator (REG) is correlated to the internal bandgap voltage. Any tolerance and deviation of the bandgap voltage will cause a deviation of the output voltage of the embedded linear regulator. In order to ease the usage, the adjustment possibilities of output voltage of the linear regulator have been built in to compensate the bandgap variation in process.

REG_LV[1:0]

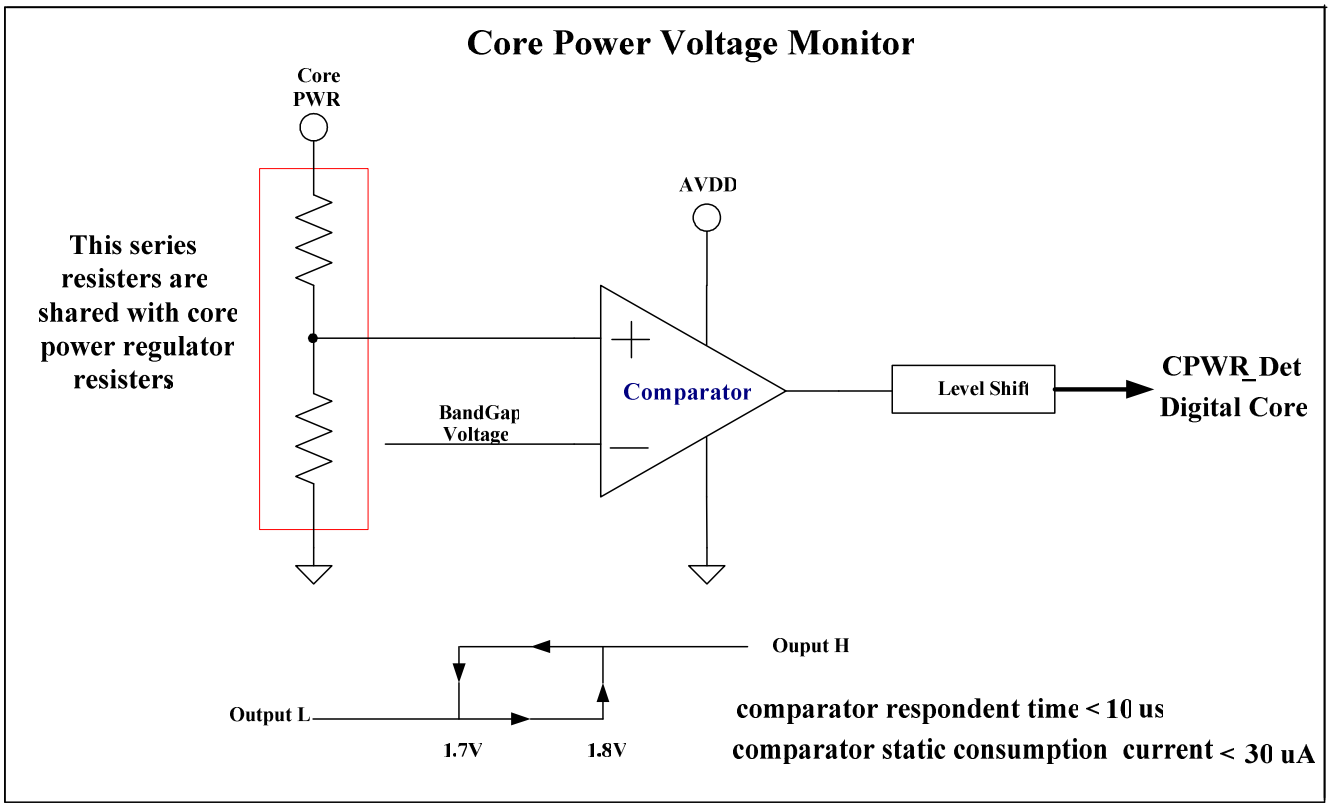
REG_LV [1:0]	REG Output Voltage
00	3.0V
01	3.1V
10	3.2V
11	3.3V

14.20 Core PWR_Det

Address	Access Mode	Value At Reset	Nominal Value
0x1518	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	CPWR_Det	RESERVED	RESERVED	Blocked (for test modes)	Blocked (for test modes)

CPWR_Det This bit is for core power voltage monitor purpose and read only. When the core power voltage is below 1.7V, this bit will set to low. If the core power voltage is above 1.8V, this bit will set to high. Normally, the core power voltage is 1.9V. This core power voltage monitor function can generate the interrupt and locate at 0x144D[5] register.



14.21 DA High Pass Filter Selection

Address	Access Mode	Value At Reset	Nominal Value
0x151A	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Disable HPF	DA_dither_select	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Disable HPF when set, disable the High Pass filter D to A directory
DA_ditehr_select when set, change D to A dither function is add level (no sign)

14.22 TI Path Selection

There is a multiplexer at the input stage to choose which the receiving signal comes from

Address	Access Mode	Value At Reset	Nominal Value
0x1521	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	TI2NtoPO2	TI2NtoPO1	RESERVED	TI2_Buffer_SEL	Blocked (for test modes)	Path_SEL

Path_SEL When set, the signal is come from TI1- and TI1+ terminal to internal TG OP Amp
When reset, the signal is come from TI2- and TI2+ terminal to internal TG OP Amp

TI2_Buffer_SEL When set this bit, the TI2 input will provide high input impedance to meet application requirement.

TI2NtoPO1 When set, the signal TI2N will be connected to internal PO1 Amp.
When reset, the signal TI2N will be disconnected to internal PO1 Amp.

TI2NtoPO2 When set, the signal TI2N will be connected to internal PO2 Amp.
When reset, the signal TI2N will be disconnected to internal PO2 Amp.

The multiplexers of the TI Path Selection are shown in Figure 14-10.

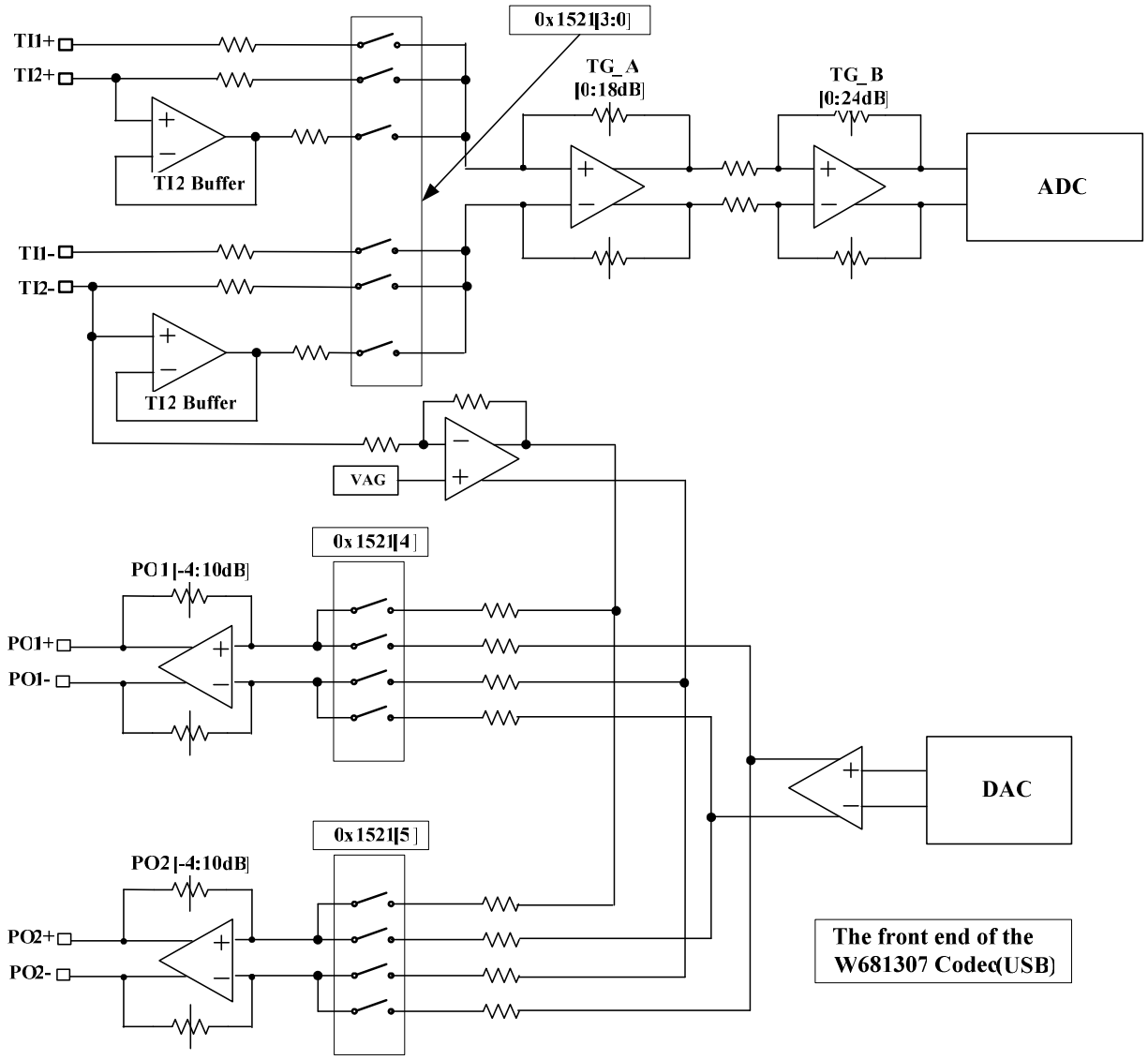


Figure 14-10 The multiplexers of the TI Path Selection

15. SERIAL PERIPHERAL INTERFACE

15.1 Serial Peripheral Interface – SPI signals

- SCK: Input pin in slave mode; output pin in master mode. Serial Clock from Master. Max clock rate is TBD MHz (depends on how fast the CPU to read a word of received data).
- /SPI_CS: Input pin in slave mode; output pin in master mode. Low active Chip Select signal from Master.
- MISO: Output pin in slave mode; input pin in master mode. Slave data out to the input of Master.
- MOSI: Input pin in slave mode; output pin in master mode. Master data out to the input of Slave.

If the phase of the clock is zero, i.e. CPHA = 0, data is latched at the rising edge of the clock with CPOL = 0, and at the falling edge of the clock with CPOL = 1. If CPHA = 1, the polarities are reversed. CPOL = 0 means falling edge, CPOL = 1 rising edge. The transmission clock edges are the reversed of sampling edges, shown in Figure 15-1. Timing diagram of CPHA = 0 and CPHA = 1 is shown in Figure 15-2 and Figure 15-3.

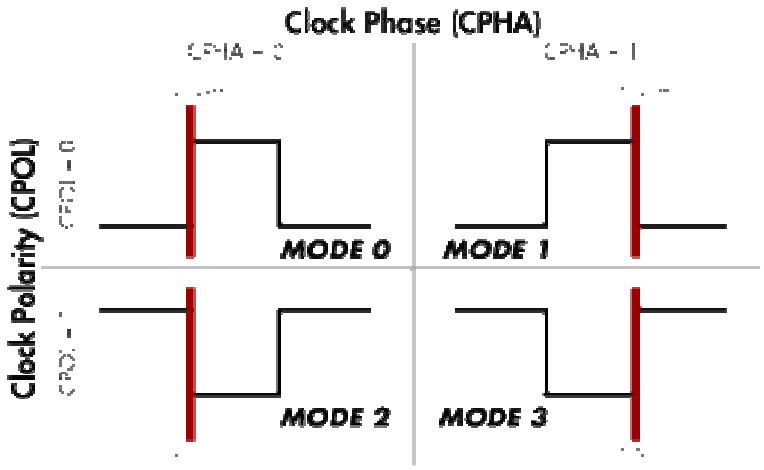


Figure 15-1 Sampling edges of different modes

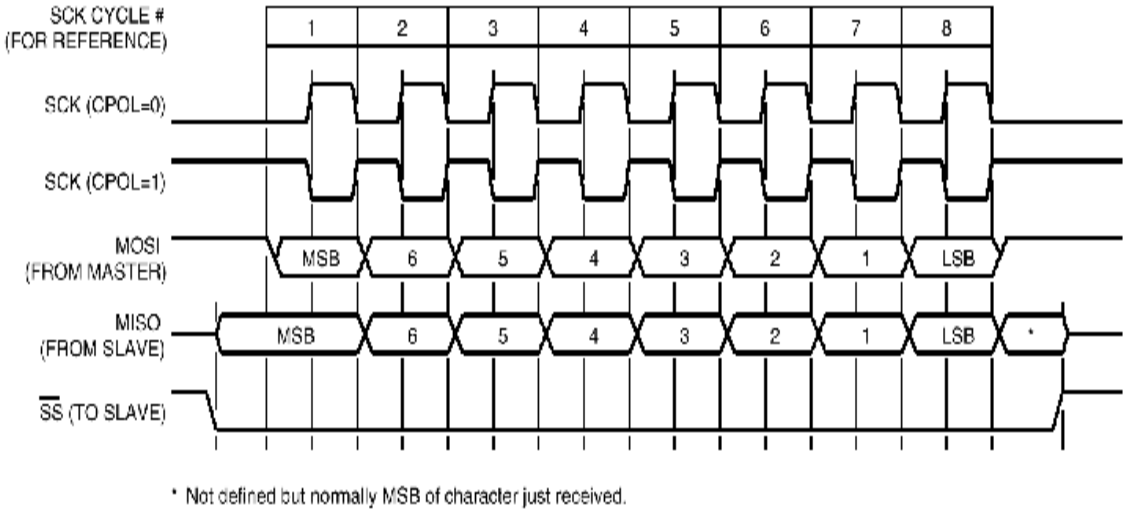
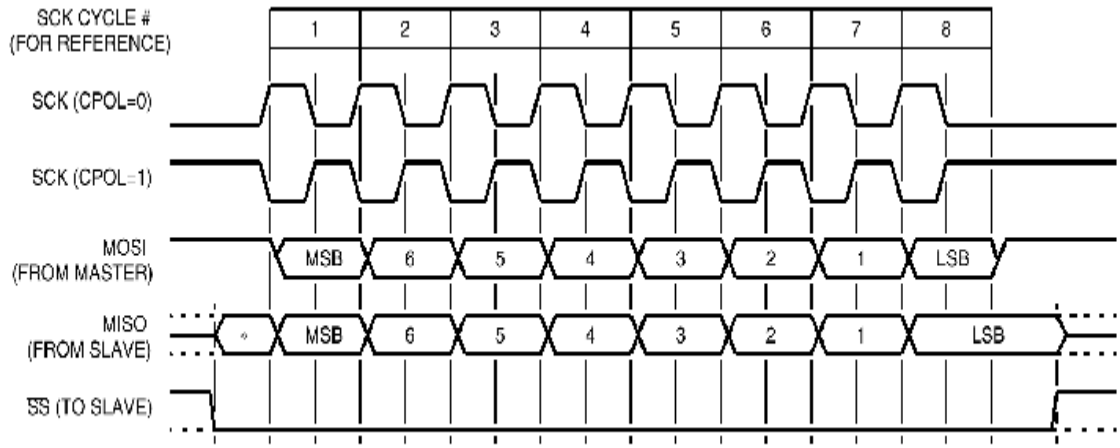


Figure 15-2 Timing diagram of CPHA = 0 ($\overline{SS}$ is the pin /SPI_CS)



*Not defined but normally LSB of previously transmitted character.

Figure 15-3 Timing Diagram of CPHA = 1 ($\overline{SS}$ is the pin /SPI_CS)

15.1.1 SPI_Control 0

Address	Access Mode	Value At Reset	Nominal Value
0x1720	R/W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPI_Enable	SPI_Master_Mode	Reserved	Reserved	DumpComp	Reserved	CPHA	CPOL

SPI_Enable SPI interface enable. If SPI_ENB=0, the SPI is disabled and pins defined as original functions. Default to 0.
Spi_master_mode set to 1 in master mode. Default to slave mode
CPOL Clock polarity, if CPOL=0, clock is active high; if CPOL=1, clock is active low. Default to 0.
CPHA Clock Phase, determined the sampling clock edge of SCLK. Default to 0.
DumBcomp When this bit is on and the received byte is the same as Dumpbyte (0x1724), then no write to RX fifo.
SPI mode 0 = 0x80; SPI mode 1 = 0x82; SPI mode 2 = 0x81; SPI mode 3 = 0x83;
Note: 0x1720[1:0] = '10' is mode 1 in figure 1; 0x1720[1:0] = '01' is mode 2 in figure 1.

15.1.2 SPI_Control 1

Address	Access Mode	Value At Reset	Nominal Value
0x1721	R/W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPI_Clock		Reserved	Reserved	RxDepth_intr[3:0]			

SPI_Clock Set master spi clock speed. **(Master mode only)**

00	1.152MHz
01	576KHz
10	256KHz
11	64KHz

The SPI in slave mode support maximum clock speed is 576K.

Rxdepth_intr An RxINT interrupt event 1723[bit 4] is generated when received byte count reaches Rxdepth_intr[bit 3:0] +1 bytes.

15.1.3 SPI Status

Address	Access Mode	Value At Reset	Nominal Value
0x1722	R	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	RxFIFOgeThreshold	TxEmpty	RxEmpty	TxOverflow	RxOverflow

RxOverflow When SPI keeps on receiving data and Rx-FIFO is full, the RxOverflow will be set to 1.
TxOverflow When 8032 writing data is fast than SPI transmitting rate, the Tx-FIFO will overflow indicated by TxOverflow bit.
RxEmpty Indicate the Tx-FIFO is currently empty.
TxEmpty Indicate the Tx-FIFO is currently empty.
RxFIFOgeThreshold When RX-FIFO reach to RxDepth_intr (0x1721[3:0]), the RxFIFOgeThreshold will set to 1.

15.1.4 SPI Interrupt Enable

Address	Access Mode	Value At Reset	Nominal Value
0x1723	R/W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	RxInt	TxEmpty	Reserved	TxOverflow	RxOverflow

According to 0x1722, these interrupts will occur if the corresponding interrupts enable.

RxOverflow Rx overflow interrupt enable.
TxOverflow Tx overflow interrupt enable.
TxEmpty Tx empty interrupt enable. (Recommended this bit served in low data rate interface application.)
RxInt Rx interrupt enable. RX interrupt occurs upon the number of rx data reaches Rxdepth_intr[3:0].

15.1.5 DumpByte

Address	Access Mode	Value At Reset	Nominal Value
0x1724	R	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DumpByte[7:0]							

If 1720[3] DumpCmp is set to "1", the received byte will be filtered out (No Write to RX-FIFO) when DumpByte is equal to Received Byte.

15.1.6 Write TX FIFO

Address	Access Mode	Value At Reset	Nominal Value
0x1725	W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TxFIFO[7:0]							

Store data in SPI TX-FIFO when micro controller writes data to this register.

15.1.7 Read RX FIFO

Address	Access Mode	Value At Reset	Nominal Value
0x1726	R	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxFIFO[7:0]							

Read data from SPI RX-FIFO when micro controller read data from this register.

15.1.8 SPI_Transfer_Size

Address	Access Mode	Value At Reset	Nominal Value
0x1727	R/W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Transfer Size [3:0]			

SPI_Transfer_Size perform (transfer size+1) bytes of Tx/Rx when start_rtx is set. (**master mode only**)

15.1.9 SPI_Start_rtx

Address	Access Mode	Value At Reset	Nominal Value
0x1728	R/W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Start_rtx

Start_rtx Set to 1 to start Tx/Rx for (transfer size+1) bytes; cleared by hardware automatically when it is done. (**master mode only**)

16. SPI FOR SERIAL DATA FLASH

16.1 Introduction to SPI of Serial Data Flash

Winbond W681307 chip embed a SPI of serial data flash (DF_SPI) port which is a 4-pin (SCK, /DF_CS, SDI, SDO) SPI Interface. This SPI interface makes W681307 chip easy to control 4-pin Serial Peripheral Interface (SPI) Data Flash memories. It has various clock speed and data format configurations by setting control register. The SPI interface can be operated at clock rates of up to CPU CLK frequency / 2.

16.2 Block Diagram

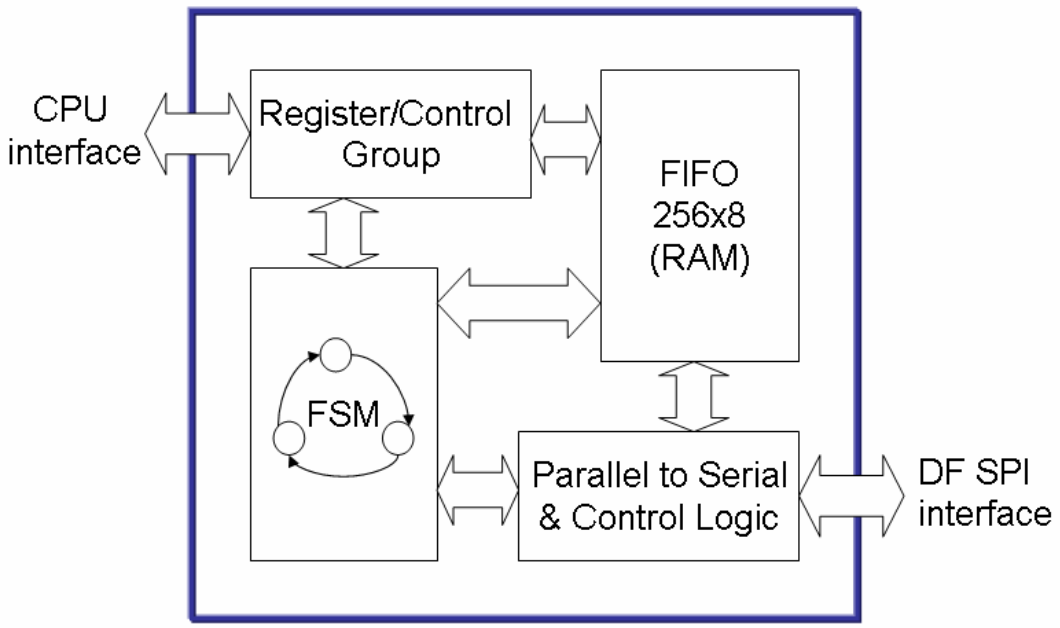
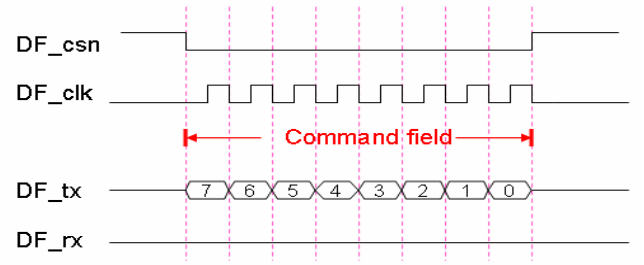


Figure 16-1 The SPI of the Serial Data Flash block diagram

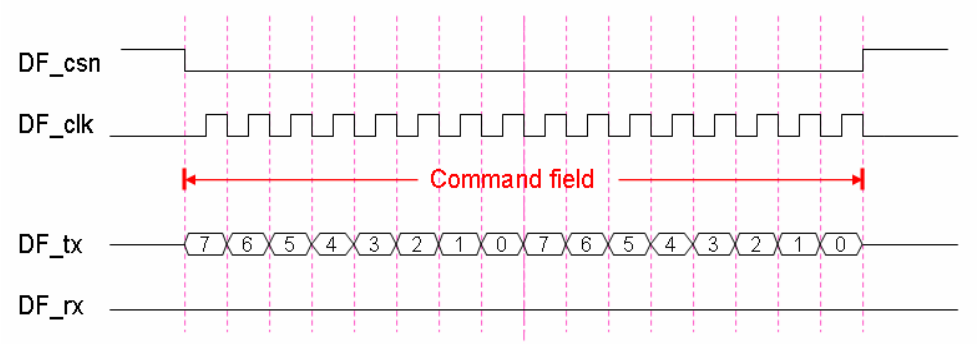
16.3 Data Format

The packet/page data format is separated to 2 fields. First one is the Command field, and the second one is Data field. Command field (1 ~ 5 bytes) is used to send the control instruction/code and access address. The Data field (0 ~ 256 bytes) is used to send/store the write/read data of serial data flash. All of Command and Data bytes are sand MSB first.

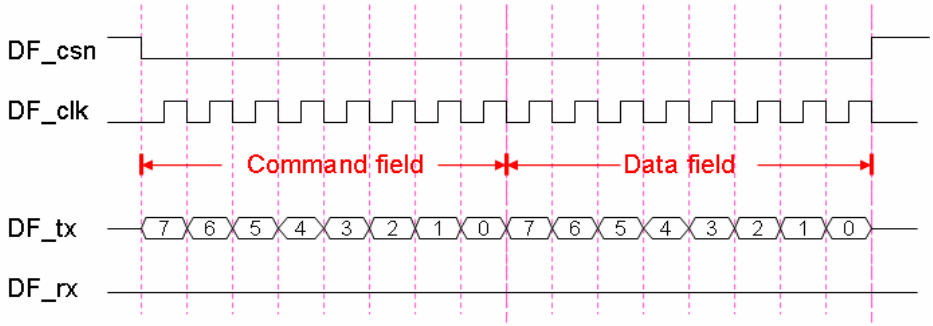
◆ Example 1: Single Byte Command Only



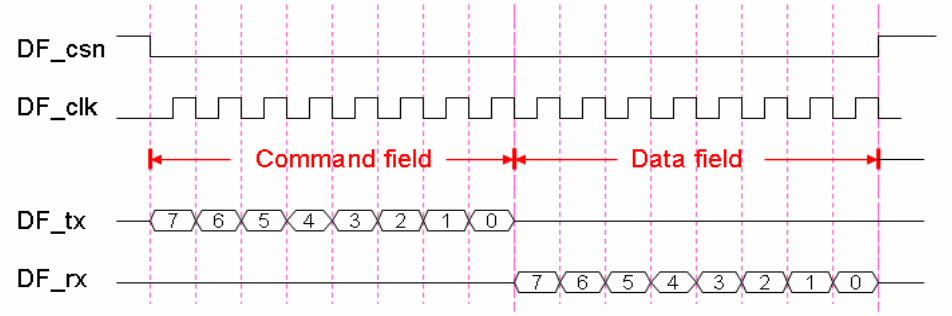
◆Example 2: Multiple Bytes Command only



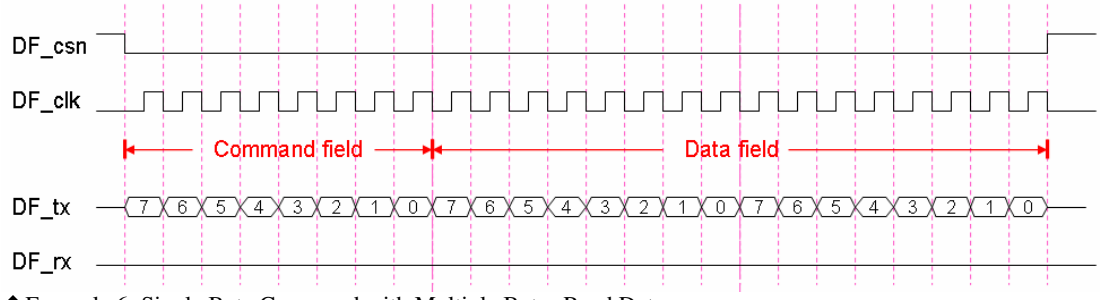
◆Example 3: Single Byte Command with Single Byte Write Data



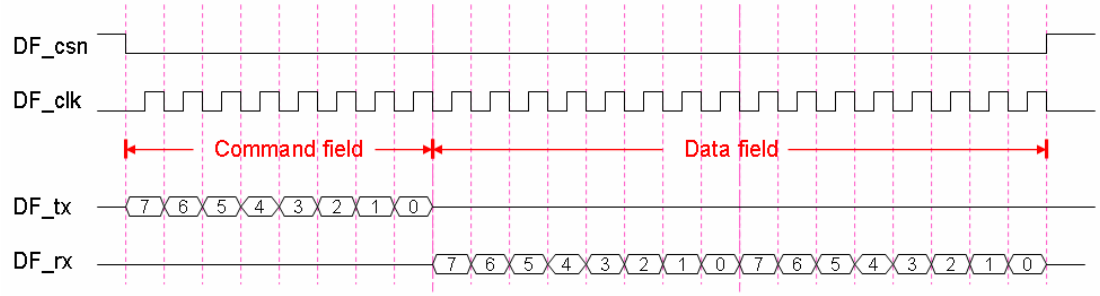
◆Example 4: Single Byte Command with Single Byte Read Data



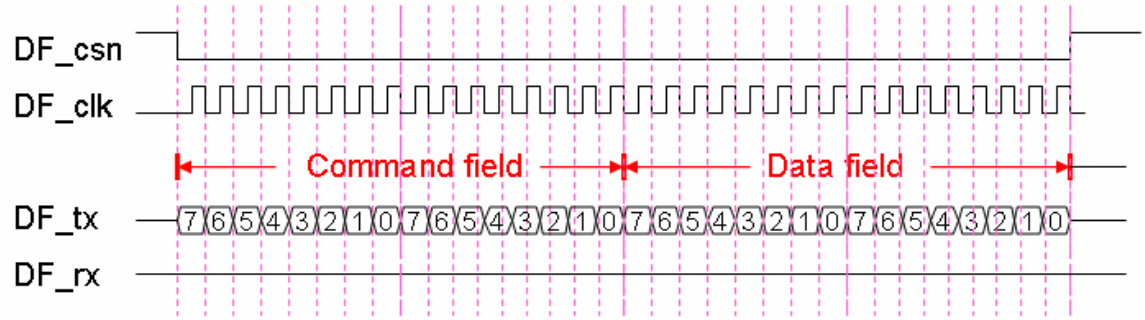
◆Example 5: Single Byte Command with Multiple Bytes Write Data



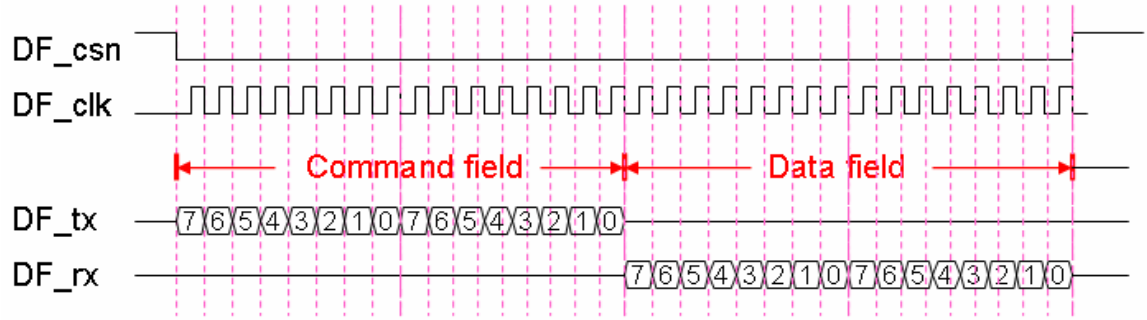
◆Example 6: Single Byte Command with Multiple Bytes Read Data



◆Example 7: Multiple Bytes Command with Multiple Bytes Write Data



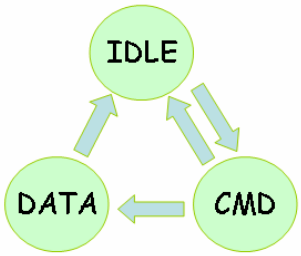
◆Example 8: Multiple Bytes Command with Multiple Bytes Read Data



Both command and data field length can be program with write the CMD_LEN (REG 0x1731[2:0]) and DATA_LEN (REG 0x1732[7:0]). The MAX command field length is 5 bytes. The MAX data field length is 256 bytes.

16.4 FSM

There have 3 states in the DF_SPI module : IDLE, CMD and DATA.



Step1. While power on reset, the FSM initial is in the IDLE state.
Step2. After enable the DF_SPI function (write REG 0x1730[7]=1), the FSM start to wait the CPU control to change to CMD state (write REG 0x1731), then force control logic to shift out the command bytes sequentially to serial data flash.
Step3. After finished shift out the command bytes, the FSM will change to DATA state if the Data_enb (REG 0x1731[4]) is true, or run back to IDLE state if the Data_enb is false.
Step4. When FSM goes into Data state, the control logic will start to shift out the write out data to serial data flash if DF_RD (REG 0x1731[3]) is false, or shift in the read back data from serial data flash if DF_RD (REG 0x1731[3]) if true.
Step5. After finished shift out/in the data bytes, the FSM will go back to IDLE state, and wait for next transition.

16.5 FIFO/RAM

The DF_SPI module takes 5 bytes register to write the control command and takes the 256x8 bytes RAM to do the Read/Write access FIFO. It supports 2 kinds of memory access method：

Type1. FIFO like method:
The CPU always read/write the same address, then the hardware control the memory read/write address, and increase the read/write point automatically after each read/write. The current write/read point can be read back at REG 0x173E/0x173F.
Type2. Direct access method:
The CPU can read/write any byte of the memory with write the read (REG 0x173F)/write (REG 0x173E) point first.

16.6 Interrupt

The DF_SPI module supports two kinds of interrupt source. One is the TX/RX finish interrupt, occur while TX/RX byte counts (REG 0x173D) is equal to DATA_LEN, the other is middle flag interrupt, occur while TX/RX byte counts (REG 0x173D) is equal to the 16 * INTR_CNT (REG 0x1733[7:4]). Any other concept, please reference to the description of the registers.

16.7 DF_SPI Register Group

16.7.1 DF_CLK

Address	Access Mode	Value At Reset	Nominal Value
0x1730	R/W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DF_ENB	CLK_REG [6:0]						

CLK_REG

Clock Divider Base to decide the DF_clk clock frequency.
DF_CLK freq. = CPU CLK freq. / (CLK_REG + 1)
EX: CLK_REG [6:0] = 0x01→ DF_CLK freq. = CPU CLK freq. / 2
CLK_REG [6:0] = 0x03 → DF_CLK freq. = CPU CLK freq. / 4
Note: CLK_REG [6:0] must ≥ 1 while DF_CLK active.

DF_ENB — When set, enable DF_SPI module.
When reset, disable DF_SPI module.
Note: The FIFO/RAM only can be access while this bit is set enable.

16.7.2 DF_CMD_LEN

Address	Access Mode	Value At Reset	Nominal Value
0x1731	R/W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			DATA_ENB	DF_RD	CMD_LEN [2:0]		

CMD_LEN — Command Field Length. (unit: byte,CMD_LEN ≦ 4)
Command Field Length = CMD_LEN + 1
EX: CMD_LEN = 0x03 → Command Field Length = 4 bytes.

DF_RD — Read/Write Flag. (1: Read,0: Write)

DATA_ENB — Enable Data Field. (1: Enable, 0: Disable)

Note: While DF_ENB = 1, write this byte will force DF module start to TX/RX

16.7.3 DF_DATA_LEN

Address	Access Mode	Value At Reset	Nominal Value
0x1732	R/W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DATA_LEN [7:0]							

DATA_LEN — Data Field Length.(unit: byte)
Data Field Length = DATA_LEN + 1
EX: DATA_LEN = 0x0F → Data Field Length = 16 bytes.

16.7.4 DF_INTR_REG

Address	Access Mode	Value At Reset	Nominal Value
0x1733	R/W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTR_CNT [3:0]				RD_FLAG	RX_OK	TX_OK	INTR_ENB

INTR_ENB — When set, enable DF module interrupt.
When reset, disable DF module interrupt.
This module support 2 kind of interrupt source. One is the TX/RX Finished interrupt (occurred while TX/RX bytes = DATA_LEN), the other is internal pre-interrupt (occurred while TX/RX bytes = INTR_CNT * 16).

TX_OK — TX Finish Interrupt.(Read Only)
This bit will be clear automatically while next TX/RX

RX_OK	RX Finish Interrupt.(Read Only) This bit will be clear automatically while next TX/RX
RD_FLAG	The same with DF_RD. (Read Only)
INTR_CNT	Internal Pre Interrupt. Internal interrupt @ TX/RX byte count = (INTR_CNT * 16). If want to disable the internal pre-interrupt, please set INTR_CNT = 0 While internal pre-interrupt occurred, the interrupt status TX_OK/RX_OK will be both zero. The RD_FLAG will indicate the pre-interrupt is TX or RX. EX:INTR_CNT [3:0] = 0x01 → internal interrupt @ TX/RX = byte 16.

16.7.5 DF_CMD_B1 ~ DF_CMD B5

Address	Access Mode	Value At Reset	Nominal Value
0x1734	R/W	00	

Address	Access Mode	Value At Reset	Nominal Value
0x1735	R/W	00	

Address	Access Mode	Value At Reset	Nominal Value
0x1736	R/W	00	

Address	Access Mode	Value At Reset	Nominal Value
0x1737	R/W	00	

Address	Access Mode	Value At Reset	Nominal Value
0x1738	R/W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD_B1 [7:0]							
CMD_B2 [7:0]							
CMD_B3 [7:0]							
CMD_B4 [7:0]							
CMD_B5 [7:0]							

CMD_B1	Command Byte 1.(0x1734)
CMD_B2	Command Byte 2.(0x1735)
CMD_B3	Command Byte 3.(0x1736)
CMD_B4	Command Byte 4.(0x1737)
CMD_B5	Command Byte 5.(0x1738)

16.7.6 DF_CLK_FORMAT

Address	Access Mode	Value At Reset	Nominal Value
0x173B	R/W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				CSN_MORE	CK_MORE	CP	CI

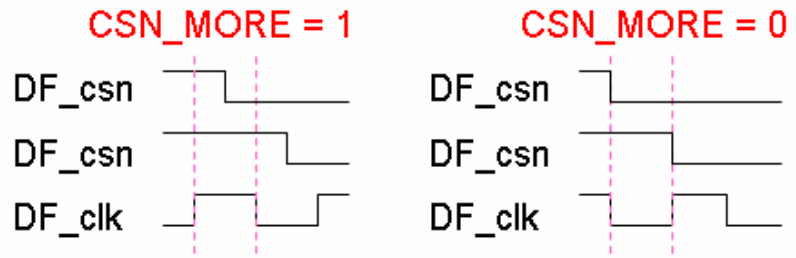
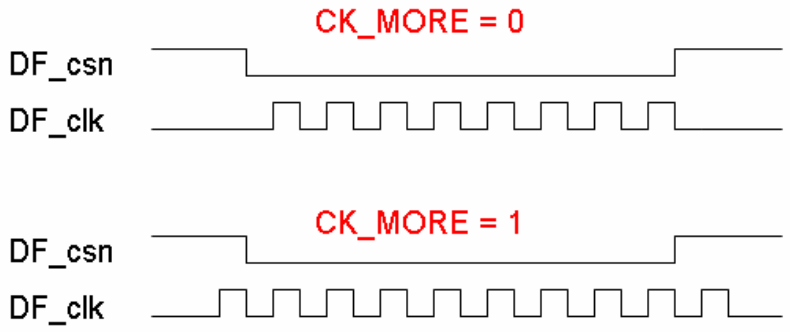
There have 4 control bits (CSN_MORE, CK_MORE, CP and CI) to decide the DF_SPI data format.

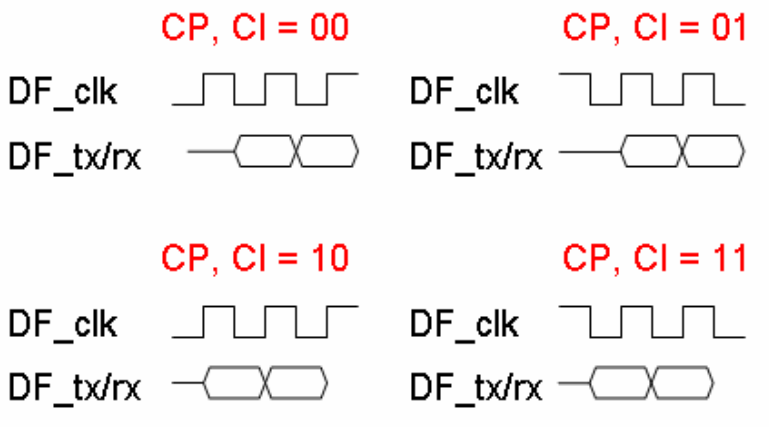
CSN_MORE — When set, DF_CSN toggling only while DF_CLK stable.

CK_MORE — Extend one more clock before/after signal DF_CSN active.

CP — DF_CLK transition position setting.
When CP = 1, DF_CLK start toggling in the middle of transfer.
When CP = 0, DF_CLK start toggling at the beginning of transfer.

CI — DF_CLK level while DF_CSN is non active.
When CI = 1, DF_CLK is high while DF_CSN is non active.
When CI = 0, DF_CLK is low while DF_CSN is non active.

CSN_MORE	When set, DF_CSN toggling only while DF_CLK stable. 
CK_MORE	Extend one more clock before/after signal DF_CSN active. 
CP	DF_CLK transition position setting. -- When CP = 1, DF_CLK start toggling in the middle of transfer. -- When CP = 0, DF_CLK start toggling at the beginning of transfer.

	
CI	DF_CLK level while DF_CSN is non active -- When CI = 1, DF_CLK is high while DF_CSN is non active. -- When CI = 0, DF_CLK is low while DF_CSN is non active.

Note: For W25X and W25P serial SPI-Flash, these control bits are all zeros.

16.7.7 DF_FIFO_DATA

Address	Access Mode	Value At Reset	Nominal Value
0x173C	R/W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO_DATA [7:0]							

FIFO_DATA — TX/RX FIFO Read/Write data.
When write this byte, i.e. put transmit data into FIFO.
When read this byte, i.e. read back the current data in FIFO.
After Read/Write this byte, the CPU read/write point will increase one automatically.

16.7.8 DF_CNT

Address	Access Mode	Value At Reset	Nominal Value
0x173D	R	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DF_CNT [7:0]							

DF_CNT — Current TX/RX byte count point.

16.7.9 DF_WR_CNT

Address	Access Mode	Value At Reset	Nominal Value
0x173E	R/W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DF_WR_CNT [7:0]							

DF_WR_CNT CPU current write-point. (unit: byte)
Write this byte will force CPU write point set to the DF_WR_CNT value.

16.7.10 DF_RD_CNT

Address	Access Mode	Value At Reset	Nominal Value
0x173F	R/W	00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DF_RD_CNT [7:0]							

DF_RD_CNT CPU current read-point. (unit: byte)
Write this byte will force CPU read point set to the DF_RD_CNT value.

16.8 Example of W25X20/40/80 Serial Flash

1. Write Enable(0x1734 = 06) / Write Disable(0x1734 = 04) / Chip Erase(0x1734 = C7) / Power-down(0x1734 = B9)
   - 0x1730 = 0x81// Set DF_enb, CLK = CPU clock / 2
   - 0x1734 = 0x06// Set CMD Byte1 0x06 / 0x04 / 0xC7 / 0xB9 (code)
   - 0x1731 = 0x00// Force 1 byte TX (CMD)

2. Read Status Register(0x1734 = 05)
   - 0x1730 = 0x87// Set DF_enb, CLK = CPU clock / 8
   - 0x1732 = 0x00// Set CMD Data Field Length = 1 byte
   - 0x1734 = 0x05// Set Byte1 0x05 (code)
   - 0x1731 = 0x18// Force 1 byte TX (CMD), and 1 byte RX

3. Write Status Register(0x1734 = 01)
   - 0x1730 = 0x8A// Set DF_enb, CLK = CPU clock / 11
   - 0x1734 = 0x01// Set CMD Byte1 0x01 (code)
   - 0x1735 = 0x04// Set CMD Byte2 0x04 (S7-S0)
   - 0x1731 = 0x01// Force 2 bytes TX (CMD)

4. Block Erase(0x1734 = D8) / Sector Erase(0x1734 = 20)
   - 0x1730 = 0x8A// Set DF_enb, CLK = CPU clock / 11
   - 0x1734 = 0xD8// Set CMD Byte1 0xD8 / 0x20 (code)
   - 0x1735 = 0x34// Set CMD Byte2 0x34 (A23-A16)
   - 0x1736 = 0x35// Set CMD Byte3 0x35 (A15-A8)
   - 0x1737 = 0x36// Set CMD Byte4 0x36 (A7-A0)
   - 0x1731 = 0x03// Force 4 bytes TX (CMD)

5. Read Data (0x1734 = 03)
   - 0x1730 = 0x8B// Set DF_enb, CLK = CPU clock / 12
   - 0x1732 = 0x0F// Set Data Field Length = 16 bytes
   - 0x1733 = 0x01// Enable Interrupt
   - 0x1734 = 0x03// Set CMD Byte1 0x03 (code)
   - 0x1735 = 0x04// Set CMD Byte2 0x04 (A23-A16)
   - 0x1736 = 0x05// Set CMD Byte3 0x05 (A15-A8)
   - 0x1737 = 0x06// Set CMD Byte4 0x06 (A7-A0)
   - 0x1731 = 0x1B// Force 4 bytes TX (CMD), and 16 bytes RX (DATA)

6. Page Program (0x1734 = 02)
   - 0x1730 = 0x83// Set DF_enb, CLK = CPU clock / 4
   - 0x1732 = 0x0F// Set Data Field Length = 16 bytes
   - 0x1734 = 0x02// Set CMD Byte1 0x02 (code)
   - 0x1735 = 0x52// Set CMD Byte2 0x54 (A23-A16)
   - 0x1736 = 0x51// Set CMD Byte3 0x55 (A15-A8)
   - 0x1737 = 0x50// Set CMD Byte4 0x56 (A7-A0)
   - 0x173E = 0x00// Reset CPU write point to 0x00
   - 0x173C = 0xD0// Write Data Byte 1 (first data byte)
   - 0x173C = 0xDF// Write Data Byte 16 (last data byte)
   - 0x1731 = 0x13// Force 4 bytes TX (CMD), and 16 bytes TX (DATA)

7. Release Power-down and Device ID (0x1734 = AB)
   - 0x1730 = 0x84// Set DF_enb, CLK = CPU clock / 5
   - 0x1732 = 0x00// Set Data Field Length = 1 bytes
   - 0x1734 = 0xAB// Set CMD Byte1 0xAB (code)
   - 0x1735 = 0x00// Set CMD Byte2 0x00 (dummy)
   - 0x1736 = 0x00// Set CMD Byte3 0x00 (dummy)
   - 0x1737 = 0x00// Set CMD Byte4 0x00 (dummy)
   - 0x1731 = 0x1B// Force 4 bytes TX (CMD), and 1 byte RX (DATA)

8. Manufacturer-Device ID(0x1734 = 90)
   - 0x1730 = 0x85// Set DF_enb, CLK = CPU clock / 6
   - 0x1732 = 0x01// Set Data Field Length = 2 bytes
   - 0x1734 = 0x90// Set CMD Byte1 0x90 (code)
   - 0x1735 = 0x00// Set CMD Byte2 0x00 (dummy)
   - 0x1736 = 0x00// Set CMD Byte3 0x00 (dummy)
   - 0x1737 = 0x00// Set CMD Byte4 0x00 (00h)
   - 0x1731 = 0x1B// Force 4 bytes TX (CMD), and 2 bytes RX (DATA)

9. JEDECID(0x1734 = 9F)
   - 0x1730 = 0x85// Set DF_enb, CLK = CPU clock / 6
   - 0x1732 = 0x02// Set Data Field Length = 3 bytes
   - 0x1734 = 0x9F// Set CMD Byte1 0x9F (code)
   - 0x1731 = 0x18// Force 1 bytes TX (CMD), and 3 bytes RX (DATA)

17. WINBOND 2-WIRE SERIAL BUS

17.1 Introduction to Winbond 2-Wire Serial bus

Winbond 2-wire serial bus (W2S) is a simple bi-directional 2-wire bus for efficient inter-IC control. This design is for W2S master use only, and governed by micro controller, typically an 8032. The W2S used in the chip is used to both read/write from/to EEPROM and control melody device. The W2S master controller equips 35 bytes FIFO performing W2S formatting and de-formatting. The micro controller can simply fill up the FIFO contents which consists of target device ID, high/low address (depend on the device format); for reading, just set read enable , for writing, keep writing data to FIFO then set write enable to launch transmission. The W2S master controller supports up to 3 kinds of page writing, i.e. 8, 16, 32 bytes. The W2S master controller designed to support maximum 32 bytes per page, and the FIFO depth is calculated as 3 header bytes (one device ID, two address) plus 32 bytes for data. It has various bus speed configurations to support wide range of EEPROM bus speed.

17.2 The Description of W2S Register

17.2.1 W2S_Enable

Address	Access Mode	Value At Reset	Nominal Value
0x1740	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W2S_ENA	W2S_Port_Sel	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	W2S_HW _Protection

W2S_ENA: Set this bit will activate W2S bus controller.
W2S_Port_Sel: Pin selection for hardware W2S bus function.

W2S_Port_Sel	Pin name	
0	P1.2 : SDA0	P1.3 : SCL0
1	P1.3 : SDA1	P1.4 : SCL1

※ If W2S_HW_Protection is set to 1, the couple of pins set by bit W2S_Port_Sel become tri-state as core power below the operation voltage (see following table).

※ Micro-C must set W2S_ENA bit before setup Force_Activity (0x1745) register, and the content of W2S Status (0x1746) is valid only if W2S_ENA bits is set to 1.
W2S_HW_Protection: Set this bit will force W2S bus pins into tri-state output mode, when the CPWR_Det is low activity. Which pins will be forced to tri-state output is dependent on the W2S_ENA and W2S_Port_Sel bits setting. The forced pins are listed as below when the bit CPWR_Det is low. That means the core power voltage is below 1.7V. And the hardware W2S bus will into protection mode to avoid the E2PROM data corruption.

Table 17-1

CPWR_Det (Read only)	**0**			**1**
W2S_HW_Protection	**0**	**1**		**Don't care**
W2S_ENA	X	**Don't care**		**Don't care**
W2S_Port_Sel	X	**0**	**1**	**Don't care**
P1.2	X	V	X	X
P1.3	X	V	V	X
P1.4	X	X	**V**	X

PS：V means this pin is forced to tri-state output mode.
X means this pin state no any change.

17.2.2 EEPROM_Config

Address	Access Mode	Value At Reset	Nominal Value
0x1741	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	EEPROM_Format		HEADER

This register is used for W2S bus read cycle.
EEPROM_Format is used for different Page Mode:

EEPROM_format	Page Mode
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	RESERVED

HEADER bit is used to support different page size of EEPROM.
"0" is for C16, "1" is for C32/64/128/256

17.2.3 Prescale_Lo

Address	Access Mode	Value At Reset	Nominal Value
0x1742	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Prescale_Lo							

This register is used to control W2S bus speed, companion with Prescale_Hi register.
For 100KHz W2S bus operation, set Prescale_Lo to 22H, and Prescale_Hi to 00H.

17.2.4 Prescale_Hi

Address	Access Mode	Value At Reset	Nominal Value
0x1743	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Prescale_Hi							

This register is used to control W2S bus speed, companion with Prescale_Lo register.
For 100KHz W2S bus operation, set Prescale_Lo to 22H, and Prescale_Hi to 00H.

Prescale Reg. Value	W2S Bus Clock
0x0068	33 KHz
0x0034	66 KHz
0x0022	100 KHz
0x0019	133 KHz
0x0014	166 KHz
0x0006	500 KHz
System Clock: 13.824 MHz	

$$\text{W2S Bus Clock} = \frac{\text{System Clock}}{4 \times (\text{Prescale} + 1)}$$

17.2.5 RdWrFIFO

Address	Access Mode	Value At Reset	Nominal Value
0x1744	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8-bit data from/to FIFO							

This register can be used for W2S both read and write W2S-bus compatible device.
Writing data (including target device ID, high address, low address, and repeat ID, Data) to this register will be automatically stored in W2S controller FIFO. When micro-C receives interrupt from W2S, micro-C need to check W2SStatus (0x1746) register to confirm the transmission is OK. If there is no error during W2S read process, micro-C can start reading FIFO content by reading RdWrFIFO register.
※ Micro-C must set RDActive bit (0x1745[5]) before start reading RdWrFIFO (0x1744) W2S FIFO content.

17.2.6 Force_Activity

Address	Access Mode	Value At Reset	Nominal Value
0x1745	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RDActive	RESERVED	Rst_Rd_Ptr	Rst_Wr_Ptr	RDWRn	RDWR_en

RDActive: Set RDActive bit will enable the read capability of RdWrFIFO (0x1744).
To achieve STOP pattern on W2S bus at power on initial, it can send “acknowledge polling” pattern.
How to send “acknowledge polling” pattern:
After bit W2S_ENA (of register 1470) set 1, writes 0x00H or 0xA0H to FIFO (0x1744H). Finally, sets Force_Activity (0x1745) to 0x01H. After these operations, W2C controller can start reading from or writing to EEPROM. This mechanism used for once when power on is an option to enhance EEPROM stability.

Set Rst_Rd_Ptr bit will rest W2S controller internal FIFO read pointer.
Set Rst_Wr_Ptr bit will rest W2S controller internal FIFO write pointer.
RDWRn: For Read operation, reset RDWRn to 0, for Write operation, set RDWRn to 1.
Set RDWR_en bit will enable read or write operation depend on RDWRn.
※ Micro-C must set W2S_ENA bit before setup Force_Activity.
※ Write 0xFF to 0x1746 to reset all W2S_Status bits and reset W2S-FIFO both read and write pointer (0x1745[3] and 0x1745[2] set to 1) and then clear (0x1745[3] and 0x1745[2] reset to 0) before enable read or write operation.

17.2.7 W2S_Status

Address	Access Mode	Value At Reset	Nominal Value
0x1746	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	FIFO_empty	FIFO_full	ACK_Fail

FIFO_empty bit will generate W2S interrupt during write operation.
FIFO_full bit will generate W2S interrupt during read operation.
ACK_Fail bit indicates that there is no response for target device during ACK period Rread or Write process, this bit will generate W2S interrupt.
※ W2S_Status register content is valid only if W2S_ENA bit has been set.

17.2.8 FIFORdPtr

Address	Access Mode	Value At Reset	Nominal Value
0x1747	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	FIFORdPtr					

This register is used to monitor W2S FIFO read pointer.

17.2.9 FIFOWrPtr

Address	Access Mode	Value At Reset	Nominal Value
0x1748	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	FIFOWrPtr					

This register is used to monitor W2S FIFO write pointer.

17.2.10 ForceAckFail

Address	Access Mode	Value At Reset	Nominal Value
0x1749	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AckFailEna	RESERVED	AckFailPtr					

AckFailEna: Enable Ack Fail Event
AckFailPtr: During write data to EEPROM or Melody devices, the Ack Fail event will occur at the AckFailPtr-th data of W2S FIFO content.

17.2.11 W2S_Misc

Address	Access Mode	Value At Reset	Nominal Value
0x174A	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	SCL_in	C_STATE			W2SIntrpt

This register only monitor several status.
SCL_in: 0: current SCL_in is pull low, 1: current SCL_in pull high.
C_STATE: current finite state machine state.
W2SIntrpt: current interrupt signal indication.

18. USB DEVICE CONTROLLER AND TRANSCEIVER

18.1 Overview

W9681307 is built in a fully functional USB 1.1 controller to be an USB device. It supports most functions of USB 1.1 standard specification and some required functions of USB audio class and HID class profiles for driver free on Microsoft OS in Skype or VOIP wireless applications. In ISP mode application, users also can download program code between PC and external ROM flash memory via USB now. The USB core embeds one 512x8 byte rom to store default descriptors. In the setting, the USB core includes four interfaces and seven endpoints to handle above applications.

18.2 Functionality

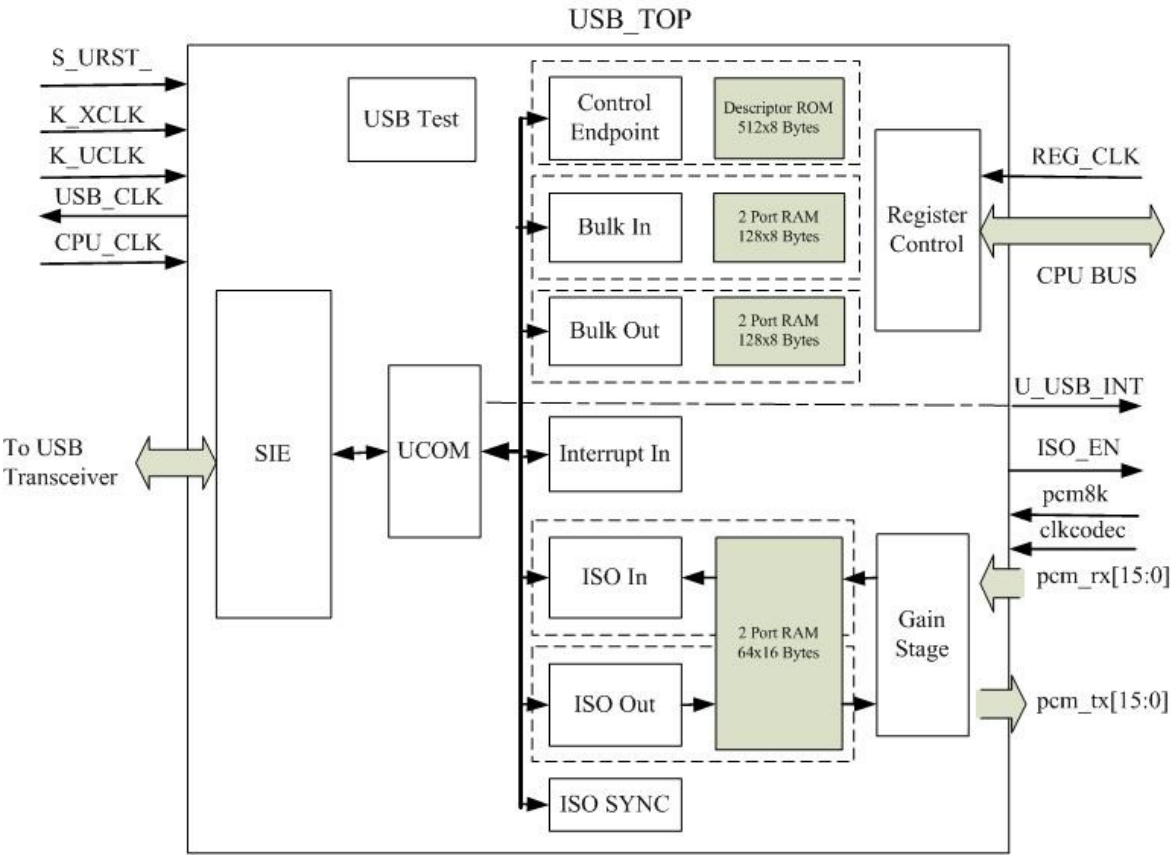


Figure 18-1 The USB block diagram

The USB block diagram is shown in Figure 18-1. The USB module supports all transfer types (Control Endpoint 0, Bulk In, Bulk Out, Interrupt In, Isochronous In, and Isochronous Out) in. USB 1.1 spec and W681307 USB embeds seven Endpoints include Control Endpoint 0. The default descriptors are stored in the 512x8 Bytes ROM. The SIE module is for handle USB series-interface-engine functions. UCOM module is a bridge to communicate SIE and all transfer type modules. Register Control module is for handle CPU read/write and data signals of W681307 USB registers. Gain Stage is required for adjust gain of pcm data in audio volume control application. USB Test module connects many internal signals to test pins for help monitor them from outside.

The feature of the USB module is as follows：

- USB Specification version 1.1 compliant
- Full-Speed (12MHz)
- Audio Class Interface and Command support (Volume Control, Mute Control)
- HID Class Interface and Command support (Set Report)
- USB ISP mode support
- Vendor Command support
- Programmable to connect/disconnect 1.5Kohm pull-up resistance on D+ bus
- Support five interfaces and seven endpoints (Control, Bulk In, Bulk Out, Interrupt In, Isochronous In, and Isochronous Out)
- Ping-Pong FIFO control for Bulk In/Bulk Out transfer to get better performance
- Provide one of three bytes isochronous in endpoint to synchronize isochronous out endpoint for let PC trim the speed of data stream to improve voice quality.

- Mass Storage Class Command support (GER_MAX_LUN)

18.2.1 Endpoints

The definitions of embedded Endpoints are in Table 18-1.

Address	Type	Direction	Maximum Packet Size (Bytes)	Memory Type
0	Control	IN/OUT	8	Registers
1	ISO	IN	16	64x16 (Shared – double buffer)
2	ISO	OUT	18	
3	Bulk	IN	64	128 x 8 (double buffer)
4	Bulk	OUT	64	128 x 8 (double buffer)
5	Interrupt	IN	8	Registers
6	ISO	IN	3	Registers

Table 18-1 W681307 USB Endpoint Definitions

18.2.2 Descriptor Rom

The default descriptors are stored in the 512x8 Bytes ROM. The address mapping and bank definition of this ROM are shown in Figure 18-2. The logical topology from these descriptors is shown in Figure 18-3.

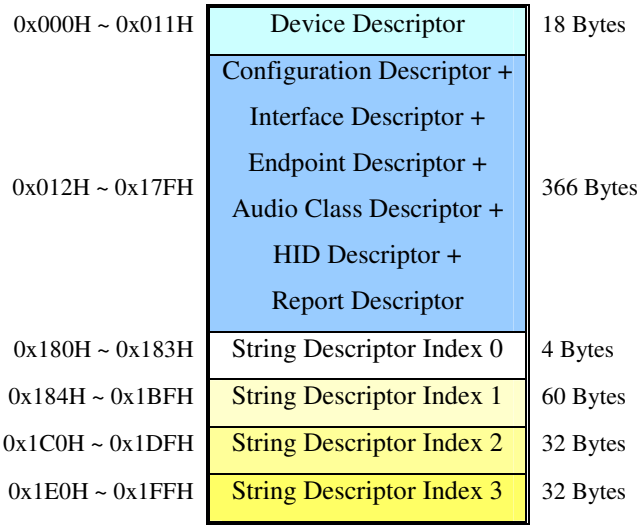


Figure 18-2 Descriptor ROM Definitions

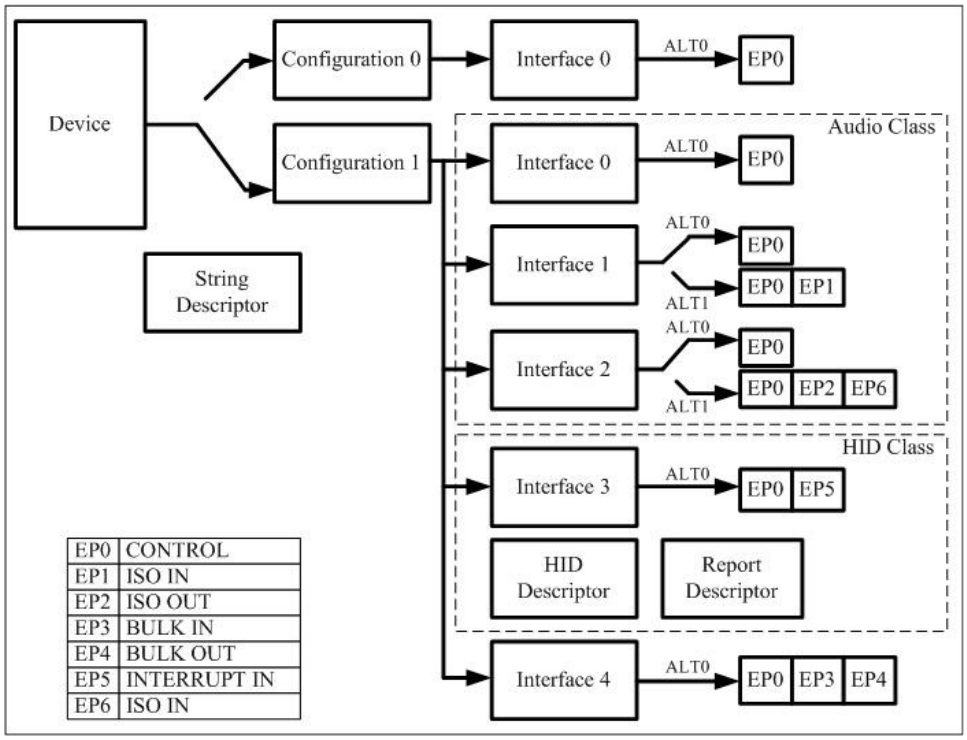


Figure 18-3 The Local Topology of Embedded Descriptors

18.2.3 Configurations and Interfaces

The configuration and interface settings in W681307 USB are shown in Figure 18-3.
The descriptions are as follows：

- ☐ Configuration 0 : The default configuration for all usb devices
  - ■Interface 0 : The default interface for all usb devices
- ☐ Configuration 1
  - ■Interface 0 : Audio Class Interface
  - ■Interface 1 : Audio Class Interface for record mode
    - ➢ Alternate 0 : record off
    - ➢ Alternate 1 : record on
  - ■Interface 2 : Audio Class Interface for play mode
    - ➢ Alternate 0 : play off
    - ➢ Alternate 1 : play on
  - ■Interface 3 : HID Class Interface for commands/status communications
  - ■Interface 4 : Non-Class Interface for USB ISP mode or mass data transfer

18.2.4 Audio Class

W681307 USB provides Audio Class interfaces so it does not need extra driver to be an USB audio device in Microsoft O/S (Windows 2000/XP). Figure 18-4 is shown an USB audio class device topology from embedded descriptors.

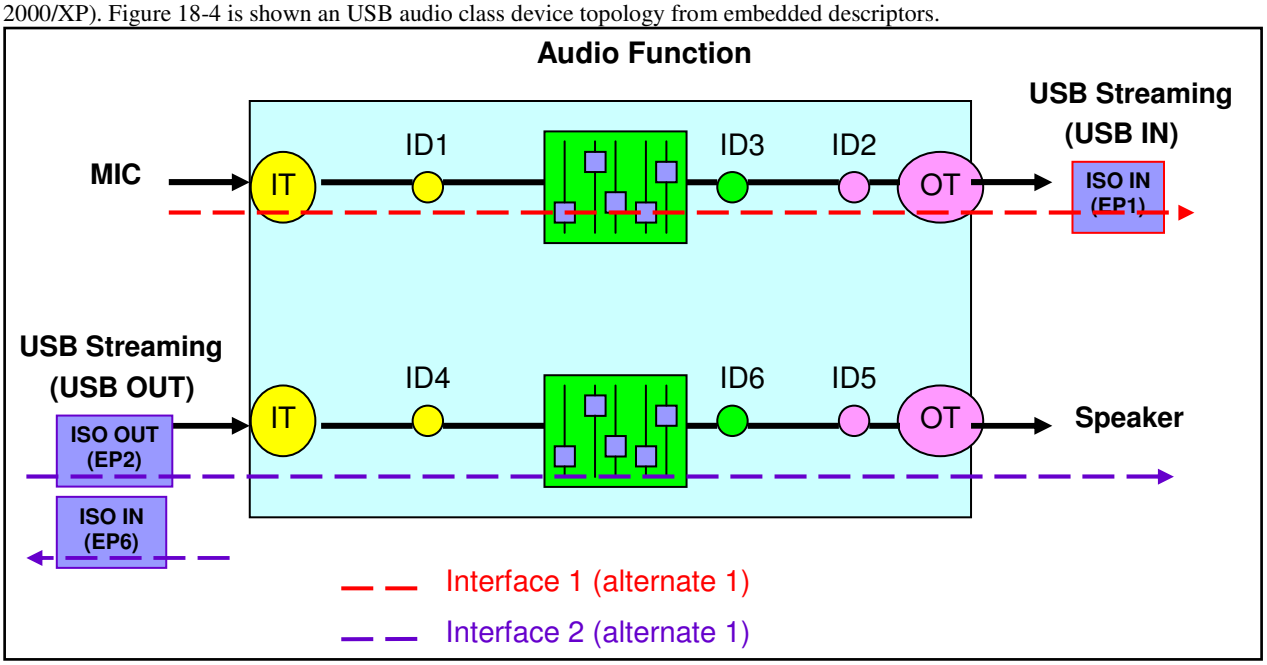


Figure 18-4 USB Audio Class Device Topology

W681307 USB implements Volume Control and Mute Control in Play and Record modes.

18.2.4.1 Play Mode

We define the play mode as the traffic flows from the host to the USB device and to the baseband. The Host can turn on/off the play mode by setting the alternative value from SET INTERFACE 2 command.

18.2.4.2 Record Mode

Define the record mode as the traffic flows from the baseband to the USB host. The Host can turn on/off the record mode by setting the alternative value from SET INTERFACE 1 command.

18.2.4.3 Mute Control

The host can issue SET_CUR command with wValue equals to 0x100 to change the Mute function of the USB device. The host can turn on/off the Mute as requests by the users. If the host selects Feature Unit number 1 (ID is 3), the Mute of audio stream from Mic to USB is changed; if the host selects Feature Unit number 2 (ID is 6), the Mute of audio stream from USB to speaker is updated. The host also can issue GET_CUR command to read back current Mute status.

Play Mode	Record Mode	Play Data to Baseband	Record Data to Host
ON	ON	If Play Mute is On, send 16'h0000; otherwise same as data from host	If Record Mute is On, send 16'h0000; otherwise same as data from Baseband
ON	OFF	If Play Mute is On, send 16'h0000; otherwise same as data from host	No data to host
OFF	ON	16'h0000	If Record Mute is On, send 16'h0000; otherwise same as data from Baseband
OFF	OFF	16'h0000	No data to host

- Play Mute On/Off means SET_CUR for Mute Control and Feature Unit ID 6 then received data = 1/0
- Record Mute On/Off means SET_CUR for Mute Control and Feature Unit ID 3 then received data = 1/0

18.2.4.4 Volume Control

The host can issue SET_CUR commands with wValue equals to 0x0200 to change the Volumes of the USB device. If the host selects Feature Unit number 1 (ID is 3), the Volume of audio stream from Mic to USB (means Record Volume) is changed; if the host selects Feature Unit number 2 (ID is 6), the Volume of audio stream from USB to speaker (means Play Volume) is updated. The host also can issue GET_CUR command to read back current volume gain value.

Data Settings & Gain Mapping		Play Data to BASEBAND	Record Data to Host
0x7FFF	+24 dB	If host sends SET_CUR for volume control in Play path, device will adjust gain of pcm_tx[15:0] via the command then enter BASEBAND after leave ISO out FIFO	If host sends SET_CUR for volume control in Record path, device will adjust gain of pcm_rx[15:0] via the command then enter ISO IN FIFO
…	+24 dB		
0x18xx	+24 dB		
0x17xx	+23 dB		
…	…		
0x01xx	+1 dB		
0x00xx	0 dB		
0xFFxx	-1 dB		
0xFExx	-2 dB		
…	…		
0xE2xx	-29 dB		
0xE1xx	-30 dB		
…	-30 dB		
0x8000	-30 dB		

- The default value of GET_CUR for Volume Control is 0x0000 (0 dB)
- GET_MIN is 0xE100 (-30dB), GET_MAX is 0x1800 (+24 dB) and GET_RES is 0x0100 (+1 dB)

18.2.4.5 Synchronization for Data Transfer

To better synchronization, an endpoint (endpoint 6) is dedicated to provide rate adjustment information to host. The descriptor can set a time interval, so the host will request the rate information (3 bytes) from that endpoint by using that frequency.

18.2.4.6 Audio Data Format

The data format is 16 bits linear PCM in Audio path and the sample frequency is 8 KHz.

18.2.5 HID Class

Interface 3 is a HID Class interface and it has one Interrupt In endpoint. The device can receive commands from host via SET REPORT and report hardware's status to host via Interrupt In transfer in Skype application.

18.2.5.1 Set (Feature) Report

In default descriptors, define 8 bytes feature report descriptors in Report Descriptor. Host can send Set Report command to device then the device can do the action after receive and analyze these 8 bytes data. We use the way to deliver Skype or Winbond commands from host to device.

18.2.5.2 Interrupt In

We use the interrupt in transfer to report the device status to host. The maximum packet size is 8 bytes and the time of polling interval is about 64 ms.

18.2.6 USB ISP mode

Interface 4 does not belong to any class. It has one Bulk In and Bulk Out endpoints. Both maximum packet sizes are 64 bytes. For gain better performance, we implement ping-pong FIFO control in Bulk In/Out transfer.

USB ISP mode uses interface 4. It can download code from PC to external flash by Bulk Out or read the code of external flash on PC by Bulk In via USB bus after install the driver.

18.2.7 Vendor Command

The Vendor command is supported. The bits [6:5] = 2 means Vendor command and bit 7 means data transfer direction in byte 0 of SETUP data in USB 1.1 spec. Based on the rules, users can define individual vendor commands and use them to communicate host and device.

18.3 USB Registers

18.3.1 USB Enable Register

Address	Access Mode	Value At Reset	Nominal Value
0x1800	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	SE0_Dis	R_PullUp	TRX_EN	PLL_EN	Suspend_EN	USB_Reset

USB_Rese Active High. Reset USB digital part. And when S/W receive RESET Interrupt (from host), could use this bit to reset USB.
Suspend_EN Active High. Active High and disable the bias current of Transceiver.
PLL_EN Active High. Enable charge pump and VCO.
TRX_EN Active High. Enable Transceiver.
R_PullUp Active High. Enable a pull-up resister (1.5K ohm) to D+.
SE0_Dis Active High, disable SE0. Default is Low, and set D+ and D- to “0”.

When USB device need to enable a pull-up resister to D+, it also need to disable SE0 state.

18.3.2 USB Interrupt Register A

18.3.2.1 Enable

Address	Access Mode	Value At Reset	Nominal Value
0x1801	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SET_HID _Intrpt	RESERVED	CDI_Intrpt	CDO_Intrpt	IRQI_Intrpt	BKO_Intrpt	BKI_Intrpt	VENDER _Intrpt

18.3.2.2 Status

Address	Access Mode	Value At Reset	Nominal Value
0x1802	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SET_HID _Intrpt	RESERVED	CDI_Intrpt	CDO_Intrpt	IRQI_Intrpt	BKO_Intrpt	BKI_Intrpt	VENDER _Intrpt

18.3.2.3 Clear

Address	Access Mode	Value At Reset	Nominal Value
0x1803	W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SET_HID _Intrpt	RESERVED	CDI_Intrpt	CDO_Intrpt	IRQI_Intrpt	BKO_Intrpt	BKI_Intrpt	VENDER _Intrpt

VENDER_Intrpt Detection of Vender request
BKI_Intrpt Detection of Bulk In(EP3) request
BKO_Intrpt Detection of Bulk Out(EP4) request
IRQI_Intrpt Detection of Interrupt In(EP5) request
CDO_Intrpt Detection of Control Out (EP0) request
CDI_Intrpt Detection of Control In(EP0) request
SET_HID_Intrpt Detection of Set HID report request

18.3.3 USB Interrupt Register B

18.3.3.1 Enable

Address	Access Mode	Value At Reset	Nominal Value
0x1804	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PlayOn _Intrpt	RecordOn _Intrpt	RESERVED	CONNECT _Intrpt	USB_ERROR_I ntrpt	Host_RESUME_I ntrpt	Host_SUSPEND _Intrpt	Host_RESET _Intrpt

18.3.3.2 Status

Address	Access Mode	Value At Reset	Nominal Value
0x1805	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PlayOn _Intrpt	RecordOn _Intrpt	RESERVED	CONNECT _Intrpt	USB_ERROR_I ntrpt	Host_RESUME_I ntrpt	Host_SUSPEND_I ntrpt	Host_RESET _Intrpt

18.3.3.3 Clear

Address	Access Mode	Value At Reset	Nominal Value
0x1806	W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PlayOn _Intrpt	RecordOn _Intrpt	RESERVED	CONNECT _Intrpt	USB_ERROR _Intrpt	Host_RESUME_I ntrpt	Host_SUSPEND _Intrpt	Host_RESET _Intrpt

Host_RESET_Intrpt Detection of Reset request.
Host_SUSPEND_Intrpt Detection of Suspend request
Host_RESUME_Intrpt Detection of Resume request
USB_ERROR_Intrpt Detection of Error request (ex: CRC)
CONNECT_Intrpt Detection of connect
RecordOn_Intrpt Detection of Record On
PlayOn_Intrpt Detection of Play On

18.3.4 EndPoint 0 – Control In/Out Registers

18.3.4.1 Control Register

Address	Access Mode	Value At Reset	Nominal Value
0x1810	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	HID_FIFO _Empty	SDO_RD	CTL_IN_RDY

CTL_IN_RDY Active High. Control In(EP0) Data is ready. S/W needs to set this bit when they finished writing the Control In Data (Max: 8 bytes)
SDO_RD Setup or Data out packet is reading for control transfer.
HID_FIFO_Empty While S/W complete to read the control HID Out Data (0x1820 ~0x1827), set "HID_FIFO_Empty" to High. USB device will send NAK before "HID_FIFO_Empty" setting to High.

18.3.4.2 Control In Data

Address	Access Mode	Value At Reset	Nominal Value
0x1811	W/R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTLI_D [7:0]							

CTLI_D Control in Data. Internal FIFO has 8 bytes.

18.3.4.3 Control HID Out Data

Address	Access Mode	Value At Reset	Nominal Value
0x1820 ~ 0x1827	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTLO_HID0 [7:0] ~ CTLO_HID7 [7:0]							

18.3.4.4 Control Out Data

Address	Access Mode	Value At Reset	Nominal Value
0x1828 ~ 0x182F	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTLO_D0 [7:0] ~ CTLO_D7 [7:0]							

18.3.5 EndPoint 1 and 2 – ISO In/Out Registers

18.3.5.1 Control Register

Address	Access Mode	Value At Reset	Nominal Value
0x1830	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ISO_EN	ISO_RST

ISO_RST Active High reset ISO In/Out function
ISO_EN Active High, enables ISO In/Out function.

18.3.5.2 ISO SYNC Speed Register

Address	Access Mode	Value At Reset	Nominal Value
0x1838~0x1839	R/W	0xFFC0	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_0[15:8]							

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_0[7:0]							

Address	Access Mode	Value At Reset	Nominal Value
0x183A~0x183B	R/W	0xFFE0	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_1[15:8]							

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_1[7:0]							

Address	Access Mode	Value At Reset	Nominal Value
0x183C~0x183D	R/W	0xFFF0	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_2[15:8]							

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_2[7:0]							

Address	Access Mode	Value At Reset	Nominal Value
0x183E~0x183F	R/W	0xFFFE	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_3[15:8]							

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_3[7:0]							

Address	Access Mode	Value At Reset	Nominal Value
0x1840~0x1841	R/W	0x0002	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_4[15:8]							

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_4[7:0]							

Address	Access Mode	Value At Reset	Nominal Value
0x1842~0x1843	R/W	0x0010	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_5[15:8]							

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_5[7:0]							

Address	Access Mode	Value At Reset	Nominal Value
0x1844~0x1845	R/W	0x0020	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_6[15:8]							

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_6[7:0]							

Address	Access Mode	Value At Reset	Nominal Value
0x1846~0x1847	R/W	0x0040	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_7[15:8]							

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISO_SYNC_SPEED_7[7:0]							

18.3.6 EndPoint 3 – Bulk In Registers

18.3.6.1 Control Register

Address	Access Mode	Value At Reset	Nominal Value
0x1848	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BKI_EN	BKI_RST

BKI_RST Active High, reset Bulk In function
BKI_EN: Active High, enable Bulk In function.

18.3.6.2 Bulk In Data

Address	Access Mode	Value At Reset	Nominal Value
0x1849	W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BKI_DATA[7:0]							

BKI_DATA Bulk_In Data except final data.

18.3.6.3 Bulk In Final Data

Address	Access Mode	Value At Reset	Nominal Value
0x184A	W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BKI_EOP_DATA[7:0]							

BKI_EOP_DATA Bulk_In end of packet data.

18.3.6.4 Bulk In FIFO Empty Flag

Address	Access Mode	Value At Reset	Nominal Value
0x184B	R		

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BKI_FIFO _Empty

BKI_FIFO_Empty FIFO 0 or FIFO 1 empty flag. S/W needs to check this bit to decide if there still had empty FIFO to write.

18.3.7 EndPoint 4 – Bulk Out Registers

18.3.7.1 Control Register

Address	Access Mode	Value At Reset	Nominal Value
0x1850	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BKO_EN	BKO_RST

BKO_RST Active High, reset Bulk Out function
BKO_EN Active High, enable Bulk Out function

18.3.7.2 Bulk Out FIFO Length

Address	Access Mode	Value At Reset	Nominal Value
0x1851	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	BKO_FIFO_LEN[6:0]						

BKO_FIFO_LEN [6:0] It will show the present FIFO length.

18.3.7.3 Bulk Out Data

Address	Access Mode	Value At Reset	Nominal Value
0x1852	R	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BKO_D [7:0]							

BKO_D Bulk Out Data.

18.3.8 EndPoint 5 – Interrupt In Registers

18.3.8.1 Control Register

Address	Access Mode	Value At Reset	Nominal Value
0x1858	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	IRQI_EN	IRQI_RST

IRQI_RST Active High, reset IRQI (EP5) function
IRQI_EN Active High, enable IRQI (EP5) function

18.3.8.2 USB Interrupt Data Length

Address	Access Mode	Value At Reset	Nominal Value
0x1859	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	IRQI_Start	IRQI_LEN [3:0]			

IRQI_LEN [3:0] Interrupt In (EP5) data length.
IRQI_Start Active High, Interrupt In (EP5) active.

18.3.8.3 Interrupt In Data

Address	Access Mode	Value At Reset	Nominal Value
0x1860 ~0x186F	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQI_D0 [7:0] ~ IRQI_D15 [7:0]							

Total 16 bytes Interrupt In Data.

18.3.9 Specific Register

Address	Access Mode	Value At Reset	Nominal Value
0x1870 -1873	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Blocked (for test modes)							

18.3.10 Specific Register

Address	Access Mode	Value At Reset	Nominal Value
0x1874	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	Blocked (for test modes)	Blocked (for test modes)	Blocked (for test modes)

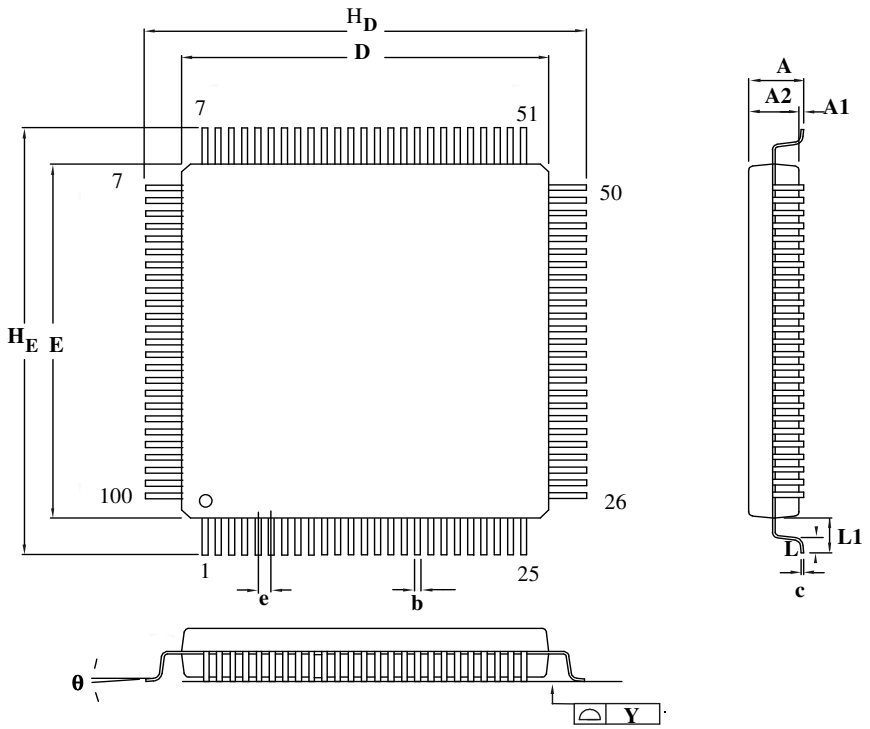
18.3.11 Specific Register

Address	Access Mode	Value At Reset	Nominal Value
0x1875	R/W	0x00	

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	Blocked (for test modes)

19. PACKAGE DIMENSIONS

100pin LQFP (14x14x1.4 mm footprint 2.0mm)



Controlling Dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.
Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Please note that all data and specifications are subject to change without notice.
All the trademarks of products and companies mentioned in this datasheet belong to their respective owners.