



LMx93, LM2903 Dual Differential Comparators

1 Features

- Single-Supply or Dual Supplies
- Wide Range of Supply Voltage
 - Maximum Rating: 2 V to 36 V
 - Tested to 30 V: Non-V Devices
 - Tested to 32 V: V-Suffix Devices
- Low Supply-Current Drain Independent of Supply Voltage: 0.4 mA (Typical) Per Comparator
- Low Input Bias Current: 25 nA (Typical)
- Low Input Offset Current: 3 nA (Typical) (LM139)
- Low Input Offset Voltage: 2 mV (Typical)
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage: ± 36 V
- Low Output Saturation Voltage
- Output Compatible With TTL, MOS, and CMOS
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Chemical or Gas Sensor
- Desktop PC
- Motor Control: AC Induction
- Weigh Scale

3 Description

These devices consist of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible as long as the difference between the two supplies is 2 V to 36 V, and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

The LM193 device is characterized for operation from -55°C to 125°C . The LM293 and LM293A devices are characterized for operation from -25°C to 85°C . The LM393 and LM393A devices are characterized for operation from 0°C to 70°C . The LM2903 device is characterized for operation from -40°C to 125°C .

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM193D, LM293D, LM293AD, LM393D, LM393AD, LM2903D	SOIC (8)	4.90 mm x 6.00 mm
LM293DGK, LM293ADGK, LM393DGK, LM393ADGK, LM2903DGK	VSSOP (8)	3.00 mm x 5.00 mm
LM293P, LM393P, LM393AP, LM2903P	PDIP (8)	9.50 mm x 6.30 mm
LM393PS, LM393APS, LM2903PS	SO (8)	6.20 mm x 7.90 mm
LM393PW, LM393APW, LM2903PW	TSSOP (8)	6.40 mm x 3.00 mm
LM193JG	GDIP (8)	10.00 mm x 7.00 mm
LM193FK	CQCC (8)	9.00 mm x 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

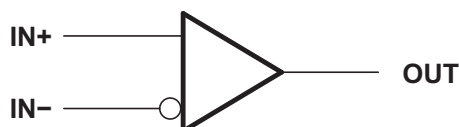


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision X (January 2014) to Revision Y	Page
Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.	1

Changes from Revision W (July 2010) to Revision X	Page
- Updated document to new TI data sheet format - no specification changes. - Updated <i>Features</i> - Removed <i>Ordering Information</i> table - Added ESD warning.	1 1 3 13

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾		36	V
V _{ID}	Differential input voltage ⁽³⁾		±36	V
V _I	Input voltage (either input)	–0.3	36	V
V _O	Output voltage		36	V
I _O	Output current		20	mA
	Duration of output short circuit to ground ⁽⁴⁾		Unlimited	
T _J	Operating virtual-junction temperature		150	°C
	Case temperature for 60 s	FK package	260	°C
	Lead temperature 1,6 mm (1/16 in) from case for 60 s	J package	300	°C
T _{stg}	Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground.
- (3) Differential voltages are at IN+ with respect to IN–.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	1000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	750

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V _{CC} (non-V devices)	2	30	V
V _{CC} (V devices)	2	32	V
T _J	–40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LMx93, LM2903							UNIT
	D (SOIC)	DGK (VSSOP)	P (PDIP)	PS (SO)	PW (TSSOP)	JG (GDIP)	FK (LCCC)	
	8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	97	172	85	95	149	—	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	—	—	—	—	—	14.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics for LMx93

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A ⁽¹⁾	LM193			LM293 LM393			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{CC} = 5 V to 30 V, V _{IC} = V _{ICR} min, V _O = 1.4 V		25°C	2	5		2	5	mV	
				Full range			9		9		
I _{IO}	Input offset current	V _O = 1.4 V		25°C	3	25		5	50	nA	
				Full range			100		250		
I _{IB}	Input bias current	V _O = 1.4 V		25°C	–25	–100		–25	–250	nA	
				Full range			–300		–400		
V _{ICR}	Common-mode input-voltage range ⁽²⁾			25°C	0 to V _{CC} – 1.5		0 to V _{CC} – 1.5		V		
				Full range	0 to V _{CC} – 2		0 to V _{CC} – 2				
A _{VD}	Large-signal differential-voltage amplification	V _{CC} = 15 V, V _O = 1.4 V to 11.4 V, R _L ≥ 15 kΩ to V _{CC}		25°C	50	200		50	200	V/mV	
I _{OH}	High-level output current	V _{OH} = 5 V	V _{ID} = 1 V	25°C	0.1			0.1	50	nA	
		V _{OH} = 30 V	V _{ID} = 1 V	Full range	1				1	μA	
V _{OL}	Low-level output voltage	I _{OL} = 4 mA, V _{ID} = –1 V		25°C	150	400		150	400	mV	
				Full range	700				700		
I _{OL}	Low-level output current	V _{OL} = 1.5 V,	V _{ID} = –1 V	25°C	6			6		mA	
I _{CC}	Supply current	R _L = ∞	V _{CC} = 5 V	25°C	0.8	1		0.8	1	mA	
			V _{CC} = 30 V	Full range	2.5				2.5		

- (1) Full range (minimum or maximum) for LM193 is –55°C to 125°C, for LM293 is 25°C to 85°C, and for LM393 is 0°C to 70°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$ for the inverting input (–), and the non-inverting input (+) can exceed the V_{CC} level; the comparator provides a proper output state. Either or both inputs can go to 30 V without damage.

6.6 Electrical Characteristics for LMx93A

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A ⁽¹⁾	LM293A LM393A			UNIT
					MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{CC} = 5 V to 30 V, V _O = 1.4 V V _{IC} = V _{ICR(min)}		25°C	1		2	mV
				Full range	4			
I _{IO}	Input offset current	V _O = 1.4 V		25°C	5		50	nA
				Full range	150			
I _{IB}	Input bias current	V _O = 1.4 V		25°C	−25		−250	nA
				Full range	−400			
V _{ICR}	Common-mode input-voltage range ⁽²⁾			25°C	0 to V _{CC} − 1.5		V	
				Full range	0 to V _{CC} − 2			
A _{VD}	Large-signal differential-voltage amplification	V _{CC} = 15 V, V _O = 1.4 V to 11.4 V, R _L ≥ 15 kΩ to V _{CC}		25°C	50	200	V/mV	
I _{OH}	High-level output current	V _{OH} = 5 V, V _{ID} = 1 V		25°C	0.1		50	nA
		V _{OH} = 30 V, V _{ID} = 1 V		Full range	1		μA	
V _{OL}	Low-level output voltage	I _{OL} = 4 mA, V _{ID} = −1 V		25°C	150		400	mV
				Full range	700			
I _{OL}	Low-level output current	V _{OL} = 1.5 V, V _{ID} = −1 V,		25°C	6		mA	
I _{CC}	Supply current (four comparators)	R _L = ∞	V _{CC} = 5 V	25°C	0.8		1	mA
			V _{CC} = 30 V	Full range	2.5			

- (1) Full range (minimum or maximum) for LM293A is 25°C to 85°C, and for LM393A is 0°C to 70°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$, but either or both inputs can go to 30 V without damage.

6.7 Electrical Characteristics for LM2903 and LM2903A

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A ⁽¹⁾	LM2903			LM2903A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{CC} = 5 V to MAX ⁽²⁾ , V _O = 1.4 V, V _{IC} = V _{ICR(min)} ,		25°C	2	7		1	2	mV	
				Full range			15				4
I _{IO}	Input offset current	V _O = 1.4 V		25°C	5	50		5	50	nA	
				Full range			200				200
I _{IB}	Input bias current	V _O = 1.4 V		25°C	–25	–250		–25	–250	nA	
				Full range			–500				–500
V _{ICR}	Common-mode input-voltage range ⁽³⁾			25°C	0 to V _{CC} – 1.5			0 to V _{CC} – 1.5		V	
				Full range	0 to V _{CC} – 2			0 to V _{CC} – 2			
A _{VD}	Large-signal differential-voltage amplification	V _{CC} = 15 V, V _O = 1.4 V to 11.4 V, R _L ≥ 15 kΩ to V _{CC}		25°C	25	100		25	100	V/mV	
I _{OH}	High-level output current	V _{OH} = 5 V,	V _{ID} = 1 V	25°C		0.1	50		0.1	50	nA
		V _{OH} = V _{CC} MAX ⁽²⁾ ,	V _{ID} = 1 V	Full range			1			1	μA
V _{OL}	Low-level output voltage	I _{OL} = 4 mA, V _{ID} = –1 V,		25°C	150	400		150	400	mV	
				Full range			700				700
I _{OL}	Low-level output current	V _{OL} = 1.5 V,	V _{ID} = –1 V	25°C	6			6		mA	
I _{CC}	Supply current	R _L = ∞	V _{CC} = 5 V	25°C	0.8	1		0.8	1	mA	
			V _{CC} = MAX	Full range			2.5				2.5

- (1) Full range (minimum or maximum) for LM2903 is –40°C to 125°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) $V_{CC} \text{ MAX} = 30\text{ V}$ for non-V devices and 32 V for V-suffix devices.
- (3) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$, but either or both inputs can go to 30 V (32 V for V-suffix devices) without damage.

6.8 Switching Characteristics

 $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		LM2901, LM293, LM293A LM393, LM393A LM2903	UNIT
			TYP	
Response time	R_L connected to 5 V through 5.1 k Ω , $C_L = 15\text{ pF}^{(1)(2)}$	100-mV input step with 5-mV overdrive	1.3	μs
		TTL-level input step	0.3	

- (1) C_L includes probe and jig capacitance.
- (2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

6.9 Typical Characteristics

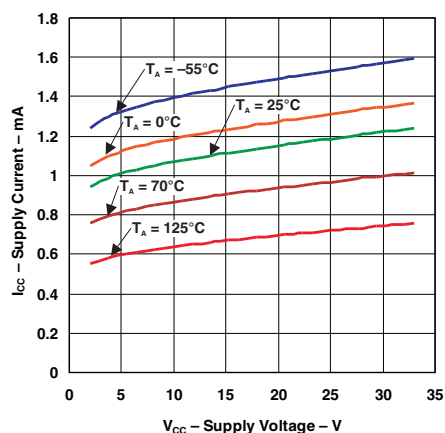


Figure 1. Supply Current vs Supply Voltage

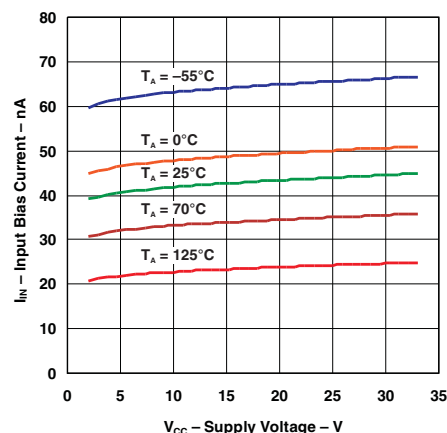


Figure 2. Input Bias Current vs Supply Voltage

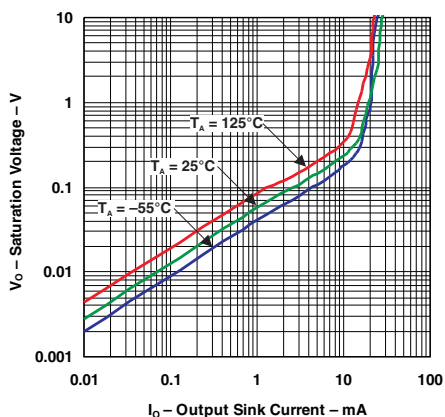
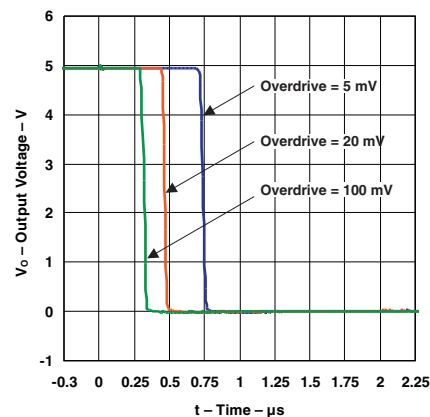
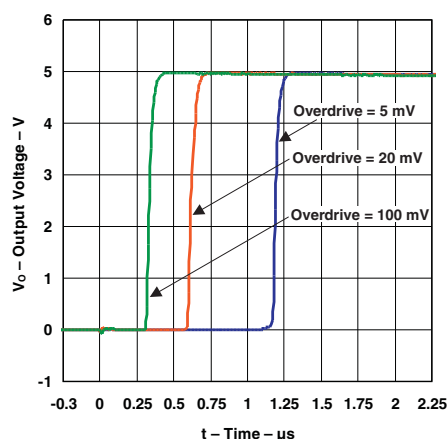


Figure 3. Output Saturation Voltage



**Figure 4. Response Time for Various Overdrives
Negative Transition**



**Figure 5. Response Time for Various Overdrives
Positive Transition**

7 Detailed Description

7.1 Overview

The LM2903 is a dual comparator with the ability to operate up to 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range (2 V to 36 V), low I_q and fast response of the devices.

The open-drain output allows the user to configure the output's logic low voltage (V_{OL}) and can be used to enable the comparator to be used in AND functionality.

7.2 Functional Block Diagram

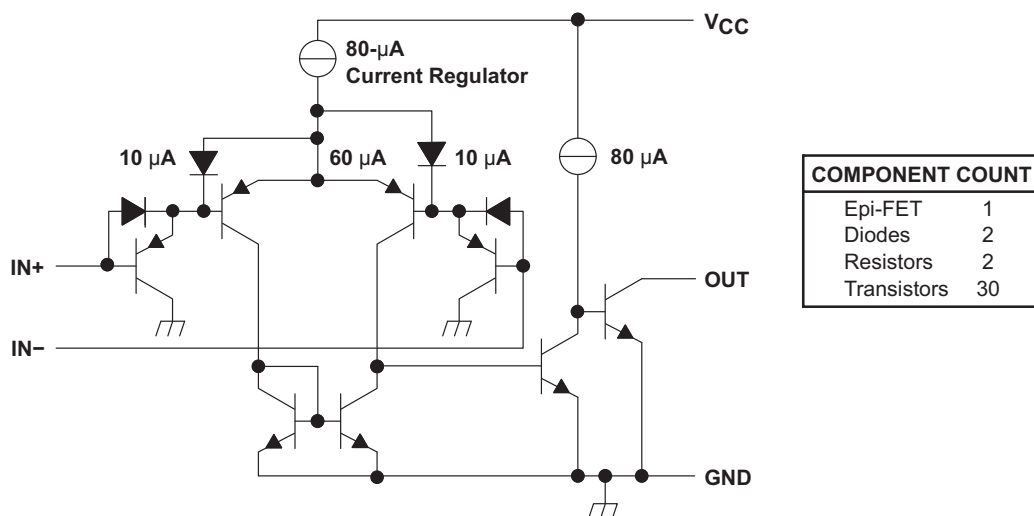


Figure 6. Schematic (Each Comparator)

7.3 Feature Description

LM2903 consists of a PNP darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing LM2903 to accurately function from ground to $V_{CC}-1.5V$ differential input. This enables much head room for modern day supplies of 3.3 V and 5 V.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN will sink current when the positive input voltage is higher than the negative input voltage and the offset voltage. The V_{OL} is resistive and will scale with the output current. See Figure 3 for V_{OL} values with respect to the output current.

7.4 Device Functional Modes

7.4.1 Voltage Comparison

The LM2903 operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

LM2903 will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LM2903 optimal for level shifting to a higher or lower voltage.

8.2 Typical Application

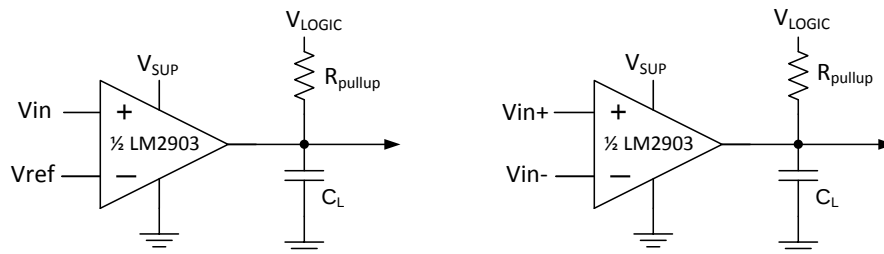


Figure 7. Single-Ended and Differential Comparator Configurations

8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to Vsup-1.5 V
Supply Voltage	2 V to 36 V
Logic Supply Voltage	2 V to 36 V
Output Current (R _{PULLUP})	1 μ A to 20 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C _L)	15 pF

8.2.2 Detailed Design Procedure

When using LM2903 in a general comparator application, determine the following:

- Input Voltage Range
- Minimum Overdrive Voltage
- Output and Drive Current
- Response Time

8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is above or below 25°C the V_{ICR} can range from 0 V to $V_{CC} - 2.0$ V. This limits the input voltage range to as high as $V_{CC} - 2.0$ V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

Below is a list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common-mode range:
 - (a) If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
 - (b) If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common-mode and IN+ is within common-mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common-mode and IN- is within common-mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common-mode, the output is low and the output transistor is sinking current

8.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). In order to make an accurate comparison the Overdrive Voltage (V_{OD}) should be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. [Figure 8](#) and [Figure 9](#) show positive and negative response times with respect to overdrive voltage.

8.2.2.3 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pullup voltage. The output current will produce a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use [Typical Characteristics](#) to determine V_{OL} based on the output current.

The output current can also effect the transient response. See [Response Time](#) for more information.

8.2.2.4 Response Time

The transient response can be determined by the load capacitance (C_L), load/pullup resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The positive response time (τ_P) is approximately $\tau_P \sim R_{PULLUP} \times C_L$
- The negative response time (τ_N) is approximately $\tau_N \sim R_{CE} \times C_L$
 - R_{CE} can be determine by taking the slope of [Typical Characteristics](#) in it's linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

8.2.3 Application Curves

The following curves were generated with 5 V on V_{CC} and V_{Logic} , $R_{PULLUP} = 5.1 \text{ k}\Omega$, and 50 pF scope probe.

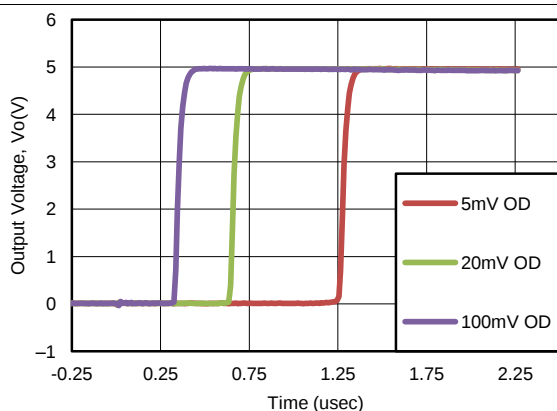


Figure 8. Response Time for Various Overdrives (Positive Transition)

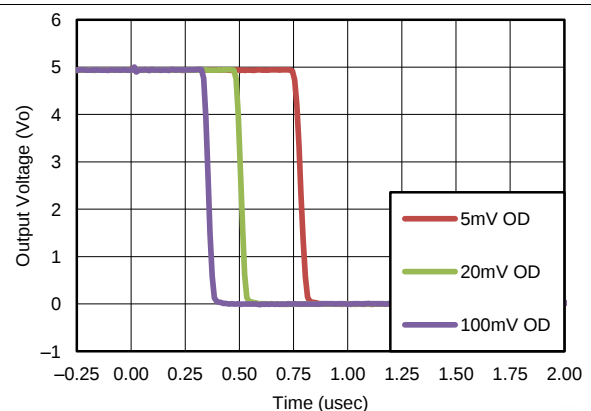


Figure 9. Response Time for Various Overdrives (Negative Transition)

9 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, TI recommends to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can eat into the input common-mode range of the comparator and create an inaccurate comparison.

10 Layout

10.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches, which can affect the high level input common-mode voltage range. In order to achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

10.2 Layout Example

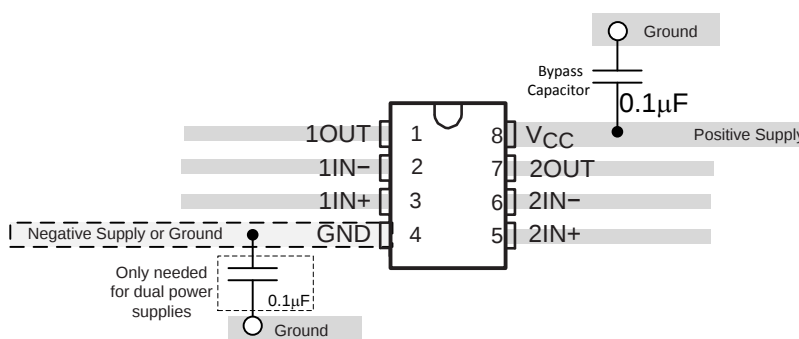


Figure 10. LM2903 Layout Example

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM193	Click here	Click here	Click here	Click here	Click here
LM293	Click here	Click here	Click here	Click here	Click here
LM293A	Click here	Click here	Click here	Click here	Click here
LM393	Click here	Click here	Click here	Click here	Click here
LM393A	Click here	Click here	Click here	Click here	Click here
LM2903	Click here	Click here	Click here	Click here	Click here
LM2903V	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM193DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM193	Samples
LM193DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM193	Samples
LM2903AVQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903AVQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903AVQPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903AVQPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(MAP ~ MAS ~ MAU)	Samples
LM2903DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(MAP ~ MAS ~ MAU)	Samples
LM2903DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DRG3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	LM2903P	Samples
LM2903PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	LM2903P	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2903PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PWRG3	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q	Samples
LM2903QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q	Samples
LM2903QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q	Samples
LM2903VQDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903V	Samples
LM2903VQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903V	Samples
LM2903VQPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903V	Samples
LM2903VQPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903V	Samples
LM293AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293A	Samples
LM293ADE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293A	Samples
LM293ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293A	Samples
LM293ADGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(MDP ~ MDS ~ MDU)	Samples
LM293ADGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	(MDP ~ MDS ~ MDU)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM293ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-25 to 85	LM293A	Samples
LM293ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293A	Samples
LM293D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	-25 to 85	(MCP ~ MCS ~ MCU)	Samples
LM293DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	(MCP ~ MCS ~ MCU)	Samples
LM293DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DRG3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU CU SN	N / A for Pkg Type	-25 to 85	LM293P	Samples
LM293PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-25 to 85	LM293P	Samples
LM393AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M8P ~ M8S ~ M8U)	Samples
LM393ADGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(M8P ~ M8S ~ M8U)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM393ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU CU SN	N / A for Pkg Type	0 to 70	LM393AP	Samples
LM393APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LM393AP	Samples
LM393APSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393APSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393APSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393APWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393APWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393APWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M9P ~ M9S ~ M9U)	Samples
LM393DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	(M9P ~ M9S ~ M9U)	Samples
LM393DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM393DRG3	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU CU SN	N / A for Pkg Type	0 to 70	LM393P	Samples
LM393PE3	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	LM393P	Samples
LM393PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	LM393P	Samples
LM393PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PWRG3	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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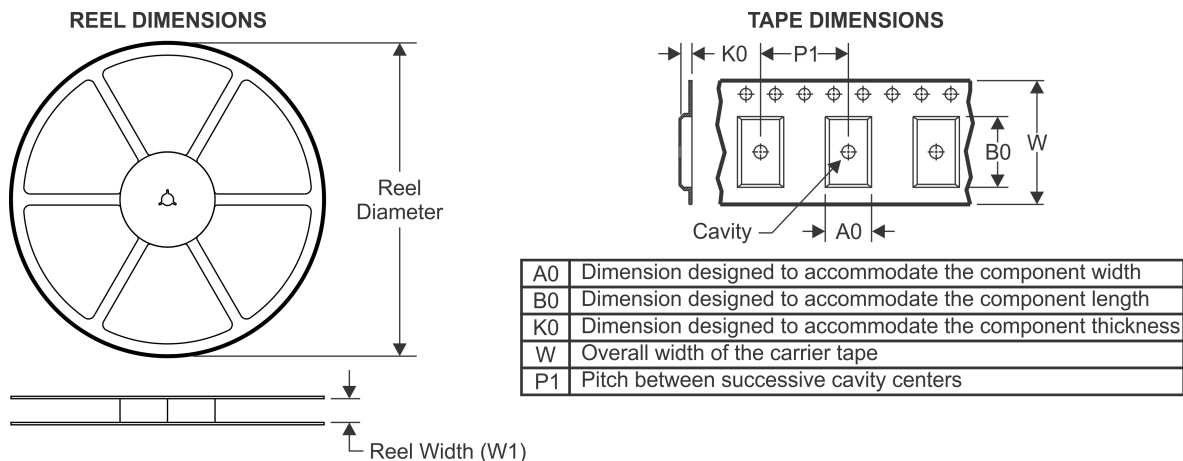
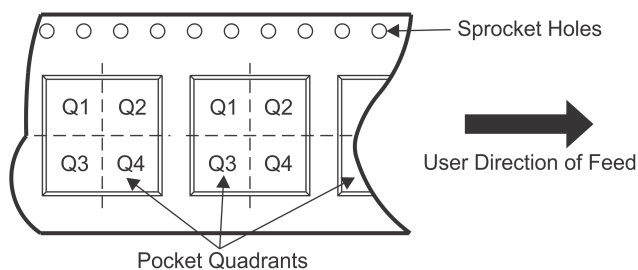
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OTHER QUALIFIED VERSIONS OF LM2903, LM293 :

- Automotive: [LM2903-Q1](#)
- Enhanced Product: [LM293-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM193DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903AVQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DR	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903PSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
LM2903PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2903VQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2903VQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM293ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM293ADR	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM293DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM293DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM293DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393APSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
LM393APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393APWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG3	SOIC	D	8	2500	330.0	15.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393PSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
LM393PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM193DR	SOIC	D	8	2500	367.0	367.0	38.0
LM2903AVQDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903AVQPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903AVQPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM2903DR	SOIC	D	8	2500	364.0	364.0	27.0
LM2903DR	SOIC	D	8	2500	333.2	345.9	28.6
LM2903DR	SOIC	D	8	2500	367.0	367.0	35.0
LM2903DR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM2903DRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM2903DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM2903PSR	SO	PS	8	2000	367.0	367.0	38.0
LM2903PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2903PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2903PWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903QDRG4	SOIC	D	8	2500	367.0	367.0	38.0
LM2903VQDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903VQPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2903VQPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LM293ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM293ADR	SOIC	D	8	2500	333.2	345.9	28.6
LM293ADR	SOIC	D	8	2500	367.0	367.0	35.0
LM293ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM293ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM293ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM293ADRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM293DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM293DR	SOIC	D	8	2500	364.0	364.0	27.0
LM293DR	SOIC	D	8	2500	367.0	367.0	35.0
LM293DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM293DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM293DRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM393ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM393ADR	SOIC	D	8	2500	333.2	345.9	28.6
LM393ADR	SOIC	D	8	2500	367.0	367.0	35.0
LM393ADR	SOIC	D	8	2500	364.0	364.0	27.0
LM393ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM393ADRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM393ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM393APSR	SO	PS	8	2000	367.0	367.0	38.0
LM393APWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM393APWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LM393APWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LM393DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM393DR	SOIC	D	8	2500	367.0	367.0	35.0
LM393DR	SOIC	D	8	2500	340.5	338.1	20.6
LM393DRG3	SOIC	D	8	2500	333.2	345.9	28.6
LM393DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM393DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM393DRG4	SOIC	D	8	2500	367.0	367.0	35.0
LM393PSR	SO	PS	8	2000	367.0	367.0	38.0
LM393PWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LM393PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM393PWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

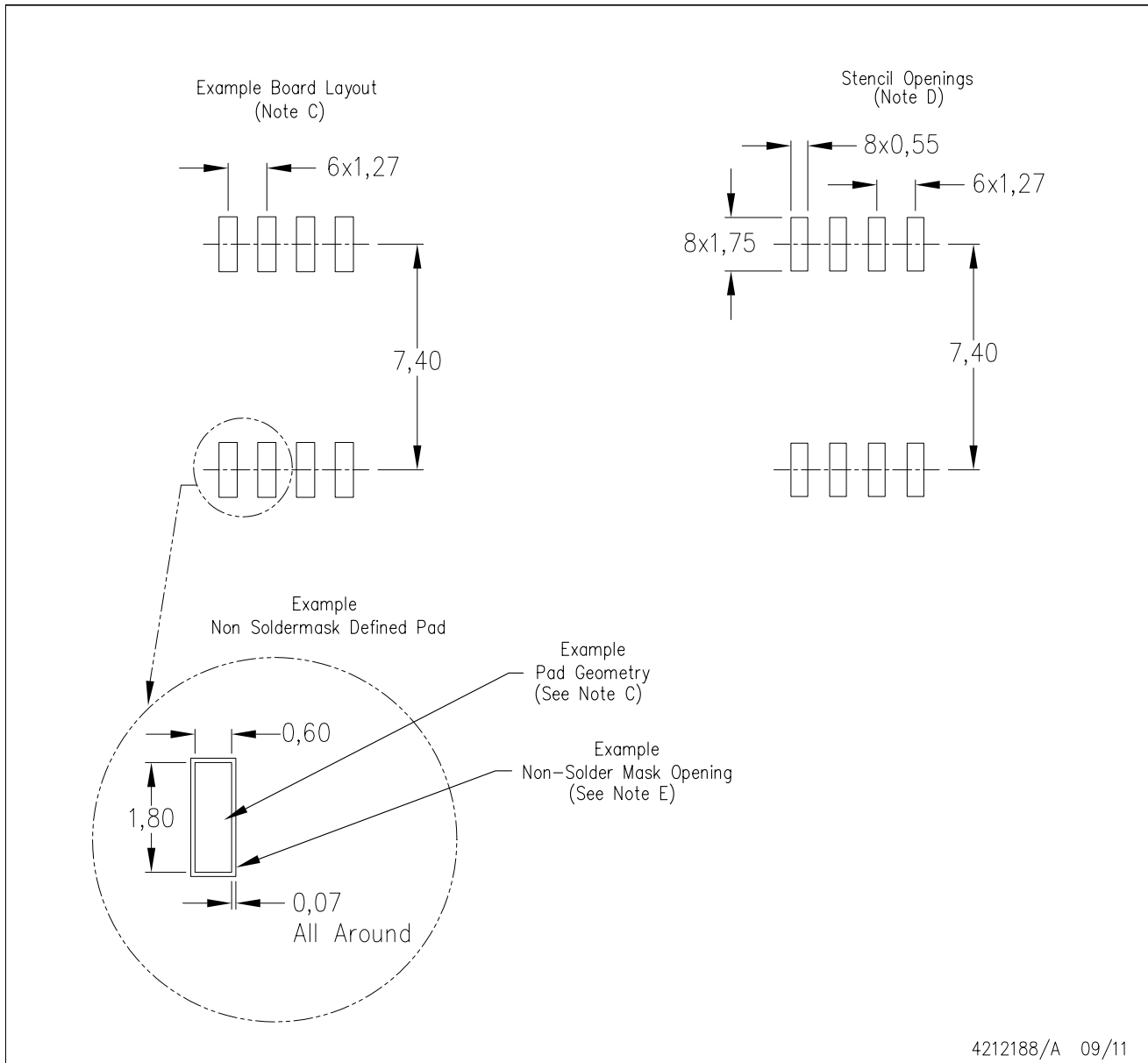


4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

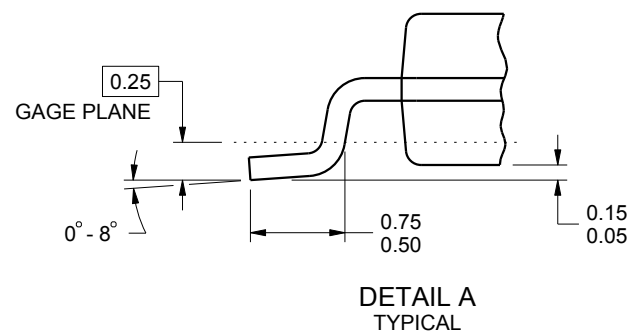
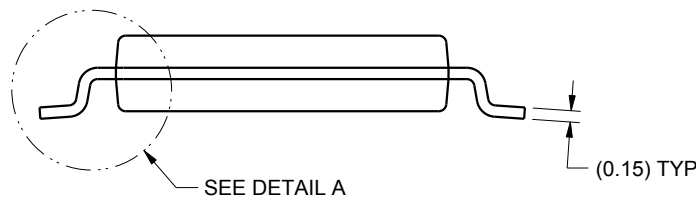
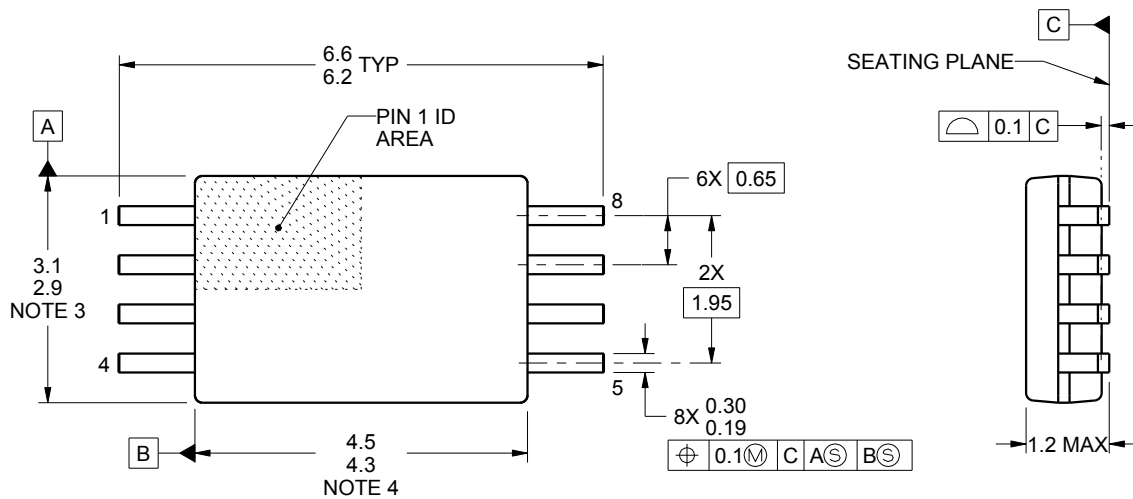
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

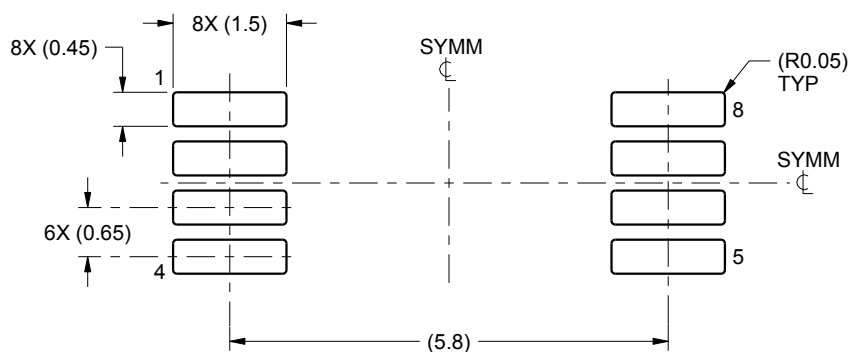
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

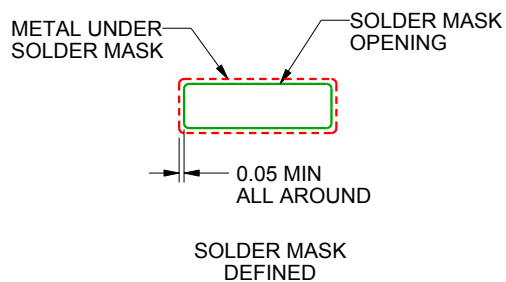
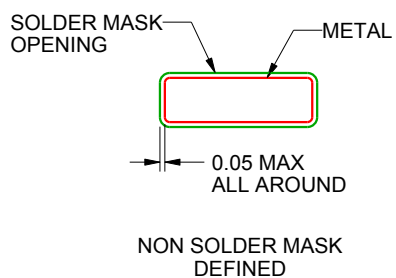
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

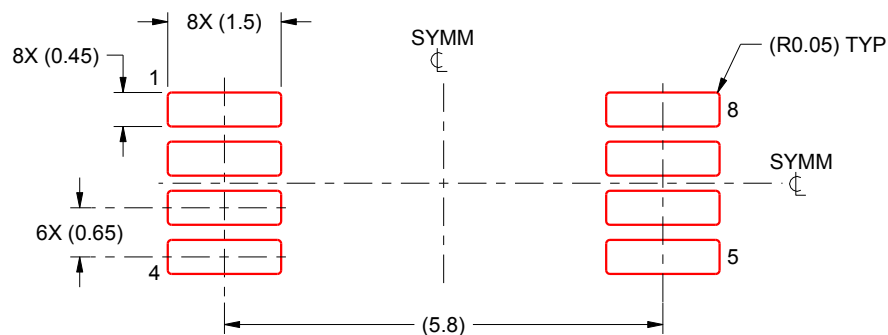
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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