High Common-Mode Voltage Difference Amplifier

AD629

FEATURES
Improved Replacement for:
INA117P and INA117KU
±270 V Common-Mode Voltage Range
Input Protection to:
±500 V Common Mode
±500 V Differential
Wide Power Supply Range (±2.5 V to ±18 V)
±10 V Output Swing on ±12 V Supply
1 mA Max Power Supply Current

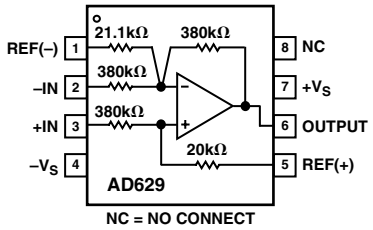
HIGH ACCURACY DC PERFORMANCE
3 ppm Max Gain Nonlinearity
20 μV/°C Max Offset Drift (AD629A)
10 μV/°C Max Offset Drift (AD629B)
10 ppm/°C Max Gain Drift

EXCELLENT AC SPECIFICATIONS
77 dB Min CMRR @ 500 Hz (AD629A)
86 dB Min CMRR @ 500 Hz (AD629B)
500 kHz Bandwidth

APPLICATIONS
High Voltage Current Sensing
Battery Cell Voltage Monitor
Power Supply Current Monitor
Motor Control
Isolation

FUNCTIONAL BLOCK DIAGRAM

8-Lead Plastic Mini-DIP (N) and SOIC (R) Packages



GENERAL DESCRIPTION

The AD629 is a difference amplifier with a very high input common-mode voltage range. It is a precision device that allows the user to accurately measure differential signals in the presence of high common-mode voltages up to ±270 V.

The AD629 can replace costly isolation amplifiers in applications that do not require galvanic isolation. The device will operate over a ±270 V common-mode voltage range and has inputs that are protected from common-mode or differential mode transients up to ±500 V.

The AD629 has low offset, low offset drift, low gain error drift, as well as low common-mode rejection drift, and excellent CMRR over a wide frequency range.

The AD629 is available in low-cost, plastic 8-lead DIP and SOIC packages. For all packages and grades, performance is guaranteed over the entire industrial temperature range from –40°C to +85°C.

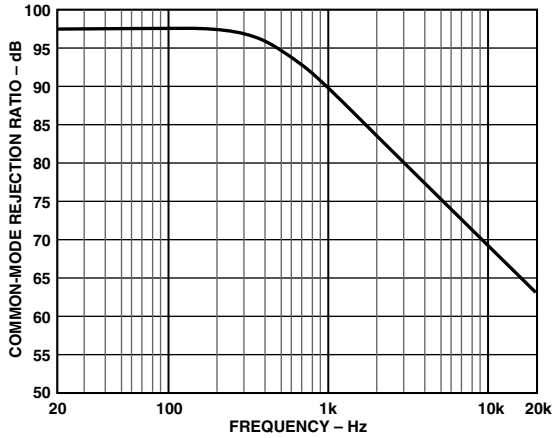


Figure 1. Common-Mode Rejection Ratio vs. Frequency

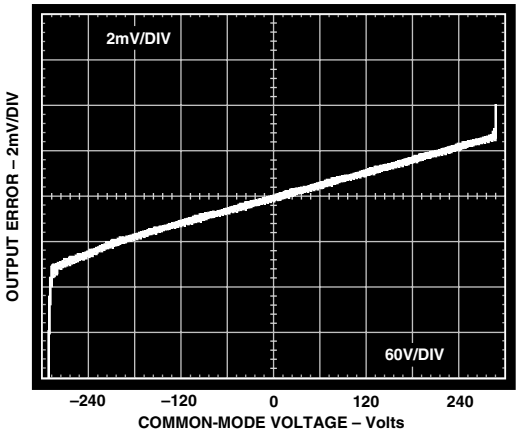


Figure 2. Common-Mode Operating Range. Error Voltage vs. Input Common-Mode Voltage

REV. A

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AD629—SPECIFICATIONS (T_A = 25°C, V_S = ±15 V unless otherwise noted)

Parameter	Condition	AD629A Min	AD629A Typ	AD629A Max	AD629B Min	AD629B Typ	AD629B Max	Unit
GAIN	V_{OUT} = ±10 V, R_L = 2 kΩ							
Nominal Gain			1			1		V/V
Gain Error			0.01	0.05		0.01	0.03	%
Gain Nonlinearity			4	10		4	10	ppm
	R_L = 10 kΩ		1			1	3	ppm
Gain vs. Temperature	$T_A = T_{MIN}$ to T_{MAX}		3	10		3	10	ppm/°C
OFFSET VOLTAGE								
Offset Voltage			0.2	1		0.1	0.5	mV
	V_S = ±5 V						1	mV
vs. Temperature	$T_A = T_{MIN}$ to T_{MAX}		6	20		3	10	µV/°C
vs. Supply (PSRR)	V_S = ±5 V to ±15 V	84	100		90	110		dB
INPUT								
Common-Mode Rejection Ratio	V_{CM} = ±250 V dc	77	88		86	96		dB
	$T_A = T_{MIN}$ to T_{MAX}	73			82			dB
	V_{CM} = 500 V p-p DC to 500 Hz	77			86			dB
	V_{CM} = 500 V p-p DC to 1 kHz		88			90		dB
Operating Voltage Range	Common-Mode			±270			±270	V
	Differential			±13			±13	V
Input Operating Impedance	Common-Mode		200			200		kΩ
	Differential		800			800		kΩ
OUTPUT								
Operating Voltage Range	R_L = 10 kΩ	±13			±13			V
	R_L = 2 kΩ	±12.5			±12.5			V
	V_S = ±12 V, R_L = 2 kΩ	±10			±10			V
Output Short Circuit Current			±25			±25		mA
Capacitive Load	Stable Operation	1000			1000			pF
DYNAMIC RESPONSE								
Small Signal –3 dB Bandwidth			500			500		kHz
Slew Rate		1.7	2.1		1.7	2.1		V/µs
Full Power Bandwidth	V_{OUT} = 20 V p-p		28			28		kHz
Settling Time	0.01%, V_{OUT} = 10 V Step		15			15		µs
	0.1%, V_{OUT} = 10 V Step		12			12		µs
	0.01%, V_{CM} = 10 V Step, V_{DIFF} = 0 V		5			5		µs
OUTPUT NOISE VOLTAGE								
0.01 Hz to 10 Hz			15			15		µV p-p
Spectral Density, ≥100 Hz[1]			550			550		nV/√Hz
POWER SUPPLY								
Operating Voltage Range		±2.5		±18	±2.5		±18	V
Quiescent Current	V_{OUT} = 0 V		0.9	1		0.9	1	mA
	T_{MIN} to T_{MAX}		1.2			1.2		mA
TEMPERATURE RANGE								
For Specified Performance	$T_A = T_{MIN}$ to T_{MAX}	–40		+85	–40		+85	°C

NOTES
[1]See Figure 19.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage V_S . . . . . ±18 V
Internal Power Dissipation[2]
DIP (N) . . . . . See Derating Curves
SOIC (R) . . . . . See Derating Curves
Input Voltage Range, Continuous . . . . . ±300 V
Common-Mode and Differential, 10 sec . . . . . ±500 V
Output Short Circuit Duration . . . . . Indefinite
Pin 1, Pin 5 . . . . . $-V_S$ – 0.3 V to $+V_S$ + 0.3 V
Maximum Junction Temperature . . . . . 150°C
Operating Temperature Range . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.
[2]Specification is for device in free air: 8-Lead Plastic DIP, θ_{JA} = 100°C/W; 8-Lead SOIC Package, θ_{JA} = 155°C/W.

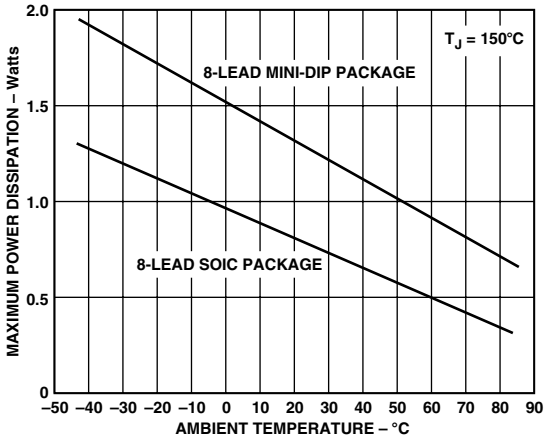


Figure 3. Derating Curve of Maximum Power Dissipation vs. Temperature for SOIC and PDIP Packages

THEORY OF OPERATION

The AD629 is a unity gain differential-to-single-ended amplifier (Diff Amp) that can reject extremely high common-mode signals (in excess of 270 V with 15 V supplies). It consists of an operational amplifier (Op Amp) and a resistor network.

In order to achieve high common-mode voltage range, an internal resistor divider (Pin 3, Pin 5) attenuates the noninverting signal by a factor of 20. Other internal resistors (Pin 1, Pin 2, and the feedback resistor) restores the gain to provide a differential gain of unity. The complete transfer function equals:

$$V_{OUT} = V(+IN) - V(-IN)$$

Laser wafer trimming provides resistor matching so that common-mode signals are rejected while differential input signals are amplified.

The op amp itself, in order to reduce output drift, uses super beta transistors in its input stage The input offset current and its associated temperature coefficient contribute no appreciable output voltage offset or drift. This has the added benefit of reducing voltage noise because the corner where 1/f noise becomes dominant is below 5 Hz. In order to reduce the dependence of gain accuracy on the op amp, the open-loop voltage gain of the op amp exceeds 20 million, and the PSRR exceeds 140 dB.

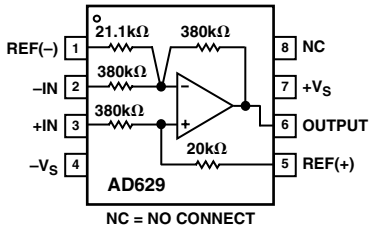


Figure 4. Functional Block Diagram

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD629AR	–40°C to +85°C	8-Lead Plastic SOIC	SO-8
AD629AR-REEL[1]	–40°C to +85°C	8-Lead Plastic SOIC	SO-8
AD629AR-REEL7[2]	–40°C to +85°C	8-Lead Plastic SOIC	SO-8
AD629BR	–40°C to +85°C	8-Lead Plastic SOIC	SO-8
AD629BR-REEL[1]	–40°C to +85°C	8-Lead Plastic SOIC	SO-8
AD629BR-REEL7[2]	–40°C to +85°C	8-Lead Plastic SOIC	SO-8
AD629AN	–40°C to +85°C	8-Lead Plastic DIP	N-8
AD629BN	–40°C to +85°C	8-Lead Plastic DIP	N-8

NOTES
[1]13" Tape and Reel of 2500 each
[2]7" Tape and Reel of 1000 each

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD629 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD629–Typical Performance Characteristics (@25°C, V_S = ±15 V unless otherwise noted)

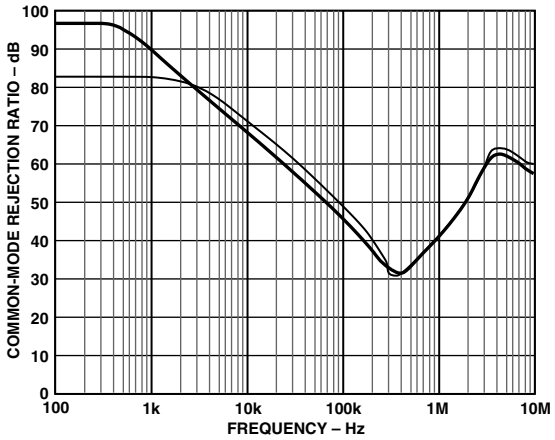


Figure 5. Common-Mode Rejection Ratio vs. Frequency

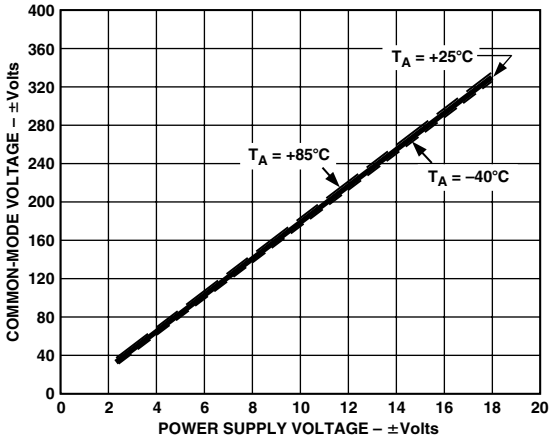


Figure 8. Common-Mode Operating Range vs. Power Supply Voltage

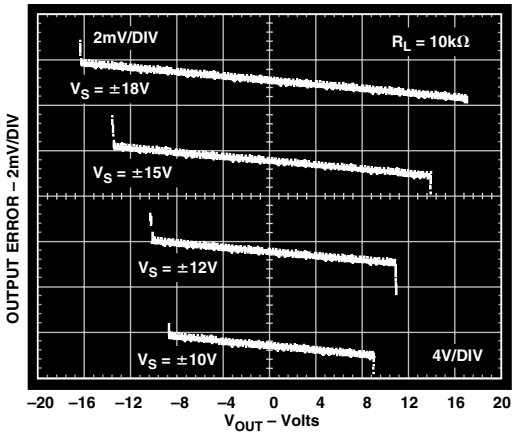


Figure 6. Typical Gain Error Normalized @ V_{OUT} = 0 V and Output Voltage Operating Range vs. Supply Voltage, R_L = 10 kΩ (Curves Offset for Clarity)

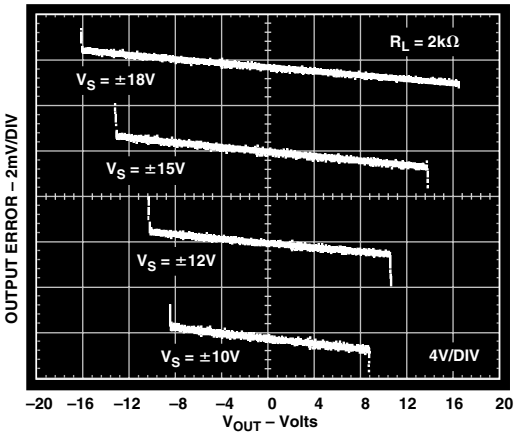


Figure 9. Typical Gain Error Normalized @ V_{OUT} = 0 V and Output Voltage Operating Range vs. Supply Voltage, R_L = 2 kΩ (Curves Offset for Clarity)

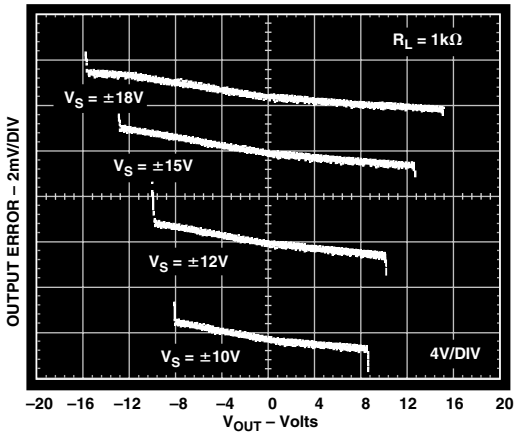


Figure 7. Typical Gain Error Normalized @ V_{OUT} = 0 V and Output Voltage Operating Range vs. Supply Voltage, R_L = 1 kΩ (Curves Offset for Clarity)

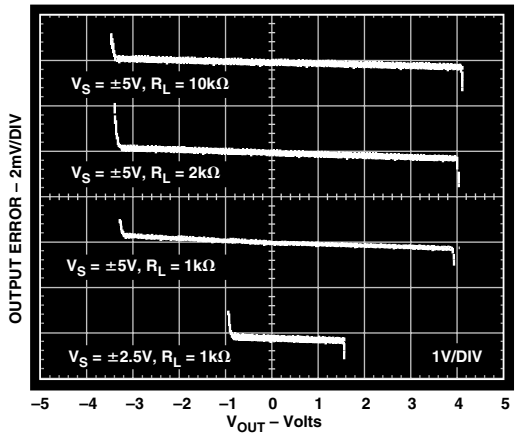


Figure 10. Typical Gain Error Normalized @ V_{OUT} = 0 V and Output Voltage Operating Range vs. Supply Voltage (Curves Offset for Clarity)

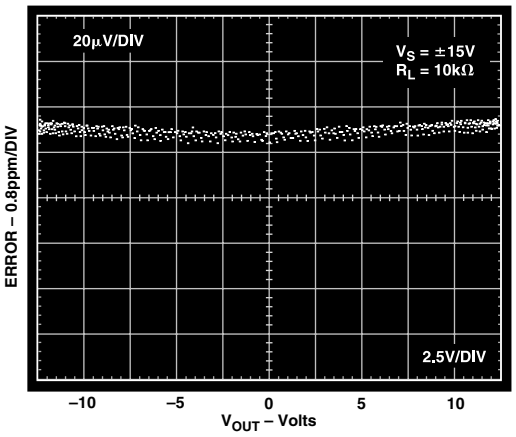


Figure 11. Gain Nonlinearity; V_S = ±15 V, R_L =10 kΩ

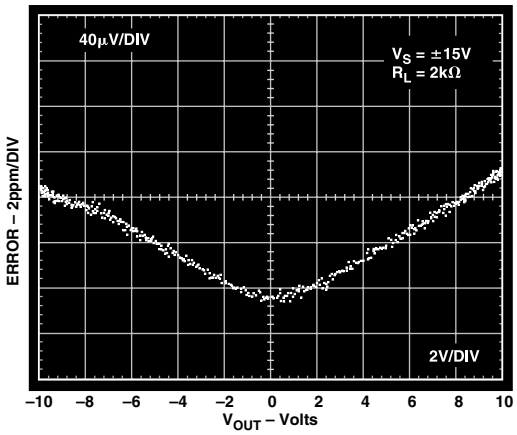


Figure 14. Gain Nonlinearity; V_S = ±15 V, R_L = 2 kΩ

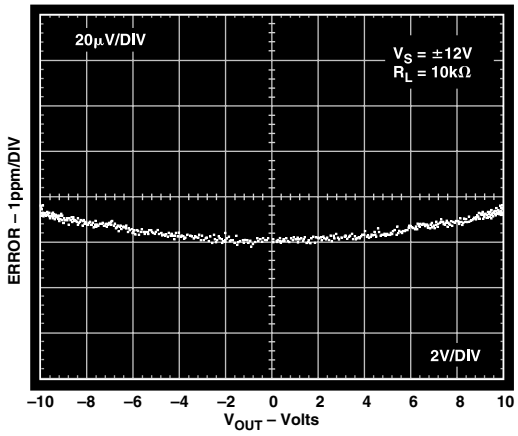


Figure 12. Gain Nonlinearity; V_S = ±12 V, R_L =10 kΩ

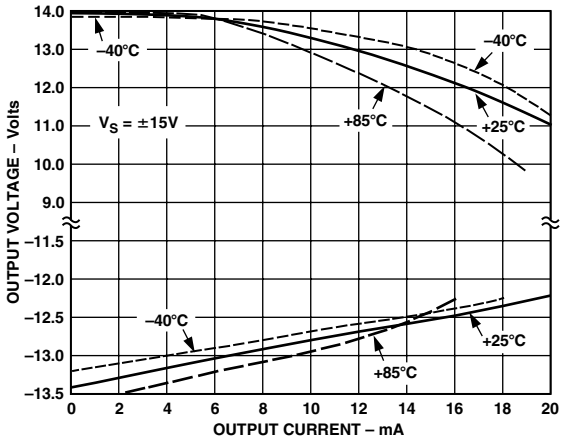


Figure 15. Output Voltage Operating Range vs. Output Current; V_S = ±15 V

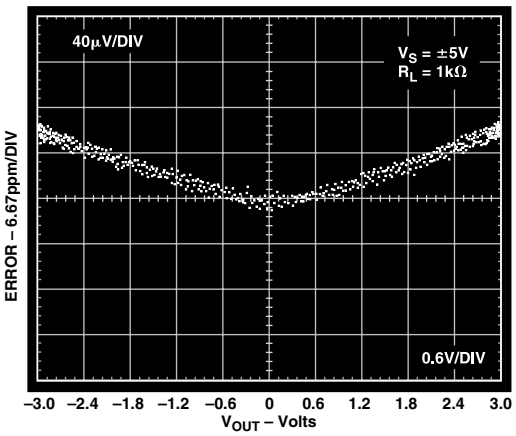


Figure 13. Gain Nonlinearity; V_S = ±5 V, R_L =1 kΩ

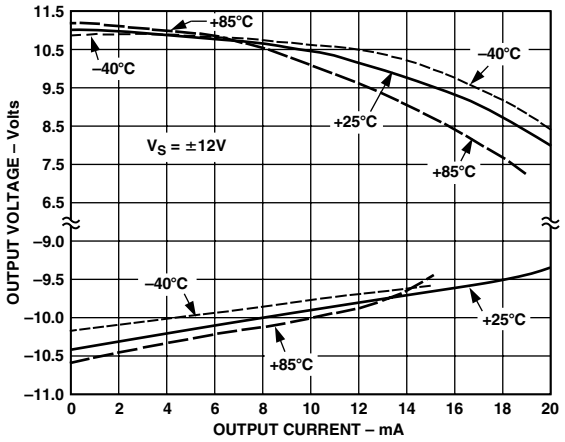


Figure 16. Output Voltage Operating Range vs. Output Current; V_S = ±12 V

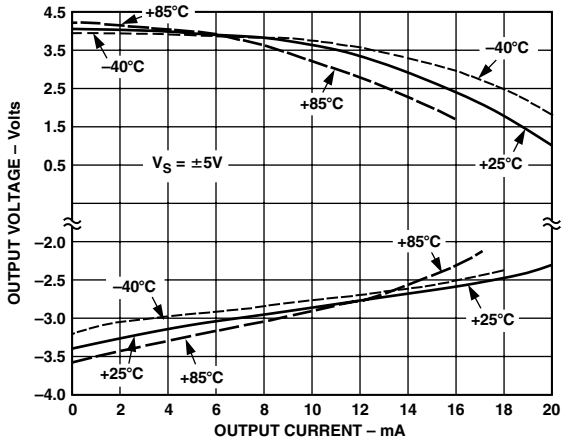


Figure 17. Output Voltage Operating Range vs. Output Current; $V_S = \pm 5$ V

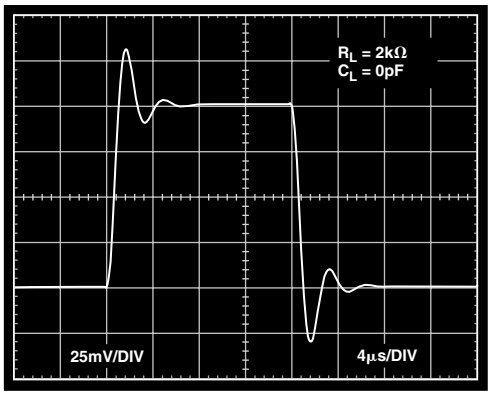


Figure 20. Small Signal Pulse Response; G = 1, R_L = 2 kΩ

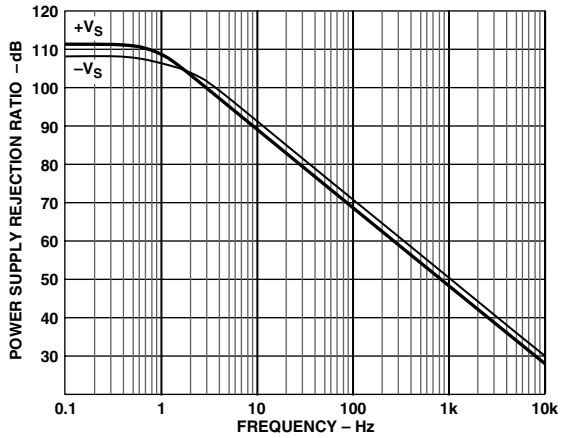


Figure 18. Power Supply Rejection Ratio vs. Frequency

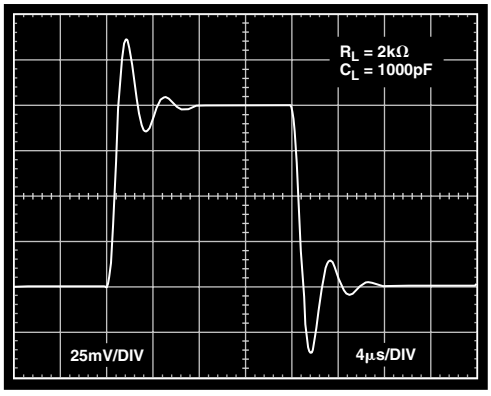


Figure 21. Small Signal Pulse Response; G = 1, R_L = 2 kΩ, C_L = 1000 pF

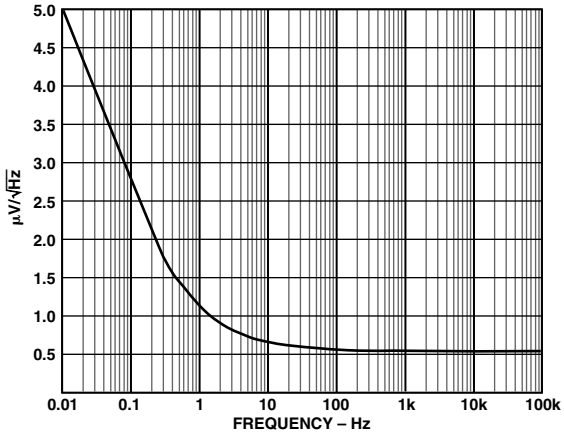


Figure 19. Voltage Noise Spectral Density vs. Frequency

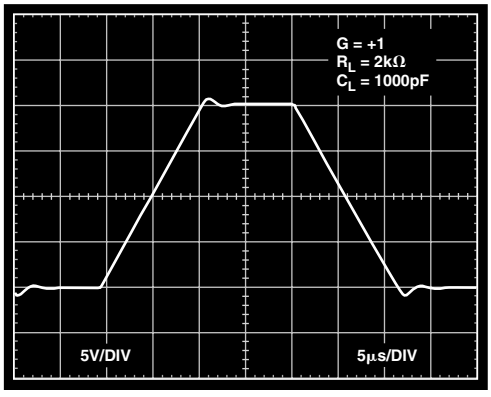


Figure 22. Large Signal Pulse Response; G = 1, R_L = 2 kΩ, C_L = 1000 pF

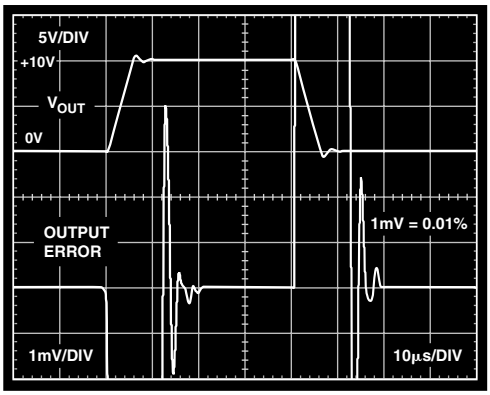


Figure 23. Settling Time to 0.01%, For 0 V to 10 V Output Step; G = –1, R_L = 2 kΩ

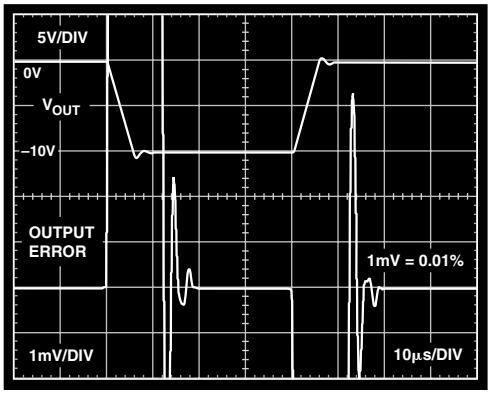


Figure 26. Settling Time to 0.01% for 0 V to –10 V Output Step; G = –1, R_L = 2 kΩ

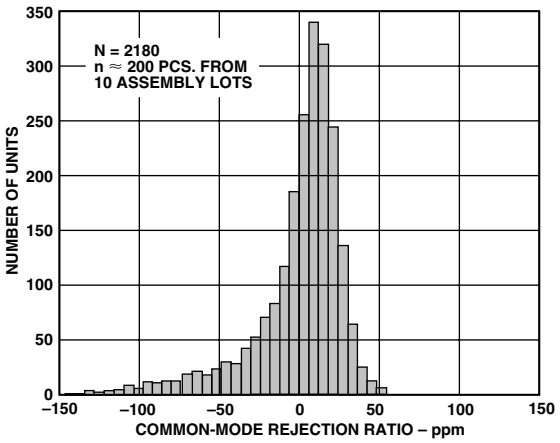


Figure 24. Typical Distribution of Common-Mode Rejection; Package Option N-8

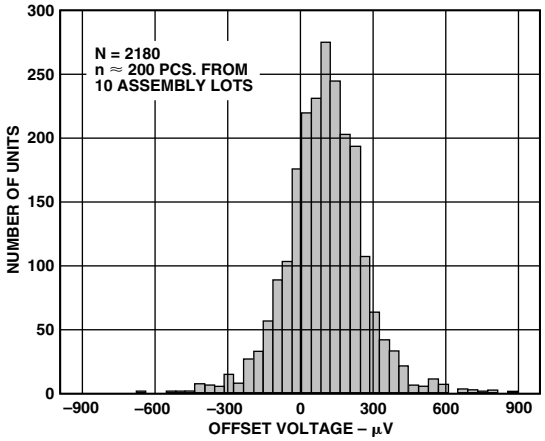


Figure 27. Typical Distribution of Offset Voltage; Package Option N-8

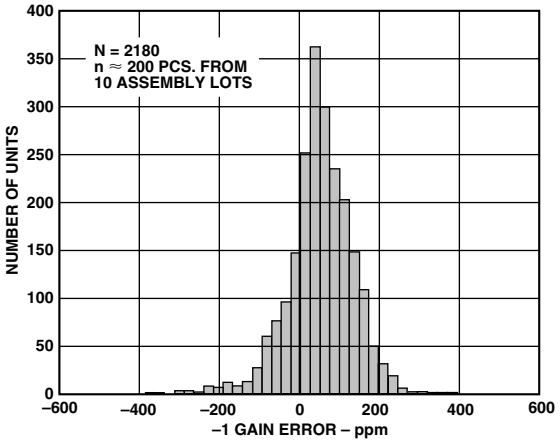


Figure 25. Typical Distribution of –1 Gain Error; Package Option N-8

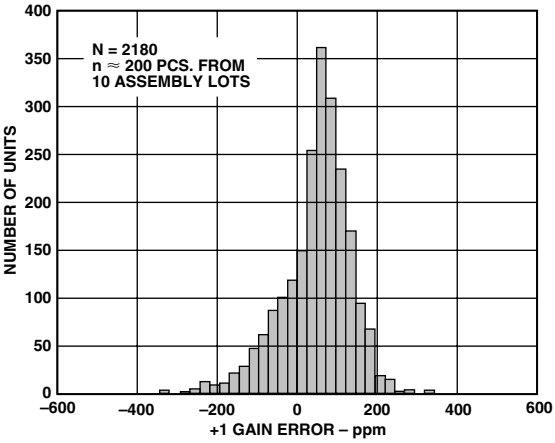


Figure 28. Typical Distribution of +1 Gain Error; Package Option N-8

APPLICATIONS

Basic Connections

Figure 29 shows the basic connections for operating the AD629 with a dual supply. A supply voltage of between ±3 V and ±18 V is applied between Pins 7 and 4. Both supplies should be decoupled close to the pins using 0.1 µF capacitors. 10 µF electrolytic capacitors, also located close to the supply pins, may also be required if low frequency noise is present on the power supply. While multiple amplifiers can be decoupled by a single set of 10 µF capacitors, each in amp should have its own set of 0.1 µF capacitors so that the decoupling point can be located physically close to the power pins.

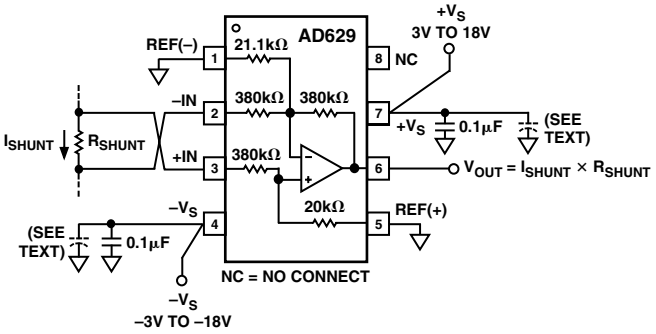


Figure 29. Basic Connections

The differential input signal, which will typically result from a load current flowing through a small shunt resistor, is applied to Pins 2 and 3 with the polarity shown in order to obtain a positive gain. The common-mode range on the differential input signal can range from –270 V to +270 V and the maximum differential range is ±13 V. When configured as shown, the device operates as a simple gain-of-one differential-to-single-ended amplifier, the output voltage being the shunt resistance times the shunt current. The output is measured with respect to Pins 1 and 5.

Pins 1 and 5 (REF(–) and REF(+)) should be grounded for a gain of unity and should be connected to the same low impedance ground plane. Failure to do this will result in degraded common-mode rejection. Pin 8 is a no connect pin and should be left open.

Single Supply Operation

Figure 30 shows the connections for operating the AD629 with a single supply. Because the output can swing to within only about 2 V of either rail, it is necessary to apply an offset to the output. This can be conveniently done by connecting REF(+) and REF(–) to a low impedance reference voltage (some analog-to-digital converters provide this voltage as an output), which is capable of sinking current. Thus, for a single supply of 10 V, V_{REF} might be set to 5 V for a bipolar input signal. This would allow the output to swing ±3 V around the central 5 V reference voltage. Alternatively, for unipolar input signals, V_{REF} could be set to about 2 V, allowing the output to swing from +2 V (for a 0 V input) to within 2 V of the positive rail.

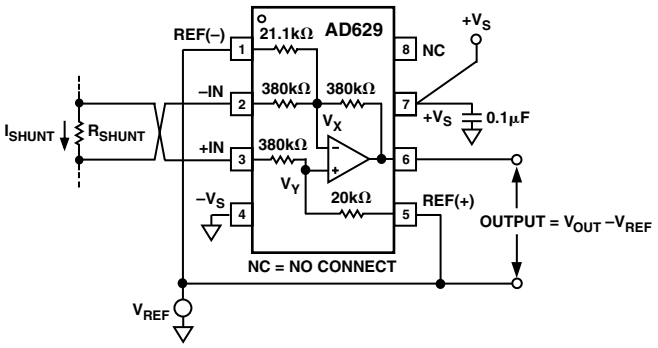


Figure 30. Operation with a Single Supply

Applying a reference voltage to REF(+) and REF(–) and operating on a single supply will reduce the input common-mode range of the AD629. The new input common-mode range depends upon the voltage at the inverting and noninverting inputs of the internal operational amplifier, labeled V_X and V_Y in Figure 30. These nodes can swing to within 1 V of either rail. So for a (single) supply voltage of 10 V, V_X and V_Y can range between 1 V and 9 V. If V_{REF} is set to 5 V, the permissible common-mode range is +85 V to –75 V. The common-mode voltage ranges can be calculated using the following equation.

$$V_{CM}(\pm) = 20\,V_{X/Y}(\pm) - 19\,V_{REF}$$

System-Level Decoupling and Grounding

The use of ground planes is recommended to minimize the impedance of ground returns (and hence the size of dc errors). Figure 31 shows how to work with grounding in a mixed-signal environment, that is, with digital and analog signals present. In order to isolate low-level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground returns. All ground pins from mixed-signal components such as analog-to-digital converters should be returned through the "high quality" analog ground plane. This includes the digital ground lines of mixed-signal converters that should also be connected to the analog ground plane. This may seem to break the rule of keeping analog and digital grounds separate, but in general, there is also a requirement to keep the voltage difference between digital and analog grounds on a converter as small as possible (typically <0.3 V). The increased noise, caused by the converter's digital return currents flowing through the analog ground plane, will typically be negligible. Maximum isolation between analog and digital is achieved by connecting the ground planes back at the supplies. Note that Figure 31, as drawn, suggests a "star" ground system for the analog circuitry, with all ground lines being connected, in this case, to the ADC's analog ground. However, when ground planes are used, it is sufficient to connect ground pins to the nearest point on the low impedance ground plane.

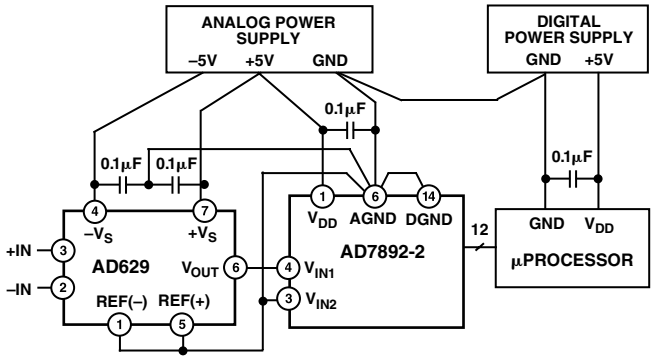


Figure 31. Optimal Grounding Practice for a Bipolar Supply Environment with Separate Analog and Digital Supplies

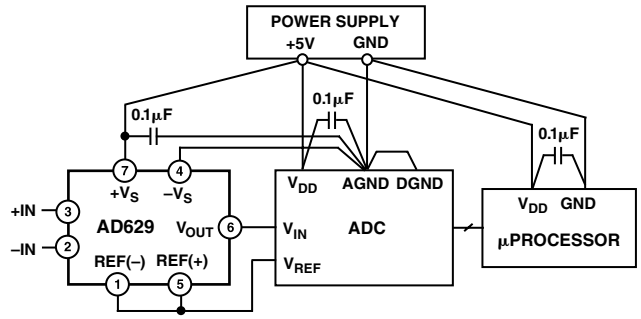


Figure 32. Optimal Ground Practice in a Single Supply Environment

If there is only a single power supply available, it must be shared by both digital and analog circuitry. Figure 32 shows how to minimize interference between the digital and analog circuitry. In this example, the ADC's reference is used to drive the AD629's REF(+) and REF(–) pins. This means that the reference must be capable of sourcing and sinking a current equal to V_{CM}/ 200 kΩ. As in the previous case, separate analog and digital ground planes should be used (reasonably thick traces can be used as an alternative to a digital ground plane). These ground planes should be connected at the power supply's ground pin. Separate traces (or power planes) should be run from the power supply to the supply pins of the digital and analog circuits. Ideally, each device should have its own power supply trace, but these can be shared by a number of devices as long as a single trace is not used to route current to both digital and analog circuitry.

Using a Large Sense Resistor

Insertion of a large shunt resistance across the input Pins 2 and 3 will imbalance the input resistor network, introducing a common-mode error. The magnitude of the error will depend on the common-mode voltage and the magnitude of R_{SHUNT}. Table I shows some sample error voltages generated by a common-mode voltage of 200 V dc with shunt resistors from 20 Ω to 2000 Ω. Assuming that the shunt resistor has been selected to utilize the full ±10 V output swing of the AD629, the error voltage becomes quite significant as R_{SHUNT} increases.

Table I. Error Resulting from Large Values of R_{SHUNT} (Uncompensated Circuit)

R_S (Ω)	Error V_{OUT} (V)	Error Indicated (mA)
20	0.01	0.5
1000	0.498	0.498
2000	1	0.5

If it is desired to measure low current or current near zero in a high common-mode environment, an external resistor equal to the shunt resistor value may be added to the low impedance side of the shunt resistor as shown in Figure 33.

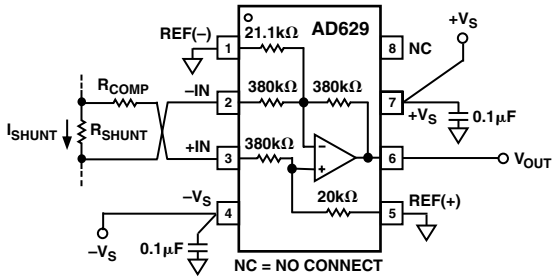


Figure 33. Compensating for Large Sense Resistors

Output Filtering

A simple 2-pole low-pass Butterworth filter can be implemented using the OP177 at the output of the AD629 to limit noise at the output, as shown in Figure 34. Table II gives recommended component values for various corner frequencies, along with the peak-to-peak output noise for each case.

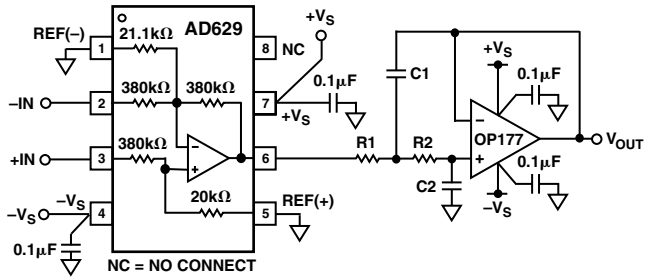


Figure 34. Filtering of Output Noise Using a 2-Pole Butterworth Filter

Table II. Recommended Values for 2-Pole Butterworth Filter

Corner Frequency	R1	R2	C1	C2	Output Noise (p-p)
No Filter					3.2 mV
50 kHz	2.94 kΩ ± 1%	1.58 kΩ ± 1%	2.2 nF ± 10%	1 nF ± 10%	1 mV
5 kHz	2.94 kΩ ± 1%	1.58 kΩ ± 1%	22 nF ± 10%	10 nF ± 10%	0.32 mV
500 Hz	2.94 kΩ ± 1%	1.58 kΩ ± 1%	220 nF ± 10%	0.1 µF ± 10%	100 µV
50 Hz	2.7 kΩ ± 10%	1.5 kΩ ± 10%	2.2 µF ± 20%	1 µF ± 20%	32 µV

Output Current and Buffering

The AD629 is designed to drive loads of 2 kΩ to within 2 V of the rails, but can deliver higher output currents at lower output voltages (see Figure 15). If higher output current is required, the AD629's output should be buffered with a precision op amp such as the OP113 as shown in Figure 35. This op amp can swing to within 1 V of either rail while driving a load as small as 600 Ω.

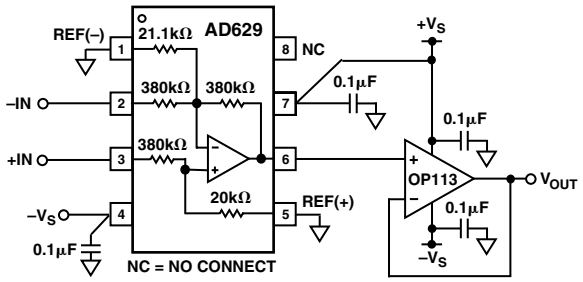


Figure 35. Output Buffering Application

A Gain of 19 Differential Amplifier

While low level signals can be connected directly to the –IN and +IN inputs of the AD629, differential input signals can also be connected as shown in Figure 36 to give a precise gain of 19. However, large common-mode voltages are no longer permissible. Cold junction compensation can be implemented using a temperature sensor such as the AD590.

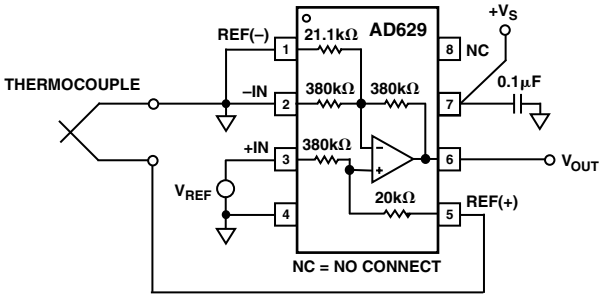


Figure 36. A Gain of 19 Thermocouple Amplifier

Error Budget Analysis Example 1

In the dc application below, the 10 A output current from a device with a high common-mode voltage (such as a power supply or current-mode amplifier) is sensed across a 1 Ω shunt resistor (Figure 37). The common-mode voltage is 200 V, and the resistor terminals are connected through a long pair of lead wires located in a high-noise environment, for example, 50 Hz/60 Hz 440 V ac power lines. The calculations in Table III assume an induced noise level of 1 V at 60 Hz on the leads, in addition to a full-scale dc differential voltage of 10 V. The error budget table quantifies the contribution of each error source. Note that the dominant error source in this example is due to the dc common-mode voltage.

Table III. AD629 vs. INA117 Error Budget Analysis Example 1 (V_{CM} = 200 V dc)

Error Source	AD629	INA117	Error, ppm of FS AD629	INA117
ACCURACY, T_A = 25°C				
Initial Gain Error	$(0.0005 \times 10) \div 10\ V \times 10^6$	$(0.0005 \times 10) \div 10\ V \times 10^6$	500	500
Offset Voltage	$(0.001\ V \div 10\ V) \times 10^6$	$(0.002\ V \div 10\ V) \times 10^6$	100	200
DC CMR (Over Temperature)	$(224 \times 10^{-6} \times 200\ V) \div 10\ V \times 10^6$	$(500 \times 10^{-6} \times 200\ V) \div 10\ V \times 10^6$	4,480	10,000
		Total Accuracy Error:	5,080	10,700
TEMPERATURE DRIFT (85°C)				
Gain	10 ppm/°C × 60°C	10 ppm/°C × 60°C	600	600
Offset Voltage	(20 μV/°C × 60°C) × 10^6/10 V	(40 μV/°C × 60°C) × 10^6/10 V	120	240
		Total Drift Error:	720	840
RESOLUTION				
Noise, Typ, 0.01–10 Hz, μV p-p	$15\ \mu V \div 10\ V \times 10^6$	$25\ \mu V \div 10\ V \times 10^6$	2	3
CMR, 60 Hz	$(141 \times 10^{-6} \times 1\ V) \div 10\ V \times 10^6$	$(500 \times 10^{-6} \times 1\ V) \div 10\ V \times 10^6$	14	50
Nonlinearity	$(10^{-5} \times 10\ V) \div 10\ V \times 10^6$	$(10^{-5} \times 10\ V) \div 10\ V \times 10^6$	10	10
		Total Resolution Error:	26	63
		Total Error:	5,826	11,603

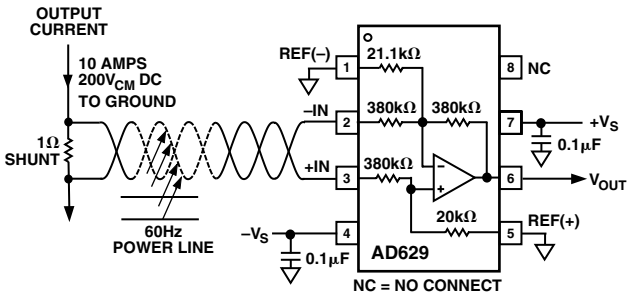


Figure 37. Error Budget Analysis Example 1. V_{IN} = 10 V Full-Scale, V_{CM} = 200 V DC. R_{SHUNT} = 1 Ω, 1 V p-p 60 Hz Power-Line Interference

Error Budget Analysis Example 2

This application is similar to the previous example except that the sensed load current is from an amplifier with an ac common-mode component of ±100 V (frequency = 500 Hz) present on the shunt (Figure 38). All other conditions are the same as before. Note that the same kind of power line interference can happen as detailed in Example 1. However, the ac common-mode component of 200 V p-p coming from the shunt is much larger than the interference of 1 V p-p, so that this interference component can be neglected.

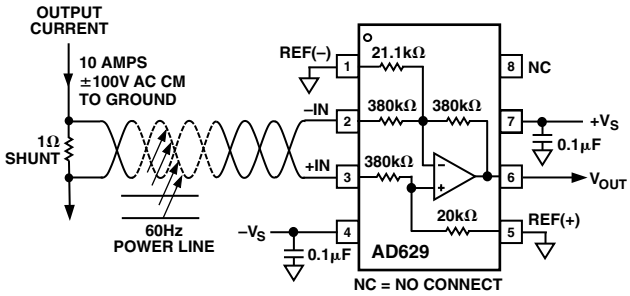


Figure 38. Error Budget Analysis Example 2. V_{IN} = 10 V Full-Scale, V_{CM} = ±100 V at 500 Hz, R_{SHUNT} = 1 Ω

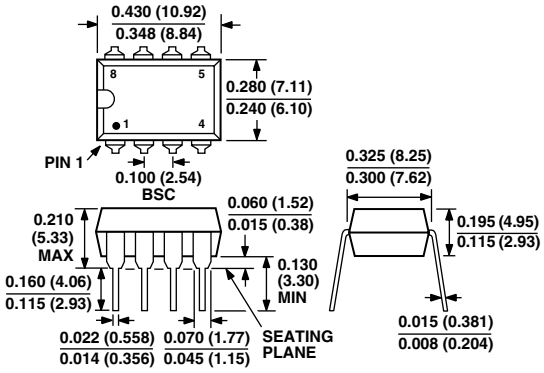
Table IV. AD629 vs. INA117 AC Error Budget Example 2 (V_{CM} = ±100 V @ 500 Hz)

Error Source	AD629	INA117	Error, ppm of FS AD629	INA117
ACCURACY, T_A = 25°C				
Initial Gain Error	(0.0005 × 10) ÷ 10 V × 10^6	(0.0005 × 10) ÷ 10 V × 10^6	500	500
Offset Voltage	(0.001 V ÷ 10 V) × 10^6	(0.002 V ÷ 10 V) × 10^6	100	200
		Total Accuracy Error:	600	700
TEMPERATURE DRIFT (85°C)				
Gain	10 ppm/°C × 60°C	10 ppm/°C × 60°C	600	600
Offset Voltage	(20 μV/°C × 60°C) × 10^6/10 V	(40 μV/°C × 60°C) × 10^6/10 V	120	240
		Total Drift Error:	720	840
RESOLUTION				
Noise, Typ, 0.01–10 Hz, μV p-p	15 μV ÷ 10 V × 10^6	25 μV ÷ 10 V × 10^6	2	3
CMR @ 60 Hz	(141 × 10^{-6} × 1 V) ÷ 10 V × 10^6	(500 × 10^{-6} × 1 V) ÷ 10 V × 10^6	14	50
Nonlinearity	(10^{-5} × 10 V) ÷ 10 V × 10^6	(10^{-5} × 10 V) ÷ 10 V × 10^6	10	10
AC CMR @ 500 Hz	(141 × 10^{-6} × 200 V) ÷ 10 V × 10^6	(500 × 10^{-6} × 200 V) ÷ 10 V × 10^6	2,820	10,000
		Total Resolution Error:	2,846	10,063
		Total Error:	4,166	11,603

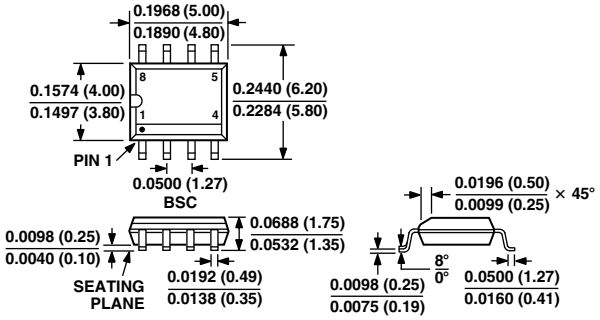
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP
(N-8)



8-Lead SOIC
(SO-8)



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