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PRODUCT INFORMATION

FX601A Tone Operated Monostable Timer

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Choice of high sensitivity or Schmitt inputs

Fast response time

Operation over a wide range of frequencies

High noise immunity on Schmitt input

Wide choice of VDD operating range

Operational parameters set by external components

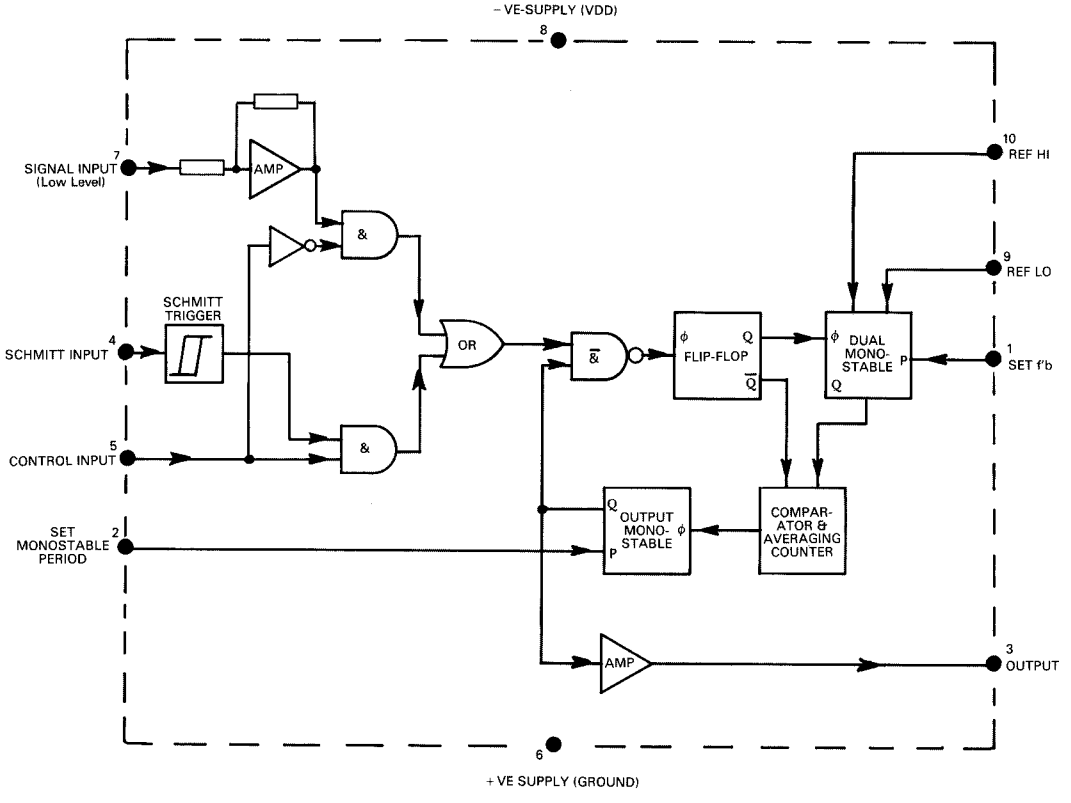


Fig. 1 FX601A Internal Block Diagram

FX601A

The FX601A is constructed in monolithic microcircuit form using PMOS technology. It is designed for use as a tone decoder in remote control, instrumentation, automation, communications and telemetry systems, where specific tone frequencies are used to control remote switching functions, such as SPM (Subscriber's Private Metering).

The FX601A is a tone triggered monostable timer, where the integral output switch is turned ON for an accurately defined time following receipt of an inband trigger tone. This timed period is externally adjustable from a few milliseconds to one hour at duty cycles of up to 90%. The trigger tone frequency, bandwidth and output monostable period are externally set using simple RC networks.

(See Fig. 1 Block Diagram. Fig. 7 Pin Data and External Component Connections)

NOTE: *External capacitors are to be low-leakage type and resistors are to be high-stability type. In the following formulae, the resistor values are in MΩ and capacitor values are in μF.*

1. SET f'b

Dual Monostable is set to Lower Bandedge (f'b) which is determined by $f'b = \frac{1}{0.69\ R1C1}$ (Hz) where 0.69 is a design constant K, recommended minimum values of *R1 = 360kΩ, C1 = 470 pF *(See Fig. 2).*
* For R1 values less than 360kΩ, refer to Fig. 3 for 'K' factor

2. SET MONOSTABLE PERIOD

Monostable Output period at pin 3 is set by a network R2 and C2 connected to this pin as shown in Fig. 7.

3. MONOSTABLE OUTPUT

An 'Open drain' output which requires a load resistor between this pin and VDD. Monostable Output period (Tm) is determined by components attached to pin 2. Tm = 0.69 R2C2, where 0.69 is a design constant K, recommended minimum values of R2 = 360kΩ and C2 = 470 pF. *(See Fig. 4).*

4. SCHMITT INPUT

High Impedance Input with a logic '0' of 33% of VDD and a logic '1' of 66% of VDD. This input is a.c. coupled and biased to a 50% VDD by means of a potential divider using two 1MΩ resistors. *(See Figs. 7 and 5).*

5. CONTROL INPUT

Selects either Low-Level Input (pin 7) when this pin is open circuit or negative (logic '1') or Schmitt Input (pin 4) when positive (logic '0').

6. +VE SUPPLY (GROUND)

The device uses negative logic (i.e. logic '1' = negative and logic '0' = positive). Either positive or negative supplies may be connected to earth. The can of the device is internally connected to the positive supply pin.

7. SIGNAL INPUT (Low-Level Input)

A high sensitivity signal input. Low-level signals should be a.c. coupled. High-level pulse signals $\geqslant (-6V)$ can be directly coupled. The signal input can be sinewave, squarewave or pulse *(See Figs. 1 and 6).*

8. −VE SUPPLY (VDD)

9. REF. LO
10. REF. HI

External network RK1, RK2 and RK3 connected as shown in Fig. 7 to set the required bandwidth. The bandwidth is determined by the ratio of RK2 to RK1.

$$RK2 = \frac{RK1 \times BW(\%)}{1.6 \times 100}$$

where RK1 = 10kΩ, RK3 = (RK1 + RK2) and 1.6 is a constant factor. The tolerance on this factor is ± 15% when measured at a bandwidth of 10%.

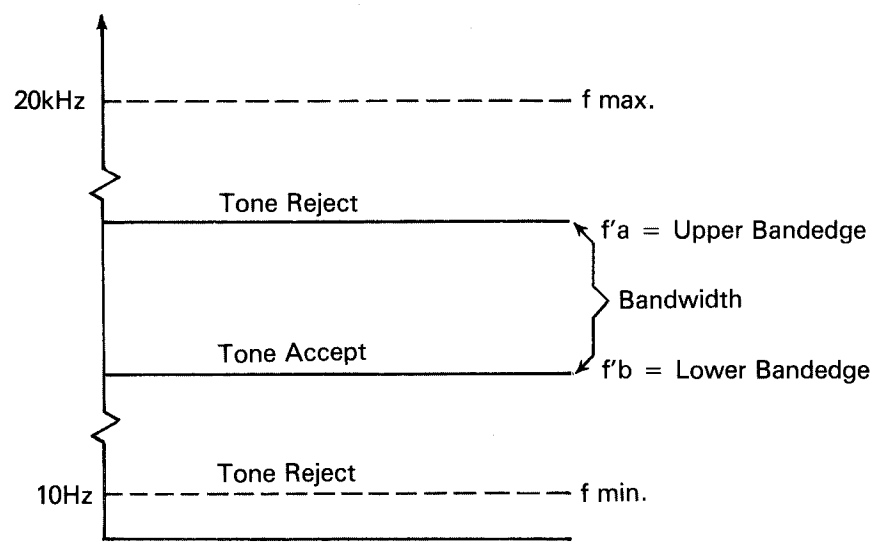


Fig.2. FX601A Typical Tone Channel

Typical Performance Curves

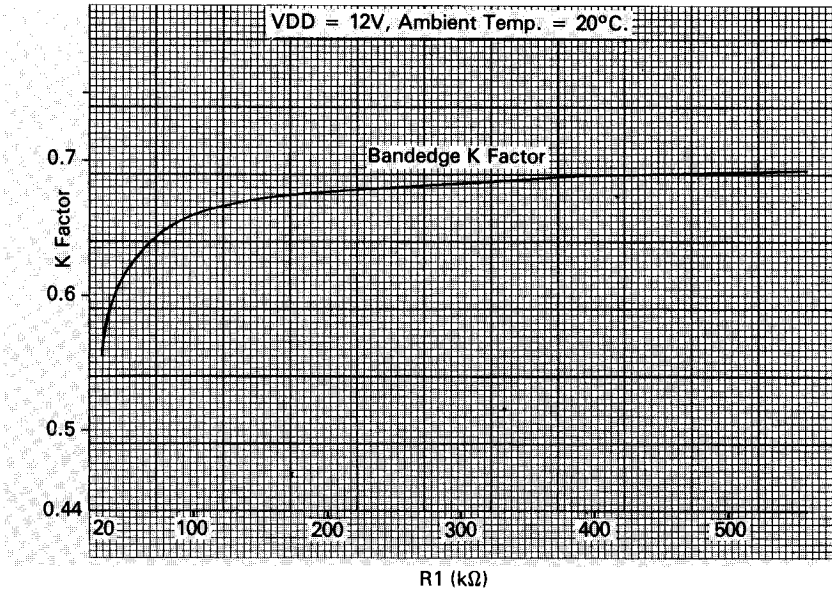


Fig. 3 FX601A Typical Variation of K Factor With R1

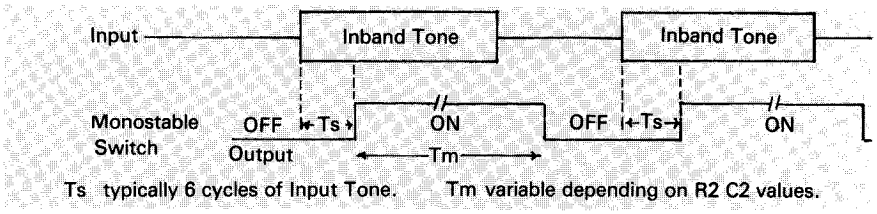


Fig. 4 FX601A Output Switching Waveform

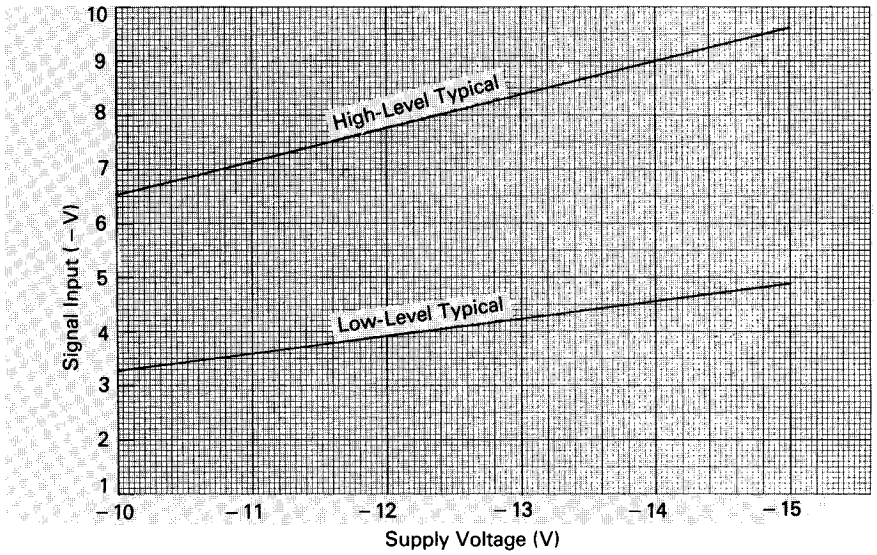


Fig. 5 FX601A Schmitt Input Thresholds

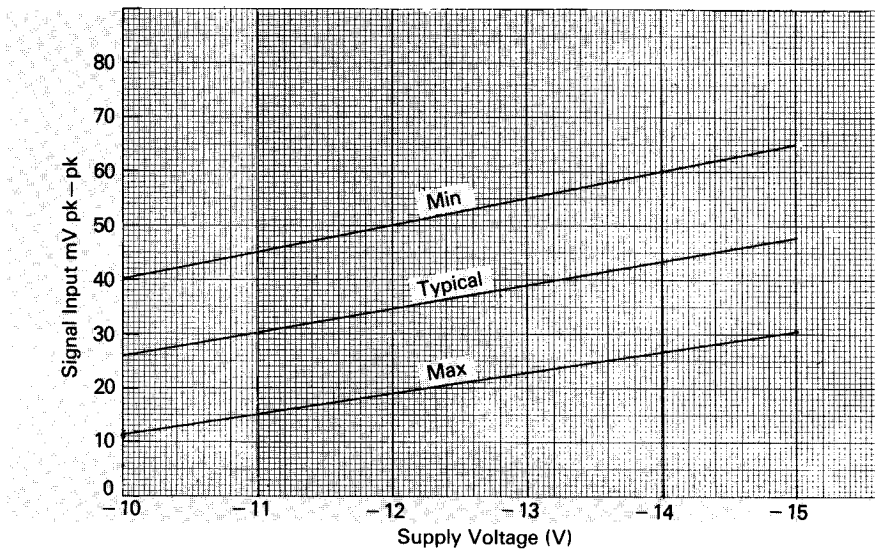


Fig. 6 FX601A Sensitivity Low-Level Input

Maximum Ratings

Max. voltage between any pin and +VE supply pin	−20V & +0.3V.
Max. output switch load current	−10mA
Max. device dissipation @ 25°C ambient temperature	400mW
Operating temperature range	−30°C to + 85°C
Storage temperature range	−55°C to + 125°C

Characteristics

(Ambient temperature = 20°C, VDD = −12.0V, operating frequencies 10Hz to 3kHz unless specified)

Symbol	Parameter	Conditions & Notes	Min.	Typ.	Max.	Unit
VDD	Supply voltage	Operating range	−10.0	−12.0	−15.0	V
IDD	Supply current			3.5	6	mA
	Sensitivity					
	Low Level Input					mV
	(Pin 7)		50		20	pk-pk
	Schmitt Input					
	(Pin 4)	Low threshold	−3.6	−4.0	−4.4	V
	(Pin 4)	High threshold	−7.6	−8.0	−8.4	V
Ts	Response Time		5	6	7	Cycle
I'in	Schmitt input leakage current (Pin 4)			100		nA
R'in	Input Impedance (Pin 7)		35	70	110	kΩ
R'on	Output ON Resistance			400	1k	Ω
	Control input logic threshold		−2.5	−3.0	−3.5	V
K	Constant K	R1 and R2 >360kΩ	0.66	0.69	0.72	

Fig. 7 **Pin Data**

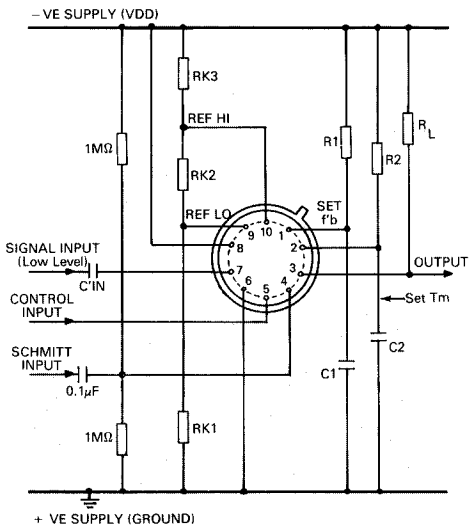
FX601A (Package Type T0 — 100)

Pin No.	Connection
1	Set f'b
2	Set Monostable Period
3	Monostable Output
4	Schmitt Input
5	Control Input
6	+VE Supply (Ground)
7	Low Level Input
8	−VE Supply (VDD)
9	Reference LO
10	Reference HI

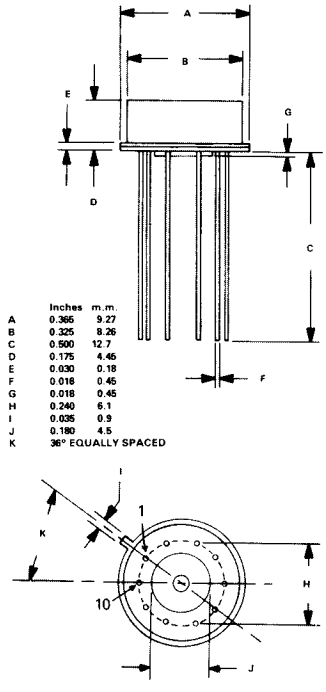
Handling Precautions

The FX601A is a PMOS integrated circuit which includes input protection. However, precautions should be taken to prevent static discharge which can cause damage.

External Component Connections



Package Outline



View from pinside

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