# A5970D

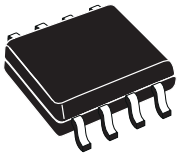
## 1.5A switch step down switching regulator for automotive applications

## Features

- Qualified following the AEC-Q100 requirements (temperature Grade 3), see PPAP for more details.
- Temperature range -40 °C to 85 °C
- Up to 1 A DC output current
- Operating input voltage from 4.4 V to 36 V
- Output voltage adjustable from 1.235 V to 35 V
- Low dropout operation: 100 % duty cycle
- 250 kHz Internally fixed frequency
- Voltage feedforward
- Zero load current operation
- Internal current limiting
- Inhibit for zero current consumption
- Synchronization
- Protection against feedback disconnection
- Thermal shutdown

## Applications

- Dedicated to automotive applications



SO-8

## Description

The A5970D is a step down monolithic power switching regulator capable to deliver up to 1 A at output voltages from 1.2 V to 35 V.

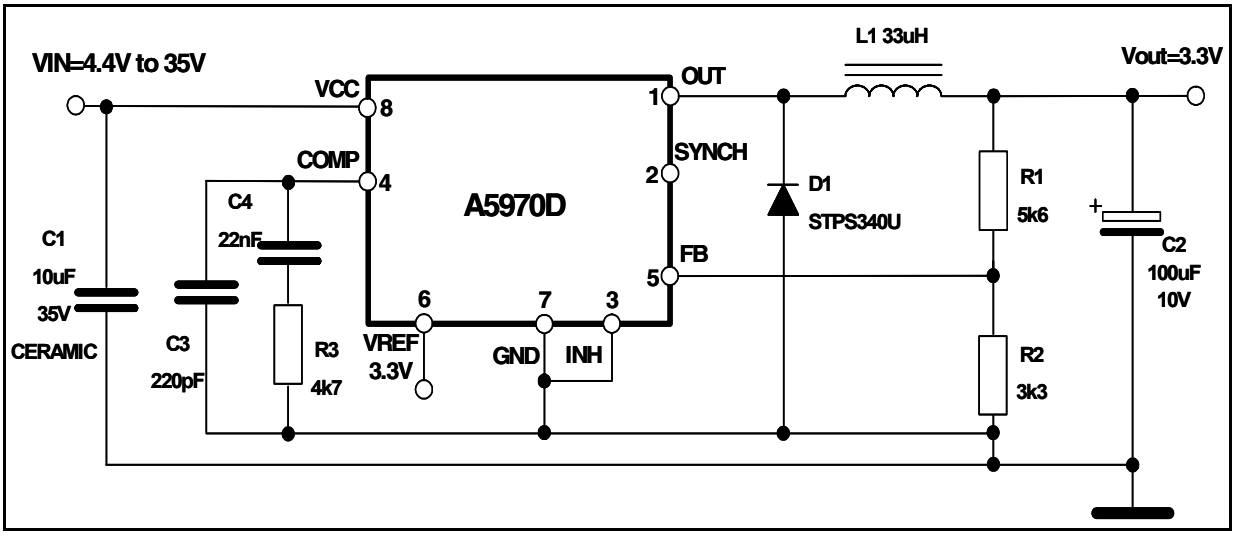
The device uses an internal P-channel D-MOS transistor (with a typical Rdson of 250 mΩ) as switching element to minimize the size of the external components.

An internal oscillator fixes the switching frequency at 250 kHz.

Having a minimum input voltage of 4.4 V only, it is particularly suitable for 5 V bus.

Pulse by pulse current limit with the internal frequency modulation offers an effective constant current short circuit protection.

**Figure 1. Typical application**

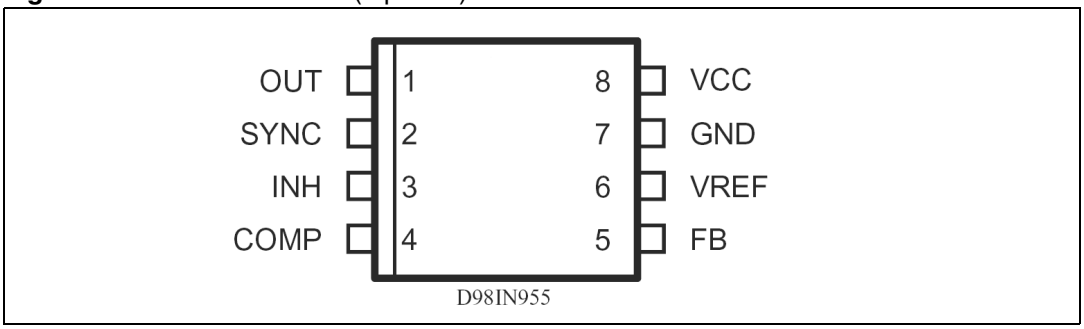


# Contents

# 1 Pin settings

## 1.1 Pin connection

**Figure 2. Pin connection** (top view)




## 1.2 Pin description

**Table 1. Pin description**

| N | Pin | Description |
|---|---|---|
| 1 | OUT | Regulator output. |
| 2 | SYNCH | Master/slave synchronization. |
| 3 | INH | A logical signal (active high) disables the device. If INH not used the pin must be grounded. When it is open an internal pull-up disable the device. |
| 4 | COMP | E/A output for frequency compensation. |
| 5 | FB | Feedback input. Connecting directly to this pin results in an output voltage of 1.23V. An extenal resistive divider is required for higher output voltages. |
| 6 | VREF | 3.3V $V_{REF}$. No cap is requested for stability. |
| 7 | GND | Ground. |
| 8 | VCC | Unregulated DC input voltage. |

# 2 Electrical data

## 2.1 Maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_8$ | Input voltage | 40 | V |
| $V_1$ | OUT pin DC voltage<br>OUT pin peak voltage at $\Delta t$=0.1µs | -1 to 40<br>-5 to 40 | V<br>V |
| $I_1$ | Maximum output current | int. limit. | |
| $V_4$ , $V_5$ | Analog pins | 4 | V |
| $V_3$ | INH | -0.3 to $V_{CC}$ | V |
| $V_2$ | SYNCH | -0.3 to 4 | V |
| $P_{TOT}$ | Power dissipation at $T_A \leq 70°C$ | 0.75 | W |
| $T_J$ | Operating junction temperature range | -40 to 150 | °C |
| $T_{STG}$ | Storage temperature range | -55 to 150 | °C |

## 2.2 Thermal data

**Table 3. Thermal data**

| Symbol | Parameter | SO8 | Unit |
|---|---|---|---|
| $R_{thJA}$ | Maximum thermal resistance junction-ambient | 120 (1) | °C/W |

1. Package mounted on board

# 3 Electrical characteristics

**Table 4. Electrical characteristics** ($T_J$=-40 to 85°C, $V_{CC}$ = 12V, unless otherwise specified)

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Operating input voltage range | $V_0$=1.235V; $I_0$=1A | 4.4 | | 36 | V |
| $R_{DS(on)}$ | Mosfet on resistance | | | 0.250 | 0.5 | Ω |
| $I_L$ | Maximum limiting current | $V_{CC}$=5V; | 1.5 | 1.87 | 2.25 | A |
| $f_{SW}$ | Switching frequency | | 212 | 250 | 280 | kHz |
| | Duty cycle | | 0 | | 100 | % |
| **Dynamic characteristics** (see test circuit). | | | | | | |
| $V_5$ | Voltage feedback | 4.4V<$V_{CC}$<36V, 20mA<$I_0$<2A | 1.198 | 1.235 | 1.272 | V |
| η | Efficiency | $V_0$=5V, $V_{CC}$=12V | | 90 | | % |
| **DC characteristics** | | | | | | |
| $I_{qop}$ | Total operating quiescent current | | | 3 | 5 | mA |
| $I_q$ | Quiescent current | Duty cycle=0; $V_{FB}$=1.5V | | | 2.5 | mA |
| $I_{qst\text{-}by}$ | Total stand-by quiescent current | $V_{inh}$ > 2.2V | | 50 | 100 | µA |
| | | $V_{CC}$=36V; $V_{inh}$ > 2.2V | | 80 | 150 | µA |
| **Inhibit** | | | | | | |
| | INH threshold voltage | Device ON | | | 0.8 | V |
| | | Device OFF | 2.2 | | | V |
| **Error amplifier** | | | | | | |
| $V_{OH}$ | High level output voltage | $V_{FB}$=1V | 3.5 | | | V |
| $V_{OL}$ | Low level output voltage | $V_{FB}$=1.5V | | | 0.4 | V |
| $I_{o\ source}$ | Source output current | $V_{COMP}$ = 1.9V; $V_{FB}$ = 1V | 190 | 300 | | µA |
| $I_{o\ sink}$ | Sink output current | $V_{COMP}$ = 1.9V; $V_{FB}$ = 1.5V | 1 | 1.5 | | mA |
| $I_b$ | Source bias current | | | 2.5 | 4 | µA |
| | DC open loop gain | $R_L$= ∞ | 50 | 65 | | dB |
| gm | Transconductance | $I_{COMP}$ = -0.1mA to 0.1mA; $V_{COMP}$ = 1.9V | | 2.3 | | mS |

**Table 4. Electrical characteristics** ($T_J$=-40 to 85°C, $V_{CC}$ = 12V, unless otherwise specified)

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Synch function** | | | | | | |
| | High input voltage | $V_{CC}$= 4.4 to 36V; | 2.5 | | $V_{REF}$ | V |
| | Low input voltage | $V_{CC}$= 4.4 to 36V; | | | 0.74 | V |
| | Slave synch current | $V_{synch}$= 0.74V (1)<br>$V_{synch}$= 2.33V | 0.11<br>0.21 | | 0.25<br>0.45 | mA |
| | Master output amplitude | $I_{source}$= 3mA | 2.75 | 3 | | V |
| | Output pulse width | no load,<br>$V_{synch}$= 1.65V | 0.20 | 0.35 | | µs |
| **Reference section** | | | | | | |
| | Reference voltage | $I_{REF}$ = 0 to 5mA<br>$V_{CC}$ = 4.4V to 36V | 3.2 | 3.3 | 3.399 | V |
| | Line regulation | $I_{REF}$ = 0mA<br>$V_{CC}$ = 4.4V to 36V | | 5 | 10 | mV |
| | Load regulation | $I_{REF}$ = 0mA | | 8 | 15 | mV |
| | Short circuit current | | 10 | 18 | 30 | mA |

1. Guaranteed by design

# 4 Typical characteristics

**Figure 3. Junction temperature vs. output current**

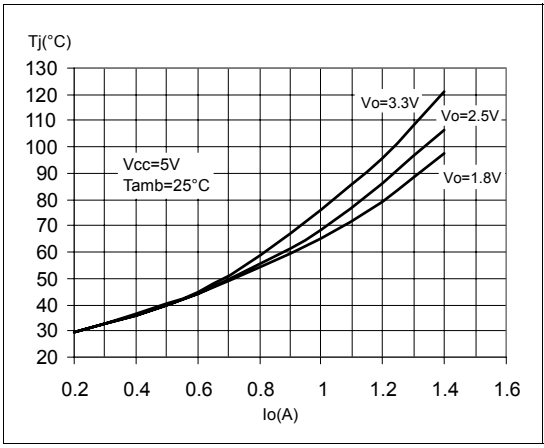



**Figure 4. Load regulator**

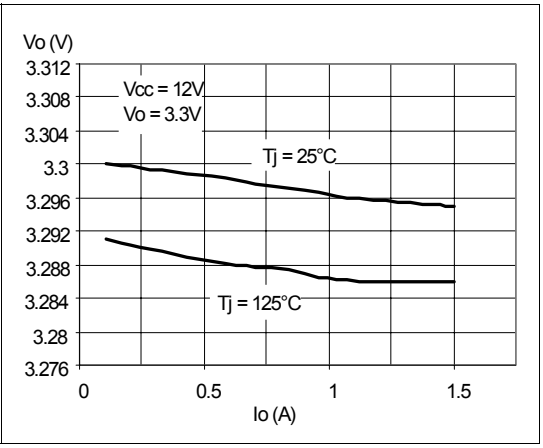



**Figure 5. Junction temperature vs. output current**

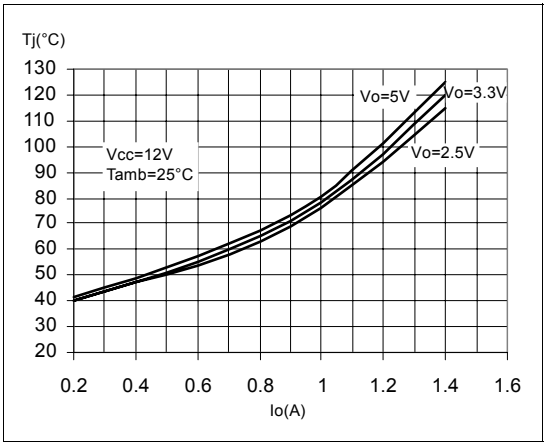



**Figure 6. Line regulator**

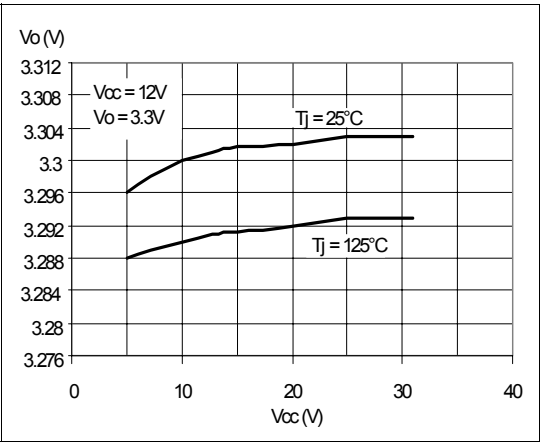



**Figure 7. Junction temperature vs. output current**

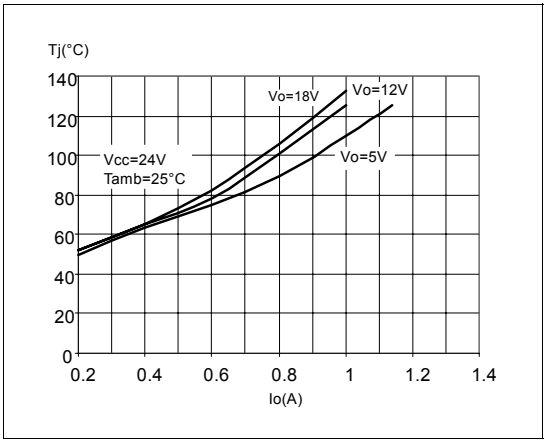



**Figure 8. Output voltage vs. junction temperature**

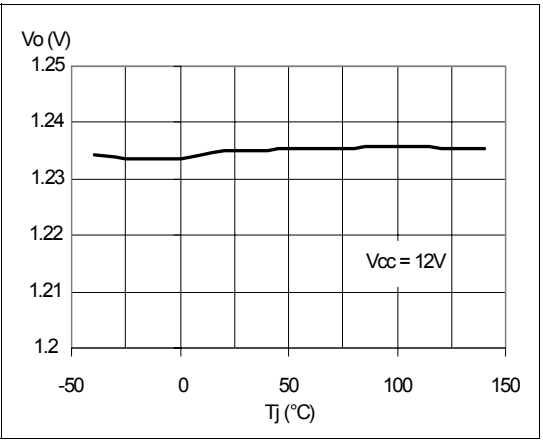


**Figure 9. Quiescent current vs. junction temperature**

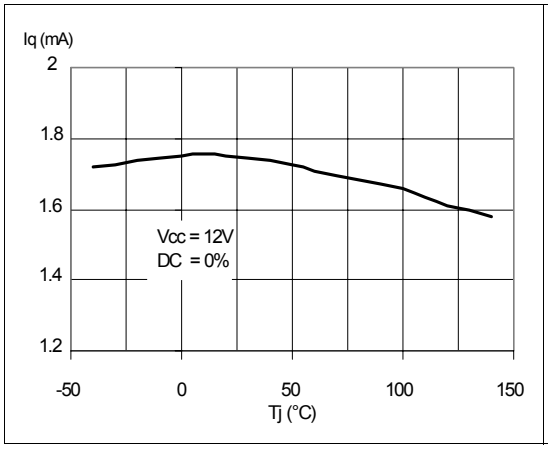



**Figure 10. Switching frequency vs. junction temperature**

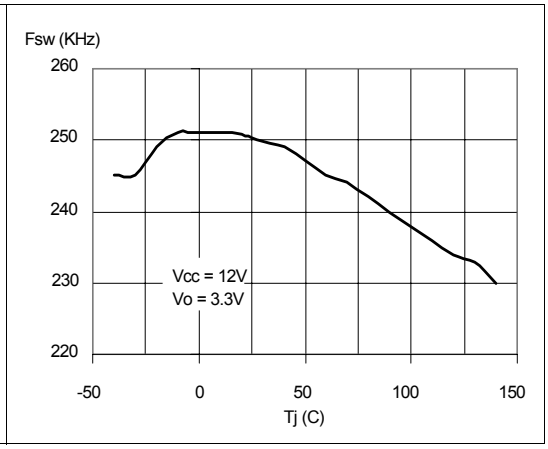



**Figure 11. Shutdown current vs.junction temperature**

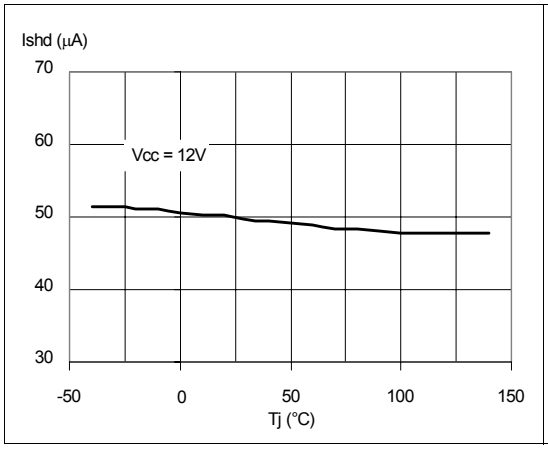



**Figure 12. Efficiency vs. output current**

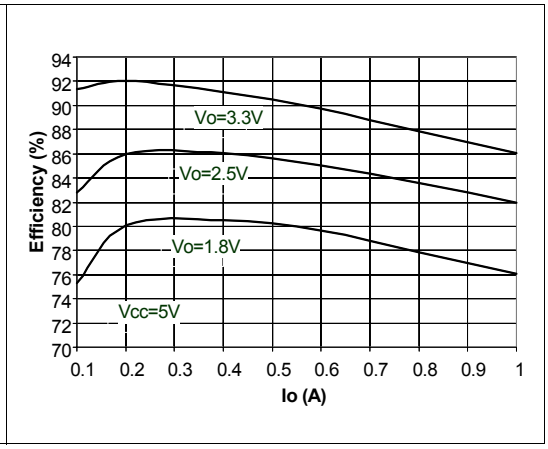
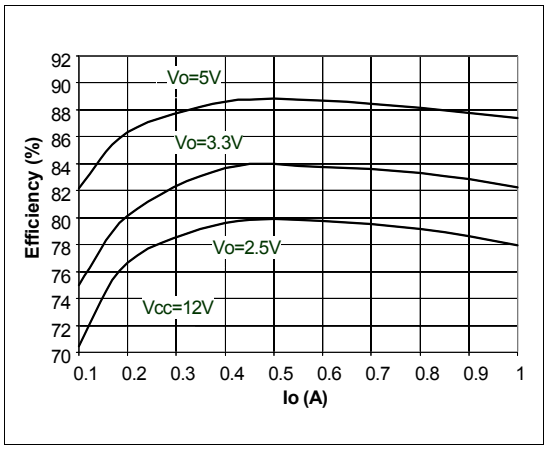



**Figure 13. Efficiency vs. output current**



# 5 Package mechanical data

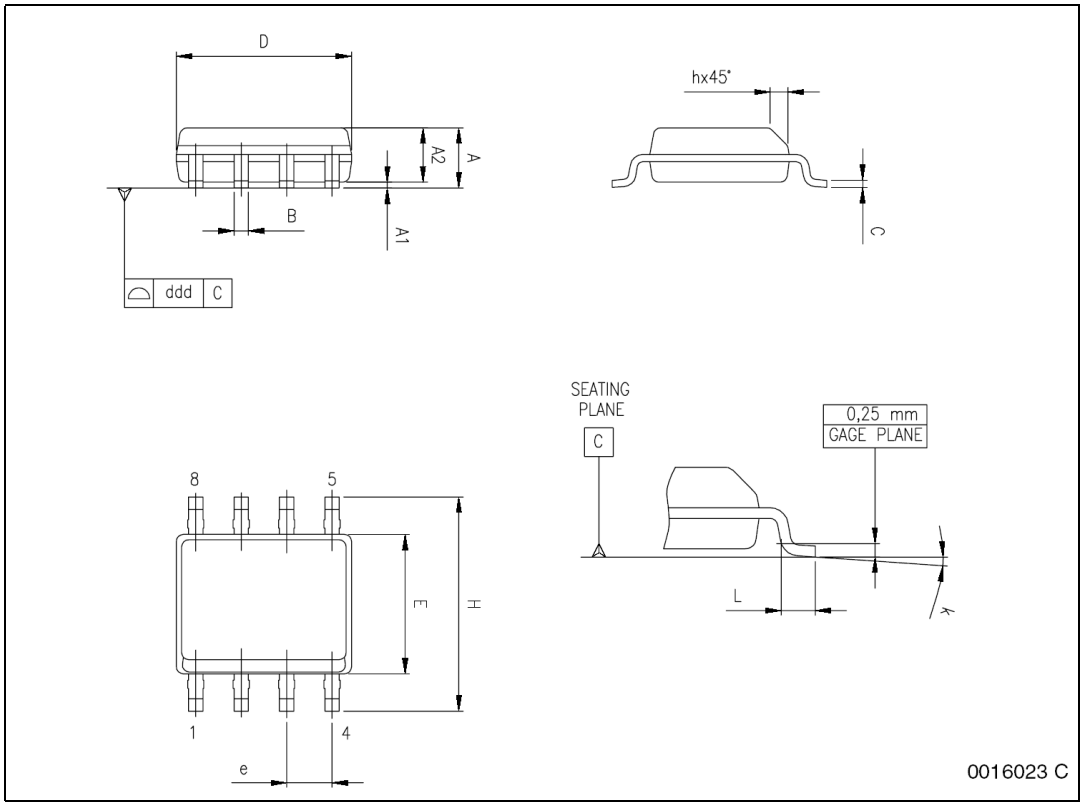
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

**Table 5. SO-8 mechanical data**

| Dim. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 1.35 | | 1.75 | 0.053 | | 0.069 |
| | | | | | | |
| A1 | 0.10 | | 0.25 | 0.004 | | 0.010 |
| A2 | 1.10 | | 1.65 | 0.043 | | 0.065 |
| B | 0.33 | | 0.51 | 0.013 | | 0.020 |
| C | 0.19 | | 0.25 | 0.007 | | 0.010 |
| D (1) | 4.80 | | 5.00 | 0.189 | | 0.197 |
| E | 3.80 | | 4.00 | 0.15 | | 0.157 |
| e | | 1.27 | | | 0.050 | |
| H | 5.80 | | 6.20 | 0.228 | | 0.244 |
| h | 0.25 | | 0.50 | 0.010 | | 0.020 |
| L | 0.40 | | 1.27 | 0.016 | | 0.050 |
| k | 0° (min.), 8° (max.) | | | | | |
| ddd | | | 0.10 | | | 0.004 |

1. Dimensions D does not include mold flash, protru-sions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

**Figure 14. Package dimensions**



# 6 Order codes

**Table 6. Order code**

| Order code | Package | Packing |
|---|---|---|
| A5970D | SO-8 | Tube |
| A5970D13TR | | Tape and reel |

# 7 Revision history

Table 7. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 06-Aug-2007 | 1 | Initial release. |
| 24-Oct-2007 | 2 | Updated: *Table 4 on page 5* |

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