

128 TAPS Single Channel Digital Potentiometer with I²C Interface

Check for Samples: [TPL0401A](#), [TPL0401B](#), [TPL0401C](#)

FEATURES

- Single Channel, 128-Position Resolution
- 10 k Ω End-to-End Resistance Options
- Low Temperature Coefficient: 35 ppm/ $^{\circ}$ C
- I²C Serial Interface
- 2.7 V to 5.5 V Single-Supply Operation
- \pm 20% Resistance Tolerance
- 'A' and 'B' Versions Have Different I²C Addresses
- 'L' Terminal of 'A' and 'B' version is internal and connected To GND
- 'H' Terminal of 'C' Version is Internal and Floating
- Operating Temperature -40° C to 125° C
- Available in Industry Standard SC70 Packages
- ESD Performance Tested per JESD 22
 - 2000 V Human Body Model (A114-B, Class II)

APPLICATIONS

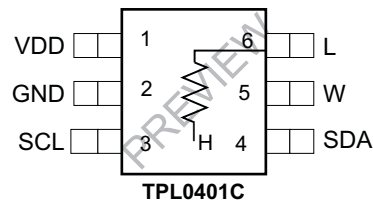
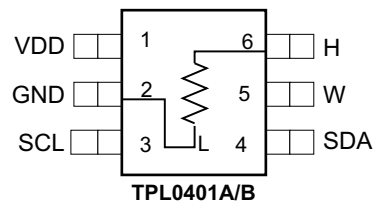
- Low Power DDR3 Voltage Reference
- Adjustable Power Supplies
- Adjustable Gain Amplifiers and Offset Trimming
- Precision Calibration of Set Point Thresholds
- Sensor Trimming and Calibration
- Mechanical Potentiometer Replacement

DESCRIPTION

The TPL0401 is a single channel, linear-taper digital potentiometer with 128 wiper positions. The TPL0401A/B have the low terminal internal and connected to GND. The position of the wiper can be adjusted using an I²C interface. The TPL0401 is available in a 6-pin SC-70 package with a specified temperature range of -40° C to 125° C. The part has a 10k end-to-end resistance and can operate with a supply voltage range of 2.7V to 5.5V. This kind of product is widely used in setting the voltage reference for low power DDR3 memory.

The TPL0401A/B have the Low Terminal internal and connected to GND. The TPL0401C has the High Terminal internal and floating.

SC-70 DCK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T _A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | END-TO-END RESISTANCE | I ² C ADDRESS | TOP-SIDE MARKING |
|------------------------------------|------------------------|---------------|-----------------------|-----------------------|--------------------------|------------------|
| -40° C to 125° C | SC70 – DCK | Tape and Reel | TPL0401A-10DCKR | 10-k Ω | 0101110 | 7TV |
| | | | TPL0401B-10DCKR | 10-k Ω | 0111110 | 7UV |
| | | | TPL0401C-50DCKR | 50-k Ω | 0101110 | TBD |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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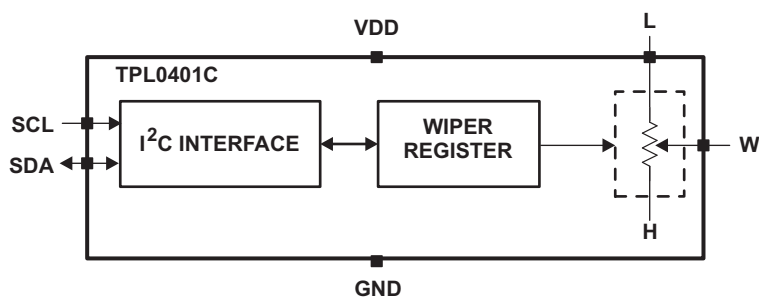
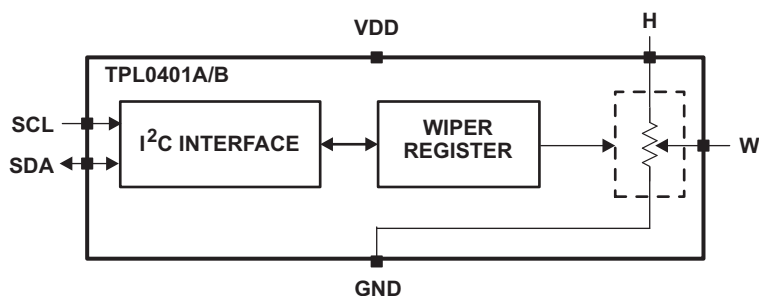


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN FUNCTIONS

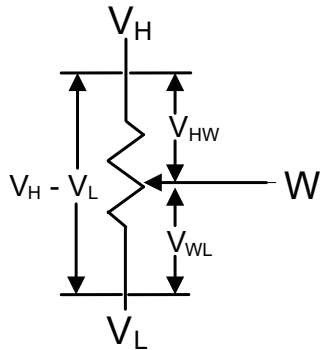
| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|------------|----------|--------|-------------------------|
| 1 | VDD | Power | Positive Supply Voltage |
| 2 | GND | Ground | Ground |
| 3 | SCL | Input | I2C Clock |
| 4 | SDA | I/O | I2C Data |
| 5 | W | I/O | Wiper terminal |
| 6 | H | I/O | High terminal |
| – | L | I/O | Low terminal |

FUNCTIONAL BLOCK DIAGRAM



DIGITAL POTENTIOMETER CONFIGURATIONS

VOLTAGE DIVIDER MODE

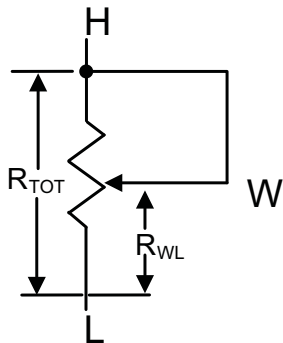


$$V_{HW} = (V_H - V_L) \times (1 - (D/128))$$

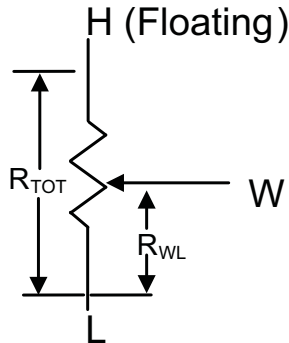
$$V_{WL} = (V_H - V_L) \times D/128$$

Where D = Decimal Value of Wiper Code

RHEOSTAT MODE A



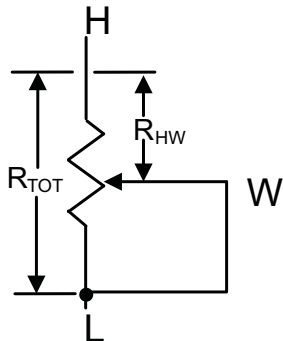
OR



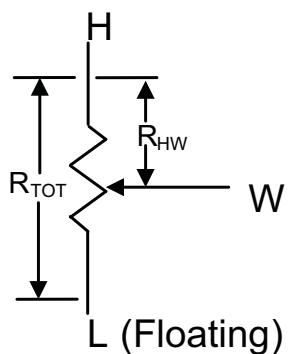
$$R_{WL} = R_{TOT} \times D/128$$

Where D = Decimal Value of Wiper Code

RHEOSTAT MODE B



OR



$$R_{HW} = R_{TOT} \times (1 - (D/128))$$

Where D = Decimal Value of Wiper Code

Figure 1. DPOT Configurations

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾⁽³⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------------|--|------|-----------------------|------|
| V _{DD} to GND | Supply voltage range | –0.3 | 7 | V |
| All other pins to GND | | –0.3 | V _{DD} +0.3 | V |
| I _H | Pulse current | | ±20 | mA |
| I _L | Continuous current | | ±5 | mA |
| I _W | | | ±1.3 | mA |
| V _I | Digital input voltage range | –0.3 | V _{DD} + 0.3 | V |
| θ _{JA} | Package thermal impedance ⁽⁴⁾ | | 259 | °C/W |
| T _{stg} | Storage temperature range | –65 | 150 | °C |

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

| | DESCRIPTION | MIN | MAX | Unit |
|---------------------------------|----------------------------------|---------------------|---------------------|------|
| V _{DD} | Supply Voltage | 2.7 | 5.5 | V |
| V _W , V _H | Terminal Voltage | 0 | V _{DD} | V |
| V _{IH} | Voltage Input High (SCLK, SDA) | 0.7 V _{DD} | | V |
| V _{IL} | Voltage Input Low (SCLK, SDA) | | 0.3 V _{DD} | V |
| I _W | Wiper Current | | ±2 | mA |
| T _A | Ambient Operating temperature | –40 | 128 | °C |

ANALOG SPECIFICATIONS

Typical values are specified at 25°C and V_{DD}=3.3V

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|-------|-------|-----------------|--------|
| R _{TOTAL} | End-to-end resistance (between H and L terminals) | TPL0401A/B-10 | 8 | 10 | 12 | kΩ |
| | | TPL0401C-50 | 40 | 50 | 60 | kΩ |
| V _H | Terminal voltage range | | 0 | | V _{DD} | V |
| R _H | Terminal resistance | | | 35 | 100 | Ω |
| R _W | Wiper resistance | | | 35 | 100 | Ω |
| C _H | Terminal capacitance | | | 10 | | pF |
| C _W | Wiper capacitance | | | 11 | | pF |
| I _{LKG} | Terminal leakage current | | | 0.1 | 1 | μA |
| TC _R | Resistance temperature coefficient | TPL0401A/B-10 | | 22 | | ppm/°C |
| | | TPL0401C-50 | | TBD | | ppm/°C |
| VOLTAGE DIVIDER MODE (TPL0401A, TPL0401B, V _H = V _{DD} , V _W = Not Loaded) | | | | | | |
| INL | Integral non-linearity | | −0.5 | | 0.5 | LSB |
| DNL | Differential non-linearity | | −0.25 | | 0.25 | LSB |
| ZS _{ERROR} | Zero-scale error | | 0 | 0.75 | 1.5 | LSB |
| FS _{ERROR} | Full-scale error | | −1.5 | −0.75 | 0 | LSB |
| T _{CV} | Ratiometric temperature coefficient | Wiper set at mid-scale | | 4 | | ppm/°C |
| BW | Bandwidth | Wiper set at mid-scale, C _{LOAD} = 10 pF | | 2862 | | kHz |
| T _{SW} | Wiper settling time | | | 0.152 | | μS |
| THD | Total harmonic distortion | V _H = 1 V _{RMS} at 1 kHz, V _L = V _{DD} /2, Measurement at W | | | 0.03 | % |
| RHEOSTAT MODE (TPL0401C) | | | | | | |
| RINL | Integral non-linearity | | | | TBD | LSB |
| RDNL | Differential non-linearity | | | | TBD | LSB |
| R _{OFFSET} | Offset | | | | TBD | LSB |
| RBW | Bandwidth | Code=0x00h, L Floating, Input applied to W, 10pF on H | | | TBD | kHz |

OPERATING SPECIFICATIONS

Typical values are specified at 25°C and V_{DD}=3.3V⁽¹⁾

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|--|------------------------------------|-----------------------|--------------------------------|-----|-------|
| I _{DD} (STBY) V _{DD} Standby current | -40 to 85°C | | | 0.5 | μA |
| | -40 to 125°C | | | 1.5 | μA |
| I _{IN-DIG} Digital Pins Leakage Current (SCL, SDA Inputs) | | -1 | | 1 | μA |
| SERIAL INTERFACE SPECS (SDA, SCL) | | | | | |
| V _{IH} Input high voltage | | 0.7 x V _{DD} | | 5.5 | V |
| V _{IL} Input low voltage | | 0 | 0.3 x V _{DD} | | V |
| V _{OL} Output low voltage | SDA Pin, I _{OL} = 4 mA | | | 0.4 | V |
| C _{IN} Pin capacitance | SCL, SDA Inputs | | 7 | | pF |
| I²C INTERFACE TIMING REQUIREMENTS | | | | | |
| | STANDARD MODE I ² C BUS | | FAST MODE I ² C BUS | | UNITS |
| | MIN | MAX | MIN | MAX | |
| f _{SCL} I ² C Clock frequency | 0 | 100 | 0 | 400 | kHz |
| t _{SCH} I ² C Clock high time | 4 | | 0.6 | | μs |
| t _{SCL} I ² C Clock low time | 4.7 | | 1.3 | | μs |
| t _{sp} I ² C Spike time | 0 | 50 | 0 | 50 | ns |
| t _{SDS} I ² C Serial data setup time | 250 | | 100 | | ns |
| t _{SDH} I ² C Serial data hold time | 0 | | 0 | | ns |
| t _{ICR} I ² C Input rise time | | 1000 | 20 + 0.1C _b | 300 | ns |
| t _{ICF} I ² C Input fall time | | 300 | 20 + 0.1C _b | 300 | ns |
| t _{ICF} I ² C Output fall time, 10 pF to 400 pF bus | | 300 | 20 + 0.1C _b | 300 | ns |
| t _{BUF} I ² C Bus free time between stop and start | 4.7 | | 1.3 | | μs |
| t _{STS} I ² C Start or repeater start condition setup time | 4.7 | | 1.3 | | μs |
| t _{STH} I ² C Start or repeater start condition hold time | 4 | | 0.6 | | μs |
| t _{SPS} I ² C Stop condition setup time | 4 | | 0.6 | | μs |
| t _{VD(DATA)} Valid data time, SCL low to SDA output valid | | 1 | | 1 | μs |
| t _{VD(DATA)} Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low | | 1 | | 1 | μs |

(1) Parameters with Min and Max limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested

TYPICAL CHARACTERISTICS

**INL vs
TAP POSITION (Potentiometer Mode)**

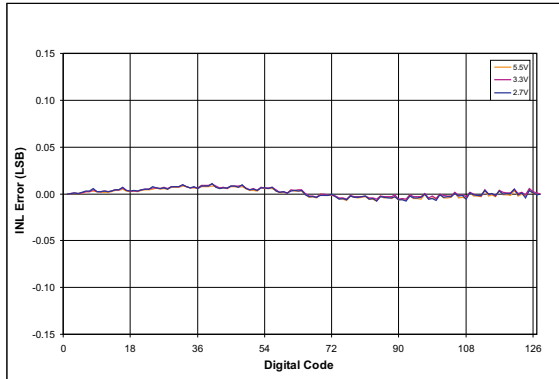


Figure 2.

**DNL vs
TAP POSITION (Potentiometer Mode)**

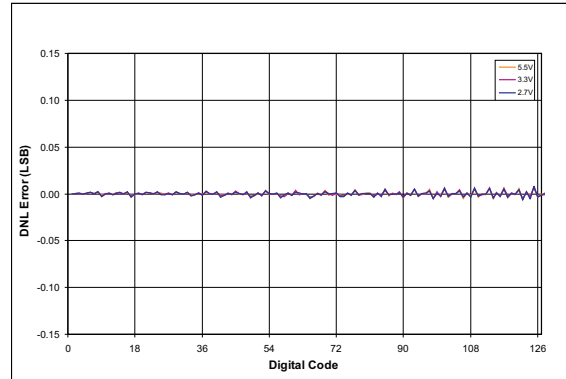


Figure 3.

**INL vs
TAP POSITION (Rheostat Mode)**

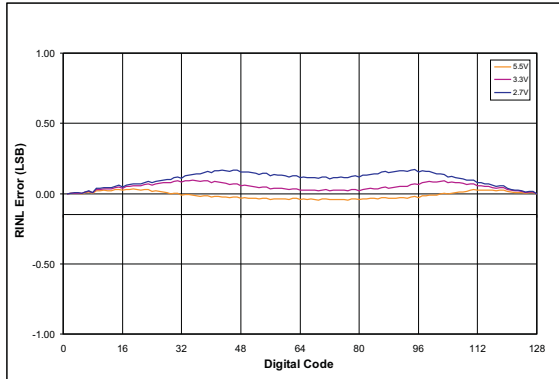


Figure 4.

**DNL vs
TAP POSITION (Rheostat Mode)**

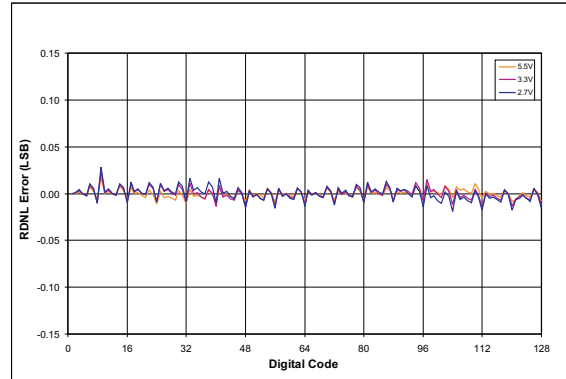


Figure 5.

**ZERO SCALE ERROR vs
TEMPERATURE**

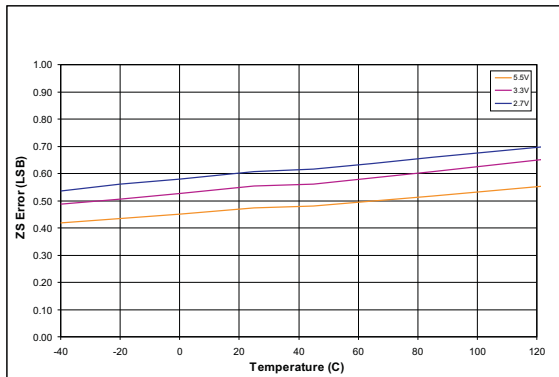


Figure 6.

**FULL SCALE ERROR vs
TEMPERATURE**

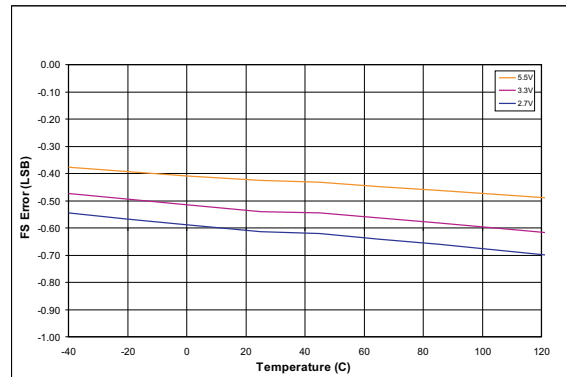


Figure 7.

TYPICAL CHARACTERISTICS (continued)

**END-TO-END RTOTAL% CHANGE vs
TEMPERATURE**

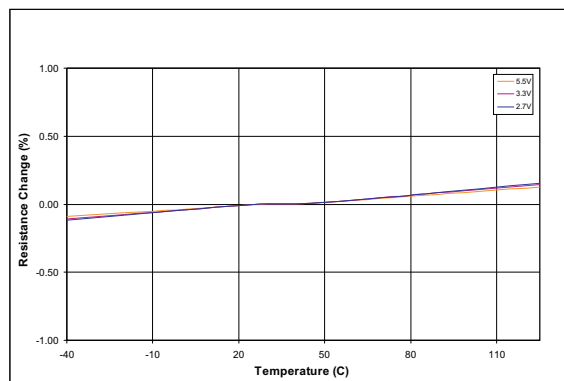


Figure 8.

**TEMPERATURE COEFFICIENT vs
TAP POSITION (Potentiometer Mode)**

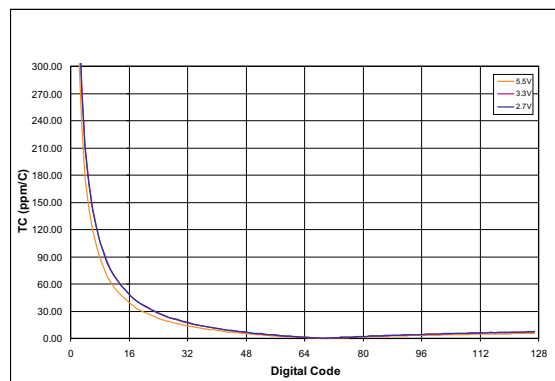


Figure 9.

**TEMPERATURE COEFFICIENT vs
TAP POSITION (Rheostat Mode)**

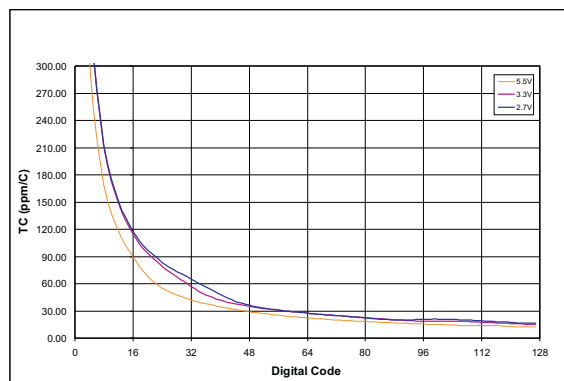


Figure 10.

FREQUENCY RESPONSE

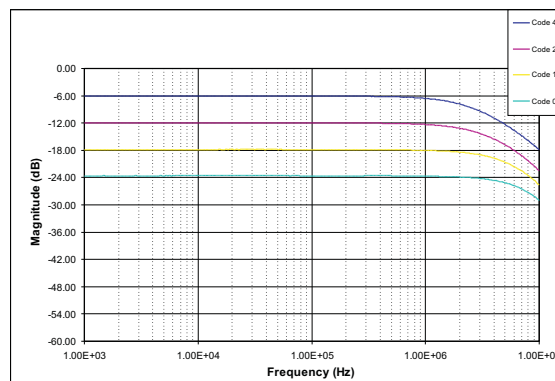


Figure 11.

SLAVE ADDRESS

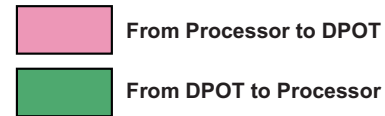
TPL0401A, TPL0401C

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|----------------|-------|-------|-------|-------|-------|-------|----------------|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | R/W |

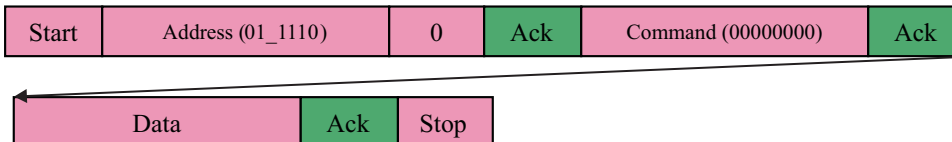
TPL0401B

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|----------------|-------|-------|-------|-------|-------|-------|----------------|
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | R/W |

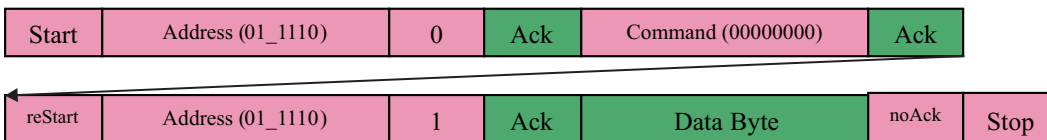
WRITE AND READ PROTOCOL



I²C Write to A Register



I²C Read From A Register



Standard I²C Interface Details

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by the master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 13). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse.

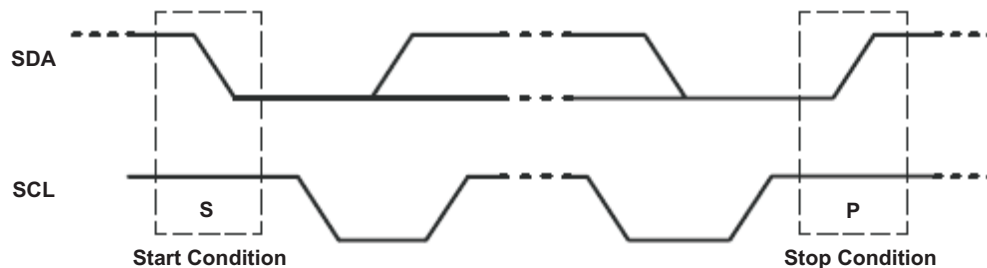


Figure 12. Definition of Start and Stop Conditions

The data byte follows the address ACK. The R/W bit is kept low for transfer from the master to the slave. The data byte is followed by an ACK sent from this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time (tpv) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see Figure 13).

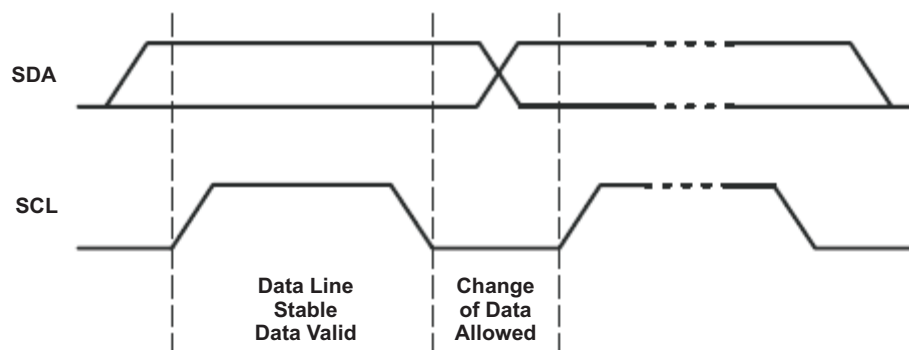


Figure 13. Bit Transfer

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 13).

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 14). Setup and hold times must be taken into account.

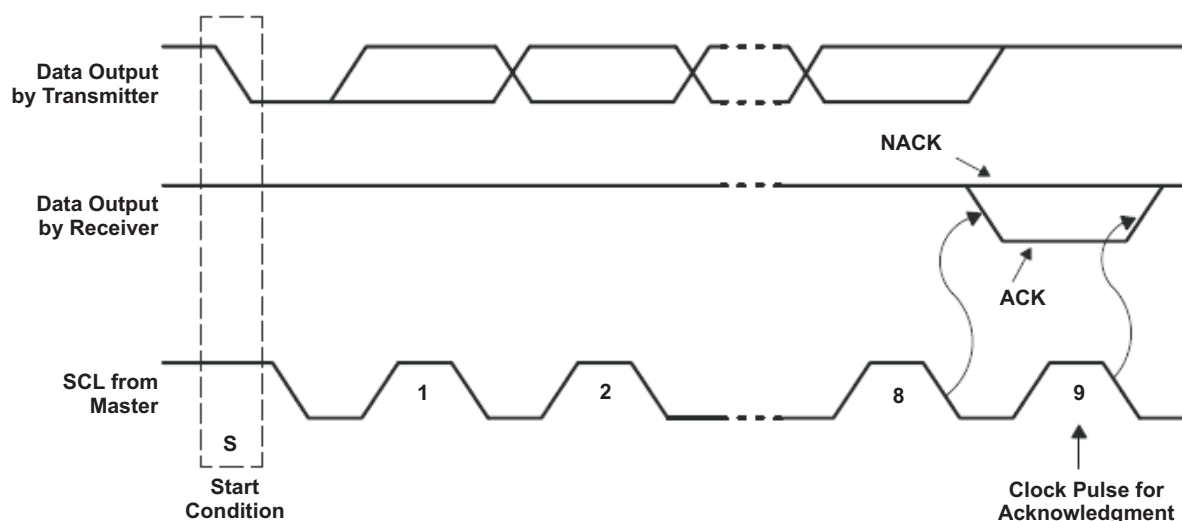


Figure 14. Acknowledgement on the I²C Bus

TYPICAL APPLICATION

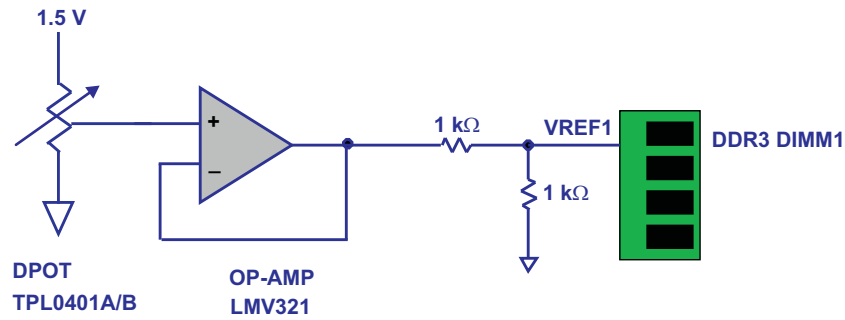


Figure 15. DDR3 Voltage Reference Adjustment

Below table shows Ideal values of resistance for a 10kΩ DPOT. The absolute values can vary significantly, but the ratio (Rh_w/R_{wl}) is extremely accurate.

Table 1. Resistance Values Table

| Step | Binary | R _{wl} (kΩ) | R _{hw} (kΩ) | R _{hw} /R _{wl} |
|------|--------|----------------------|----------------------|----------------------------------|
| 0 | 0 | 0.00 | 10.00 | 0.00 |
| 1 | 1 | 0.08 | 9.92 | 0.01 |
| 2 | 10 | 0.16 | 9.84 | 0.02 |
| 3 | 11 | 0.23 | 9.77 | 0.02 |
| 4 | 100 | 0.31 | 9.69 | 0.03 |
| 5 | 101 | 0.39 | 9.61 | 0.04 |
| 6 | 110 | 0.47 | 9.53 | 0.05 |
| 7 | 111 | 0.55 | 9.45 | 0.06 |
| 8 | 1000 | 0.63 | 9.38 | 0.07 |
| 9 | 1001 | 0.70 | 9.30 | 0.08 |
| 10 | 1010 | 0.78 | 9.22 | 0.08 |
| 11 | 1011 | 0.86 | 9.14 | 0.09 |
| 12 | 1100 | 0.94 | 9.06 | 0.10 |
| 13 | 1101 | 1.02 | 8.98 | 0.11 |
| 14 | 1110 | 1.09 | 8.91 | 0.12 |
| 15 | 1111 | 1.17 | 8.83 | 0.13 |
| 16 | 10000 | 1.25 | 8.75 | 0.14 |
| 17 | 10001 | 1.33 | 8.67 | 0.15 |
| 18 | 10010 | 1.41 | 8.59 | 0.16 |
| 19 | 10011 | 1.48 | 8.52 | 0.17 |
| 20 | 10100 | 1.56 | 8.44 | 0.19 |
| 21 | 10101 | 1.64 | 8.36 | 0.20 |
| 22 | 10110 | 1.72 | 8.28 | 0.21 |
| 23 | 10111 | 1.80 | 8.20 | 0.22 |
| 24 | 11000 | 1.88 | 8.13 | 0.23 |
| 25 | 11001 | 1.95 | 8.05 | 0.24 |
| 26 | 11010 | 2.03 | 7.97 | 0.25 |
| 27 | 11011 | 2.11 | 7.89 | 0.27 |
| 28 | 11100 | 2.19 | 7.81 | 0.28 |
| 29 | 11101 | 2.27 | 7.73 | 0.29 |
| 30 | 11110 | 2.34 | 7.66 | 0.31 |
| 31 | 11111 | 2.42 | 7.58 | 0.32 |

Table 1. Resistance Values Table (continued)

| Step | Binary | Rwl (kΩ) | Rhw (kΩ) | Rhw/Rwl |
|------|---------|----------|----------|---------|
| 32 | 100000 | 2.50 | 7.50 | 0.33 |
| 33 | 100001 | 2.58 | 7.42 | 0.35 |
| 34 | 100010 | 2.66 | 7.34 | 0.36 |
| 35 | 100011 | 2.73 | 7.27 | 0.38 |
| 36 | 100100 | 2.81 | 7.19 | 0.39 |
| 37 | 100101 | 2.89 | 7.11 | 0.41 |
| 38 | 100110 | 2.97 | 7.03 | 0.42 |
| 39 | 100111 | 3.05 | 6.95 | 0.44 |
| 40 | 101000 | 3.13 | 6.88 | 0.45 |
| 41 | 101001 | 3.20 | 6.80 | 0.47 |
| 42 | 101010 | 3.28 | 6.72 | 0.49 |
| 43 | 101011 | 3.36 | 6.64 | 0.51 |
| 44 | 101100 | 3.44 | 6.56 | 0.52 |
| 45 | 101101 | 3.52 | 6.48 | 0.54 |
| 46 | 101110 | 3.59 | 6.41 | 0.56 |
| 47 | 101111 | 3.67 | 6.33 | 0.58 |
| 48 | 110000 | 3.75 | 6.25 | 0.60 |
| 49 | 110001 | 3.83 | 6.17 | 0.62 |
| 50 | 110010 | 3.91 | 6.09 | 0.64 |
| 51 | 110011 | 3.98 | 6.02 | 0.66 |
| 52 | 110100 | 4.06 | 5.94 | 0.68 |
| 53 | 110101 | 4.14 | 5.86 | 0.71 |
| 54 | 110110 | 4.22 | 5.78 | 0.73 |
| 55 | 110111 | 4.30 | 5.70 | 0.75 |
| 56 | 111000 | 4.38 | 5.63 | 0.78 |
| 57 | 111001 | 4.45 | 5.55 | 0.80 |
| 58 | 111010 | 4.53 | 5.47 | 0.83 |
| 59 | 111011 | 4.61 | 5.39 | 0.86 |
| 60 | 111100 | 4.69 | 5.31 | 0.88 |
| 61 | 111101 | 4.77 | 5.23 | 0.91 |
| 62 | 111110 | 4.84 | 5.16 | 0.94 |
| 63 | 111111 | 4.92 | 5.08 | 0.97 |
| 64 | 1000000 | 5.00 | 5.00 | 1.00 |
| 65 | 1000001 | 5.08 | 4.92 | 1.03 |
| 66 | 1000010 | 5.16 | 4.84 | 1.06 |
| 67 | 1000011 | 5.23 | 4.77 | 1.10 |
| 68 | 1000100 | 5.31 | 4.69 | 1.13 |
| 69 | 1000101 | 5.39 | 4.61 | 1.17 |
| 70 | 1000110 | 5.47 | 4.53 | 1.21 |
| 71 | 1000111 | 5.55 | 4.45 | 1.25 |
| 72 | 1001000 | 5.63 | 4.38 | 1.29 |
| 73 | 1001001 | 5.70 | 4.30 | 1.33 |
| 74 | 1001010 | 5.78 | 4.22 | 1.37 |
| 75 | 1001011 | 5.86 | 4.14 | 1.42 |
| 76 | 1001100 | 5.94 | 4.06 | 1.46 |
| 77 | 1001101 | 6.02 | 3.98 | 1.51 |
| 78 | 1001110 | 6.09 | 3.91 | 1.56 |

Table 1. Resistance Values Table (continued)

| Step | Binary | Rwl (kΩ) | Rhw (kΩ) | Rhw/Rwl |
|------|---------|----------|----------|---------|
| 79 | 1001111 | 6.17 | 3.83 | 1.61 |
| 80 | 1010000 | 6.25 | 3.75 | 1.67 |
| 81 | 1010001 | 6.33 | 3.67 | 1.72 |
| 82 | 1010010 | 6.41 | 3.59 | 1.78 |
| 83 | 1010011 | 6.48 | 3.52 | 1.84 |
| 84 | 1010100 | 6.56 | 3.44 | 1.91 |
| 85 | 1010101 | 6.64 | 3.36 | 1.98 |
| 86 | 1010110 | 6.72 | 3.28 | 2.05 |
| 87 | 1010111 | 6.80 | 3.20 | 2.12 |
| 88 | 1011000 | 6.88 | 3.13 | 2.20 |
| 89 | 1011001 | 6.95 | 3.05 | 2.28 |
| 90 | 1011010 | 7.03 | 2.97 | 2.37 |
| 91 | 1011011 | 7.11 | 2.89 | 2.46 |
| 92 | 1011100 | 7.19 | 2.81 | 2.56 |
| 93 | 1011101 | 7.27 | 2.73 | 2.66 |
| 94 | 1011110 | 7.34 | 2.66 | 2.76 |
| 95 | 1011111 | 7.42 | 2.58 | 2.88 |
| 96 | 1100000 | 7.50 | 2.50 | 3.00 |
| 97 | 1100001 | 7.58 | 2.42 | 3.13 |
| 98 | 1100010 | 7.66 | 2.34 | 3.27 |
| 99 | 1100011 | 7.73 | 2.27 | 3.41 |
| 100 | 1100100 | 7.81 | 2.19 | 3.57 |
| 101 | 1100101 | 7.89 | 2.11 | 3.74 |
| 102 | 1100110 | 7.97 | 2.03 | 3.92 |
| 103 | 1100111 | 8.05 | 1.95 | 4.12 |
| 104 | 1101000 | 8.13 | 1.88 | 4.33 |
| 105 | 1101001 | 8.20 | 1.80 | 4.57 |
| 106 | 1101010 | 8.28 | 1.72 | 4.82 |
| 107 | 1101011 | 8.36 | 1.64 | 5.10 |
| 108 | 1101100 | 8.44 | 1.56 | 5.40 |
| 109 | 1101101 | 8.52 | 1.48 | 5.74 |
| 110 | 1101110 | 8.59 | 1.41 | 6.11 |
| 111 | 1101111 | 8.67 | 1.33 | 6.53 |
| 112 | 1110000 | 8.75 | 1.25 | 7.00 |
| 113 | 1110001 | 8.83 | 1.17 | 7.53 |
| 114 | 1110010 | 8.91 | 1.09 | 8.14 |
| 115 | 1110011 | 8.98 | 1.02 | 8.85 |
| 116 | 1110100 | 9.06 | 0.94 | 9.67 |
| 117 | 1110101 | 9.14 | 0.86 | 10.64 |
| 118 | 1110110 | 9.22 | 0.78 | 11.80 |
| 119 | 1110111 | 9.30 | 0.70 | 13.22 |
| 120 | 1111000 | 9.38 | 0.63 | 15.00 |
| 121 | 1111001 | 9.45 | 0.55 | 17.29 |
| 122 | 1111010 | 9.53 | 0.47 | 20.33 |
| 123 | 1111011 | 9.61 | 0.39 | 24.60 |
| 124 | 1111100 | 9.69 | 0.31 | 31.00 |
| 125 | 1111101 | 9.77 | 0.23 | 41.67 |

Table 1. Resistance Values Table (continued)

| Step | Binary | Rwl (k Ω) | Rhw (k Ω) | Rhw/Rwl |
|------|---------|-------------------|-------------------|---------|
| 126 | 1111110 | 9.84 | 0.16 | 63.00 |
| 127 | 1111111 | 9.92 | 0.08 | 127.00 |

Changes from Original (September 2011) to Revision A**Page**

| | |
|---|-------------------|
| • Added TPL0401C device to the Datasheet. | 1 |
| • Added TPL0401C Package. | 1 |
| • Added TPL0401C Functional Block Diagram. | 2 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPL0401A-10DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (7TD ~ 7TV) | Samples |
| TPL0401B-10DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (7UD ~ 7UV) | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

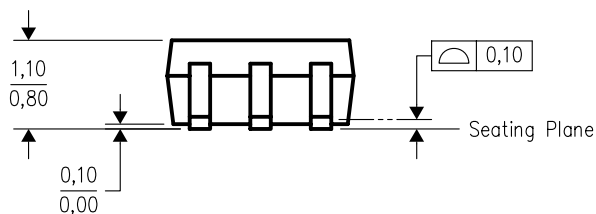
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPL0401A-10DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |
| TPL0401B-10DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.41 | 2.41 | 1.2 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS



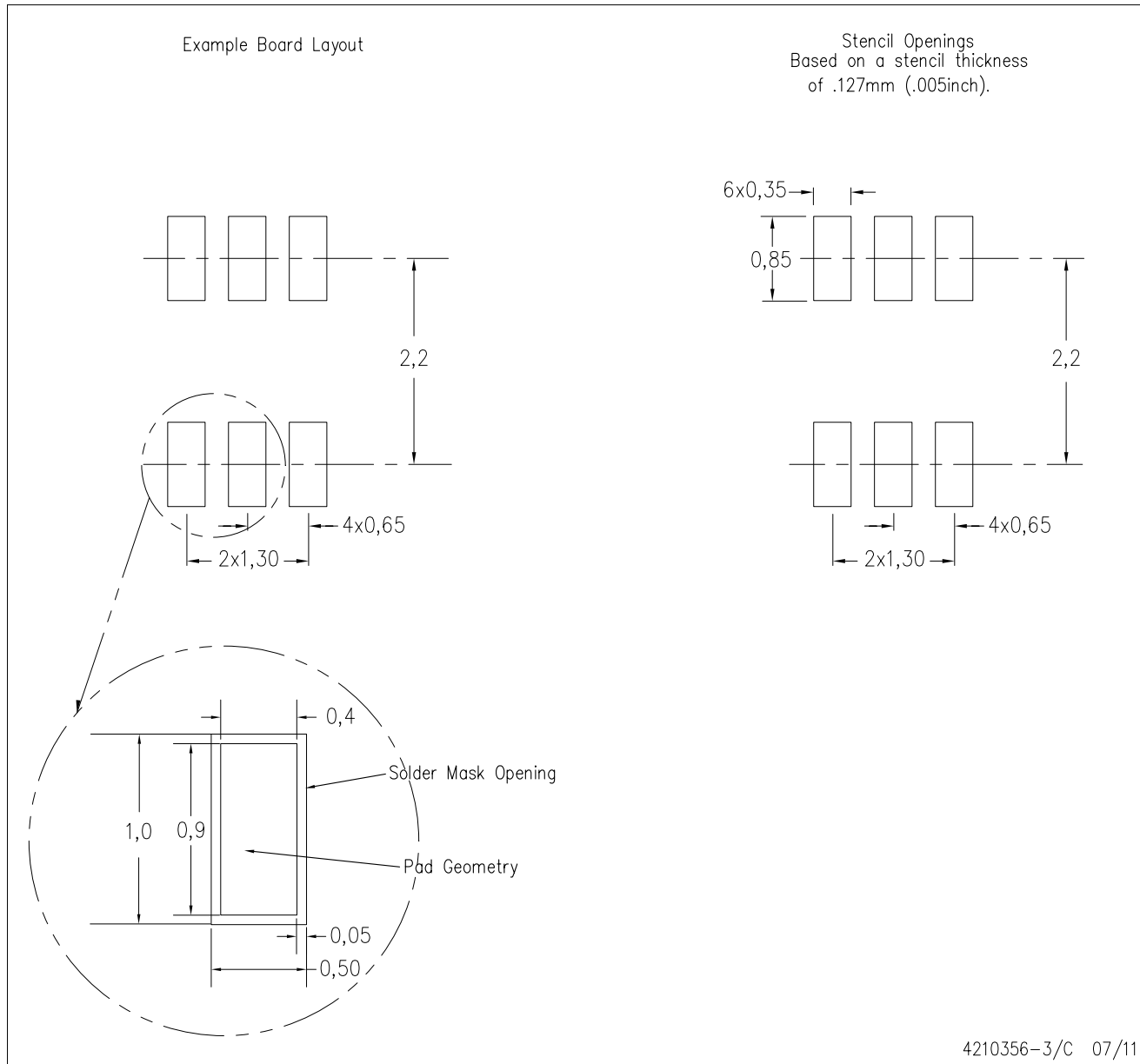
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPL0401A-10DCKR | SC70 | DCK | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| TPL0401B-10DCKR | SC70 | DCK | 6 | 3000 | 202.0 | 201.0 | 28.0 |



DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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