



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Mar.23.2006
Rev. 1.1	Revised $V_{IL} = 0.6V \Rightarrow 0.8V$	Jun.09.2006
Rev. 1.2	Revised <u>PACKAGE OUTLINE DIMENSION</u> (TSOP II)	Apr.12.2007
Rev. 2.0	Added LL Spec. Revised TEST CONDITION of I_{SB1}/I_{DR} Added -12ns Spec. Revised I_{CC} and I_{SB1} Added I grade	Jun.25.2007
Rev. 2.1	Revised <u>ABSOLUTE MAXIMUN RATINGS</u> Revised TEST CONDITION of I_{CC} Revised <u>FEATURES & ORDERING INFORMATION</u> Lead free and green package available to Green package available Deleted T_{SOLDER} in <u>ABSOLUTE MAXIMUN RATINGS</u> Added packing type in <u>ORDERING INFORMATION</u>	Apr.17.2009
Rev. 2.2	Added package type TFBGA	May.06.2010
Rev. 2.3	Revised <u>ORDERING INFORMATION</u> in page 12	Aug.30.2010
Rev. 2.4	Revised -12ns spec as -10ns spec and related parameter	July.03.2013
Rev. 2.5	Revised <u>ORDERING INFORMATION</u> in page 11 Correct <u>ORDERING INFORMATION</u> Typo. Added power type in <u>ORDERING INFORMATION</u>	May.20.2016
Rev. 2.6	Added -12ns Spec. Revised I_{SB1} & I_{CC} Revised <u>PIN DESCRIPTION</u> in page 2 Deleted -25ns Spec. Deleted Package Type: 48-ball 6mm x 8mm TFBGA Deleted WRITE CYCLE Notes : 1. WE#,CE#, LB#, UB# must be high during all address transitions. In page 9	Dec.27.2016

FEATURES

- Fast access time : 10/12/15/20ns
- Low power consumption:
Operating current : 120/80/100/80mA(TYP.)
Standby current :
3.5mA (TYP. for 10/12ns)
0.1mA (TYP. for 15/20ns)
20μA (TYP. for 15/20ns LL version)
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
UB# (DQ8 ~ DQ15)
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 44-pin 400mil TSOP II

GENERAL DESCRIPTION

The LY6125616 is a 4,194,304-bit low power CMOS static random access memory organized as 262,144 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

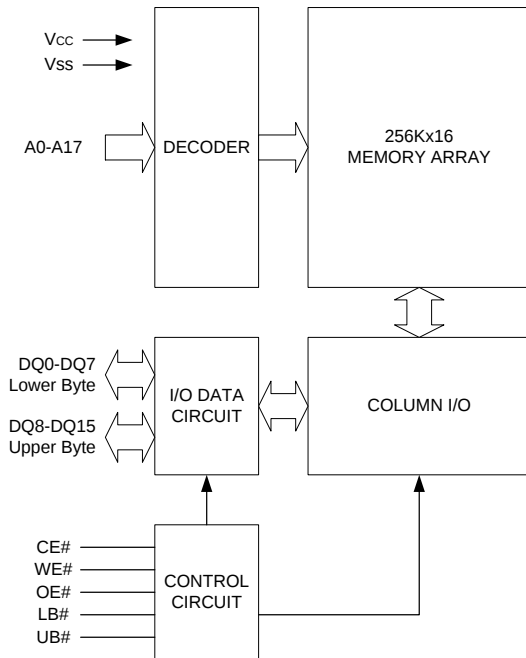
The LY6125616 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY6125616 operates from a single power supply of 5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	V _{CC} Range	Speed	Power Dissipation	
				Standby(I _{SB1} , TYP.)	Operating(I _{CC} , TYP.)
LY6125616	0 ~ 70°C	4.5 ~ 5.5V	10/12ns	3.5mA	120/80mA
LY6125616(I)	-40 ~ 85°C	4.5 ~ 5.5V	10/12ns	3.5mA	120/80mA
LY6125616	0 ~ 70°C	4.5 ~ 5.5V	15/20ns	0.1mA	100/80mA
LY6125616(E)	-20 ~ 80°C	4.5 ~ 5.5V	15/20ns	0.1mA	100/80mA
LY6125616(I)	-40 ~ 85°C	4.5 ~ 5.5V	15/20ns	0.1mA	100/80mA
LY6125616(LL)	0 ~ 70°C	4.5 ~ 5.5V	15/20ns	20μA(LL)	100/80mA
LY6125616(LLI)	-40 ~ 85°C	4.5 ~ 5.5V	15/20ns	20μA(LL)	100/80mA

FUNCTIONAL BLOCK DIAGRAM

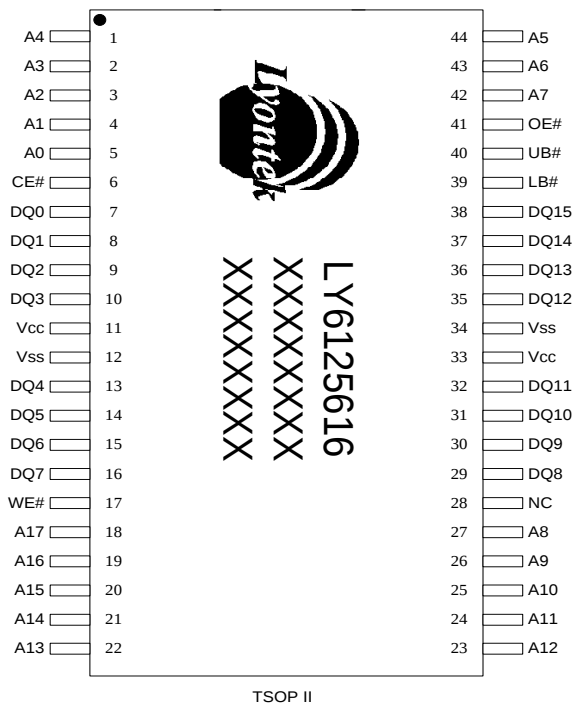


PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
DQ0 - DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vcc	Power Supply
Vss	Ground
NC	No Connection



PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0 - DQ7	DQ8 - DQ15	
Standby	H	X	X	X	X	High-Z	High-Z	I _{SB1}
Output Disable	L	H	H	X	X	High-Z	High-Z	I _{CC}
	L	X	X	H	H	High-Z	High-Z	
Read	L	L	H	L	H	D _{OUT}	High-Z	I _{CC}
	L	L	H	H	L	High-Z	D _{OUT}	
	L	L	H	L	L	D _{OUT}	D _{OUT}	
Write	L	X	L	L	H	D _{IN}	High-Z	I _{CC}
	L	X	L	H	L	High-Z	D _{IN}	
	L	X	L	L	L	D _{IN}	D _{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. *4	MAX.	UNIT
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input High Voltage	V_{IH}^{*1}		2.2	-	$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}^{*2}		- 0.3	-	0.8	V
Input Leakage Current	I_{LI}	$V_{CC} \geq V_{IN} \geq V_{SS}$	- 1	-	1	μA
Output Leakage Current	I_{LO}	$V_{CC} \geq V_{OUT} \geq V_{SS}$, Output Disabled	- 1	-	1	μA
Output High Voltage	V_{OH}	$I_{OH} = -4mA$	2.4	-	-	V
Output Low Voltage	V_{OL}	$I_{OL} = 8mA$	-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = MIN. $CE\# = V_{IL}$, $I_{I/O} = 0mA$ Others at V_{IL} or V_{IH}	10	-	120	mA
			12	-	80	mA
			15	-	100	mA
			20	-	80	mA
Standby Power Supply Current	I_{SB1}	$CE\# \geq V_{CC} - 0.2V$ Others at $0.2V / V_{CC}-0.2V$	10/12	-	3.5	mA
			15/20	-	0.1	3^{*5} mA
			15/20LL	-	20	100^{*6} μA

Notes:

- $V_{IH}(\max) = V_{CC} + 2.0V$ for pulse width less than 6ns.
- $V_{IL}(\min) = V_{SS} - 2.0V$ for pulse width less than 6ns.
- Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- Typical values are included for reference only and are not guaranteed or tested.
Typical valued are measured at $V_{CC} = V_{CC}(\text{TYP.})$ and $T_A = 25^\circ C$
- 1mA for special request
- 50 μA for special request

CAPACITANCE ($T_A = 25^\circ C$, $f = 1.0MHz$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL$, $I_{OH}/I_{OL} = -8mA/16mA$



AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY6125616-10		LY6125616-12		LY6125616-15		LY6125616-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	10	-	12	-	15	-	20	-	ns
Address Access Time	t _{AA}	-	10	-	12	-	15	-	20	ns
Chip Enable Access Time	t _{ACE}	-	10	-	12	-	15	-	20	ns
Output Enable Access Time	t _{OE}	-	5	-	6	-	7	-	8	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	2	-	3	-	4	-	4	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	5	-	6	-	7	-	8	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	5	-	6	-	7	-	8	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	3	-	3	-	ns
LB#, UB# Access Time	t _{BA}	-	5	-	6	-	7	-	8	ns
LB#, UB# to High-Z Output	t _{BHZ} *	-	5	-	6	-	7	-	8	ns
LB#, UB# to Low-Z Output	t _{BLZ} *	2	-	3	-	4	-	4	-	ns

(2) WRITE CYCLE

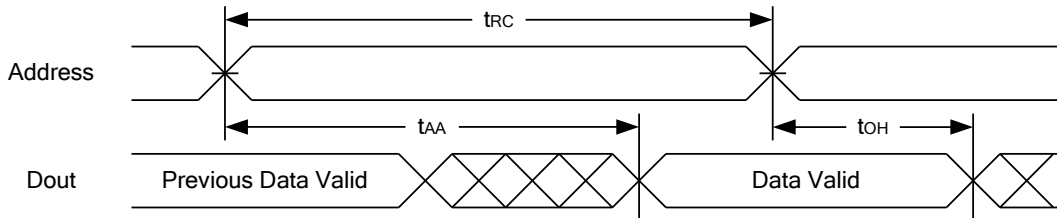
PARAMETER	SYM.	LY6125616-10		LY6125616-12		LY6125616-15		LY6125616-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	10	-	12	-	15	-	20	-	ns
Address Valid to End of Write	t _{AW}	8	-	10	-	12	-	16	-	ns
Chip Enable to End of Write	t _{CW}	8	-	10	-	12	-	16	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	8	-	9	-	10	-	11	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	6	-	7	-	8	-	9	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	2	-	3	-	4	-	5	-	ns
Write to Output in High-Z	t _{WHZ} *	-	6	-	7	-	8	-	9	ns
LB#, UB# Valid to End of Write	t _{EW}	8	-	10	-	12	-	16	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

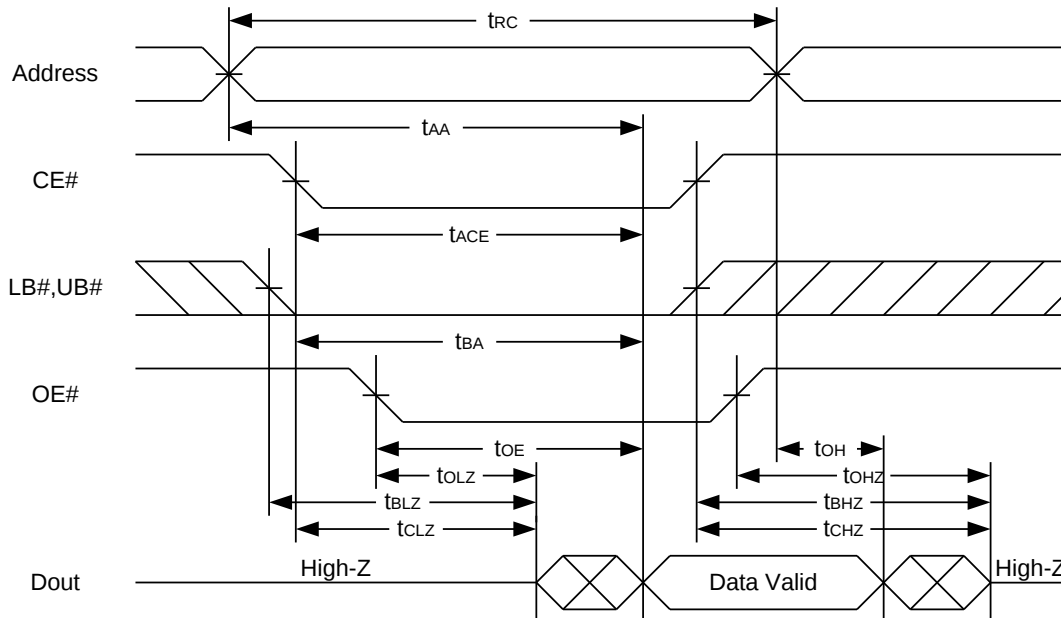


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

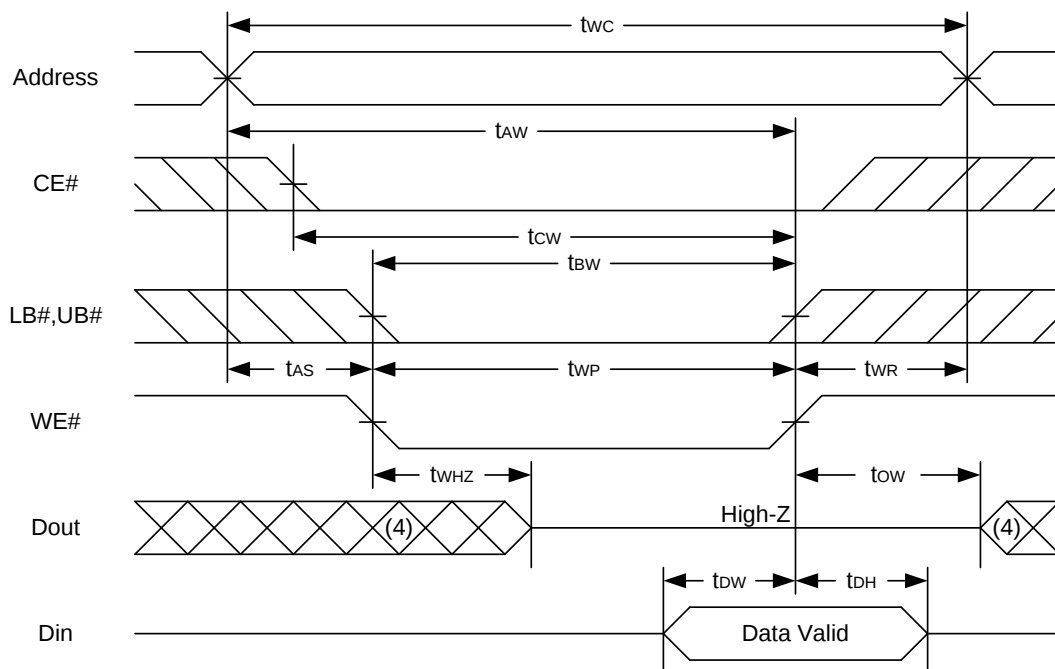


Notes :

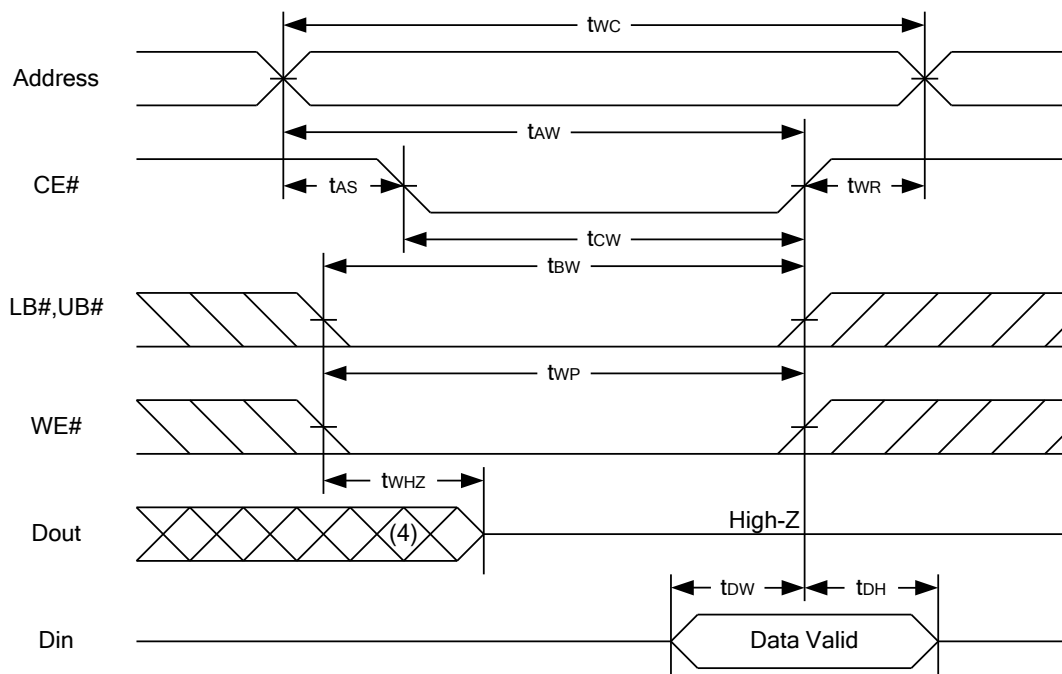
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)

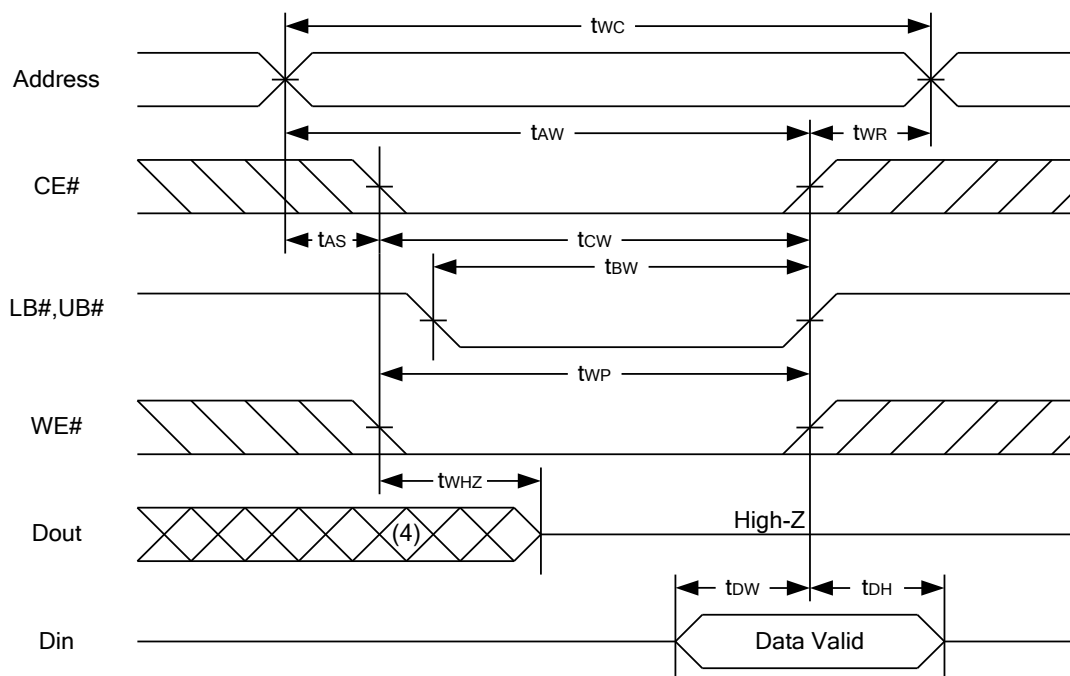


WRITE CYCLE 2 (CE# Controlled) (1,4,5)





WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



Notes :

- 1.A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
- 2.During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
- 3.During this period, I/O pins are in the output state, and input signals must not be applied.
- 4.If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

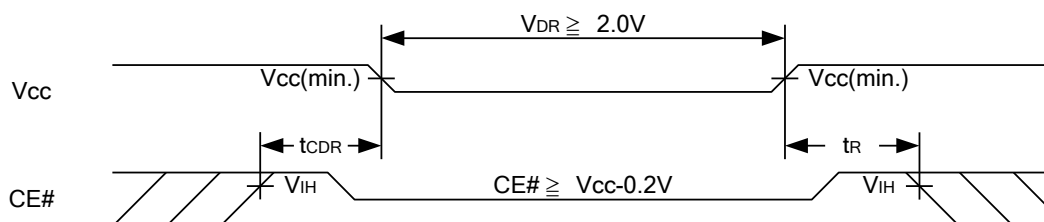


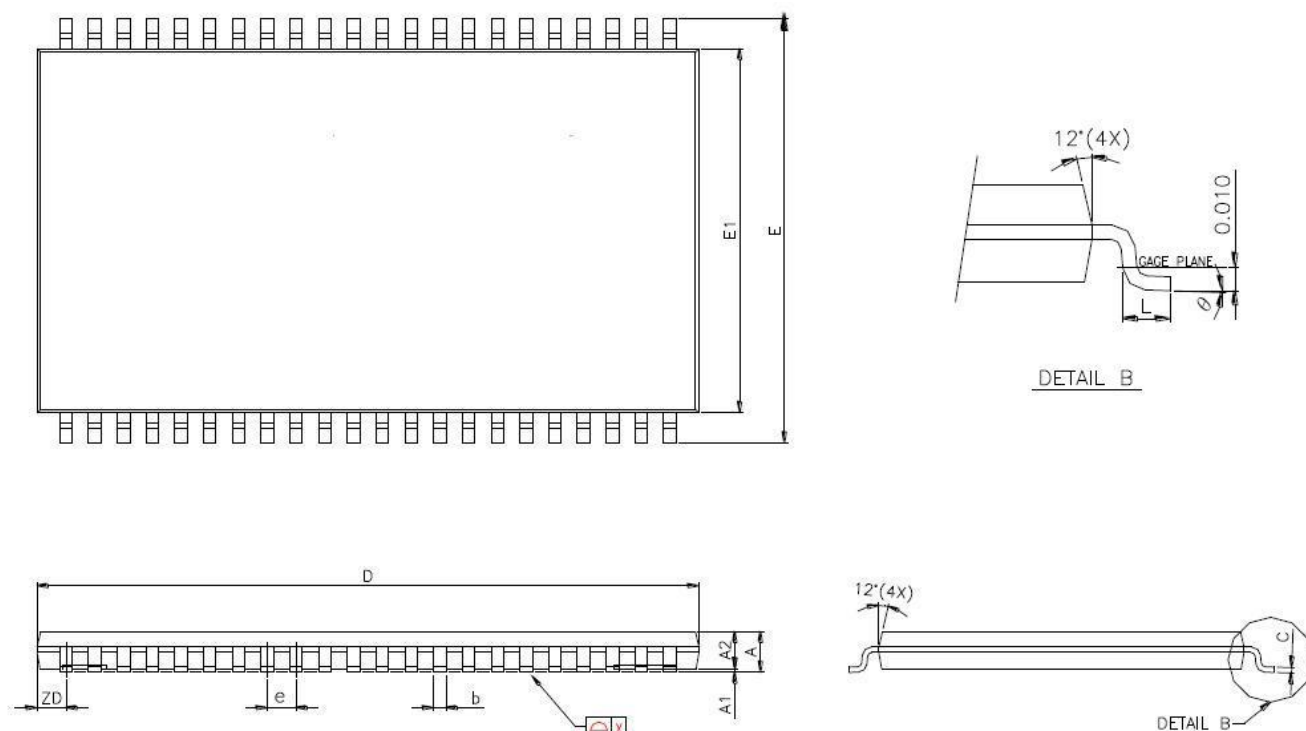
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# $\geq$ V _{CC} - 0.2V	2.0	-	5.5	V
Data Retention Current	I _{DR}	V _{CC} = 2.0V, CE# $\geq$ V _{CC} - 0.2V Other pins at 0.2V or V _{CC} -0.2V	10/12	-	-	10 mA
			15/20	-	0.05	2 mA
			15/20LL	-	10	50 μ A
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC} *	-	-	ns

t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM



PACKAGE OUTLINE DIMENSION
44-pin 400mil TSOP II Package Outline Dimension


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°

**ORDERING INFORMATION**

Package Type	Access Time (Speed)(ns)	Power Type	Temperature Range(°C)	Packing Type	Lyontek Item No.
44-pin (400mil) TSOP II	10	Normal Power	0°C~70°C	Tray	LY6125616ML-10
				Tape Reel	LY6125616ML-10T
			-40°C~85°C	Tray	LY6125616ML-10I
				Tape Reel	LY6125616ML-10IT
	12	Normal Power	0°C~70°C	Tray	LY6125616ML-12
				Tape Reel	LY6125616ML-12T
			-40°C~85°C	Tray	LY6125616ML-12I
				Tape Reel	LY6125616ML-12IT
	15	Normal Power	0°C~70°C	Tray	LY6125616ML-15
				Tape Reel	LY6125616ML-15T
			-20°C~80°C	Tray	LY6125616ML-15E
				Tape Reel	LY6125616ML-15ET
			-40°C~85°C	Tray	LY6125616ML-15I
				Tape Reel	LY6125616ML-15IT
		Ultra Low Power	0°C~70°C	Tray	LY6125616ML-15LL
				Tape Reel	LY6125616ML-15LLT
			-40°C~85°C	Tray	LY6125616ML-15LLI
				Tape Reel	LY6125616ML-15LLIT
	20	Normal Power	0°C~70°C	Tray	LY6125616ML-20
				Tape Reel	LY6125616ML-20T
			-20°C~80°C	Tray	LY6125616ML-20E
				Tape Reel	LY6125616ML-20ET
			-40°C~85°C	Tray	LY6125616ML-20I
				Tape Reel	LY6125616ML-20IT
		Ultra Low Power	0°C~70°C	Tray	LY6125616ML-20LL
				Tape Reel	LY6125616ML-20LLT
			-40°C~85°C	Tray	LY6125616ML-20LLI
				Tape Reel	LY6125616ML-20LLIT



Lyontek Inc.

LY6125616

Rev. 2.6

5V 256K X 16 BIT HIGH SPEED CMOS SRAM

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