DLP® 0.45 WXGA DMD

Check for Samples: DLP4500

FEATURES

- **0.45-Inch (11.43 mm) Diagonal Micromirror Array**
  - **912 × 1140 Array of Aluminum, Micrometer-Sized Mirrors**
  - **7.6-µm Micromirror Pitch**
  - **±12° Micromirror Tilt Angle (Relative to Flat State)**
  - **Side Illumination for Optimized Efficiency**
  - **3-µs Micromirror Cross Over Time**
- **Highly Efficient in Visible Light (420 nm–700 nm):**
  - **Window Transmission 97% (Single Pass, Through Two Window Surfaces)**
  - **Micromirror Reflectivity 89.4%**
  - **Array Diffraction Efficiency 86%**
  - **Array Fill Factor 92%**
  - **Polarization Independent**
- **Up to WXGA Resolution (1280 x 800) Wide Aspect Ratio Display**
- **24-Bit, Double Data Rate (DDR) Input Data Bus**
- **80-MHz to 120-MHz Input Data Clock Rate**
- **Integrated Micromirror Driver Circuitry**
- **Supports –10 °C to 70 °C**
- **9.1 mm-x 20.7-mm Package Footprint**
  - **Available in package FQE (up to 200 Lumens)**
  - **Available in package FQD (up to 500 Lumens)**
- **Dedicated DLPC350 Controller for Reliable Operation**

APPLICATIONS

- **Machine Vision**
- **Industrial Inspection**
- **3D Scanning**
- **3D Optical Metrology**
- **Automated Fingerprint Identification**
- **Face Recognition**
- **Augmented Reality**
- **Interactive Display**
- **Information Overlay**
- **Spectroscopy**
- **Chemical Analyzers**
- **Medical Instruments**
- **Photo-Stimulation**
- **Virtual Gauges**

DESCRIPTION

The DLP4500 digital micromirror device (DMD) is a digitally controlled MOEMS (micro-opto-electromechanical system) spatial light modulator (SLM). When coupled to an appropriate optical system, the DLP4500 can be used to modulate the amplitude and/or direction of incoming light. The DLP4500 creates light patterns with speed, precision, and efficiency.

Architecturally, the DLP4500 is a latchable, electrical-in/optical-out semiconductor device. This architecture makes the DLP4500 well suited for use in applications such as 3D scanning or metrology with structured light, augmented reality, microscopy, medical instruments, and spectroscopy. The compact physical size of the DLP4500 is well-suited for portable equipment where small form factor and lower cost are important. The compact package compliments the small size of LEDs to enable highly efficient, robust light engines.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The DLP4500 is one of two devices in the DLP 0.45 WXGA chip set (see Figure 1). Proper function and reliable operation of the DLP4500 requires that it be used in conjunction with the DLPC350 controller. See the DLP 0.45 WXGA Chip-set data sheet (TI literature number DLPU009) for further details. Figure 2 shows a typical system application using the DLP 0.45-inch WXGA chip set.

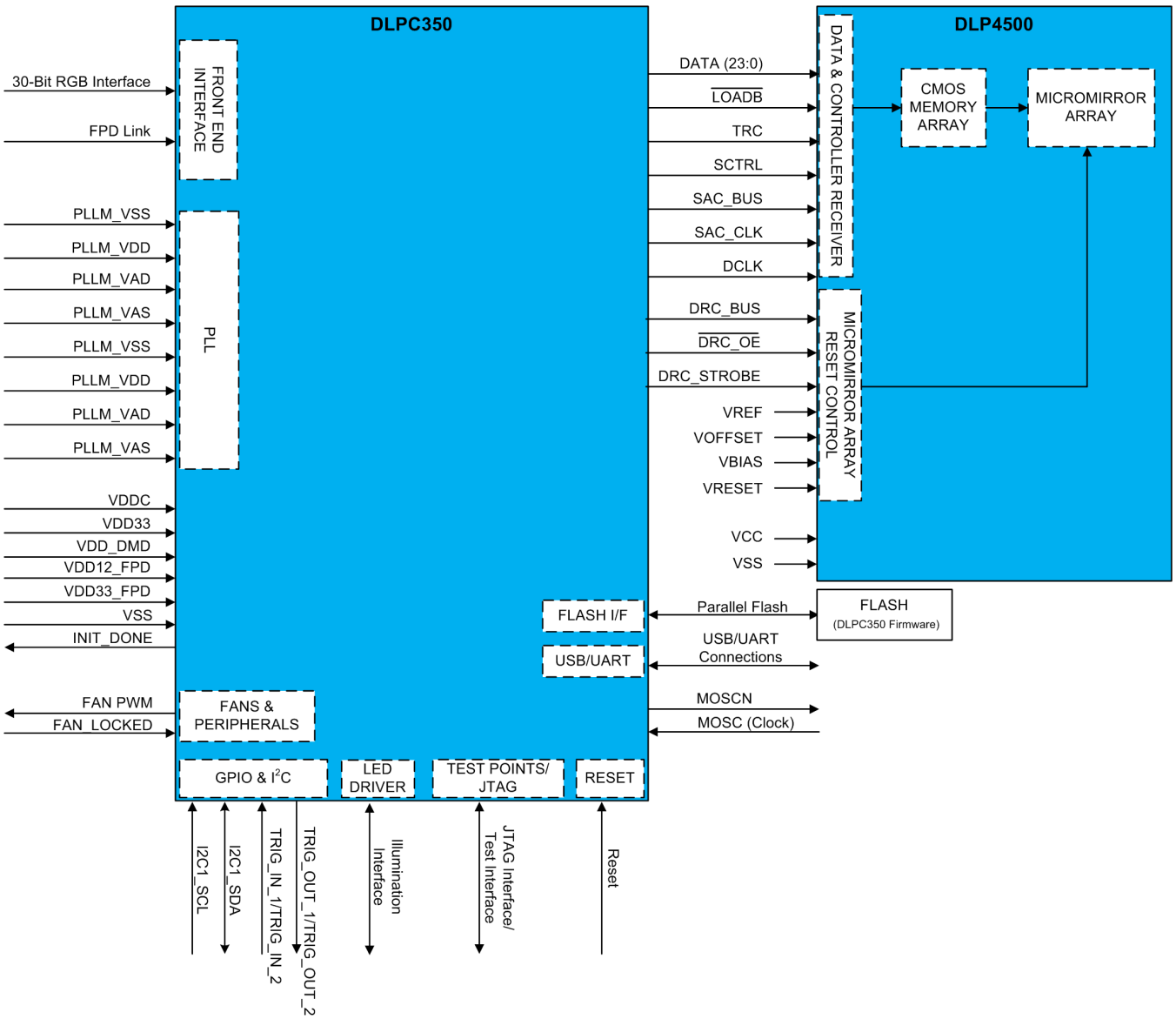

Figure 1. DLP 0.45 WXGA Chip Set

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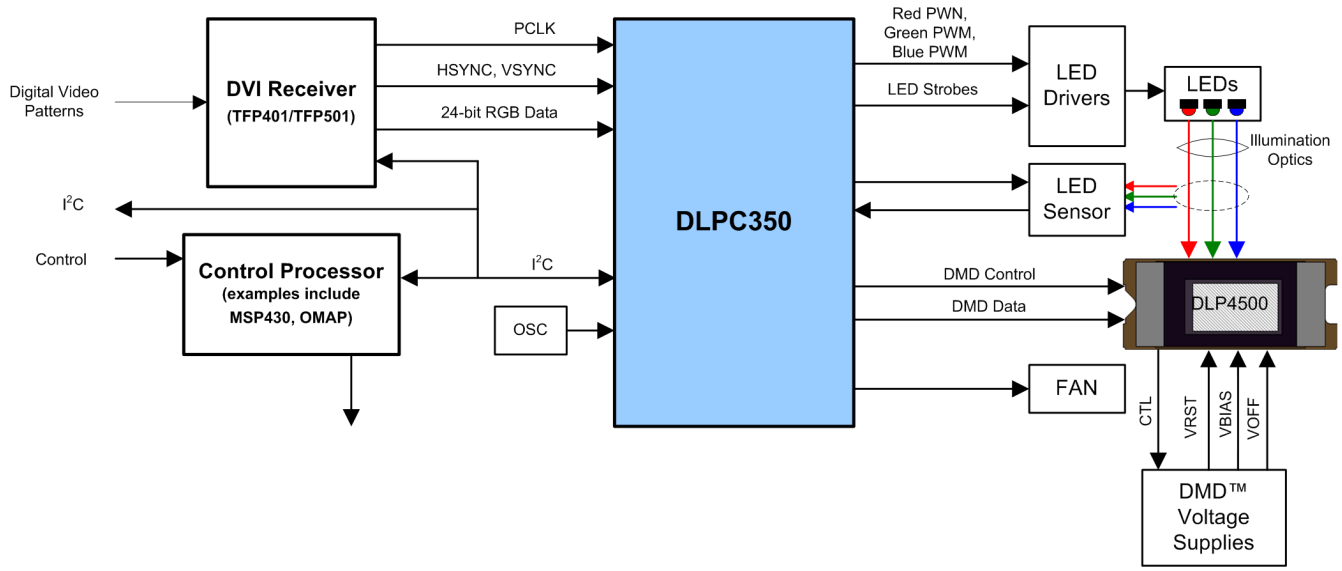

Figure 2. Typical Application

Electrically, the DLP4500 consists of a two-dimensional array of 1-bit CMOS memory cells, organized in a grid of 912 memory cell columns by 1140 memory cell rows. The CMOS memory array is addressed on column-by-column basis, over a 24-bit double data rate (DDR) bus. Addressing is handled via a serial control bus. The specific CMOS memory access protocol is handled by the DLPC350 digital controller.

Optically, the DLP4500 consists of 1,039,680 highly reflective, digitally switchable, micrometer-sized mirrors (micromirrors) organized in a two-dimensional array. The micromirror array consists of 912 micromirror columns by 1140 micromirror rows in diamond pixel configuration (Figure 3). Due to the diamond pixel configuration, the columns of each odd row are offset by half a pixel from the columns of the even row.

Each aluminum micromirror is approximately 7.6 microns in size (see *Micromirror Pitch* in Figure 3), and is switchable between two discrete angular positions: –12° and +12°. The angular positions α and β are measured relative to a 0° *flat reference when the mirrors are parked in their inactive state*, parallel to the array plane (see Figure 4). The parked position is not a latched position. Individual micromirror angular positions are relatively flat, but will vary. The tilt direction is perpendicular to the hinge-axis. The on-state landed position is directed toward the left side of the package (see Figure 3).

Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the mirror *clocking pulse* is applied. The angular position (–12° or +12°) of the individual micromirrors changes synchronously with a micromirror clocking pulse, rather than being coincident with the CMOS memory cell data update. Therefore, writing a logic 1 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a +12° position. Writing a logic 0 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a –12° position.

Updating the angular position of the micromirror array consists of two steps. First, updating the contents of the CMOS memory. Second, application of a mirror reset to all or a portion of the micromirror array (depending upon the configuration of the system). Mirror reset pulses are generated internally by the DLP4500 DMD, with application of the pulses being coordinated by the DLPC350 controller. See *Switching Characteristics* for timing specifications.

Around the perimeter of the 912 × 1140 array of micromirrors is a uniform band of *border* micromirrors. The border micromirrors are not user-addressable. The border micromirrors land in the –12° position once power has been applied to the device. There are 10 border micromirrors on each side of the 912 by 1140 active array.

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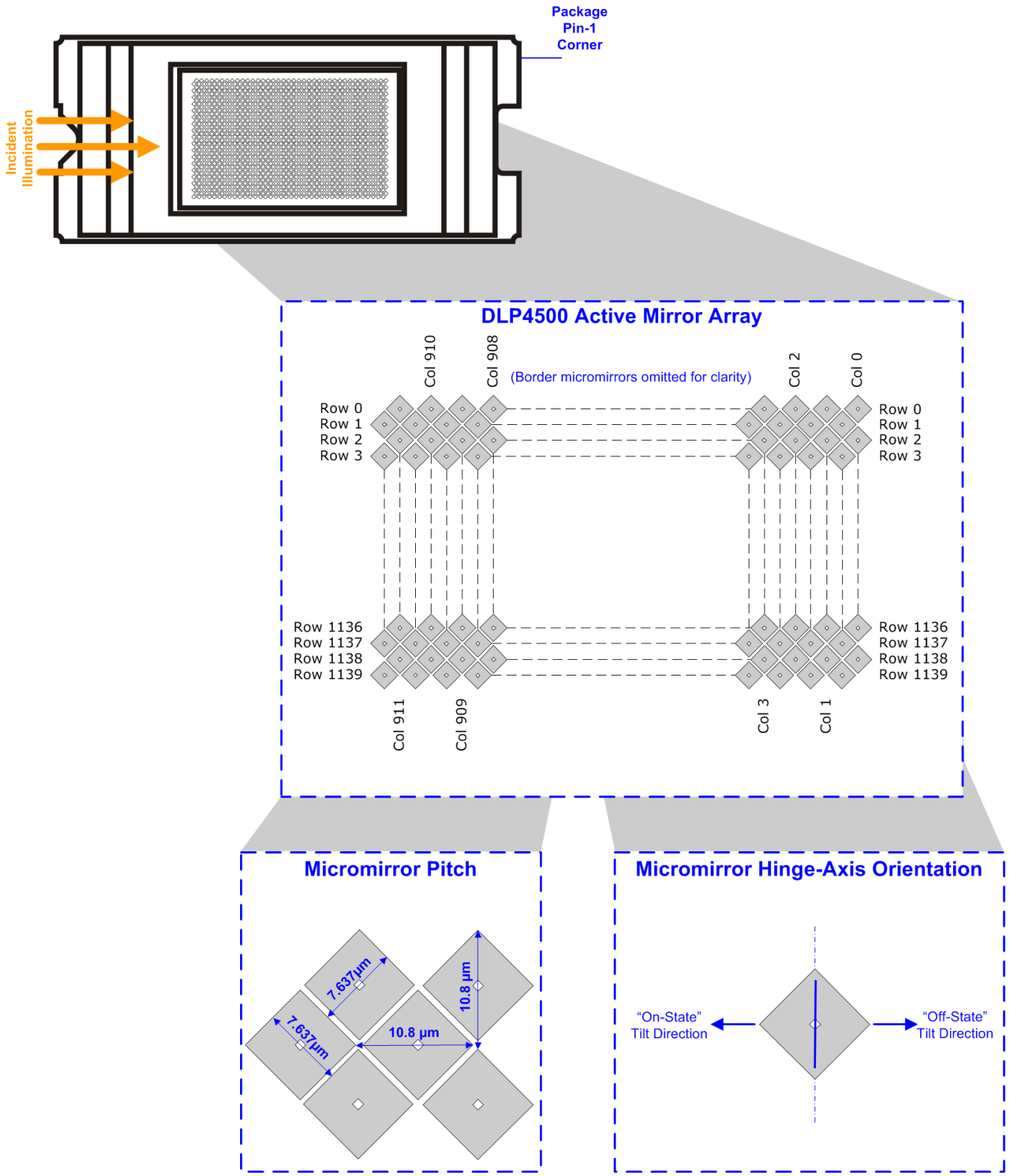

Figure 3. Micromirror Array, Pitch, and Hinge-Axis Orientation

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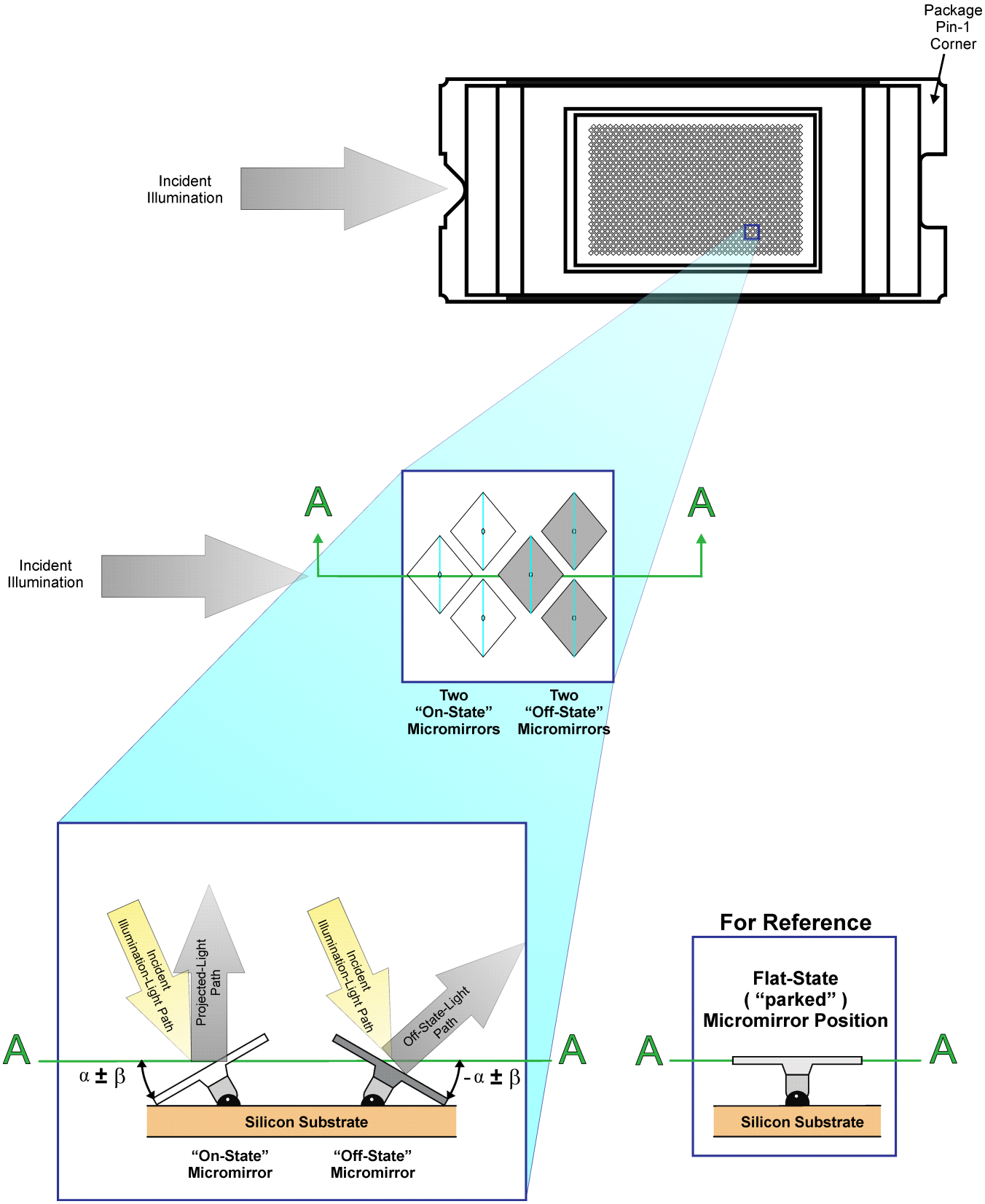

Figure 4. Micromirror Landed Positions and Light Paths

Related Documents

The following documents contain additional information related to the use of the DLP4500 device:

Table 1. Related Documents

DOCUMENT	TI LITERATURE NUMBER
DLP 0.45 WXGA Chip Set data sheet	DLPU009
DLPC350 Digital Controller data sheet	DLPS029
DLPC350 Software Programmer's Guide	DLPU010

Device Nomenclature

Figure 5 provides a legend for reading the complete device name for any DLP device.

Table 2. Package-Specific Information

PACKAGE TYPE	ALTERNATE NAME	MAXIMUM LUMENS	CONNECTOR
FQE	s241	200	Panasonic AXT580124
FQD	s310	500	Neoconix FBX0040CMFF6AU00

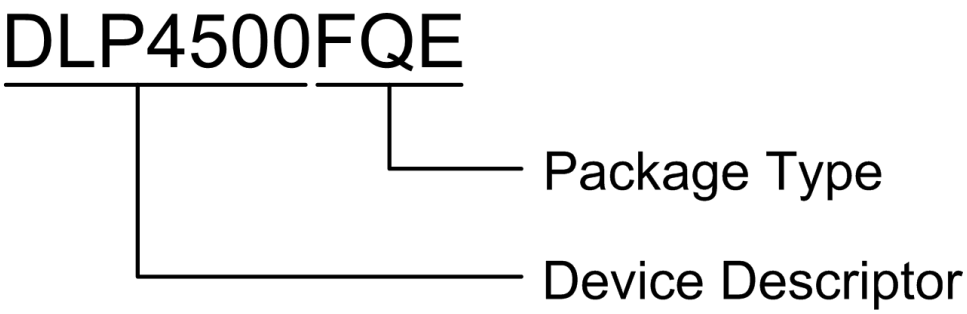

Figure 5. Device Nomenclature

Device Markings

The device marking consists of the fields shown in Figure 6.

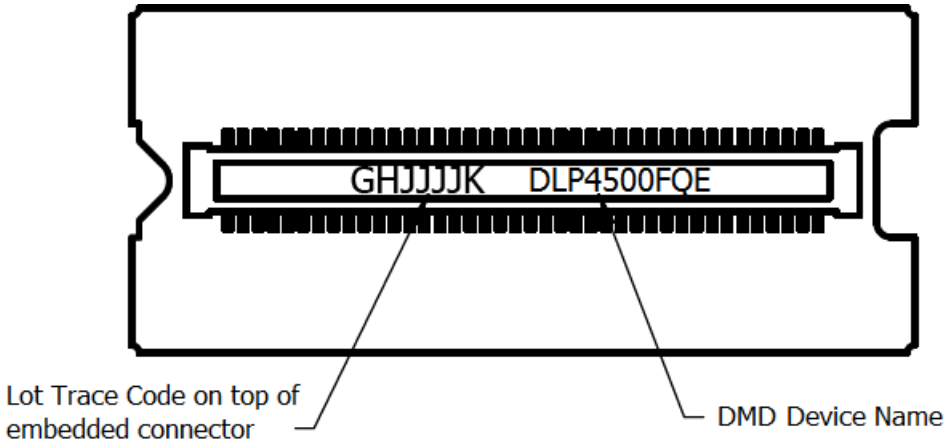

Figure 6. Device Marking for FQE

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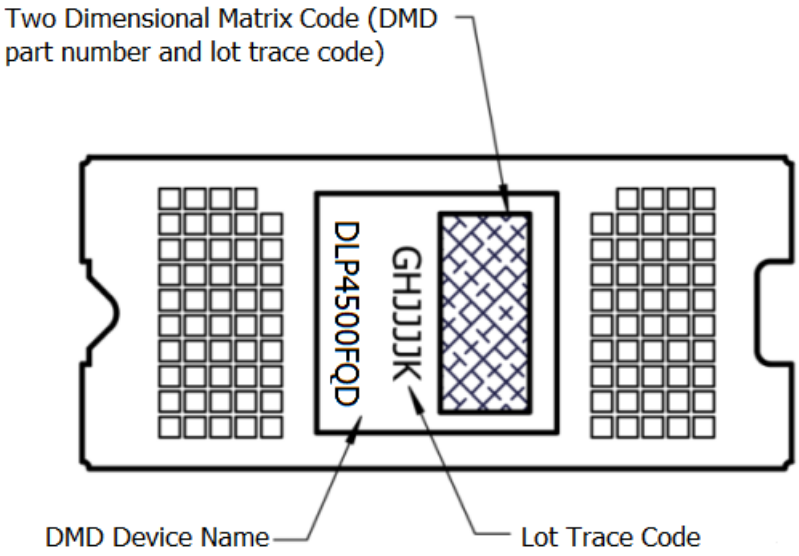

Figure 7. Device Marking for FQD

Device Terminals

This section describes the input/output characteristics of signals that interface to the DLP4500, organized by functional groups. Table 3 includes I/O, Type, Internal Termination, Clock Domain, and Data Rate characteristics which are further described in subsequent sections.

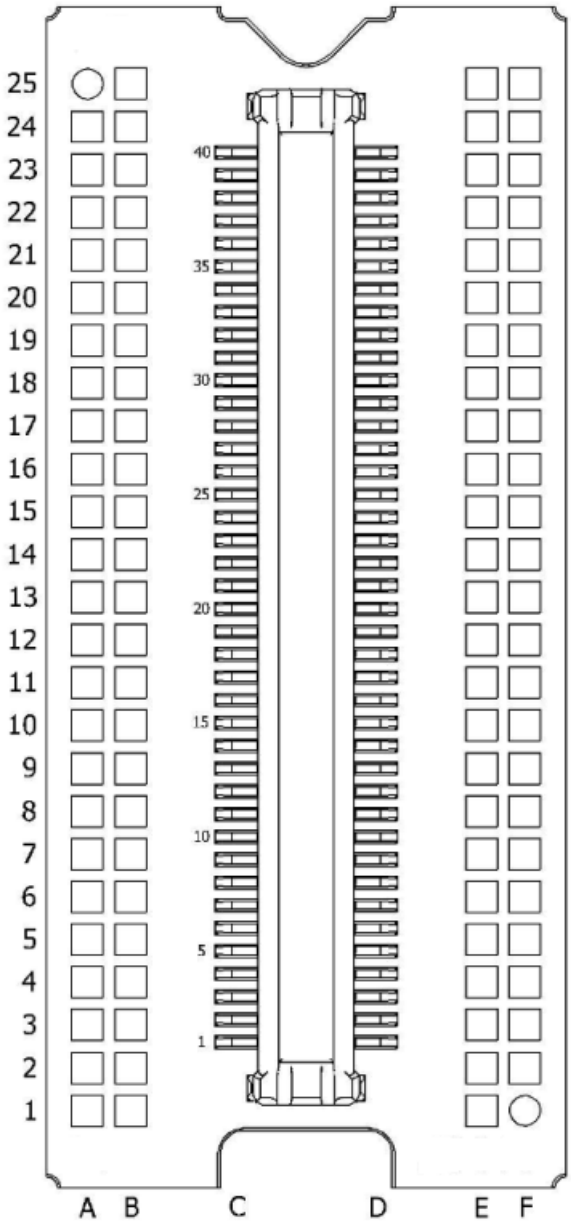

Figure 8. Package Connector Signal Names (Device Bottom View) for FQE

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Table 3. Connector Pins for FQE

TERMINAL NAME	CONNECTOR PINS	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	DATA RATE	DESCRIPTION
Data Inputs							
DATA(0)	C12	Input	LVCMOS	None	DCLK	DDR	Input data bus
DATA(1)	C10	Input	LVCMOS	None	DCLK	DDR	
DATA(2)	C9	Input	LVCMOS	None	DCLK	DDR	
DATA(3)	C7	Input	LVCMOS	None	DCLK	DDR	
DATA(4)	C4	Input	LVCMOS	None	DCLK	DDR	
DATA(5)	C6	Input	LVCMOS	None	DCLK	DDR	
DATA(6)	C3	Input	LVCMOS	None	DCLK	DDR	
DATA(7)	C13	Input	LVCMOS	None	DCLK	DDR	
DATA(8)	C15	Input	LVCMOS	None	DCLK	DDR	
DATA(9)	C16	Input	LVCMOS	None	DCLK	DDR	
DATA(10)	C18	Input	LVCMOS	None	DCLK	DDR	
DATA(11)	C19	Input	LVCMOS	None	DCLK	DDR	
DATA(12)	C21	Input	LVCMOS	None	DCLK	DDR	
DATA(13)	C22	Input	LVCMOS	None	DCLK	DDR	
DATA(14)	D22	Input	LVCMOS	None	DCLK	DDR	
DATA(15)	D21	Input	LVCMOS	None	DCLK	DDR	
DATA(16)	D19	Input	LVCMOS	None	DCLK	DDR	
DATA(17)	D4	Input	LVCMOS	None	DCLK	DDR	
DATA(18)	D9	Input	LVCMOS	None	DCLK	DDR	
DATA(19)	D10	Input	LVCMOS	None	DCLK	DDR	
DATA(20)	D6	Input	LVCMOS	None	DCLK	DDR	
DATA(21)	D16	Input	LVCMOS	None	DCLK	DDR	
DATA(22)	D7	Input	LVCMOS	None	DCLK	DDR	
DATA(23)	D15	Input	LVCMOS	None	DCLK	DDR	
DCLK	D13	Input	LVCMOS	None	–	–	Input data bus clock
Data Control Inputs							
$\overline{\text{LOADB}}$	D12	Input	LVCMOS	None	DCLK	DDR	Parallel data load enable
TRC	D3	Input	LVCMOS	None	DCLK	DDR	Input data toggle rate control
SCTRL	D18	Input	LVCMOS	None	DCLK	DDR	Serial control bus
SAC_BUS	D33	Input	LVCMOS	None	SAC_CLK	–	Stepped address control serial bus data
SAC_CLK	D29	Input	LVCMOS	None	–	–	Stepped address control serial bus clock
Mirror Reset Control Inputs							
DRC_BUS	C29	Input	LVCMOS	None	SAC_CLK		DMD reset-control serial bus
$\overline{\text{DRC_OE}}$	C33	Input	LVCMOS	None	–	–	Active-low output enable signal for internal DMD Reset driver circuitry
DRC_STROBE	C36	Input	LVCMOS	None	SAC_CLK		Strobe signal for DMD Reset Control inputs
Power							
VBIAS	C31, C32	Power	Analog	None	–	–	Mirror Reset Bias Voltage
VOFFSET	D25, D26	Power	Analog	None	–	–	Mirror Reset Offset Voltage
VRESET	D31, D32	Power	Analog	None	–	–	Mirror Reset Voltage
VREF	C25, C26	Power	Analog	None	–	–	Power Supply for Low Voltage CMOS Double-Data-Rate (DDR) Interface

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Table 3. Connector Pins for FQE (continued)

TERMINAL NAME	CONNECTOR PINS	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	DATA RATE	DESCRIPTION
VCC	C1, C2, C34, C35, C37, C38, C39, C40, D1, D2, D34, D35, D37, D38, D39, D40	Power	Analog	None	–	–	Power Supply for LVCMOS Logic
VSS	C5, C8, C11, C14, C17, C20, C23, C24, C27, C28, C30, D5, D8, D11, D14, D17, D20, D23, D24, D27, D28, D30	Power	Analog	None	–	–	Ground - Common return for all power inputs
No connect	A1-A25, B1-B25, D36, E1-E25, F1-F25	–	–	–	–	–	For proper device operation, leave these terminals unconnected.

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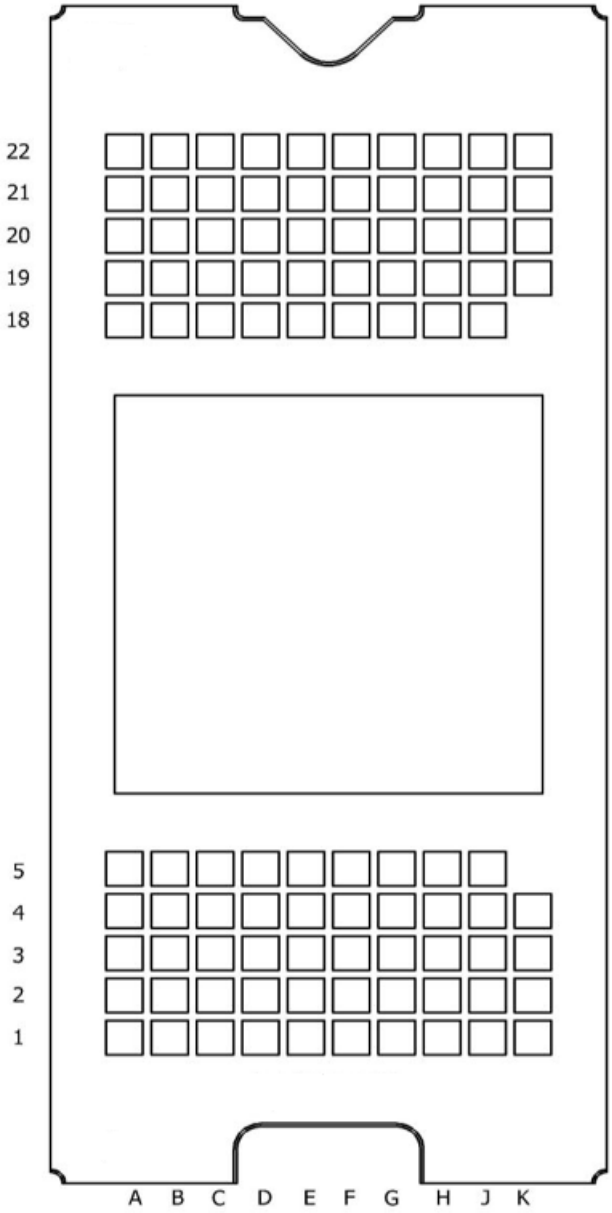

Figure 9. Package Connector Signal Names (Device Bottom View) for FQD

Table 4. Connector Pins for FQD

TERMINAL NAME	CONNECTOR PINS	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	DATA RATE	DESCRIPTION
Data Inputs							
DATA(0)	A1	Input	LVCMOS	None	DCLK	DDR	Input data bus
DATA(1)	A2	Input	LVCMOS	None	DCLK	DDR	
DATA(2)	A3	Input	LVCMOS	None	DCLK	DDR	
DATA(3)	A4	Input	LVCMOS	None	DCLK	DDR	
DATA(4)	B1	Input	LVCMOS	None	DCLK	DDR	
DATA(5)	B3	Input	LVCMOS	None	DCLK	DDR	
DATA(6)	C1	Input	LVCMOS	None	DCLK	DDR	
DATA(7)	C3	Input	LVCMOS	None	DCLK	DDR	
DATA(8)	C4	Input	LVCMOS	None	DCLK	DDR	
DATA(9)	D1	Input	LVCMOS	None	DCLK	DDR	
DATA(10)	D4	Input	LVCMOS	None	DCLK	DDR	
DATA(11)	E1	Input	LVCMOS	None	DCLK	DDR	
DATA(12)	E4	Input	LVCMOS	None	DCLK	DDR	
DATA(13)	F1	Input	LVCMOS	None	DCLK	DDR	
DATA(14)	F3	Input	LVCMOS	None	DCLK	DDR	
DATA(15)	G1	Input	LVCMOS	None	DCLK	DDR	
DATA(16)	G2	Input	LVCMOS	None	DCLK	DDR	
DATA(17)	G4	Input	LVCMOS	None	DCLK	DDR	
DATA(18)	H1	Input	LVCMOS	None	DCLK	DDR	
DATA(19)	H2	Input	LVCMOS	None	DCLK	DDR	
DATA(20)	H4	Input	LVCMOS	None	DCLK	DDR	
DATA(21)	J1	Input	LVCMOS	None	DCLK	DDR	
DATA(22)	J3	Input	LVCMOS	None	DCLK	DDR	
DATA(23)	J4	Input	LVCMOS	None	DCLK	DDR	
DCLK	K1	Input	LVCMOS	None	–	–	Input data bus clock
Data Control Inputs							
$\overline{\text{LOADB}}$	K2	Input	LVCMOS	None	DCLK	DDR	Parallel data load enable
TRC	K4	Input	LVCMOS	None	DCLK	DDR	Input data toggle rate control
SCTRL	K3	Input	LVCMOS	None	DCLK	DDR	Serial control bus
SAC_BUS	C20	Input	LVCMOS	None	SAC_CLK	–	Stepped address control serial bus data
SAC_CLK	C22	Input	LVCMOS	None	–	–	Stepped address control serial bus clock
Mirror Reset Control Inputs							
DRC_BUS	B21	Input	LVCMOS	None	SAC_CLK		DMD reset-control serial bus
$\overline{\text{DRC_OE}}$	A20	Input	LVCMOS	None	–	–	Active-low output enable signal for internal DMD Reset driver circuitry
DRC_STROBE	A22	Input	LVCMOS	None	SAC_CLK		Strobe signal for DMD Reset Control inputs
Power							
VBIAS	C19, D19	Power	Analog	None	–	–	Mirror Reset Bias Voltage
VOFFSET	A19, K19	Power	Analog	None	–	–	Mirror Reset Offset Voltage
VRESET	E19, F19	Power	Analog	None	–	–	Mirror Reset Voltage
VREF	B19, J19	Power	Analog	None	–	–	Power Supply for Low Voltage CMOS Double-Data-Rate (DDR) Interface

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Table 4. Connector Pins for FQD (continued)

TERMINAL NAME	CONNECTOR PINS	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	DATA RATE	DESCRIPTION
VCC	B22, C2, D21, E2, E20, E22, F21, G3, G19, G20, G22, H19, H21, J20, J22, K21	Power	Analog	None	–	–	Power Supply for LVCMOS Logic
VSS	A21, B2, B4, B20, C21, D2, D3, D20, D22, E3, E21, F2, F4, F20, F22, G21, H3, H20, H22, J2, J21, K20	Power	Analog	None	–	–	Ground - Common return for all power inputs
No connect	A5, A18, B5, B18, C5, C18, D5, D18, E5, E18, F5, F18, G5, G18, H5, H18, J5, J18, K22	–	–	–	–	–	For proper device operation, leave these terminals unconnected.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. The *Absolute Maximum Ratings* are stress ratings only, and functional performance of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
Electrical					
VCC	Voltage applied to VCC (1)		–0.5	4	V
VREF	Voltage applied to VREF (1)		–0.5	4	V
VOFFSET	Voltage applied to VOFFSET (1) (2)		–0.50	8.75	V
VBIAS	Voltage applied to VBIAS (1) (2)		–0.5	17.0	V
VRESET	Voltage applied to VRESET (1)		–11	0.5	V
	Supply voltage delta |VBIAS – VOFFSET| (2)			8.75	V
	Voltage applied to all other input terminals		–0.5	VREF + 0.5	V
	Current required from a high-level output	V_{OH} = 1.4 V		–9	mA
	Current required from a low-level output	V_{OL} = 0.4 V		18	mA
Environmental					
	Storage temperature range (3) (4) (5)		-40	85	°C
	Storage humidity (3) (4) (5)	Non-condensing	0	95	% RH
	Illumination power density (5) (6)	< 420 nm		0.68	mW/cm^2
		420 nm to 700 nm	See (7)		
		> 700 nm		10	
	Electrostatic discharge immunity (8)	All pins		2000	V

(1) All voltages referenced to VSS (ground). Voltages VCC, VREF, VOFFSET, VBIAS, and VRESET are required for proper DMD operation.
(2) Exceeding the recommended allowable absolute voltage difference between VBIAS and VOFFSET may result in excessive current draw.
(3) Simultaneous exposure to high storage temperature and high storage humidity may affect device reliability.
(4) As a best practice, TI recommends storing the DMD in a temperature and humidity controlled environment.
(5) Optimal, long-term performance of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty-cycle, ambient temperature (storage and operating), case temperature, ambient humidity (storage and operating), and power on/off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle. Contact your local TI representative for additional information related to optimizing the DMD performance.
(6) Total integrated illumination power density above or below the indicated wavelength threshold.
(7) Limited only by the resulting array temperature. S the *Thermal Characteristics* for information related to calculating the micromirror array temperature.
(8) Tested in accordance with JESD22-A114-B Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the *Recommended Operating Conditions*. No level of performance is implied when operating the device above or below the *Recommended Operating Conditions* limits.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ELECTRICAL						
VREF	LVCMOS interface supply voltage (1)		1.6	1.9	2.0	V
VCC	LVCMOS logic supply voltage (1)		2.375	2.500	2.625	V
VOFFSET	Mirror electrode and HVCMOS supply voltage (1)(2)		8.25	8.500	8.75	V
VBIAS	Mirror electrode voltage (1)(2)		15.5	16 .0	16.5	V
VRESET	Mirror electrode voltage (1)		– 9.5	–10.0	–10.5	V
	Delta supply voltage |VBIAS – VOFFSET| (2)				8.75	V
V_{T+}	Positive-going threshold voltage		0.4 × VREF		0.7 × VREF	V
V_{T-}	Negative-going threshold voltage		0.3 × VREF		0.6 × VREF	V
V_{hys}	Hysteresis voltage ($V_{T+} – V_{T-}$)		0.1 × VREF		0.4 × VREF	V
f_{DCLK}	DCLK clock frequency		80		120	MHz
MECHANICAL						
Package FQE	Static load applied to the package electrical connector area (3)	Uniformly distributed across the three datum-A areas and the datum-E area.			110	N
	Static load applied to the DMD mounting area (3)				110	N
Package FQD	Load applied to the thermal interface area (3)				62	N
	Load applied to the electrical interface areas (3)	Uniformly distributed over 2 areas			55	N
ENVIRONMENTAL						
Operating Case Temperature			See (4).	26	See (4).	°C
Operating Humidity (4)		non-condensing		60	See (4)	% RH
Operating Device Temperature Gradient (5)					10	°C
Operating Landed Duty-Cycle (4)(6)			See (4)	25	See (4)	%

(1) Voltages VCC, VREF, VOFFSET, VBIAS, VRESET are required for proper DMD operation. All voltages referenced to VSS (ground).
(2) Exceeding the recommended voltage difference between VBIAS and VOFFSET may result in excessive current draw.
(3) See System Interface Load diagrams on the next pages.
(4) Optimal, long-term performance of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty-cycle, ambient temperature (storage and operating), case temperature, ambient humidity (storage and operating), and power on/off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle. Contact your local TI representative for additional information related to optimizing the DMD performance.
(5) As measured between any two points on or within the package including the mirror array. See the *Thermal Characteristics* for information related to calculating the micromirror array temperature.
(6) Landed Duty-Cycle refers to the percentage of time an individual micromirror spends landed in one state (+12° or -12°) versus the other state (-12° or +12°).

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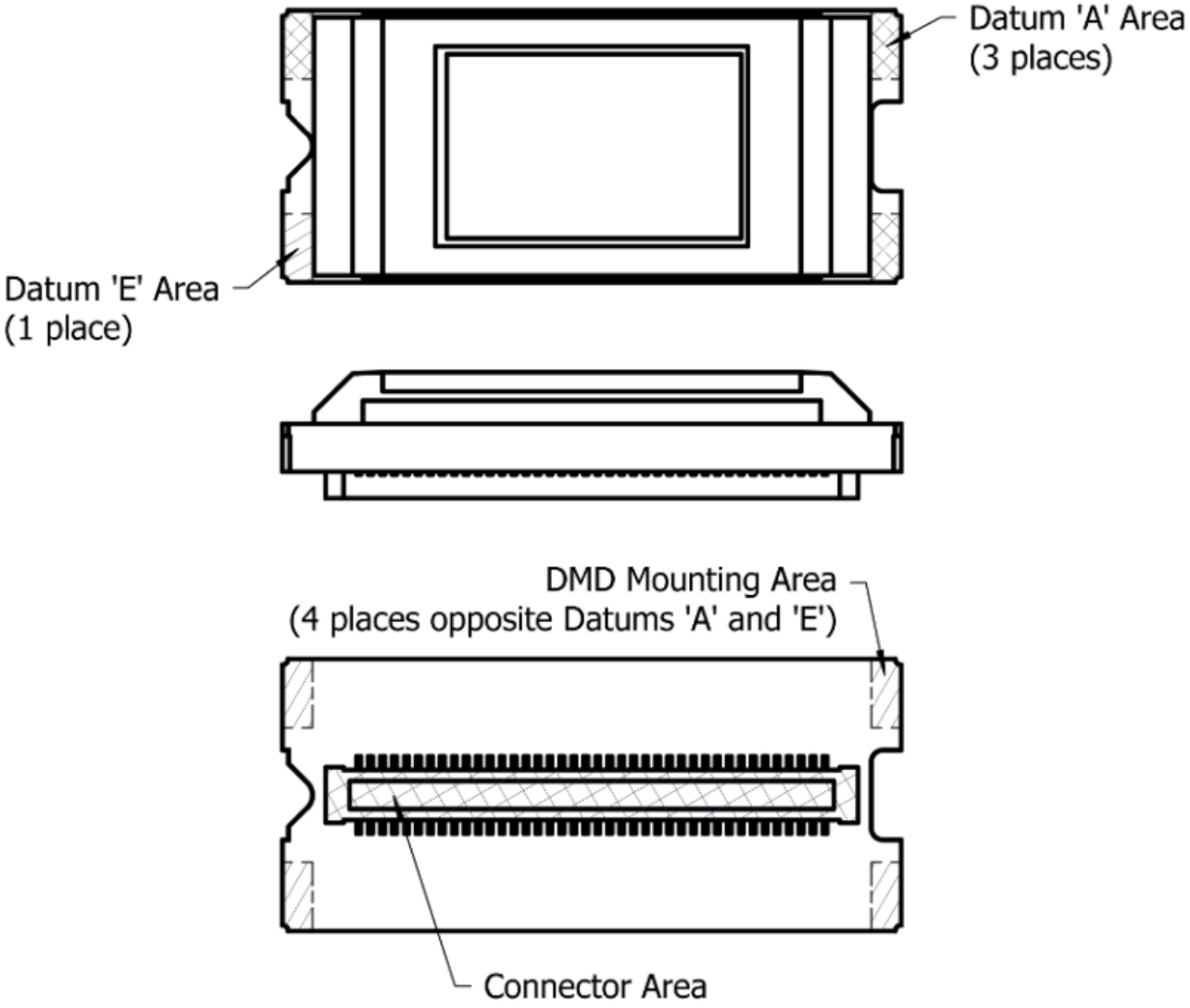

Figure 10. System Interface Loads for FQE

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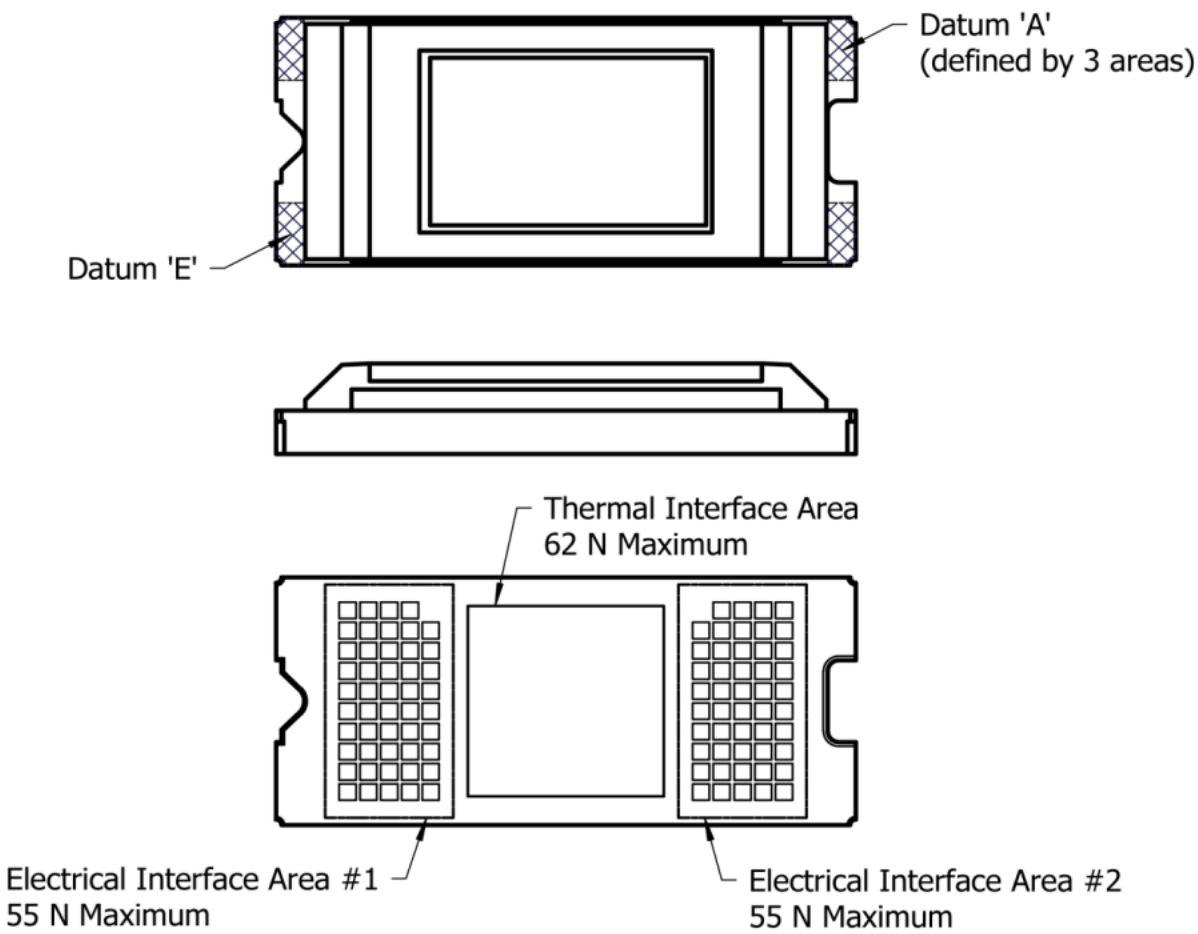

Figure 11. System Interface Loads for FQD

ELECTRICAL CHARACTERISTICS

over the range of recommended supply voltage and recommended case operating temperature (unless otherwise noted)

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 2.5 V,	I_{OH} = –21 mA	1.7			V
V_{OL}	Low-level output voltage	V_{CC} = 2.5 V,	I_{OH} = 15 mA			0.4	V
I_{OH}	High-level output current	V_{OH} = 1.4 V				-9	mA
I_{OL}	Low-level output current	V_{OL} = 0.4 V				18	mA
I_{IL}	Low-level input current(1)	V_{REF} = 2.00 V	V_I = 0 V	–50			nA
I_{IH}	High-level input current(1)	VREF = 2.00 V	V_I = VREF			50	nA
I_{REF}	Current into VREF terminal	VREF = 2.00 V	f_{DCLK} = 120 MHz		2.15	2.75	mA
I_{CC}	Current into VCC terminal	VCC = 2.75 V	f_{DCLK} = 120 MHz		125	160	mA
I_{OFFSET}	Current into VOFFSET terminal(2)	VOFFSET = 8.75 V	3 Global Resets within Time Period = 200µs		3	3.3	mA
I_{BIAS}	Current into VBIAS terminal(2)(3)	VBIAS = 16.5 V	3 Global Resets within Time Period = 200µs		2.55	3.55	mA
I_{RESET}	Current into VRESET terminal	VRESET = –10.5 V			2.45	3.10	mA
P_{REF}	Power into VREF terminal(4)	VREF = 2.00 V	f_{DCLK} = 120 MHz		3.87	5.50	mW
P_{CC}	Power into VCC terminal(4)	VCC = 2.75 V	f_{DCLK} = 120 MHz		312.5	440.0	mW
P_{OFFSET}	Power into VOFFSET terminal(4)	VOFFSET = 8.75 V	3 Global Resets within Time Period = 200µs		25.5	28.9	mW
P_{BIAS}	Power into VBIAS terminal(4)	VBIAS = 16.5 V	3 Global Resets within Time Period = 200µs		40.8	58.6	mW
P_{RESET}	Power into VRESET terminal(4)	VRESET = –10.5 V			24.5	32.6	mW
C_I	Input capacitance	f = 1 MHz				10	pF
C_O	Output capacitance	f = 1 MHz				10	pF

(1) Applies to LVCMOS pins only. LVCMOS pins do not have pull-up or pull-down configurations.
(2) Exceeding the maximum allowable absolute voltage difference between VBIAS and VOFFSET may result in excesses current draw. See the *Absolute Maximum Ratings* for further details.
(3) When $\overline{DRC_OE}$ = High, the internal reset drivers are tri-stated and I_{BIAS} standby current is 6.5mA.
(4) In some applications, the total DMD heat load can be dominated by the amount of incident light energy absorbed. See the *Thermal Characteristics* for further details.

Measurement Conditions

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. *Figure 12* shows an equivalent test load circuit for the output under test. The load capacitance value stated is only for characterization and measurement of ac timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

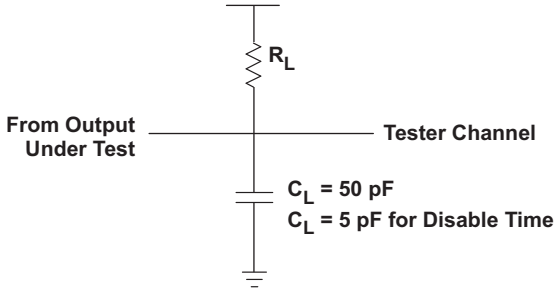

Figure 12. Test Load Circuit for AC Timing Measurements

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SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_{s1}	Setup time: DATA before rising or falling edge of DCLK(1)		0.7			ns
	Setup time: TRC before rising or falling edge of DCLK(1)		0.7			
	Setup time: SCTRL before rising or falling edge of DCLK(1)		0.7			
t_{s2}	Setup time: $\overline{\text{LOADB}}$ low before rising edge of DCLK(1)		0.7			ns
t_{s3}	Setup time: SAC_BUS low before rising edge of SAC_CLK(1)		1			ns
t_{s4}	Setup time: DRC_BUS high before rising edge of SAC_CLK(1)		1			ns
t_{s5}	Setup time: DRC_STROBE high before rising edge of SAC_CLK(1)		1			ns
t_{h1}	Hold time: DATA after rising or falling edge of DCLK(1)		0.7			ns
	Hold time: TRC after rising or falling edge of DCLK (1)		0.7			
	Hold time: SCTRL after rising or falling edge of DCLK(1)		0.7			
t_{h2}	Hold time: $\overline{\text{LOADB}}$ low after falling edge of DCLK(1)		0.7			ns
t_{h3}	Hold time: SAC_BUS low after rising edge of SAC_CLK (1)		1			ns
t_{h4}	Hold time: DRC_BUS after rising edge of SAC_CLK(1)		1			ns
t_{h5}	Hold time: DRC_STROBE after rising edge of SAC_CLK(1)		1			ns
t_{c1}	Clock cycle: DCLK		8.33	10	12.5	ns
t_{c3}	Clock cycle: SAC_CLK		12.5	13.33	14.3	ns
t_{w1}	Pulse width high or low: DCLK		3.33			ns
t_{w2}	Pulse width low: $\overline{\text{LOADB}}$		4.73			ns
t_{w3}	Pulse width high or low: SAC_CLK		5			ns
t_{w5}	Pulse width high: DRC_STROBE		7			ns
t_r	Rise time (20% - 80%): DCLK / SAC_CLK	VREF = 1.8V			1.08	ns
	Rise time (20% - 80%): DATA / TRC / SCTRL / $\overline{\text{LOADB}}$	VREF = 1.8V			1.08	
t_f	Fall time (20% - 80%): DCLK / SAC_CLK	VREF = 1.8V			1.08	ns
	Fall time (20% - 80%): DATA / TRC / SCTRL / $\overline{\text{LOADB}}$				1.08	

(1) For fast input slew rate > 1 V/ns. For slow slew rates > 0.5ns and < 1ns, the setup and hold times will be longer. For every 0.1V decrease in slew rate from 1 V/ns, add 150 picoseconds on setup and hold. The numbers assume all the slew rates for all the inputs and the clock are the same.

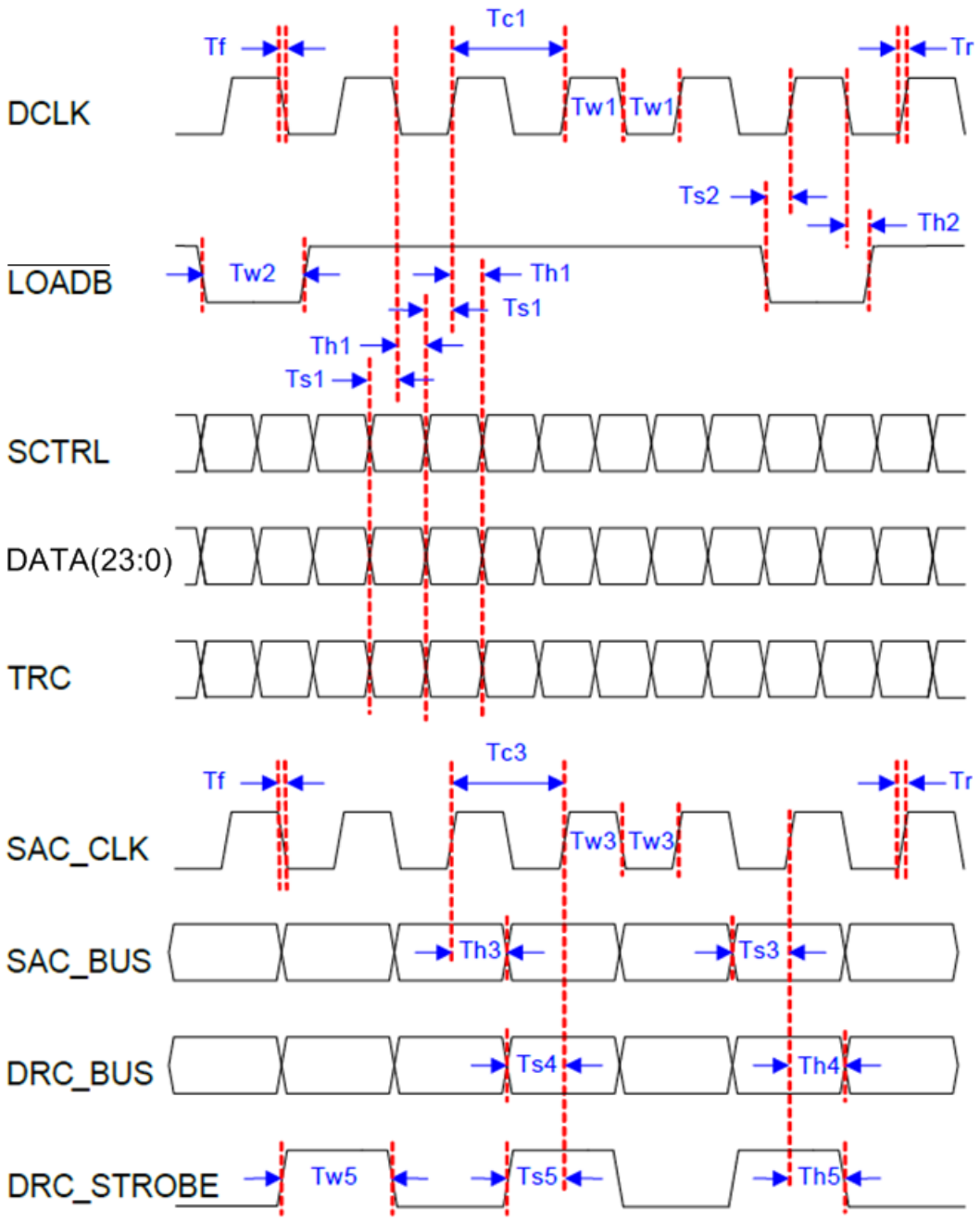

Figure 13. Switching Characteristics

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POWER SUPPLY SEQUENCING REQUIREMENTS

DLP4500 includes five voltage-level supplies (V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET}). For reliable operation of DLP4500, the following power supply sequencing requirements must be followed.

CAUTION

Reliable performance of the DMD requires that the following conditions be met:

1. That the V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supply inputs all be present during operation.
2. That the V_{CC}, V_{REF}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supplies be sequenced on and off in the manner prescribed below.

Repeated failure to adhere to the prescribed power-up and power-down procedures may affect device reliability

DMD Power Supply Power-Up Procedure

Step 1: Power up V_{CC} and V_{REF} in any order

Step 2: Wait for V_{CC} and V_{REF} to each reach a stable level within their respective recommended operating ranges.

Step 3: Power up V_{BIAS}, V_{OFFSET}, and V_{RESET} in any order, provided that the maximum delta-voltage between V_{BIAS} and V_{OFFSET} is not exceeded (see Absolute Maximum Ratings for details).

Note 1: ***During the power-up procedure, the DMD LVCMOS inputs should not be driven high until after Step 2 has been completed.***

Note 2: ***Power supply slew rates during power up are unrestricted, provided that all other conditions are met.***

DMD Power Supply Power-Down Procedure

Step 1: Command the chip set controller to execute a mirror-parking sequence. See the controller data sheet (listed in *Related Documents*) for details.

Step 2: Power down V_{BIAS}, V_{OFFSET}, and V_{RESET} in any order, provided that the maximum delta voltage between V_{BIAS} and V_{OFFSET} is not exceeded (see *Absolute Maximum Ratings* for details).

Step 3: Wait for V_{BIAS}, V_{OFFSET}, and V_{RESET} to each discharge to a stable level within 4 V of the reference ground.

Step 4: Power down V_{CC} and V_{REF} in any order.

Note 1: ***During the power-down procedure, the DMD LVCMOS inputs should be held at a level less than V_{REF} + 0.3 volts.***

Note 2: ***Power-supply slew rates during power down are unrestricted, provided that all other conditions are met.***

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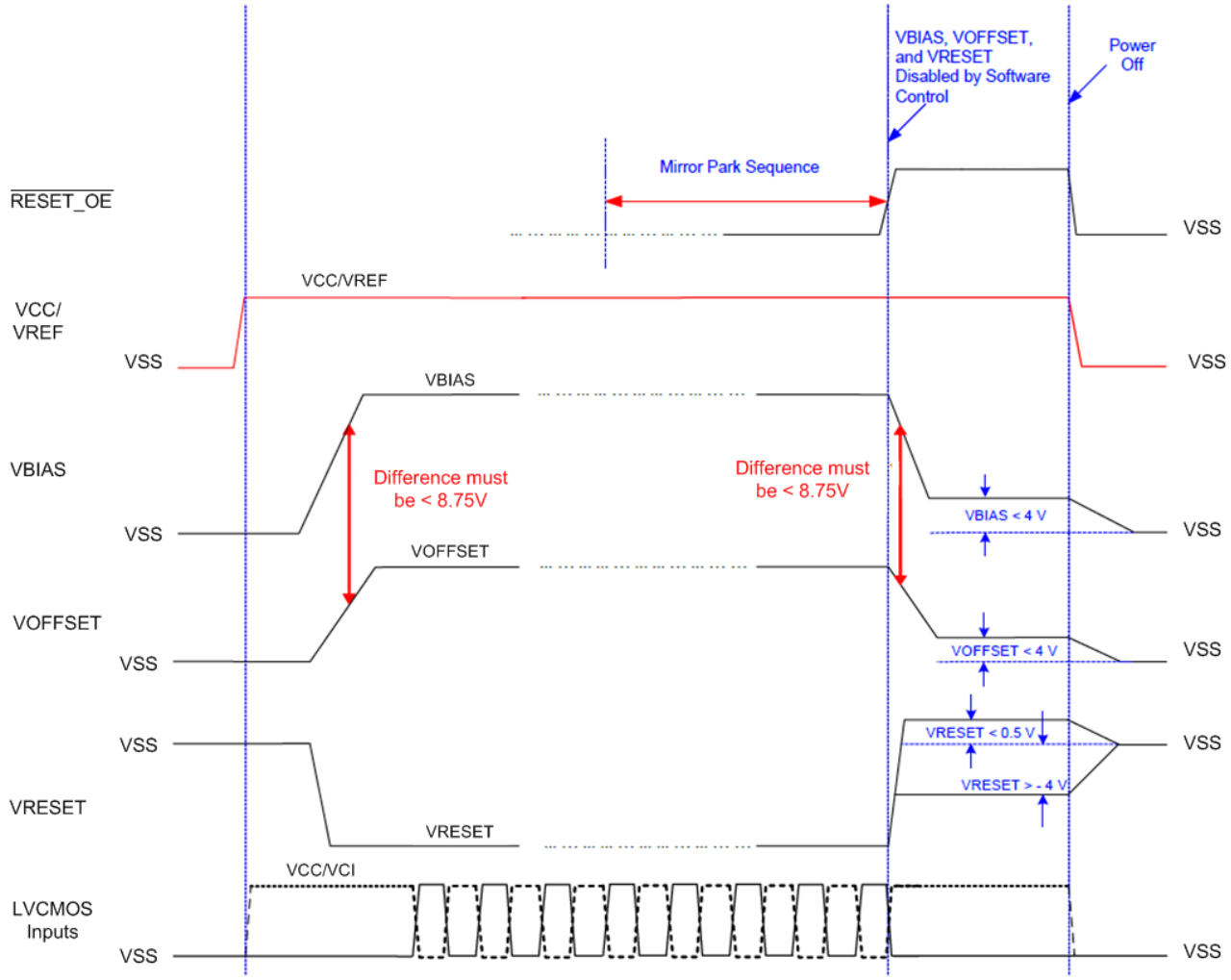

Figure 14. Power-Up / Power-Down Timing

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Micromirror Array Physical Characteristics

Physical characteristics of the micromirror array are provided in Table 5.

Table 5. Micromirror Array Physical Characteristics

PARAMETER	VALUE	UNITS
Number of active micromirror rows (1)	1140	micromirrors
Number of active micromirror columns (1)	912	micromirrors
Micromirror pitch, diagonal (1)	7.637	µm
Micromirror pitch, vertical and horizontal (1)	10.8	µm
Micromirror active array height (2)	1140	micromirrors
	6161.4	µm
Micromirror active array width (2)	912	micromirrors
	9855	µm
Micromirror array border (3)	10	mirrors/side

(1) See Figure 3.
(2) See Figure 15.
(3) The mirrors that form the array border are hard-wired to tilt in the –12° ("Off") direction once power is applied to the DMD (see Figure 3 and Figure 4).

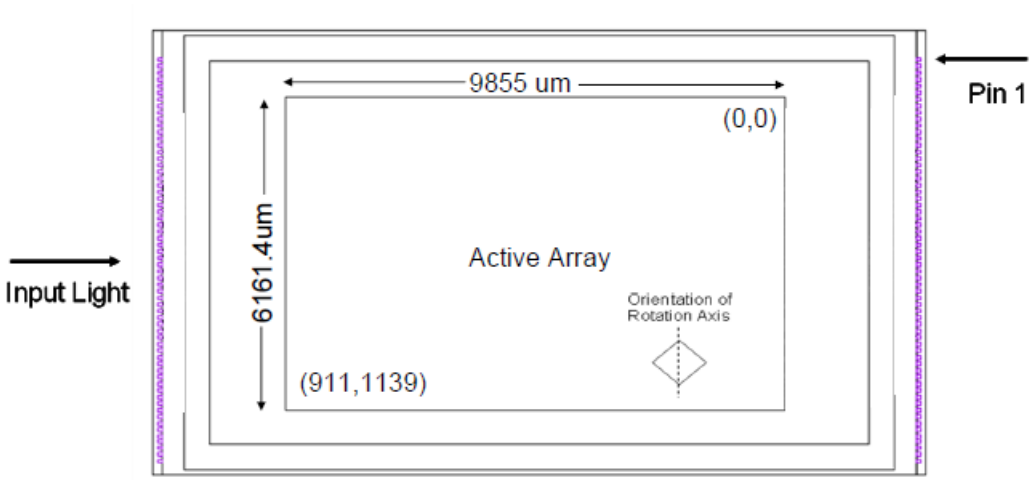

Figure 15. DLP4500 Micromirror Active Area

Micromirror Array Optical Characteristics

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. See the related application reports (listed in Related Documents) for guidelines.

Table 6. Optical Parameters

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
α Micromirror tilt angle	DMD *parked* state(1)(3)(4), see (10)		0		degrees
	DMD "landed" state(1)(5)(6), see (10)	11	12	13	
β Micromirror tilt angle variation(1)(5)(7)(8)(9)	See (10)	–1		1	degrees
Micromirror crossover time(2)(12)			5		µs
Micromirror switching time(12)			16		µs
Non-operating micromirrors(11)	Non-adjacent micromirrors			10	micromirrors
	Adjacent micromirrors			0	
Orientation of the micromirror axis-of-rotation(13)		89	90	91	degrees
Micromirror array optical efficiency(14)(15)	420 nm to 700 nm, with all micromirrors in the ON state		66%		
Mirror metal specular reflectivity (420 nm – 700 nm)			89.4%		
Window material			Corning Eagle XG		
Window refractive index	At 546.1 nm		1.5119		
Window aperture			See (16)		
Illumination Overfill(17)					

(1) Measured relative to the plane formed by the overall micromirror array

(2) Micromirror crossover time is primarily a function of the natural response time of the micromirrors.

(3) *Parking* the micromirror array returns all of the micromirrors to a relatively flat (0˚) state (as measured relative to the plane formed by the overall micromirror array).

(4) When the micromirror array is *parked*, the tilt angle of each individual micromirror is uncontrolled.

(5) Additional variation exists between the micromirror array and the package datums.

(6) When the micromirror array is *landed*, the tilt angle of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror *landing* in an nominal angular position of +12 degrees. A binary value of 0 results in a micromirror *landing* in an nominal angular position of –12 degrees.

(7) Represents the *landed* tilt angle variation relative to the nominal *landed* tilt angle

(8) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.

(9) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations and/or system contrast variations.

(10) See Figure 4.

(11) Non-operating micromirror is defined as a micromirror that is unable to transition nominally from the –12 degree position to +12 degrees or vice versa.

(12) Performance as measured at the start of life.

(13) Measured relative to the package datums B and C, shown in the Package Mechanical Data section at the end of this document.

(14) The minimum or maximum DMD optical efficiency observed in a specific application depends on numerous application-specific design variables, such as:

- Illumination wavelength, bandwidth/line-width, degree of coherence
- Illumination angle, plus angle tolerance
- Illumination and projection aperture size, and location in the system optical path
- IIllumination overfill of the DMD micromirror array
- Aberrations present in the illumination source and/or path
- Aberrations present in the projection path
- etc.

The specified nominal DMD optical efficiency is based on the following use conditions:

- Visible illumination (420 nm–700 nm)

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- Input illumination optical axis oriented at 24° relative to the window normal
- Projection optical axis oriented at 0° relative to the window normal
- f/3 illumination aperture
- f/2.4 projection aperture

Based on these use conditions, the nominal DMD optical efficiency results from the following four components:

- Micromirror array fill factor: nominally 92.5%
- Micromirror array diffraction efficiency: nominally 86%
- Micromirror surface reflectivity: nominally 88%
- Window transmission: nominally 97% (single pass, through two surface transitions)

(15) Does not account for the effect of micromirror switching duty cycle, which is application dependant. Micromirror switching duty cycle represents the percentage of time that the micromirror is actually reflecting light from the optical illumination path to the optical projection path. This duty cycle depends on the illumination aperture size, the projection aperture size, and the micromirror array update rate.

(16) See the Package Mechanical Characteristics for details regarding the size and location of the window aperture.

(17) The active area of the DLP4500 is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can create artifacts from the mechanical features that surround the active array and other surface anomalies that may be visible on the projected image. The illumination optical system should be designed to limit light flux incident anywhere outside the active array less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause visible artifacts.

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Thermal Characteristics

Achieving optimal DMD performance requires proper management of the maximum DMD case temperature, the maximum temperature of any individual micromirror in the active array, the maximum temperature of the window aperture, and the temperature gradient between any two points on or within the package.

See the *Absolute Maximum Ratings* and *Recommended Operation Conditions* for applicable temperature limits.

Package Thermal Resistance

The DMD is designed to conduct the absorbed and dissipated heat back to the Series FQE or FQD package where it can be removed by an appropriate system thermal management. The system thermal management must be capable of maintaining the package within the specified operational temperatures at the Thermal Test Point location, see Figure 16 or Figure 17. The total heat load on the DMD is typically driven by the incident light absorbed by the active area; although other contributions can include light energy absorbed by the window aperture, electrical power dissipation of the array, and/or parasitic heating.

Table 7. FQE and FQD Package Thermal Resistance

	Min	Nom	Max	Units
Thermal resistance from active area to case			2	°C/W

Case Temperature

The temperature of the DMD case can be measured directly. For consistency, a thermal test point location is defined, as shown in Figure 16 and Figure 17.

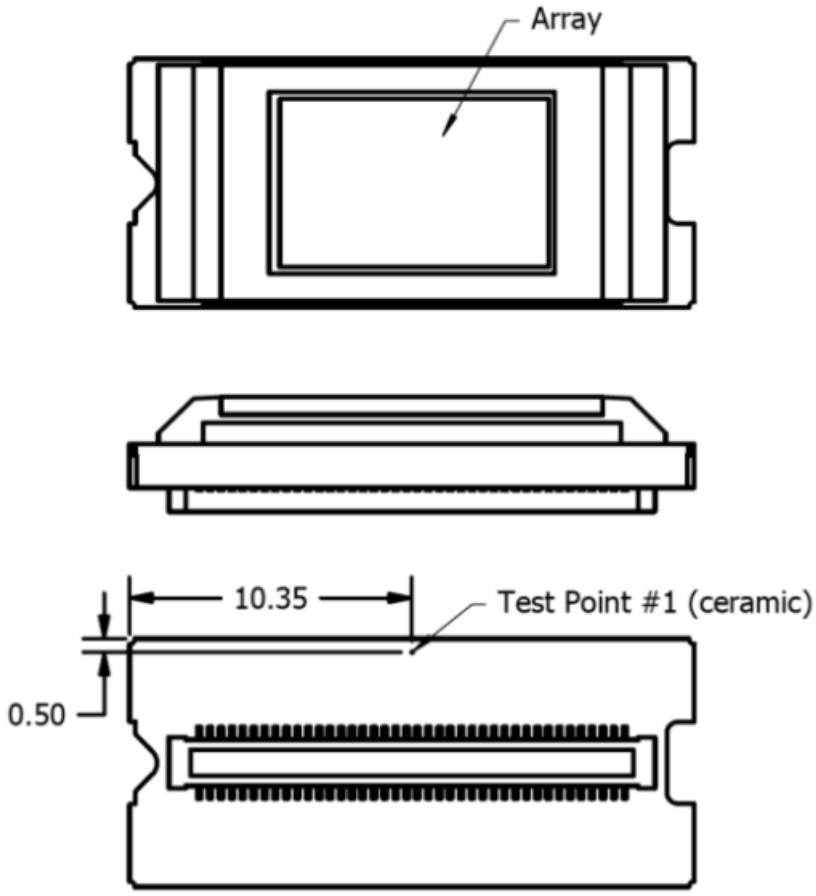

Figure 16. Thermal Test Point Location for FQE

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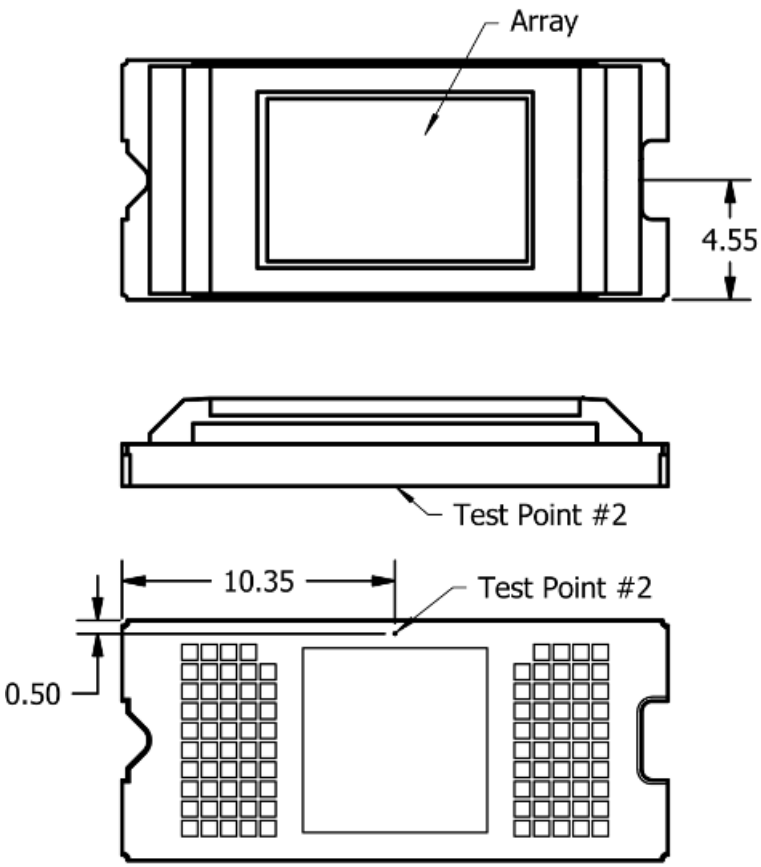

Figure 17. Thermal Test Point Location for FQD

Micromirror Array Temperature Calculation

Micromirror array temperature cannot be measured directly. Therefore, it must be computed analytically from:

Thermal test point location (See Test Point #1 in Figure 16 for FQE and Test Point #2 in Figure 17 for FQD)

Package thermal resistance

Electrical power dissipation

Illumination heat load

The relationship between the micromirror array and the reference ceramic temperature, Thermocouple Location (Test Point #1 in Figure 16 for FQE and Test Point #2 in Figure 17 for FQD), is provided by the following equations:

$T_{Array} = T_{Ceramic} + (Q_{Array} \times R_{Array\text{-}To\text{-}Ceramic})$

$Q_{Array} = Q_{Elec} + Q_{Illum}$

$Q_{Illum} = C_{L2W} \times SL$

where the following elements are defined as:

T_{Array} = computed micromirror array temperature (°C)

$T_{Ceramic}$ = ceramic case temperature (°C) (Test Point location)

Q_{Array} = Total DMD array power (electrical + absorbed) (W)

$R_{Array\text{-}to\text{-}Ceramic}$ = thermal resistance of DMD package from array to TC3 (°C/W)

Q_{Elec} = nominal electrical power (W)

Q_{Illum} = absorbed illumination heat (W)

C_{L2W} = Lumens-to-watts constant, estimated at 0.00293 watt/lumen, based on array characteristics. It assumes a spectral efficiency of 300 lumens/watt for the projected light, illumination distribution of 83.7% on the active array, and 16.3% on the array border and window aperture.

SL = measured screen lumens (lumens)

These equations are based on traditional 1-chip DLP system with a total projection efficiency from the DMD to the screen of 87%. An example calculation for package FQE is provided below. DMD electrical power dissipation varies and is dependent on the voltage, data rates, and operating frequencies. The nominal electrical power dissipation used in this calculation is 0.25 watts. Screen lumens is 200 lumens. The ceramic case temperature at Test Point #1 is 55°C. Using these values in the above equations, the following values are computed:

$Q_{Array} = Q_{Elec} + C_{L2W} \times SL = 0.25\ W + (0.00293\ W/Lumen \times 200\ Lumen) = 0.836\ W$

$T_{Array} = T_{Ceramic} + (Q_{Array} \times R_{Array\text{-}To\text{-}Ceramic}) = 55\ °C + (0.836\ W \times 2°C/W) = 56.67°C$

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed the device From: Preview To: Production	1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DLP4500FQD	ACTIVE	LCCC	FQD	98	5	Green (RoHS & no Sb/Br)	Call TI	Level-1-NC-NC			Samples
DLP4500FQE	ACTIVE	LCCC	FQE	80	5	Green (RoHS & no Sb/Br)	Call TI	Level-1-NC-NC			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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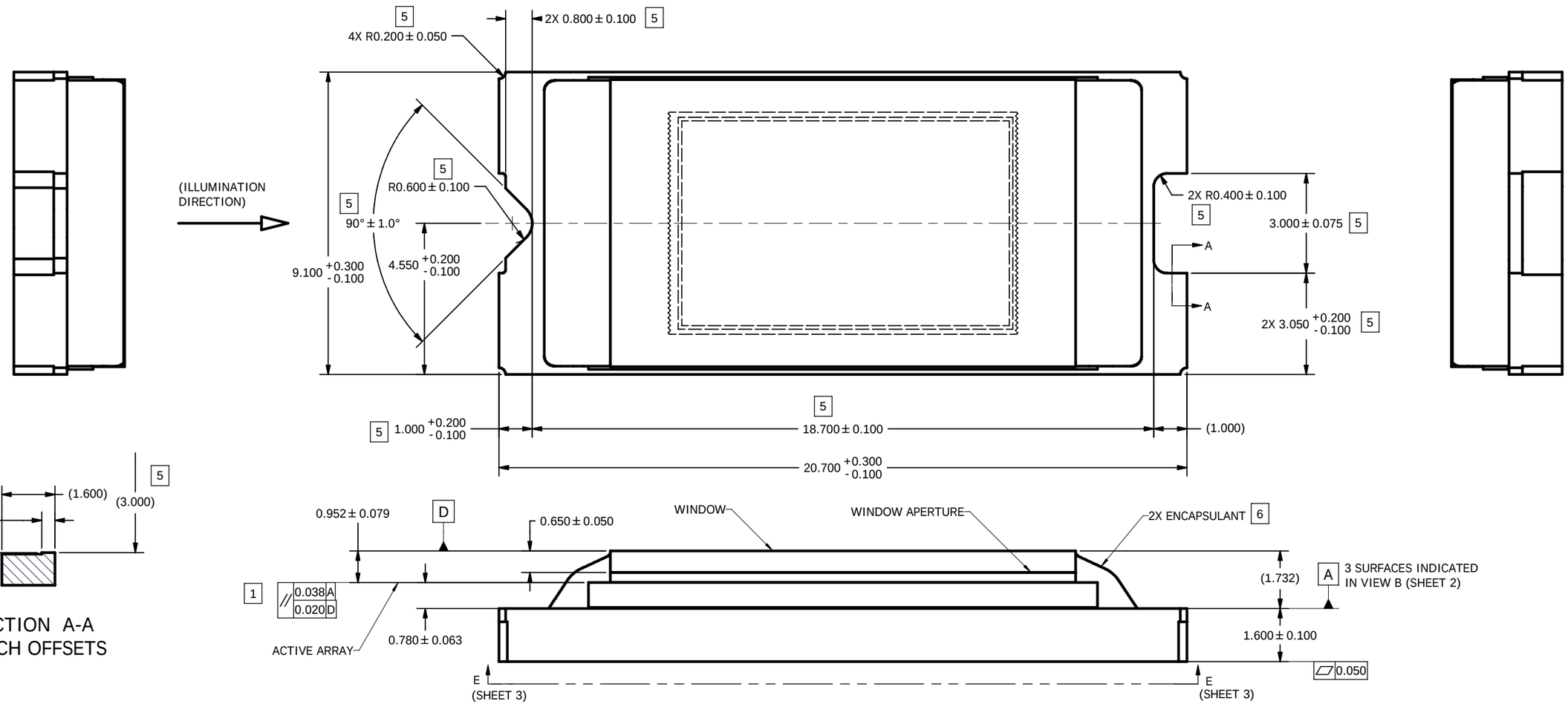
REVISIONS

REV	DESCRIPTION	DATE	BY
A	ECO 2104138 INITIAL RELEASE	01/20/2010	J. HOLM
B	ECO 2121955 CORRECT APERTURE X DIMENSIONS VIEW D	1/23/2012	BMH

NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. DMD MARKING TO APPEAR ON SYMBOLIZATION PAD.
5. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
6. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEWS C AND D (SHEET 2).
7. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, WHEN MOUNTING IN SYSTEM.



NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- REMOVE ALL BURRS AND SHARP EDGES
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	J. HOLM	12/11/2009
ENGINEER	J. HOLM	12/11/2009
QA/CE	P. KONRAD	1/20/2010
CM	F. ARMSTRONG	1/20/2010
APPROVED	J. HALL	1/20/2010

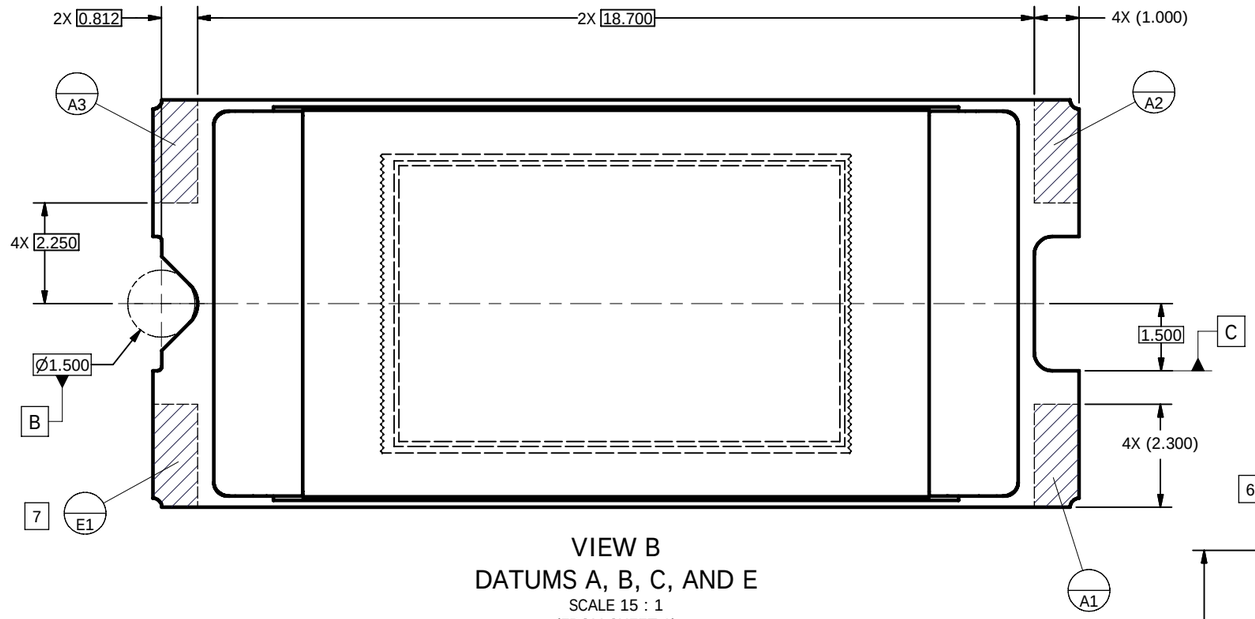
TEXAS INSTRUMENTS
Dallas Texas

TITLE
ICD, MECHANICAL, DMD,
.45 WXGA-800 DDR SERIES 310

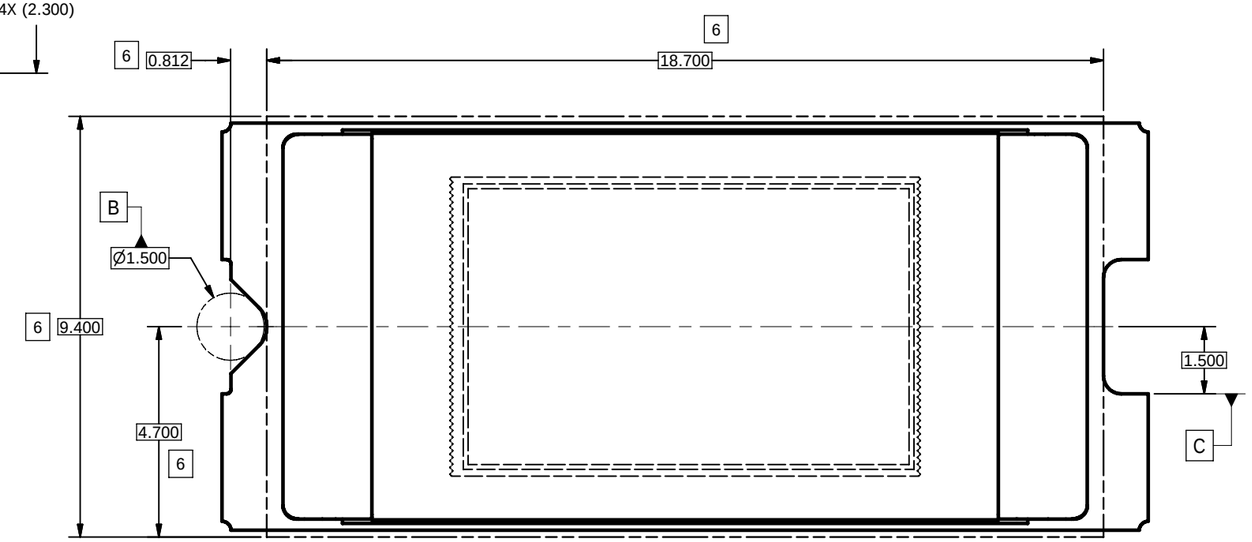
SIZE D | DWG NO 2510852 | REV B

SCALE 15:1 | SHEET 1 OF 3

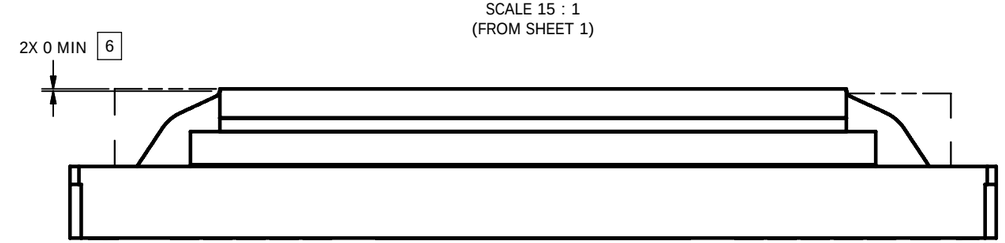
INV11-2006a



VIEW B
DATUMS A, B, C, AND E
SCALE 15 : 1
(FROM SHEET 1)



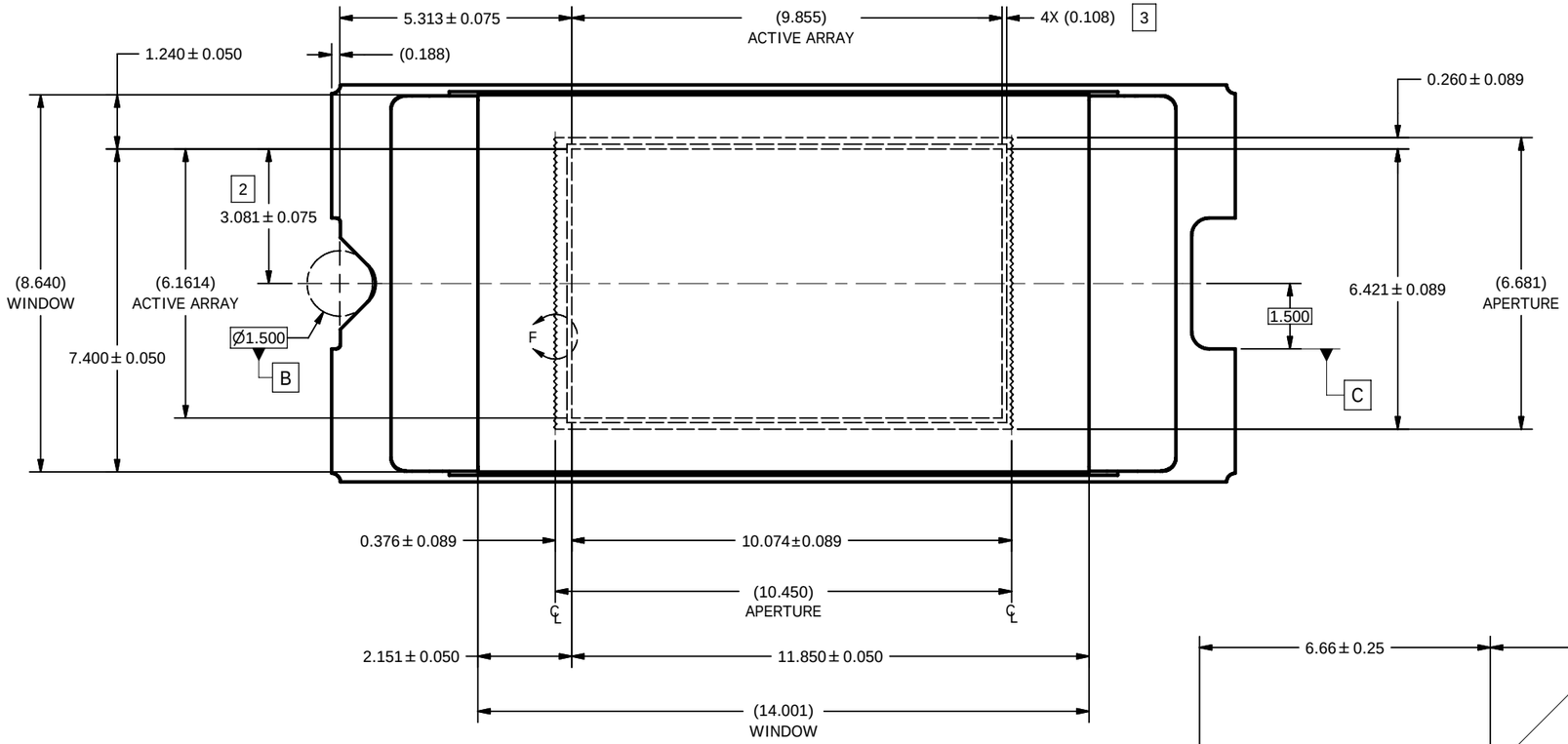
VIEW C
ENCAPSULANT MAXIMUM X/Y DIMENSIONS
SCALE 15 : 1
(FROM SHEET 1)



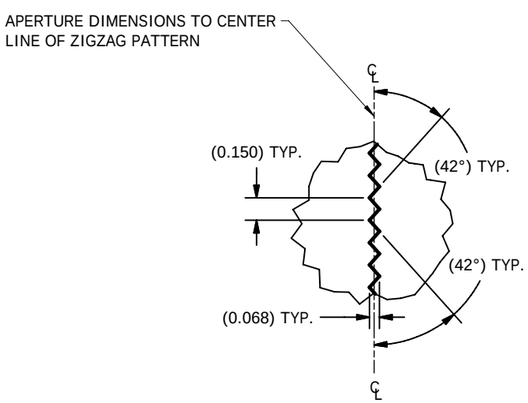
VIEW D
ENCAPSULANT MAXIMUM HEIGHT
SCALE 15 : 1

TEXAS INSTRUMENTS Dallas Texas	DRAWN J. HOLM	DATE 12/11/2009	SIZE D		DWG NO 2510852	REV B
			SCALE		SHEET 2 OF 3	

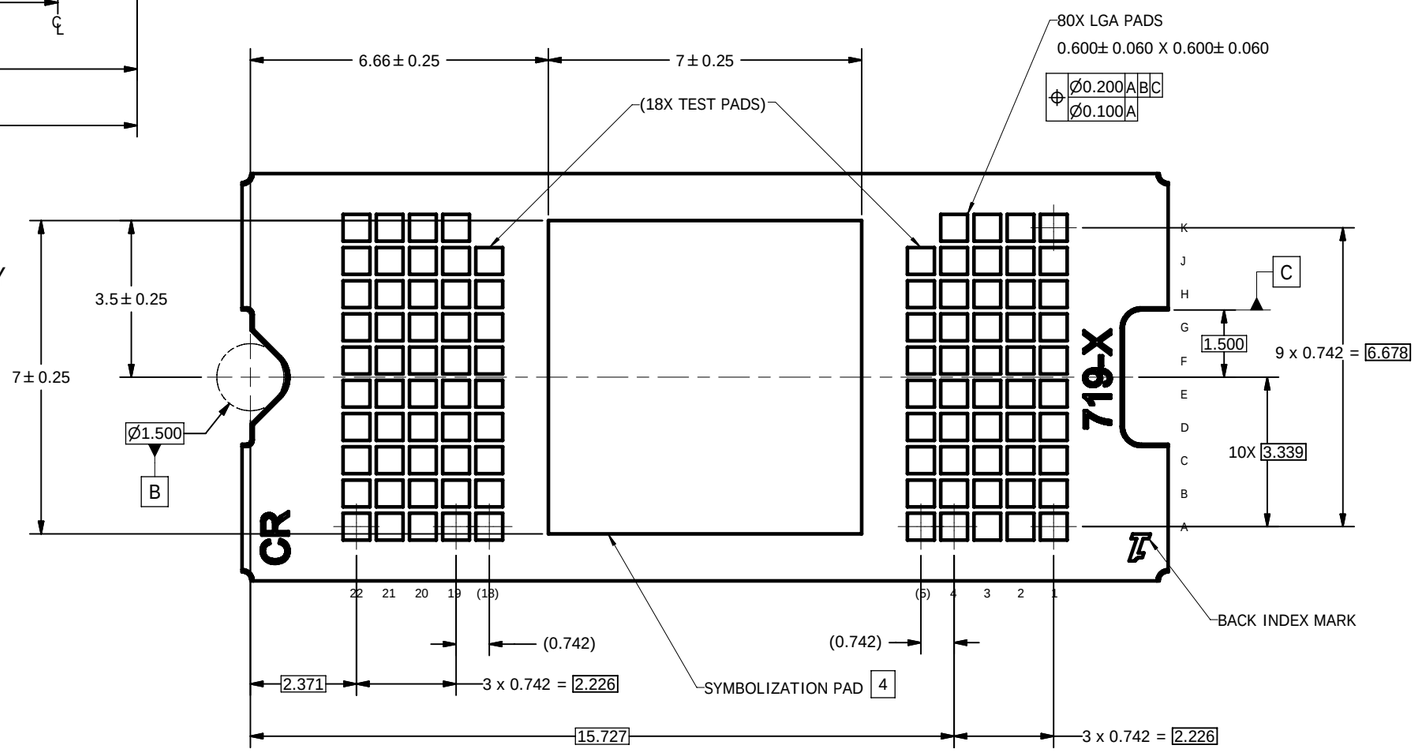
INV11-2006a



VIEW D
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL F
APERTURE SHORT EDGES
SCALE 50 : 1



VIEW E-E
BACK SIDE METALLIZATION
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN J. HOLM	DATE 12/11/2009	SIZE D	DWG NO 2510852	REV B
			SCALE	SHEET 3 OF 3	

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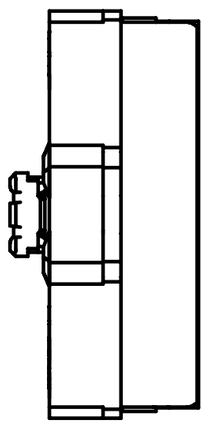
REVISIONS

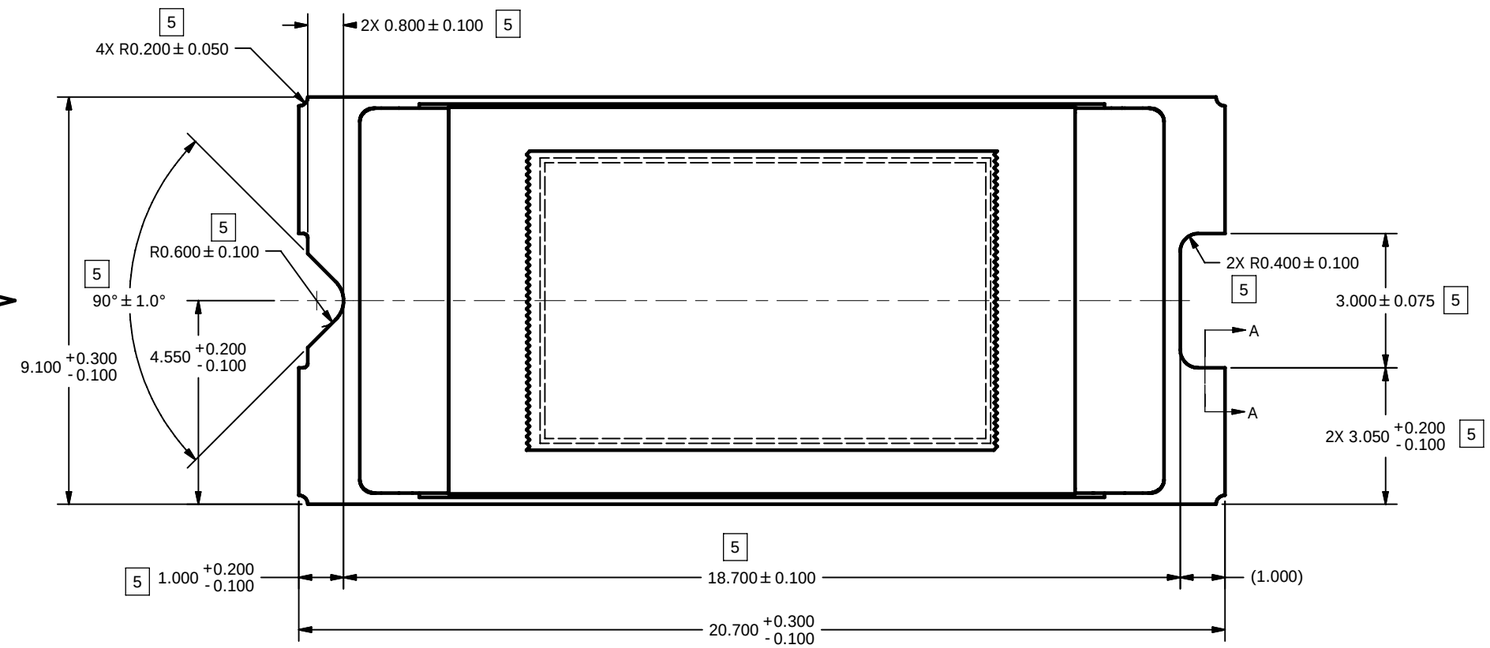
REV	DESCRIPTION	DATE	BY
A	ECO #2109845 - INITIAL RELEASE	8/16/2010	JLH
B	ECO #2121955 - CORRECT APERTURE X DIM'S IN VIEW D	1/23/2012	BMH

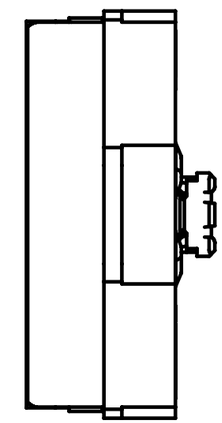
NOTES UNLESS OTHERWISE SPECIFIED:

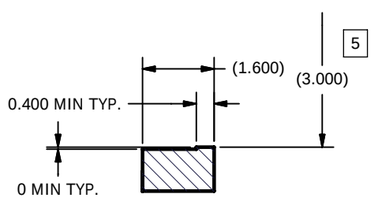
1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. DMD MARKING TO APPEAR IN CONNECTOR RECESS.
5. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
6. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEWS C AND D (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
7. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, WHEN MOUNTING IN SYSTEM.
8. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.



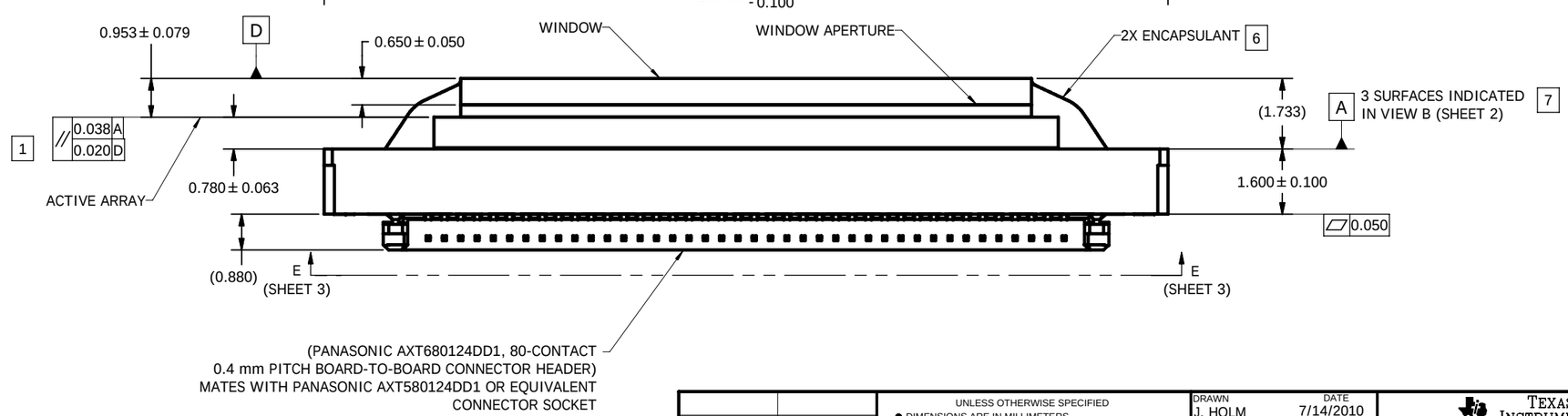
(ILLUMINATION DIRECTION)







5 SECTION A-A
NOTCH OFFSETS



NEXT ASSY	USED ON
NONE	0314DA

APPLICATION

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- REMOVE ALL BURRS AND SHARP EDGES
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

		DATE
DRAWN	J. HOLM	7/14/2010
ENGINEER	J. HOLM	7/13/2010
QA/CE		
CM		
APPROVED		

TEXAS INSTRUMENTS
Dallas Texas

TITLE
ICD, MECHANICAL, DMD,
.45 WXGA-800 DDR SERIES 241

SIZE	DWG NO	REV
D	2511423	B

SCALE 15:1 SHEET 1 OF 3

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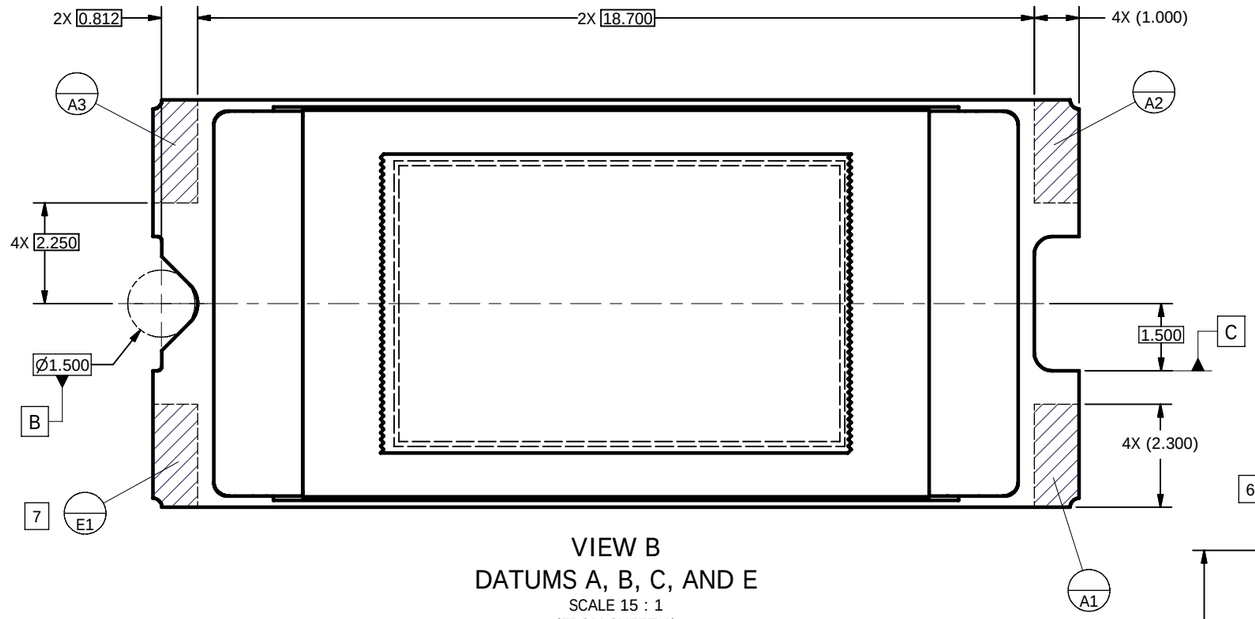
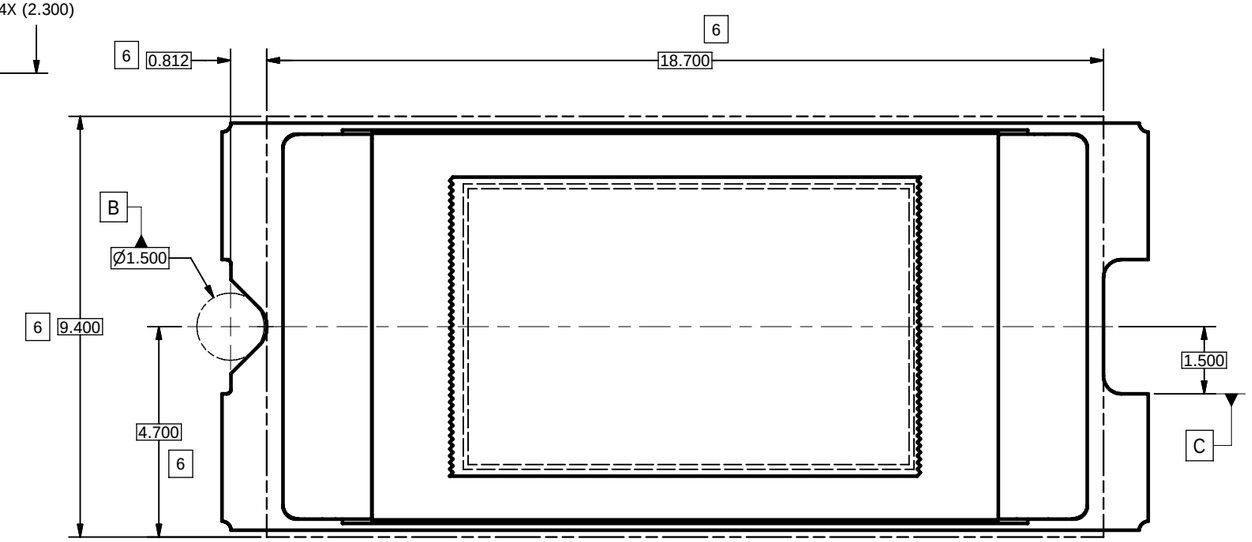
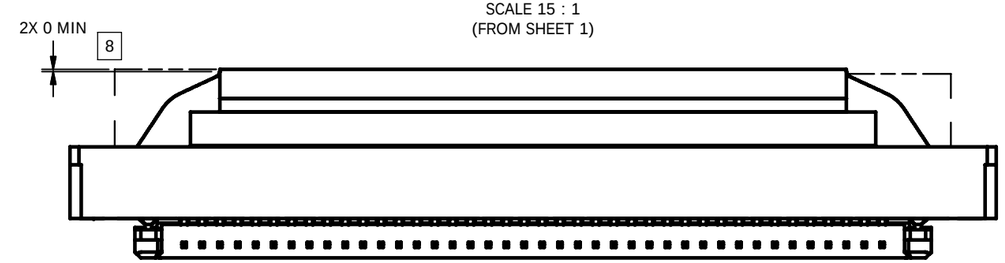


VIEW B
DATUMS A, B, C, AND E
SCALE 15 : 1
(FROM SHEET 1)



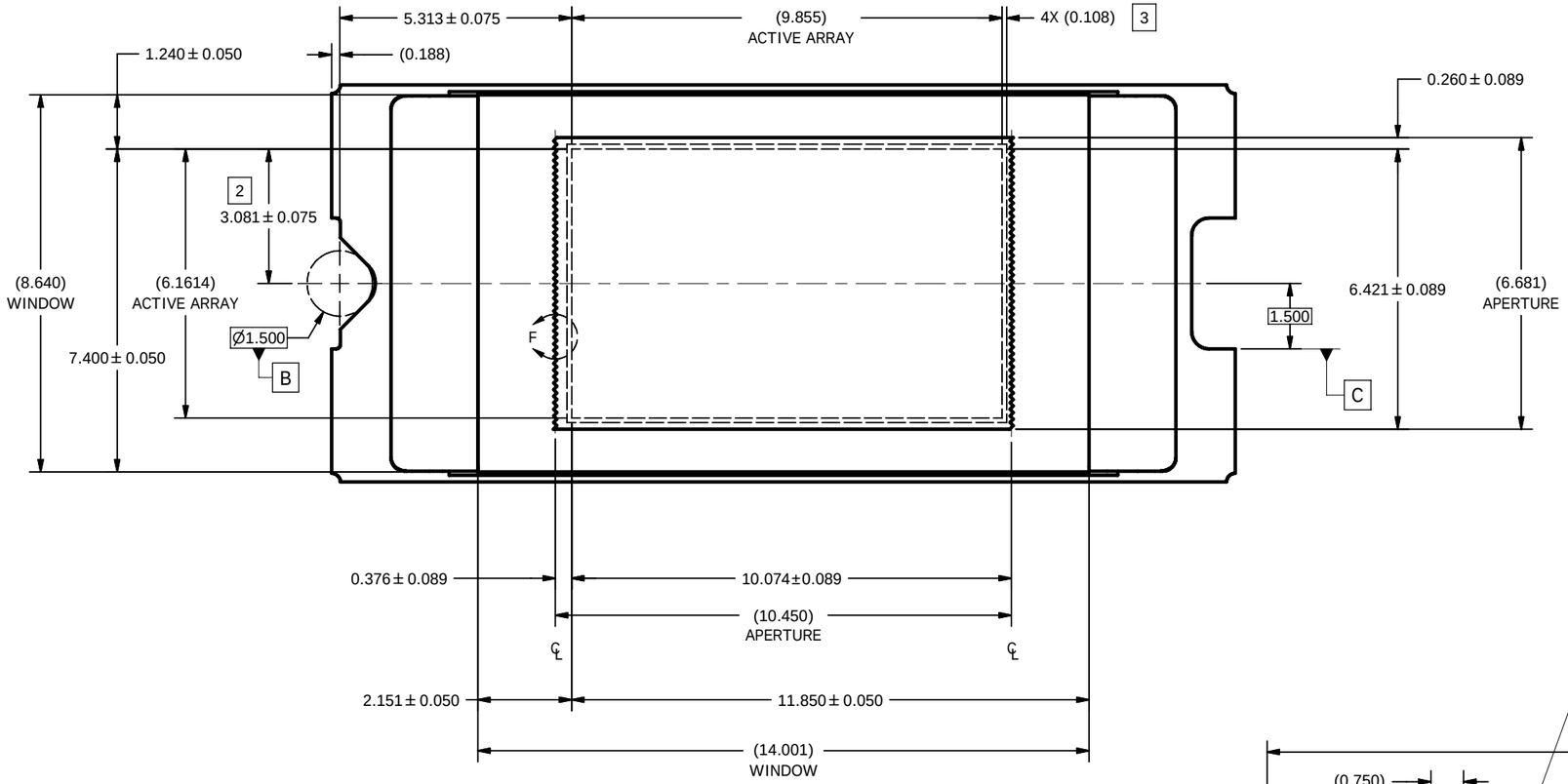
VIEW C
ENCAPSULANT MAXIMUM X/Y DIMENSIONS
SCALE 15 : 1
(FROM SHEET 1)



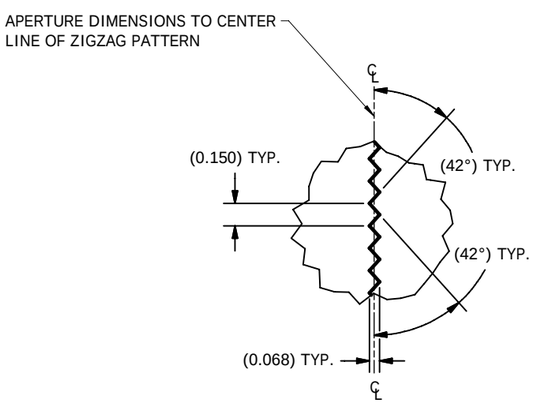
VIEW D
ENCAPSULANT MAXIMUM HEIGHT
SCALE 15 : 1

TEXAS INSTRUMENTS Dallas Texas	DRAWN J. HOLM	DATE 7/14/2010	SIZE D		DWG NO 2511423	REV B
			SCALE		SHEET 2 OF 3	

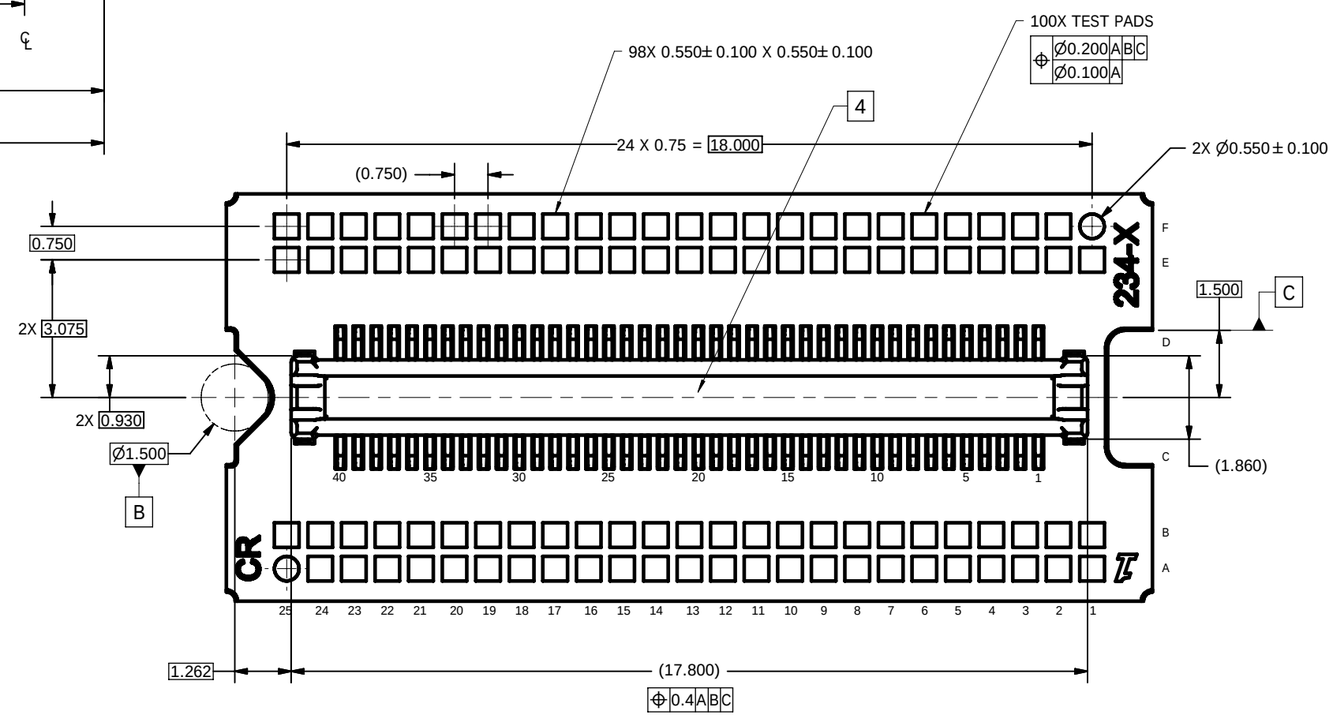
INV11-2006a



VIEW D
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL F
APERTURE SHORT EDGES
SCALE 50 : 1



VIEW E-E
TEST PADS AND CONNECTOR
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN J. HOLM	DATE 7/14/2010	SIZE D	DWG NO 2511423	REV B
			SCALE	SHEET 3 OF 3	

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