# Stratix III Device Handbook, Volume 2

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# Chapter Revision Dates

The chapter in this book was revised on the following date. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1 Stratix III Device Datasheet: DC and Switching Characteristics
Revised: *July 2010*
Part Number: *SIII52001-2.3*

This handbook provides comprehensive information about the Altera® Stratix® III family of devices.

## How to Contact Altera

For the most up-to-date information about Altera products, see the following table.

| Contact *(Note 1)* | Contact Method | Address |
|---|---|---|
| Technical support | Website | www.altera.com/support |
| Technical training | Website | www.altera.com/training |
| | Email | custrain@altera.com |
| Product literature | Website | www.altera.com/literature |
| Non-technical support (General) | Email | nacomp@altera.com |
| (Software Licensing) | Email | authorization@altera.com |

**Note:**

(1) You can also contact your local Altera sales office or sales representative.

## Typographic Conventions

The following table shows the typographic conventions that this document uses.

| Visual Cue | Meaning |
|---|---|
| **Bold Type with Initial Capital Letters** | Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box. |
| **bold type** | External timing parameters, directory names, project names, disk drive names, file names, file name extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file. |
| *Italic Type with Initial Capital Letters* | Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.* |
| *Italic type* | Internal timing parameters and variables are shown in italic type. Examples: $t_{PIA}$, $n + 1$.<br>Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file. |
| Initial Capital Letters | Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu. |
| "Subheading Title" | References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions." |

| Visual Cue | Meaning |
|---|---|
| `Courier type` | Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`.<br><br>Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier. |
| 1., 2., 3., and<br>a., b., c., etc. | Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure. |
| ■ ■ | Bullets are used in a list of items when the sequence of the items is not important. |
| ✓ | The checkmark indicates a procedure that consists of one step only. |
| ☞ | The hand points to information that requires special attention. |
| CAUTION | A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work. |
| WARNING | A warning calls attention to a condition or possible situation that can cause injury to the user. |
| ↵ | The angled arrow indicates you should press the Enter key. |
| 👣 | The feet direct you to more information on a particular topic. |


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# Section I. DC & Switching Characteristics of Stratix III Devices

When Stratix® III devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Stratix III devices, system designers must consider the operating requirements discussed in the following chapter:

- Chapter 1, Stratix III Device Datasheet: DC and Switching Characteristics

## Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

# 1. Stratix III Device Datasheet: DC and Switching Characteristics

SIII52001-2.3

## Electrical Characteristics

This chapter describes the electrical characteristics, switching characteristics, and I/O timing for Stratix® III devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include core performance specifications and periphery performance. A glossary is also included for your reference.

## Operating Conditions

When Stratix III devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Stratix III devices, system designers must consider the operating requirements described in this chapter.

Stratix III devices are offered in both commercial and industrial grades. Commercial devices are offered in –2 (fastest), –3, –4, and –4L speed grades. Industrial devices are offered only in –3, –4, and –4L speed grades.

In this chapter, a prefix associated with the operating temperature range is attached to the speed grades; commercial with a "C" prefix and industrial with an "I" prefix. For example, commercial devices are indicated as C2, C3, C4, and C4L per respective speed grades. Industrial devices are indicated as I3, I4, and I4L.

### Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix III devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Conditions beyond those listed in Table 1–1 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods may have adverse effects on the device.

**Table 1–1.** Absolute Maximum Ratings for Stratix III Devices *(Note 1)* (Part 1 of 2)

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{CCL}$ | Selectable core voltage power supply | -0.5 | 1.65 | V |
| $V_{CC}$ | I/O registers power supply | -0.5 | 1.65 | V |
| $V_{CCD_PLL}$ | Phase-locked loop (PLL) digital power supply | -0.5 | 1.65 | V |
| $V_{CCA_PLL}$ | PLL analog power supply | -0.5 | 3.75 | V |
| $V_{CCPT}$ | Programmable power technology power supply | -0.5 | 3.75 | V |
| $V_{CCPGM}$ | Configuration pins power supply | -0.5 | 3.9 | V |
| $V_{CCPD}$ | I/O pre-driver power supply | -0.5 | 3.9 | V |
| $V_{CCIO}$ | I/O power supply | -0.5 | 3.9 | V |

**Table 1–1.** Absolute Maximum Ratings for Stratix III Devices *(Note 1)* (Part 2 of 2)

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{CC_CLKIN}$ | Differential clock input power supply (top and bottom I/O banks only) | -0.5 | 3.75 | V |
| $V_{CCBAT}$ | Battery back-up power supply for design security volatile key register | -0.5 | 3.75 | V |
| $V_I$ | DC Input voltage | -0.5 | 4.0 | V |
| $T_J$ | Operating junction temperature | -55 | 125 | °C |
| $I_{OUT}$ | DC output current, per pin | -25 | 40 | mA |
| $T_{STG}$ | Storage temperature (No bias) | -65 | 150 | °C |

**Note to Table 1–1:**

(1) Supply voltage specifications apply to voltage readings taken at the device pins, not the power supply.

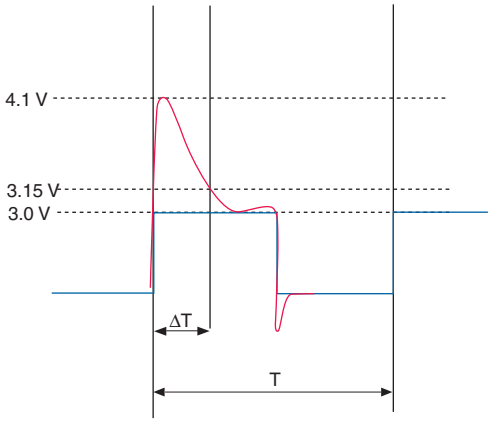
### Sinusoidal Maximum Allowed Overshoot/Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in Table 1–2 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as percentage of high-time over the lifetime of the device.

A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.2 V can only be at 4.2 V for 15.8% over the lifetime of the device; for a device lifetime of 10 years, this is equivalent to 15.8% of ten years which is 18.96 months. Figure 1–1 shows how to determine the overshoot duration.

**Figure 1–1.** Overshoot Duration




In the example shown in Figure 1–1, the overshoot voltage is shown in red and is present at the Stratix III pin, up to 4.1 V. From Table 1–2, for an overshoot of up to 4.1 V, the percentage of high time for overshoot > 3.15 V can be as high as 46% over an 11.4-year period. The percentage of high time is calculated as (delta T/T) * 100. This 11.4-year period assumes the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations where the device is in an idle state, lifetimes are increased.

**Table 1–2.** Maximum Allowed Overshoot During Transitions

| Symbol | Parameter | Condition | Overshoot Duration as a % of High Time | Unit |
|---|---|---|---|---|
| Vi (AC) | AC Input Voltage *(1)* | 4 | 100.000 | % |
| | | 4.05 | 79.330 | % |
| | | 4.1 | 46.270 | % |
| | | 4.15 | 27.030 | % |
| | | 4.2 | 15.800 | % |
| | | 4.25 | 9.240 | % |
| | | 4.3 | 5.410 | % |
| | | 4.35 | 3.160 | % |
| | | 4.4 | 1.850 | % |
| | | 4.45 | 1.080 | % |
| | | 4.5 | 0.630 | % |
| | | 4.55 | 0.370 | % |
| | | 4.6 | 0.220 | % |
| | | 4.65 | 0.130 | % |
| | | 4.7 | 0.074 | % |
| | | 4.75 | 0.043 | % |
| | | 4.8 | 0.025 | % |
| | | 4.85 | 0.015 | % |

**Note to Table 1–2:**

(1) This input voltage is regardless of the $V_{CCIO}$ supply which is used to power up the input buffer.

## Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Stratix III devices. Table 1–3 lists the steady-state voltage and current values expected from Stratix III devices. All supplies are required to monotonically reach their full-rail values within $t_{RAMP}$.

**Table 1–3.** Recommended Operating Conditions for Stratix III Devices (Part 1 of 2)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCL}$ | Selectable core voltage power supply for internal logic and input buffers | — | 1.05 | 1.1 | 1.15 | V |
| | Selectable core voltage power supply for internal logic and input buffers | — | 0.86 | 0.9 | 0.94 | V |
| $V_{CC}$ | I/O registers power supply | — | 1.05 | 1.1 | 1.15 | V |
| $V_{CCD_PLL}$ | PLL digital power supply | — | 1.05 | 1.1 | 1.15 | V |
| $V_{CCA_PLL}$ | PLL analog power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCPT}$ | Power supply for the programmable power technology | — | 2.375 | 2.5 | 2.625 | V |

**Table 1–3.** Recommended Operating Conditions for Stratix III Devices (Part 2 of 2)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCPGM}$ | Configuration pins power supply, 3.3 V | — | 3.135 | 3.3 | 3.465 | V |
| | Configuration pins power supply, 3.0 V | — | 2.85 | 3 | 3.15 | V |
| | Configuration pins power supply, 2.5 V | — | 2.375 | 2.5 | 2.625 | V |
| | Configuration pins power supply, 1.8 V | — | 1.71 | 1.8 | 1.89 | V |
| $V_{CCPD}$ *(1)* | I/O pre-driver power supply, 3.3 V | — | 3.135 | 3.3 | 3.465 | V |
| | I/O pre-driver power supply, 3.0 V | — | 2.85 | 3 | 3.15 | V |
| | I/O pre-driver power supply, 2.5 V | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCIO}$ | I/O power supply, 3.3 V | — | 3.135 | 3.3 | 3.465 | V |
| | I/O power supply, 3.0 V | — | 2.85 | 3 | 3.15 | V |
| | I/O power supply, 2.5 V | — | 2.375 | 2.5 | 2.625 | V |
| | I/O power supply, 1.8 V | — | 1.71 | 1.8 | 1.89 | V |
| | I/O power supply, 1.5 V | — | 1.425 | 1.5 | 1.575 | V |
| | I/O power supply, 1.2 V | — | 1.14 | 1.2 | 1.26 | V |
| $V_{CC_CLKIN}$ | Differential clock input power supply (top and bottom I/O banks only) | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCBAT}$ *(3)* | Battery back-up power supply for design security volatile key register | — | 1.0 | — | 3.3 | V |
| $V_I$ | DC Input voltage | — | -0.3 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | For commercial use | 0 | — | 85 | °C |
| | | For industrial use *(2)* | -40 | — | 100 | °C |
| $t_{RAMP}$ | Power Supply Ramptime (For $V_{CCPT}$) | Normal POR (PORSEL=0) | 50 µs | — | 5 ms | — |
| | | Fast POR (PORSEL=1) | 50 µs | — | 5 ms | — |
| | Power Supply Ramptime (For all power supplies except $V_{CCPT}$) | Normal POR (PORSEL=0) | 50 µs | — | 100 ms | — |
| | | Fast POR (PORSEL=1) | 50 µs | — | 12 ms | — |

**Notes to Table 1–3:**

(1) $V_{CCPD}$ is 2.5, 3.0, or 3.3 V. For a 3.3-V I/O standard, $V_{CCPD}$ = 3.3 V. For a 3.0-V I/O standard, $V_{CCPD}$ = 3.0 V. For a 2.5-V or lower I/O standard, $V_{CCPD}$ = 2.5 V.

(2) For the EP3SL340, EP3SE260, and EP3SL200 devices in the I4L ordering code, the industrial junction temperature range is from 0° C to 100° C, regardless of supply voltage.

(3) Altera recommends a 3.0-V nominal battery voltage when connecting $V_{CCBAT}$ to a battery for volatile key backup. If you do not use the volatile security key, you may connect the $V_{CCBAT}$ to either GND or a 3.0-V power supply.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## DC Characteristics

This section lists the input pin capacitances, on-chip termination tolerance, and hot- socketing specifications.

### Supply Current

Standby current is the current the device draws after the device is configured with no inputs/outputs toggling and no activity in the device. Because these currents vary largely with the resources used, use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design.

Table 1–4 lists supply current specifications for $V_{CC_CLKIN}$ and $V_{CCPGM}$. Use the EPE to get supply current estimates for the remaining power supplies.

**Table 1–4.** Supply Current Specifications for $V_{CC_CLKIN}$ and $V_{CCPGM}$

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $I_{CLKIN}$ | $V_{CC_CLKIN}$ current specifications | 0 | 250 | mA |
| $I_{PGM}$ | $V_{CCPGM}$ current specifications | 0 | 250 | mA |

### I/O Pin Leakage Current

Table 1–5 lists Stratix III I/O pin leakage current specifications.

**Table 1–5.** I/O Pin Leakage Current for Stratix III Devices *(Note 1)*, *(2)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input Pin Leakage Current | $V_I = V_{CCIOMAX}$ to 0 V | -10 | — | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O Pin Leakage Current | $V_O = V_{CCIOMAX}$ to 0 V | -10 | — | 10 | µA |

**Notes to Table 1–5:**

(1) This value is specified for normal device operation. The value may vary during power-up. This applies for all $V_{CCIO}$ settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) The 10-µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

### Bus Hold Specifications

Table 1–6 lists the Stratix III device family bus hold specifications.

**Table 1–6.** Bus Hold Parameters for Stratix III Devices (Part 1 of 2)

| Parameter | Symbol | Conditions | $V_{CCIO}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V/3.3 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (maximum) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | µA |
| High sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (minimum) | -22.5 | — | -25.0 | — | -30.0 | — | -50.0 | — | -70.0 | — | µA |
| Low overdrive current | $I_{ODL}$ | $0V < V_{IN} < V_{CCIO}$ | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | µA |

**Table 1–6.** Bus Hold Parameters for Stratix III Devices (Part 2 of 2)

| Parameter | Symbol | Conditions | $V_{CCIO}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V/3.3 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| High overdrive current | $I_{ODH}$ | $0V < V_{IN} < V_{CCIO}$ | — | -120 | — | -160 | — | -200 | — | -300 | — | -500 | µA |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

### On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for the I/Os connected to the calibration block. Table 1–7 lists the Stratix III OCT calibration block accuracy specifications.

**Table 1–7.** On-Chip Termination Calibration Accuracy Specifications for Stratix III Devices *(Note 1)*

| Symbol | Description | Conditions | Calibration Accuracy | | | Unit |
|---|---|---|---|---|---|---|
| | | | C2 | C3, I3 | C4, I4 | |
| 25-Ω $R_S$ *(2)* 3.3, 3.0, 2.5, 1.8, 1.5, 1.2 | Internal series termination with calibration (25-Ω setting) | $V_{CCIO}$ = 3.3, 3.0, 2.5, 1.8, 1.5, 1.2 V | ±8 | ±8 | ±8 | % |
| 50-Ω $R_S$ 3.3, 3.0, 2.5, 1.8, 1.5, 1.2 | Internal series termination with calibration (50-Ω setting) | $V_{CCIO}$ = 3.3, 3.0, 2.5, 1.8, 1.5, 1.2 V | ±8 | ±8 | ±8 | % |
| 50-Ω $R_T$ 2.5, 1.8, 1.5, 1.2 | Internal parallel termination with calibration (50-Ω setting) | $V_{CCIO}$ = 2.5, 1.8, 1.5, 1.2 V | ±10 | ±10 | ±10 | % |
| 20-Ω $R_S$ to 60-Ω $R_S$ 3.3, 3.0, 2.5, 1.8, 1.5, 1.2 | Expanded range for internal series termination with calibration (Between 20-Ω to 60-Ω setting) | $V_{CCIO}$ = 3.3, 3.0, 2.5, 1.8, 1.5, 1.2 V *(3)* | ±10 | ±10 | ±10 | % |
| 25-Ω $R_{S_left_shift}$ | Internal left shift series termination with calibration (25-Ω $R_{S_left_shift}$ setting) | $V_{CCIO}$ = 3.3, 3.0, 2.5, 1.8, 1.5, 1.2 V | ±10 | ±10 | ±10 | % |
| $R_{OCT_CAL}$ | Internal series termination with calibration | *(4)* | | | | |

**Notes to Table 1–7:**

(1) OCT calibration accuracy is valid at the time of calibration only.
(2) 25-Ω $R_S$ not supported for 1.5 V and 1.2 V in Row I/O.
(3) 1.5 V and 1.2 V only supports 40-Ω to 60-Ω expanded range.
(4) For resistance tolerance after power-up calibration, refer to Equation 1–1 and Table 1–9 on page 1–8.

The accuracy listed in Table 1–7 is valid at the time of calibration. If the voltage or temperature changes, the termination resistance value varies. Table 1–8 lists the resistance tolerance for Stratix III OCT.

**Table 1–8.** On-Chip Termination Resistance Tolerance Specification for Stratix III Devices

| Symbol | Description | Conditions | Resistance Tolerance | | | Unit |
|---|---|---|---|---|---|---|
| | | | C2 | C3, I3 | C4, I4 | |
| $R_{OCT_UNCAL}$ | Internal series termination without calibration | — | | | | |
| 25-Ω $R_S$ 3.3, 3.0, 2.5 | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 3.3, 3.0, 2.5 V | ±30 | ±40 | ±40 | % |
| 25-Ω $R_S$ 1.8, 1.5 | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.8, 1.5 V | ±30 | ±50 | ±50 | % |
| 25-Ω $R_S$ 1.2 | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.2 V | ±35 | ±60 | ±60 | % |
| 50-Ω $R_S$ 3.3, 3.0, 2.5 | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 3.3, 3.0, 2.5 V | ±30 | ±40 | ±40 | % |
| 50-Ω $R_S$ 1.8, 1.5 | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.8, 1.5 V | ±30 | ±50 | ±50 | % |
| 50-Ω $R_S$ 1.2 | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.2 V | ±35 | ±60 | ±60 | % |
| $R_D$ | Internal differential termination for LVDS technology (100-Ω setting) | $V_{CCIO}$ = 2.5 V | -15 to 35 | | | % |

Table 1–9 lists OCT variation with temperature and voltage after power-up calibration. Use Table 1–9 and Equation 1–1 to determine OCT variation without re-calibration.

**Equation 1–1.** OCT Variation Without Re-Calibration *(Note 1)*

$$R_{OCT} = R_{SCAL}\left(1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle\right)$$

**Notes to Equation 1–1:**

(1) $R_{OCT}$ value calculated from Equation 1–1 shows the range of OCT resistance with the variation of temperature and $V_{CCIO}$.
(2) $R_{SCAL}$ is the OCT resistance value at power-up.
(3) $\Delta T$ is the variation of temperature with respect to the temperature at power-up.
(4) $\Delta V$ is the variation of voltage with respect to the $V_{CCIO}$ at power-up.
(5) dR/dT is the percentage change of $R_{SCAL}$ with temperature.
(6) dR/dV is the percentage change of $R_{SCAL}$ with voltage.

**Table 1–9.** On-Chip Termination Variation after Power-up Calibration *(Note 1)*

| Symbol | Description | $V_{CCIO}$ (V) | Commercial Typical | Unit |
|---|---|---|---|---|
| dR/dV | OCT variation with voltage without re-calibration | 3 | 0.029 | %/mV |
| | | 2.5 | 0.036 | %/mV |
| | | 1.8 | 0.065 | %/mV |
| | | 1.5 | 0.104 | %/mV |
| | | 1.2 | 0.177 | %/mV |
| dR/dT | OCT variation with temperature without re-calibration | 3 | 0.294 | %/°C |
| | | 2.5 | 0.301 | %/°C |
| | | 1.8 | 0.355 | %/°C |
| | | 1.5 | 0.344 | %/°C |
| | | 1.2 | 0.348 | %/°C |

**Note to Table 1–9:**

(1) Valid for $V_{CCIO}$ range of ± 5% and temperature range of 0° to 85° C.

### Pin Capacitance

Table 1–10 lists the Stratix III device family pin capacitance.

**Table 1–10.** Pin Capacitance for Stratix III Device Family

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $C_{IOTB}$ | Input capacitance on top and bottom I/O pins | 4 | pF |
| $C_{IOLR}$ | Input capacitance on left and right I/O pins | 4 | pF |
| $C_{CLKTB}$ | Input capacitance on top and bottom non-dedicated clock input pins | 4 | pF |
| $C_{CLKLR}$ | Input capacitance on left and right non-dedicated clock input pins | 4 | pF |
| $C_{OUTFB}$ | Input capacitance on dual-purpose clock output and feedback pins | 5 | pF |
| $C_{CLK1}$, $C_{CLK3}$, $C_{CLK8}$, and $C_{CLK10}$ | Input capacitance for dedicated clock input pins | 2 | pF |

### Hot-Socketing

Table 1–11 lists the hot-socketing specifications for Stratix III devices.

**Table 1–11.** Hot-Socketing Specifications for Stratix III Devices

| Symbol | Parameter | Maximum |
|---|---|---|
| $\lvert I_{IOPIN}\rvert$(DC) | DC current per I/O pin | 300 µA |
| $\lvert I_{IOPIN}\rvert$(AC) | AC current per I/O pin | 8 mA *(1)* |

**Note to Table 1–11:**

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $\lvert I_{IOPIN}\rvert$ = C dv/dt, in which C is I/O pin capacitance and dv/dt is the slew rate.

### Internal Weak Pull-Up Resistor

Table 1–12 lists the weak pull-up resistor values for Stratix III devices.

**Table 1–12.** Internal Weak Pull-Up Resistor for Stratix III Devices *(Note 1)*, *(3)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if the programmable pull-up resistor option is enabled | $V_{CCIO}$ = 3.3 V ± 5% *(2)* | — | 25 | — | kΩ |
| | | $V_{CCIO}$ = 3.0 V ± 5% *(2)* | — | 25 | — | kΩ |
| | | $V_{CCIO}$ = 2.5 V ± 5% *(2)* | — | 25 | — | kΩ |
| | | $V_{CCIO}$ = 1.8 V ± 5% *(2)* | — | 25 | — | kΩ |
| | | $V_{CCIO}$ = 1.5 V ± 5% *(2)* | — | 25 | — | kΩ |
| | | $V_{CCIO}$ = 1.2 V ± 5% *(2)* | — | 25 | — | kΩ |

**Notes to Table 1–12:**

(1) All I/O pins have an option to enable weak pull-up except configuration, test, and JTAG pins.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

(3) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25k Ω.

## I/O Standard Specifications

The following tables list input voltage sensitivities ($V_{IH}$ and $V_{IL}$), output voltages ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$) for all I/O standards supported by Stratix III devices. $V_{OL}$ and $V_{OH}$ values are valid at the corresponding $I_{OL}$ and $I_{OH}$, respectively.

Table 1–13 through Table 1–18 list the Stratix III device family I/O standard specifications. Refer to "Glossary" on page 1–326 for an explanation of terms used in the Table 1–14 through Table 1–18.

**Table 1–13.** Single-Ended I/O Standards Specifications

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | IOL (mA) | IOH (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 3.3-V LVTTL | 3.135 | 3.3 | 3.465 | -0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | -2 |
| 3.0-V LVTTL | 2.85 | 3 | 3.15 | -0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | -2 |
| 3.3-V LVCMOS | 3.135 | 3.3 | 3.465 | -0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| 3.0-V LVCMOS | 2.85 | 3 | 3.15 | -0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ - 0.2 | 0.1 | -0.1 |
| 2.5-V LVTTL/ LVCMOS | 2.375 | 2.5 | 2.625 | -0.3 | 0.7 | 1.7 | 3.6 | 0.2 | 2.1 | 0.1 | -0.1 |
| | | 2.5 | 2.625 | -0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | -1 |
| | | 2.5 | 2.625 | -0.3 | 0.7 | 1.7 | 3.6 | 0.7 | 1.7 | 2 | -2 |
| 1.8-V LVTTL / LVCMOS | 1.71 | 1.8 | 1.89 | -0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ - 0.45 | 2 | -2 |
| 1.5-V LVTTL/ LVCMOS | 1.425 | 1.5 | 1.575 | -0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 * $V_{CCIO}$ | 0.75 * $V_{CCIO}$ | 2 | -2 |
| 1.2-V LVTTL / LVCMOS | 1.14 | 1.2 | 1.26 | -0.3 | 0.35 * $V_{CCIO}$ | 0.65 * $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 * $V_{CCIO}$ | 0.75 * $V_{CCIO}$ | 2 | -2 |
| 3.0-V PCI | 2.85 | 3 | 3.15 | — | 0.3 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 3.6 | 0.1 * $V_{CCIO}$ | 0.9 * $V_{CCIO}$ | 1.5 | -0.5 |
| 3.0-V PCI-X | 2.85 | 3 | 3.15 | — | 0.35 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | — | 0.1 * $V_{CCIO}$ | 0.9 * $V_{CCIO}$ | 1.5 | -0.5 |

Refer to the figure in "Single-Ended Voltage Referenced I/O Standard" in the "Glossary" on page 1–326 for voltage referenced receiver input waveform and explanation of terms used in Table 1–14.

**Table 1–14.** Single-Ended SSTL and HSTL I/O Reference Voltage Specifications

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 CLASS I, II | 2.375 | 2.5 | 2.625 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | $V_{REF}$ - 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 CLASS I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ - 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 CLASS I, II | 1.425 | 1.5 | 1.575 | 0.47 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.53 * $V_{CCIO}$ | 0.47 * $V_{CCIO}$ | $V_{REF}$ | 0.53 * $V_{CCIO}$ |
| HSTL-18 CLASS I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}$/2 | — |
| HSTL-15 CLASS I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}$/2 | — |
| HSTL-12 CLASS I, II | 1.14 | 1.2 | 1.26 | 0.47 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.53 * $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |

**Table 1–15.** Single-Ended SSTL and HSTL I/O Standards Signal Specifications *(Note 1)* (Part 1 of 2)

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | IOL (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 CLASS I | -0.3 | $V_{REF}$ - 0.15 | $V_{REF}$ +0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.31 | $V_{REF}$ + 0.31 | VTT - 0.57 | VTT + 0.57 | 8.1 | -8.1 |
| SSTL-2 CLASS II | -0.3 | $V_{REF}$ - 0.15 | $V_{REF}$ +0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ - 0.31 | $V_{REF}$ + 0.31 | VTT - 0.76 | VTT + 0.76 | 16.2 | -16.2 |
| SSTL-18 CLASS I | -0.3 | $V_{REF}$ -0.125 | $V_{REF}$ +0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ -0.25 | $V_{REF}$ + 0.25 | VTT - 0.475 | VTT + 0.475 | 6.7 | -6.7 |
| SSTL-18 CLASS II | -0.3 | $V_{REF}$ -0.125 | $V_{REF}$ +0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ -0.25 | $V_{REF}$ + 0.25 | 0.28 | $V_{CCIO}$ - 0.28 | 13.4 | -13.4 |
| SSTL-15 CLASS I | -0.3 | $V_{REF}$ -0.1 | $V_{REF}$ +0.1 | $V_{CCIO}$ + 0.3 | $V_{REF}$ -0.175 | $V_{REF}$ + 0.175 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | 8 | -8 |
| SSTL-15 CLASS II | -0.3 | $V_{REF}$ -0.1 | $V_{REF}$ +0.1 | $V_{CCIO}$ + 0.3 | $V_{REF}$ -0.175 | $V_{REF}$ + 0.175 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | 16 | -16 |
| HSTL-18 CLASS I | -0.3 | $V_{REF}$ -0.1 | $V_{REF}$ +0.1 | $V_{CCIO}$ + 0.3 | $V_{REF}$ -0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ - 0.4 | 8 | -8 |
| HSTL-18 CLASS II | -0.3 | $V_{REF}$ -0.1 | $V_{REF}$ +0.1 | $V_{CCIO}$ + 0.3 | $V_{REF}$ -0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ - 0.4 | 16 | -16 |
| HSTL-15 CLASS I | -0.3 | $V_{REF}$ -0.1 | $V_{REF}$ +0.1 | $V_{CCIO}$ + 0.3 | $V_{REF}$ -0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ - 0.4 | 8 | -8 |
| HSTL-15 CLASS II | -0.3 | $V_{REF}$ -0.1 | $V_{REF}$ +0.1 | $V_{CCIO}$ + 0.3 | $V_{REF}$ -0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ - 0.4 | 16 | -16 |
| HSTL-12 CLASS I | -0.15 | $V_{REF}$ -0.08 | $V_{REF}$ +0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ -0.15 | $V_{REF}$ + 0.15 | 0.25* $V_{CCIO}$ | 0.75 * $V_{CCIO}$ | 8 | -8 |

**Table 1–15.** Single-Ended SSTL and HSTL I/O Standards Signal Specifications *(Note 1)* (Part 2 of 2)

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | IOL (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| HSTL-12 CLASS II | -0.15 | $V_{REF}$ -0.08 | $V_{REF}$ +0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ -0.15 | $V_{REF}$ + 0.15 | 0.25* $V_{CCIO}$ | 0.75 * $V_{CCIO}$ | 16 | -16 |

**Note to Table 1–15:**

(1) Use the current strength settings that are equal or larger than the $I_{OL}$ and $I_{OH}$ values listed to meet the $V_{OL}$ and $V_{OH}$ specifications for each line. OCT or lower current strengths may provide better signal integrity and lower power.

Refer to the figures for "Differential I/O Standards" in "Glossary" on page 1–326 for the receiver input and transmitter output waveforms, and for all the differential I/O standards (LVDS, mini-LVDS, RSDS). $V_{CC_CLKIN}$ is the power supply for the differential column clock input pins. $V_{CCPD}$ is the power supply for the row I/Os and all other column I/Os.

**Table 1–16.** Differential SSTL I/O Standard Specifications

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{SWING\ (DC)}$ (V) | | $V_{X\ (AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | | $V_{OX\ (AC)}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max | Min | Typ | Max |
| SSTL-2 CLASS I, II | 2.375 | 2.5 | 2.625 | 0.3 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ - 0.2 | — | $V_{CCIO}/2$ + 0.2 | 0.62 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ - 0.15 | — | $V_{CCIO}/2$ + 0.15 |
| SSTL-18 CLASS I, II | 1.71 | 1.8 | 1.89 | 0.25 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ -0.175 | — | $V_{CCIO}/2$ + 0.175 | 0.5 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ -0.125 | — | $V_{CCIO}/2$ +0.125 |
| SSTL-15 CLASS I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | — | $V_{CCIO}/2$ | — | 0.35 | — | — | $V_{CCIO}/2$ | — |

**Table 1–17.** Differential HSTL I/O Standards Specifications

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 CLASS I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 CLASS I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |
| HSTL-12 CLASS I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ + 0.3 | — | 0.5* $V_{CCIO}$ | — | 0.4* $V_{CCIO}$ | 0.5* $V_{CCIO}$ | 0.6* $V_{CCIO}$ | 0.3 | $V_{CCIO}$ + 0.48 |

**Table 1–18.** Differential I/O Standard Specifications (Part 1 of 2)

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (V) *(1)* | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) *(2)* | | | $V_{OCM}$ (V) *(2)* | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| 2.5 V LVDS (Row I/O) | 2.375 | 2.5 | 2.625 | 0.1 | $V_{CM}$ = 1.25 | — | 0.05 *(6)* | $D_{max} \leq 700$ Mbps | 1.8 *(6)* | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| | 2.375 | 2.5 | 2.625 | 0.1 | $V_{CM}$ = 1.25 | — | 1.05 *(6)* | $D_{max} > 700$ Mbps | 1.55 *(6)* | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |

**Table 1–18.** Differential I/O Standard Specifications (Part 2 of 2)

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (V) *(1)* | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) *(2)* | | | $V_{OCM}$ (V) *(2)* | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| 2.5 V LVDS (Column I/O) | 2.375 | 2.5 | 2.625 | 0.1 | $V_{CM}$ = 1.25 | — | 0.05 *(6)* | $D_{max} \leq 700$ Mbps | 1.8 *(6)* | 0.247 | — | 0.6 | 1.0 | 1.25 | 1.5 |
| | 2.375 | 2.5 | 2.625 | 0.1 | $V_{CM}$ = 1.25 | — | 1.05 *(6)* | $D_{max} > 700$ Mbps | 1.55 *(6)* | 0.247 | — | 0.6 | 1.0 | 1.25 | 1.5 |
| RSDS (Row I/O) | 2.375 | 2.5 | 2.625 | 0.1 | $V_{CM}$ = 1.25 | — | 0.3 | — | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| RSDS (Column I/O) | 2.375 | 2.5 | 2.625 | 0.1 | $V_{CM}$ = 1.25 | — | 0.3 | — | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.5 |
| Mini-LVDS (Row I/O) | 2.375 | 2.5 | 2.625 | 0.2 | — | 0.6 | 0.4 | — | 1.325 | 0.25 | — | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS (Column I/O) | 2.375 | 2.5 | 2.625 | 0.2 | — | 0.6 | 0.4 | — | 1.325 | 0.25 | — | 0.6 | 0.5 | 1.2 | 1.5 |
| LVPECL *(3)* | 2.375 *(5)* | 2.5 *(5)* | 2.625 *(5)* | 0.3 | — | — | 0.6 | $D_{max} \leq 700$ Mbps | 1.8 *(4)* | — | — | — | — | — | — |
| | 2.375 *(5)* | 2.5 *(5)* | 2.625 *(5)* | 0.3 | — | — | 1.0 | $D_{max} > 700$ Mbps | 1.6 *(4)* | — | — | — | — | — | — |

**Notes to Table 1–18:**

(1) The minimum $V_{ID}$ value is applicable over the entire common mode range, $V_{CM}$.

(2) RL range: $90 \leq RL \leq 110\ \Omega$.

(3) Column and row I/O banks support LVPECL I/O standards for input operation only on dedicated clock input pins. Differential clock inputs in column I/O use $V_{CC_CLKIN}$ that must be powered by 2.5 V. Differential clock inputs in row I/O banks are powered by $V_{CCPD}$.

(4) The receiver voltage input range for the data rate when $D_{max} > 700$ Mbps is $0.85\ V \leq V_{IN} \leq 1.75\ V$.
The receiver voltage input range for the data rate when $D_{max} \leq 700$ Mbps is $0.45\ V \leq V_{IN} \leq 1.95\ V$.

(5) Power supply for the column I/O LVPECL differential clock input buffer is $V_{CC_CLKIN}$.

(6) The receiver voltage input range for the data rate when $D_{max} > 700$ Mbps is $1.0\ V \leq V_{IN} \leq 1.6\ V$.
The receiver voltage input range for the data rate when $D_{max} \leq 700$ Mbps is zero $V \leq V_{IN} \leq 1.85\ V$.

## Power Consumption

Altera offers two ways to estimate power for a design: the Excel-based Early Power Estimator (EPE) and the Quartus® II **PowerPlay Power Analyzer** feature.

The interactive Excel-based Early Power Estimator is typically used prior to designing the FPGA in order to get a magnitude estimate of the device power. The Quartus II **PowerPlay Power Analyzer** provides estimation based on the specifics of the design after place-and-route is complete. The **PowerPlay Power Analyzer** can apply a combination of user-entered, simulation-derived, and estimated signal activities which, when combined with detailed circuit models, can yield very accurate power estimation.

Refer to Table 1–4 on page 1–5 for supply current estimates for $V_{CCPGM}$ and $V_{CC_CLKIN}$. Use the EPE and PowerPlay Power Analyzer for current estimates of remaining power supplies.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide For Stratix III FPGAs* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

# Switching Characteristics

This section provides performance characteristics of Stratix III core and periphery blocks for commercial grade devices.

These characteristics can be designated as **Preliminary** and **Final** and each designation is defined below.

**Preliminary**—Preliminary characteristics are created using simulation results, process data, and other known parameters.

**Final**—Final numbers are based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. The upper-right hand corner of a table shows the designation as **Preliminary** or **Final**.

## Core Performance Specifications

These sections describe the Clock Tree, PLL, digital signal processing (DSP), TriMatrix, and Configuration and JTAG specifications.

### Clock Tree Specifications

Table 1–19 lists the clock tree performance specifications for the logic array, DSP blocks, and TriMatrix Memory blocks for Stratix III devices.

**Table 1–19.** Clock Tree Performance for Stratix III Devices

| Device | C2 | C3, I3 | C4, I4 | C4L, I4L | | Unit |
|---|---|---|---|---|---|---|
| | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 0.9 V | |
| EP3SL50 | 730 | 700 | 450 | 450 | 375 | MHz |
| EP3SL70 | 730 | 700 | 450 | 450 | 375 | MHz |
| EP3SL110 | 730 | 700 | 450 | 450 | 375 | MHz |
| EP3SL150 | 730 | 700 | 450 | 450 | 375 | MHz |
| EP3SL200 | 730 | 700 | 450 | 450 | 375 | MHz |
| EP3SE260 | 730 | 700 | 450 | 450 | 375 | MHz |
| EP3SL340 | 730 | 700 | 450 | 450 | 375 | MHz |
| EP3SE50 | 730 | 700 | 450 | 450 | 375 | MHz |
| EP3SE80 | 730 | 700 | 450 | 450 | 375 | MHz |
| EP3SE110 | 730 | 700 | 450 | 450 | 375 | MHz |

### PLL Specifications

Table 1–20 lists the Stratix III PLL specifications when operating in both the commercial junction temperature range (0 to 85° C) and the industrial junction temperature range (-40 to 100° C), except for EP3SL340, EP3SE260, and EP3SL200 devices in the I4L ordering code, where the industrial junction temperature range is from 0° C to 100° C, regardless of supply voltage. Refer to the figure in "PLL Specifications" in "Glossary" on page 1–326 for the PLL block diagram.

**Table 1–20.** PLL Specifications for Stratix III Devices (Part 1 of 3)

| Symbol | Parameter | C2 | | | C3, I3 | | | C4, I4 | | | C4L, I4L | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CCL}$ = 1.1 V | | | $V_{CCL}$ = 1.1 V | | | $V_{CCL}$ = 1.1 V | | | $V_{CCL}$ = 1.1 V | | | $V_{CCL}$ = 0.9 V | | | |
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{IN}$ | Input clock frequency | 5 | — | 800 *(1)* | 5 | — | 717 *(1)* | 5 | — | 717 *(1)* | 5 | — | 717 *(1)* | 5 | — | 717 *(1)* | MHz |
| $f_{INPFD}$ | Input frequency to the PFD | 5 | — | 325 | 5 | — | 325 | 5 | — | 325 | 5 | — | 325 | 5 | — | 325 | MHz |
| $f_{VCO}$ | PLL VCO operating range | 600 | — | 1600 | 600 | — | 1300 | 600 | — | 1300 | 600 | — | 1300 | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | 40 | — | 60 | 40 | — | 60 | 40 | — | 60 | 40 | — | 60 | % |
| $f_{OUT}$ | Output frequency for internal global or regional clock | — | — | 600 *(2)* | — | — | 500 *(2)* | — | — | 450 *(2)* | — | — | 450 *(2)* | — | — | 375 *(2)* | MHz |
| $f_{OUT_EXT}$ | Output frequency for dedicated external clock output | — | — | 800 *(2)* | — | — | 717 *(2)* | — | — | 717 *(2)* | — | — | 717 *(2)* | — | — | 717 *(2)* | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{FCOMP}$ | External feedback clock compensation time | — | — | 10 | — | — | 10 | — | — | 10 | — | — | 10 | — | — | 10 | ns |
| $t_{CONFIGPLL}$ | Time required to reconfigure scan chain | — | 3.5 | — | — | 3.5 | — | — | 3.5 | — | — | 3.5 | — | — | 3.5 | — | scanclk cycles |
| $t_{CONFIGPHASE}$ | Time required to reconfigure phase shift | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | scanclk cycles |
| $f_{SCANCLK}$ | `scanclk` frequency | — | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from end of device configuration | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | — | — | 1 | ms |


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**Table 1–20.** PLL Specifications for Stratix III Devices (Part 2 of 3)

| Symbol | Parameter | C2 | | | C3, I3 | | | C4, I4 | | | C4L, I4L | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CCL}$ = 1.1 V | | | $V_{CCL}$ = 1.1 V | | | $V_{CCL}$ = 1.1 V | | | $V_{CCL}$ = 1.1 V | | | $V_{CCL}$ = 0.9 V | | | |
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{CLBW}$ | PLL closed-loop low bandwidth | — | 0.3 | — | — | 0.3 | — | — | 0.3 | — | — | 0.3 | — | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | — | 1.5 | — | — | 1.5 | — | — | 1.5 | — | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth *(6)* | — | 4 | — | — | 4 | — | — | 4 | — | — | 4 | — | — | 4 | — | MHz |
| $t_{PLL_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | — | — | ±50 | — | — | ±50 | — | — | ±50 | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on areset signal | 10 | — | — | 10 | — | — | 10 | — | — | 10 | — | — | 10 | — | — | ns |
| $t_{INCCJ}$ *(3)*, *(4)* | Input clock cycle to cycle jitter ($F_{REF} \geq 100$ MHz) | — | — | 0.15 | — | — | 0.15 | — | — | 0.15 | — | — | 0.15 | — | — | 0.1 | UI (p-p) |
| | Input clock cycle to cycle jitter ($F_{REF} < 100$ MHz) | — | — | ±750 | — | — | ±750 | — | — | ±750 | — | — | ±750 | — | — | ±500 | ps (p-p) |
| $t_{OUTPJ_DC}$ *(5)* | Period Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz) | — | — | 175 | — | — | 175 | — | — | 175 | — | — | 175 | — | — | 225 | ps (p-p) |
| | Period Jitter for dedicated clock output ($F_{OUT} < 100$ MHz) | — | — | 17.5 | — | — | 17.5 | — | — | 17.5 | — | — | 17.5 | — | — | 22.5 | mUI (p-p) |
| $t_{OUTCCJ_DC}$ *(5)* | Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz) | — | — | 175 | — | — | 175 | — | — | 175 | — | — | 175 | — | — | 225 | ps (p-p) |
| | Cycle to Cycle Jitter for dedicated clock output ($F_{OUT} < 100$ MHz) | — | — | 17.5 | — | — | 17.5 | — | — | 17.5 | — | — | 17.5 | — | — | 22.5 | mUI (p-p) |
| $t_{OUTPJ_IO}$ *(5)*, *(8)* | Period Jitter for clock output on regular IO ($F_{OUT} \geq 100$ MHz) | — | — | 600 | — | — | 600 | — | — | 600 | — | — | 600 | — | — | 750 | ps (p-p) |
| | Period Jitter for clock output on regular IO ($F_{OUT} < 100$ MHz) | — | — | 60 | — | — | 60 | — | — | 60 | — | — | 60 | — | — | 75 | mUI (p-p) |

**Table 1–20.** PLL Specifications for Stratix III Devices (Part 3 of 3)

| Symbol | Parameter | C2 | | | C3, I3 | | | C4, I4 | | | C4L, I4L | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CCL}$ = 1.1 V | | | $V_{CCL}$ = 1.1 V | | | $V_{CCL}$ = 1.1 V | | | $V_{CCL}$ = 1.1 V | | | $V_{CCL}$ = 0.9 V | | | |
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{OUTCCJ_IO}$ *(5)*, *(8)* | Cycle to Cycle Jitter for clock output on regular IO ($F_{OUT} \geq 100$ MHz) | — | — | 600 | — | — | 600 | — | — | 600 | — | — | 600 | — | — | 750 | ps (p-p) |
| | Cycle to Cycle Jitter for clock output on regular IO ($F_{OUT} < 100$ MHz) | — | — | 60 | — | — | 60 | — | — | 60 | — | — | 60 | — | — | 75 | mUI (p-p) |
| $t_{CASC_OUTPJ_DC}$ *(5)*, *(7)* | Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq$ 100 MHz) | — | — | 250 | — | — | 250 | — | — | 250 | — | — | 250 | — | — | 325 | ps (p-p) |
| | Period Jitter for dedicated clock output in cascaded PLLs ($F_{OUT}$ <100 MHz) | — | — | 25 | — | — | 25 | — | — | 25 | — | — | 25 | — | — | 32.5 | mUI (p-p) |
| $f_{DRIFT}$ | Frequency drift after PFDENA is disabled for duration of 100 µs | — | — | ±10 | — | — | ±10 | — | — | ±10 | — | — | ±10 | — | — | ±10 | % |

**Notes to Table 1–20:**

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O $f_{max}$ or $f_{out}$ of the PLL.

(3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source, which is less than 120 ps.

(4) $F_{REF}$ is fIN/N when N = 1.

(5) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied.

(6) High bandwidth PLL settings are not supported in external feedback mode.

(7) The cascaded PLL specification is only applicable with the following conditions:
a) Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
b) Downstream PLL: Downstream PLL BW > 2 MHz

(8) External memory interface clock output jitter specifications use a different measurement method and are available in Table 1–33 on page 1–29.


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## DSP Block Specifications

Table 1–21 lists the Stratix III DSP block performance specifications.

**Table 1–21.** DSP Block Performance Specifications for Stratix III Devices *(Note 1)*

| Mode | Number of Multipliers | C2 *(5)* | C3 | C4 | C4L | | I3 | I4 | I4L | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 9×9-bit multiplier (a, c, e, g) *(2)* | 1 | 440 | 365 | 315 | 315 | 240 | 345 | 315 | 225 | MHz |
| 9×9-bit multiplier (b, d, f, h) *(2)* | 1 | 500 | 410 | 375 | 375 | 270 | 385 | 375 | 250 | MHz |
| 12×12-bit multiplier (a, e) *(3)* | 1 | 440 | 365 | 315 | 315 | 240 | 345 | 315 | 225 | MHz |
| 12×12-bit multiplier (b, d, f, h) *(3)* | 1 | 500 | 410 | 375 | 375 | 270 | 385 | 375 | 250 | MHz |
| 18×18-bit multiplier | 1 | 600 | 495 | 440 | 440 | 320 | 470 | 440 | 300 | MHz |
| 36×36-bit multiplier | 1 | 440 | 365 | 315 | 315 | 220 | 345 | 315 | 205 | MHz |
| Double mode | 1 | 440 | 365 | 315 | 315 | 220 | 345 | 315 | 205 | MHz |
| 18×18-bit multiply adder | 2 | 490 | 405 | 345 | 345 | 250 | 380 | 345 | 235 | MHz |
| 18×18-bit multiply adder | 4 | 490 | 405 | 345 | 345 | 250 | 380 | 345 | 235 | MHz |
| 18×18-bit multiply adder with loop back | 2 | 490 | 405 | 345 | 345 | 250 | 380 | 345 | 235 | MHz |
| 18×18-bit multiply adder with loop back *(4)* | 2 | 390 | 320 | 300 | 240 | 180 | 300 | 300 | 135 | MHz |
| 18×18-bit multiply accumulator | 4 | 475 | 390 | 330 | 330 | 240 | 370 | 330 | 225 | MHz |
| 18×18-bit multiply adder with chainout | 4 | 475 | 390 | 330 | 330 | 240 | 370 | 330 | 225 | MHz |
| Input Cascade Independent output of four 18×18 bit multiplier | 4 | 550 | 455 | 415 | 415 | 270 | 430 | 415 | 250 | MHz |
| 36-bit shift (32 bit data) | 1 | 475 | 390 | 330 | 330 | 250 | 370 | 330 | 235 | MHz |

**Notes to Table 1–21:**

(1) Maximum is for a fully pipelined block with **Round** and **Saturation** disabled.

(2) The DSP block implements eight independent 9b×9b multiplies using a, b, c, d for the top DSP half block and e, f, g, h for the bottom DSP half block multipliers.

(3) The DSP block implements six independent 12b×12b multiplies using a, b, d for the top DSP half block and e, f, h for the bottom DSP half block multipliers.

(4) Maximum for loopback input registers disabled, **Round** and **Saturation** disabled, pipeline and output registers enabled.

(5) The $F_{max}$ for the EP3SL200, EP3SE260, and EP3SL340 devices at the C2 speed grade is 7% slower than the C2 values shown in the table.

## TriMatrix Memory Block Specifications

Table 1–22 lists the Stratix III TriMatrix Memory Block specifications.

**Table 1–22.** TriMatrix Memory Block Performance Specifications for Stratix III Devices *(Note 1)* (Part 1 of 3)

| Memory Block Type | Mode | ALUTs | TriMatrix Memory | C2 *(6)* | C3 | C4 | C4L | | I3 | I4 | I4L | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| MLAB | Single port 16 × 10 | 0 | 1 | 600 | 500 | 450 | 450 | 340 | 475 | 450 | 320 | MHz |
| | Simple dual-port 16 × 20 | 0 | 1 | 600 | 500 | 450 | 450 | 340 | 475 | 450 | 320 | MHz |
| | ROM 64 × 10 | 0 | 1 | 600 | 500 | 450 | 450 | 370 | 475 | 450 | 350 | MHz |
| | ROM 32 × 20 | 0 | 1 | 600 | 500 | 450 | 450 | 340 | 475 | 450 | 320 | MHz |
| M9K *(2)* | Single-port 8K × 1 | 0 | 1 | 550 | 465 | 390 | 390 | 245 | 440 | 390 | 230 | MHz |
| | Single-port 4K × 2 or 2K × 4 | 0 | 1 | 575 | 485 | 405 | 405 | 255 | 460 | 405 | 230 | MHz |
| | Single-port 1K × 9, 512 × 18, or 256 × 36 | 0 | 1 | 565 | 475 | 395 | 395 | 245 | 450 | 395 | 220 | MHz |
| | Simple dual-port, 8K × 1 | 0 | 1 | 545 | 460 | 385 | 385 | 240 | 435 | 385 | 225 | MHz |
| | Simple dual-port, 4K × 2 or 2K × 4 | 0 | 1 | 570 | 480 | 400 | 400 | 250 | 455 | 400 | 225 | MHz |
| | Simple dual-port, 1K × 9, 512 × 18, or 256 × 36 | 0 | 1 | 565 | 475 | 395 | 395 | 245 | 450 | 395 | 220 | MHz |
| | Simple dual-port, 8K × 1, 4K × 2 or 2K × 4 with read-during-write option set to **Old Data** | 0 | 1 | 375 | 312 | 265 | 265 | 205 | 295 | 265 | 185 | MHz |
| | Simple dual-port, 1K × 9, 512 × 18, 256 × 36 with read-during-write option set to **Old Data** | 0 | 1 | 375 | 312 | 265 | 265 | 200 | 295 | 265 | 180 | MHz |
| | True dual-port, 8K × 1 | 0 | 1 | 530 | 440 | 370 | 370 | 230 | 420 | 370 | 215 | MHz |
| | True dual-port, 4K × 2 or 2K × 4 | 0 | 1 | 550 | 460 | 385 | 385 | 240 | 435 | 385 | 215 | MHz |
| | True dual-port, 1K × 9 or 512 × 18 | 0 | 1 | 545 | 460 | 380 | 380 | 235 | 435 | 380 | 210 | MHz |
| | True dual-port, 8K × 1, 4K × 2, or 2K × 4 with read-during-write option set to **Old Data** | 0 | 1 | 350 | 295 | 245 | 245 | 175 | 280 | 245 | 160 | MHz |
| | True dual-port, 1K × 9 or 512 × 18 with read-during-write option set to **Old Data** | 0 | 1 | 340 | 285 | 240 | 240 | 165 | 270 | 240 | 150 | MHz |
| | ROM 1P, 8K × 1, 4K × 2, or 2K × 4 | 0 | 1 | 580 | 485 | 405 | 405 | 260 | 460 | 405 | 235 | MHz |
| | ROM 1P, 1K × 9, 512 × 18, or 256 × 36 | 0 | 1 | 575 | 485 | 405 | 405 | 255 | 460 | 405 | 230 | MHz |
| | ROM 2P, 8K × 1, 4K × 2, or 2K × 4 | 0 | 1 | 580 | 485 | 405 | 405 | 265 | 460 | 405 | 240 | MHz |
| | ROM 2P, 1K × 9, or 512 × 18 | 0 | 1 | 575 | 485 | 405 | 405 | 260 | 460 | 405 | 235 | MHz |
| | Min Pulse Width (Clock High Time) | — | — | 800 | 1000 | 1100 | 1100 | 1800 | 1000 | 1100 | 1800 | ps |
| | Min Pulse Width (Clock Low Time) | — | — | 500 | 625 | 690 | 690 | 1100 | 625 | 690 | 1100 | ps |

**Table 1–22.** TriMatrix Memory Block Performance Specifications for Stratix III Devices *(Note 1)* (Part 2 of 3)

| Memory Block Type | Mode | ALUTs | TriMatrix Memory | C2 *(6)* | C3 | C4 | C4L | | I3 | I4 | I4L | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| M144K *(3)*, *(4)* | True dual-port 16K × 9 or 8K × 18 | 0 | 1 | 350 | 300 | 245 | 245 | 180 | 280 | 245 | 170 | MHz |
| | True dual-port 4K × 36 | 0 | 1 | 520 | 430 | 365 | 365 | 250 | 405 | 365 | 235 | MHz |
| | Simple dual-port 16K × 9 or 8K × 18 | 0 | 1 | 350 | 300 | 245 | 245 | 180 | 280 | 245 | 170 | MHz |
| | Simple dual-port 4K × 36 or 2K × 72 | 0 | 1 | 565 | 470 | 395 | 395 | 225 | 440 | 395 | 210 | MHz |
| | ROM 1Port | 0 | 1 | 580 | 470 | 425 | 425 | 260 | 470 | 425 | 260 | MHz |
| | ROM 2 Port | 0 | 1 | 545 | 450 | 380 | 380 | 260 | 425 | 380 | 245 | MHz |
| | Single-port 16K × 9 or 8K × 18 | 0 | 1 | 385 | 330 | 270 | 270 | 240 | 310 | 270 | 195 | MHz |
| | Single-port 4K × 36 | 0 | 1 | 580 | 470 | 425 | 425 | 210 | 470 | 425 | 195 | MHz |
| | True dual-port 16K × 9, 8K × 18, or 4K × 36 with read-during-write option set to **Old Data** | 0 | 1 | 325 | 270 | 225 | 225 | 165 | 255 | 225 | 155 | MHz |
| | Simple dual-port 16K × 9, 8K × 18, 4K × 36, or 2K × 72 with read-during-write option set to "Old Data" | 0 | 1 | 350 | 292 | 250 | 250 | 200 | 275 | 250 | 190 | MHz |
| | Simple dual-port 2K × 64 (with ECC) | 0 | 1 | 255 | 210 | 180 | 180 | 130 | 195 | 180 | 120 | MHz |
| | Min Pulse Width (Clock High Time) | — | — | 800 | 1000 | 1100 | 1100 | 1800 | 1000 | 1100 | 1800 | ps |
| | Min Pulse Width (Clock Low Time) | — | — | 500 | 625 | 690 | 690 | 1100 | 625 | 690 | 1100 | ps |
| M144K *(3)*, *(5)* | True dual-port 16K × 9 or 8K × 18 | 0 | 1 | 425 | 360 | 300 | 300 | 210 | 340 | 300 | 195 | MHz |
| | True dual-port 4K × 36 | 0 | 1 | 520 | 430 | 365 | 365 | 250 | 405 | 365 | 235 | MHz |
| | Simple dual-port 16K × 9 or 8K × 18 | 0 | 1 | 425 | 360 | 300 | 300 | 210 | 340 | 300 | 195 | MHz |
| | Simple dual-port 4K × 36 or 2K × 72 | 0 | 1 | 565 | 470 | 395 | 395 | 225 | 440 | 395 | 210 | MHz |
| | ROM 1Port | 0 | 1 | 580 | 470 | 425 | 425 | 260 | 470 | 425 | 260 | MHz |
| | ROM 2 Port | 0 | 1 | 545 | 450 | 380 | 380 | 260 | 425 | 380 | 245 | MHz |
| | Single-port 16K × 9 or 8K × 18 | 0 | 1 | 475 | 405 | 335 | 335 | 210 | 380 | 335 | 195 | MHz |
| | Single-port 4K × 36 | 0 | 1 | 580 | 470 | 425 | 425 | 210 | 470 | 425 | 195 | MHz |
| | True dual-port 16K × 9, 8K × 18, or 4K × 36 with read-during-write option set to **Old Data** | 0 | 1 | 325 | 270 | 225 | 225 | 165 | 255 | 225 | 155 | MHz |
| | Simple dual-port 16K × 9, 8K × 18, 4K × 36, or 2K × 72 with read-during-write option set to **Old Data** | 0 | 1 | 350 | 292 | 250 | 250 | 200 | 275 | 250 | 190 | MHz |

**Table 1–22.** TriMatrix Memory Block Performance Specifications for Stratix III Devices *(Note 1)* (Part 3 of 3)

| Memory Block Type | Mode | ALUTs | TriMatrix Memory | C2 *(6)* | C3 | C4 | C4L | | I3 | I4 | I4L | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| M144K *(3)*, *(5)* | Simple dual-port 2K × 64 (with ECC) | 0 | 1 | 255 | 210 | 180 | 180 | 130 | 195 | 180 | 120 | MHz |
| | Min Pulse Width (Clock High Time) | — | — | 800 | 1000 | 1100 | 1100 | 1800 | 1000 | 1100 | 1800 | ps |
| | Min Pulse Width (Clock Low Time) | — | — | 500 | 625 | 690 | 690 | 1100 | 625 | 690 | 1100 | ps |

**Notes to Table 1–22:**

(1) Use a memory block clock that comes through global clock routing from an on-chip PLL set to 50% output duty cycle to achieve the maximum memory block performance. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) The $F_{max}$ shown for M9K degrades 2% when you use the Error Detection CRC feature on the device, except for the C4L speed grade with $V_{CCL}$ = 0.9 V. For the C4L speed grade with $V_{CCL}$ = 0.9V, there is no degradation in $F_{max}$ when you use the Error Detection CRC feature.

(3) The $F_{max}$ shown for M144K degrades 10 MHz when you use byte-enable support on M144K.

(4) $F_{max}$ is applicable when the **COMPTABILITY** option is turned ON.

(5) $F_{max}$ is applicable when the **COMPTABILITY** option is turned OFF. This option is turned ON by default in Quartus II software.

(6) The $F_{max}$ for the EP3SL200, EP3SE260, and EP3SL340 devices at the C2 speed grade is 7% slower than the C2 values shown in the table.

## Configuration and JTAG Specifications

Table 1–23 lists the Stratix III configuration mode specifications.

**Table 1–23.** Configuration Mode Specifications for Stratix III Devices *(Note 1)*

| Programming Mode | DCLK $F_{max}$ | Unit |
|---|---|---|
| Passive Serial | 100 | MHz |
| Fast Passive Parallel *(2)* | 100 | MHz |
| Fast Active Serial *(3)* | 40 | MHz |

**Notes to Table 1–23:**

(1) DCLK $F_{max}$ is restricted when you enable the Remote Update feature. For more information, refer to the *Remote Update Circuitry (ALTREMOTE_UPDATE) Megafunction User Guide*.

(2) The data rate must be 4× slower than the clock when you use decompression and/or encryption.

(3) For more information about the minimum and typical DCLK $F_{max}$ value in Fast Active Serial configuration, refer to the *Configuring Stratix III Devices* chapter.

Table 1–24 lists the JTAG timing parameters and values for Stratix III devices. Refer to the figure for "HIGH-SPEED I/O Block" in the "Glossary" on page 1–326 for the JTAG timing requirements.

**Table 1–24.** JTAG Timing Parameters and Values for Stratix III Devices

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 30 | — | ns |
| $t_{JCH}$ | TCK clock high time | 14 | — | ns |
| $t_{JCL}$ | TCK clock low time | 14 | — | ns |
| $t_{JPSU}$ (TDI) | JTAG port setup time for TDI | 1 | — | ns |
| $t_{JPSU}$ (TMS) | JTAG port setup time for TMS | 3 | — | ns |
| $t_{JPH}$ | JTAG port hold time | 5 | — | ns |
| $t_{JPCO}$ | JTAG port clock to output | — | 11 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | — | 14 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | — | 14 | ns |

## Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfacing, such as the LVDS high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. For example, Stratix III devices I/O configured with voltage referenced I/O standards can achieve up to the stated system interfacing speed as indicated in "External Memory Interface Specifications" on page 1–25. General-purpose I/O standards such as 3.3, 3.0, 2.5, 1.8, or 1.5 LVTTL/LVCMOS are capable of typical 167 MHz and 1.2 LVCMOS at 100MHz interfacing frequency with 10pF load.

Actual achievable frequency depends on design- and system-specific factors. You must perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

### High-Speed I/O Specifications

Refer to the "Glossary" on page 1–326 for the definitions of the high-speed timing specifications.

Table 1–25 lists the true and emulated LVDS specifications for Stratix III devices.

**Table 1–25.** True and Emulated LVDS Specifications for Stratix III Devices *(Note 1)*, *(2)* (Part 1 of 3)

| Symbol | Conditions | C2 | | | C3, I3 | | | C4, I4 | | | C4L, I4L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK_in}$ (input clock frequency)—True Differential I/O Standards | Clock boost factor W = 1 to 40 *(3)* | 5 | — | 800 | 5 | — | 717 | 5 | — | 717 | 5 | — | 717 | MHz |
| $f_{HSCLK_in}$ (input clock frequency)—Single Ended I/O Standards *(9)* | Clock boost factor W = 1 to 40 *(3)* | 5 | — | 800 | 5 | — | 717 | 5 | — | 717 | 5 | — | 717 | MHz |
| $f_{HSCLK_out}$ (output clock frequency) | — | 5 | — | 800 *(7)* | 5 | — | 717 *(7)* | 5 | — | 717 *(7)* | 5 | — | 717 *(7)* | MHz |
| **Transmitter** | | | | | | | | | | | | | | |
| $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 *(8)* | *(4)* | — | 1600 | *(4)* | — | 1250 | *(4)* | — | 1250 | *(4)* | — | 1250 | Mbps |
| | SERDES factor J = 2, Uses DDR Register | *(4)* | — | *(4)* | *(4)* | — | *(4)* | *(4)* | — | *(4)* | *(4)* | — | *(4)* | Mbps |
| | SERDES factor J = 1, Uses SDR Register | *(4)* | — | *(4)* | *(4)* | — | *(4)* | *(4)* | — | *(4)* | *(4)* | — | *(4)* | Mbps |
| LVDS_E_3R -$f_{HSDR}$ (data rate) | SERDES factor J = 4 to 10 | *(4)* | — | 1100 | *(4)* | — | 1100 | *(4)* | — | 800 | *(4)* | — | 800 | Mbps |

**Table 1–25.** True and Emulated LVDS Specifications for Stratix III Devices *(Note 1)*, *(2)* (Part 2 of 3)

| Symbol | Conditions | C2 | | | C3, I3 | | | C4, I4 | | | C4L, I4L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| LVDS_E_1R -$f_{HSDR}$ (data rate) | SERDES factor J = 4 to 10 | *(4)* | — | 311 | *(4)* | — | 200 | *(4)* | — | 200 | *(4)* | — | 200 | Mbps |
| $t_{x\ Jitter}$ *(5)* | Total Jitter for Data Rate, 600 Mbps – 1.6 Gbps | — | — | 160 | — | — | 160 | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate, < 600 Mbps | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| $t_{DUTY}$ | $T_X$ output duty cycle for both True and Emulated Differential I/O | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{RISE}$ & $t_{FALL}$ | True Differential I/O Standards | — | — | 160 | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| $t_{RISE}$ & $t_{FALL}$ | Emulated Differential I/O Standards with Three External Output Resistor Network | — | — | 310 | — | — | 310 | — | — | 350 | — | — | 350 | ps |
| $t_{RISE}$ & $t_{FALL}$ | Emulated Differential I/O Standards with One External Output Resistor Network | — | — | 460 | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| TCCS | True Differential I/O Standards | — | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | ps |
| TCCS | Emulated Differential I/O Standards | — | — | 250 | — | — | 250 | — | — | 250 | — | — | 250 | ps |
| **Receiver** | | | | | | | | | | | | | | |
| $f_{HSDRDPA}$ (data rate) | SERDES factor J = 3 to 10 | 150 | — | 1600 | 150 | — | 1250 | 150 | — | 1250 | 150 | — | 1250 | Mbps |
| $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | *(4)* | — | *(6)* | *(4)* | — | *(6)* | *(4)* | — | *(6)* | *(4)* | — | *(6)* | Mbps |
| | SERDES factor J = 2, Uses DDR Registers | *(4)* | — | *(6)* | *(4)* | — | *(6)* | *(4)* | — | *(6)* | *(4)* | — | *(6)* | Mbps |
| | SERDES factor J = 1, Uses an SDR Register | *(4)* | — | *(6)* | *(4)* | — | *(6)* | *(4)* | — | *(6)* | *(4)* | — | *(6)* | Mbps |
| DPA | | | | | | | | | | | | | | |
| DPA run length | — | — | — | 10000 | — | — | 10000 | — | — | 10000 | — | — | 10000 | UI |
| Soft CDR mode | | | | | | | | | | | | | | |
| Soft-CDR PPM tolerance | — | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ± PPM |


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**Table 1–25.** True and Emulated LVDS Specifications for Stratix III Devices *(Note 1)*, *(2)* (Part 3 of 3)

| Symbol | Conditions | C2 | | | C3, I3 | | | C4, I4 | | | C4L, I4L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Non DPA Mode** | | | | | | | | | | | | | | |
| Sampling Window | — | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ps |

**Notes to Table 1–25:**

(1) When J = 3 to 10, the SERDES block is used.

(2) When J = 1 or 2, the SERDES block is bypassed.

(3) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(4) The minimum and maximum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) used. The I/O differential buffer and input register do not have a minimum toggle rate.

(5) The $t_{xJitter}$ specification is for the true LVDS I/O standard only.

(6) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. Consider the board skew margin, transmitter delay margin, as well as the receiver sampling margin to determine the maximum data rate supported.

(7) This is achieved by using the LVDS and DPA clock network.

(8) If the receiver (with DPA enabled) and the transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(9) This is only applied to DPA and Soft-CDR modes.

Table 1–26 lists the DPA lock time specifications for Stratix III devices.

**Table 1–26.** DPA Lock Time Specifications for Stratix III Devices *(Note 1)*, *(2)*, *(3)* (Part 1 of 2)

| Standard | Training Pattern | Number of Data Transitions in one Repetition of Training Pattern | Number of repetitions per 256 Data Transition *(4)* | Condition *(5)* | Min | Typ | Max |
|---|---|---|---|---|---|---|---|
| SPI-4 | 0000000000 1111111111 | 2 | 128 | without DPA PLL calibration | 256 data transitions | — | — |
| | | | | with DPA PLL calibration | 3×256 data transitions + 2×96 slow clock cycles *(6)* | — | — |
| Parallel Rapid I/O | 00001111 | 2 | 128 | without DPA PLL calibration | 256 data transitions | — | — |
| | | | | with DPA PLL calibration | 3×256 data transitions + 2×96 slow clock cycles *(6)* | — | — |
| | 10010000 | 4 | 64 | without DPA PLL calibration | 256 data transitions | — | — |
| | | | | with DPA PLL calibration | 3×256 data transitions + 2×96 slow clock cycles *(6)* | — | — |

**Table 1–26.** DPA Lock Time Specifications for Stratix III Devices *(Note 1)*, *(2)*, *(3)* (Part 2 of 2)

| Standard | Training Pattern | Number of Data Transitions in one Repetition of Training Pattern | Number of repetitions per 256 Data Transition *(4)* | Condition *(5)* | Min | Typ | Max |
|---|---|---|---|---|---|---|---|
| Miscellaneous | 10101010 | 8 | 32 | without DPA PLL calibration | 256 data transitions | — | — |
| | | | | with DPA PLL calibration | 3×256 data transitions + 2×96 slow clock cycles *(6)* | — | — |
| | 01010101 | 8 | 32 | without DPA PLL calibration | 256 data transitions | — | — |
| | | | | with DPA PLL calibration | 3×256 data transitions + 2×96 slow clock cycles *(6)* | — | — |

**Notes to Table 1–26:**

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) These are the number of repetitions for the stated training pattern to achieve 256 data transitions.

(5) Altera recommends PLL re-calibration for the situations below to guarantee DPA locking:

- Sparse data transitions. For example: Repeating sequences of ten 1s and ten 0s.
- 0 PPM frequency difference and/or 0° phase difference between the clock and data.

(6) Slow clock = data rate (Hz)/ Deserialization factor.

Figure 1–2 shows the DPA time specification with DPA PLL calibration enabled.

**Figure 1–2.** DPA Lock Time Specification with DPA PLL Calibration Enabled

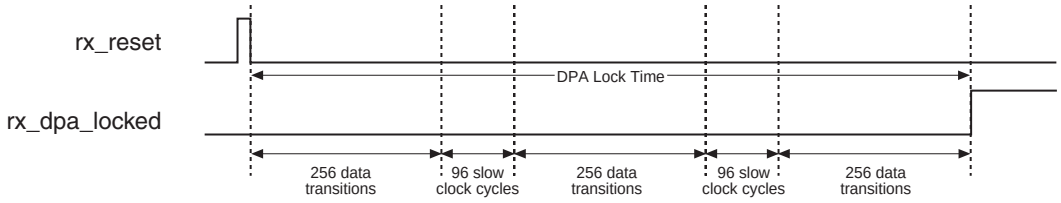


Figure 1–3 shows the LVDS Soft-CDR/ DPA sinusoidal jitter tolerance specifications for Stratix III devices.

**Figure 1–3.** LVDS Soft-CDR/DPA Sinusiodal Jitter Tolerance Specification for Stratix III Devices

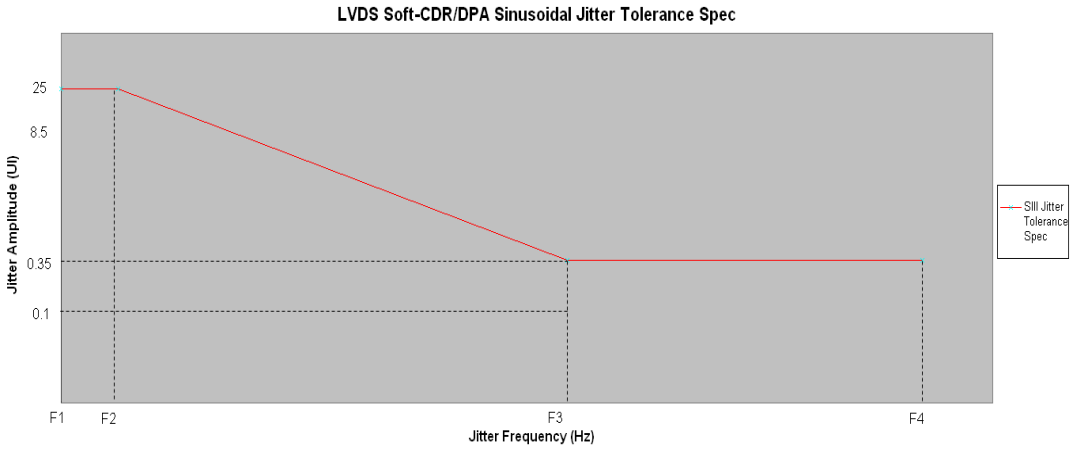



Table 1–27 lists the LVDS Soft-CDR/ DPA sinusiodal jitter mask values for Stratix III devices.

**Table 1–27.** LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for Stratix III Devices

| Jitter Frequency (Hz) | | Jitter Amplitude | Unit |
|---|---|---|---|
| F1 | 10,000 | 25.000 | UI |
| F2 | 17,565 | 25.000 | UI |
| F3 | 1,493,000 | 0.350 | UI |
| F4 | 50,000,000 | 0.350 | UI |

## External Memory Interface Specifications

The following sections describe the external memory I/O timing specifications and the DLL and DQS block specifications.

For more information about the maximum clock rate support for external memory interfaces with a half-rate or full-rate controller, refer to *Section III: System Performance Specifications* of the *External Memory Interfaces Handbook*.

### External Memory I/O Timing Specifications

Table 1–28 and Table 1–29 list Stratix III device timing uncertainties on the read and write data paths. Use these specifications to determine timing margins for source synchronous paths between the Stratix III FPGA and the external memory device. For more information, refer to the figure for "SW (sampling window)" in the "Glossary" on page 1–326.

**Table 1–28.** Sampling Window (SW)—Read Side *(Note 1)*

| Memory Type | I/O Standard | Width | C2 | | C3, I3 | | C4, I4 | | C4L, I4L | | C4L, I4L | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CCL}$ = 1.1 V | | $V_{CCL}$ = 1.1 V | | $V_{CCL}$ = 1.1 V | | $V_{CCL}$ = 1.1 V | | $V_{CCL}$ = 0.9 V | |
| | | | SW (ps) | | SW (ps) | | SW (ps) | | SW (ps) | | SW (ps) | |
| | | | Setup | Hold | Setup | Hold | Setup | Hold | Setup | Hold | Setup | Hold |
| DDR3 SDRAM (with 8 or 10 tap phase offset, 300 MHz–400 MHz) | 1.5-V SSTL | ×4, ×8 | 172 | 296 | 234 | 296 | 257 | 311 | 257 | 311 | 257 | 311 |
| DDR3 SDRAM (with Deskew circuitry, 401 MHz–533 MHz) | 1.5-V SSTL | ×4, ×8 | 300 | 213 | — | — | — | — | — | — | — | — |
| DDR3 SDRAM (Non-leveling interface) | 1.5-V SSTL | ×4, ×8 | 172 | 296 | 234 | 296 | 257 | 311 | 257 | 311 | 257 | 311 |
| DDR2 SDRAM Differential DQS | 1.8-V SSTL | ×4, ×8 | 181 | 306 | 234 | 326 | 257 | 326 | 257 | 326 | 257 | 326 |
| DDR2 SDRAM Single-ended DQS | 1.8-V SSTL | ×4, ×8 | 231 | 256 | 284 | 276 | 307 | 276 | 307 | 276 | 307 | 276 |
| DDR SDRAM Single-ended DQS | 2.5-V SSTL | ×4, ×8 | 231 | 256 | 284 | 261 | 307 | 261 | 307 | 261 | 307 | 261 |
| QDRII/II+ SRAM | 1.5-V HSTL | ×9, ×18, ×36 | 261 | 286 | 314 | 291 | 337 | 291 | 337 | 291 | 337 | 291 |
| QDRII/II+ SRAM Emulation *(2)* | 1.5-V HSTL | ×36 | 261 | 328 | 314 | 337 | 337 | 350 | 337 | 350 | 337 | 350 |
| QDRII/II+ SRAM | 1.8-V HSTL | ×9, ×18, ×36 | 261 | 286 | 314 | 291 | 337 | 291 | 337 | 291 | 337 | 291 |
| QDRII/II+ SRAM Emulation *(2)* | 1.8-V HSTL | ×36 | 261 | 328 | 314 | 337 | 337 | 350 | 337 | 350 | 337 | 350 |
| RLDRAM II | 1.5-V HSTL | ×9, ×18 | 211 | 336 | 264 | 356 | 287 | 356 | 287 | 356 | 287 | 356 |
| RLDRAM II | 1.8-V HSTL | ×9, ×18 | 211 | 336 | 264 | 356 | 287 | 356 | 287 | 356 | 287 | 356 |

**Notes to Table 1–28:**

(1) The values apply to Column I/Os, Row I/Os and Hybrid mode interface. Column I/Os refer to top and bottom I/Os. Hybrid mode refers to DQ/DQS groups wrapping over Column I/Os and Row I/Os of the device.

(2) For implementation, refer to the "Supporting ×36 QDRII+/QDRII SRAM Interfaces in the F780 and F1152-Pin Packages" section in the *External Memory Interfaces in Stratix III Devices* chapter.

**Table 1–29.** Transmitter Channel-to-Channel Skew (TCCS)—Write Side *(Note 1)* (Part 1 of 2)

| Memory Type | I/O Standard | Width | C2 | | C3, I3 | | C4, I4 | | C4L, I4L | | C4L, I4L | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CCL}$ = 1.1 V | | $V_{CCL}$ = 1.1 V | | $V_{CCL}$ = 1.1 V | | $V_{CCL}$ = 1.1 V | | $V_{CCL}$ = 0.9 V | |
| | | | TCCS (ps) | | TCCS (ps) | | TCCS (ps) | | TCCS (ps) | | TCCS (ps) | |
| | | | Lead | Lag | Lead | Lag | Lead | Lag | Lead | Lag | Lead | Lag |
| DDR3 SDRAM (with Deskew circuitry, 401 MHz–533 MHz) | 1.5-V SSTL | ×4, ×8 | 253 | 262 | — | — | — | — | — | — | — | — |
| DDR3 SDRAM (8-tap phase offset, 375 MHz–400 MHz) | 1.5-V SSTL | ×4, ×8 | 293 | 284 | 341 | 332 | — | — | — | — | — | — |
| DDR3 SDRAM (8-tap phase offset, 360 MHz–375 MHz) | 1.5-V SSTL | ×4, ×8 | 293 | 284 | 341 | 373 | — | — | — | — | — | — |
| DDR3 SDRAM (10-tap phase offset, 333 MHz–360 MHz) | 1.5-V SSTL | ×4, ×8 | 169 | 470 | 217 | 496 | 258 | 528 | 258 | 528 | — | — |
| DDR3 SDRAM (10-tap phase offset, 300 MHz–333 MHz) | 1.5-V SSTL | ×4, ×8 | 169 | 470 | 217 | 496 | 258 | 528 | 258 | 528 | — | — |
| DDR3 SDRAM (Non-leveling interface) | 1.5-V SSTL | ×4, ×8 | 268 | 246 | 230 | 355 | 250 | 388 | 250 | 388 | 250 | 388 |
| DDR2 SDRAM Differential DQS | 1.8-V SSTL | ×4, ×8 | 229 | 246 | 230 | 355 | 250 | 388 | 250 | 388 | 350 | 488 |
| DDR2 SDRAM Single-ended DQS | 1.8-V SSTL | ×4, ×8 | 316 | 168 | 318 | 239 | 346 | 260 | 346 | 260 | 446 | 360 |
| DDR SDRAM Single-ended DQS | 2.5-V SSTL | ×4, ×8 | 313 | 157 | 315 | 222 | 343 | 242 | 343 | 242 | 443 | 342 |
| QDRII/II+ SRAM | 1.5-V HSTL | ×9, ×18, ×36 | 290 | 278 | 292 | 388 | 315 | 421 | 315 | 421 | 415 | 521 |
| QDRII/II+ SRAM Emulation *(2)* | 1.5-V HSTL | ×36 | 310 | 298 | 312 | 408 | 335 | 441 | 335 | 441 | 435 | 541 |

**Table 1–29.** Transmitter Channel-to-Channel Skew (TCCS)—Write Side *(Note 1)* (Part 2 of 2)

| Memory Type | I/O Standard | Width | C2 | | C3, I3 | | C4, I4 | | C4L, I4L | | C4L, I4L | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CCL}$ = 1.1 V | | $V_{CCL}$ = 1.1 V | | $V_{CCL}$ = 1.1 V | | $V_{CCL}$ = 1.1 V | | $V_{CCL}$ = 0.9 V | |
| | | | TCCS (ps) | | TCCS (ps) | | TCCS (ps) | | TCCS (ps) | | TCCS (ps) | |
| | | | Lead | Lag | Lead | Lag | Lead | Lag | Lead | Lag | Lead | Lag |
| QDRII/II+ SRAM | 1.8-V HSTL | ×9, ×18, ×36 | 259 | 276 | 260 | 385 | 280 | 418 | 280 | 418 | 380 | 518 |
| QDRII/II+ SRAM Emulation *(2)* | 1.8-V HSTL | ×36 | 279 | 296 | 280 | 405 | 300 | 438 | 300 | 438 | 400 | 538 |
| RLDRAM II | 1.5-V HSTL | ×9, ×18 | 290 | 278 | 292 | 388 | 315 | 421 | 315 | 421 | 415 | 521 |
| RLDRAM II | 1.8-V HSTL | ×9, ×18 | 259 | 276 | 260 | 385 | 280 | 418 | 280 | 418 | 380 | 518 |

**Notes to Table 1–29:**

(1) The values apply to Column I/Os, Row I/Os, and Hybrid mode interfaces. Column I/Os refer to top and bottom I/Os. Hybrid mode refers to DQ/DQS groups wrapping over Column I/Os and Row I/Os of the device.

(2) For implementation, refer to the "Supporting ×36 QDRII+/QDRII SRAM Interfaces in the F780 and F1152-Pin Packages" section in the *External Memory Interfaces in Stratix III Devices* chapter.

### DLL and DQS Logic Block Specifications

Table 1–30 lists the DLL frequency range specifications for Stratix III devices.

**Table 1–30.** DLL Frequency Range Specifications for Stratix III Devices

| Frequency Mode | Frequency Range (MHz) | | | | Available Phase Shift | Number of Delay Chains | DQS Delay Buffer Mode *(1)* |
|---|---|---|---|---|---|---|---|
| | C2 | C3, I3 | C4, I4 | C4L, I4L | | | |
| 0 | 90 – 150 | 90 – 140 | 90 – 120 | 90 – 120 | 22.5°, 45°, 67.5°, 90° | 16 | Low |
| 1 | 120 – 200 | 120 – 190 | 120 – 170 | 120 – 170 | 30°, 60°, 90°, 120° | 12 | Low |
| 2 | 150 – 240 | 150 – 230 | 150 – 200 | 150 – 200 | 36°, 72°, 108°, 144° | 10 | Low |
| 3 | 180 – 300 | 180 – 290 | 180 – 250 | 180 – 250 | 45°, 90°,135°, 180° | 8 | Low |
| 4 | 240 – 370 | 240 – 350 | 240 – 310 | 240 – 310 | 30°, 60°, 90°,120° | 12 | High |
| 5 | 290 – 450 | 290 – 420 | 290 – 370 | 290 – 370 | 36°, 72°, 108°, 144° | 10 | High |
| 6 | 360 – 560 | 360 – 530 | 360 – 460 | 360 – 460 | 45°, 90°, 135°, 180° | 8 | High |
| 7 | 470 – 740 | 470 – 700 | 470 – 610 | 470 – 610 | 60°, 120°, 180°, 240° | 6 | High |

**Note to Table 1–30:**

(1) "Low" indicates a 6-bit DQS delay setting; "high" indicates a 5-bit DQS delay setting.

Table 1–31 lists the average DQS phase offset delay per setting for Stratix III devices.

**Table 1–31.** Average DQS Phase Offset Delay per Setting for Stratix III Devices *(Note 1)*, *(2)*, *(3)*

| Speed Grade | Min | Typ | Max | Unit |
|---|---|---|---|---|
| C2 | 7 | 10 | 13 | ps |
| C3, I3 | 7 | 11 | 15 | ps |
| C4, I4 | 7 | 11.5 | 16 | ps |
| C4L, I4L | 7 | 11.5 | 16 | ps |

**Notes to Table 1–31:**

(1) The valid settings for phase offset are -64 to +63 for frequency modes 0 to 3 and -32 to +31 for frequency modes 4 to 6.

(2) The typical value equals the average of the minimum and maximum values.

(3) The delay settings are linear with a cumulative delay variation of ± 20 ps for all speed grades. For example, when using a C2 speed grade and applying 10° phase offset settings to a 90° phase shift at 400 MHz, the expected minimum cumulative delay is [625 ps + (10*7 ps) - 20 ps] = 675 ps.

Table 1–32 lists the DQS phase shift error specification for DLL-delayed clock ($t_{DQS_PSERR}$) for Stratix III devices.

**Table 1–32.** DQS Phase Shift Error Specification for DLL-Delayed Clock ($t_{DQS_PSERR}$) for Stratix III Devices *(Note 1)*

| Number of DQS Delay Buffer | C2 | C3, I3 | C4, C4L, I4, I4L | Unit |
|---|---|---|---|---|
| 1 | ±13 | ±14 | ±15 | ps |
| 2 | ±26 | ±28 | ±30 | ps |
| 3 | ±39 | ±42 | ±45 | ps |
| 4 | ±52 | ±56 | ±60 | ps |

**Note to Table 1–32:**

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a C2 speed grade is ± 39 ps.

Table 1–33 lists the memory output jitter specification for Stratix III devices.

**Table 1–33.** Memory Output Clock Jitter Specification for Stratix III Devices *(Note 1)*, *(2)*

| Parameter | Clock Network | Symbol | C2 | | C3, I3 | | C4, I4 | | C4L, I4L | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CCL}$ = 1.1V | | $V_{CCL}$ = 1.1V | | $V_{CCL}$ = 1.1V | | $V_{CCL}$ = 1.1V | | $V_{CCL}$ = 0.9V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Clock period jitter | Regional | tJIT(per) | –75 | 75 | –85 | 85 | –100 | 100 | –100 | 100 | –120 | 120 | ps |
| Cycle-to-cycle period jitter | Regional | tJIT(cc) | –150 | 150 | –170 | 170 | –190 | 190 | –190 | 190 | –230 | 230 | ps |
| Duty cycle jitter | Regional | tJIT(duty) | –80 | 80 | –90 | 90 | –100 | 100 | –100 | 100 | –140 | 140 | ps |
| Clock period jitter | Global | tJIT(per) | –113 | 113 | –128 | 128 | –150 | 150 | –150 | 150 | –180 | 180 | ps |
| Cycle-to-cycle period jitter | Global | tJIT(cc) | –225 | 225 | –255 | 255 | –285 | 285 | –285 | 285 | –340 | 340 | ps |
| Duty cycle jitter | Global | tJIT(duty) | –120 | 120 | –135 | 135 | –150 | 150 | –150 | 150 | –180 | 180 | ps |

**Notes to Table 1–33:**

(1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 standard.

(2) The clock jitter specification applies to memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a regional or global clock network as specified. Altera recommends using the regional clock networks whenever possible.

### OCT Calibration Block Specifications

Table 1–34 lists the on-chip termination calibration block specifications for Stratix III devices.

**Table 1–34.** On-Chip Termination Calibration Block Specification

| Symbol | Description | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| OCTUSRCLK | Clock required by OCT calibration blocks | — | — | 20 | MHz |
| $t_{OCTCAL}$ | Number of OCTUSRCLK clock cycles required for OCT Rs and Rt calibration | — | 1000 | — | cycles |
| $t_{OCTSHIFT}$ | Number of OCTUSRCLK clock cycles required for OCT code to shift out per OCT calibration block | — | 28 | — | cycles |
| $t_{RS_RT}$ | Time required to dynamically switch from Rs to Rt | — | 2.5 | — | ns |

### DCD Specifications

Table 1–35 lists the worst case duty cycle distortion for Stratix III devices.

**Table 1–35.** Duty Cycle Distortion on Stratix III I/O Pins *(Note 1)*

| Symbol | C2 | | C3 | | C4 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | % |

**Note to Table 1–35:**

(1) The DCD specification applies to clock outputs from the PLLs, global clock tree, and IOE driving dedicated and general-purpose I/O pins.

# I/O Timing

The following sections describe the timing models, preliminary and final timings, I/O timing measurement methodology, I/O default capacitive loading, programmable IOE delay, programmable output buffer delay, user I/O timing, and dedicated clock pin timing.

## Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix III device densities and speed grades. This section describes the performance of the Stratix III device I/Os.

All specifications except the fast model are representative of worst-case supply voltage and junction temperature conditions. Fast model specifications are representative of best case process, supply voltage, and junction temperature conditions.

The timing numbers listed in this section are extracted from the Quartus II software version 8.1.

## Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during design compilation if the timing models are preliminary. Table 1–36 lists the status of the Stratix III device timing models.

Preliminary status means that the timing models are subject to change in future Quartus II releases. Initially, timing numbers are created using simulation results, process data, and other known parameters. Parts of the timing models may be correlated to silicon measurements. Various tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing models are based on simulation models that are characterized versus the actual device measurements under all allowable operating conditions. When the timing models are final, all or most of the Stratix III family devices have been completely characterized and no further changes to the timing model are expected.

**Table 1–36.** Timing Model Status for Stratix III Devices

| Device | Preliminary | Final |
|---|---|---|
| EP3SL50 | — | ✓ |
| EP3SL70 | — | ✓ |
| EP3SL110 | — | ✓ |
| EP3SL150 | — | ✓ |
| EP3SL200 | — | ✓ |
| EP3SL340 | — | ✓ |
| EP3SE50 | — | ✓ |
| EP3SE80 | — | ✓ |
| EP3SE110 | — | ✓ |
| EP3SE260 | — | ✓ |

## I/O Timing Measurement Methodology

Altera characterizes timing delays at the worst-case process, minimum voltage, and maximum temperature for input register setup time ($t_{su}$) and hold time ($t_h$). The Quartus II software uses the following equations to calculate $t_{su}$ and $t_h$ timing for the Stratix III devices input signals.

$t_{su}$ =

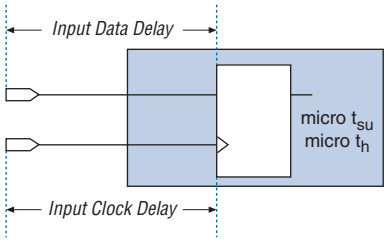
+ data delay from the input pin to the input register
+ micro setup time of the input register
- clock delay from the input pin to the input register

$t_h$ =

- data delay from the input pin to the input register
+ micro hold time of the input register
+ clock delay from the input pin to the input register

Figure 1–4 shows the setup and hold timing diagram for input registers.

**Figure 1–4.** Input Register Setup and Hold Timing Diagram




For output timing, different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X, which use 10 pF) loading. The timing is specified up to the output pin of the FPGA device. The Quartus II software calculates I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

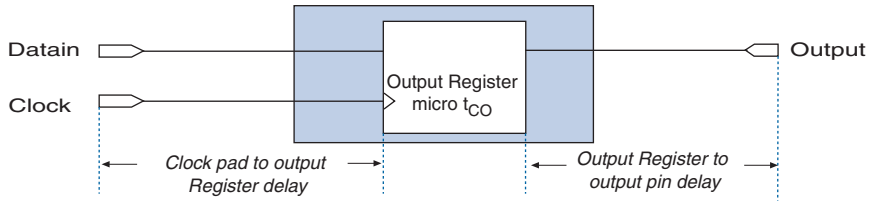
The following measurements are made during device characterization. Altera measures clock-to-output delays ($t_{co}$) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions listed in Table 1–37 on page 1–34. The following equation describes clock-pin-to-output-pin timing for Stratix III devices.

The $t_{co}$ from the clock pin to the I/O pin =

+ delay from the clock pad to the I/O output register
+ IOE output register clock-to-output delay
+ delay from the output register to the output pin

Figure 1–5 shows the output register clock to output timing diagram.

**Figure 1–5.** Output Register Clock to Output Timing Diagram



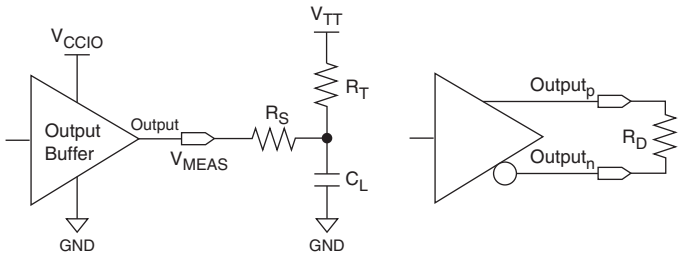

Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the Stratix III Device Handbook. Perform the following steps:

1. Simulate the output driver of choice into the generalized test setup using values from Table 1–37.
2. Record the time to $V_{MEAS}$ at the far end of the PCB trace.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to $V_{MEAS}$ at the far end of the PCB trace.

5. Compare the results of steps 2 and 4. The increase or decrease in delay must be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-output) of the PCB trace.

The Quartus II software reports the timing with the conditions listed in Table 1–37 using Equation 1–1 on page 1–7. Figure 1–6 shows the circuit that is represented by the output timing of the Quartus II software.

**Figure 1–6.** Output Delay Timing Report Setup for Single-Ended Outputs and Dedicated Differential Outputs *(Note 1)*




**Note to Figure 1–6:**

(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay must be accounted for with IBIS model simulations.

Figure 1–7 and Figure 1–8 show the circuit that is represented by the output timing of the Quartus II software for differential outputs with single and multiple external resistors, respectively.

**Figure 1–7.** Output Delay Timing Report Setup for Differential Outputs with Single External Resistor

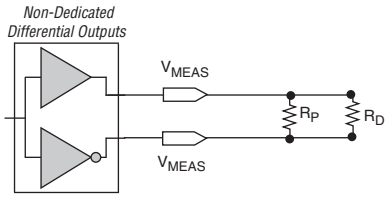



**Figure 1–8.** Output Delay Timing Report Setup for Differential Outputs with Three External Resistor

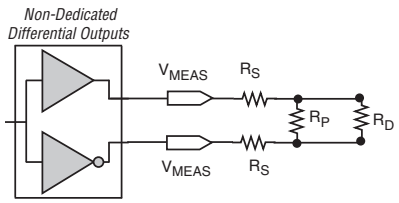


**Table 1–37.** Output Timing Measurement Methodology for Output Pins (Part 1 of 3)

| I/O Standard | Loading and Termination | | | | | | | | | Measurement Point |
|---|---|---|---|---|---|---|---|---|---|---|
| | $R_S$ | $R_D$ | $R_T$ | $R_P$ | $V_{CCIO}$ | $V_{CCPD}$ | $V_{CC}$ | $V_{TT}$ | $C_L$ (pF) | $V_{MEAS}$ (v) |
| 3.3-V LVTTL | — | — | — | — | 3.135 | 3.135 | 1.05 | — | 0 | 1.5675 |
| 3.3-V LVCMOS | — | — | — | — | 3.135 | 3.135 | 1.05 | — | 0 | 1.5675 |
| 3.0-V LVTTL | — | — | — | — | 2.85 | 2.85 | 1.05 | — | 0 | 1.425 |
| 3.0-V LVCMOS | — | — | — | — | 2.85 | 2.85 | 1.05 | — | 0 | 1.425 |
| 2.5-V | — | — | — | — | 2.375 | 2.375 | 1.05 | — | 0 | 1.1875 |
| 1.8-V | — | — | — | — | 1.71 | 2.375 | 1.05 | — | 0 | 0.855 |
| 1.5-V | — | — | — | — | 1.425 | 2.375 | 1.05 | — | 0 | 0.7125 |
| 1.2-V | — | — | — | — | 1.14 | 2.375 | 1.05 | — | 0 | 0.57 |
| PCI | — | — | — | — | 2.85 | 2.85 | 1.05 | — | 10 | 1.425 |
| PCI-X | — | — | — | — | 2.85 | 2.85 | 1.05 | — | 10 | 1.425 |
| SSTL-2 CLASS I | 25 | — | 50 | — | 2.325 | 2.325 | 1.02 | 1.25 | 0 | 1.1625 |
| SSTL-2 CLASS II | 25 | — | 25 | — | 2.325 | 2.325 | 1.02 | 1.25 | 0 | 1.1625 |
| SSTL-18 CLASS I | 25 | — | 50 | — | 1.66 | 2.325 | 1.02 | 0.90 | 0 | 0.83 |
| SSTL-18 CLASS II | 25 | — | 25 | — | 1.66 | 2.325 | 1.02 | 0.90 | 0 | 0.83 |
| SSTL-15 CLASS I | 25 | — | 50 | — | 1.375 | 2.325 | 1.02 | 0.75 | 0 | 0.6875 |
| SSTL-15 CLASS II | 25 | — | 25 | — | 1.375 | 2.325 | 1.02 | 0.75 | 0 | 0.6875 |
| 1.8-V HSTL CLASS I | — | — | 50 | — | 1.66 | 2.325 | 1.02 | 0.90 | 0 | 0.83 |
| 1.8-V HSTL CLASS II | — | — | 25 | — | 1.66 | 2.325 | 1.02 | 0.90 | 0 | 0.83 |
| 1.5-V HSTL CLASS I | — | — | 50 | — | 1.375 | 2.325 | 1.02 | 0.75 | 0 | 0.6875 |
| 1.5-V HSTL CLASS II | — | — | 25 | — | 1.375 | 2.325 | 1.02 | 0.75 | 0 | 0.6875 |
| 1.2-V HSTL CLASS I | — | — | 50 | — | 1.09 | 2.325 | 1.02 | 0.60 | 0 | 0.545 |
| 1.2-V HSTL CLASS II | — | — | 25 | — | 1.09 | 2.325 | 1.02 | 0.60 | 0 | 0.545 |
| Differential SSTL-2 CLASS I | 25 | — | 50 | — | 2.325 | 2.325 | 1.02 | 1.25 | 0 | 1.1625 |
| Differential SSTL-2 CLASS II | 25 | — | 25 | — | 2.325 | 2.325 | 1.02 | 1.25 | 0 | 1.1625 |
| Differential SSTL-18 CLASS I | 25 | — | 50 | — | 1.66 | 2.325 | 1.02 | 0.90 | 0 | 0.83 |
| Differential SSTL-18 CLASS II | 25 | — | 25 | — | 1.66 | 2.325 | 1.02 | 0.90 | 0 | 0.83 |
| 1.8-V Differential HSTL CLASS I | — | — | 50 | — | 1.66 | 2.325 | 1.02 | 0.90 | 0 | 0.83 |
| 1.8-V Differential HSTL CLASS II | — | — | 25 | — | 1.66 | 2.325 | 1.02 | 0.90 | 0 | 0.83 |
| 1.5-V Differential HSTL CLASS I | — | — | 50 | — | 1.375 | 2.325 | 1.02 | 0.75 | 0 | 0.6875 |

**Table 1–37.** Output Timing Measurement Methodology for Output Pins (Part 2 of 3)

| I/O Standard | Loading and Termination | | | | | | | | | Measurement Point |
|---|---|---|---|---|---|---|---|---|---|---|
| | $R_S$ | $R_D$ | $R_T$ | $R_P$ | $V_{CCIO}$ | $V_{CCPD}$ | $V_{CC}$ | $V_{TT}$ | $C_L$ (pF) | $V_{MEAS}$ (v) |
| 1.5-V Differential HSTL CLASS II | — | — | 25 | — | 1.375 | 2.325 | 1.02 | 0.75 | 0 | 0.6875 |
| 1.2-V Differential HSTL CLASS I | — | — | 50 | — | 1.09 | 2.325 | 1.02 | 0.60 | 0 | 0.545 |
| 1.2-V Differential HSTL CLASS II | — | — | 25 | — | 1.09 | 2.325 | 1.02 | 0.60 | 0 | 0.545 |
| LVDS | — | 100 | — | — | 2.325 | 2.325 | 1.02 | — | 0 | 1.1625 |
| MINI-LVDS | — | 100 | — | — | 2.325 | 2.325 | 1.02 | — | 0 | 1.1625 |
| RSDS | — | 100 | — | — | 2.325 | 2.325 | 1.02 | — | 0 | 1.1625 |
| LVDS_E_1R | — | 100 | — | 120 | 2.325 | 2.325 | 1.02 | — | 0 | 1.1625 |
| LVDS_E_3R | 120 | 100 | — | 170 | 2.325 | 2.325 | 1.02 | — | 0 | 1.1625 |

**Table 1–37.** Output Timing Measurement Methodology for Output Pins (Part 3 of 3)

| I/O Standard | Loading and Termination | | | | | | | | | Measurement Point |
|---|---|---|---|---|---|---|---|---|---|---|
| | $R_S$ | $R_D$ | $R_T$ | $R_P$ | $V_{CCIO}$ | $V_{CCPD}$ | $V_{CC}$ | $V_{TT}$ | $C_L$ (pF) | $V_{MEAS}$ (v) |
| MINI-LVDS_E_1R | — | 100 | — | 120 | 2.325 | 2.325 | 1.02 | — | 0 | 1.1625 |
| MINI-LVDS_E_3R | 120 | 100 | — | 170 | 2.325 | 2.325 | 1.02 | — | 0 | 1.1625 |
| RSDS_E_1R | — | 100 | — | 120 | 2.325 | 2.325 | 1.02 | — | 0 | 1.1625 |
| RSDS_E_3R | 120 | 100 | — | 170 | 2.325 | 2.325 | 1.02 | — | 0 | 1.1625 |

**Notes to Table 1–37:**

(1) Hyper transport is not supported by Stratix III devices.
(2) LVPECL outputs are not supported by Stratix III devices.
(3) You can change the Quartus II timing conditions using the Advanced I/O Timing feature.
(4) $V_{CC}$ is nominally 1.1 V less 50 mV (1.05 V).
(5) Terminated I/O standards require an additional 30 mV IR drop on $V_{CC}$ (1.02 V).
(6) Terminated I/O standards require an additional 50 mV IR drop on $V_{CCIO}$ and $V_{CCPD}$.

## I/O Default Capacitive Loading

Table 1–38 lists the default capacitive loading of various I/O standards.

**Table 1–38.** Default Loading of Various I/O Standards for Stratix III Devices (Part 1 of 2)

| I/O Standard | Capacitive Load | Unit |
|---|---|---|
| 3.3-V LVTTL | 0 | pF |
| 3.3-V LVCMOS | 0 | pF |
| 3.0-V LVTTL | 0 | pF |
| 3.0-V LVCMOS | 0 | pF |
| 2.5-V LVTTL/LVCMOS | 0 | pF |
| 1.8-V LVTTL/LVCMOS | 0 | pF |
| 1.5-V LVTTL/LVCMOS | 0 | pF |
| 3.0-V PCI | 10 | pF |
| 3.0-V PCI-X | 10 | pF |
| SSTL-2 CLASS I | 0 | pF |
| SSTL-2 CLASS II | 0 | pF |
| SSTL-18 CLASS I | 0 | pF |
| SSTL-18 CLASS II | 0 | pF |
| 1.5-V HSTL CLASS I | 0 | pF |
| 1.5-V HSTL CLASS II | 0 | pF |
| 1.8-V HSTL CLASS I | 0 | pF |
| 1.8-V HSTL CLASS II | 0 | pF |
| 1.2-V HSTL | 0 | pF |
| Differential SSTL-2 CLASS I | 0 | pF |
| Differential SSTL-2 CLASS II | 0 | pF |
| Differential SSTL-18 CLASS I | 0 | pF |

**Table 1–38.** Default Loading of Various I/O Standards for Stratix III Devices (Part 2 of 2)

| I/O Standard | Capacitive Load | Unit |
|---|---|---|
| Differential SSTL-18 CLASS II | 0 | pF |
| 1.8-V Differential HSTL CLASS I | 0 | pF |
| 1.8-V Differential HSTL CLASS II | 0 | pF |
| 1.5-V Differential HSTL CLASS I | 0 | pF |
| 1.5-V Differential HSTL CLASS II | 0 | pF |
| 1.2-V Differential HSTL CLASS I | 0 | pF |
| 1.2-V Differential HSTL CLASS II | 0 | pF |
| LVDS | 0 | pF |

## Programmable IOE Delay

Table 1–39 lists the Stratix III IOE programmable delay settings.

For more information about the annotation of delays in the IOE, refer to Figure 7–7 in the *Stratix III Device I/O Features* chapter.

**Table 1–39.** IOE Programmable Delay for Stratix III Devices *(Note 1)*

| Parameter | Available Settings | Min Offset *(2)* | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 0.9 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 1.1 V | $V_{CCL}$ = 0.9 V | |
| | | | Max Offset | Max Offset | Max Offset | Max Offset | Max Offset | Max Offset | Max Offset | Max Offset | Max Offset | Max Offset | Max Offset | |
| D1 | 15 | 0 | 442 | 491 | 748 | 829 | 916 | 871 | 833 | 870 | 957 | 915 | 833 | ps |
| D2 | 7 | 0 | 248 | 285 | 387 | 412 | 442 | 427 | 411 | 433 | 464 | 448 | 411 | ps |
| D3 | 7 | 0 | 1625 | 1806 | 2747 | 3058 | 3371 | 3218 | 3084 | 3210 | 3540 | 3382 | 3084 | ps |
| D4 | 15 | 0 | 491 | 517 | 726 | 872 | 884 | 844 | 808 | 845 | 928 | 887 | 808 | ps |
| D5 | 15 | 0 | 452 | 503 | 764 | 801 | 930 | 887 | 850 | 889 | 977 | 932 | 850 | ps |
| D6 | 6 | 0 | 179 | 199 | 305 | 337 | 370 | 354 | 339 | 354 | 389 | 371 | 339 | ps |

**Notes to Table 1–39:**

(1) You can set the parameter values in the Quartus II software by selecting D1, D2, D3, D4, D5, and D6 in the Assignment Name column.

(2) The minimum offset represented in this table does not include the intrinsic delay.

## Programmable Output Buffer Delay

Table 1–40 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

**Table 1–40.** Programmable Output Buffer Delay *(Note 1)*

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $D_{OUTBUF}$ | Rising and/or Falling Edge delay | 0 (default) | ps |
| | | 50 | ps |
| | | 100 | ps |
| | | 150 | ps |

**Note to Table 1–40:**

(1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges with the specific values stated in this table for the **Output Buffer Delay** assignment.

## User I/O Pin Timing

Table 1–41 through Table 1–140 list user I/O pin timing for Stratix III devices. I/O buffer $t_{su}$, $t_h$, and $t_{co}$ are reported for the cases when the I/O clock is driven by a non-PLL global clock (GCLK) and the PLL is driven by the global clock (GCLK-PLL). For $t_{su}$, $t_h$, and $t_{co}$ using the regional clock, add the value from the adder tables listed for each device to the GCLK/GCLK-PLL values for the device.

### EP3SL50 I/O Timing Parameters

Table 1–41 through Table 1–44 list the maximum I/O timing parameters for EP3SL50 devices for single-ended I/O standards.

Table 1–41 lists the EP3SL50 column pins input timing parameters for single-ended I/O standards.

**Table 1–41.** EP3SL50 Column Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -0.690 | -0.689 | -1.004 | -1.103 | -1.311 | -1.266 | -1.627 | -1.103 | -1.311 | -1.266 | -1.627 | ns |
| | | $t_h$ | 0.816 | 0.814 | 1.182 | 1.304 | 1.531 | 1.475 | 1.830 | 1.304 | 1.531 | 1.475 | 1.830 | ns |
| | GCLK PLL | $t_{su}$ | -0.975 | -0.975 | -1.405 | -1.532 | -1.773 | -1.713 | -2.026 | -1.532 | -1.773 | -1.713 | -2.026 | ns |
| | | $t_h$ | 1.226 | 1.226 | 1.774 | 1.947 | 2.232 | 2.148 | 2.471 | 1.947 | 2.232 | 2.148 | 2.471 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -0.690 | -0.689 | -1.004 | -1.103 | -1.311 | -1.266 | -1.627 | -1.103 | -1.311 | -1.266 | -1.627 | ns |
| | | $t_h$ | 0.816 | 0.814 | 1.182 | 1.304 | 1.531 | 1.475 | 1.830 | 1.304 | 1.531 | 1.475 | 1.830 | ns |
| | GCLK PLL | $t_{su}$ | -0.975 | -0.975 | -1.405 | -1.532 | -1.773 | -1.713 | -2.026 | -1.532 | -1.773 | -1.713 | -2.026 | ns |
| | | $t_h$ | 1.226 | 1.226 | 1.774 | 1.947 | 2.232 | 2.148 | 2.471 | 1.947 | 2.232 | 2.148 | 2.471 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -0.701 | -0.700 | -1.003 | -1.105 | -1.310 | -1.265 | -1.626 | -1.105 | -1.310 | -1.265 | -1.626 | ns |
| | | $t_h$ | 0.827 | 0.825 | 1.181 | 1.306 | 1.530 | 1.474 | 1.829 | 1.306 | 1.530 | 1.474 | 1.829 | ns |
| | GCLK PLL | $t_{su}$ | -0.986 | -0.986 | -1.404 | -1.534 | -1.772 | -1.712 | -2.025 | -1.534 | -1.772 | -1.712 | -2.025 | ns |
| | | $t_h$ | 1.237 | 1.237 | 1.773 | 1.949 | 2.231 | 2.147 | 2.470 | 1.949 | 2.231 | 2.147 | 2.470 | ns |


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**Table 1–41.** EP3SL50 Column Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -0.701 | -0.700 | -1.003 | -1.105 | -1.310 | -1.265 | -1.626 | -1.105 | -1.310 | -1.265 | -1.626 | ns |
| | | $t_h$ | 0.827 | 0.825 | 1.181 | 1.306 | 1.530 | 1.474 | 1.829 | 1.306 | 1.530 | 1.474 | 1.829 | ns |
| | GCLK PLL | $t_{su}$ | -0.986 | -0.986 | -1.404 | -1.534 | -1.772 | -1.712 | -2.025 | -1.534 | -1.772 | -1.712 | -2.025 | ns |
| | | $t_h$ | 1.237 | 1.237 | 1.773 | 1.949 | 2.231 | 2.147 | 2.470 | 1.949 | 2.231 | 2.147 | 2.470 | ns |
| 2.5 V | GCLK | $t_{su}$ | -0.696 | -0.695 | -1.012 | -1.117 | -1.329 | -1.284 | -1.645 | -1.117 | -1.329 | -1.284 | -1.645 | ns |
| | | $t_h$ | 0.822 | 0.820 | 1.190 | 1.318 | 1.549 | 1.493 | 1.848 | 1.318 | 1.549 | 1.493 | 1.848 | ns |
| | GCLK PLL | $t_{su}$ | -0.981 | -0.981 | -1.413 | -1.546 | -1.791 | -1.731 | -2.044 | -1.546 | -1.791 | -1.731 | -2.044 | ns |
| | | $t_h$ | 1.232 | 1.232 | 1.782 | 1.961 | 2.250 | 2.166 | 2.489 | 1.961 | 2.250 | 2.166 | 2.489 | ns |
| 1.8 V | GCLK | $t_{su}$ | -0.716 | -0.715 | -1.052 | -1.153 | -1.327 | -1.282 | -1.643 | -1.153 | -1.327 | -1.282 | -1.643 | ns |
| | | $t_h$ | 0.844 | 0.842 | 1.230 | 1.354 | 1.547 | 1.491 | 1.846 | 1.354 | 1.547 | 1.491 | 1.846 | ns |
| | GCLK PLL | $t_{su}$ | -1.003 | -1.003 | -1.453 | -1.582 | -1.789 | -1.729 | -2.042 | -1.582 | -1.789 | -1.729 | -2.042 | ns |
| | | $t_h$ | 1.256 | 1.256 | 1.822 | 1.997 | 2.248 | 2.164 | 2.487 | 1.997 | 2.248 | 2.164 | 2.487 | ns |
| 1.5 V | GCLK | $t_{su}$ | -0.706 | -0.705 | -1.029 | -1.121 | -1.257 | -1.212 | -1.573 | -1.121 | -1.257 | -1.212 | -1.573 | ns |
| | | $t_h$ | 0.834 | 0.832 | 1.207 | 1.322 | 1.477 | 1.421 | 1.776 | 1.322 | 1.477 | 1.421 | 1.776 | ns |
| | GCLK PLL | $t_{su}$ | -0.993 | -0.993 | -1.430 | -1.550 | -1.719 | -1.659 | -1.972 | -1.550 | -1.719 | -1.659 | -1.972 | ns |
| | | $t_h$ | 1.246 | 1.246 | 1.799 | 1.965 | 2.178 | 2.094 | 2.417 | 1.965 | 2.178 | 2.094 | 2.417 | ns |
| 1.2 V | GCLK | $t_{su}$ | -0.654 | -0.653 | -0.952 | -1.022 | -1.101 | -1.056 | -1.417 | -1.022 | -1.101 | -1.056 | -1.417 | ns |
| | | $t_h$ | 0.782 | 0.780 | 1.130 | 1.223 | 1.321 | 1.265 | 1.620 | 1.223 | 1.321 | 1.265 | 1.620 | ns |
| | GCLK PLL | $t_{su}$ | -0.941 | -0.941 | -1.353 | -1.451 | -1.563 | -1.503 | -1.816 | -1.451 | -1.563 | -1.503 | -1.816 | ns |
| | | $t_h$ | 1.194 | 1.194 | 1.722 | 1.866 | 2.022 | 1.938 | 2.261 | 1.866 | 2.022 | 1.938 | 2.261 | ns |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -0.625 | -0.624 | -0.924 | -1.006 | -1.103 | -1.058 | -1.419 | -1.006 | -1.103 | -1.058 | -1.419 | ns |
| | | $t_h$ | 0.753 | 0.751 | 1.102 | 1.207 | 1.323 | 1.267 | 1.622 | 1.207 | 1.323 | 1.267 | 1.622 | ns |
| | GCLK PLL | $t_{su}$ | -0.912 | -0.912 | -1.325 | -1.435 | -1.565 | -1.505 | -1.818 | -1.435 | -1.565 | -1.505 | -1.818 | ns |
| | | $t_h$ | 1.165 | 1.165 | 1.694 | 1.850 | 2.024 | 1.940 | 2.263 | 1.850 | 2.024 | 1.940 | 2.263 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -0.625 | -0.624 | -0.924 | -1.006 | -1.103 | -1.058 | -1.419 | -1.006 | -1.103 | -1.058 | -1.419 | ns |
| | | $t_h$ | 0.753 | 0.751 | 1.102 | 1.207 | 1.323 | 1.267 | 1.622 | 1.207 | 1.323 | 1.267 | 1.622 | ns |
| | GCLK PLL | $t_{su}$ | -0.912 | -0.912 | -1.325 | -1.435 | -1.565 | -1.505 | -1.818 | -1.435 | -1.565 | -1.505 | -1.818 | ns |
| | | $t_h$ | 1.165 | 1.165 | 1.694 | 1.850 | 2.024 | 1.940 | 2.263 | 1.850 | 2.024 | 1.940 | 2.263 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -0.619 | -0.618 | -0.912 | -1.001 | -1.103 | -1.056 | -1.417 | -1.001 | -1.103 | -1.056 | -1.417 | ns |
| | | $t_h$ | 0.747 | 0.745 | 1.089 | 1.199 | 1.320 | 1.264 | 1.615 | 1.199 | 1.320 | 1.264 | 1.615 | ns |
| | GCLK PLL | $t_{su}$ | -0.906 | -0.906 | -1.312 | -1.427 | -1.562 | -1.500 | -1.816 | -1.427 | -1.562 | -1.500 | -1.816 | ns |
| | | $t_h$ | 1.159 | 1.159 | 1.681 | 1.839 | 2.018 | 1.934 | 2.256 | 1.839 | 2.018 | 1.934 | 2.256 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -0.619 | -0.618 | -0.912 | -1.001 | -1.103 | -1.056 | -1.417 | -1.001 | -1.103 | -1.056 | -1.417 | ns |
| | | $t_h$ | 0.747 | 0.745 | 1.089 | 1.199 | 1.320 | 1.264 | 1.615 | 1.199 | 1.320 | 1.264 | 1.615 | ns |
| | GCLK PLL | $t_{su}$ | -0.906 | -0.906 | -1.312 | -1.427 | -1.562 | -1.500 | -1.816 | -1.427 | -1.562 | -1.500 | -1.816 | ns |
| | | $t_h$ | 1.159 | 1.159 | 1.681 | 1.839 | 2.018 | 1.934 | 2.256 | 1.839 | 2.018 | 1.934 | 2.256 | ns |

**Table 1–41.** EP3SL50 Column Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -0.608 | -0.607 | -0.903 | -0.990 | -1.084 | -1.037 | -1.398 | -0.990 | -1.084 | -1.037 | -1.398 | ns |
| | | $t_h$ | 0.736 | 0.734 | 1.079 | 1.188 | 1.301 | 1.245 | 1.596 | 1.188 | 1.301 | 1.245 | 1.596 | ns |
| | GCLK PLL | $t_{su}$ | -0.895 | -0.895 | -1.301 | -1.416 | -1.543 | -1.481 | -1.797 | -1.416 | -1.543 | -1.481 | -1.797 | ns |
| | | $t_h$ | 1.148 | 1.148 | 1.669 | 1.828 | 1.999 | 1.915 | 2.237 | 1.828 | 1.999 | 1.915 | 2.237 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.608 | -0.607 | -0.903 | -0.990 | -1.084 | -1.037 | -1.398 | -0.990 | -1.084 | -1.037 | -1.398 | ns |
| | | $t_h$ | 0.736 | 0.734 | 1.079 | 1.188 | 1.301 | 1.245 | 1.596 | 1.188 | 1.301 | 1.245 | 1.596 | ns |
| | GCLK PLL | $t_{su}$ | -0.895 | -0.895 | -1.301 | -1.416 | -1.543 | -1.481 | -1.797 | -1.416 | -1.543 | -1.481 | -1.797 | ns |
| | | $t_h$ | 1.148 | 1.148 | 1.669 | 1.828 | 1.999 | 1.915 | 2.237 | 1.828 | 1.999 | 1.915 | 2.237 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.619 | -0.618 | -0.912 | -1.001 | -1.103 | -1.056 | -1.417 | -1.001 | -1.103 | -1.056 | -1.417 | ns |
| | | $t_h$ | 0.747 | 0.745 | 1.089 | 1.199 | 1.320 | 1.264 | 1.615 | 1.199 | 1.320 | 1.264 | 1.615 | ns |
| | GCLK PLL | $t_{su}$ | -0.906 | -0.906 | -1.312 | -1.427 | -1.562 | -1.500 | -1.816 | -1.427 | -1.562 | -1.500 | -1.816 | ns |
| | | $t_h$ | 1.159 | 1.159 | 1.681 | 1.839 | 2.018 | 1.934 | 2.256 | 1.839 | 2.018 | 1.934 | 2.256 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.619 | -0.618 | -0.912 | -1.001 | -1.103 | -1.056 | -1.417 | -1.001 | -1.103 | -1.056 | -1.417 | ns |
| | | $t_h$ | 0.747 | 0.745 | 1.089 | 1.199 | 1.320 | 1.264 | 1.615 | 1.199 | 1.320 | 1.264 | 1.615 | ns |
| | GCLK PLL | $t_{su}$ | -0.906 | -0.906 | -1.312 | -1.427 | -1.562 | -1.500 | -1.816 | -1.427 | -1.562 | -1.500 | -1.816 | ns |
| | | $t_h$ | 1.159 | 1.159 | 1.681 | 1.839 | 2.018 | 1.934 | 2.256 | 1.839 | 2.018 | 1.934 | 2.256 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.608 | -0.607 | -0.903 | -0.990 | -1.084 | -1.037 | -1.398 | -0.990 | -1.084 | -1.037 | -1.398 | ns |
| | | $t_h$ | 0.736 | 0.734 | 1.079 | 1.188 | 1.301 | 1.245 | 1.596 | 1.188 | 1.301 | 1.245 | 1.596 | ns |
| | GCLK PLL | $t_{su}$ | -0.895 | -0.895 | -1.301 | -1.416 | -1.543 | -1.481 | -1.797 | -1.416 | -1.543 | -1.481 | -1.797 | ns |
| | | $t_h$ | 1.148 | 1.148 | 1.669 | 1.828 | 1.999 | 1.915 | 2.237 | 1.828 | 1.999 | 1.915 | 2.237 | ns |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.608 | -0.607 | -0.903 | -0.990 | -1.084 | -1.037 | -1.398 | -0.990 | -1.084 | -1.037 | -1.398 | ns |
| | | $t_h$ | 0.736 | 0.734 | 1.079 | 1.188 | 1.301 | 1.245 | 1.596 | 1.188 | 1.301 | 1.245 | 1.596 | ns |
| | GCLK PLL | $t_{su}$ | -0.895 | -0.895 | -1.301 | -1.416 | -1.543 | -1.481 | -1.797 | -1.416 | -1.543 | -1.481 | -1.797 | ns |
| | | $t_h$ | 1.148 | 1.148 | 1.669 | 1.828 | 1.999 | 1.915 | 2.237 | 1.828 | 1.999 | 1.915 | 2.237 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.596 | -0.595 | -0.893 | -0.979 | -1.068 | -1.021 | -1.382 | -0.979 | -1.068 | -1.021 | -1.382 | ns |
| | | $t_h$ | 0.724 | 0.722 | 1.069 | 1.177 | 1.285 | 1.229 | 1.580 | 1.177 | 1.285 | 1.229 | 1.580 | ns |
| | GCLK PLL | $t_{su}$ | -0.883 | -0.883 | -1.291 | -1.405 | -1.527 | -1.465 | -1.781 | -1.405 | -1.527 | -1.465 | -1.781 | ns |
| | | $t_h$ | 1.136 | 1.136 | 1.659 | 1.817 | 1.983 | 1.899 | 2.221 | 1.817 | 1.983 | 1.899 | 2.221 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -0.596 | -0.595 | -0.893 | -0.979 | -1.068 | -1.021 | -1.382 | -0.979 | -1.068 | -1.021 | -1.382 | ns |
| | | $t_h$ | 0.724 | 0.722 | 1.069 | 1.177 | 1.285 | 1.229 | 1.580 | 1.177 | 1.285 | 1.229 | 1.580 | ns |
| | GCLK PLL | $t_{su}$ | -0.883 | -0.883 | -1.291 | -1.405 | -1.527 | -1.465 | -1.781 | -1.405 | -1.527 | -1.465 | -1.781 | ns |
| | | $t_h$ | 1.136 | 1.136 | 1.659 | 1.817 | 1.983 | 1.899 | 2.221 | 1.817 | 1.983 | 1.899 | 2.221 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | -0.701 | -0.700 | -1.003 | -1.105 | -1.310 | -1.265 | -1.626 | -1.105 | -1.310 | -1.265 | -1.626 | ns |
| | | $t_h$ | 0.827 | 0.825 | 1.181 | 1.306 | 1.530 | 1.474 | 1.829 | 1.306 | 1.530 | 1.474 | 1.829 | ns |
| | GCLK PLL | $t_{su}$ | -0.986 | -0.986 | -1.404 | -1.534 | -1.772 | -1.712 | -2.025 | -1.534 | -1.772 | -1.712 | -2.025 | ns |
| | | $t_h$ | 1.237 | 1.237 | 1.773 | 1.949 | 2.231 | 2.147 | 2.470 | 1.949 | 2.231 | 2.147 | 2.470 | ns |


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Table 1–42 lists the EP3SL50 row pins input timing parameters for single-ended I/O standards.

**Table 1–42.** EP3SL50 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -0.884 | -0.914 | -1.291 | -1.412 | -1.634 | -1.580 | -1.842 | -1.428 | -1.639 | -1.588 | -1.875 | ns |
| | | $t_h$ | 0.997 | 1.040 | 1.554 | 1.774 | 1.924 | 1.808 | 1.834 | 1.768 | 1.931 | 1.777 | 1.885 | ns |
| | GCLK PLL | $t_{su}$ | 0.910 | 0.917 | 1.476 | 1.619 | 1.864 | 1.796 | 2.057 | 1.645 | 1.878 | 1.814 | 2.090 | ns |
| | | $t_h$ | -0.661 | -0.656 | -1.291 | -1.412 | -1.634 | -1.580 | -1.842 | -1.428 | -1.639 | -1.588 | -1.875 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -0.884 | -0.914 | -1.291 | -1.412 | -1.634 | -1.580 | -1.842 | -1.428 | -1.639 | -1.588 | -1.875 | ns |
| | | $t_h$ | 0.997 | 1.040 | 1.554 | 1.774 | 1.924 | 1.808 | 1.834 | 1.768 | 1.931 | 1.777 | 1.885 | ns |
| | GCLK PLL | $t_{su}$ | 0.910 | 0.917 | 1.476 | 1.619 | 1.864 | 1.796 | 2.057 | 1.645 | 1.878 | 1.814 | 2.090 | ns |
| | | $t_h$ | -0.661 | -0.656 | -1.288 | -1.413 | -1.637 | -1.583 | -1.845 | -1.427 | -1.644 | -1.593 | -1.880 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -0.890 | -0.925 | 1.473 | 1.620 | 1.867 | 1.799 | 2.060 | 1.644 | 1.883 | 1.819 | 2.095 | ns |
| | | $t_h$ | 1.003 | 1.051 | -1.288 | -1.413 | -1.637 | -1.583 | -1.845 | -1.427 | -1.644 | -1.593 | -1.880 | ns |
| | GCLK PLL | $t_{su}$ | 0.904 | 0.906 | 1.557 | 1.773 | 1.921 | 1.805 | 1.831 | 1.769 | 1.926 | 1.772 | 1.880 | ns |
| | | $t_h$ | -0.655 | -0.645 | 1.473 | 1.620 | 1.867 | 1.799 | 2.060 | 1.644 | 1.883 | 1.819 | 2.095 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -0.890 | -0.925 | 1.482 | 1.633 | 1.882 | 1.814 | 2.075 | 1.653 | 1.893 | 1.829 | 2.105 | ns |
| | | $t_h$ | 1.003 | 1.051 | -1.297 | -1.426 | -1.652 | -1.598 | -1.860 | -1.436 | -1.654 | -1.603 | -1.890 | ns |
| | GCLK PLL | $t_{su}$ | 0.904 | 0.906 | 1.548 | 1.760 | 1.906 | 1.790 | 1.816 | 1.760 | 1.916 | 1.762 | 1.870 | ns |
| | | $t_h$ | -0.655 | -0.645 | 1.482 | 1.633 | 1.882 | 1.814 | 2.075 | 1.653 | 1.893 | 1.829 | 2.105 | ns |
| 2.5 V | GCLK | $t_{su}$ | -0.878 | -0.918 | 1.551 | 1.770 | 1.914 | 1.799 | 1.828 | 1.772 | 1.922 | 1.804 | 1.879 | ns |
| | | $t_h$ | 0.991 | 1.044 | 1.554 | 1.698 | 1.914 | 1.845 | 2.111 | 1.718 | 1.928 | 1.862 | 2.141 | ns |
| | GCLK PLL | $t_{su}$ | 0.916 | 0.913 | -1.369 | -1.491 | -1.684 | -1.629 | -1.895 | -1.501 | -1.688 | -1.635 | -1.926 | ns |
| | | $t_h$ | -0.667 | -0.652 | 1.551 | 1.770 | 1.914 | 1.799 | 1.828 | 1.772 | 1.922 | 1.804 | 1.879 | ns |
| 1.8 V | GCLK | $t_{su}$ | -0.940 | -0.982 | 1.575 | 1.802 | 1.982 | 1.867 | 1.896 | 1.803 | 1.987 | 1.869 | 1.944 | ns |
| | | $t_h$ | 0.930 | 0.925 | 1.530 | 1.666 | 1.846 | 1.777 | 2.043 | 1.687 | 1.863 | 1.797 | 2.076 | ns |
| | GCLK PLL | $t_{su}$ | 1.054 | 1.109 | -1.345 | -1.459 | -1.616 | -1.561 | -1.827 | -1.470 | -1.623 | -1.570 | -1.861 | ns |
| | | $t_h$ | -0.930 | -0.971 | 1.654 | 1.903 | 2.141 | 2.026 | 2.055 | 1.899 | 2.142 | 2.024 | 2.099 | ns |
| 1.5 V | GCLK | $t_{su}$ | 0.940 | 0.936 | 1.451 | 1.565 | 1.687 | 1.618 | 1.884 | 1.591 | 1.708 | 1.642 | 1.921 | ns |
| | | $t_h$ | 1.044 | 1.098 | -1.266 | -1.358 | -1.457 | -1.402 | -1.668 | -1.374 | -1.468 | -1.415 | -1.706 | ns |
| | GCLK PLL | $t_{su}$ | -0.870 | -0.918 | 1.634 | 1.869 | 2.126 | 2.010 | 2.036 | 1.872 | 2.133 | 1.979 | 2.087 | ns |
| | | $t_h$ | 1.000 | 0.989 | 1.396 | 1.524 | 1.662 | 1.594 | 1.855 | 1.541 | 1.676 | 1.612 | 1.888 | ns |
| 1.2 V | GCLK | $t_{su}$ | 0.984 | 1.045 | -1.228 | -1.331 | -1.452 | -1.396 | -1.664 | -1.342 | -1.461 | -1.407 | -1.699 | ns |
| | | $t_h$ | -0.821 | -0.860 | 1.692 | -1.331 | -1.452 | -1.396 | -1.664 | -1.342 | -1.461 | -1.407 | -1.699 | ns |
| | GCLK PLL | $t_{su}$ | 0.973 | 0.971 | 1.413 | 1.536 | 1.680 | 1.611 | 1.876 | 1.557 | 1.698 | 1.633 | 1.910 | ns |
| | | $t_h$ | 0.935 | 0.987 | -1.228 | 1.930 | 2.146 | 2.032 | 2.059 | 1.931 | 2.149 | 2.032 | 2.106 | ns |

**Table 1–42.** EP3SL50 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -0.821 | -0.860 | 1.692 | 1.930 | 2.146 | 2.032 | 2.059 | 1.931 | 2.149 | 2.032 | 2.106 | ns |
| | | $t_h$ | 0.973 | 0.971 | 1.413 | -1.483 | -1.648 | -1.564 | -1.586 | -1.477 | -1.641 | -1.554 | -1.632 | ns |
| | GCLK PLL | $t_{su}$ | 0.935 | 0.987 | -1.228 | -1.331 | -1.452 | -1.396 | -1.664 | -1.342 | -1.461 | -1.407 | -1.699 | ns |
| | | $t_h$ | -0.844 | -0.883 | 1.692 | 1.536 | 1.680 | 1.611 | 1.876 | 1.557 | 1.698 | 1.633 | 1.910 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | 1.026 | 1.024 | 1.413 | 1.930 | 2.146 | 2.032 | 2.059 | 1.931 | 2.149 | 2.032 | 2.106 | ns |
| | | $t_h$ | 0.958 | 1.010 | -1.228 | -1.483 | -1.648 | -1.564 | -1.586 | -1.477 | -1.641 | -1.554 | -1.632 | ns |
| | GCLK PLL | $t_{su}$ | -0.844 | -0.883 | -1.309 | -1.321 | -1.434 | -1.378 | -1.646 | -1.331 | -1.444 | -1.390 | -1.682 | ns |
| | | $t_h$ | 1.026 | 1.024 | -1.213 | 1.526 | 1.662 | 1.593 | 1.858 | 1.546 | 1.681 | 1.616 | 1.893 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | 0.958 | 1.010 | 1.399 | 1.940 | 2.164 | 2.050 | 2.077 | 1.942 | 2.166 | 2.049 | 2.123 | ns |
| | | $t_h$ | -0.830 | -0.871 | 1.692 | 1.940 | 2.164 | 2.050 | 2.077 | 1.942 | 2.166 | 2.049 | 2.123 | ns |
| | GCLK PLL | $t_{su}$ | 1.040 | 1.036 | 1.413 | -1.493 | -1.666 | -1.582 | -1.604 | -1.488 | -1.658 | -1.571 | -1.649 | ns |
| | | $t_h$ | 0.944 | 0.998 | -1.228 | -1.321 | -1.434 | -1.378 | -1.646 | -1.331 | -1.444 | -1.390 | -1.682 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -0.844 | -0.883 | 1.692 | -1.483 | -1.648 | -1.564 | -1.586 | -1.477 | -1.641 | -1.554 | -1.632 | ns |
| | | $t_h$ | 1.026 | 1.024 | 1.413 | -1.331 | -1.452 | -1.396 | -1.664 | -1.342 | -1.461 | -1.407 | -1.699 | ns |
| | GCLK PLL | $t_{su}$ | 0.958 | 1.010 | -1.228 | 1.536 | 1.680 | 1.611 | 1.876 | 1.557 | 1.698 | 1.633 | 1.910 | ns |
| | | $t_h$ | -0.844 | -0.883 | -1.309 | 1.930 | 2.146 | 2.032 | 2.059 | 1.931 | 2.149 | 2.032 | 2.106 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | 1.026 | 1.024 | -1.213 | -1.483 | -1.648 | -1.564 | -1.586 | -1.477 | -1.641 | -1.554 | -1.632 | ns |
| | | $t_h$ | 0.958 | 1.010 | 1.399 | -1.331 | -1.452 | -1.396 | -1.664 | -1.342 | -1.461 | -1.407 | -1.699 | ns |
| | GCLK PLL | $t_{su}$ | -0.830 | -0.871 | 1.707 | 1.536 | 1.680 | 1.611 | 1.876 | 1.557 | 1.698 | 1.633 | 1.910 | ns |
| | | $t_h$ | 1.040 | 1.036 | -1.309 | 1.930 | 2.146 | 2.032 | 2.059 | 1.931 | 2.149 | 2.032 | 2.106 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | 0.944 | 0.998 | -1.213 | -1.483 | -1.648 | -1.564 | -1.586 | -1.477 | -1.641 | -1.554 | -1.632 | ns |
| | | $t_h$ | -0.830 | -0.871 | -1.318 | 1.940 | 2.164 | 2.050 | 2.077 | 1.942 | 2.166 | 2.049 | 2.123 | ns |
| | GCLK PLL | $t_{su}$ | 1.040 | 1.036 | -1.204 | -1.493 | -1.666 | -1.582 | -1.604 | -1.488 | -1.658 | -1.571 | -1.649 | ns |
| | | $t_h$ | 0.944 | 0.998 | 1.390 | -1.321 | -1.434 | -1.378 | -1.646 | -1.331 | -1.444 | -1.390 | -1.682 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.821 | -0.859 | 1.716 | 1.526 | 1.662 | 1.593 | 1.858 | 1.546 | 1.681 | 1.616 | 1.893 | ns |
| | | $t_h$ | 1.049 | 1.048 | -1.318 | 1.940 | 2.164 | 2.050 | 2.077 | 1.942 | 2.166 | 2.049 | 2.123 | ns |
| | GCLK PLL | $t_{su}$ | 0.935 | 0.986 | -1.204 | -1.493 | -1.666 | -1.582 | -1.604 | -1.488 | -1.658 | -1.571 | -1.649 | ns |
| | | $t_h$ | -0.821 | -0.859 | -1.318 | 1.950 | 2.180 | 2.066 | 2.093 | 1.951 | 2.182 | 2.065 | 2.139 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | 1.049 | 1.048 | -1.288 | -1.503 | -1.682 | -1.598 | -1.620 | -1.497 | -1.674 | -1.587 | -1.665 | ns |
| | | $t_h$ | 0.935 | 0.986 | 1.557 | -1.311 | -1.418 | -1.362 | -1.630 | -1.322 | -1.428 | -1.374 | -1.666 | ns |
| | GCLK PLL | $t_{su}$ | -0.890 | -0.925 | 1.473 | 1.516 | 1.646 | 1.577 | 1.842 | 1.537 | 1.665 | 1.600 | 1.877 | ns |
| | | $t_h$ | 1.003 | 1.051 | -1.288 | 1.950 | 2.180 | 2.066 | 2.093 | 1.951 | 2.182 | 2.065 | 2.139 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | 0.904 | 0.906 | 1.557 | -1.503 | -1.682 | -1.598 | -1.620 | -1.497 | -1.674 | -1.587 | -1.665 | ns |
| | | $t_h$ | -0.655 | -0.645 | 1.473 | -1.311 | -1.418 | -1.362 | -1.630 | -1.322 | -1.428 | -1.374 | -1.666 | ns |
| | GCLK PLL | $t_{su}$ | -0.890 | -0.925 | 1.473 | 1.516 | 1.646 | 1.577 | 1.842 | 1.537 | 1.665 | 1.600 | 1.877 | ns |
| | | $t_h$ | 1.003 | 1.051 | 1.473 | 1.950 | 2.180 | 2.066 | 2.093 | 1.951 | 2.182 | 2.065 | 2.139 | ns |

**Table 1–42.** EP3SL50 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | 0.904 | 0.906 | 1.473 | -1.503 | -1.682 | -1.598 | -1.620 | -1.497 | -1.674 | -1.587 | -1.665 | ns |
| | | $t_h$ | -0.655 | -0.645 | 1.473 | -1.311 | -1.418 | -1.362 | -1.630 | -1.322 | -1.428 | -1.374 | -1.666 | ns |
| | GCLK PLL | $t_{su}$ | -0.884 | -0.914 | -1.291 | -1.412 | -1.634 | -1.580 | -1.842 | -1.428 | -1.639 | -1.588 | -1.875 | ns |
| | | $t_h$ | 0.997 | 1.040 | 1.554 | 1.774 | 1.924 | 1.808 | 1.834 | 1.768 | 1.931 | 1.777 | 1.885 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | 0.910 | 0.917 | 1.476 | 1.619 | 1.864 | 1.796 | 2.057 | 1.645 | 1.878 | 1.814 | 2.090 | ns |
| | | $t_h$ | -0.661 | -0.656 | -1.291 | -1.412 | -1.634 | -1.580 | -1.842 | -1.428 | -1.639 | -1.588 | -1.875 | ns |
| | GCLK PLL | $t_{su}$ | -0.884 | -0.914 | -1.291 | -1.412 | -1.634 | -1.580 | -1.842 | -1.428 | -1.639 | -1.588 | -1.875 | ns |
| | | $t_h$ | 0.997 | 1.040 | 1.554 | 1.774 | 1.924 | 1.808 | 1.834 | 1.768 | 1.931 | 1.777 | 1.885 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | 0.910 | 0.917 | 1.476 | 1.619 | 1.864 | 1.796 | 2.057 | 1.645 | 1.878 | 1.814 | 2.090 | ns |
| | | $t_h$ | -0.661 | -0.656 | -1.288 | -1.413 | -1.637 | -1.583 | -1.845 | -1.427 | -1.644 | -1.593 | -1.880 | ns |
| | GCLK PLL | $t_{su}$ | -0.890 | -0.925 | 1.473 | 1.620 | 1.867 | 1.799 | 2.060 | 1.644 | 1.883 | 1.819 | 2.095 | ns |
| | | $t_h$ | 1.003 | 1.051 | -1.288 | -1.413 | -1.637 | -1.583 | -1.845 | -1.427 | -1.644 | -1.593 | -1.880 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | 0.904 | 0.906 | 1.557 | 1.773 | 1.921 | 1.805 | 1.831 | 1.769 | 1.926 | 1.772 | 1.880 | ns |
| | | $t_h$ | -0.655 | -0.645 | 1.473 | 1.620 | 1.867 | 1.799 | 2.060 | 1.644 | 1.883 | 1.819 | 2.095 | ns |
| | GCLK PLL | $t_{su}$ | -0.890 | -0.925 | 1.482 | 1.633 | 1.882 | 1.814 | 2.075 | 1.653 | 1.893 | 1.829 | 2.105 | ns |
| | | $t_h$ | 1.003 | 1.051 | -1.297 | -1.426 | -1.652 | -1.598 | -1.860 | -1.436 | -1.654 | -1.603 | -1.890 | ns |

Table 1–43 lists the EP3SL50 column pins output timing parameters for single-ended I/O standards.

**Table 1–43.** EP3SL50 Column Pins output Timing Parameters (Part 1 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.168 | 3.156 | 4.382 | 4.742 | 5.210 | 5.092 | 5.294 | 4.742 | 5.210 | 5.092 | 5.294 | ns |
| | | GCLK PLL | $t_{co}$ | 3.524 | 3.524 | 4.905 | 5.304 | 5.820 | 5.677 | 5.944 | 5.304 | 5.820 | 5.677 | 5.944 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.101 | 3.089 | 4.273 | 4.631 | 5.097 | 4.979 | 5.181 | 4.631 | 5.097 | 4.979 | 5.181 | ns |
| | | GCLK PLL | $t_{co}$ | 3.457 | 3.457 | 4.796 | 5.193 | 5.707 | 5.564 | 5.831 | 5.193 | 5.707 | 5.564 | 5.831 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.015 | 3.003 | 4.170 | 4.532 | 5.005 | 4.887 | 5.089 | 4.532 | 5.005 | 4.887 | 5.089 | ns |
| | | GCLK PLL | $t_{co}$ | 3.371 | 3.371 | 4.692 | 5.094 | 5.615 | 5.472 | 5.739 | 5.094 | 5.615 | 5.472 | 5.739 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.008 | 2.996 | 4.153 | 4.504 | 4.964 | 4.846 | 5.048 | 4.504 | 4.964 | 4.846 | 5.048 | ns |
| | | GCLK PLL | $t_{co}$ | 3.364 | 3.364 | 4.675 | 5.066 | 5.574 | 5.431 | 5.698 | 5.066 | 5.574 | 5.431 | 5.698 | ns |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.174 | 3.162 | 4.387 | 4.747 | 5.217 | 5.099 | 5.301 | 4.747 | 5.217 | 5.099 | 5.301 | ns |
| | | GCLK PLL | $t_{co}$ | 3.530 | 3.530 | 4.909 | 5.309 | 5.827 | 5.684 | 5.951 | 5.309 | 5.827 | 5.684 | 5.951 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.019 | 3.007 | 4.180 | 4.549 | 5.016 | 4.898 | 5.100 | 4.549 | 5.016 | 4.898 | 5.100 | ns |
| | | GCLK PLL | $t_{co}$ | 3.375 | 3.375 | 4.702 | 5.111 | 5.626 | 5.483 | 5.750 | 5.111 | 5.626 | 5.483 | 5.750 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.026 | 3.014 | 4.174 | 4.528 | 4.990 | 4.872 | 5.074 | 4.528 | 4.990 | 4.872 | 5.074 | ns |
| | | GCLK PLL | $t_{co}$ | 3.382 | 3.382 | 4.696 | 5.090 | 5.600 | 5.457 | 5.724 | 5.090 | 5.600 | 5.457 | 5.724 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.010 | 2.998 | 4.151 | 4.503 | 4.961 | 4.843 | 5.045 | 4.503 | 4.961 | 4.843 | 5.045 | ns |
| | | GCLK PLL | $t_{co}$ | 3.366 | 3.366 | 4.674 | 5.065 | 5.571 | 5.428 | 5.695 | 5.065 | 5.571 | 5.428 | 5.695 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.132 | 3.120 | 4.349 | 4.710 | 5.177 | 5.059 | 5.261 | 4.710 | 5.177 | 5.059 | 5.261 | ns |
| | | GCLK PLL | $t_{co}$ | 3.488 | 3.488 | 4.872 | 5.272 | 5.787 | 5.644 | 5.911 | 5.272 | 5.787 | 5.644 | 5.911 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.021 | 3.009 | 4.219 | 4.576 | 5.040 | 4.923 | 5.122 | 4.576 | 5.040 | 4.923 | 5.122 | ns |
| | | GCLK PLL | $t_{co}$ | 3.377 | 3.377 | 4.742 | 5.138 | 5.650 | 5.508 | 5.773 | 5.138 | 5.650 | 5.508 | 5.773 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.985 | 2.973 | 4.156 | 4.507 | 4.966 | 4.849 | 5.049 | 4.507 | 4.966 | 4.849 | 5.049 | ns |
| | | GCLK PLL | $t_{co}$ | 3.341 | 3.341 | 4.679 | 5.069 | 5.576 | 5.434 | 5.699 | 5.069 | 5.576 | 5.434 | 5.699 | ns |
| | 16mA | GCLK | $t_{co}$ | 2.967 | 2.955 | 4.127 | 4.479 | 4.937 | 4.819 | 5.021 | 4.479 | 4.937 | 4.819 | 5.021 | ns |
| | | GCLK PLL | $t_{co}$ | 3.323 | 3.323 | 4.650 | 5.041 | 5.547 | 5.404 | 5.671 | 5.041 | 5.547 | 5.404 | 5.671 | ns |


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**Table 1–43.** EP3SL50 Column Pins output Timing Parameters (Part 2 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.046 | 3.034 | 4.253 | 4.610 | 5.075 | 4.958 | 5.157 | 4.610 | 5.075 | 4.958 | 5.157 | ns |
| | | GCLK PLL | $t_{co}$ | 3.402 | 3.402 | 4.776 | 5.172 | 5.685 | 5.543 | 5.808 | 5.172 | 5.685 | 5.543 | 5.808 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.967 | 2.955 | 4.130 | 4.481 | 4.940 | 4.823 | 5.022 | 4.481 | 4.940 | 4.823 | 5.022 | ns |
| | | GCLK PLL | $t_{co}$ | 3.323 | 3.323 | 4.652 | 5.043 | 5.550 | 5.408 | 5.673 | 5.043 | 5.550 | 5.408 | 5.673 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.962 | 2.950 | 4.122 | 4.474 | 4.931 | 4.813 | 5.015 | 4.474 | 4.931 | 4.813 | 5.015 | ns |
| | | GCLK PLL | $t_{co}$ | 3.318 | 3.318 | 4.645 | 5.036 | 5.541 | 5.398 | 5.665 | 5.036 | 5.541 | 5.398 | 5.665 | ns |
| | 16mA | GCLK | $t_{co}$ | 2.953 | 2.941 | 4.108 | 4.459 | 4.916 | 4.798 | 5.000 | 4.459 | 4.916 | 4.798 | 5.000 | ns |
| | | GCLK PLL | $t_{co}$ | 3.309 | 3.309 | 4.631 | 5.021 | 5.526 | 5.383 | 5.650 | 5.021 | 5.526 | 5.383 | 5.650 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.168 | 3.156 | 4.460 | 4.837 | 5.322 | 5.205 | 5.405 | 4.837 | 5.322 | 5.205 | 5.405 | ns |
| | | GCLK PLL | $t_{co}$ | 3.524 | 3.524 | 4.983 | 5.399 | 5.932 | 5.790 | 6.055 | 5.399 | 5.932 | 5.790 | 6.055 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.068 | 3.056 | 4.341 | 4.711 | 5.190 | 5.073 | 5.272 | 4.711 | 5.190 | 5.073 | 5.272 | ns |
| | | GCLK PLL | $t_{co}$ | 3.424 | 3.424 | 4.864 | 5.273 | 5.800 | 5.658 | 5.923 | 5.273 | 5.800 | 5.658 | 5.923 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.024 | 3.012 | 4.254 | 4.620 | 5.094 | 4.976 | 5.178 | 4.620 | 5.094 | 4.976 | 5.178 | ns |
| | | GCLK PLL | $t_{co}$ | 3.380 | 3.380 | 4.777 | 5.182 | 5.704 | 5.561 | 5.828 | 5.182 | 5.704 | 5.561 | 5.828 | ns |
| | 16mA | GCLK | $t_{co}$ | 2.986 | 2.974 | 4.215 | 4.578 | 5.051 | 4.933 | 5.135 | 4.578 | 5.051 | 4.933 | 5.135 | ns |
| | | GCLK PLL | $t_{co}$ | 3.342 | 3.342 | 4.738 | 5.140 | 5.661 | 5.518 | 5.785 | 5.140 | 5.661 | 5.518 | 5.785 | ns |

**Table 1–43.** EP3SL50 Column Pins output Timing Parameters (Part 3 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.359 | 3.347 | 4.782 | 5.197 | 5.726 | 5.608 | 5.810 | 5.197 | 5.726 | 5.608 | 5.810 | ns |
| | | GCLK PLL | $t_{co}$ | 3.715 | 3.715 | 5.304 | 5.759 | 6.336 | 6.193 | 6.460 | 5.759 | 6.336 | 6.193 | 6.460 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.178 | 3.166 | 4.503 | 4.888 | 5.379 | 5.262 | 5.461 | 4.888 | 5.379 | 5.262 | 5.461 | ns |
| | | GCLK PLL | $t_{co}$ | 3.534 | 3.534 | 5.025 | 5.450 | 5.989 | 5.847 | 6.112 | 5.450 | 5.989 | 5.847 | 6.112 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.096 | 3.084 | 4.396 | 4.773 | 5.268 | 5.150 | 5.352 | 4.773 | 5.268 | 5.150 | 5.352 | ns |
| | | GCLK PLL | $t_{co}$ | 3.452 | 3.452 | 4.918 | 5.335 | 5.878 | 5.735 | 6.002 | 5.335 | 5.878 | 5.735 | 6.002 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.076 | 3.064 | 4.337 | 4.719 | 5.202 | 5.084 | 5.286 | 4.719 | 5.202 | 5.084 | 5.286 | ns |
| | | GCLK PLL | $t_{co}$ | 3.432 | 3.432 | 4.860 | 5.281 | 5.812 | 5.669 | 5.936 | 5.281 | 5.812 | 5.669 | 5.936 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.013 | 3.001 | 4.276 | 4.644 | 5.121 | 5.003 | 5.205 | 4.644 | 5.121 | 5.003 | 5.205 | ns |
| | | GCLK PLL | $t_{co}$ | 3.369 | 3.369 | 4.799 | 5.206 | 5.731 | 5.588 | 5.855 | 5.206 | 5.731 | 5.588 | 5.855 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.995 | 2.983 | 4.256 | 4.623 | 5.098 | 4.980 | 5.182 | 4.623 | 5.098 | 4.980 | 5.182 | ns |
| | | GCLK PLL | $t_{co}$ | 3.351 | 3.351 | 4.778 | 5.185 | 5.708 | 5.565 | 5.832 | 5.185 | 5.708 | 5.565 | 5.832 | ns |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.305 | 3.293 | 4.710 | 5.129 | 5.664 | 5.546 | 5.748 | 5.129 | 5.664 | 5.546 | 5.748 | ns |
| | | GCLK PLL | $t_{co}$ | 3.661 | 3.661 | 5.233 | 5.691 | 6.274 | 6.131 | 6.398 | 5.691 | 6.274 | 6.131 | 6.398 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.093 | 3.081 | 4.391 | 4.773 | 5.272 | 5.154 | 5.356 | 4.773 | 5.272 | 5.154 | 5.356 | ns |
| | | GCLK PLL | $t_{co}$ | 3.449 | 3.449 | 4.914 | 5.335 | 5.882 | 5.739 | 6.006 | 5.335 | 5.882 | 5.739 | 6.006 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.068 | 3.056 | 4.324 | 4.713 | 5.205 | 5.087 | 5.289 | 4.713 | 5.205 | 5.087 | 5.289 | ns |
| | | GCLK PLL | $t_{co}$ | 3.424 | 3.424 | 4.847 | 5.275 | 5.815 | 5.672 | 5.939 | 5.275 | 5.815 | 5.672 | 5.939 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.057 | 3.045 | 4.307 | 4.688 | 5.185 | 5.067 | 5.269 | 4.688 | 5.185 | 5.067 | 5.269 | ns |
| | | GCLK PLL | $t_{co}$ | 3.413 | 3.413 | 4.830 | 5.250 | 5.795 | 5.652 | 5.919 | 5.250 | 5.795 | 5.652 | 5.919 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.002 | 2.990 | 4.269 | 4.637 | 5.115 | 4.997 | 5.199 | 4.637 | 5.115 | 4.997 | 5.199 | ns |
| | | GCLK PLL | $t_{co}$ | 3.358 | 3.358 | 4.792 | 5.199 | 5.725 | 5.582 | 5.849 | 5.199 | 5.725 | 5.582 | 5.849 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.997 | 2.985 | 4.253 | 4.626 | 5.104 | 4.986 | 5.188 | 4.626 | 5.104 | 4.986 | 5.188 | ns |
| | | GCLK PLL | $t_{co}$ | 3.353 | 3.353 | 4.775 | 5.188 | 5.714 | 5.571 | 5.838 | 5.188 | 5.714 | 5.571 | 5.838 | ns |


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**Table 1–43.** EP3SL50 Column Pins output Timing Parameters (Part 4 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.221 | 3.209 | 4.636 | 5.065 | 5.608 | 5.490 | 5.692 | 5.065 | 5.608 | 5.490 | 5.692 | ns |
| | | GCLK PLL | $t_{co}$ | 3.577 | 3.577 | 5.159 | 5.627 | 6.218 | 6.075 | 6.342 | 5.627 | 6.218 | 6.075 | 6.342 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.098 | 3.086 | 4.411 | 4.803 | 5.322 | 5.204 | 5.406 | 4.803 | 5.322 | 5.204 | 5.406 | ns |
| | | GCLK PLL | $t_{co}$ | 3.454 | 3.454 | 4.933 | 5.365 | 5.932 | 5.789 | 6.056 | 5.365 | 5.932 | 5.789 | 6.056 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.060 | 3.048 | 4.318 | 4.714 | 5.209 | 5.091 | 5.293 | 4.714 | 5.209 | 5.091 | 5.293 | ns |
| | | GCLK PLL | $t_{co}$ | 3.416 | 3.416 | 4.841 | 5.276 | 5.819 | 5.676 | 5.943 | 5.276 | 5.819 | 5.676 | 5.943 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.013 | 3.001 | 4.290 | 4.665 | 5.153 | 5.035 | 5.237 | 4.665 | 5.153 | 5.035 | 5.237 | ns |
| | | GCLK PLL | $t_{co}$ | 3.369 | 3.369 | 4.813 | 5.227 | 5.763 | 5.620 | 5.887 | 5.227 | 5.763 | 5.620 | 5.887 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.013 | 3.001 | 4.247 | 4.612 | 5.084 | 4.966 | 5.168 | 4.612 | 5.084 | 4.966 | 5.168 | ns |
| | | GCLK PLL | $t_{co}$ | 3.369 | 3.369 | 4.770 | 5.174 | 5.694 | 5.551 | 5.818 | 5.174 | 5.694 | 5.551 | 5.818 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.010 | 2.998 | 4.244 | 4.609 | 5.080 | 4.962 | 5.164 | 4.609 | 5.080 | 4.962 | 5.164 | ns |
| | | GCLK PLL | $t_{co}$ | 3.366 | 3.366 | 4.767 | 5.171 | 5.690 | 5.547 | 5.814 | 5.171 | 5.690 | 5.547 | 5.814 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.008 | 2.996 | 4.244 | 4.610 | 5.081 | 4.963 | 5.165 | 4.610 | 5.081 | 4.963 | 5.165 | ns |
| | | GCLK PLL | $t_{co}$ | 3.364 | 3.364 | 4.767 | 5.172 | 5.691 | 5.548 | 5.815 | 5.172 | 5.691 | 5.548 | 5.815 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 2.999 | 2.987 | 4.230 | 4.594 | 5.066 | 4.948 | 5.150 | 4.594 | 5.066 | 4.948 | 5.150 | ns |
| | | GCLK PLL | $t_{co}$ | 3.355 | 3.355 | 4.752 | 5.156 | 5.676 | 5.533 | 5.800 | 5.156 | 5.676 | 5.533 | 5.800 | ns |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.020 | 3.008 | 4.259 | 4.626 | 5.100 | 4.982 | 5.184 | 4.626 | 5.100 | 4.982 | 5.184 | ns |
| | | GCLK PLL | $t_{co}$ | 3.376 | 3.376 | 4.782 | 5.188 | 5.710 | 5.567 | 5.834 | 5.188 | 5.710 | 5.567 | 5.834 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.016 | 3.004 | 4.257 | 4.624 | 5.098 | 4.980 | 5.182 | 4.624 | 5.098 | 4.980 | 5.182 | ns |
| | | GCLK PLL | $t_{co}$ | 3.372 | 3.372 | 4.780 | 5.186 | 5.708 | 5.565 | 5.832 | 5.186 | 5.708 | 5.565 | 5.832 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.005 | 2.993 | 4.247 | 4.615 | 5.089 | 4.971 | 5.173 | 4.615 | 5.089 | 4.971 | 5.173 | ns |
| | | GCLK PLL | $t_{co}$ | 3.361 | 3.361 | 4.770 | 5.177 | 5.699 | 5.556 | 5.823 | 5.177 | 5.699 | 5.556 | 5.823 | ns |
| | 10mA | GCLK | $t_{co}$ | 2.994 | 2.982 | 4.235 | 4.602 | 5.076 | 4.958 | 5.160 | 4.602 | 5.076 | 4.958 | 5.160 | ns |
| | | GCLK PLL | $t_{co}$ | 3.350 | 3.350 | 4.757 | 5.164 | 5.686 | 5.543 | 5.810 | 5.164 | 5.686 | 5.543 | 5.810 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.994 | 2.982 | 4.234 | 4.602 | 5.076 | 4.958 | 5.160 | 4.602 | 5.076 | 4.958 | 5.160 | ns |
| | | GCLK PLL | $t_{co}$ | 3.350 | 3.350 | 4.757 | 5.164 | 5.686 | 5.543 | 5.810 | 5.164 | 5.686 | 5.543 | 5.810 | ns |

**Table 1–43.** EP3SL50 Column Pins output Timing Parameters (Part 5 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.000 | 2.988 | 4.233 | 4.599 | 5.071 | 4.953 | 5.155 | 4.599 | 5.071 | 4.953 | 5.155 | ns |
| | | GCLK PLL | $t_{co}$ | 3.356 | 3.356 | 4.756 | 5.161 | 5.681 | 5.538 | 5.805 | 5.161 | 5.681 | 5.538 | 5.805 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.003 | 2.991 | 4.241 | 4.608 | 5.083 | 4.965 | 5.167 | 4.608 | 5.083 | 4.965 | 5.167 | ns |
| | | GCLK PLL | $t_{co}$ | 3.359 | 3.359 | 4.764 | 5.170 | 5.693 | 5.550 | 5.817 | 5.170 | 5.693 | 5.550 | 5.817 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.024 | 3.012 | 4.269 | 4.638 | 5.113 | 4.995 | 5.197 | 4.638 | 5.113 | 4.995 | 5.197 | ns |
| | | GCLK PLL | $t_{co}$ | 3.380 | 3.380 | 4.791 | 5.200 | 5.723 | 5.580 | 5.847 | 5.200 | 5.723 | 5.580 | 5.847 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.010 | 2.998 | 4.258 | 4.628 | 5.104 | 4.986 | 5.188 | 4.628 | 5.104 | 4.986 | 5.188 | ns |
| | | GCLK PLL | $t_{co}$ | 3.366 | 3.366 | 4.781 | 5.190 | 5.714 | 5.571 | 5.838 | 5.190 | 5.714 | 5.571 | 5.838 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.999 | 2.987 | 4.245 | 4.614 | 5.090 | 4.972 | 5.174 | 4.614 | 5.090 | 4.972 | 5.174 | ns |
| | | GCLK PLL | $t_{co}$ | 3.355 | 3.355 | 4.767 | 5.176 | 5.700 | 5.557 | 5.824 | 5.176 | 5.700 | 5.557 | 5.824 | ns |
| | 10mA | GCLK | $t_{co}$ | 2.998 | 2.986 | 4.248 | 4.617 | 5.094 | 4.976 | 5.178 | 4.617 | 5.094 | 4.976 | 5.178 | ns |
| | | GCLK PLL | $t_{co}$ | 3.354 | 3.354 | 4.770 | 5.179 | 5.704 | 5.561 | 5.828 | 5.179 | 5.704 | 5.561 | 5.828 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.995 | 2.983 | 4.242 | 4.612 | 5.088 | 4.970 | 5.172 | 4.612 | 5.088 | 4.970 | 5.172 | ns |
| | | GCLK PLL | $t_{co}$ | 3.351 | 3.351 | 4.765 | 5.174 | 5.698 | 5.555 | 5.822 | 5.174 | 5.698 | 5.555 | 5.822 | ns |
| SSTL-15 CLASS II | 8mA | GCLK | $t_{co}$ | 2.997 | 2.985 | 4.231 | 4.598 | 5.071 | 4.953 | 5.155 | 4.598 | 5.071 | 4.953 | 5.155 | ns |
| | | GCLK PLL | $t_{co}$ | 3.353 | 3.353 | 4.754 | 5.160 | 5.681 | 5.538 | 5.805 | 5.160 | 5.681 | 5.538 | 5.805 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.000 | 2.988 | 4.238 | 4.607 | 5.082 | 4.964 | 5.166 | 4.607 | 5.082 | 4.964 | 5.166 | ns |
| | | GCLK PLL | $t_{co}$ | 3.356 | 3.356 | 4.761 | 5.169 | 5.692 | 5.549 | 5.816 | 5.169 | 5.692 | 5.549 | 5.816 | ns |


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**Table 1–43.** EP3SL50 Column Pins output Timing Parameters (Part 6 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.007 | 2.995 | 4.233 | 4.598 | 5.069 | 4.951 | 5.153 | 4.598 | 5.069 | 4.951 | 5.153 | ns |
| | | GCLK PLL | $t_{co}$ | 3.363 | 3.363 | 4.756 | 5.160 | 5.679 | 5.536 | 5.803 | 5.160 | 5.679 | 5.536 | 5.803 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.000 | 2.988 | 4.231 | 4.596 | 5.068 | 4.950 | 5.152 | 4.596 | 5.068 | 4.950 | 5.152 | ns |
| | | GCLK PLL | $t_{co}$ | 3.356 | 3.356 | 4.754 | 5.158 | 5.678 | 5.535 | 5.802 | 5.158 | 5.678 | 5.535 | 5.802 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.992 | 2.980 | 4.224 | 4.589 | 5.061 | 4.943 | 5.145 | 4.589 | 5.061 | 4.943 | 5.145 | ns |
| | | GCLK PLL | $t_{co}$ | 3.348 | 3.348 | 4.746 | 5.151 | 5.671 | 5.528 | 5.795 | 5.151 | 5.671 | 5.528 | 5.795 | ns |
| | 10mA | GCLK | $t_{co}$ | 2.995 | 2.983 | 4.227 | 4.592 | 5.065 | 4.947 | 5.149 | 4.592 | 5.065 | 4.947 | 5.149 | ns |
| | | GCLK PLL | $t_{co}$ | 3.351 | 3.351 | 4.749 | 5.154 | 5.675 | 5.532 | 5.799 | 5.154 | 5.675 | 5.532 | 5.799 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.992 | 2.980 | 4.229 | 4.596 | 5.069 | 4.951 | 5.153 | 4.596 | 5.069 | 4.951 | 5.153 | ns |
| | | GCLK PLL | $t_{co}$ | 3.348 | 3.348 | 4.752 | 5.158 | 5.679 | 5.536 | 5.803 | 5.158 | 5.679 | 5.536 | 5.803 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.000 | 2.988 | 4.228 | 4.593 | 5.065 | 4.947 | 5.149 | 4.593 | 5.065 | 4.947 | 5.149 | ns |
| | | GCLK PLL | $t_{co}$ | 3.356 | 3.356 | 4.751 | 5.155 | 5.675 | 5.532 | 5.799 | 5.155 | 5.675 | 5.532 | 5.799 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.012 | 3.000 | 4.242 | 4.608 | 5.080 | 4.962 | 5.164 | 4.608 | 5.080 | 4.962 | 5.164 | ns |
| | | GCLK PLL | $t_{co}$ | 3.368 | 3.368 | 4.764 | 5.170 | 5.690 | 5.547 | 5.814 | 5.170 | 5.690 | 5.547 | 5.814 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.008 | 2.996 | 4.243 | 4.609 | 5.083 | 4.965 | 5.167 | 4.609 | 5.083 | 4.965 | 5.167 | ns |
| | | GCLK PLL | $t_{co}$ | 3.364 | 3.364 | 4.765 | 5.171 | 5.693 | 5.550 | 5.817 | 5.171 | 5.693 | 5.550 | 5.817 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.004 | 2.992 | 4.238 | 4.605 | 5.078 | 4.960 | 5.162 | 4.605 | 5.078 | 4.960 | 5.162 | ns |
| | | GCLK PLL | $t_{co}$ | 3.360 | 3.360 | 4.761 | 5.167 | 5.688 | 5.545 | 5.812 | 5.167 | 5.688 | 5.545 | 5.812 | ns |
| | 10mA | GCLK | $t_{co}$ | 2.997 | 2.985 | 4.231 | 4.598 | 5.071 | 4.953 | 5.155 | 4.598 | 5.071 | 4.953 | 5.155 | ns |
| | | GCLK PLL | $t_{co}$ | 3.353 | 3.353 | 4.754 | 5.160 | 5.681 | 5.538 | 5.805 | 5.160 | 5.681 | 5.538 | 5.805 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.998 | 2.986 | 4.238 | 4.606 | 5.081 | 4.963 | 5.165 | 4.606 | 5.081 | 4.963 | 5.165 | ns |
| | | GCLK PLL | $t_{co}$ | 3.354 | 3.354 | 4.761 | 5.168 | 5.691 | 5.548 | 5.815 | 5.168 | 5.691 | 5.548 | 5.815 | ns |
| 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 2.996 | 2.984 | 4.219 | 4.584 | 5.055 | 4.937 | 5.139 | 4.584 | 5.055 | 4.937 | 5.139 | ns |
| | | GCLK PLL | $t_{co}$ | 3.352 | 3.352 | 4.742 | 5.146 | 5.665 | 5.522 | 5.789 | 5.146 | 5.665 | 5.522 | 5.789 | ns |

**Table 1–43.** EP3SL50 Column Pins output Timing Parameters (Part 7 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.015 | 3.003 | 4.256 | 4.625 | 5.101 | 4.983 | 5.185 | 4.625 | 5.101 | 4.983 | 5.185 | ns |
| | | GCLK PLL | $t_{co}$ | 3.371 | 3.371 | 4.778 | 5.187 | 5.711 | 5.568 | 5.835 | 5.187 | 5.711 | 5.568 | 5.835 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.007 | 2.995 | 4.247 | 4.616 | 5.092 | 4.974 | 5.176 | 4.616 | 5.092 | 4.974 | 5.176 | ns |
| | | GCLK PLL | $t_{co}$ | 3.363 | 3.363 | 4.769 | 5.178 | 5.702 | 5.559 | 5.826 | 5.178 | 5.702 | 5.559 | 5.826 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.008 | 2.996 | 4.254 | 4.624 | 5.101 | 4.983 | 5.185 | 4.624 | 5.101 | 4.983 | 5.185 | ns |
| | | GCLK PLL | $t_{co}$ | 3.364 | 3.364 | 4.777 | 5.186 | 5.711 | 5.568 | 5.835 | 5.186 | 5.711 | 5.568 | 5.835 | ns |
| | 10mA | GCLK | $t_{co}$ | 2.997 | 2.985 | 4.241 | 4.611 | 5.087 | 4.969 | 5.171 | 4.611 | 5.087 | 4.969 | 5.171 | ns |
| | | GCLK PLL | $t_{co}$ | 3.353 | 3.353 | 4.764 | 5.173 | 5.697 | 5.554 | 5.821 | 5.173 | 5.697 | 5.554 | 5.821 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.997 | 2.985 | 4.241 | 4.611 | 5.088 | 4.970 | 5.172 | 4.611 | 5.088 | 4.970 | 5.172 | ns |
| | | GCLK PLL | $t_{co}$ | 3.353 | 3.353 | 4.764 | 5.173 | 5.698 | 5.555 | 5.822 | 5.173 | 5.698 | 5.555 | 5.822 | ns |
| 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.018 | 3.006 | 4.257 | 4.626 | 5.101 | 4.983 | 5.185 | 4.626 | 5.101 | 4.983 | 5.185 | ns |
| | | GCLK PLL | $t_{co}$ | 3.374 | 3.374 | 4.780 | 5.188 | 5.711 | 5.568 | 5.835 | 5.188 | 5.711 | 5.568 | 5.835 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.121 | 3.109 | 4.302 | 4.660 | 5.126 | 5.008 | 5.210 | 4.660 | 5.126 | 5.008 | 5.210 | ns |
| | | GCLK PLL | $t_{co}$ | 3.477 | 3.477 | 4.825 | 5.222 | 5.736 | 5.593 | 5.860 | 5.222 | 5.736 | 5.593 | 5.860 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.121 | 3.109 | 4.302 | 4.660 | 5.126 | 5.008 | 5.210 | 4.660 | 5.126 | 5.008 | 5.210 | ns |
| | | GCLK PLL | $t_{co}$ | 3.477 | 3.477 | 4.825 | 5.222 | 5.736 | 5.593 | 5.860 | 5.222 | 5.736 | 5.593 | 5.860 | ns |

Table 1–44 lists the EP3SL50 row pins output timing parameters for single-ended I/O standards.

**Table 1–44.** EP3SL50 Row Pins output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.197 | 3.438 | 4.781 | 5.176 | 5.684 | 5.549 | 5.751 | 5.305 | 5.818 | 5.682 | 5.828 | ns |
| | | GCLK PLL | $t_{co}$ | 1.482 | 1.677 | 2.061 | 2.175 | 2.372 | 2.388 | 2.308 | 2.295 | 2.495 | 2.512 | 2.303 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.104 | 3.333 | 4.651 | 5.038 | 5.540 | 5.405 | 5.607 | 5.164 | 5.669 | 5.533 | 5.679 | ns |
| | | GCLK PLL | $t_{co}$ | 1.415 | 1.606 | 1.951 | 2.037 | 2.228 | 2.244 | 2.164 | 2.154 | 2.346 | 2.363 | 2.154 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.014 | 3.233 | 4.532 | 4.915 | 5.412 | 5.277 | 5.479 | 5.037 | 5.537 | 5.401 | 5.547 | ns |
| | | GCLK PLL | $t_{co}$ | 1.336 | 1.517 | 1.845 | 1.930 | 2.100 | 2.116 | 2.036 | 2.046 | 2.214 | 2.260 | 2.022 | ns |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.207 | 3.442 | 4.789 | 5.181 | 5.689 | 5.554 | 5.756 | 5.311 | 5.823 | 5.687 | 5.833 | ns |
| | | GCLK PLL | $t_{co}$ | 1.492 | 1.684 | 2.065 | 2.180 | 2.377 | 2.393 | 2.313 | 2.301 | 2.500 | 2.517 | 2.308 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.018 | 3.237 | 4.538 | 4.921 | 5.418 | 5.283 | 5.485 | 5.043 | 5.544 | 5.408 | 5.554 | ns |
| | | GCLK PLL | $t_{co}$ | 1.340 | 1.521 | 1.856 | 1.945 | 2.106 | 2.122 | 2.042 | 2.058 | 2.221 | 2.269 | 2.029 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.151 | 3.384 | 4.733 | 5.129 | 5.641 | 5.506 | 5.708 | 5.262 | 5.776 | 5.640 | 5.786 | ns |
| | | GCLK PLL | $t_{co}$ | 1.442 | 1.638 | 2.028 | 2.128 | 2.329 | 2.345 | 2.265 | 2.252 | 2.453 | 2.470 | 2.261 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.026 | 3.257 | 4.580 | 4.970 | 5.477 | 5.342 | 5.544 | 5.100 | 5.612 | 5.475 | 5.621 | ns |
| | | GCLK PLL | $t_{co}$ | 1.341 | 1.526 | 1.891 | 1.969 | 2.165 | 2.181 | 2.101 | 2.090 | 2.289 | 2.305 | 2.096 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.987 | 3.206 | 4.498 | 4.887 | 5.389 | 5.254 | 5.456 | 5.014 | 5.519 | 5.382 | 5.528 | ns |
| | | GCLK PLL | $t_{co}$ | 1.304 | 1.488 | 1.831 | 1.903 | 2.077 | 2.093 | 2.013 | 2.016 | 2.196 | 2.222 | 2.003 | ns |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.065 | 3.303 | 4.627 | 5.022 | 5.530 | 5.395 | 5.597 | 5.154 | 5.665 | 5.528 | 5.674 | ns |
| | | GCLK PLL | $t_{co}$ | 1.363 | 1.550 | 1.926 | 2.021 | 2.218 | 2.234 | 2.154 | 2.144 | 2.342 | 2.358 | 2.149 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.969 | 3.188 | 4.463 | 4.848 | 5.350 | 5.215 | 5.417 | 4.974 | 5.479 | 5.342 | 5.488 | ns |
| | | GCLK PLL | $t_{co}$ | 1.291 | 1.472 | 1.803 | 1.874 | 2.038 | 2.054 | 1.974 | 1.986 | 2.156 | 2.193 | 1.963 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.177 | 3.420 | 4.865 | 5.283 | 5.813 | 5.678 | 5.880 | 5.422 | 5.955 | 5.818 | 5.964 | ns |
| | | GCLK PLL | $t_{co}$ | 1.468 | 1.675 | 2.136 | 2.282 | 2.501 | 2.517 | 2.437 | 2.412 | 2.632 | 2.648 | 2.439 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.067 | 3.321 | 4.710 | 5.120 | 5.643 | 5.508 | 5.710 | 5.255 | 5.781 | 5.644 | 5.790 | ns |
| | | GCLK PLL | $t_{co}$ | 1.383 | 1.572 | 2.012 | 2.119 | 2.331 | 2.347 | 2.267 | 2.245 | 2.458 | 2.474 | 2.265 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.021 | 3.245 | 4.599 | 5.001 | 5.517 | 5.382 | 5.584 | 5.132 | 5.651 | 5.514 | 5.660 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.528 | 1.928 | 2.015 | 2.205 | 2.221 | 2.141 | 2.132 | 2.328 | 2.354 | 2.135 | ns |

**Table 1–44.** EP3SL50 Row Pins output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.410 | 3.667 | 5.251 | 5.711 | 6.288 | 6.153 | 6.355 | 5.859 | 6.439 | 6.303 | 6.449 | ns |
| | | GCLK PLL | $t_{co}$ | 1.695 | 1.941 | 2.589 | 2.710 | 2.976 | 2.992 | 2.912 | 2.849 | 3.116 | 3.133 | 2.924 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.191 | 3.465 | 4.924 | 5.343 | 5.883 | 5.748 | 5.950 | 5.494 | 6.033 | 5.896 | 6.042 | ns |
| | | GCLK PLL | $t_{co}$ | 1.470 | 1.739 | 2.262 | 2.342 | 2.571 | 2.587 | 2.507 | 2.484 | 2.710 | 2.726 | 2.517 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.120 | 3.363 | 4.771 | 5.193 | 5.724 | 5.589 | 5.791 | 5.326 | 5.860 | 5.724 | 5.870 | ns |
| | | GCLK PLL | $t_{co}$ | 1.405 | 1.637 | 2.109 | 2.192 | 2.412 | 2.428 | 2.348 | 2.316 | 2.537 | 2.554 | 2.345 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.098 | 3.327 | 4.698 | 5.111 | 5.630 | 5.494 | 5.701 | 5.242 | 5.766 | 5.630 | 5.776 | ns |
| | | GCLK PLL | $t_{co}$ | 1.367 | 1.563 | 2.032 | 2.099 | 2.316 | 2.332 | 2.252 | 2.221 | 2.443 | 2.460 | 2.251 | ns |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.321 | 3.585 | 5.161 | 5.625 | 6.216 | 6.081 | 6.283 | 5.766 | 6.363 | 6.227 | 6.373 | ns |
| | | GCLK PLL | $t_{co}$ | 1.606 | 1.859 | 2.499 | 2.624 | 2.904 | 2.920 | 2.840 | 2.756 | 3.040 | 3.057 | 2.848 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.114 | 3.344 | 4.756 | 5.188 | 5.725 | 5.590 | 5.792 | 5.320 | 5.859 | 5.723 | 5.869 | ns |
| | | GCLK PLL | $t_{co}$ | 1.383 | 1.602 | 2.094 | 2.187 | 2.413 | 2.429 | 2.349 | 2.310 | 2.536 | 2.553 | 2.344 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.087 | 3.318 | 4.683 | 5.103 | 5.630 | 5.494 | 5.701 | 5.235 | 5.762 | 5.627 | 5.773 | ns |
| | | GCLK PLL | $t_{co}$ | 1.356 | 1.554 | 2.021 | 2.091 | 2.307 | 2.323 | 2.243 | 2.212 | 2.431 | 2.448 | 2.239 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.068 | 3.307 | 4.666 | 5.079 | 5.611 | 5.475 | 5.682 | 5.211 | 5.743 | 5.608 | 5.754 | ns |
| | | GCLK PLL | $t_{co}$ | 1.337 | 1.545 | 1.999 | 2.073 | 2.288 | 2.304 | 2.224 | 2.194 | 2.409 | 2.426 | 2.217 | ns |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.264 | 3.510 | 5.071 | 5.539 | 6.141 | 6.006 | 6.208 | 5.678 | 6.279 | 6.143 | 6.289 | ns |
| | | GCLK PLL | $t_{co}$ | 1.549 | 1.784 | 2.409 | 2.538 | 2.829 | 2.845 | 2.765 | 2.668 | 2.956 | 2.973 | 2.764 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.119 | 3.348 | 4.778 | 5.216 | 5.766 | 5.631 | 5.833 | 5.345 | 5.901 | 5.765 | 5.911 | ns |
| | | GCLK PLL | $t_{co}$ | 1.388 | 1.595 | 2.116 | 2.215 | 2.454 | 2.470 | 2.390 | 2.335 | 2.578 | 2.595 | 2.386 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.008 | 3.232 | 4.577 | 4.973 | 5.485 | 5.350 | 5.552 | 5.099 | 5.613 | 5.477 | 5.623 | ns |
| | | GCLK PLL | $t_{co}$ | 1.330 | 1.516 | 1.921 | 2.006 | 2.173 | 2.189 | 2.109 | 2.119 | 2.290 | 2.340 | 2.098 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.003 | 3.228 | 4.571 | 4.968 | 5.477 | 5.342 | 5.544 | 5.095 | 5.606 | 5.470 | 5.616 | ns |
| | | GCLK PLL | $t_{co}$ | 1.325 | 1.512 | 1.918 | 2.004 | 2.166 | 2.184 | 2.106 | 2.118 | 2.284 | 2.339 | 2.096 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 2.994 | 3.217 | 4.556 | 4.952 | 5.450 | 5.315 | 5.517 | 5.078 | 5.579 | 5.452 | 5.589 | ns |
| | | GCLK PLL | $t_{co}$ | 1.316 | 1.501 | 1.903 | 1.988 | 2.149 | 2.167 | 2.089 | 2.101 | 2.266 | 2.321 | 2.078 | ns |


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**Table 1–44.** EP3SL50 Row Pins output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.047 | 3.271 | 4.617 | 5.015 | 5.525 | 5.389 | 5.596 | 5.141 | 5.653 | 5.518 | 5.664 | ns |
| | | GCLK PLL | $t_{co}$ | 1.316 | 1.519 | 1.927 | 1.998 | 2.198 | 2.216 | 2.138 | 2.111 | 2.316 | 2.333 | 2.127 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.042 | 3.266 | 4.615 | 5.014 | 5.524 | 5.388 | 5.595 | 5.139 | 5.651 | 5.516 | 5.662 | ns |
| | | GCLK PLL | $t_{co}$ | 1.311 | 1.505 | 1.924 | 1.997 | 2.197 | 2.215 | 2.137 | 2.109 | 2.314 | 2.331 | 2.125 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.031 | 3.255 | 4.605 | 5.004 | 5.514 | 5.378 | 5.585 | 5.130 | 5.642 | 5.507 | 5.653 | ns |
| | | GCLK PLL | $t_{co}$ | 1.300 | 1.493 | 1.907 | 1.987 | 2.187 | 2.205 | 2.127 | 2.100 | 2.305 | 2.322 | 2.116 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.020 | 3.244 | 4.592 | 4.991 | 5.501 | 5.365 | 5.572 | 5.118 | 5.630 | 5.495 | 5.641 | ns |
| | | GCLK PLL | $t_{co}$ | 1.289 | 1.476 | 1.891 | 1.974 | 2.174 | 2.192 | 2.114 | 2.088 | 2.293 | 2.310 | 2.104 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.020 | 3.243 | 4.592 | 4.991 | 5.501 | 5.365 | 5.572 | 5.117 | 5.630 | 5.495 | 5.641 | ns |
| | | GCLK PLL | $t_{co}$ | 1.289 | 1.475 | 1.890 | 1.974 | 2.174 | 2.192 | 2.114 | 2.087 | 2.293 | 2.310 | 2.104 | ns |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.028 | 3.250 | 4.591 | 4.988 | 5.496 | 5.360 | 5.567 | 5.113 | 5.624 | 5.489 | 5.635 | ns |
| | | GCLK PLL | $t_{co}$ | 1.297 | 1.482 | 1.888 | 1.971 | 2.169 | 2.187 | 2.109 | 2.083 | 2.287 | 2.304 | 2.098 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.029 | 3.253 | 4.597 | 4.996 | 5.506 | 5.370 | 5.577 | 5.122 | 5.635 | 5.500 | 5.646 | ns |
| | | GCLK PLL | $t_{co}$ | 1.298 | 1.485 | 1.892 | 1.979 | 2.179 | 2.197 | 2.119 | 2.092 | 2.298 | 2.315 | 2.109 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.050 | 3.274 | 4.626 | 5.026 | 5.538 | 5.402 | 5.609 | 5.151 | 5.665 | 5.530 | 5.676 | ns |
| | | GCLK PLL | $t_{co}$ | 1.319 | 1.515 | 1.938 | 2.009 | 2.211 | 2.229 | 2.151 | 2.121 | 2.328 | 2.345 | 2.139 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.036 | 3.260 | 4.615 | 5.016 | 5.528 | 5.392 | 5.599 | 5.142 | 5.656 | 5.521 | 5.667 | ns |
| | | GCLK PLL | $t_{co}$ | 1.305 | 1.493 | 1.920 | 1.999 | 2.201 | 2.219 | 2.141 | 2.112 | 2.319 | 2.336 | 2.130 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.025 | 3.248 | 4.602 | 5.003 | 5.515 | 5.379 | 5.586 | 5.129 | 5.643 | 5.508 | 5.654 | ns |
| | | GCLK PLL | $t_{co}$ | 1.294 | 1.480 | 1.903 | 1.986 | 2.188 | 2.206 | 2.128 | 2.099 | 2.306 | 2.323 | 2.117 | ns |

**Table 1–44.** EP3SL50 Row Pins output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.035 | 3.256 | 4.590 | 4.986 | 5.494 | 5.358 | 5.565 | 5.112 | 5.621 | 5.486 | 5.632 | ns |
| | | GCLK PLL | $t_{co}$ | 1.304 | 1.491 | 1.894 | 1.969 | 2.167 | 2.185 | 2.107 | 2.082 | 2.284 | 2.301 | 2.095 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.028 | 3.250 | 4.588 | 4.985 | 5.493 | 5.357 | 5.564 | 5.111 | 5.621 | 5.486 | 5.632 | ns |
| | | GCLK PLL | $t_{co}$ | 1.297 | 1.482 | 1.885 | 1.968 | 2.166 | 2.184 | 2.106 | 2.081 | 2.284 | 2.301 | 2.095 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.019 | 3.242 | 4.581 | 4.978 | 5.486 | 5.350 | 5.557 | 5.104 | 5.614 | 5.479 | 5.625 | ns |
| | | GCLK PLL | $t_{co}$ | 1.288 | 1.474 | 1.877 | 1.961 | 2.159 | 2.177 | 2.099 | 2.074 | 2.277 | 2.294 | 2.088 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.022 | 3.244 | 4.584 | 4.981 | 5.490 | 5.354 | 5.561 | 5.107 | 5.617 | 5.482 | 5.628 | ns |
| | | GCLK PLL | $t_{co}$ | 1.291 | 1.476 | 1.879 | 1.964 | 2.163 | 2.181 | 2.103 | 2.077 | 2.280 | 2.297 | 2.091 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.018 | 3.241 | 4.586 | 4.984 | 5.493 | 5.357 | 5.564 | 5.110 | 5.622 | 5.487 | 5.633 | ns |
| | | GCLK PLL | $t_{co}$ | 1.287 | 1.473 | 1.881 | 1.967 | 2.166 | 2.184 | 2.106 | 2.080 | 2.285 | 2.302 | 2.096 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.026 | 3.249 | 4.584 | 4.981 | 5.489 | 5.353 | 5.560 | 5.106 | 5.616 | 5.481 | 5.627 | ns |
| | | GCLK PLL | $t_{co}$ | 1.295 | 1.481 | 1.879 | 1.964 | 2.162 | 2.180 | 2.102 | 2.076 | 2.279 | 2.296 | 2.090 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.041 | 3.262 | 4.599 | 4.996 | 5.505 | 5.369 | 5.576 | 5.121 | 5.632 | 5.497 | 5.643 | ns |
| | | GCLK PLL | $t_{co}$ | 1.310 | 1.498 | 1.905 | 1.979 | 2.178 | 2.196 | 2.118 | 2.091 | 2.295 | 2.312 | 2.106 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.035 | 3.257 | 4.600 | 4.998 | 5.507 | 5.371 | 5.578 | 5.123 | 5.635 | 5.500 | 5.646 | ns |
| | | GCLK PLL | $t_{co}$ | 1.304 | 1.489 | 1.901 | 1.981 | 2.180 | 2.198 | 2.120 | 2.093 | 2.298 | 2.315 | 2.109 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.031 | 3.253 | 4.595 | 4.993 | 5.502 | 5.366 | 5.573 | 5.118 | 5.629 | 5.494 | 5.640 | ns |
| | | GCLK PLL | $t_{co}$ | 1.300 | 1.485 | 1.895 | 1.976 | 2.175 | 2.193 | 2.115 | 2.088 | 2.292 | 2.309 | 2.103 | ns |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.043 | 3.264 | 4.612 | 5.012 | 5.524 | 5.388 | 5.595 | 5.137 | 5.651 | 5.516 | 5.662 | ns |
| | | GCLK PLL | $t_{co}$ | 1.312 | 1.497 | 1.916 | 1.995 | 2.197 | 2.215 | 2.137 | 2.107 | 2.314 | 2.331 | 2.125 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.034 | 3.256 | 4.603 | 5.003 | 5.515 | 5.379 | 5.586 | 5.128 | 5.642 | 5.507 | 5.653 | ns |
| | | GCLK PLL | $t_{co}$ | 1.303 | 1.488 | 1.905 | 1.986 | 2.188 | 2.206 | 2.128 | 2.098 | 2.305 | 2.322 | 2.116 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.033 | 3.256 | 4.610 | 5.011 | 5.524 | 5.388 | 5.595 | 5.137 | 5.652 | 5.517 | 5.663 | ns |
| | | GCLK PLL | $t_{co}$ | 1.302 | 1.488 | 1.909 | 1.994 | 2.197 | 2.215 | 2.137 | 2.107 | 2.315 | 2.332 | 2.126 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.114 | 3.338 | 4.626 | 5.016 | 5.494 | 5.359 | 5.561 | 5.144 | 5.625 | 5.513 | 5.635 | ns |
| | | GCLK PLL | $t_{co}$ | 1.436 | 1.622 | 1.973 | 2.052 | 2.208 | 2.226 | 2.148 | 2.167 | 2.327 | 2.382 | 2.139 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.114 | 3.338 | 4.626 | 5.016 | 5.494 | 5.359 | 5.561 | 5.144 | 5.625 | 5.513 | 5.635 | ns |
| | | GCLK PLL | $t_{co}$ | 1.436 | 1.622 | 1.973 | 2.052 | 2.208 | 2.226 | 2.148 | 2.167 | 2.327 | 2.382 | 2.139 | ns |


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Table 1–45 through Table 1–48 list the maximum I/O timing parameters for EP3SL50 devices for differential I/O standards.

Table 1–45 lists the EP3SL50 column pins input timing parameters for differential I/O standards.

**Table 1–45.** EP3SL50 Column Pins Input Timing Parameters (Part 1 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -0.697 | -0.717 | -1.072 | -1.182 | -1.294 | -1.237 | -1.524 | -1.183 | -1.296 | -1.242 | -1.562 | ns |
| | | $t_h$ | 0.814 | 0.849 | 1.257 | 1.389 | 1.522 | 1.454 | 1.740 | 1.398 | 1.532 | 1.469 | 1.777 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.159 | 1.821 | 2.053 | 2.279 | 2.166 | 2.172 | 2.063 | 2.288 | 2.173 | 2.219 | ns |
| | | $t_h$ | -0.892 | -0.893 | -1.424 | -1.606 | -1.781 | -1.696 | -1.696 | -1.608 | -1.782 | -1.694 | -1.742 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -0.697 | -0.717 | -1.072 | -1.182 | -1.294 | -1.237 | -1.524 | -1.183 | -1.296 | -1.242 | -1.562 | ns |
| | | $t_h$ | 0.814 | 0.849 | 1.257 | 1.389 | 1.522 | 1.454 | 1.740 | 1.398 | 1.532 | 1.469 | 1.777 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.159 | 1.821 | 2.053 | 2.279 | 2.166 | 2.172 | 2.063 | 2.288 | 2.173 | 2.219 | ns |
| | | $t_h$ | -0.892 | -0.893 | -1.424 | -1.606 | -1.781 | -1.696 | -1.696 | -1.608 | -1.782 | -1.694 | -1.742 | ns |
| RSDS | GCLK | $t_{su}$ | -0.705 | -0.729 | -1.082 | -1.193 | -1.310 | -1.253 | -1.540 | -1.194 | -1.311 | -1.257 | -1.577 | ns |
| | | $t_h$ | 0.822 | 0.861 | 1.267 | 1.400 | 1.538 | 1.470 | 1.756 | 1.409 | 1.547 | 1.484 | 1.792 | ns |
| | GCLK PLL | $t_{su}$ | 1.135 | 1.147 | 1.811 | 2.042 | 2.263 | 2.150 | 2.156 | 2.052 | 2.273 | 2.158 | 2.204 | ns |
| | | $t_h$ | -0.884 | -0.881 | -1.414 | -1.595 | -1.765 | -1.680 | -1.680 | -1.597 | -1.767 | -1.679 | -1.727 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.705 | -0.729 | -1.082 | -1.193 | -1.310 | -1.253 | -1.540 | -1.194 | -1.311 | -1.257 | -1.577 | ns |
| | | $t_h$ | 0.822 | 0.861 | 1.267 | 1.400 | 1.538 | 1.470 | 1.756 | 1.409 | 1.547 | 1.484 | 1.792 | ns |
| | GCLK PLL | $t_{su}$ | 1.135 | 1.147 | 1.811 | 2.042 | 2.263 | 2.150 | 2.156 | 2.052 | 2.273 | 2.158 | 2.204 | ns |
| | | $t_h$ | -0.884 | -0.881 | -1.414 | -1.595 | -1.765 | -1.680 | -1.680 | -1.597 | -1.767 | -1.679 | -1.727 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.717 | -0.740 | -1.091 | -1.204 | -1.329 | -1.272 | -1.559 | -1.205 | -1.329 | -1.275 | -1.595 | ns |
| | | $t_h$ | 0.834 | 0.872 | 1.277 | 1.411 | 1.557 | 1.489 | 1.775 | 1.420 | 1.565 | 1.502 | 1.810 | ns |
| | GCLK PLL | $t_{su}$ | 1.123 | 1.136 | 1.802 | 2.031 | 2.244 | 2.131 | 2.137 | 2.041 | 2.255 | 2.140 | 2.186 | ns |
| | | $t_h$ | -0.872 | -0.870 | -1.404 | -1.584 | -1.746 | -1.661 | -1.661 | -1.586 | -1.749 | -1.661 | -1.709 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.717 | -0.740 | -1.091 | -1.204 | -1.329 | -1.272 | -1.559 | -1.205 | -1.329 | -1.275 | -1.595 | ns |
| | | $t_h$ | 0.834 | 0.872 | 1.277 | 1.411 | 1.557 | 1.489 | 1.775 | 1.420 | 1.565 | 1.502 | 1.810 | ns |
| | GCLK PLL | $t_{su}$ | 1.123 | 1.136 | 1.802 | 2.031 | 2.244 | 2.131 | 2.137 | 2.041 | 2.255 | 2.140 | 2.186 | ns |
| | | $t_h$ | -0.872 | -0.870 | -1.404 | -1.584 | -1.746 | -1.661 | -1.661 | -1.586 | -1.749 | -1.661 | -1.709 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.705 | -0.729 | -1.082 | -1.193 | -1.310 | -1.253 | -1.540 | -1.194 | -1.311 | -1.257 | -1.577 | ns |
| | | $t_h$ | 0.822 | 0.861 | 1.267 | 1.400 | 1.538 | 1.470 | 1.756 | 1.409 | 1.547 | 1.484 | 1.792 | ns |
| | GCLK PLL | $t_{su}$ | 1.135 | 1.147 | 1.811 | 2.042 | 2.263 | 2.150 | 2.156 | 2.052 | 2.273 | 2.158 | 2.204 | ns |
| | | $t_h$ | -0.884 | -0.881 | -1.414 | -1.595 | -1.765 | -1.680 | -1.680 | -1.597 | -1.767 | -1.679 | -1.727 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.705 | -0.729 | -1.082 | -1.193 | -1.310 | -1.253 | -1.540 | -1.194 | -1.311 | -1.257 | -1.577 | ns |
| | | $t_h$ | 0.822 | 0.861 | 1.267 | 1.400 | 1.538 | 1.470 | 1.756 | 1.409 | 1.547 | 1.484 | 1.792 | ns |
| | GCLK PLL | $t_{su}$ | 1.135 | 1.147 | 1.811 | 2.042 | 2.263 | 2.150 | 2.156 | 2.052 | 2.273 | 2.158 | 2.204 | ns |
| | | $t_h$ | -0.884 | -0.881 | -1.414 | -1.595 | -1.765 | -1.680 | -1.680 | -1.597 | -1.767 | -1.679 | -1.727 | ns |

**Table 1–45.** EP3SL50 Column Pins Input Timing Parameters (Part 2 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.717 | -0.740 | -1.091 | -1.204 | -1.329 | -1.272 | -1.559 | -1.205 | -1.329 | -1.275 | -1.595 | ns |
| | | $t_h$ | 0.834 | 0.872 | 1.277 | 1.411 | 1.557 | 1.489 | 1.775 | 1.420 | 1.565 | 1.502 | 1.810 | ns |
| | GCLK PLL | $t_{su}$ | 1.123 | 1.136 | 1.802 | 2.031 | 2.244 | 2.131 | 2.137 | 2.041 | 2.255 | 2.140 | 2.186 | ns |
| | | $t_h$ | -0.872 | -0.870 | -1.404 | -1.584 | -1.746 | -1.661 | -1.661 | -1.586 | -1.749 | -1.661 | -1.709 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.717 | -0.740 | -1.091 | -1.204 | -1.329 | -1.272 | -1.559 | -1.205 | -1.329 | -1.275 | -1.595 | ns |
| | | $t_h$ | 0.834 | 0.872 | 1.277 | 1.411 | 1.557 | 1.489 | 1.775 | 1.420 | 1.565 | 1.502 | 1.810 | ns |
| | GCLK PLL | $t_{su}$ | 1.123 | 1.136 | 1.802 | 2.031 | 2.244 | 2.131 | 2.137 | 2.041 | 2.255 | 2.140 | 2.186 | ns |
| | | $t_h$ | -0.872 | -0.870 | -1.404 | -1.584 | -1.746 | -1.661 | -1.661 | -1.586 | -1.749 | -1.661 | -1.709 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.724 | -0.746 | -1.103 | -1.209 | -1.329 | -1.274 | -1.558 | -1.209 | -1.324 | -1.273 | -1.591 | ns |
| | | $t_h$ | 0.841 | 0.878 | 1.290 | 1.419 | 1.560 | 1.492 | 1.779 | 1.427 | 1.565 | 1.501 | 1.811 | ns |
| | GCLK PLL | $t_{su}$ | 1.116 | 1.130 | 1.790 | 2.026 | 2.244 | 2.129 | 2.138 | 2.037 | 2.260 | 2.142 | 2.190 | ns |
| | | $t_h$ | -0.865 | -0.864 | -1.391 | -1.576 | -1.743 | -1.658 | -1.657 | -1.579 | -1.749 | -1.662 | -1.708 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -0.724 | -0.746 | -1.103 | -1.209 | -1.329 | -1.274 | -1.558 | -1.209 | -1.324 | -1.273 | -1.591 | ns |
| | | $t_h$ | 0.841 | 0.878 | 1.290 | 1.419 | 1.560 | 1.492 | 1.779 | 1.427 | 1.565 | 1.501 | 1.811 | ns |
| | GCLK PLL | $t_{su}$ | 1.116 | 1.130 | 1.790 | 2.026 | 2.244 | 2.129 | 2.138 | 2.037 | 2.260 | 2.142 | 2.190 | ns |
| | | $t_h$ | -0.865 | -0.864 | -1.391 | -1.576 | -1.743 | -1.658 | -1.657 | -1.579 | -1.749 | -1.662 | -1.708 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -0.697 | -0.717 | -1.072 | -1.182 | -1.294 | -1.237 | -1.524 | -1.183 | -1.296 | -1.242 | -1.562 | ns |
| | | $t_h$ | 0.814 | 0.849 | 1.257 | 1.389 | 1.522 | 1.454 | 1.740 | 1.398 | 1.532 | 1.469 | 1.777 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.159 | 1.821 | 2.053 | 2.279 | 2.166 | 2.172 | 2.063 | 2.288 | 2.173 | 2.219 | ns |
| | | $t_h$ | -0.892 | -0.893 | -1.424 | -1.606 | -1.781 | -1.696 | -1.696 | -1.608 | -1.782 | -1.694 | -1.742 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.697 | -0.717 | -1.072 | -1.182 | -1.294 | -1.237 | -1.524 | -1.183 | -1.296 | -1.242 | -1.562 | ns |
| | | $t_h$ | 0.814 | 0.849 | 1.257 | 1.389 | 1.522 | 1.454 | 1.740 | 1.398 | 1.532 | 1.469 | 1.777 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.159 | 1.821 | 2.053 | 2.279 | 2.166 | 2.172 | 2.063 | 2.288 | 2.173 | 2.219 | ns |
| | | $t_h$ | -0.892 | -0.893 | -1.424 | -1.606 | -1.781 | -1.696 | -1.696 | -1.608 | -1.782 | -1.694 | -1.742 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.705 | -0.729 | -1.082 | -1.193 | -1.310 | -1.253 | -1.540 | -1.194 | -1.311 | -1.257 | -1.577 | ns |
| | | $t_h$ | 0.822 | 0.861 | 1.267 | 1.400 | 1.538 | 1.470 | 1.756 | 1.409 | 1.547 | 1.484 | 1.792 | ns |
| | GCLK PLL | $t_{su}$ | 1.135 | 1.147 | 1.811 | 2.042 | 2.263 | 2.150 | 2.156 | 2.052 | 2.273 | 2.158 | 2.204 | ns |
| | | $t_h$ | -0.884 | -0.881 | -1.414 | -1.595 | -1.765 | -1.680 | -1.680 | -1.597 | -1.767 | -1.679 | -1.727 | ns |

Table 1–46 lists the EP3SL50 row pins input timing parameters for differential I/O standards.

**Table 1–46.** EP3SL50 Row Pins Input Timing Parameters (Part 1 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -0.919 | -0.939 | -0.988 | -0.952 | -1.089 | -1.040 | -1.316 | -0.916 | -1.048 | -1.000 | -1.349 | ns |
| | | $t_h$ | 1.042 | 1.077 | 1.209 | 1.205 | 1.369 | 1.306 | 1.580 | 1.182 | 1.339 | 1.280 | 1.613 | ns |
| | GCLK PLL | $t_{su}$ | 0.882 | 0.896 | 1.863 | 2.243 | 2.446 | 2.322 | 2.342 | 2.291 | 2.500 | 2.376 | 2.393 | ns |
| | | $t_h$ | -0.625 | -0.625 | -1.430 | -1.749 | -1.896 | -1.802 | -1.817 | -1.783 | -1.936 | -1.843 | -1.865 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -0.919 | -0.939 | -0.988 | -0.952 | -1.089 | -1.040 | -1.316 | -0.916 | -1.048 | -1.000 | -1.349 | ns |
| | | $t_h$ | 1.042 | 1.077 | 1.209 | 1.205 | 1.369 | 1.306 | 1.580 | 1.182 | 1.339 | 1.280 | 1.613 | ns |
| | GCLK PLL | $t_{su}$ | 0.882 | 0.896 | 1.863 | 2.243 | 2.446 | 2.322 | 2.342 | 2.291 | 2.500 | 2.376 | 2.393 | ns |
| | | $t_h$ | -0.625 | -0.625 | -1.430 | -1.749 | -1.896 | -1.802 | -1.817 | -1.783 | -1.936 | -1.843 | -1.865 | ns |
| RSDS | GCLK | $t_{su}$ | -0.919 | -0.939 | -0.988 | -0.952 | -1.089 | -1.040 | -1.316 | -0.916 | -1.048 | -1.000 | -1.349 | ns |
| | | $t_h$ | 1.042 | 1.077 | 1.209 | 1.205 | 1.369 | 1.306 | 1.580 | 1.182 | 1.339 | 1.280 | 1.613 | ns |
| | GCLK PLL | $t_{su}$ | 0.882 | 0.896 | 1.863 | 2.243 | 2.446 | 2.322 | 2.342 | 2.291 | 2.500 | 2.376 | 2.393 | ns |
| | | $t_h$ | -0.625 | -0.625 | -1.430 | -1.749 | -1.896 | -1.802 | -1.817 | -1.783 | -1.936 | -1.843 | -1.865 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.734 | -0.764 | -1.085 | -1.186 | -1.286 | -1.234 | -1.505 | -1.193 | -1.291 | -1.242 | -1.543 | ns |
| | | $t_h$ | 0.850 | 0.893 | 1.274 | 1.394 | 1.516 | 1.451 | 1.720 | 1.410 | 1.531 | 1.470 | 1.758 | ns |
| | GCLK PLL | $t_{su}$ | 1.077 | 1.081 | 1.776 | 2.019 | 2.257 | 2.138 | 2.163 | 2.024 | 2.263 | 2.144 | 2.209 | ns |
| | | $t_h$ | -0.827 | -0.819 | -1.375 | -1.570 | -1.756 | -1.667 | -1.687 | -1.565 | -1.751 | -1.663 | -1.730 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.734 | -0.764 | -1.085 | -1.186 | -1.286 | -1.234 | -1.505 | -1.193 | -1.291 | -1.242 | -1.543 | ns |
| | | $t_h$ | 0.850 | 0.893 | 1.274 | 1.394 | 1.516 | 1.451 | 1.720 | 1.410 | 1.531 | 1.470 | 1.758 | ns |
| | GCLK PLL | $t_{su}$ | 1.077 | 1.081 | 1.776 | 2.019 | 2.257 | 2.138 | 2.163 | 2.024 | 2.263 | 2.144 | 2.209 | ns |
| | | $t_h$ | -0.827 | -0.819 | -1.375 | -1.570 | -1.756 | -1.667 | -1.687 | -1.565 | -1.751 | -1.663 | -1.730 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.743 | -0.776 | -1.094 | -1.196 | -1.302 | -1.250 | -1.521 | -1.202 | -1.307 | -1.258 | -1.559 | ns |
| | | $t_h$ | 0.859 | 0.905 | 1.283 | 1.404 | 1.532 | 1.467 | 1.736 | 1.419 | 1.547 | 1.486 | 1.774 | ns |
| | GCLK PLL | $t_{su}$ | 1.068 | 1.069 | 1.767 | 2.009 | 2.241 | 2.122 | 2.147 | 2.015 | 2.247 | 2.128 | 2.193 | ns |
| | | $t_h$ | -0.818 | -0.807 | -1.366 | -1.560 | -1.740 | -1.651 | -1.671 | -1.556 | -1.735 | -1.647 | -1.714 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.743 | -0.776 | -1.094 | -1.196 | -1.302 | -1.250 | -1.521 | -1.202 | -1.307 | -1.258 | -1.559 | ns |
| | | $t_h$ | 0.859 | 0.905 | 1.283 | 1.404 | 1.532 | 1.467 | 1.736 | 1.419 | 1.547 | 1.486 | 1.774 | ns |
| | GCLK PLL | $t_{su}$ | 1.068 | 1.069 | 1.767 | 2.009 | 2.241 | 2.122 | 2.147 | 2.015 | 2.247 | 2.128 | 2.193 | ns |
| | | $t_h$ | -0.818 | -0.807 | -1.366 | -1.560 | -1.740 | -1.651 | -1.671 | -1.556 | -1.735 | -1.647 | -1.714 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.757 | -0.788 | -1.107 | -1.206 | -1.320 | -1.268 | -1.539 | -1.213 | -1.324 | -1.275 | -1.576 | ns |
| | | $t_h$ | 0.873 | 0.917 | 1.295 | 1.414 | 1.550 | 1.485 | 1.754 | 1.430 | 1.564 | 1.503 | 1.791 | ns |
| | GCLK PLL | $t_{su}$ | 1.054 | 1.057 | 1.754 | 1.999 | 2.223 | 2.104 | 2.129 | 2.004 | 2.230 | 2.111 | 2.176 | ns |
| | | $t_h$ | -0.804 | -0.795 | -1.354 | -1.550 | -1.722 | -1.633 | -1.653 | -1.545 | -1.718 | -1.630 | -1.697 | ns |

**Table 1–46.** EP3SL50 Row Pins Input Timing Parameters (Part 2 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.757 | -0.788 | -1.107 | -1.206 | -1.320 | -1.268 | -1.539 | -1.213 | -1.324 | -1.275 | -1.576 | ns |
| | | $t_h$ | 0.873 | 0.917 | 1.295 | 1.414 | 1.550 | 1.485 | 1.754 | 1.430 | 1.564 | 1.503 | 1.791 | ns |
| | GCLK PLL | $t_{su}$ | 1.054 | 1.057 | 1.754 | 1.999 | 2.223 | 2.104 | 2.129 | 2.004 | 2.230 | 2.111 | 2.176 | ns |
| | | $t_h$ | -0.804 | -0.795 | -1.354 | -1.550 | -1.722 | -1.633 | -1.653 | -1.545 | -1.718 | -1.630 | -1.697 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.743 | -0.776 | -1.094 | -1.196 | -1.302 | -1.250 | -1.521 | -1.202 | -1.307 | -1.258 | -1.559 | ns |
| | | $t_h$ | 0.859 | 0.905 | 1.283 | 1.404 | 1.532 | 1.467 | 1.736 | 1.419 | 1.547 | 1.486 | 1.774 | ns |
| | GCLK PLL | $t_{su}$ | 1.068 | 1.069 | 1.767 | 2.009 | 2.241 | 2.122 | 2.147 | 2.015 | 2.247 | 2.128 | 2.193 | ns |
| | | $t_h$ | -0.818 | -0.807 | -1.366 | -1.560 | -1.740 | -1.651 | -1.671 | -1.556 | -1.735 | -1.647 | -1.714 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.743 | -0.776 | -1.094 | -1.196 | -1.302 | -1.250 | -1.521 | -1.202 | -1.307 | -1.258 | -1.559 | ns |
| | | $t_h$ | 0.859 | 0.905 | 1.283 | 1.404 | 1.532 | 1.467 | 1.736 | 1.419 | 1.547 | 1.486 | 1.774 | ns |
| | GCLK PLL | $t_{su}$ | 1.068 | 1.069 | 1.767 | 2.009 | 2.241 | 2.122 | 2.147 | 2.015 | 2.247 | 2.128 | 2.193 | ns |
| | | $t_h$ | -0.818 | -0.807 | -1.366 | -1.560 | -1.740 | -1.651 | -1.671 | -1.556 | -1.735 | -1.647 | -1.714 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -0.757 | -0.788 | -1.107 | -1.206 | -1.320 | -1.268 | -1.539 | -1.213 | -1.324 | -1.275 | -1.576 | ns |
| | | $t_h$ | 0.873 | 0.917 | 1.295 | 1.414 | 1.550 | 1.485 | 1.754 | 1.430 | 1.564 | 1.503 | 1.791 | ns |
| | GCLK PLL | $t_{su}$ | 1.054 | 1.057 | 1.754 | 1.999 | 2.223 | 2.104 | 2.129 | 2.004 | 2.230 | 2.111 | 2.176 | ns |
| | | $t_h$ | -0.804 | -0.795 | -1.354 | -1.550 | -1.722 | -1.633 | -1.653 | -1.545 | -1.718 | -1.630 | -1.697 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -0.757 | -0.788 | -1.107 | -1.206 | -1.320 | -1.268 | -1.539 | -1.213 | -1.324 | -1.275 | -1.576 | ns |
| | | $t_h$ | 0.873 | 0.917 | 1.295 | 1.414 | 1.550 | 1.485 | 1.754 | 1.430 | 1.564 | 1.503 | 1.791 | ns |
| | GCLK PLL | $t_{su}$ | 1.054 | 1.057 | 1.754 | 1.999 | 2.223 | 2.104 | 2.129 | 2.004 | 2.230 | 2.111 | 2.176 | ns |
| | | $t_h$ | -0.804 | -0.795 | -1.354 | -1.550 | -1.722 | -1.633 | -1.653 | -1.545 | -1.718 | -1.630 | -1.697 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.756 | -0.787 | -1.112 | -1.212 | -1.321 | -1.270 | -1.540 | -1.214 | -1.320 | -1.273 | -1.573 | ns |
| | | $t_h$ | 0.872 | 0.916 | 1.300 | 1.422 | 1.554 | 1.489 | 1.759 | 1.434 | 1.563 | 1.502 | 1.792 | ns |
| | GCLK PLL | $t_{su}$ | 1.045 | 1.048 | 1.739 | 1.983 | 2.212 | 2.092 | 2.118 | 1.993 | 2.224 | 2.103 | 2.169 | ns |
| | | $t_h$ | -0.795 | -0.786 | -1.339 | -1.532 | -1.708 | -1.619 | -1.638 | -1.531 | -1.709 | -1.621 | -1.686 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.756 | -0.787 | -1.112 | -1.212 | -1.321 | -1.270 | -1.540 | -1.214 | -1.320 | -1.273 | -1.573 | ns |
| | | $t_h$ | 0.872 | 0.916 | 1.300 | 1.422 | 1.554 | 1.489 | 1.759 | 1.434 | 1.563 | 1.502 | 1.792 | ns |
| | GCLK PLL | $t_{su}$ | 1.045 | 1.048 | 1.739 | 1.983 | 2.212 | 2.092 | 2.118 | 1.993 | 2.224 | 2.103 | 2.169 | ns |
| | | $t_h$ | -0.795 | -0.786 | -1.339 | -1.532 | -1.708 | -1.619 | -1.638 | -1.531 | -1.709 | -1.621 | -1.686 | ns |

Table 1–47 lists the EP3SL50 column pins output timing parameters for differential I/O standards.

**Table 1–47.** EP3SL50 Column Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.029 | 3.246 | 4.575 | 4.976 | 5.487 | 5.347 | 5.565 | 5.101 | 5.612 | 5.474 | 5.631 | ns |
| | | GCLK PLL | $t_{co}$ | 3.025 | 3.249 | 4.622 | 5.031 | 5.549 | 5.409 | 5.627 | 5.160 | 5.678 | 5.540 | 5.697 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.029 | 3.246 | 4.575 | 4.976 | 5.487 | 5.347 | 5.565 | 5.101 | 5.612 | 5.474 | 5.631 | ns |
| | | GCLK PLL | $t_{co}$ | 3.025 | 3.249 | 4.622 | 5.031 | 5.549 | 5.409 | 5.627 | 5.160 | 5.678 | 5.540 | 5.697 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.029 | 3.246 | 4.575 | 4.976 | 5.487 | 5.347 | 5.565 | 5.101 | 5.612 | 5.474 | 5.631 | ns |
| | | GCLK PLL | $t_{co}$ | 3.025 | 3.249 | 4.622 | 5.031 | 5.549 | 5.409 | 5.627 | 5.160 | 5.678 | 5.540 | 5.697 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.056 | 3.279 | 4.646 | 5.054 | 5.571 | 5.431 | 5.649 | 5.181 | 5.698 | 5.560 | 5.717 | ns |
| | | GCLK PLL | $t_{co}$ | 3.046 | 3.269 | 4.636 | 5.043 | 5.561 | 5.421 | 5.639 | 5.170 | 5.688 | 5.550 | 5.707 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.046 | 3.269 | 4.639 | 5.047 | 5.565 | 5.425 | 5.643 | 5.175 | 5.693 | 5.555 | 5.712 | ns |
| | | GCLK PLL | $t_{co}$ | 3.039 | 3.263 | 4.632 | 5.041 | 5.559 | 5.419 | 5.637 | 5.168 | 5.687 | 5.549 | 5.706 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.038 | 3.261 | 4.629 | 5.038 | 5.556 | 5.416 | 5.634 | 5.165 | 5.683 | 5.545 | 5.702 | ns |
| | | GCLK PLL | $t_{co}$ | 3.060 | 3.283 | 4.650 | 5.058 | 5.575 | 5.435 | 5.653 | 5.185 | 5.703 | 5.565 | 5.722 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.050 | 3.272 | 4.629 | 5.035 | 5.550 | 5.410 | 5.628 | 5.161 | 5.676 | 5.538 | 5.695 | ns |
| | | GCLK PLL | $t_{co}$ | 3.045 | 3.268 | 4.629 | 5.035 | 5.551 | 5.411 | 5.629 | 5.162 | 5.678 | 5.540 | 5.697 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.043 | 3.266 | 4.628 | 5.034 | 5.549 | 5.409 | 5.627 | 5.161 | 5.677 | 5.539 | 5.696 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.257 | 4.618 | 5.024 | 5.540 | 5.400 | 5.618 | 5.151 | 5.667 | 5.529 | 5.686 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.036 | 3.259 | 4.624 | 5.031 | 5.548 | 5.408 | 5.626 | 5.159 | 5.676 | 5.538 | 5.695 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.256 | 4.607 | 5.012 | 5.526 | 5.386 | 5.604 | 5.138 | 5.652 | 5.514 | 5.671 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.047 | 3.269 | 4.625 | 5.030 | 5.544 | 5.404 | 5.622 | 5.157 | 5.671 | 5.533 | 5.690 | ns |
| | | GCLK PLL | $t_{co}$ | 3.043 | 3.266 | 4.626 | 5.032 | 5.548 | 5.408 | 5.626 | 5.159 | 5.675 | 5.537 | 5.694 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.033 | 3.255 | 4.615 | 5.021 | 5.536 | 5.396 | 5.614 | 5.148 | 5.663 | 5.525 | 5.682 | ns |
| | | GCLK PLL | $t_{co}$ | 3.031 | 3.253 | 4.613 | 5.018 | 5.534 | 5.394 | 5.612 | 5.146 | 5.661 | 5.523 | 5.680 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.031 | 3.254 | 4.616 | 5.023 | 5.539 | 5.399 | 5.617 | 5.150 | 5.667 | 5.529 | 5.686 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.257 | 4.613 | 5.018 | 5.533 | 5.393 | 5.611 | 5.145 | 5.660 | 5.522 | 5.679 | ns |

**Table 1–47.** EP3SL50 Column Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.061 | 3.286 | 4.658 | 5.066 | 5.583 | 5.443 | 5.661 | 5.193 | 5.710 | 5.572 | 5.729 | ns |
| | | GCLK PLL | $t_{co}$ | 3.047 | 3.272 | 4.646 | 5.055 | 5.573 | 5.433 | 5.651 | 5.183 | 5.701 | 5.563 | 5.720 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.035 | 3.259 | 4.629 | 5.037 | 5.555 | 5.415 | 5.633 | 5.165 | 5.683 | 5.545 | 5.702 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.259 | 4.632 | 5.041 | 5.559 | 5.419 | 5.637 | 5.169 | 5.688 | 5.550 | 5.707 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.031 | 3.255 | 4.625 | 5.033 | 5.552 | 5.412 | 5.630 | 5.162 | 5.680 | 5.542 | 5.699 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.257 | 4.618 | 5.024 | 5.540 | 5.400 | 5.618 | 5.151 | 5.667 | 5.529 | 5.686 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.036 | 3.259 | 4.626 | 5.034 | 5.551 | 5.411 | 5.629 | 5.161 | 5.679 | 5.541 | 5.698 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.289 | 4.657 | 5.064 | 5.581 | 5.441 | 5.659 | 5.192 | 5.708 | 5.570 | 5.727 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.053 | 3.277 | 4.645 | 5.052 | 5.569 | 5.429 | 5.647 | 5.180 | 5.696 | 5.558 | 5.715 | ns |
| | | GCLK PLL | $t_{co}$ | 3.048 | 3.273 | 4.645 | 5.053 | 5.570 | 5.430 | 5.648 | 5.181 | 5.698 | 5.560 | 5.717 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.034 | 3.258 | 4.627 | 5.034 | 5.551 | 5.411 | 5.629 | 5.162 | 5.680 | 5.542 | 5.699 | ns |
| | | GCLK PLL | $t_{co}$ | 3.032 | 3.256 | 4.625 | 5.032 | 5.549 | 5.409 | 5.627 | 5.160 | 5.677 | 5.539 | 5.696 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.036 | 3.258 | 4.617 | 5.022 | 5.537 | 5.397 | 5.615 | 5.149 | 5.664 | 5.526 | 5.683 | ns |
| | | GCLK PLL | $t_{co}$ | 3.036 | 3.259 | 4.625 | 5.032 | 5.549 | 5.409 | 5.627 | 5.160 | 5.677 | 5.539 | 5.696 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.052 | 3.276 | 4.641 | 5.047 | 5.563 | 5.423 | 5.641 | 5.175 | 5.690 | 5.552 | 5.709 | ns |
| | | GCLK PLL | $t_{co}$ | 3.052 | 3.276 | 4.641 | 5.047 | 5.563 | 5.423 | 5.641 | 5.175 | 5.690 | 5.552 | 5.709 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.042 | 3.266 | 4.631 | 5.037 | 5.553 | 5.413 | 5.631 | 5.165 | 5.681 | 5.543 | 5.700 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.258 | 4.617 | 5.022 | 5.537 | 5.397 | 5.615 | 5.149 | 5.664 | 5.526 | 5.683 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.029 | 3.246 | 4.575 | 4.976 | 5.487 | 5.347 | 5.565 | 5.101 | 5.612 | 5.474 | 5.631 | ns |
| | | GCLK PLL | $t_{co}$ | 3.025 | 3.249 | 4.622 | 5.031 | 5.549 | 5.409 | 5.627 | 5.160 | 5.678 | 5.540 | 5.697 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.029 | 3.246 | 4.575 | 4.976 | 5.487 | 5.347 | 5.565 | 5.101 | 5.612 | 5.474 | 5.631 | ns |
| | | GCLK PLL | $t_{co}$ | 3.025 | 3.249 | 4.622 | 5.031 | 5.549 | 5.409 | 5.627 | 5.160 | 5.678 | 5.540 | 5.697 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.029 | 3.246 | 4.575 | 4.976 | 5.487 | 5.347 | 5.565 | 5.101 | 5.612 | 5.474 | 5.631 | ns |
| | | GCLK PLL | $t_{co}$ | 3.025 | 3.249 | 4.622 | 5.031 | 5.549 | 5.409 | 5.627 | 5.160 | 5.678 | 5.540 | 5.697 | ns |


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**Table 1–47.** EP3SL50 Column Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.056 | 3.279 | 4.646 | 5.054 | 5.571 | 5.431 | 5.649 | 5.181 | 5.698 | 5.560 | 5.717 | ns |
| | | GCLK PLL | $t_{co}$ | 3.046 | 3.269 | 4.636 | 5.043 | 5.561 | 5.421 | 5.639 | 5.170 | 5.688 | 5.550 | 5.707 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.046 | 3.269 | 4.639 | 5.047 | 5.565 | 5.425 | 5.643 | 5.175 | 5.693 | 5.555 | 5.712 | ns |
| | | GCLK PLL | $t_{co}$ | 3.039 | 3.263 | 4.632 | 5.041 | 5.559 | 5.419 | 5.637 | 5.168 | 5.687 | 5.549 | 5.706 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.038 | 3.261 | 4.629 | 5.038 | 5.556 | 5.416 | 5.634 | 5.165 | 5.683 | 5.545 | 5.702 | ns |
| | | GCLK PLL | $t_{co}$ | 3.060 | 3.283 | 4.650 | 5.058 | 5.575 | 5.435 | 5.653 | 5.185 | 5.703 | 5.565 | 5.722 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.050 | 3.272 | 4.629 | 5.035 | 5.550 | 5.410 | 5.628 | 5.161 | 5.676 | 5.538 | 5.695 | ns |
| | | GCLK PLL | $t_{co}$ | 3.045 | 3.268 | 4.629 | 5.035 | 5.551 | 5.411 | 5.629 | 5.162 | 5.678 | 5.540 | 5.697 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.043 | 3.266 | 4.628 | 5.034 | 5.549 | 5.409 | 5.627 | 5.161 | 5.677 | 5.539 | 5.696 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.257 | 4.618 | 5.024 | 5.540 | 5.400 | 5.618 | 5.151 | 5.667 | 5.529 | 5.686 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.036 | 3.259 | 4.624 | 5.031 | 5.548 | 5.408 | 5.626 | 5.159 | 5.676 | 5.538 | 5.695 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.256 | 4.607 | 5.012 | 5.526 | 5.386 | 5.604 | 5.138 | 5.652 | 5.514 | 5.671 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.047 | 3.269 | 4.625 | 5.030 | 5.544 | 5.404 | 5.622 | 5.157 | 5.671 | 5.533 | 5.690 | ns |
| | | GCLK PLL | $t_{co}$ | 3.043 | 3.266 | 4.626 | 5.032 | 5.548 | 5.408 | 5.626 | 5.159 | 5.675 | 5.537 | 5.694 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.033 | 3.255 | 4.615 | 5.021 | 5.536 | 5.396 | 5.614 | 5.148 | 5.663 | 5.525 | 5.682 | ns |
| | | GCLK PLL | $t_{co}$ | 3.031 | 3.253 | 4.613 | 5.018 | 5.534 | 5.394 | 5.612 | 5.146 | 5.661 | 5.523 | 5.680 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.031 | 3.254 | 4.616 | 5.023 | 5.539 | 5.399 | 5.617 | 5.150 | 5.667 | 5.529 | 5.686 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.257 | 4.613 | 5.018 | 5.533 | 5.393 | 5.611 | 5.145 | 5.660 | 5.522 | 5.679 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.061 | 3.286 | 4.658 | 5.066 | 5.583 | 5.443 | 5.661 | 5.193 | 5.710 | 5.572 | 5.729 | ns |
| | | GCLK PLL | $t_{co}$ | 3.047 | 3.272 | 4.646 | 5.055 | 5.573 | 5.433 | 5.651 | 5.183 | 5.701 | 5.563 | 5.720 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.035 | 3.259 | 4.629 | 5.037 | 5.555 | 5.415 | 5.633 | 5.165 | 5.683 | 5.545 | 5.702 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.259 | 4.632 | 5.041 | 5.559 | 5.419 | 5.637 | 5.169 | 5.688 | 5.550 | 5.707 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.031 | 3.255 | 4.625 | 5.033 | 5.552 | 5.412 | 5.630 | 5.162 | 5.680 | 5.542 | 5.699 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.257 | 4.618 | 5.024 | 5.540 | 5.400 | 5.618 | 5.151 | 5.667 | 5.529 | 5.686 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.036 | 3.259 | 4.626 | 5.034 | 5.551 | 5.411 | 5.629 | 5.161 | 5.679 | 5.541 | 5.698 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.289 | 4.657 | 5.064 | 5.581 | 5.441 | 5.659 | 5.192 | 5.708 | 5.570 | 5.727 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.053 | 3.277 | 4.645 | 5.052 | 5.569 | 5.429 | 5.647 | 5.180 | 5.696 | 5.558 | 5.715 | ns |
| | | GCLK PLL | $t_{co}$ | 3.048 | 3.273 | 4.645 | 5.053 | 5.570 | 5.430 | 5.648 | 5.181 | 5.698 | 5.560 | 5.717 | ns |

**Table 1–47.** EP3SL50 Column Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.034 | 3.258 | 4.627 | 5.034 | 5.551 | 5.411 | 5.629 | 5.162 | 5.680 | 5.542 | 5.699 | ns |
| | | GCLK PLL | $t_{co}$ | 3.032 | 3.256 | 4.625 | 5.032 | 5.549 | 5.409 | 5.627 | 5.160 | 5.677 | 5.539 | 5.696 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.036 | 3.258 | 4.617 | 5.022 | 5.537 | 5.397 | 5.615 | 5.149 | 5.664 | 5.526 | 5.683 | ns |
| | | GCLK PLL | $t_{co}$ | 3.036 | 3.259 | 4.625 | 5.032 | 5.549 | 5.409 | 5.627 | 5.160 | 5.677 | 5.539 | 5.696 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.052 | 3.276 | 4.641 | 5.047 | 5.563 | 5.423 | 5.641 | 5.175 | 5.690 | 5.552 | 5.709 | ns |
| | | GCLK PLL | $t_{co}$ | 3.052 | 3.276 | 4.641 | 5.047 | 5.563 | 5.423 | 5.641 | 5.175 | 5.690 | 5.552 | 5.709 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.042 | 3.266 | 4.631 | 5.037 | 5.553 | 5.413 | 5.631 | 5.165 | 5.681 | 5.543 | 5.700 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.258 | 4.617 | 5.022 | 5.537 | 5.397 | 5.615 | 5.149 | 5.664 | 5.526 | 5.683 | ns |

Table 1–48 lists the EP3SL50 row pins output timing parameters for differential I/O standards.

**Table 1–48.** EP3SL50 Row Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | — | GCLK | $t_{co}$ | 2.668 | 2.842 | 3.979 | 4.346 | 4.821 | 4.685 | 4.892 | 4.453 | 4.930 | 4.795 | 4.940 | ns |
| | | GCLK PLL | $t_{co}$ | 3.062 | 3.288 | 4.646 | 5.055 | 5.575 | 5.431 | 5.630 | 5.186 | 5.709 | 5.565 | 5.694 | ns |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.044 | 3.278 | 4.684 | 5.101 | 5.629 | 5.485 | 5.684 | 5.237 | 5.770 | 5.626 | 5.755 | ns |
| | | GCLK PLL | $t_{co}$ | 2.668 | 2.842 | 3.979 | 4.346 | 4.821 | 4.685 | 4.892 | 4.453 | 4.930 | 4.795 | 4.940 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.062 | 3.288 | 4.646 | 5.055 | 5.575 | 5.431 | 5.630 | 5.186 | 5.709 | 5.565 | 5.694 | ns |
| | | GCLK PLL | $t_{co}$ | 3.044 | 3.278 | 4.684 | 5.101 | 5.629 | 5.485 | 5.684 | 5.237 | 5.770 | 5.626 | 5.755 | ns |
| MINI-LVDS | — | GCLK | $t_{co}$ | 2.668 | 2.842 | 3.979 | 4.346 | 4.821 | 4.685 | 4.892 | 4.453 | 4.930 | 4.795 | 4.940 | ns |
| | | GCLK PLL | $t_{co}$ | 3.062 | 3.288 | 4.646 | 5.055 | 5.575 | 5.431 | 5.630 | 5.186 | 5.709 | 5.565 | 5.694 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.044 | 3.278 | 4.684 | 5.101 | 5.629 | 5.485 | 5.684 | 5.237 | 5.770 | 5.626 | 5.755 | ns |
| | | GCLK PLL | $t_{co}$ | 3.098 | 3.331 | 4.730 | 5.145 | 5.672 | 5.528 | 5.727 | 5.280 | 5.809 | 5.665 | 5.794 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.084 | 3.317 | 4.717 | 5.132 | 5.659 | 5.515 | 5.714 | 5.266 | 5.796 | 5.652 | 5.781 | ns |
| | | GCLK PLL | $t_{co}$ | 3.080 | 3.313 | 4.715 | 5.132 | 5.660 | 5.516 | 5.715 | 5.266 | 5.798 | 5.654 | 5.783 | ns |
| RSDS | — | GCLK | $t_{co}$ | 3.096 | 3.328 | 4.716 | 5.129 | 5.654 | 5.510 | 5.709 | 5.263 | 5.791 | 5.647 | 5.776 | ns |
| | | GCLK PLL | $t_{co}$ | 3.085 | 3.318 | 4.712 | 5.125 | 5.651 | 5.507 | 5.706 | 5.260 | 5.788 | 5.644 | 5.773 | ns |

**Table 1–48.** EP3SL50 Row Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.082 | 3.315 | 4.710 | 5.123 | 5.649 | 5.505 | 5.704 | 5.258 | 5.787 | 5.643 | 5.772 | ns |
| | | GCLK PLL | $t_{co}$ | 3.093 | 3.325 | 4.711 | 5.124 | 5.648 | 5.504 | 5.703 | 5.257 | 5.785 | 5.641 | 5.770 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.083 | 3.316 | 4.709 | 5.122 | 5.647 | 5.503 | 5.702 | 5.257 | 5.785 | 5.641 | 5.770 | ns |
| | | GCLK PLL | $t_{co}$ | 3.069 | 3.302 | 4.694 | 5.107 | 5.633 | 5.489 | 5.688 | 5.242 | 5.770 | 5.626 | 5.755 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.066 | 3.298 | 4.690 | 5.103 | 5.629 | 5.485 | 5.684 | 5.238 | 5.766 | 5.622 | 5.751 | ns |
| | | GCLK PLL | $t_{co}$ | 3.063 | 3.296 | 4.691 | 5.106 | 5.632 | 5.488 | 5.687 | 5.241 | 5.770 | 5.626 | 5.755 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.064 | 3.296 | 4.681 | 5.094 | 5.619 | 5.475 | 5.674 | 5.228 | 5.756 | 5.612 | 5.741 | ns |
| | | GCLK PLL | $t_{co}$ | 3.113 | 3.349 | 4.752 | 5.167 | 5.695 | 5.551 | 5.750 | 5.302 | 5.832 | 5.688 | 5.817 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.089 | 3.325 | 4.734 | 5.150 | 5.678 | 5.534 | 5.733 | 5.285 | 5.817 | 5.673 | 5.802 | ns |
| | | GCLK PLL | $t_{co}$ | 3.071 | 3.306 | 4.712 | 5.128 | 5.656 | 5.512 | 5.711 | 5.263 | 5.795 | 5.651 | 5.780 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.117 | 3.352 | 4.752 | 5.167 | 5.694 | 5.550 | 5.749 | 5.302 | 5.832 | 5.688 | 5.817 | ns |
| | | GCLK PLL | $t_{co}$ | 3.102 | 3.337 | 4.738 | 5.152 | 5.679 | 5.535 | 5.734 | 5.287 | 5.817 | 5.673 | 5.802 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.091 | 3.326 | 4.733 | 5.149 | 5.676 | 5.532 | 5.731 | 5.284 | 5.815 | 5.671 | 5.800 | ns |
| | | GCLK PLL | $t_{co}$ | 3.071 | 3.306 | 4.710 | 5.125 | 5.653 | 5.509 | 5.708 | 5.261 | 5.791 | 5.647 | 5.776 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.068 | 3.302 | 4.706 | 5.122 | 5.649 | 5.505 | 5.704 | 5.257 | 5.788 | 5.644 | 5.773 | ns |
| | | GCLK PLL | $t_{co}$ | 3.073 | 3.306 | 4.697 | 5.110 | 5.635 | 5.491 | 5.690 | 5.244 | 5.772 | 5.628 | 5.757 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.066 | 3.299 | 4.696 | 5.111 | 5.638 | 5.494 | 5.693 | 5.247 | 5.777 | 5.633 | 5.762 | ns |
| | | GCLK PLL | $t_{co}$ | 3.094 | 3.328 | 4.724 | 5.138 | 5.664 | 5.520 | 5.719 | 5.273 | 5.802 | 5.658 | 5.787 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.076 | 3.311 | 4.709 | 5.123 | 5.649 | 5.505 | 5.704 | 5.258 | 5.787 | 5.643 | 5.772 | ns |
| | | GCLK PLL | $t_{co}$ | 3.062 | 3.295 | 4.686 | 5.099 | 5.624 | 5.480 | 5.679 | 5.234 | 5.762 | 5.618 | 5.747 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 8mA | GCLK | $t_{co}$ | 2.668 | 2.842 | 3.979 | 4.346 | 4.821 | 4.685 | 4.892 | 4.453 | 4.930 | 4.795 | 4.940 | ns |
| | | GCLK PLL | $t_{co}$ | 3.062 | 3.288 | 4.646 | 5.055 | 5.575 | 5.431 | 5.630 | 5.186 | 5.709 | 5.565 | 5.694 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 10mA | GCLK | $t_{co}$ | 3.044 | 3.278 | 4.684 | 5.101 | 5.629 | 5.485 | 5.684 | 5.237 | 5.770 | 5.626 | 5.755 | ns |
| | | GCLK PLL | $t_{co}$ | 2.668 | 2.842 | 3.979 | 4.346 | 4.821 | 4.685 | 4.892 | 4.453 | 4.930 | 4.795 | 4.940 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 12mA | GCLK | $t_{co}$ | 3.062 | 3.288 | 4.646 | 5.055 | 5.575 | 5.431 | 5.630 | 5.186 | 5.709 | 5.565 | 5.694 | ns |
| | | GCLK PLL | $t_{co}$ | 3.044 | 3.278 | 4.684 | 5.101 | 5.629 | 5.485 | 5.684 | 5.237 | 5.770 | 5.626 | 5.755 | ns |

**Table 1–48.** EP3SL50 Row Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 2.668 | 2.842 | 3.979 | 4.346 | 4.821 | 4.685 | 4.892 | 4.453 | 4.930 | 4.795 | 4.940 | ns |
| | | GCLK PLL | $t_{co}$ | 3.062 | 3.288 | 4.646 | 5.055 | 5.575 | 5.431 | 5.630 | 5.186 | 5.709 | 5.565 | 5.694 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.044 | 3.278 | 4.684 | 5.101 | 5.629 | 5.485 | 5.684 | 5.237 | 5.770 | 5.626 | 5.755 | ns |
| | | GCLK PLL | $t_{co}$ | 3.098 | 3.331 | 4.730 | 5.145 | 5.672 | 5.528 | 5.727 | 5.280 | 5.809 | 5.665 | 5.794 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.084 | 3.317 | 4.717 | 5.132 | 5.659 | 5.515 | 5.714 | 5.266 | 5.796 | 5.652 | 5.781 | ns |
| | | GCLK PLL | $t_{co}$ | 3.080 | 3.313 | 4.715 | 5.132 | 5.660 | 5.516 | 5.715 | 5.266 | 5.798 | 5.654 | 5.783 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.096 | 3.328 | 4.716 | 5.129 | 5.654 | 5.510 | 5.709 | 5.263 | 5.791 | 5.647 | 5.776 | ns |
| | | GCLK PLL | $t_{co}$ | 3.085 | 3.318 | 4.712 | 5.125 | 5.651 | 5.507 | 5.706 | 5.260 | 5.788 | 5.644 | 5.773 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.082 | 3.315 | 4.710 | 5.123 | 5.649 | 5.505 | 5.704 | 5.258 | 5.787 | 5.643 | 5.772 | ns |
| | | GCLK PLL | $t_{co}$ | 3.093 | 3.325 | 4.711 | 5.124 | 5.648 | 5.504 | 5.703 | 5.257 | 5.785 | 5.641 | 5.770 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.083 | 3.316 | 4.709 | 5.122 | 5.647 | 5.503 | 5.702 | 5.257 | 5.785 | 5.641 | 5.770 | ns |
| | | GCLK PLL | $t_{co}$ | 3.069 | 3.302 | 4.694 | 5.107 | 5.633 | 5.489 | 5.688 | 5.242 | 5.770 | 5.626 | 5.755 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.066 | 3.298 | 4.690 | 5.103 | 5.629 | 5.485 | 5.684 | 5.238 | 5.766 | 5.622 | 5.751 | ns |
| | | GCLK PLL | $t_{co}$ | 3.063 | 3.296 | 4.691 | 5.106 | 5.632 | 5.488 | 5.687 | 5.241 | 5.770 | 5.626 | 5.755 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 10mA | GCLK | $t_{co}$ | 3.064 | 3.296 | 4.681 | 5.094 | 5.619 | 5.475 | 5.674 | 5.228 | 5.756 | 5.612 | 5.741 | ns |
| | | GCLK PLL | $t_{co}$ | 3.113 | 3.349 | 4.752 | 5.167 | 5.695 | 5.551 | 5.750 | 5.302 | 5.832 | 5.688 | 5.817 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 12mA | GCLK | $t_{co}$ | 3.089 | 3.325 | 4.734 | 5.150 | 5.678 | 5.534 | 5.733 | 5.285 | 5.817 | 5.673 | 5.802 | ns |
| | | GCLK PLL | $t_{co}$ | 3.071 | 3.306 | 4.712 | 5.128 | 5.656 | 5.512 | 5.711 | 5.263 | 5.795 | 5.651 | 5.780 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.117 | 3.352 | 4.752 | 5.167 | 5.694 | 5.550 | 5.749 | 5.302 | 5.832 | 5.688 | 5.817 | ns |
| | | GCLK PLL | $t_{co}$ | 3.102 | 3.337 | 4.738 | 5.152 | 5.679 | 5.535 | 5.734 | 5.287 | 5.817 | 5.673 | 5.802 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.091 | 3.326 | 4.733 | 5.149 | 5.676 | 5.532 | 5.731 | 5.284 | 5.815 | 5.671 | 5.800 | ns |
| | | GCLK PLL | $t_{co}$ | 3.071 | 3.306 | 4.710 | 5.125 | 5.653 | 5.509 | 5.708 | 5.261 | 5.791 | 5.647 | 5.776 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.068 | 3.302 | 4.706 | 5.122 | 5.649 | 5.505 | 5.704 | 5.257 | 5.788 | 5.644 | 5.773 | ns |
| | | GCLK PLL | $t_{co}$ | 3.073 | 3.306 | 4.697 | 5.110 | 5.635 | 5.491 | 5.690 | 5.244 | 5.772 | 5.628 | 5.757 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 12mA | GCLK | $t_{co}$ | 3.066 | 3.299 | 4.696 | 5.111 | 5.638 | 5.494 | 5.693 | 5.247 | 5.777 | 5.633 | 5.762 | ns |
| | | GCLK PLL | $t_{co}$ | 3.094 | 3.328 | 4.724 | 5.138 | 5.664 | 5.520 | 5.719 | 5.273 | 5.802 | 5.658 | 5.787 | ns |


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**Table 1–48.** EP3SL50 Row Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.076 | 3.311 | 4.709 | 5.123 | 5.649 | 5.505 | 5.704 | 5.258 | 5.787 | 5.643 | 5.772 | ns |
| | | GCLK PLL | $t_{co}$ | 3.062 | 3.295 | 4.686 | 5.099 | 5.624 | 5.480 | 5.679 | 5.234 | 5.762 | 5.618 | 5.747 | ns |

Table 1–49 and Table 1–50 list the EP3SL50 regional clock (RCLK) adder values that must be added to the GCLK values. Use these adder values to determine I/O timing when the I/O pin is driven using the regional clock. This applies to all I/O standards supported by Stratix III devices.

Table 1–49 lists the EP3SL50 column pin delay adders when using the regional clock.

**Table 1–49.** EP3SL50 Column Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.239 | 0.258 | 0.341 | 0.365 | 0.39 | 0.377 | 0.439 | 0.375 | 0.399 | 0.388 | 0.441 | ns |
| RCLK PLL input adder | 0.008 | 0.009 | 0.014 | 0.017 | 0.019 | 0.017 | 0.02 | 0.018 | 0.019 | 0.017 | 0.02 | ns |
| RCLK output adder | -0.068 | -0.07 | -0.09 | -0.092 | -0.094 | -0.091 | -0.169 | -0.086 | -0.087 | -0.09 | -0.17 | ns |
| RCLK PLL output adder | 1.614 | 1.649 | 2.575 | 2.89 | 3.164 | 3.011 | 3.22 | 2.908 | 3.217 | 3.063 | 3.338 | ns |

Table 1–50 lists the EP3SL50 row pin delay adders when using the regional clock.

**Table 1–50.** EP3SL50 Row Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.111 | 0.124 | 0.178 | 0.193 | 0.208 | 0.2 | 0.263 | 0.197 | 0.213 | 0.203 | 0.266 | ns |
| RCLK PLL input adder | 0.101 | 0.107 | 0.156 | 0.174 | 0.194 | 0.184 | 0.251 | 0.177 | 0.196 | 0.188 | 0.249 | ns |
| RCLK output adder | -0.113 | -0.127 | -0.181 | -0.196 | -0.213 | -0.205 | -0.271 | -0.199 | -0.217 | -0.209 | -0.273 | ns |
| RCLK PLL output adder | -0.107 | -0.113 | -0.164 | -0.185 | -0.213 | -0.2 | -0.266 | -0.184 | -0.212 | -0.198 | -0.262 | ns |

## EP3SL70 I/O Timing Parameters

Table 1–51 through Table 1–54 list the maximum I/O timing parameters for EP3SL70 devices for single-ended I/O standards.

Table 1–51 lists the EP3SL70 column pins input timing parameters for single-ended I/O standards.

**Table 1–51.** EP3SL70 Column Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -0.812 | -0.811 | -1.154 | -1.261 | -1.312 | -1.266 | -1.645 | -1.261 | -1.312 | -1.266 | -1.645 | ns |
| | | $t_h$ | 0.934 | 0.934 | 1.327 | 1.457 | 1.533 | 1.475 | 1.850 | 1.457 | 1.533 | 1.475 | 1.850 | ns |
| | GCLK PLL | $t_{su}$ | -0.965 | -0.965 | -1.395 | -1.522 | -1.763 | -1.703 | -2.094 | -1.522 | -1.763 | -1.703 | -2.094 | ns |
| | | $t_h$ | 1.216 | 1.216 | 1.764 | 1.937 | 2.222 | 2.138 | 2.540 | 1.937 | 2.222 | 2.138 | 2.540 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -0.812 | -0.811 | -1.154 | -1.261 | -1.312 | -1.266 | -1.645 | -1.261 | -1.312 | -1.266 | -1.645 | ns |
| | | $t_h$ | 0.934 | 0.934 | 1.327 | 1.457 | 1.533 | 1.475 | 1.850 | 1.457 | 1.533 | 1.475 | 1.850 | ns |
| | GCLK PLL | $t_{su}$ | -0.965 | -0.965 | -1.395 | -1.522 | -1.763 | -1.703 | -2.094 | -1.522 | -1.763 | -1.703 | -2.094 | ns |
| | | $t_h$ | 1.216 | 1.216 | 1.764 | 1.937 | 2.222 | 2.138 | 2.540 | 1.937 | 2.222 | 2.138 | 2.540 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -0.823 | -0.822 | -1.153 | -1.263 | -1.311 | -1.265 | -1.644 | -1.263 | -1.311 | -1.265 | -1.644 | ns |
| | | $t_h$ | 0.945 | 0.945 | 1.326 | 1.459 | 1.532 | 1.474 | 1.849 | 1.459 | 1.532 | 1.474 | 1.849 | ns |
| | GCLK PLL | $t_{su}$ | -0.976 | -0.976 | -1.394 | -1.524 | -1.762 | -1.702 | -2.093 | -1.524 | -1.762 | -1.702 | -2.093 | ns |
| | | $t_h$ | 1.227 | 1.227 | 1.763 | 1.939 | 2.221 | 2.137 | 2.539 | 1.939 | 2.221 | 2.137 | 2.539 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -0.823 | -0.822 | -1.153 | -1.263 | -1.311 | -1.265 | -1.644 | -1.263 | -1.311 | -1.265 | -1.644 | ns |
| | | $t_h$ | 0.945 | 0.945 | 1.326 | 1.459 | 1.532 | 1.474 | 1.849 | 1.459 | 1.532 | 1.474 | 1.849 | ns |
| | GCLK PLL | $t_{su}$ | -0.976 | -0.976 | -1.394 | -1.524 | -1.762 | -1.702 | -2.093 | -1.524 | -1.762 | -1.702 | -2.093 | ns |
| | | $t_h$ | 1.227 | 1.227 | 1.763 | 1.939 | 2.221 | 2.137 | 2.539 | 1.939 | 2.221 | 2.137 | 2.539 | ns |
| 2.5 V | GCLK | $t_{su}$ | -0.818 | -0.817 | -1.162 | -1.275 | -1.330 | -1.284 | -1.663 | -1.275 | -1.330 | -1.284 | -1.663 | ns |
| | | $t_h$ | 0.940 | 0.940 | 1.335 | 1.471 | 1.551 | 1.493 | 1.868 | 1.471 | 1.551 | 1.493 | 1.868 | ns |
| | GCLK PLL | $t_{su}$ | -0.971 | -0.971 | -1.403 | -1.536 | -1.781 | -1.721 | -2.112 | -1.536 | -1.781 | -1.721 | -2.112 | ns |
| | | $t_h$ | 1.222 | 1.222 | 1.772 | 1.951 | 2.240 | 2.156 | 2.558 | 1.951 | 2.240 | 2.156 | 2.558 | ns |
| 1.8 V | GCLK | $t_{su}$ | -0.840 | -0.839 | -1.202 | -1.311 | -1.328 | -1.282 | -1.661 | -1.311 | -1.328 | -1.282 | -1.661 | ns |
| | | $t_h$ | 0.964 | 0.964 | 1.375 | 1.507 | 1.549 | 1.491 | 1.866 | 1.507 | 1.549 | 1.491 | 1.866 | ns |
| | GCLK PLL | $t_{su}$ | -0.993 | -0.993 | -1.443 | -1.572 | -1.779 | -1.719 | -2.110 | -1.572 | -1.779 | -1.719 | -2.110 | ns |
| | | $t_h$ | 1.246 | 1.246 | 1.812 | 1.987 | 2.238 | 2.154 | 2.556 | 1.987 | 2.238 | 2.154 | 2.556 | ns |
| 1.5 V | GCLK | $t_{su}$ | -0.830 | -0.829 | -1.179 | -1.279 | -1.258 | -1.212 | -1.591 | -1.279 | -1.258 | -1.212 | -1.591 | ns |
| | | $t_h$ | 0.954 | 0.954 | 1.352 | 1.475 | 1.479 | 1.421 | 1.796 | 1.475 | 1.479 | 1.421 | 1.796 | ns |
| | GCLK PLL | $t_{su}$ | -0.983 | -0.983 | -1.420 | -1.540 | -1.709 | -1.649 | -2.040 | -1.540 | -1.709 | -1.649 | -2.040 | ns |
| | | $t_h$ | 1.236 | 1.236 | 1.789 | 1.955 | 2.168 | 2.084 | 2.486 | 1.955 | 2.168 | 2.084 | 2.486 | ns |
| 1.2 V | GCLK | $t_{su}$ | -0.778 | -0.777 | -1.102 | -1.180 | -1.102 | -1.056 | -1.435 | -1.180 | -1.102 | -1.056 | -1.435 | ns |
| | | $t_h$ | 0.902 | 0.902 | 1.275 | 1.376 | 1.323 | 1.265 | 1.640 | 1.376 | 1.323 | 1.265 | 1.640 | ns |
| | GCLK PLL | $t_{su}$ | -0.931 | -0.931 | -1.343 | -1.441 | -1.553 | -1.493 | -1.884 | -1.441 | -1.553 | -1.493 | -1.884 | ns |
| | | $t_h$ | 1.184 | 1.184 | 1.712 | 1.856 | 2.012 | 1.928 | 2.330 | 1.856 | 2.012 | 1.928 | 2.330 | ns |

**Table 1–51.** EP3SL70 Column Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -0.749 | -0.748 | -1.074 | -1.164 | -1.104 | -1.058 | -1.437 | -1.164 | -1.104 | -1.058 | -1.437 | ns |
| | | $t_h$ | 0.873 | 0.873 | 1.247 | 1.360 | 1.325 | 1.267 | 1.642 | 1.360 | 1.325 | 1.267 | 1.642 | ns |
| | GCLK PLL | $t_{su}$ | -0.902 | -0.902 | -1.315 | -1.425 | -1.555 | -1.495 | -1.886 | -1.425 | -1.555 | -1.495 | -1.886 | ns |
| | | $t_h$ | 1.155 | 1.155 | 1.684 | 1.840 | 2.014 | 1.930 | 2.332 | 1.840 | 2.014 | 1.930 | 2.332 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -0.749 | -0.748 | -1.074 | -1.164 | -1.104 | -1.058 | -1.437 | -1.164 | -1.104 | -1.058 | -1.437 | ns |
| | | $t_h$ | 0.873 | 0.873 | 1.247 | 1.360 | 1.325 | 1.267 | 1.642 | 1.360 | 1.325 | 1.267 | 1.642 | ns |
| | GCLK PLL | $t_{su}$ | -0.902 | -0.902 | -1.315 | -1.425 | -1.555 | -1.495 | -1.886 | -1.425 | -1.555 | -1.495 | -1.886 | ns |
| | | $t_h$ | 1.155 | 1.155 | 1.684 | 1.840 | 2.014 | 1.930 | 2.332 | 1.840 | 2.014 | 1.930 | 2.332 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -0.743 | -0.742 | -1.061 | -1.156 | -1.104 | -1.056 | -1.435 | -1.156 | -1.104 | -1.056 | -1.435 | ns |
| | | $t_h$ | 0.867 | 0.867 | 1.234 | 1.349 | 1.322 | 1.264 | 1.635 | 1.349 | 1.322 | 1.264 | 1.635 | ns |
| | GCLK PLL | $t_{su}$ | -0.896 | -0.896 | -1.302 | -1.417 | -1.552 | -1.490 | -1.884 | -1.417 | -1.552 | -1.490 | -1.884 | ns |
| | | $t_h$ | 1.149 | 1.149 | 1.671 | 1.829 | 2.008 | 1.924 | 2.325 | 1.829 | 2.008 | 1.924 | 2.325 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -0.743 | -0.742 | -1.061 | -1.156 | -1.104 | -1.056 | -1.435 | -1.156 | -1.104 | -1.056 | -1.435 | ns |
| | | $t_h$ | 0.867 | 0.867 | 1.234 | 1.349 | 1.322 | 1.264 | 1.635 | 1.349 | 1.322 | 1.264 | 1.635 | ns |
| | GCLK PLL | $t_{su}$ | -0.896 | -0.896 | -1.302 | -1.417 | -1.552 | -1.490 | -1.884 | -1.417 | -1.552 | -1.490 | -1.884 | ns |
| | | $t_h$ | 1.149 | 1.149 | 1.671 | 1.829 | 2.008 | 1.924 | 2.325 | 1.829 | 2.008 | 1.924 | 2.325 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -0.732 | -0.731 | -1.050 | -1.145 | -1.085 | -1.037 | -1.416 | -1.145 | -1.085 | -1.037 | -1.416 | ns |
| | | $t_h$ | 0.856 | 0.856 | 1.222 | 1.338 | 1.303 | 1.245 | 1.616 | 1.338 | 1.303 | 1.245 | 1.616 | ns |
| | GCLK PLL | $t_{su}$ | -0.885 | -0.885 | -1.291 | -1.406 | -1.533 | -1.471 | -1.865 | -1.406 | -1.533 | -1.471 | -1.865 | ns |
| | | $t_h$ | 1.138 | 1.138 | 1.659 | 1.818 | 1.989 | 1.905 | 2.306 | 1.818 | 1.989 | 1.905 | 2.306 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.732 | -0.731 | -1.050 | -1.145 | -1.085 | -1.037 | -1.416 | -1.145 | -1.085 | -1.037 | -1.416 | ns |
| | | $t_h$ | 0.856 | 0.856 | 1.222 | 1.338 | 1.303 | 1.245 | 1.616 | 1.338 | 1.303 | 1.245 | 1.616 | ns |
| | GCLK PLL | $t_{su}$ | -0.885 | -0.885 | -1.291 | -1.406 | -1.533 | -1.471 | -1.865 | -1.406 | -1.533 | -1.471 | -1.865 | ns |
| | | $t_h$ | 1.138 | 1.138 | 1.659 | 1.818 | 1.989 | 1.905 | 2.306 | 1.818 | 1.989 | 1.905 | 2.306 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.743 | -0.742 | -1.061 | -1.156 | -1.104 | -1.056 | -1.435 | -1.156 | -1.104 | -1.056 | -1.435 | ns |
| | | $t_h$ | 0.867 | 0.867 | 1.234 | 1.349 | 1.322 | 1.264 | 1.635 | 1.349 | 1.322 | 1.264 | 1.635 | ns |
| | GCLK PLL | $t_{su}$ | -0.896 | -0.896 | -1.302 | -1.417 | -1.552 | -1.490 | -1.884 | -1.417 | -1.552 | -1.490 | -1.884 | ns |
| | | $t_h$ | 1.149 | 1.149 | 1.671 | 1.829 | 2.008 | 1.924 | 2.325 | 1.829 | 2.008 | 1.924 | 2.325 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.743 | -0.742 | -1.061 | -1.156 | -1.104 | -1.056 | -1.435 | -1.156 | -1.104 | -1.056 | -1.435 | ns |
| | | $t_h$ | 0.867 | 0.867 | 1.234 | 1.349 | 1.322 | 1.264 | 1.635 | 1.349 | 1.322 | 1.264 | 1.635 | ns |
| | GCLK PLL | $t_{su}$ | -0.896 | -0.896 | -1.302 | -1.417 | -1.552 | -1.490 | -1.884 | -1.417 | -1.552 | -1.490 | -1.884 | ns |
| | | $t_h$ | 1.149 | 1.149 | 1.671 | 1.829 | 2.008 | 1.924 | 2.325 | 1.829 | 2.008 | 1.924 | 2.325 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.732 | -0.731 | -1.050 | -1.145 | -1.085 | -1.037 | -1.416 | -1.145 | -1.085 | -1.037 | -1.416 | ns |
| | | $t_h$ | 0.856 | 0.856 | 1.222 | 1.338 | 1.303 | 1.245 | 1.616 | 1.338 | 1.303 | 1.245 | 1.616 | ns |
| | GCLK PLL | $t_{su}$ | -0.885 | -0.885 | -1.291 | -1.406 | -1.533 | -1.471 | -1.865 | -1.406 | -1.533 | -1.471 | -1.865 | ns |
| | | $t_h$ | 1.138 | 1.138 | 1.659 | 1.818 | 1.989 | 1.905 | 2.306 | 1.818 | 1.989 | 1.905 | 2.306 | ns |

**Table 1–51.** EP3SL70 Column Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.732 | -0.731 | -1.050 | -1.145 | -1.085 | -1.037 | -1.416 | -1.145 | -1.085 | -1.037 | -1.416 | ns |
| | | $t_h$ | 0.856 | 0.856 | 1.222 | 1.338 | 1.303 | 1.245 | 1.616 | 1.338 | 1.303 | 1.245 | 1.616 | ns |
| | GCLK PLL | $t_{su}$ | -0.885 | -0.885 | -1.291 | -1.406 | -1.533 | -1.471 | -1.865 | -1.406 | -1.533 | -1.471 | -1.865 | ns |
| | | $t_h$ | 1.138 | 1.138 | 1.659 | 1.818 | 1.989 | 1.905 | 2.306 | 1.818 | 1.989 | 1.905 | 2.306 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.720 | -0.719 | -1.040 | -1.134 | -1.069 | -1.021 | -1.400 | -1.134 | -1.069 | -1.021 | -1.400 | ns |
| | | $t_h$ | 0.844 | 0.844 | 1.212 | 1.327 | 1.287 | 1.229 | 1.600 | 1.327 | 1.287 | 1.229 | 1.600 | ns |
| | GCLK PLL | $t_{su}$ | -0.873 | -0.873 | -1.281 | -1.395 | -1.517 | -1.455 | -1.849 | -1.395 | -1.517 | -1.455 | -1.849 | ns |
| | | $t_h$ | 1.126 | 1.126 | 1.649 | 1.807 | 1.973 | 1.889 | 2.290 | 1.807 | 1.973 | 1.889 | 2.290 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -0.720 | -0.719 | -1.040 | -1.134 | -1.069 | -1.021 | -1.400 | -1.134 | -1.069 | -1.021 | -1.400 | ns |
| | | $t_h$ | 0.844 | 0.844 | 1.212 | 1.327 | 1.287 | 1.229 | 1.600 | 1.327 | 1.287 | 1.229 | 1.600 | ns |
| | GCLK PLL | $t_{su}$ | -0.873 | -0.873 | -1.281 | -1.395 | -1.517 | -1.455 | -1.849 | -1.395 | -1.517 | -1.455 | -1.849 | ns |
| | | $t_h$ | 1.126 | 1.126 | 1.649 | 1.807 | 1.973 | 1.889 | 2.290 | 1.807 | 1.973 | 1.889 | 2.290 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | -0.823 | -0.822 | -1.153 | -1.263 | -1.311 | -1.265 | -1.644 | -1.263 | -1.311 | -1.265 | -1.644 | ns |
| | | $t_h$ | 0.945 | 0.945 | 1.326 | 1.459 | 1.532 | 1.474 | 1.849 | 1.459 | 1.532 | 1.474 | 1.849 | ns |
| | GCLK PLL | $t_{su}$ | -0.976 | -0.976 | -1.394 | -1.524 | -1.762 | -1.702 | -2.093 | -1.524 | -1.762 | -1.702 | -2.093 | ns |
| | | $t_h$ | 1.227 | 1.227 | 1.763 | 1.939 | 2.221 | 2.137 | 2.539 | 1.939 | 2.221 | 2.137 | 2.539 | ns |

Table 1–52 lists the EP3SL70 row pins input timing parameters for single-ended I/O standards.

**Table 1–52.** EP3SL70 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -0.811 | -0.836 | -1.185 | -1.296 | -1.513 | -1.460 | -1.732 | -1.306 | -1.513 | -1.464 | -1.763 | ns |
| | | $t_h$ | 0.925 | 0.962 | 1.582 | 1.801 | 1.915 | 1.799 | 1.814 | 1.796 | 1.923 | 1.804 | 1.865 | ns |
| | GCLK PLL | $t_{su}$ | 0.937 | 0.945 | 1.371 | 1.505 | 1.747 | 1.679 | 1.951 | 1.526 | 1.756 | 1.693 | 1.982 | ns |
| | | $t_h$ | -0.688 | -0.684 | -1.185 | -1.296 | -1.513 | -1.460 | -1.732 | -1.306 | -1.513 | -1.464 | -1.763 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -0.811 | -0.836 | -1.185 | -1.296 | -1.513 | -1.460 | -1.732 | -1.306 | -1.513 | -1.464 | -1.763 | ns |
| | | $t_h$ | 0.925 | 0.962 | 1.582 | 1.801 | 1.915 | 1.799 | 1.814 | 1.796 | 1.923 | 1.804 | 1.865 | ns |
| | GCLK PLL | $t_{su}$ | 0.937 | 0.945 | 1.371 | 1.505 | 1.747 | 1.679 | 1.951 | 1.526 | 1.756 | 1.693 | 1.982 | ns |
| | | $t_h$ | -0.688 | -0.684 | -1.182 | -1.297 | -1.516 | -1.463 | -1.735 | -1.305 | -1.518 | -1.469 | -1.768 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -0.817 | -0.847 | 1.368 | 1.506 | 1.750 | 1.682 | 1.954 | 1.525 | 1.761 | 1.698 | 1.987 | ns |
| | | $t_h$ | 0.931 | 0.973 | -1.182 | -1.297 | -1.516 | -1.463 | -1.735 | -1.305 | -1.518 | -1.469 | -1.768 | ns |
| | GCLK PLL | $t_{su}$ | 0.931 | 0.934 | 1.585 | 1.800 | 1.912 | 1.796 | 1.811 | 1.797 | 1.918 | 1.799 | 1.860 | ns |
| | | $t_h$ | -0.682 | -0.673 | 1.368 | 1.506 | 1.750 | 1.682 | 1.954 | 1.525 | 1.761 | 1.698 | 1.987 | ns |

**Table 1–52.** EP3SL70 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -0.817 | -0.847 | 1.377 | 1.519 | 1.765 | 1.697 | 1.969 | 1.534 | 1.771 | 1.708 | 1.997 | ns |
| | | $t_h$ | 0.931 | 0.973 | -1.191 | -1.310 | -1.531 | -1.478 | -1.750 | -1.314 | -1.528 | -1.479 | -1.778 | ns |
| | GCLK PLL | $t_{su}$ | 0.931 | 0.934 | 1.576 | 1.787 | 1.897 | 1.781 | 1.796 | 1.788 | 1.908 | 1.789 | 1.850 | ns |
| | | $t_h$ | -0.682 | -0.673 | 1.377 | 1.519 | 1.765 | 1.697 | 1.969 | 1.534 | 1.771 | 1.708 | 1.997 | ns |
| 2.5 V | GCLK | $t_{su}$ | -0.805 | -0.840 | 1.518 | 1.758 | 1.994 | 1.874 | 1.798 | 1.758 | 1.917 | 1.798 | 1.849 | ns |
| | | $t_h$ | 0.919 | 0.966 | 1.447 | 1.676 | 1.892 | 1.823 | 2.114 | 1.723 | 1.933 | 1.867 | 2.146 | ns |
| | GCLK PLL | $t_{su}$ | 0.943 | 0.941 | -1.259 | -1.469 | -1.662 | -1.607 | -1.898 | -1.507 | -1.694 | -1.641 | -1.931 | ns |
| | | $t_h$ | -0.694 | -0.680 | 1.518 | 1.758 | 1.994 | 1.874 | 1.798 | 1.758 | 1.917 | 1.798 | 1.849 | ns |
| 1.8 V | GCLK | $t_{su}$ | -0.946 | -0.899 | 1.542 | 1.790 | 2.062 | 1.942 | 1.866 | 1.789 | 1.982 | 1.863 | 1.914 | ns |
| | | $t_h$ | 0.914 | 0.891 | 1.423 | 1.644 | 1.824 | 1.755 | 2.046 | 1.692 | 1.868 | 1.802 | 2.081 | ns |
| | GCLK PLL | $t_{su}$ | 1.060 | 1.028 | -1.235 | -1.437 | -1.594 | -1.539 | -1.830 | -1.476 | -1.629 | -1.576 | -1.866 | ns |
| | | $t_h$ | -0.936 | -0.888 | 1.621 | 1.891 | 2.221 | 2.101 | 2.025 | 1.885 | 2.137 | 2.018 | 2.069 | ns |
| 1.5 V | GCLK | $t_{su}$ | 0.924 | 0.902 | 1.344 | 1.543 | 1.665 | 1.596 | 1.887 | 1.596 | 1.713 | 1.647 | 1.926 | ns |
| | | $t_h$ | 1.050 | 1.017 | -1.156 | -1.336 | -1.435 | -1.380 | -1.671 | -1.380 | -1.474 | -1.421 | -1.711 | ns |
| | GCLK PLL | $t_{su}$ | -0.876 | -0.835 | 1.662 | 1.896 | 2.117 | 2.001 | 2.016 | 1.900 | 2.125 | 2.006 | 2.067 | ns |
| | | $t_h$ | 0.984 | 0.955 | 1.291 | 1.410 | 1.545 | 1.477 | 1.749 | 1.422 | 1.554 | 1.491 | 1.780 | ns |
| 1.2 V | GCLK | $t_{su}$ | 0.990 | 0.964 | -1.118 | -1.309 | -1.430 | -1.374 | -1.667 | -1.348 | -1.467 | -1.413 | -1.704 | ns |
| | | $t_h$ | -0.747 | -0.781 | 1.659 | -1.309 | -1.430 | -1.374 | -1.667 | -1.348 | -1.467 | -1.413 | -1.704 | ns |
| | GCLK PLL | $t_{su}$ | 1.000 | 0.999 | 1.306 | 1.514 | 1.658 | 1.589 | 1.879 | 1.562 | 1.703 | 1.638 | 1.915 | ns |
| | | $t_h$ | 0.862 | 0.908 | -1.118 | 1.918 | 2.223 | 2.104 | 2.029 | 1.917 | 2.144 | 2.026 | 2.076 | ns |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -0.747 | -0.781 | 1.659 | 1.918 | 2.223 | 2.104 | 2.029 | 1.917 | 2.144 | 2.026 | 2.076 | ns |
| | | $t_h$ | 1.000 | 0.999 | 1.306 | -1.472 | -1.722 | -1.633 | -1.557 | -1.461 | -1.635 | -1.548 | -1.601 | ns |
| | GCLK PLL | $t_{su}$ | 0.862 | 0.908 | -1.118 | -1.309 | -1.430 | -1.374 | -1.667 | -1.348 | -1.467 | -1.413 | -1.704 | ns |
| | | $t_h$ | -0.850 | -0.800 | 1.659 | 1.514 | 1.658 | 1.589 | 1.879 | 1.562 | 1.703 | 1.638 | 1.915 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | 1.010 | 0.990 | 1.306 | 1.918 | 2.223 | 2.104 | 2.029 | 1.917 | 2.144 | 2.026 | 2.076 | ns |
| | | $t_h$ | 0.964 | 0.929 | -1.118 | -1.472 | -1.722 | -1.633 | -1.557 | -1.461 | -1.635 | -1.548 | -1.601 | ns |
| | GCLK PLL | $t_{su}$ | -0.850 | -0.800 | -1.276 | -1.299 | -1.412 | -1.356 | -1.649 | -1.337 | -1.450 | -1.396 | -1.687 | ns |
| | | $t_h$ | 1.010 | 0.990 | -1.105 | 1.504 | 1.640 | 1.571 | 1.861 | 1.551 | 1.686 | 1.621 | 1.898 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | 0.964 | 0.929 | 1.294 | 1.928 | 2.241 | 2.122 | 2.047 | 1.928 | 2.161 | 2.043 | 2.093 | ns |
| | | $t_h$ | -0.836 | -0.788 | 1.659 | 1.928 | 2.241 | 2.122 | 2.047 | 1.928 | 2.161 | 2.043 | 2.093 | ns |
| | GCLK PLL | $t_{su}$ | 1.024 | 1.002 | 1.306 | -1.482 | -1.740 | -1.651 | -1.575 | -1.472 | -1.652 | -1.565 | -1.618 | ns |
| | | $t_h$ | 0.950 | 0.917 | -1.118 | -1.299 | -1.412 | -1.356 | -1.649 | -1.337 | -1.450 | -1.396 | -1.687 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -0.850 | -0.800 | 1.659 | -1.472 | -1.722 | -1.633 | -1.557 | -1.461 | -1.635 | -1.548 | -1.601 | ns |
| | | $t_h$ | 1.010 | 0.990 | 1.306 | -1.309 | -1.430 | -1.374 | -1.667 | -1.348 | -1.467 | -1.413 | -1.704 | ns |
| | GCLK PLL | $t_{su}$ | 0.964 | 0.929 | -1.118 | 1.514 | 1.658 | 1.589 | 1.879 | 1.562 | 1.703 | 1.638 | 1.915 | ns |
| | | $t_h$ | -0.850 | -0.800 | -1.276 | 1.918 | 2.223 | 2.104 | 2.029 | 1.917 | 2.144 | 2.026 | 2.076 | ns |

**Table 1–52.** EP3SL70 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | 1.010 | 0.990 | -1.105 | -1.472 | -1.722 | -1.633 | -1.557 | -1.461 | -1.635 | -1.548 | -1.601 | ns |
| | | $t_h$ | 0.964 | 0.929 | 1.294 | -1.309 | -1.430 | -1.374 | -1.667 | -1.348 | -1.467 | -1.413 | -1.704 | ns |
| | GCLK PLL | $t_{su}$ | -0.836 | -0.788 | 1.674 | 1.514 | 1.658 | 1.589 | 1.879 | 1.562 | 1.703 | 1.638 | 1.915 | ns |
| | | $t_h$ | 1.024 | 1.002 | -1.276 | 1.918 | 2.223 | 2.104 | 2.029 | 1.917 | 2.144 | 2.026 | 2.076 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | 0.950 | 0.917 | -1.105 | -1.472 | -1.722 | -1.633 | -1.557 | -1.461 | -1.635 | -1.548 | -1.601 | ns |
| | | $t_h$ | -0.836 | -0.788 | -1.285 | 1.928 | 2.241 | 2.122 | 2.047 | 1.928 | 2.161 | 2.043 | 2.093 | ns |
| | GCLK PLL | $t_{su}$ | 1.024 | 1.002 | -1.096 | -1.482 | -1.740 | -1.651 | -1.575 | -1.472 | -1.652 | -1.565 | -1.618 | ns |
| | | $t_h$ | 0.950 | 0.917 | 1.285 | -1.299 | -1.412 | -1.356 | -1.649 | -1.337 | -1.450 | -1.396 | -1.687 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.827 | -0.776 | 1.683 | 1.504 | 1.640 | 1.571 | 1.861 | 1.551 | 1.686 | 1.621 | 1.898 | ns |
| | | $t_h$ | 1.033 | 1.014 | -1.285 | 1.928 | 2.241 | 2.122 | 2.047 | 1.928 | 2.161 | 2.043 | 2.093 | ns |
| | GCLK PLL | $t_{su}$ | 0.941 | 0.905 | -1.096 | -1.482 | -1.740 | -1.651 | -1.575 | -1.472 | -1.652 | -1.565 | -1.618 | ns |
| | | $t_h$ | -0.827 | -0.776 | -1.285 | 1.938 | 2.257 | 2.138 | 2.063 | 1.937 | 2.177 | 2.059 | 2.109 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | 1.033 | 1.014 | -1.182 | -1.492 | -1.756 | -1.667 | -1.591 | -1.481 | -1.668 | -1.581 | -1.634 | ns |
| | | $t_h$ | 0.941 | 0.905 | 1.585 | -1.289 | -1.396 | -1.340 | -1.633 | -1.328 | -1.434 | -1.380 | -1.671 | ns |
| | GCLK PLL | $t_{su}$ | -0.817 | -0.847 | 1.368 | 1.494 | 1.624 | 1.555 | 1.845 | 1.542 | 1.670 | 1.605 | 1.882 | ns |
| | | $t_h$ | 0.931 | 0.973 | -1.182 | 1.938 | 2.257 | 2.138 | 2.063 | 1.937 | 2.177 | 2.059 | 2.109 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | 0.931 | 0.934 | 1.585 | -1.492 | -1.756 | -1.667 | -1.591 | -1.481 | -1.668 | -1.581 | -1.634 | ns |
| | | $t_h$ | -0.682 | -0.673 | 1.368 | -1.289 | -1.396 | -1.340 | -1.633 | -1.328 | -1.434 | -1.380 | -1.671 | ns |
| | GCLK PLL | $t_{su}$ | -0.817 | -0.847 | 1.368 | 1.494 | 1.624 | 1.555 | 1.845 | 1.542 | 1.670 | 1.605 | 1.882 | ns |
| | | $t_h$ | 0.931 | 0.973 | 1.368 | 1.938 | 2.257 | 2.138 | 2.063 | 1.937 | 2.177 | 2.059 | 2.109 | ns |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | 0.931 | 0.934 | 1.368 | -1.492 | -1.756 | -1.667 | -1.591 | -1.481 | -1.668 | -1.581 | -1.634 | ns |
| | | $t_h$ | -0.682 | -0.673 | 1.368 | -1.289 | -1.396 | -1.340 | -1.633 | -1.328 | -1.434 | -1.380 | -1.671 | ns |
| | GCLK PLL | $t_{su}$ | -0.811 | -0.836 | -1.185 | -1.296 | -1.513 | -1.460 | -1.732 | -1.306 | -1.513 | -1.464 | -1.763 | ns |
| | | $t_h$ | 0.925 | 0.962 | 1.582 | 1.801 | 1.915 | 1.799 | 1.814 | 1.796 | 1.923 | 1.804 | 1.865 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | 0.937 | 0.945 | 1.371 | 1.505 | 1.747 | 1.679 | 1.951 | 1.526 | 1.756 | 1.693 | 1.982 | ns |
| | | $t_h$ | -0.688 | -0.684 | -1.185 | -1.296 | -1.513 | -1.460 | -1.732 | -1.306 | -1.513 | -1.464 | -1.763 | ns |
| | GCLK PLL | $t_{su}$ | -0.811 | -0.836 | -1.185 | -1.296 | -1.513 | -1.460 | -1.732 | -1.306 | -1.513 | -1.464 | -1.763 | ns |
| | | $t_h$ | 0.925 | 0.962 | 1.582 | 1.801 | 1.915 | 1.799 | 1.814 | 1.796 | 1.923 | 1.804 | 1.865 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | 0.937 | 0.945 | 1.371 | 1.505 | 1.747 | 1.679 | 1.951 | 1.526 | 1.756 | 1.693 | 1.982 | ns |
| | | $t_h$ | -0.688 | -0.684 | -1.182 | -1.297 | -1.516 | -1.463 | -1.735 | -1.305 | -1.518 | -1.469 | -1.768 | ns |
| | GCLK PLL | $t_{su}$ | -0.817 | -0.847 | 1.368 | 1.506 | 1.750 | 1.682 | 1.954 | 1.525 | 1.761 | 1.698 | 1.987 | ns |
| | | $t_h$ | 0.931 | 0.973 | -1.182 | -1.297 | -1.516 | -1.463 | -1.735 | -1.305 | -1.518 | -1.469 | -1.768 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | 0.931 | 0.934 | 1.585 | 1.800 | 1.912 | 1.796 | 1.811 | 1.797 | 1.918 | 1.799 | 1.860 | ns |
| | | $t_h$ | -0.682 | -0.673 | 1.368 | 1.506 | 1.750 | 1.682 | 1.954 | 1.525 | 1.761 | 1.698 | 1.987 | ns |
| | GCLK PLL | $t_{su}$ | -0.817 | -0.847 | 1.377 | 1.519 | 1.765 | 1.697 | 1.969 | 1.534 | 1.771 | 1.708 | 1.997 | ns |
| | | $t_h$ | 0.931 | 0.973 | -1.191 | -1.310 | -1.531 | -1.478 | -1.750 | -1.314 | -1.528 | -1.479 | -1.778 | ns |

Table 1–53 lists the EP3SL70 column pins output timing parameters for single-ended I/O standards.

**Table 1–53.** EP3SL70 Column Pins Output Timing Parameters (Part 1 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.187 | 3.187 | 4.411 | 4.765 | 5.226 | 5.105 | 5.313 | 4.765 | 5.226 | 5.105 | 5.313 | ns |
| | | GCLK PLL | $t_{co}$ | 3.514 | 3.514 | 4.895 | 5.293 | 5.823 | 5.680 | 5.963 | 5.293 | 5.823 | 5.680 | 5.963 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.120 | 3.120 | 4.302 | 4.654 | 5.113 | 4.992 | 5.200 | 4.654 | 5.113 | 4.992 | 5.200 | ns |
| | | GCLK PLL | $t_{co}$ | 3.447 | 3.447 | 4.786 | 5.182 | 5.710 | 5.567 | 5.850 | 5.182 | 5.710 | 5.567 | 5.850 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.034 | 3.034 | 4.198 | 4.556 | 5.021 | 4.900 | 5.108 | 4.556 | 5.021 | 4.900 | 5.108 | ns |
| | | GCLK PLL | $t_{co}$ | 3.361 | 3.361 | 4.682 | 5.083 | 5.618 | 5.475 | 5.760 | 5.083 | 5.618 | 5.475 | 5.760 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.028 | 3.028 | 4.182 | 4.528 | 4.980 | 4.859 | 5.067 | 4.528 | 4.980 | 4.859 | 5.067 | ns |
| | | GCLK PLL | $t_{co}$ | 3.354 | 3.354 | 4.665 | 5.055 | 5.577 | 5.434 | 5.718 | 5.055 | 5.577 | 5.434 | 5.718 | ns |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.193 | 3.193 | 4.415 | 4.770 | 5.233 | 5.112 | 5.320 | 4.770 | 5.233 | 5.112 | 5.320 | ns |
| | | GCLK PLL | $t_{co}$ | 3.520 | 3.520 | 4.899 | 5.298 | 5.830 | 5.687 | 5.971 | 5.298 | 5.830 | 5.687 | 5.971 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.038 | 3.038 | 4.209 | 4.573 | 5.032 | 4.911 | 5.119 | 4.573 | 5.032 | 4.911 | 5.119 | ns |
| | | GCLK PLL | $t_{co}$ | 3.365 | 3.365 | 4.692 | 5.100 | 5.629 | 5.486 | 5.770 | 5.100 | 5.629 | 5.486 | 5.770 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.045 | 3.045 | 4.203 | 4.552 | 5.006 | 4.885 | 5.093 | 4.552 | 5.006 | 4.885 | 5.093 | ns |
| | | GCLK PLL | $t_{co}$ | 3.372 | 3.372 | 4.686 | 5.079 | 5.603 | 5.460 | 5.746 | 5.079 | 5.603 | 5.460 | 5.746 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.029 | 3.029 | 4.180 | 4.527 | 4.977 | 4.856 | 5.064 | 4.527 | 4.977 | 4.856 | 5.064 | ns |
| | | GCLK PLL | $t_{co}$ | 3.356 | 3.356 | 4.664 | 5.054 | 5.574 | 5.431 | 5.717 | 5.054 | 5.574 | 5.431 | 5.717 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.150 | 3.150 | 4.378 | 4.733 | 5.193 | 5.072 | 5.280 | 4.733 | 5.193 | 5.072 | 5.280 | ns |
| | | GCLK PLL | $t_{co}$ | 3.478 | 3.478 | 4.862 | 5.261 | 5.790 | 5.647 | 5.954 | 5.261 | 5.790 | 5.647 | 5.954 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.043 | 3.043 | 4.250 | 4.602 | 5.056 | 4.936 | 5.142 | 4.602 | 5.056 | 4.936 | 5.142 | ns |
| | | GCLK PLL | $t_{co}$ | 3.367 | 3.367 | 4.732 | 5.127 | 5.652 | 5.510 | 5.837 | 5.127 | 5.652 | 5.510 | 5.837 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.005 | 3.005 | 4.184 | 4.530 | 4.982 | 4.862 | 5.068 | 4.530 | 4.982 | 4.862 | 5.068 | ns |
| | | GCLK PLL | $t_{co}$ | 3.331 | 3.331 | 4.669 | 5.058 | 5.578 | 5.436 | 5.773 | 5.058 | 5.578 | 5.436 | 5.773 | ns |
| | 16mA | GCLK | $t_{co}$ | 2.986 | 2.986 | 4.156 | 4.503 | 4.953 | 4.832 | 5.040 | 4.503 | 4.953 | 4.832 | 5.040 | ns |
| | | GCLK PLL | $t_{co}$ | 3.313 | 3.313 | 4.640 | 5.030 | 5.550 | 5.407 | 5.750 | 5.030 | 5.550 | 5.407 | 5.750 | ns |

**Table 1–53.** EP3SL70 Column Pins Output Timing Parameters (Part 2 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.067 | 3.067 | 4.284 | 4.635 | 5.091 | 4.971 | 5.177 | 4.635 | 5.091 | 4.971 | 5.177 | ns |
| | | GCLK PLL | $t_{co}$ | 3.392 | 3.392 | 4.766 | 5.161 | 5.687 | 5.545 | 5.873 | 5.161 | 5.687 | 5.545 | 5.873 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.988 | 2.988 | 4.160 | 4.505 | 4.956 | 4.836 | 5.042 | 4.505 | 4.956 | 4.836 | 5.042 | ns |
| | | GCLK PLL | $t_{co}$ | 3.313 | 3.313 | 4.642 | 5.032 | 5.552 | 5.410 | 5.763 | 5.032 | 5.552 | 5.410 | 5.763 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.981 | 2.981 | 4.152 | 4.498 | 4.947 | 4.826 | 5.034 | 4.498 | 4.947 | 4.826 | 5.034 | ns |
| | | GCLK PLL | $t_{co}$ | 3.308 | 3.308 | 4.635 | 5.025 | 5.544 | 5.401 | 5.732 | 5.025 | 5.544 | 5.401 | 5.732 | ns |
| | 16mA | GCLK | $t_{co}$ | 2.972 | 2.972 | 4.137 | 4.482 | 4.932 | 4.811 | 5.019 | 4.482 | 4.932 | 4.811 | 5.019 | ns |
| | | GCLK PLL | $t_{co}$ | 3.299 | 3.299 | 4.621 | 5.010 | 5.529 | 5.386 | 5.737 | 5.010 | 5.529 | 5.386 | 5.737 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.187 | 3.187 | 4.490 | 4.860 | 5.338 | 5.218 | 5.424 | 4.860 | 5.338 | 5.218 | 5.424 | ns |
| | | GCLK PLL | $t_{co}$ | 3.514 | 3.514 | 4.973 | 5.388 | 5.934 | 5.792 | 6.081 | 5.388 | 5.934 | 5.792 | 6.081 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.090 | 3.090 | 4.371 | 4.735 | 5.206 | 5.086 | 5.292 | 4.735 | 5.206 | 5.086 | 5.292 | ns |
| | | GCLK PLL | $t_{co}$ | 3.414 | 3.414 | 4.854 | 5.262 | 5.802 | 5.660 | 5.957 | 5.262 | 5.802 | 5.660 | 5.957 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.045 | 3.045 | 4.284 | 4.644 | 5.110 | 4.989 | 5.197 | 4.644 | 5.110 | 4.989 | 5.197 | ns |
| | | GCLK PLL | $t_{co}$ | 3.370 | 3.370 | 4.767 | 5.171 | 5.707 | 5.564 | 5.879 | 5.171 | 5.707 | 5.564 | 5.879 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.006 | 3.006 | 4.245 | 4.602 | 5.067 | 4.946 | 5.154 | 4.602 | 5.067 | 4.946 | 5.154 | ns |
| | | GCLK PLL | $t_{co}$ | 3.332 | 3.332 | 4.728 | 5.129 | 5.664 | 5.521 | 5.822 | 5.129 | 5.664 | 5.521 | 5.822 | ns |


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**Table 1–53.** EP3SL70 Column Pins Output Timing Parameters (Part 3 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.378 | 3.378 | 4.810 | 5.219 | 5.742 | 5.621 | 5.829 | 5.219 | 5.742 | 5.621 | 5.829 | ns |
| | | GCLK PLL | $t_{co}$ | 3.705 | 3.705 | 5.294 | 5.748 | 6.339 | 6.196 | 6.478 | 5.748 | 6.339 | 6.196 | 6.478 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.200 | 3.200 | 4.533 | 4.912 | 5.395 | 5.275 | 5.481 | 4.912 | 5.395 | 5.275 | 5.481 | ns |
| | | GCLK PLL | $t_{co}$ | 3.524 | 3.524 | 5.015 | 5.439 | 5.991 | 5.849 | 6.147 | 5.439 | 5.991 | 5.849 | 6.147 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.115 | 3.115 | 4.424 | 4.796 | 5.284 | 5.163 | 5.371 | 4.796 | 5.284 | 5.163 | 5.371 | ns |
| | | GCLK PLL | $t_{co}$ | 3.442 | 3.442 | 4.908 | 5.324 | 5.881 | 5.738 | 6.035 | 5.324 | 5.881 | 5.738 | 6.035 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.095 | 3.095 | 4.366 | 4.742 | 5.218 | 5.097 | 5.305 | 4.742 | 5.218 | 5.097 | 5.305 | ns |
| | | GCLK PLL | $t_{co}$ | 3.422 | 3.422 | 4.850 | 5.270 | 5.815 | 5.672 | 5.958 | 5.270 | 5.815 | 5.672 | 5.958 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.032 | 3.032 | 4.306 | 4.668 | 5.137 | 5.016 | 5.224 | 4.668 | 5.137 | 5.016 | 5.224 | ns |
| | | GCLK PLL | $t_{co}$ | 3.359 | 3.359 | 4.789 | 5.195 | 5.734 | 5.591 | 5.889 | 5.195 | 5.734 | 5.591 | 5.889 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.015 | 3.015 | 4.285 | 4.647 | 5.114 | 4.993 | 5.201 | 4.647 | 5.114 | 4.993 | 5.201 | ns |
| | | GCLK PLL | $t_{co}$ | 3.341 | 3.341 | 4.768 | 5.174 | 5.711 | 5.568 | 5.856 | 5.174 | 5.711 | 5.568 | 5.856 | ns |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.324 | 3.324 | 4.739 | 5.152 | 5.680 | 5.559 | 5.767 | 5.152 | 5.680 | 5.559 | 5.767 | ns |
| | | GCLK PLL | $t_{co}$ | 3.651 | 3.651 | 5.223 | 5.680 | 6.277 | 6.134 | 6.423 | 5.680 | 6.277 | 6.134 | 6.423 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.112 | 3.112 | 4.420 | 4.795 | 5.288 | 5.167 | 5.375 | 4.795 | 5.288 | 5.167 | 5.375 | ns |
| | | GCLK PLL | $t_{co}$ | 3.439 | 3.439 | 4.904 | 5.324 | 5.885 | 5.742 | 6.037 | 5.324 | 5.885 | 5.742 | 6.037 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.088 | 3.088 | 4.353 | 4.737 | 5.221 | 5.100 | 5.308 | 4.737 | 5.221 | 5.100 | 5.308 | ns |
| | | GCLK PLL | $t_{co}$ | 3.414 | 3.414 | 4.837 | 5.264 | 5.818 | 5.675 | 5.960 | 5.264 | 5.818 | 5.675 | 5.960 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.076 | 3.076 | 4.337 | 4.712 | 5.201 | 5.080 | 5.288 | 4.712 | 5.201 | 5.080 | 5.288 | ns |
| | | GCLK PLL | $t_{co}$ | 3.403 | 3.403 | 4.820 | 5.239 | 5.798 | 5.655 | 5.943 | 5.239 | 5.798 | 5.655 | 5.943 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.021 | 3.021 | 4.298 | 4.661 | 5.131 | 5.010 | 5.218 | 4.661 | 5.131 | 5.010 | 5.218 | ns |
| | | GCLK PLL | $t_{co}$ | 3.348 | 3.348 | 4.782 | 5.188 | 5.728 | 5.585 | 5.880 | 5.188 | 5.728 | 5.585 | 5.880 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.015 | 3.015 | 4.281 | 4.648 | 5.120 | 4.999 | 5.207 | 4.648 | 5.120 | 4.999 | 5.207 | ns |
| | | GCLK PLL | $t_{co}$ | 3.343 | 3.343 | 4.765 | 5.177 | 5.717 | 5.574 | 5.859 | 5.177 | 5.717 | 5.574 | 5.859 | ns |

**Table 1–53.** EP3SL70 Column Pins Output Timing Parameters (Part 4 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.240 | 3.240 | 4.665 | 5.087 | 5.624 | 5.503 | 5.711 | 5.087 | 5.624 | 5.503 | 5.711 | ns |
| | | GCLK PLL | $t_{co}$ | 3.567 | 3.567 | 5.149 | 5.616 | 6.221 | 6.078 | 6.363 | 5.616 | 6.221 | 6.078 | 6.363 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.118 | 3.118 | 4.440 | 4.827 | 5.338 | 5.217 | 5.425 | 4.827 | 5.338 | 5.217 | 5.425 | ns |
| | | GCLK PLL | $t_{co}$ | 3.444 | 3.444 | 4.923 | 5.354 | 5.935 | 5.792 | 6.078 | 5.354 | 5.935 | 5.792 | 6.078 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.080 | 3.080 | 4.347 | 4.737 | 5.225 | 5.104 | 5.312 | 4.737 | 5.225 | 5.104 | 5.312 | ns |
| | | GCLK PLL | $t_{co}$ | 3.406 | 3.406 | 4.831 | 5.265 | 5.822 | 5.679 | 5.964 | 5.265 | 5.822 | 5.679 | 5.964 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.031 | 3.031 | 4.318 | 4.687 | 5.169 | 5.048 | 5.256 | 4.687 | 5.169 | 5.048 | 5.256 | ns |
| | | GCLK PLL | $t_{co}$ | 3.359 | 3.359 | 4.803 | 5.216 | 5.766 | 5.623 | 5.917 | 5.216 | 5.766 | 5.623 | 5.917 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.032 | 3.032 | 4.275 | 4.634 | 5.100 | 4.979 | 5.187 | 4.634 | 5.100 | 4.979 | 5.187 | ns |
| | | GCLK PLL | $t_{co}$ | 3.359 | 3.359 | 4.760 | 5.163 | 5.697 | 5.554 | 5.874 | 5.163 | 5.697 | 5.554 | 5.874 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.029 | 3.029 | 4.272 | 4.630 | 5.096 | 4.975 | 5.183 | 4.630 | 5.096 | 4.975 | 5.183 | ns |
| | | GCLK PLL | $t_{co}$ | 3.356 | 3.356 | 4.757 | 5.160 | 5.693 | 5.550 | 5.869 | 5.160 | 5.693 | 5.550 | 5.869 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.028 | 3.028 | 4.272 | 4.631 | 5.097 | 4.976 | 5.184 | 4.631 | 5.097 | 4.976 | 5.184 | ns |
| | | GCLK PLL | $t_{co}$ | 3.354 | 3.354 | 4.757 | 5.161 | 5.694 | 5.551 | 5.870 | 5.161 | 5.694 | 5.551 | 5.870 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.019 | 3.019 | 4.259 | 4.617 | 5.082 | 4.961 | 5.169 | 4.617 | 5.082 | 4.961 | 5.169 | ns |
| | | GCLK PLL | $t_{co}$ | 3.345 | 3.345 | 4.742 | 5.145 | 5.679 | 5.536 | 5.854 | 5.145 | 5.679 | 5.536 | 5.854 | ns |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.039 | 3.039 | 4.287 | 4.648 | 5.116 | 4.995 | 5.203 | 4.648 | 5.116 | 4.995 | 5.203 | ns |
| | | GCLK PLL | $t_{co}$ | 3.366 | 3.366 | 4.772 | 5.177 | 5.713 | 5.570 | 5.893 | 5.177 | 5.713 | 5.570 | 5.893 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.035 | 3.035 | 4.285 | 4.646 | 5.114 | 4.993 | 5.201 | 4.646 | 5.114 | 4.993 | 5.201 | ns |
| | | GCLK PLL | $t_{co}$ | 3.362 | 3.362 | 4.770 | 5.175 | 5.711 | 5.568 | 5.891 | 5.175 | 5.711 | 5.568 | 5.891 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.025 | 3.025 | 4.276 | 4.637 | 5.105 | 4.984 | 5.192 | 4.637 | 5.105 | 4.984 | 5.192 | ns |
| | | GCLK PLL | $t_{co}$ | 3.351 | 3.351 | 4.760 | 5.166 | 5.702 | 5.559 | 5.889 | 5.166 | 5.702 | 5.559 | 5.889 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.013 | 3.013 | 4.263 | 4.624 | 5.092 | 4.971 | 5.179 | 4.624 | 5.092 | 4.971 | 5.179 | ns |
| | | GCLK PLL | $t_{co}$ | 3.340 | 3.340 | 4.747 | 5.153 | 5.689 | 5.546 | 5.864 | 5.153 | 5.689 | 5.546 | 5.864 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.013 | 3.013 | 4.263 | 4.624 | 5.092 | 4.971 | 5.179 | 4.624 | 5.092 | 4.971 | 5.179 | ns |
| | | GCLK PLL | $t_{co}$ | 3.340 | 3.340 | 4.747 | 5.153 | 5.689 | 5.546 | 5.863 | 5.153 | 5.689 | 5.546 | 5.863 | ns |


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**Table 1–53.** EP3SL70 Column Pins Output Timing Parameters (Part 5 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.020 | 3.020 | 4.262 | 4.621 | 5.087 | 4.966 | 5.174 | 4.621 | 5.087 | 4.966 | 5.174 | ns |
| | | GCLK PLL | $t_{co}$ | 3.346 | 3.346 | 4.746 | 5.150 | 5.684 | 5.541 | 5.866 | 5.150 | 5.684 | 5.541 | 5.866 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.022 | 3.022 | 4.269 | 4.630 | 5.099 | 4.978 | 5.186 | 4.630 | 5.099 | 4.978 | 5.186 | ns |
| | | GCLK PLL | $t_{co}$ | 3.349 | 3.349 | 4.754 | 5.159 | 5.696 | 5.553 | 5.889 | 5.159 | 5.696 | 5.553 | 5.889 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.042 | 3.042 | 4.297 | 4.659 | 5.129 | 5.008 | 5.216 | 4.659 | 5.129 | 5.008 | 5.216 | ns |
| | | GCLK PLL | $t_{co}$ | 3.370 | 3.370 | 4.781 | 5.189 | 5.726 | 5.583 | 5.908 | 5.189 | 5.726 | 5.583 | 5.908 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.030 | 3.030 | 4.287 | 4.650 | 5.120 | 4.999 | 5.207 | 4.650 | 5.120 | 4.999 | 5.207 | ns |
| | | GCLK PLL | $t_{co}$ | 3.356 | 3.356 | 4.771 | 5.179 | 5.717 | 5.574 | 5.894 | 5.179 | 5.717 | 5.574 | 5.894 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.018 | 3.018 | 4.273 | 4.636 | 5.106 | 4.985 | 5.193 | 4.636 | 5.106 | 4.985 | 5.193 | ns |
| | | GCLK PLL | $t_{co}$ | 3.345 | 3.345 | 4.757 | 5.165 | 5.703 | 5.560 | 5.879 | 5.165 | 5.703 | 5.560 | 5.879 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.017 | 3.017 | 4.275 | 4.639 | 5.110 | 4.989 | 5.197 | 4.639 | 5.110 | 4.989 | 5.197 | ns |
| | | GCLK PLL | $t_{co}$ | 3.344 | 3.344 | 4.760 | 5.168 | 5.707 | 5.564 | 5.876 | 5.168 | 5.707 | 5.564 | 5.876 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.014 | 3.014 | 4.270 | 4.633 | 5.104 | 4.983 | 5.191 | 4.633 | 5.104 | 4.983 | 5.191 | ns |
| | | GCLK PLL | $t_{co}$ | 3.341 | 3.341 | 4.755 | 5.163 | 5.701 | 5.558 | 5.870 | 5.163 | 5.701 | 5.558 | 5.870 | ns |
| SSTL-15 CLASS II | 8mA | GCLK | $t_{co}$ | 3.016 | 3.016 | 4.260 | 4.620 | 5.087 | 4.966 | 5.174 | 4.620 | 5.087 | 4.966 | 5.174 | ns |
| | | GCLK PLL | $t_{co}$ | 3.343 | 3.343 | 4.744 | 5.149 | 5.684 | 5.541 | 5.867 | 5.149 | 5.684 | 5.541 | 5.867 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.019 | 3.019 | 4.267 | 4.628 | 5.098 | 4.977 | 5.185 | 4.628 | 5.098 | 4.977 | 5.185 | ns |
| | | GCLK PLL | $t_{co}$ | 3.346 | 3.346 | 4.751 | 5.158 | 5.695 | 5.552 | 5.891 | 5.158 | 5.695 | 5.552 | 5.891 | ns |

**Table 1–53.** EP3SL70 Column Pins Output Timing Parameters (Part 6 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.026 | 3.026 | 4.261 | 4.619 | 5.085 | 4.964 | 5.172 | 4.619 | 5.085 | 4.964 | 5.172 | ns |
| | | GCLK PLL | $t_{co}$ | 3.353 | 3.353 | 4.746 | 5.149 | 5.682 | 5.539 | 5.868 | 5.149 | 5.682 | 5.539 | 5.868 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.020 | 3.020 | 4.260 | 4.619 | 5.084 | 4.963 | 5.171 | 4.619 | 5.084 | 4.963 | 5.171 | ns |
| | | GCLK PLL | $t_{co}$ | 3.346 | 3.346 | 4.744 | 5.147 | 5.681 | 5.538 | 5.873 | 5.147 | 5.681 | 5.538 | 5.873 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.012 | 3.012 | 4.252 | 4.611 | 5.077 | 4.956 | 5.164 | 4.611 | 5.077 | 4.956 | 5.164 | ns |
| | | GCLK PLL | $t_{co}$ | 3.338 | 3.338 | 4.736 | 5.140 | 5.674 | 5.531 | 5.855 | 5.140 | 5.674 | 5.531 | 5.855 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.014 | 3.014 | 4.255 | 4.614 | 5.081 | 4.960 | 5.168 | 4.614 | 5.081 | 4.960 | 5.168 | ns |
| | | GCLK PLL | $t_{co}$ | 3.341 | 3.341 | 4.739 | 5.143 | 5.678 | 5.535 | 5.858 | 5.143 | 5.678 | 5.535 | 5.858 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.011 | 3.011 | 4.257 | 4.617 | 5.085 | 4.964 | 5.172 | 4.617 | 5.085 | 4.964 | 5.172 | ns |
| | | GCLK PLL | $t_{co}$ | 3.338 | 3.338 | 4.742 | 5.147 | 5.682 | 5.539 | 5.865 | 5.147 | 5.682 | 5.539 | 5.865 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.019 | 3.019 | 4.256 | 4.615 | 5.081 | 4.960 | 5.168 | 4.615 | 5.081 | 4.960 | 5.168 | ns |
| | | GCLK PLL | $t_{co}$ | 3.346 | 3.346 | 4.741 | 5.144 | 5.678 | 5.535 | 5.869 | 5.144 | 5.678 | 5.535 | 5.869 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.031 | 3.031 | 4.269 | 4.629 | 5.096 | 4.975 | 5.183 | 4.629 | 5.096 | 4.975 | 5.183 | ns |
| | | GCLK PLL | $t_{co}$ | 3.358 | 3.358 | 4.754 | 5.159 | 5.693 | 5.550 | 5.881 | 5.159 | 5.693 | 5.550 | 5.881 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.027 | 3.027 | 4.272 | 4.632 | 5.099 | 4.978 | 5.186 | 4.632 | 5.099 | 4.978 | 5.186 | ns |
| | | GCLK PLL | $t_{co}$ | 3.354 | 3.354 | 4.755 | 5.160 | 5.696 | 5.553 | 5.878 | 5.160 | 5.696 | 5.553 | 5.878 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.023 | 3.023 | 4.267 | 4.627 | 5.094 | 4.973 | 5.181 | 4.627 | 5.094 | 4.973 | 5.181 | ns |
| | | GCLK PLL | $t_{co}$ | 3.350 | 3.350 | 4.751 | 5.156 | 5.691 | 5.548 | 5.873 | 5.156 | 5.691 | 5.548 | 5.873 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.016 | 3.016 | 4.260 | 4.620 | 5.087 | 4.966 | 5.174 | 4.620 | 5.087 | 4.966 | 5.174 | ns |
| | | GCLK PLL | $t_{co}$ | 3.343 | 3.343 | 4.744 | 5.149 | 5.684 | 5.541 | 5.867 | 5.149 | 5.684 | 5.541 | 5.867 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.016 | 3.016 | 4.266 | 4.627 | 5.097 | 4.976 | 5.184 | 4.627 | 5.097 | 4.976 | 5.184 | ns |
| | | GCLK PLL | $t_{co}$ | 3.344 | 3.344 | 4.751 | 5.157 | 5.694 | 5.551 | 5.870 | 5.157 | 5.694 | 5.551 | 5.870 | ns |
| 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.014 | 3.014 | 4.247 | 4.605 | 5.071 | 4.950 | 5.158 | 4.605 | 5.071 | 4.950 | 5.158 | ns |
| | | GCLK PLL | $t_{co}$ | 3.342 | 3.342 | 4.732 | 5.135 | 5.668 | 5.525 | 5.855 | 5.135 | 5.668 | 5.525 | 5.855 | ns |


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**Table 1–53.** EP3SL70 Column Pins Output Timing Parameters (Part 7 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.035 | 3.035 | 4.284 | 4.647 | 5.117 | 4.996 | 5.204 | 4.647 | 5.117 | 4.996 | 5.204 | ns |
| | | GCLK PLL | $t_{co}$ | 3.361 | 3.361 | 4.768 | 5.176 | 5.714 | 5.571 | 5.900 | 5.176 | 5.714 | 5.571 | 5.900 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.026 | 3.026 | 4.275 | 4.638 | 5.108 | 4.987 | 5.195 | 4.638 | 5.108 | 4.987 | 5.195 | ns |
| | | GCLK PLL | $t_{co}$ | 3.353 | 3.353 | 4.759 | 5.167 | 5.705 | 5.562 | 5.888 | 5.167 | 5.705 | 5.562 | 5.888 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.026 | 3.026 | 4.282 | 4.646 | 5.117 | 4.996 | 5.204 | 4.646 | 5.117 | 4.996 | 5.204 | ns |
| | | GCLK PLL | $t_{co}$ | 3.354 | 3.354 | 4.767 | 5.175 | 5.714 | 5.571 | 5.891 | 5.175 | 5.714 | 5.571 | 5.891 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.016 | 3.016 | 4.269 | 4.632 | 5.103 | 4.982 | 5.190 | 4.632 | 5.103 | 4.982 | 5.190 | ns |
| | | GCLK PLL | $t_{co}$ | 3.343 | 3.343 | 4.754 | 5.162 | 5.700 | 5.557 | 5.885 | 5.162 | 5.700 | 5.557 | 5.885 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.016 | 3.016 | 4.270 | 4.633 | 5.104 | 4.983 | 5.191 | 4.633 | 5.104 | 4.983 | 5.191 | ns |
| | | GCLK PLL | $t_{co}$ | 3.343 | 3.343 | 4.754 | 5.162 | 5.701 | 5.558 | 5.877 | 5.162 | 5.701 | 5.558 | 5.877 | ns |
| 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.037 | 3.037 | 4.286 | 4.648 | 5.117 | 4.996 | 5.204 | 4.648 | 5.117 | 4.996 | 5.204 | ns |
| | | GCLK PLL | $t_{co}$ | 3.364 | 3.364 | 4.770 | 5.177 | 5.714 | 5.571 | 5.914 | 5.177 | 5.714 | 5.571 | 5.914 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.140 | 3.140 | 4.331 | 4.684 | 5.142 | 5.021 | 5.229 | 4.684 | 5.142 | 5.021 | 5.229 | ns |
| | | GCLK PLL | $t_{co}$ | 3.467 | 3.467 | 4.815 | 5.211 | 5.739 | 5.596 | 5.945 | 5.211 | 5.739 | 5.596 | 5.945 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.140 | 3.140 | 4.331 | 4.684 | 5.142 | 5.021 | 5.229 | 4.684 | 5.142 | 5.021 | 5.229 | ns |
| | | GCLK PLL | $t_{co}$ | 3.467 | 3.467 | 4.815 | 5.211 | 5.739 | 5.596 | 5.945 | 5.211 | 5.739 | 5.596 | 5.945 | ns |

Table 1–54 lists the EP3SL70 row pins output timing parameters for single-ended I/O standards.

**Table 1–54.** EP3SL70 Row Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.182 | 3.424 | 4.767 | 5.163 | 5.668 | 5.532 | 5.739 | 5.293 | 5.802 | 5.667 | 5.813 | ns |
| | | GCLK PLL | $t_{co}$ | 1.474 | 1.669 | 2.054 | 2.135 | 2.377 | 2.393 | 2.266 | 2.251 | 2.501 | 2.515 | 2.258 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.089 | 3.319 | 4.637 | 5.025 | 5.524 | 5.388 | 5.595 | 5.152 | 5.653 | 5.518 | 5.664 | ns |
| | | GCLK PLL | $t_{co}$ | 1.408 | 1.598 | 1.944 | 2.023 | 2.233 | 2.249 | 2.152 | 2.138 | 2.352 | 2.366 | 2.142 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.990 | 3.213 | 4.518 | 4.902 | 5.396 | 5.260 | 5.467 | 5.025 | 5.521 | 5.386 | 5.532 | ns |
| | | GCLK PLL | $t_{co}$ | 1.329 | 1.509 | 1.838 | 1.923 | 2.119 | 2.138 | 2.056 | 2.039 | 2.235 | 2.252 | 2.043 | ns |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.192 | 3.428 | 4.775 | 5.168 | 5.673 | 5.537 | 5.744 | 5.299 | 5.807 | 5.672 | 5.818 | ns |
| | | GCLK PLL | $t_{co}$ | 1.476 | 1.676 | 2.058 | 2.140 | 2.382 | 2.398 | 2.275 | 2.259 | 2.506 | 2.520 | 2.270 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.994 | 3.219 | 4.524 | 4.908 | 5.402 | 5.266 | 5.473 | 5.031 | 5.528 | 5.393 | 5.539 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.513 | 1.849 | 1.938 | 2.129 | 2.148 | 2.066 | 2.051 | 2.244 | 2.261 | 2.052 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.136 | 3.370 | 4.719 | 5.116 | 5.625 | 5.489 | 5.696 | 5.250 | 5.760 | 5.625 | 5.771 | ns |
| | | GCLK PLL | $t_{co}$ | 1.435 | 1.630 | 2.021 | 2.103 | 2.334 | 2.350 | 2.232 | 2.219 | 2.459 | 2.473 | 2.224 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.011 | 3.243 | 4.566 | 4.957 | 5.461 | 5.325 | 5.532 | 5.088 | 5.596 | 5.460 | 5.606 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.518 | 1.884 | 1.961 | 2.170 | 2.186 | 2.087 | 2.077 | 2.295 | 2.308 | 2.078 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.972 | 3.192 | 4.484 | 4.874 | 5.373 | 5.237 | 5.444 | 5.002 | 5.503 | 5.367 | 5.513 | ns |
| | | GCLK PLL | $t_{co}$ | 1.297 | 1.480 | 1.824 | 1.896 | 2.082 | 2.099 | 2.017 | 2.009 | 2.202 | 2.215 | 2.005 | ns |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.050 | 3.289 | 4.613 | 5.009 | 5.514 | 5.378 | 5.585 | 5.142 | 5.649 | 5.513 | 5.659 | ns |
| | | GCLK PLL | $t_{co}$ | 1.356 | 1.542 | 1.919 | 1.996 | 2.223 | 2.239 | 2.123 | 2.111 | 2.348 | 2.361 | 2.114 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.950 | 3.170 | 4.449 | 4.835 | 5.334 | 5.198 | 5.405 | 4.962 | 5.463 | 5.327 | 5.473 | ns |
| | | GCLK PLL | $t_{co}$ | 1.284 | 1.464 | 1.796 | 1.867 | 2.052 | 2.071 | 1.989 | 1.979 | 2.169 | 2.185 | 1.976 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.162 | 3.406 | 4.851 | 5.270 | 5.797 | 5.661 | 5.868 | 5.410 | 5.939 | 5.803 | 5.949 | ns |
| | | GCLK PLL | $t_{co}$ | 1.461 | 1.667 | 2.129 | 2.229 | 2.506 | 2.522 | 2.377 | 2.351 | 2.638 | 2.651 | 2.376 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.052 | 3.307 | 4.696 | 5.107 | 5.627 | 5.491 | 5.698 | 5.243 | 5.765 | 5.629 | 5.775 | ns |
| | | GCLK PLL | $t_{co}$ | 1.376 | 1.564 | 2.005 | 2.094 | 2.336 | 2.352 | 2.235 | 2.214 | 2.464 | 2.477 | 2.231 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.006 | 3.231 | 4.585 | 4.988 | 5.501 | 5.365 | 5.572 | 5.120 | 5.635 | 5.499 | 5.645 | ns |
| | | GCLK PLL | $t_{co}$ | 1.319 | 1.520 | 1.921 | 2.008 | 2.210 | 2.226 | 2.144 | 2.125 | 2.334 | 2.347 | 2.137 | ns |

**Table 1–54.** EP3SL70 Row Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.350 | 3.691 | 5.275 | 5.573 | 6.134 | 5.998 | 6.210 | 5.723 | 6.286 | 6.151 | 6.297 | ns |
| | | GCLK PLL | $t_{co}$ | 1.728 | 1.915 | 2.562 | 2.717 | 2.981 | 2.999 | 2.946 | 2.881 | 3.150 | 3.167 | 2.958 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.177 | 3.489 | 4.948 | 5.247 | 5.774 | 5.638 | 5.850 | 5.397 | 5.925 | 5.789 | 5.935 | ns |
| | | GCLK PLL | $t_{co}$ | 1.503 | 1.713 | 2.235 | 2.349 | 2.576 | 2.594 | 2.541 | 2.516 | 2.744 | 2.760 | 2.551 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.102 | 3.387 | 4.795 | 5.142 | 5.673 | 5.537 | 5.749 | 5.283 | 5.819 | 5.684 | 5.830 | ns |
| | | GCLK PLL | $t_{co}$ | 1.438 | 1.611 | 2.082 | 2.199 | 2.417 | 2.435 | 2.382 | 2.348 | 2.571 | 2.588 | 2.379 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.084 | 3.313 | 4.718 | 5.089 | 5.608 | 5.472 | 5.684 | 5.227 | 5.747 | 5.612 | 5.758 | ns |
| | | GCLK PLL | $t_{co}$ | 1.378 | 1.557 | 2.005 | 2.106 | 2.321 | 2.339 | 2.286 | 2.253 | 2.477 | 2.494 | 2.285 | ns |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.292 | 3.609 | 5.185 | 5.500 | 6.071 | 5.935 | 6.147 | 5.644 | 6.221 | 6.086 | 6.232 | ns |
| | | GCLK PLL | $t_{co}$ | 1.639 | 1.833 | 2.472 | 2.631 | 2.909 | 2.927 | 2.874 | 2.788 | 3.074 | 3.091 | 2.882 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.100 | 3.352 | 4.780 | 5.142 | 5.677 | 5.541 | 5.753 | 5.280 | 5.820 | 5.685 | 5.831 | ns |
| | | GCLK PLL | $t_{co}$ | 1.397 | 1.576 | 2.067 | 2.194 | 2.418 | 2.436 | 2.383 | 2.342 | 2.570 | 2.587 | 2.378 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.073 | 3.304 | 4.707 | 5.081 | 5.608 | 5.472 | 5.684 | 5.220 | 5.747 | 5.612 | 5.758 | ns |
| | | GCLK PLL | $t_{co}$ | 1.370 | 1.548 | 1.994 | 2.098 | 2.312 | 2.330 | 2.277 | 2.244 | 2.465 | 2.482 | 2.273 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.054 | 3.295 | 4.685 | 5.057 | 5.589 | 5.453 | 5.665 | 5.196 | 5.728 | 5.593 | 5.739 | ns |
| | | GCLK PLL | $t_{co}$ | 1.361 | 1.537 | 1.972 | 2.080 | 2.293 | 2.311 | 2.258 | 2.226 | 2.443 | 2.460 | 2.251 | ns |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.222 | 3.534 | 5.095 | 5.432 | 6.010 | 5.874 | 6.086 | 5.576 | 6.152 | 6.017 | 6.163 | ns |
| | | GCLK PLL | $t_{co}$ | 1.582 | 1.758 | 2.382 | 2.545 | 2.834 | 2.852 | 2.799 | 2.700 | 2.990 | 3.007 | 2.798 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.105 | 3.345 | 4.802 | 5.170 | 5.725 | 5.589 | 5.801 | 5.309 | 5.864 | 5.729 | 5.875 | ns |
| | | GCLK PLL | $t_{co}$ | 1.402 | 1.578 | 2.089 | 2.222 | 2.459 | 2.477 | 2.424 | 2.367 | 2.612 | 2.629 | 2.420 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 2.991 | 3.217 | 4.563 | 4.960 | 5.469 | 5.333 | 5.540 | 5.087 | 5.597 | 5.462 | 5.608 | ns |
| | | GCLK PLL | $t_{co}$ | 1.323 | 1.508 | 1.914 | 1.999 | 2.197 | 2.216 | 2.134 | 2.112 | 2.315 | 2.332 | 2.123 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.979 | 3.205 | 4.555 | 4.952 | 5.461 | 5.325 | 5.532 | 5.079 | 5.590 | 5.455 | 5.601 | ns |
| | | GCLK PLL | $t_{co}$ | 1.318 | 1.504 | 1.911 | 1.997 | 2.195 | 2.214 | 2.132 | 2.111 | 2.314 | 2.331 | 2.122 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 2.963 | 3.187 | 4.530 | 4.927 | 5.434 | 5.298 | 5.505 | 5.053 | 5.563 | 5.428 | 5.574 | ns |
| | | GCLK PLL | $t_{co}$ | 1.309 | 1.493 | 1.896 | 1.981 | 2.178 | 2.197 | 2.115 | 2.094 | 2.296 | 2.313 | 2.104 | ns |

**Table 1–54.** EP3SL70 Row Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.033 | 3.269 | 4.613 | 4.993 | 5.503 | 5.367 | 5.579 | 5.126 | 5.638 | 5.503 | 5.649 | ns |
| | | GCLK PLL | $t_{co}$ | 1.339 | 1.501 | 1.909 | 1.997 | 2.194 | 2.212 | 2.159 | 2.134 | 2.340 | 2.357 | 2.148 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.028 | 3.255 | 4.610 | 4.992 | 5.502 | 5.366 | 5.578 | 5.124 | 5.636 | 5.501 | 5.647 | ns |
| | | GCLK PLL | $t_{co}$ | 1.324 | 1.496 | 1.907 | 1.996 | 2.192 | 2.210 | 2.157 | 2.132 | 2.338 | 2.355 | 2.146 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.017 | 3.243 | 4.593 | 4.982 | 5.492 | 5.356 | 5.568 | 5.115 | 5.627 | 5.492 | 5.638 | ns |
| | | GCLK PLL | $t_{co}$ | 1.313 | 1.485 | 1.897 | 1.986 | 2.175 | 2.193 | 2.140 | 2.115 | 2.322 | 2.339 | 2.130 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.006 | 3.220 | 4.577 | 4.969 | 5.479 | 5.343 | 5.555 | 5.103 | 5.615 | 5.480 | 5.626 | ns |
| | | GCLK PLL | $t_{co}$ | 1.290 | 1.474 | 1.884 | 1.973 | 2.160 | 2.178 | 2.125 | 2.100 | 2.307 | 2.324 | 2.115 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.006 | 3.219 | 4.576 | 4.969 | 5.479 | 5.343 | 5.555 | 5.102 | 5.615 | 5.480 | 5.626 | ns |
| | | GCLK PLL | $t_{co}$ | 1.290 | 1.473 | 1.884 | 1.973 | 2.159 | 2.177 | 2.124 | 2.099 | 2.306 | 2.323 | 2.114 | ns |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.014 | 3.228 | 4.574 | 4.966 | 5.474 | 5.338 | 5.550 | 5.098 | 5.609 | 5.474 | 5.620 | ns |
| | | GCLK PLL | $t_{co}$ | 1.299 | 1.480 | 1.883 | 1.970 | 2.153 | 2.171 | 2.118 | 2.094 | 2.299 | 2.316 | 2.107 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.015 | 3.223 | 4.573 | 4.974 | 5.484 | 5.348 | 5.560 | 5.107 | 5.620 | 5.485 | 5.631 | ns |
| | | GCLK PLL | $t_{co}$ | 1.299 | 1.483 | 1.889 | 1.978 | 2.155 | 2.173 | 2.120 | 2.096 | 2.303 | 2.320 | 2.111 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.036 | 3.265 | 4.624 | 5.004 | 5.516 | 5.380 | 5.592 | 5.136 | 5.650 | 5.515 | 5.661 | ns |
| | | GCLK PLL | $t_{co}$ | 1.335 | 1.504 | 1.918 | 2.008 | 2.211 | 2.229 | 2.176 | 2.147 | 2.356 | 2.373 | 2.164 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.022 | 3.243 | 4.606 | 4.994 | 5.506 | 5.370 | 5.582 | 5.127 | 5.641 | 5.506 | 5.652 | ns |
| | | GCLK PLL | $t_{co}$ | 1.312 | 1.490 | 1.907 | 1.998 | 2.194 | 2.212 | 2.159 | 2.131 | 2.340 | 2.357 | 2.148 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.011 | 3.226 | 4.589 | 4.981 | 5.493 | 5.357 | 5.569 | 5.114 | 5.628 | 5.493 | 5.639 | ns |
| | | GCLK PLL | $t_{co}$ | 1.295 | 1.478 | 1.894 | 1.985 | 2.176 | 2.194 | 2.141 | 2.113 | 2.323 | 2.340 | 2.131 | ns |

**Table 1–54.** EP3SL70 Row Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.021 | 3.241 | 4.580 | 4.964 | 5.472 | 5.336 | 5.548 | 5.097 | 5.606 | 5.471 | 5.617 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.486 | 1.882 | 1.968 | 2.156 | 2.174 | 2.121 | 2.098 | 2.302 | 2.319 | 2.110 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.014 | 3.229 | 4.571 | 4.963 | 5.471 | 5.335 | 5.547 | 5.096 | 5.606 | 5.471 | 5.617 | ns |
| | | GCLK PLL | $t_{co}$ | 1.302 | 1.480 | 1.880 | 1.967 | 2.148 | 2.166 | 2.113 | 2.090 | 2.295 | 2.312 | 2.103 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.005 | 3.217 | 4.563 | 4.956 | 5.464 | 5.328 | 5.540 | 5.089 | 5.599 | 5.464 | 5.610 | ns |
| | | GCLK PLL | $t_{co}$ | 1.289 | 1.472 | 1.873 | 1.960 | 2.140 | 2.158 | 2.105 | 2.082 | 2.287 | 2.304 | 2.095 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.008 | 3.219 | 4.565 | 4.959 | 5.468 | 5.332 | 5.544 | 5.092 | 5.602 | 5.467 | 5.613 | ns |
| | | GCLK PLL | $t_{co}$ | 1.292 | 1.474 | 1.876 | 1.963 | 2.143 | 2.161 | 2.108 | 2.085 | 2.290 | 2.307 | 2.098 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.004 | 3.214 | 4.563 | 4.962 | 5.471 | 5.335 | 5.547 | 5.095 | 5.607 | 5.472 | 5.618 | ns |
| | | GCLK PLL | $t_{co}$ | 1.288 | 1.471 | 1.878 | 1.966 | 2.143 | 2.161 | 2.108 | 2.085 | 2.291 | 2.308 | 2.099 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.012 | 3.218 | 4.558 | 4.959 | 5.467 | 5.331 | 5.543 | 5.091 | 5.601 | 5.466 | 5.612 | ns |
| | | GCLK PLL | $t_{co}$ | 1.296 | 1.479 | 1.876 | 1.963 | 2.134 | 2.152 | 2.099 | 2.078 | 2.280 | 2.297 | 2.088 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.027 | 3.248 | 4.591 | 4.974 | 5.483 | 5.347 | 5.559 | 5.106 | 5.617 | 5.482 | 5.628 | ns |
| | | GCLK PLL | $t_{co}$ | 1.321 | 1.492 | 1.891 | 1.978 | 2.171 | 2.189 | 2.136 | 2.110 | 2.316 | 2.333 | 2.124 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.021 | 3.238 | 4.587 | 4.976 | 5.485 | 5.349 | 5.561 | 5.108 | 5.620 | 5.485 | 5.631 | ns |
| | | GCLK PLL | $t_{co}$ | 1.309 | 1.487 | 1.892 | 1.980 | 2.167 | 2.185 | 2.132 | 2.107 | 2.313 | 2.330 | 2.121 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.017 | 3.233 | 4.581 | 4.971 | 5.480 | 5.344 | 5.556 | 5.103 | 5.614 | 5.479 | 5.625 | ns |
| | | GCLK PLL | $t_{co}$ | 1.305 | 1.483 | 1.887 | 1.975 | 2.161 | 2.179 | 2.126 | 2.101 | 2.307 | 2.324 | 2.115 | ns |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.029 | 3.247 | 4.602 | 4.990 | 5.502 | 5.366 | 5.578 | 5.122 | 5.636 | 5.501 | 5.647 | ns |
| | | GCLK PLL | $t_{co}$ | 1.320 | 1.494 | 1.904 | 1.994 | 2.189 | 2.207 | 2.154 | 2.124 | 2.333 | 2.350 | 2.141 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.020 | 3.235 | 4.591 | 4.981 | 5.493 | 5.357 | 5.569 | 5.113 | 5.627 | 5.492 | 5.638 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.486 | 1.895 | 1.985 | 2.177 | 2.195 | 2.142 | 2.113 | 2.322 | 2.339 | 2.130 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.019 | 3.233 | 4.595 | 4.989 | 5.502 | 5.366 | 5.578 | 5.122 | 5.637 | 5.502 | 5.648 | ns |
| | | GCLK PLL | $t_{co}$ | 1.305 | 1.486 | 1.902 | 1.993 | 2.183 | 2.201 | 2.148 | 2.119 | 2.329 | 2.346 | 2.137 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.076 | 3.300 | 4.588 | 4.978 | 5.480 | 5.342 | 5.550 | 5.105 | 5.610 | 5.474 | 5.621 | ns |
| | | GCLK PLL | $t_{co}$ | 1.429 | 1.614 | 1.966 | 2.045 | 2.237 | 2.256 | 2.174 | 2.160 | 2.357 | 2.374 | 2.165 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.076 | 3.300 | 4.588 | 4.978 | 5.480 | 5.342 | 5.550 | 5.105 | 5.610 | 5.474 | 5.621 | ns |
| | | GCLK PLL | $t_{co}$ | 1.429 | 1.614 | 1.966 | 2.045 | 2.237 | 2.256 | 2.174 | 2.160 | 2.357 | 2.374 | 2.165 | ns |

Table 1–55 through Table 1–60 list the maximum I/O timing parameters for EP3SL70 devices for differential I/O standards.

Table 1–55 lists the EP3SL70 column pins input timing parameters for differential I/O standards.

**Table 1–55.** EP3SL70 Column Pins Input Timing Parameters (Part 1 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -0.697 | -0.717 | -1.072 | -1.182 | -1.294 | -1.237 | -1.524 | -1.183 | -1.296 | -1.242 | -1.562 | ns |
| | | $t_h$ | 0.814 | 0.849 | 1.257 | 1.389 | 1.522 | 1.454 | 1.740 | 1.398 | 1.532 | 1.469 | 1.777 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.159 | 1.821 | 2.053 | 2.279 | 2.166 | 2.172 | 2.063 | 2.288 | 2.173 | 2.219 | ns |
| | | $t_h$ | -0.892 | -0.893 | -1.424 | -1.606 | -1.781 | -1.696 | -1.696 | -1.608 | -1.782 | -1.694 | -1.742 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -0.697 | -0.717 | -1.072 | -1.182 | -1.294 | -1.237 | -1.524 | -1.183 | -1.296 | -1.242 | -1.562 | ns |
| | | $t_h$ | 0.814 | 0.849 | 1.257 | 1.389 | 1.522 | 1.454 | 1.740 | 1.398 | 1.532 | 1.469 | 1.777 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.159 | 1.821 | 2.053 | 2.279 | 2.166 | 2.172 | 2.063 | 2.288 | 2.173 | 2.219 | ns |
| | | $t_h$ | -0.892 | -0.893 | -1.424 | -1.606 | -1.781 | -1.696 | -1.696 | -1.608 | -1.782 | -1.694 | -1.742 | ns |
| RSDS | GCLK | $t_{su}$ | -0.705 | -0.729 | -1.082 | -1.193 | -1.310 | -1.253 | -1.540 | -1.194 | -1.311 | -1.257 | -1.577 | ns |
| | | $t_h$ | 0.822 | 0.861 | 1.267 | 1.400 | 1.538 | 1.470 | 1.756 | 1.409 | 1.547 | 1.484 | 1.792 | ns |
| | GCLK PLL | $t_{su}$ | 1.135 | 1.147 | 1.811 | 2.042 | 2.263 | 2.150 | 2.156 | 2.052 | 2.273 | 2.158 | 2.204 | ns |
| | | $t_h$ | -0.884 | -0.881 | -1.414 | -1.595 | -1.765 | -1.680 | -1.680 | -1.597 | -1.767 | -1.679 | -1.727 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.705 | -0.729 | -1.082 | -1.193 | -1.310 | -1.253 | -1.540 | -1.194 | -1.311 | -1.257 | -1.577 | ns |
| | | $t_h$ | 0.822 | 0.861 | 1.267 | 1.400 | 1.538 | 1.470 | 1.756 | 1.409 | 1.547 | 1.484 | 1.792 | ns |
| | GCLK PLL | $t_{su}$ | 1.135 | 1.147 | 1.811 | 2.042 | 2.263 | 2.150 | 2.156 | 2.052 | 2.273 | 2.158 | 2.204 | ns |
| | | $t_h$ | -0.884 | -0.881 | -1.414 | -1.595 | -1.765 | -1.680 | -1.680 | -1.597 | -1.767 | -1.679 | -1.727 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.717 | -0.740 | -1.091 | -1.204 | -1.329 | -1.272 | -1.559 | -1.205 | -1.329 | -1.275 | -1.595 | ns |
| | | $t_h$ | 0.834 | 0.872 | 1.277 | 1.411 | 1.557 | 1.489 | 1.775 | 1.420 | 1.565 | 1.502 | 1.810 | ns |
| | GCLK PLL | $t_{su}$ | 1.123 | 1.136 | 1.802 | 2.031 | 2.244 | 2.131 | 2.137 | 2.041 | 2.255 | 2.140 | 2.186 | ns |
| | | $t_h$ | -0.872 | -0.870 | -1.404 | -1.584 | -1.746 | -1.661 | -1.661 | -1.586 | -1.749 | -1.661 | -1.709 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.717 | -0.740 | -1.091 | -1.204 | -1.329 | -1.272 | -1.559 | -1.205 | -1.329 | -1.275 | -1.595 | ns |
| | | $t_h$ | 0.834 | 0.872 | 1.277 | 1.411 | 1.557 | 1.489 | 1.775 | 1.420 | 1.565 | 1.502 | 1.810 | ns |
| | GCLK PLL | $t_{su}$ | 1.123 | 1.136 | 1.802 | 2.031 | 2.244 | 2.131 | 2.137 | 2.041 | 2.255 | 2.140 | 2.186 | ns |
| | | $t_h$ | -0.872 | -0.870 | -1.404 | -1.584 | -1.746 | -1.661 | -1.661 | -1.586 | -1.749 | -1.661 | -1.709 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.705 | -0.729 | -1.082 | -1.193 | -1.310 | -1.253 | -1.540 | -1.194 | -1.311 | -1.257 | -1.577 | ns |
| | | $t_h$ | 0.822 | 0.861 | 1.267 | 1.400 | 1.538 | 1.470 | 1.756 | 1.409 | 1.547 | 1.484 | 1.792 | ns |
| | GCLK PLL | $t_{su}$ | 1.135 | 1.147 | 1.811 | 2.042 | 2.263 | 2.150 | 2.156 | 2.052 | 2.273 | 2.158 | 2.204 | ns |
| | | $t_h$ | -0.884 | -0.881 | -1.414 | -1.595 | -1.765 | -1.680 | -1.680 | -1.597 | -1.767 | -1.679 | -1.727 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.705 | -0.729 | -1.082 | -1.193 | -1.310 | -1.253 | -1.540 | -1.194 | -1.311 | -1.257 | -1.577 | ns |
| | | $t_h$ | 0.822 | 0.861 | 1.267 | 1.400 | 1.538 | 1.470 | 1.756 | 1.409 | 1.547 | 1.484 | 1.792 | ns |
| | GCLK PLL | $t_{su}$ | 1.135 | 1.147 | 1.811 | 2.042 | 2.263 | 2.150 | 2.156 | 2.052 | 2.273 | 2.158 | 2.204 | ns |
| | | $t_h$ | -0.884 | -0.881 | -1.414 | -1.595 | -1.765 | -1.680 | -1.680 | -1.597 | -1.767 | -1.679 | -1.727 | ns |

**Table 1–55.** EP3SL70 Column Pins Input Timing Parameters (Part 2 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.717 | -0.740 | -1.091 | -1.204 | -1.329 | -1.272 | -1.559 | -1.205 | -1.329 | -1.275 | -1.595 | ns |
| | | $t_h$ | 0.834 | 0.872 | 1.277 | 1.411 | 1.557 | 1.489 | 1.775 | 1.420 | 1.565 | 1.502 | 1.810 | ns |
| | GCLK PLL | $t_{su}$ | 1.123 | 1.136 | 1.802 | 2.031 | 2.244 | 2.131 | 2.137 | 2.041 | 2.255 | 2.140 | 2.186 | ns |
| | | $t_h$ | -0.872 | -0.870 | -1.404 | -1.584 | -1.746 | -1.661 | -1.661 | -1.586 | -1.749 | -1.661 | -1.709 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.717 | -0.740 | -1.091 | -1.204 | -1.329 | -1.272 | -1.559 | -1.205 | -1.329 | -1.275 | -1.595 | ns |
| | | $t_h$ | 0.834 | 0.872 | 1.277 | 1.411 | 1.557 | 1.489 | 1.775 | 1.420 | 1.565 | 1.502 | 1.810 | ns |
| | GCLK PLL | $t_{su}$ | 1.123 | 1.136 | 1.802 | 2.031 | 2.244 | 2.131 | 2.137 | 2.041 | 2.255 | 2.140 | 2.186 | ns |
| | | $t_h$ | -0.872 | -0.870 | -1.404 | -1.584 | -1.746 | -1.661 | -1.661 | -1.586 | -1.749 | -1.661 | -1.709 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.724 | -0.746 | -1.103 | -1.209 | -1.329 | -1.274 | -1.558 | -1.209 | -1.324 | -1.273 | -1.591 | ns |
| | | $t_h$ | 0.841 | 0.878 | 1.290 | 1.419 | 1.560 | 1.492 | 1.779 | 1.427 | 1.565 | 1.501 | 1.811 | ns |
| | GCLK PLL | $t_{su}$ | 1.116 | 1.130 | 1.790 | 2.026 | 2.244 | 2.129 | 2.138 | 2.037 | 2.260 | 2.142 | 2.190 | ns |
| | | $t_h$ | -0.865 | -0.864 | -1.391 | -1.576 | -1.743 | -1.658 | -1.657 | -1.579 | -1.749 | -1.662 | -1.708 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -0.724 | -0.746 | -1.103 | -1.209 | -1.329 | -1.274 | -1.558 | -1.209 | -1.324 | -1.273 | -1.591 | ns |
| | | $t_h$ | 0.841 | 0.878 | 1.290 | 1.419 | 1.560 | 1.492 | 1.779 | 1.427 | 1.565 | 1.501 | 1.811 | ns |
| | GCLK PLL | $t_{su}$ | 1.116 | 1.130 | 1.790 | 2.026 | 2.244 | 2.129 | 2.138 | 2.037 | 2.260 | 2.142 | 2.190 | ns |
| | | $t_h$ | -0.865 | -0.864 | -1.391 | -1.576 | -1.743 | -1.658 | -1.657 | -1.579 | -1.749 | -1.662 | -1.708 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -0.697 | -0.717 | -1.072 | -1.182 | -1.294 | -1.237 | -1.524 | -1.183 | -1.296 | -1.242 | -1.562 | ns |
| | | $t_h$ | 0.814 | 0.849 | 1.257 | 1.389 | 1.522 | 1.454 | 1.740 | 1.398 | 1.532 | 1.469 | 1.777 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.159 | 1.821 | 2.053 | 2.279 | 2.166 | 2.172 | 2.063 | 2.288 | 2.173 | 2.219 | ns |
| | | $t_h$ | -0.892 | -0.893 | -1.424 | -1.606 | -1.781 | -1.696 | -1.696 | -1.608 | -1.782 | -1.694 | -1.742 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.697 | -0.717 | -1.072 | -1.182 | -1.294 | -1.237 | -1.524 | -1.183 | -1.296 | -1.242 | -1.562 | ns |
| | | $t_h$ | 0.814 | 0.849 | 1.257 | 1.389 | 1.522 | 1.454 | 1.740 | 1.398 | 1.532 | 1.469 | 1.777 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.159 | 1.821 | 2.053 | 2.279 | 2.166 | 2.172 | 2.063 | 2.288 | 2.173 | 2.219 | ns |
| | | $t_h$ | -0.892 | -0.893 | -1.424 | -1.606 | -1.781 | -1.696 | -1.696 | -1.608 | -1.782 | -1.694 | -1.742 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.705 | -0.729 | -1.082 | -1.193 | -1.310 | -1.253 | -1.540 | -1.194 | -1.311 | -1.257 | -1.577 | ns |
| | | $t_h$ | 0.822 | 0.861 | 1.267 | 1.400 | 1.538 | 1.470 | 1.756 | 1.409 | 1.547 | 1.484 | 1.792 | ns |
| | GCLK PLL | $t_{su}$ | 1.135 | 1.147 | 1.811 | 2.042 | 2.263 | 2.150 | 2.156 | 2.052 | 2.273 | 2.158 | 2.204 | ns |
| | | $t_h$ | -0.884 | -0.881 | -1.414 | -1.595 | -1.765 | -1.680 | -1.680 | -1.597 | -1.767 | -1.679 | -1.727 | ns |

Table 1–56 lists the EP3SL70 row pins input timing parameters for differential I/O standards.

**Table 1–56.** EP3SL70 Row Pins Input Timing Parameters (Part 1 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -0.919 | -0.939 | -0.988 | -0.952 | -1.089 | -1.040 | -1.316 | -0.916 | -1.048 | -1.000 | -1.349 | ns |
| | | $t_h$ | 1.042 | 1.077 | 1.209 | 1.205 | 1.369 | 1.306 | 1.580 | 1.182 | 1.339 | 1.280 | 1.613 | ns |
| | GCLK PLL | $t_{su}$ | 0.882 | 0.896 | 1.863 | 2.243 | 2.446 | 2.322 | 2.342 | 2.291 | 2.500 | 2.376 | 2.393 | ns |
| | | $t_h$ | -0.625 | -0.625 | -1.430 | -1.749 | -1.896 | -1.802 | -1.817 | -1.783 | -1.936 | -1.843 | -1.865 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -0.919 | -0.939 | -0.988 | -0.952 | -1.089 | -1.040 | -1.316 | -0.916 | -1.048 | -1.000 | -1.349 | ns |
| | | $t_h$ | 1.042 | 1.077 | 1.209 | 1.205 | 1.369 | 1.306 | 1.580 | 1.182 | 1.339 | 1.280 | 1.613 | ns |
| | GCLK PLL | $t_{su}$ | 0.882 | 0.896 | 1.863 | 2.243 | 2.446 | 2.322 | 2.342 | 2.291 | 2.500 | 2.376 | 2.393 | ns |
| | | $t_h$ | -0.625 | -0.625 | -1.430 | -1.749 | -1.896 | -1.802 | -1.817 | -1.783 | -1.936 | -1.843 | -1.865 | ns |
| RSDS | GCLK | $t_{su}$ | -0.919 | -0.939 | -0.988 | -0.952 | -1.089 | -1.040 | -1.316 | -0.916 | -1.048 | -1.000 | -1.349 | ns |
| | | $t_h$ | 1.042 | 1.077 | 1.209 | 1.205 | 1.369 | 1.306 | 1.580 | 1.182 | 1.339 | 1.280 | 1.613 | ns |
| | GCLK PLL | $t_{su}$ | 0.882 | 0.896 | 1.863 | 2.243 | 2.446 | 2.322 | 2.342 | 2.291 | 2.500 | 2.376 | 2.393 | ns |
| | | $t_h$ | -0.625 | -0.625 | -1.430 | -1.749 | -1.896 | -1.802 | -1.817 | -1.783 | -1.936 | -1.843 | -1.865 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.734 | -0.764 | -1.085 | -1.186 | -1.286 | -1.234 | -1.505 | -1.193 | -1.291 | -1.242 | -1.543 | ns |
| | | $t_h$ | 0.850 | 0.893 | 1.274 | 1.394 | 1.516 | 1.451 | 1.720 | 1.410 | 1.531 | 1.470 | 1.758 | ns |
| | GCLK PLL | $t_{su}$ | 1.077 | 1.081 | 1.776 | 2.019 | 2.257 | 2.138 | 2.163 | 2.024 | 2.263 | 2.144 | 2.209 | ns |
| | | $t_h$ | -0.827 | -0.819 | -1.375 | -1.570 | -1.756 | -1.667 | -1.687 | -1.565 | -1.751 | -1.663 | -1.730 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.734 | -0.764 | -1.085 | -1.186 | -1.286 | -1.234 | -1.505 | -1.193 | -1.291 | -1.242 | -1.543 | ns |
| | | $t_h$ | 0.850 | 0.893 | 1.274 | 1.394 | 1.516 | 1.451 | 1.720 | 1.410 | 1.531 | 1.470 | 1.758 | ns |
| | GCLK PLL | $t_{su}$ | 1.077 | 1.081 | 1.776 | 2.019 | 2.257 | 2.138 | 2.163 | 2.024 | 2.263 | 2.144 | 2.209 | ns |
| | | $t_h$ | -0.827 | -0.819 | -1.375 | -1.570 | -1.756 | -1.667 | -1.687 | -1.565 | -1.751 | -1.663 | -1.730 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.743 | -0.776 | -1.094 | -1.196 | -1.302 | -1.250 | -1.521 | -1.202 | -1.307 | -1.258 | -1.559 | ns |
| | | $t_h$ | 0.859 | 0.905 | 1.283 | 1.404 | 1.532 | 1.467 | 1.736 | 1.419 | 1.547 | 1.486 | 1.774 | ns |
| | GCLK PLL | $t_{su}$ | 1.068 | 1.069 | 1.767 | 2.009 | 2.241 | 2.122 | 2.147 | 2.015 | 2.247 | 2.128 | 2.193 | ns |
| | | $t_h$ | -0.818 | -0.807 | -1.366 | -1.560 | -1.740 | -1.651 | -1.671 | -1.556 | -1.735 | -1.647 | -1.714 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.743 | -0.776 | -1.094 | -1.196 | -1.302 | -1.250 | -1.521 | -1.202 | -1.307 | -1.258 | -1.559 | ns |
| | | $t_h$ | 0.859 | 0.905 | 1.283 | 1.404 | 1.532 | 1.467 | 1.736 | 1.419 | 1.547 | 1.486 | 1.774 | ns |
| | GCLK PLL | $t_{su}$ | 1.068 | 1.069 | 1.767 | 2.009 | 2.241 | 2.122 | 2.147 | 2.015 | 2.247 | 2.128 | 2.193 | ns |
| | | $t_h$ | -0.818 | -0.807 | -1.366 | -1.560 | -1.740 | -1.651 | -1.671 | -1.556 | -1.735 | -1.647 | -1.714 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.757 | -0.788 | -1.107 | -1.206 | -1.320 | -1.268 | -1.539 | -1.213 | -1.324 | -1.275 | -1.576 | ns |
| | | $t_h$ | 0.873 | 0.917 | 1.295 | 1.414 | 1.550 | 1.485 | 1.754 | 1.430 | 1.564 | 1.503 | 1.791 | ns |
| | GCLK PLL | $t_{su}$ | 1.054 | 1.057 | 1.754 | 1.999 | 2.223 | 2.104 | 2.129 | 2.004 | 2.230 | 2.111 | 2.176 | ns |
| | | $t_h$ | -0.804 | -0.795 | -1.354 | -1.550 | -1.722 | -1.633 | -1.653 | -1.545 | -1.718 | -1.630 | -1.697 | ns |

**Table 1–56.** EP3SL70 Row Pins Input Timing Parameters (Part 2 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.757 | -0.788 | -1.107 | -1.206 | -1.320 | -1.268 | -1.539 | -1.213 | -1.324 | -1.275 | -1.576 | ns |
| | | $t_h$ | 0.873 | 0.917 | 1.295 | 1.414 | 1.550 | 1.485 | 1.754 | 1.430 | 1.564 | 1.503 | 1.791 | ns |
| | GCLK PLL | $t_{su}$ | 1.054 | 1.057 | 1.754 | 1.999 | 2.223 | 2.104 | 2.129 | 2.004 | 2.230 | 2.111 | 2.176 | ns |
| | | $t_h$ | -0.804 | -0.795 | -1.354 | -1.550 | -1.722 | -1.633 | -1.653 | -1.545 | -1.718 | -1.630 | -1.697 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.743 | -0.776 | -1.094 | -1.196 | -1.302 | -1.250 | -1.521 | -1.202 | -1.307 | -1.258 | -1.559 | ns |
| | | $t_h$ | 0.859 | 0.905 | 1.283 | 1.404 | 1.532 | 1.467 | 1.736 | 1.419 | 1.547 | 1.486 | 1.774 | ns |
| | GCLK PLL | $t_{su}$ | 1.068 | 1.069 | 1.767 | 2.009 | 2.241 | 2.122 | 2.147 | 2.015 | 2.247 | 2.128 | 2.193 | ns |
| | | $t_h$ | -0.818 | -0.807 | -1.366 | -1.560 | -1.740 | -1.651 | -1.671 | -1.556 | -1.735 | -1.647 | -1.714 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.743 | -0.776 | -1.094 | -1.196 | -1.302 | -1.250 | -1.521 | -1.202 | -1.307 | -1.258 | -1.559 | ns |
| | | $t_h$ | 0.859 | 0.905 | 1.283 | 1.404 | 1.532 | 1.467 | 1.736 | 1.419 | 1.547 | 1.486 | 1.774 | ns |
| | GCLK PLL | $t_{su}$ | 1.068 | 1.069 | 1.767 | 2.009 | 2.241 | 2.122 | 2.147 | 2.015 | 2.247 | 2.128 | 2.193 | ns |
| | | $t_h$ | -0.818 | -0.807 | -1.366 | -1.560 | -1.740 | -1.651 | -1.671 | -1.556 | -1.735 | -1.647 | -1.714 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -0.757 | -0.788 | -1.107 | -1.206 | -1.320 | -1.268 | -1.539 | -1.213 | -1.324 | -1.275 | -1.576 | ns |
| | | $t_h$ | 0.873 | 0.917 | 1.295 | 1.414 | 1.550 | 1.485 | 1.754 | 1.430 | 1.564 | 1.503 | 1.791 | ns |
| | GCLK PLL | $t_{su}$ | 1.054 | 1.057 | 1.754 | 1.999 | 2.223 | 2.104 | 2.129 | 2.004 | 2.230 | 2.111 | 2.176 | ns |
| | | $t_h$ | -0.804 | -0.795 | -1.354 | -1.550 | -1.722 | -1.633 | -1.653 | -1.545 | -1.718 | -1.630 | -1.697 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -0.757 | -0.788 | -1.107 | -1.206 | -1.320 | -1.268 | -1.539 | -1.213 | -1.324 | -1.275 | -1.576 | ns |
| | | $t_h$ | 0.873 | 0.917 | 1.295 | 1.414 | 1.550 | 1.485 | 1.754 | 1.430 | 1.564 | 1.503 | 1.791 | ns |
| | GCLK PLL | $t_{su}$ | 1.054 | 1.057 | 1.754 | 1.999 | 2.223 | 2.104 | 2.129 | 2.004 | 2.230 | 2.111 | 2.176 | ns |
| | | $t_h$ | -0.804 | -0.795 | -1.354 | -1.550 | -1.722 | -1.633 | -1.653 | -1.545 | -1.718 | -1.630 | -1.697 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.756 | -0.787 | -1.112 | -1.212 | -1.321 | -1.270 | -1.540 | -1.214 | -1.320 | -1.273 | -1.573 | ns |
| | | $t_h$ | 0.872 | 0.916 | 1.300 | 1.422 | 1.554 | 1.489 | 1.759 | 1.434 | 1.563 | 1.502 | 1.792 | ns |
| | GCLK PLL | $t_{su}$ | 1.045 | 1.048 | 1.739 | 1.983 | 2.212 | 2.092 | 2.118 | 1.993 | 2.224 | 2.103 | 2.169 | ns |
| | | $t_h$ | -0.795 | -0.786 | -1.339 | -1.532 | -1.708 | -1.619 | -1.638 | -1.531 | -1.709 | -1.621 | -1.686 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.756 | -0.787 | -1.112 | -1.212 | -1.321 | -1.270 | -1.540 | -1.214 | -1.320 | -1.273 | -1.573 | ns |
| | | $t_h$ | 0.872 | 0.916 | 1.300 | 1.422 | 1.554 | 1.489 | 1.759 | 1.434 | 1.563 | 1.502 | 1.792 | ns |
| | GCLK PLL | $t_{su}$ | 1.045 | 1.048 | 1.739 | 1.983 | 2.212 | 2.092 | 2.118 | 1.993 | 2.224 | 2.103 | 2.169 | ns |
| | | $t_h$ | -0.795 | -0.786 | -1.339 | -1.532 | -1.708 | -1.619 | -1.638 | -1.531 | -1.709 | -1.621 | -1.686 | ns |

Table 1–57 lists the EP3SL70 column pins output timing parameters for differential I/O standards.

**Table 1–57.** EP3SL70 Column Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.029 | 3.246 | 4.575 | 4.976 | 5.487 | 5.347 | 5.565 | 5.101 | 5.612 | 5.474 | 5.631 | ns |
| | | GCLK PLL | $t_{co}$ | 3.025 | 3.249 | 4.622 | 5.031 | 5.549 | 5.409 | 5.627 | 5.160 | 5.678 | 5.540 | 5.697 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.029 | 3.246 | 4.575 | 4.976 | 5.487 | 5.347 | 5.565 | 5.101 | 5.612 | 5.474 | 5.631 | ns |
| | | GCLK PLL | $t_{co}$ | 3.025 | 3.249 | 4.622 | 5.031 | 5.549 | 5.409 | 5.627 | 5.160 | 5.678 | 5.540 | 5.697 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.029 | 3.246 | 4.575 | 4.976 | 5.487 | 5.347 | 5.565 | 5.101 | 5.612 | 5.474 | 5.631 | ns |
| | | GCLK PLL | $t_{co}$ | 3.025 | 3.249 | 4.622 | 5.031 | 5.549 | 5.409 | 5.627 | 5.160 | 5.678 | 5.540 | 5.697 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.056 | 3.279 | 4.646 | 5.054 | 5.571 | 5.431 | 5.649 | 5.181 | 5.698 | 5.560 | 5.717 | ns |
| | | GCLK PLL | $t_{co}$ | 3.046 | 3.269 | 4.636 | 5.043 | 5.561 | 5.421 | 5.639 | 5.170 | 5.688 | 5.550 | 5.707 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.046 | 3.269 | 4.639 | 5.047 | 5.565 | 5.425 | 5.643 | 5.175 | 5.693 | 5.555 | 5.712 | ns |
| | | GCLK PLL | $t_{co}$ | 3.039 | 3.263 | 4.632 | 5.041 | 5.559 | 5.419 | 5.637 | 5.168 | 5.687 | 5.549 | 5.706 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.038 | 3.261 | 4.629 | 5.038 | 5.556 | 5.416 | 5.634 | 5.165 | 5.683 | 5.545 | 5.702 | ns |
| | | GCLK PLL | $t_{co}$ | 3.060 | 3.283 | 4.650 | 5.058 | 5.575 | 5.435 | 5.653 | 5.185 | 5.703 | 5.565 | 5.722 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.050 | 3.272 | 4.629 | 5.035 | 5.550 | 5.410 | 5.628 | 5.161 | 5.676 | 5.538 | 5.695 | ns |
| | | GCLK PLL | $t_{co}$ | 3.045 | 3.268 | 4.629 | 5.035 | 5.551 | 5.411 | 5.629 | 5.162 | 5.678 | 5.540 | 5.697 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.043 | 3.266 | 4.628 | 5.034 | 5.549 | 5.409 | 5.627 | 5.161 | 5.677 | 5.539 | 5.696 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.257 | 4.618 | 5.024 | 5.540 | 5.400 | 5.618 | 5.151 | 5.667 | 5.529 | 5.686 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.036 | 3.259 | 4.624 | 5.031 | 5.548 | 5.408 | 5.626 | 5.159 | 5.676 | 5.538 | 5.695 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.256 | 4.607 | 5.012 | 5.526 | 5.386 | 5.604 | 5.138 | 5.652 | 5.514 | 5.671 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.047 | 3.269 | 4.625 | 5.030 | 5.544 | 5.404 | 5.622 | 5.157 | 5.671 | 5.533 | 5.690 | ns |
| | | GCLK PLL | $t_{co}$ | 3.043 | 3.266 | 4.626 | 5.032 | 5.548 | 5.408 | 5.626 | 5.159 | 5.675 | 5.537 | 5.694 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.033 | 3.255 | 4.615 | 5.021 | 5.536 | 5.396 | 5.614 | 5.148 | 5.663 | 5.525 | 5.682 | ns |
| | | GCLK PLL | $t_{co}$ | 3.031 | 3.253 | 4.613 | 5.018 | 5.534 | 5.394 | 5.612 | 5.146 | 5.661 | 5.523 | 5.680 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.031 | 3.254 | 4.616 | 5.023 | 5.539 | 5.399 | 5.617 | 5.150 | 5.667 | 5.529 | 5.686 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.257 | 4.613 | 5.018 | 5.533 | 5.393 | 5.611 | 5.145 | 5.660 | 5.522 | 5.679 | ns |

**Table 1–57.** EP3SL70 Column Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.061 | 3.286 | 4.658 | 5.066 | 5.583 | 5.443 | 5.661 | 5.193 | 5.710 | 5.572 | 5.729 | ns |
| | | GCLK PLL | $t_{co}$ | 3.047 | 3.272 | 4.646 | 5.055 | 5.573 | 5.433 | 5.651 | 5.183 | 5.701 | 5.563 | 5.720 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.035 | 3.259 | 4.629 | 5.037 | 5.555 | 5.415 | 5.633 | 5.165 | 5.683 | 5.545 | 5.702 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.259 | 4.632 | 5.041 | 5.559 | 5.419 | 5.637 | 5.169 | 5.688 | 5.550 | 5.707 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.031 | 3.255 | 4.625 | 5.033 | 5.552 | 5.412 | 5.630 | 5.162 | 5.680 | 5.542 | 5.699 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.257 | 4.618 | 5.024 | 5.540 | 5.400 | 5.618 | 5.151 | 5.667 | 5.529 | 5.686 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.036 | 3.259 | 4.626 | 5.034 | 5.551 | 5.411 | 5.629 | 5.161 | 5.679 | 5.541 | 5.698 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.289 | 4.657 | 5.064 | 5.581 | 5.441 | 5.659 | 5.192 | 5.708 | 5.570 | 5.727 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.053 | 3.277 | 4.645 | 5.052 | 5.569 | 5.429 | 5.647 | 5.180 | 5.696 | 5.558 | 5.715 | ns |
| | | GCLK PLL | $t_{co}$ | 3.048 | 3.273 | 4.645 | 5.053 | 5.570 | 5.430 | 5.648 | 5.181 | 5.698 | 5.560 | 5.717 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.034 | 3.258 | 4.627 | 5.034 | 5.551 | 5.411 | 5.629 | 5.162 | 5.680 | 5.542 | 5.699 | ns |
| | | GCLK PLL | $t_{co}$ | 3.032 | 3.256 | 4.625 | 5.032 | 5.549 | 5.409 | 5.627 | 5.160 | 5.677 | 5.539 | 5.696 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.036 | 3.258 | 4.617 | 5.022 | 5.537 | 5.397 | 5.615 | 5.149 | 5.664 | 5.526 | 5.683 | ns |
| | | GCLK PLL | $t_{co}$ | 3.036 | 3.259 | 4.625 | 5.032 | 5.549 | 5.409 | 5.627 | 5.160 | 5.677 | 5.539 | 5.696 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.052 | 3.276 | 4.641 | 5.047 | 5.563 | 5.423 | 5.641 | 5.175 | 5.690 | 5.552 | 5.709 | ns |
| | | GCLK PLL | $t_{co}$ | 3.052 | 3.276 | 4.641 | 5.047 | 5.563 | 5.423 | 5.641 | 5.175 | 5.690 | 5.552 | 5.709 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.042 | 3.266 | 4.631 | 5.037 | 5.553 | 5.413 | 5.631 | 5.165 | 5.681 | 5.543 | 5.700 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.258 | 4.617 | 5.022 | 5.537 | 5.397 | 5.615 | 5.149 | 5.664 | 5.526 | 5.683 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.029 | 3.246 | 4.575 | 4.976 | 5.487 | 5.347 | 5.565 | 5.101 | 5.612 | 5.474 | 5.631 | ns |
| | | GCLK PLL | $t_{co}$ | 3.025 | 3.249 | 4.622 | 5.031 | 5.549 | 5.409 | 5.627 | 5.160 | 5.678 | 5.540 | 5.697 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.029 | 3.246 | 4.575 | 4.976 | 5.487 | 5.347 | 5.565 | 5.101 | 5.612 | 5.474 | 5.631 | ns |
| | | GCLK PLL | $t_{co}$ | 3.025 | 3.249 | 4.622 | 5.031 | 5.549 | 5.409 | 5.627 | 5.160 | 5.678 | 5.540 | 5.697 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.029 | 3.246 | 4.575 | 4.976 | 5.487 | 5.347 | 5.565 | 5.101 | 5.612 | 5.474 | 5.631 | ns |
| | | GCLK PLL | $t_{co}$ | 3.025 | 3.249 | 4.622 | 5.031 | 5.549 | 5.409 | 5.627 | 5.160 | 5.678 | 5.540 | 5.697 | ns |

**Table 1–57.** EP3SL70 Column Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.056 | 3.279 | 4.646 | 5.054 | 5.571 | 5.431 | 5.649 | 5.181 | 5.698 | 5.560 | 5.717 | ns |
| | | GCLK PLL | $t_{co}$ | 3.046 | 3.269 | 4.636 | 5.043 | 5.561 | 5.421 | 5.639 | 5.170 | 5.688 | 5.550 | 5.707 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.046 | 3.269 | 4.639 | 5.047 | 5.565 | 5.425 | 5.643 | 5.175 | 5.693 | 5.555 | 5.712 | ns |
| | | GCLK PLL | $t_{co}$ | 3.039 | 3.263 | 4.632 | 5.041 | 5.559 | 5.419 | 5.637 | 5.168 | 5.687 | 5.549 | 5.706 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.038 | 3.261 | 4.629 | 5.038 | 5.556 | 5.416 | 5.634 | 5.165 | 5.683 | 5.545 | 5.702 | ns |
| | | GCLK PLL | $t_{co}$ | 3.060 | 3.283 | 4.650 | 5.058 | 5.575 | 5.435 | 5.653 | 5.185 | 5.703 | 5.565 | 5.722 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.050 | 3.272 | 4.629 | 5.035 | 5.550 | 5.410 | 5.628 | 5.161 | 5.676 | 5.538 | 5.695 | ns |
| | | GCLK PLL | $t_{co}$ | 3.045 | 3.268 | 4.629 | 5.035 | 5.551 | 5.411 | 5.629 | 5.162 | 5.678 | 5.540 | 5.697 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.043 | 3.266 | 4.628 | 5.034 | 5.549 | 5.409 | 5.627 | 5.161 | 5.677 | 5.539 | 5.696 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.257 | 4.618 | 5.024 | 5.540 | 5.400 | 5.618 | 5.151 | 5.667 | 5.529 | 5.686 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.036 | 3.259 | 4.624 | 5.031 | 5.548 | 5.408 | 5.626 | 5.159 | 5.676 | 5.538 | 5.695 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.256 | 4.607 | 5.012 | 5.526 | 5.386 | 5.604 | 5.138 | 5.652 | 5.514 | 5.671 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.047 | 3.269 | 4.625 | 5.030 | 5.544 | 5.404 | 5.622 | 5.157 | 5.671 | 5.533 | 5.690 | ns |
| | | GCLK PLL | $t_{co}$ | 3.043 | 3.266 | 4.626 | 5.032 | 5.548 | 5.408 | 5.626 | 5.159 | 5.675 | 5.537 | 5.694 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.033 | 3.255 | 4.615 | 5.021 | 5.536 | 5.396 | 5.614 | 5.148 | 5.663 | 5.525 | 5.682 | ns |
| | | GCLK PLL | $t_{co}$ | 3.031 | 3.253 | 4.613 | 5.018 | 5.534 | 5.394 | 5.612 | 5.146 | 5.661 | 5.523 | 5.680 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.031 | 3.254 | 4.616 | 5.023 | 5.539 | 5.399 | 5.617 | 5.150 | 5.667 | 5.529 | 5.686 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.257 | 4.613 | 5.018 | 5.533 | 5.393 | 5.611 | 5.145 | 5.660 | 5.522 | 5.679 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.061 | 3.286 | 4.658 | 5.066 | 5.583 | 5.443 | 5.661 | 5.193 | 5.710 | 5.572 | 5.729 | ns |
| | | GCLK PLL | $t_{co}$ | 3.047 | 3.272 | 4.646 | 5.055 | 5.573 | 5.433 | 5.651 | 5.183 | 5.701 | 5.563 | 5.720 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.035 | 3.259 | 4.629 | 5.037 | 5.555 | 5.415 | 5.633 | 5.165 | 5.683 | 5.545 | 5.702 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.259 | 4.632 | 5.041 | 5.559 | 5.419 | 5.637 | 5.169 | 5.688 | 5.550 | 5.707 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.031 | 3.255 | 4.625 | 5.033 | 5.552 | 5.412 | 5.630 | 5.162 | 5.680 | 5.542 | 5.699 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.257 | 4.618 | 5.024 | 5.540 | 5.400 | 5.618 | 5.151 | 5.667 | 5.529 | 5.686 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.036 | 3.259 | 4.626 | 5.034 | 5.551 | 5.411 | 5.629 | 5.161 | 5.679 | 5.541 | 5.698 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.289 | 4.657 | 5.064 | 5.581 | 5.441 | 5.659 | 5.192 | 5.708 | 5.570 | 5.727 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.053 | 3.277 | 4.645 | 5.052 | 5.569 | 5.429 | 5.647 | 5.180 | 5.696 | 5.558 | 5.715 | ns |
| | | GCLK PLL | $t_{co}$ | 3.048 | 3.273 | 4.645 | 5.053 | 5.570 | 5.430 | 5.648 | 5.181 | 5.698 | 5.560 | 5.717 | ns |

**Table 1–57.** EP3SL70 Column Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.034 | 3.258 | 4.627 | 5.034 | 5.551 | 5.411 | 5.629 | 5.162 | 5.680 | 5.542 | 5.699 | ns |
| | | GCLK PLL | $t_{co}$ | 3.032 | 3.256 | 4.625 | 5.032 | 5.549 | 5.409 | 5.627 | 5.160 | 5.677 | 5.539 | 5.696 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.036 | 3.258 | 4.617 | 5.022 | 5.537 | 5.397 | 5.615 | 5.149 | 5.664 | 5.526 | 5.683 | ns |
| | | GCLK PLL | $t_{co}$ | 3.036 | 3.259 | 4.625 | 5.032 | 5.549 | 5.409 | 5.627 | 5.160 | 5.677 | 5.539 | 5.696 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.052 | 3.276 | 4.641 | 5.047 | 5.563 | 5.423 | 5.641 | 5.175 | 5.690 | 5.552 | 5.709 | ns |
| | | GCLK PLL | $t_{co}$ | 3.052 | 3.276 | 4.641 | 5.047 | 5.563 | 5.423 | 5.641 | 5.175 | 5.690 | 5.552 | 5.709 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.042 | 3.266 | 4.631 | 5.037 | 5.553 | 5.413 | 5.631 | 5.165 | 5.681 | 5.543 | 5.700 | ns |
| | | GCLK PLL | $t_{co}$ | 3.035 | 3.258 | 4.617 | 5.022 | 5.537 | 5.397 | 5.615 | 5.149 | 5.664 | 5.526 | 5.683 | ns |

Table 1–58 lists the EP3SL70 row pins output timing parameters for differential I/O standards.

**Table 1–58.** EP3SL70 Row Pins Output Timing Parameters (Part 1 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | — | GCLK | $t_{co}$ | 2.668 | 2.842 | 3.979 | 4.346 | 4.821 | 4.685 | 4.892 | 4.453 | 4.930 | 4.795 | 4.940 | ns |
| | | GCLK PLL | $t_{co}$ | 3.062 | 3.288 | 4.646 | 5.055 | 5.575 | 5.431 | 5.630 | 5.186 | 5.709 | 5.565 | 5.694 | ns |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.044 | 3.278 | 4.684 | 5.101 | 5.629 | 5.485 | 5.684 | 5.237 | 5.770 | 5.626 | 5.755 | ns |
| | | GCLK PLL | $t_{co}$ | 2.668 | 2.842 | 3.979 | 4.346 | 4.821 | 4.685 | 4.892 | 4.453 | 4.930 | 4.795 | 4.940 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.062 | 3.288 | 4.646 | 5.055 | 5.575 | 5.431 | 5.630 | 5.186 | 5.709 | 5.565 | 5.694 | ns |
| | | GCLK PLL | $t_{co}$ | 3.044 | 3.278 | 4.684 | 5.101 | 5.629 | 5.485 | 5.684 | 5.237 | 5.770 | 5.626 | 5.755 | ns |
| MINI-LVDS | — | GCLK | $t_{co}$ | 2.668 | 2.842 | 3.979 | 4.346 | 4.821 | 4.685 | 4.892 | 4.453 | 4.930 | 4.795 | 4.940 | ns |
| | | GCLK PLL | $t_{co}$ | 3.062 | 3.288 | 4.646 | 5.055 | 5.575 | 5.431 | 5.630 | 5.186 | 5.709 | 5.565 | 5.694 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.044 | 3.278 | 4.684 | 5.101 | 5.629 | 5.485 | 5.684 | 5.237 | 5.770 | 5.626 | 5.755 | ns |
| | | GCLK PLL | $t_{co}$ | 3.098 | 3.331 | 4.730 | 5.145 | 5.672 | 5.528 | 5.727 | 5.280 | 5.809 | 5.665 | 5.794 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.084 | 3.317 | 4.717 | 5.132 | 5.659 | 5.515 | 5.714 | 5.266 | 5.796 | 5.652 | 5.781 | ns |
| | | GCLK PLL | $t_{co}$ | 3.080 | 3.313 | 4.715 | 5.132 | 5.660 | 5.516 | 5.715 | 5.266 | 5.798 | 5.654 | 5.783 | ns |
| RSDS | — | GCLK | $t_{co}$ | 3.096 | 3.328 | 4.716 | 5.129 | 5.654 | 5.510 | 5.709 | 5.263 | 5.791 | 5.647 | 5.776 | ns |
| | | GCLK PLL | $t_{co}$ | 3.085 | 3.318 | 4.712 | 5.125 | 5.651 | 5.507 | 5.706 | 5.260 | 5.788 | 5.644 | 5.773 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.082 | 3.315 | 4.710 | 5.123 | 5.649 | 5.505 | 5.704 | 5.258 | 5.787 | 5.643 | 5.772 | ns |
| | | GCLK PLL | $t_{co}$ | 3.093 | 3.325 | 4.711 | 5.124 | 5.648 | 5.504 | 5.703 | 5.257 | 5.785 | 5.641 | 5.770 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.083 | 3.316 | 4.709 | 5.122 | 5.647 | 5.503 | 5.702 | 5.257 | 5.785 | 5.641 | 5.770 | ns |
| | | GCLK PLL | $t_{co}$ | 3.069 | 3.302 | 4.694 | 5.107 | 5.633 | 5.489 | 5.688 | 5.242 | 5.770 | 5.626 | 5.755 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.066 | 3.298 | 4.690 | 5.103 | 5.629 | 5.485 | 5.684 | 5.238 | 5.766 | 5.622 | 5.751 | ns |
| | | GCLK PLL | $t_{co}$ | 3.063 | 3.296 | 4.691 | 5.106 | 5.632 | 5.488 | 5.687 | 5.241 | 5.770 | 5.626 | 5.755 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.064 | 3.296 | 4.681 | 5.094 | 5.619 | 5.475 | 5.674 | 5.228 | 5.756 | 5.612 | 5.741 | ns |
| | | GCLK PLL | $t_{co}$ | 3.113 | 3.349 | 4.752 | 5.167 | 5.695 | 5.551 | 5.750 | 5.302 | 5.832 | 5.688 | 5.817 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.089 | 3.325 | 4.734 | 5.150 | 5.678 | 5.534 | 5.733 | 5.285 | 5.817 | 5.673 | 5.802 | ns |
| | | GCLK PLL | $t_{co}$ | 3.071 | 3.306 | 4.712 | 5.128 | 5.656 | 5.512 | 5.711 | 5.263 | 5.795 | 5.651 | 5.780 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.117 | 3.352 | 4.752 | 5.167 | 5.694 | 5.550 | 5.749 | 5.302 | 5.832 | 5.688 | 5.817 | ns |
| | | GCLK PLL | $t_{co}$ | 3.102 | 3.337 | 4.738 | 5.152 | 5.679 | 5.535 | 5.734 | 5.287 | 5.817 | 5.673 | 5.802 | ns |

**Table 1–58.** EP3SL70 Row Pins Output Timing Parameters (Part 2 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.091 | 3.326 | 4.733 | 5.149 | 5.676 | 5.532 | 5.731 | 5.284 | 5.815 | 5.671 | 5.800 | ns |
| | | GCLK PLL | $t_{co}$ | 3.071 | 3.306 | 4.710 | 5.125 | 5.653 | 5.509 | 5.708 | 5.261 | 5.791 | 5.647 | 5.776 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.068 | 3.302 | 4.706 | 5.122 | 5.649 | 5.505 | 5.704 | 5.257 | 5.788 | 5.644 | 5.773 | ns |
| | | GCLK PLL | $t_{co}$ | 3.073 | 3.306 | 4.697 | 5.110 | 5.635 | 5.491 | 5.690 | 5.244 | 5.772 | 5.628 | 5.757 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.066 | 3.299 | 4.696 | 5.111 | 5.638 | 5.494 | 5.693 | 5.247 | 5.777 | 5.633 | 5.762 | ns |
| | | GCLK PLL | $t_{co}$ | 3.094 | 3.328 | 4.724 | 5.138 | 5.664 | 5.520 | 5.719 | 5.273 | 5.802 | 5.658 | 5.787 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.076 | 3.311 | 4.709 | 5.123 | 5.649 | 5.505 | 5.704 | 5.258 | 5.787 | 5.643 | 5.772 | ns |
| | | GCLK PLL | $t_{co}$ | 3.062 | 3.295 | 4.686 | 5.099 | 5.624 | 5.480 | 5.679 | 5.234 | 5.762 | 5.618 | 5.747 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 8mA | GCLK | $t_{co}$ | 2.668 | 2.842 | 3.979 | 4.346 | 4.821 | 4.685 | 4.892 | 4.453 | 4.930 | 4.795 | 4.940 | ns |
| | | GCLK PLL | $t_{co}$ | 3.062 | 3.288 | 4.646 | 5.055 | 5.575 | 5.431 | 5.630 | 5.186 | 5.709 | 5.565 | 5.694 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 10mA | GCLK | $t_{co}$ | 3.044 | 3.278 | 4.684 | 5.101 | 5.629 | 5.485 | 5.684 | 5.237 | 5.770 | 5.626 | 5.755 | ns |
| | | GCLK PLL | $t_{co}$ | 2.668 | 2.842 | 3.979 | 4.346 | 4.821 | 4.685 | 4.892 | 4.453 | 4.930 | 4.795 | 4.940 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 12mA | GCLK | $t_{co}$ | 3.062 | 3.288 | 4.646 | 5.055 | 5.575 | 5.431 | 5.630 | 5.186 | 5.709 | 5.565 | 5.694 | ns |
| | | GCLK PLL | $t_{co}$ | 3.044 | 3.278 | 4.684 | 5.101 | 5.629 | 5.485 | 5.684 | 5.237 | 5.770 | 5.626 | 5.755 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 2.668 | 2.842 | 3.979 | 4.346 | 4.821 | 4.685 | 4.892 | 4.453 | 4.930 | 4.795 | 4.940 | ns |
| | | GCLK PLL | $t_{co}$ | 3.062 | 3.288 | 4.646 | 5.055 | 5.575 | 5.431 | 5.630 | 5.186 | 5.709 | 5.565 | 5.694 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.044 | 3.278 | 4.684 | 5.101 | 5.629 | 5.485 | 5.684 | 5.237 | 5.770 | 5.626 | 5.755 | ns |
| | | GCLK PLL | $t_{co}$ | 3.098 | 3.331 | 4.730 | 5.145 | 5.672 | 5.528 | 5.727 | 5.280 | 5.809 | 5.665 | 5.794 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.084 | 3.317 | 4.717 | 5.132 | 5.659 | 5.515 | 5.714 | 5.266 | 5.796 | 5.652 | 5.781 | ns |
| | | GCLK PLL | $t_{co}$ | 3.080 | 3.313 | 4.715 | 5.132 | 5.660 | 5.516 | 5.715 | 5.266 | 5.798 | 5.654 | 5.783 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.096 | 3.328 | 4.716 | 5.129 | 5.654 | 5.510 | 5.709 | 5.263 | 5.791 | 5.647 | 5.776 | ns |
| | | GCLK PLL | $t_{co}$ | 3.085 | 3.318 | 4.712 | 5.125 | 5.651 | 5.507 | 5.706 | 5.260 | 5.788 | 5.644 | 5.773 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.082 | 3.315 | 4.710 | 5.123 | 5.649 | 5.505 | 5.704 | 5.258 | 5.787 | 5.643 | 5.772 | ns |
| | | GCLK PLL | $t_{co}$ | 3.093 | 3.325 | 4.711 | 5.124 | 5.648 | 5.504 | 5.703 | 5.257 | 5.785 | 5.641 | 5.770 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.083 | 3.316 | 4.709 | 5.122 | 5.647 | 5.503 | 5.702 | 5.257 | 5.785 | 5.641 | 5.770 | ns |
| | | GCLK PLL | $t_{co}$ | 3.069 | 3.302 | 4.694 | 5.107 | 5.633 | 5.489 | 5.688 | 5.242 | 5.770 | 5.626 | 5.755 | ns |

**Table 1–58.** EP3SL70 Row Pins Output Timing Parameters (Part 3 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.066 | 3.298 | 4.690 | 5.103 | 5.629 | 5.485 | 5.684 | 5.238 | 5.766 | 5.622 | 5.751 | ns |
| | | GCLK PLL | $t_{co}$ | 3.063 | 3.296 | 4.691 | 5.106 | 5.632 | 5.488 | 5.687 | 5.241 | 5.770 | 5.626 | 5.755 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 10mA | GCLK | $t_{co}$ | 3.064 | 3.296 | 4.681 | 5.094 | 5.619 | 5.475 | 5.674 | 5.228 | 5.756 | 5.612 | 5.741 | ns |
| | | GCLK PLL | $t_{co}$ | 3.113 | 3.349 | 4.752 | 5.167 | 5.695 | 5.551 | 5.750 | 5.302 | 5.832 | 5.688 | 5.817 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 12mA | GCLK | $t_{co}$ | 3.089 | 3.325 | 4.734 | 5.150 | 5.678 | 5.534 | 5.733 | 5.285 | 5.817 | 5.673 | 5.802 | ns |
| | | GCLK PLL | $t_{co}$ | 3.071 | 3.306 | 4.712 | 5.128 | 5.656 | 5.512 | 5.711 | 5.263 | 5.795 | 5.651 | 5.780 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.117 | 3.352 | 4.752 | 5.167 | 5.694 | 5.550 | 5.749 | 5.302 | 5.832 | 5.688 | 5.817 | ns |
| | | GCLK PLL | $t_{co}$ | 3.102 | 3.337 | 4.738 | 5.152 | 5.679 | 5.535 | 5.734 | 5.287 | 5.817 | 5.673 | 5.802 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.091 | 3.326 | 4.733 | 5.149 | 5.676 | 5.532 | 5.731 | 5.284 | 5.815 | 5.671 | 5.800 | ns |
| | | GCLK PLL | $t_{co}$ | 3.071 | 3.306 | 4.710 | 5.125 | 5.653 | 5.509 | 5.708 | 5.261 | 5.791 | 5.647 | 5.776 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.068 | 3.302 | 4.706 | 5.122 | 5.649 | 5.505 | 5.704 | 5.257 | 5.788 | 5.644 | 5.773 | ns |
| | | GCLK PLL | $t_{co}$ | 3.073 | 3.306 | 4.697 | 5.110 | 5.635 | 5.491 | 5.690 | 5.244 | 5.772 | 5.628 | 5.757 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 12mA | GCLK | $t_{co}$ | 3.066 | 3.299 | 4.696 | 5.111 | 5.638 | 5.494 | 5.693 | 5.247 | 5.777 | 5.633 | 5.762 | ns |
| | | GCLK PLL | $t_{co}$ | 3.094 | 3.328 | 4.724 | 5.138 | 5.664 | 5.520 | 5.719 | 5.273 | 5.802 | 5.658 | 5.787 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.076 | 3.311 | 4.709 | 5.123 | 5.649 | 5.505 | 5.704 | 5.258 | 5.787 | 5.643 | 5.772 | ns |
| | | GCLK PLL | $t_{co}$ | 3.062 | 3.295 | 4.686 | 5.099 | 5.624 | 5.480 | 5.679 | 5.234 | 5.762 | 5.618 | 5.747 | ns |

Table 1–59 and Table 1–60 list the EP3SL70 regional clock (RCLK) adder values that must be added to the GCLK values. Use these adder values to determine I/O timing when the I/O pin is driven using the regional clock. This applies to all I/O standards supported by Stratix III devices.

Table 1–59 lists the EP3SL70 column pin delay adders when using the regional clock.

**Table 1–59.** EP3SL70 Column Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.158 | 0.168 | 0.225 | 0.241 | 0.257 | 0.247 | 0.313 | 0.244 | 0.258 | 0.252 | 0.315 | ns |
| RCLK PLL input adder | -0.014 | -0.012 | -0.007 | -0.003 | -0.002 | -0.005 | 0.191 | -0.003 | -0.003 | -0.004 | 0.191 | ns |
| RCLK output adder | -0.114 | -0.116 | -0.137 | -0.139 | -0.141 | -0.137 | -0.215 | -0.132 | -0.133 | -0.136 | -0.215 | ns |
| RCLK PLL output adder | 1.642 | 1.675 | 2.599 | 2.912 | 3.223 | 3.071 | 3.22 | 2.931 | 3.238 | 3.083 | 3.338 | ns |

Table 1–60 lists the EP3SL70 row pin delay adders when using the regional clock.

**Table 1–60.** EP3SL70 Row Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.111 | 0.123 | 0.177 | 0.192 | 0.207 | 0.198 | 0.263 | 0.194 | 0.212 | 0.201 | 0.266 | ns |
| RCLK PLL input adder | 0.099 | 0.105 | 0.156 | 0.175 | 0.195 | 0.185 | 0.263 | 0.177 | 0.195 | 0.188 | 0.263 | ns |
| RCLK output adder | -0.113 | -0.127 | -0.183 | -0.198 | -0.213 | -0.205 | -0.272 | -0.202 | -0.216 | -0.21 | -0.273 | ns |
| RCLK PLL output adder | -0.107 | -0.112 | -0.164 | -0.185 | -0.202 | -0.193 | -0.258 | -0.184 | -0.204 | -0.197 | -0.257 | ns |

## EP3SL110 I/O Timing Parameters

Table 1–61 through Table 1–65 list the maximum I/O timing parameters for EP3SL110 devices for single-ended I/O standards.

Table 1–61 lists the EP3SL110 column pins input timing parameters for single-ended I/O standards.

**Table 1–61.** EP3SL110 Column Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -0.917 | -0.917 | -1.333 | -1.452 | -1.682 | -1.627 | -1.980 | -1.452 | -1.682 | -1.627 | -1.980 | ns |
| | | $t_h$ | 1.053 | 1.053 | 1.524 | 1.667 | 1.918 | 1.850 | 2.205 | 1.667 | 1.918 | 1.850 | 2.205 | ns |
| | GCLK PLL | $t_{su}$ | -1.234 | -1.176 | -1.704 | -1.940 | -2.210 | -2.135 | -2.470 | -1.940 | -2.210 | -2.135 | -2.470 | ns |
| | | $t_h$ | 1.512 | 1.460 | 2.116 | 2.394 | 2.710 | 2.610 | 2.971 | 2.394 | 2.710 | 2.610 | 2.971 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -0.917 | -0.917 | -1.333 | -1.452 | -1.682 | -1.627 | -1.980 | -1.452 | -1.682 | -1.627 | -1.980 | ns |
| | | $t_h$ | 1.053 | 1.053 | 1.524 | 1.667 | 1.918 | 1.850 | 2.205 | 1.667 | 1.918 | 1.850 | 2.205 | ns |
| | GCLK PLL | $t_{su}$ | -1.234 | -1.176 | -1.704 | -1.940 | -2.210 | -2.135 | -2.470 | -1.940 | -2.210 | -2.135 | -2.470 | ns |
| | | $t_h$ | 1.512 | 1.460 | 2.116 | 2.394 | 2.710 | 2.610 | 2.971 | 2.394 | 2.710 | 2.610 | 2.971 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -0.928 | -0.928 | -1.332 | -1.454 | -1.681 | -1.626 | -1.979 | -1.454 | -1.681 | -1.626 | -1.979 | ns |
| | | $t_h$ | 1.064 | 1.064 | 1.523 | 1.669 | 1.917 | 1.849 | 2.204 | 1.669 | 1.917 | 1.849 | 2.204 | ns |
| | GCLK PLL | $t_{su}$ | -1.245 | -1.187 | -1.703 | -1.942 | -2.209 | -2.134 | -2.469 | -1.942 | -2.209 | -2.134 | -2.469 | ns |
| | | $t_h$ | 1.523 | 1.471 | 2.115 | 2.396 | 2.709 | 2.609 | 2.970 | 2.396 | 2.709 | 2.609 | 2.970 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -0.928 | -0.928 | -1.332 | -1.454 | -1.681 | -1.626 | -1.979 | -1.454 | -1.681 | -1.626 | -1.979 | ns |
| | | $t_h$ | 1.064 | 1.064 | 1.523 | 1.669 | 1.917 | 1.849 | 2.204 | 1.669 | 1.917 | 1.849 | 2.204 | ns |
| | GCLK PLL | $t_{su}$ | -1.245 | -1.187 | -1.703 | -1.942 | -2.209 | -2.134 | -2.469 | -1.942 | -2.209 | -2.134 | -2.469 | ns |
| | | $t_h$ | 1.523 | 1.471 | 2.115 | 2.396 | 2.709 | 2.609 | 2.970 | 2.396 | 2.709 | 2.609 | 2.970 | ns |
| 2.5 V | GCLK | $t_{su}$ | -0.923 | -0.923 | -1.341 | -1.466 | -1.700 | -1.645 | -1.998 | -1.466 | -1.700 | -1.645 | -1.998 | ns |
| | | $t_h$ | 1.059 | 1.059 | 1.532 | 1.681 | 1.936 | 1.868 | 2.223 | 1.681 | 1.936 | 1.868 | 2.223 | ns |
| | GCLK PLL | $t_{su}$ | -1.240 | -1.182 | -1.712 | -1.954 | -2.228 | -2.153 | -2.488 | -1.954 | -2.228 | -2.153 | -2.488 | ns |
| | | $t_h$ | 1.518 | 1.466 | 2.124 | 2.408 | 2.728 | 2.628 | 2.989 | 2.408 | 2.728 | 2.628 | 2.989 | ns |

**Table 1–61.** EP3SL110 Column Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | GCLK | $t_{su}$ | -0.943 | -0.943 | -1.381 | -1.502 | -1.698 | -1.643 | -1.996 | -1.502 | -1.698 | -1.643 | -1.996 | ns |
| | | $t_h$ | 1.081 | 1.081 | 1.572 | 1.717 | 1.934 | 1.866 | 2.221 | 1.717 | 1.934 | 1.866 | 2.221 | ns |
| | GCLK PLL | $t_{su}$ | -1.262 | -1.202 | -1.752 | -1.990 | -2.226 | -2.151 | -2.486 | -1.990 | -2.226 | -2.151 | -2.486 | ns |
| | | $t_h$ | 1.542 | 1.488 | 2.164 | 2.444 | 2.726 | 2.626 | 2.987 | 2.444 | 2.726 | 2.626 | 2.987 | ns |
| 1.5 V | GCLK | $t_{su}$ | -0.933 | -0.933 | -1.358 | -1.470 | -1.628 | -1.573 | -1.926 | -1.470 | -1.628 | -1.573 | -1.926 | ns |
| | | $t_h$ | 1.071 | 1.071 | 1.549 | 1.685 | 1.864 | 1.796 | 2.151 | 1.685 | 1.864 | 1.796 | 2.151 | ns |
| | GCLK PLL | $t_{su}$ | -1.252 | -1.192 | -1.729 | -1.958 | -2.156 | -2.081 | -2.416 | -1.958 | -2.156 | -2.081 | -2.416 | ns |
| | | $t_h$ | 1.532 | 1.478 | 2.141 | 2.412 | 2.656 | 2.556 | 2.917 | 2.412 | 2.656 | 2.556 | 2.917 | ns |
| 1.2 V | GCLK | $t_{su}$ | -0.881 | -0.881 | -1.281 | -1.371 | -1.472 | -1.417 | -1.770 | -1.371 | -1.472 | -1.417 | -1.770 | ns |
| | | $t_h$ | 1.019 | 1.019 | 1.472 | 1.586 | 1.708 | 1.640 | 1.995 | 1.586 | 1.708 | 1.640 | 1.995 | ns |
| | GCLK PLL | $t_{su}$ | -1.200 | -1.140 | -1.652 | -1.859 | -2.000 | -1.925 | -2.260 | -1.859 | -2.000 | -1.925 | -2.260 | ns |
| | | $t_h$ | 1.480 | 1.426 | 2.064 | 2.313 | 2.500 | 2.400 | 2.761 | 2.313 | 2.500 | 2.400 | 2.761 | ns |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -0.852 | -0.852 | -1.253 | -1.355 | -1.474 | -1.419 | -1.772 | -1.355 | -1.474 | -1.419 | -1.772 | ns |
| | | $t_h$ | 0.990 | 0.990 | 1.444 | 1.570 | 1.710 | 1.642 | 1.997 | 1.570 | 1.710 | 1.642 | 1.997 | ns |
| | GCLK PLL | $t_{su}$ | -1.171 | -1.111 | -1.624 | -1.843 | -2.002 | -1.927 | -2.262 | -1.843 | -2.002 | -1.927 | -2.262 | ns |
| | | $t_h$ | 1.451 | 1.397 | 2.036 | 2.297 | 2.502 | 2.402 | 2.763 | 2.297 | 2.502 | 2.402 | 2.763 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -0.852 | -0.852 | -1.253 | -1.355 | -1.474 | -1.419 | -1.772 | -1.355 | -1.474 | -1.419 | -1.772 | ns |
| | | $t_h$ | 0.990 | 0.990 | 1.444 | 1.570 | 1.710 | 1.642 | 1.997 | 1.570 | 1.710 | 1.642 | 1.997 | ns |
| | GCLK PLL | $t_{su}$ | -1.171 | -1.111 | -1.624 | -1.843 | -2.002 | -1.927 | -2.262 | -1.843 | -2.002 | -1.927 | -2.262 | ns |
| | | $t_h$ | 1.451 | 1.397 | 2.036 | 2.297 | 2.502 | 2.402 | 2.763 | 2.297 | 2.502 | 2.402 | 2.763 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -0.846 | -0.846 | -1.241 | -1.350 | -1.474 | -1.417 | -1.773 | -1.350 | -1.474 | -1.417 | -1.773 | ns |
| | | $t_h$ | 0.984 | 0.984 | 1.431 | 1.562 | 1.707 | 1.639 | 1.993 | 1.562 | 1.707 | 1.639 | 1.993 | ns |
| | GCLK PLL | $t_{su}$ | -1.165 | -1.105 | -1.612 | -1.835 | -1.999 | -1.922 | -2.263 | -1.835 | -1.999 | -1.922 | -2.263 | ns |
| | | $t_h$ | 1.445 | 1.391 | 2.023 | 2.286 | 2.496 | 2.396 | 2.759 | 2.286 | 2.496 | 2.396 | 2.759 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -0.846 | -0.846 | -1.241 | -1.350 | -1.474 | -1.417 | -1.773 | -1.350 | -1.474 | -1.417 | -1.773 | ns |
| | | $t_h$ | 0.984 | 0.984 | 1.431 | 1.562 | 1.707 | 1.639 | 1.993 | 1.562 | 1.707 | 1.639 | 1.993 | ns |
| | GCLK PLL | $t_{su}$ | -1.165 | -1.105 | -1.612 | -1.835 | -1.999 | -1.922 | -2.263 | -1.835 | -1.999 | -1.922 | -2.263 | ns |
| | | $t_h$ | 1.445 | 1.391 | 2.023 | 2.286 | 2.496 | 2.396 | 2.759 | 2.286 | 2.496 | 2.396 | 2.759 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -0.835 | -0.835 | -1.232 | -1.339 | -1.455 | -1.398 | -1.754 | -1.339 | -1.455 | -1.398 | -1.754 | ns |
| | | $t_h$ | 0.973 | 0.973 | 1.421 | 1.551 | 1.688 | 1.620 | 1.974 | 1.551 | 1.688 | 1.620 | 1.974 | ns |
| | GCLK PLL | $t_{su}$ | -1.154 | -1.094 | -1.603 | -1.824 | -1.980 | -1.903 | -2.244 | -1.824 | -1.980 | -1.903 | -2.244 | ns |
| | | $t_h$ | 1.434 | 1.380 | 2.013 | 2.275 | 2.477 | 2.377 | 2.740 | 2.275 | 2.477 | 2.377 | 2.740 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.835 | -0.835 | -1.232 | -1.339 | -1.455 | -1.398 | -1.754 | -1.339 | -1.455 | -1.398 | -1.754 | ns |
| | | $t_h$ | 0.973 | 0.973 | 1.421 | 1.551 | 1.688 | 1.620 | 1.974 | 1.551 | 1.688 | 1.620 | 1.974 | ns |
| | GCLK PLL | $t_{su}$ | -1.154 | -1.094 | -1.603 | -1.824 | -1.980 | -1.903 | -2.244 | -1.824 | -1.980 | -1.903 | -2.244 | ns |
| | | $t_h$ | 1.434 | 1.380 | 2.013 | 2.275 | 2.477 | 2.377 | 2.740 | 2.275 | 2.477 | 2.377 | 2.740 | ns |

**Table 1–61.** EP3SL110 Column Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.846 | -0.846 | -1.241 | -1.350 | -1.474 | -1.417 | -1.773 | -1.350 | -1.474 | -1.417 | -1.773 | ns |
| | | $t_h$ | 0.984 | 0.984 | 1.431 | 1.562 | 1.707 | 1.639 | 1.993 | 1.562 | 1.707 | 1.639 | 1.993 | ns |
| | GCLK PLL | $t_{su}$ | -1.165 | -1.105 | -1.612 | -1.835 | -1.999 | -1.922 | -2.263 | -1.835 | -1.999 | -1.922 | -2.263 | ns |
| | | $t_h$ | 1.445 | 1.391 | 2.023 | 2.286 | 2.496 | 2.396 | 2.759 | 2.286 | 2.496 | 2.396 | 2.759 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.846 | -0.846 | -1.241 | -1.350 | -1.474 | -1.417 | -1.773 | -1.350 | -1.474 | -1.417 | -1.773 | ns |
| | | $t_h$ | 0.984 | 0.984 | 1.431 | 1.562 | 1.707 | 1.639 | 1.993 | 1.562 | 1.707 | 1.639 | 1.993 | ns |
| | GCLK PLL | $t_{su}$ | -1.165 | -1.105 | -1.612 | -1.835 | -1.999 | -1.922 | -2.263 | -1.835 | -1.999 | -1.922 | -2.263 | ns |
| | | $t_h$ | 1.445 | 1.391 | 2.023 | 2.286 | 2.496 | 2.396 | 2.759 | 2.286 | 2.496 | 2.396 | 2.759 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.835 | -0.835 | -1.232 | -1.339 | -1.455 | -1.398 | -1.754 | -1.339 | -1.455 | -1.398 | -1.754 | ns |
| | | $t_h$ | 0.973 | 0.973 | 1.421 | 1.551 | 1.688 | 1.620 | 1.974 | 1.551 | 1.688 | 1.620 | 1.974 | ns |
| | GCLK PLL | $t_{su}$ | -1.154 | -1.094 | -1.603 | -1.824 | -1.980 | -1.903 | -2.244 | -1.824 | -1.980 | -1.903 | -2.244 | ns |
| | | $t_h$ | 1.434 | 1.380 | 2.013 | 2.275 | 2.477 | 2.377 | 2.740 | 2.275 | 2.477 | 2.377 | 2.740 | ns |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.835 | -0.835 | -1.232 | -1.339 | -1.455 | -1.398 | -1.754 | -1.339 | -1.455 | -1.398 | -1.754 | ns |
| | | $t_h$ | 0.973 | 0.973 | 1.421 | 1.551 | 1.688 | 1.620 | 1.974 | 1.551 | 1.688 | 1.620 | 1.974 | ns |
| | GCLK PLL | $t_{su}$ | -1.154 | -1.094 | -1.603 | -1.824 | -1.980 | -1.903 | -2.244 | -1.824 | -1.980 | -1.903 | -2.244 | ns |
| | | $t_h$ | 1.434 | 1.380 | 2.013 | 2.275 | 2.477 | 2.377 | 2.740 | 2.275 | 2.477 | 2.377 | 2.740 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.823 | -0.823 | -1.222 | -1.328 | -1.439 | -1.382 | -1.738 | -1.328 | -1.439 | -1.382 | -1.738 | ns |
| | | $t_h$ | 0.961 | 0.961 | 1.411 | 1.540 | 1.672 | 1.604 | 1.958 | 1.540 | 1.672 | 1.604 | 1.958 | ns |
| | GCLK PLL | $t_{su}$ | -1.142 | -1.082 | -1.593 | -1.813 | -1.964 | -1.887 | -2.228 | -1.813 | -1.964 | -1.887 | -2.228 | ns |
| | | $t_h$ | 1.422 | 1.368 | 2.003 | 2.264 | 2.461 | 2.361 | 2.724 | 2.264 | 2.461 | 2.361 | 2.724 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -0.823 | -0.823 | -1.222 | -1.328 | -1.439 | -1.382 | -1.738 | -1.328 | -1.439 | -1.382 | -1.738 | ns |
| | | $t_h$ | 0.961 | 0.961 | 1.411 | 1.540 | 1.672 | 1.604 | 1.958 | 1.540 | 1.672 | 1.604 | 1.958 | ns |
| | GCLK PLL | $t_{su}$ | -1.142 | -1.082 | -1.593 | -1.813 | -1.964 | -1.887 | -2.228 | -1.813 | -1.964 | -1.887 | -2.228 | ns |
| | | $t_h$ | 1.422 | 1.368 | 2.003 | 2.264 | 2.461 | 2.361 | 2.724 | 2.264 | 2.461 | 2.361 | 2.724 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | -0.928 | -0.928 | -1.332 | -1.454 | -1.681 | -1.626 | -1.979 | -1.454 | -1.681 | -1.626 | -1.979 | ns |
| | | $t_h$ | 1.064 | 1.064 | 1.523 | 1.669 | 1.917 | 1.849 | 2.204 | 1.669 | 1.917 | 1.849 | 2.204 | ns |
| | GCLK PLL | $t_{su}$ | -1.245 | -1.187 | -1.703 | -1.942 | -2.209 | -2.134 | -2.469 | -1.942 | -2.209 | -2.134 | -2.469 | ns |
| | | $t_h$ | 1.523 | 1.471 | 2.115 | 2.396 | 2.709 | 2.609 | 2.970 | 2.396 | 2.709 | 2.609 | 2.970 | ns |

Table 1–62 lists the EP3SL110 row pins input timing parameters for single-ended I/O standards.

**Table 1–62.** EP3SL110 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -0.910 | -0.883 | -1.252 | -1.441 | -1.559 | -1.604 | -1.843 | -1.465 | -1.551 | -1.605 | -1.881 | ns |
| | | $t_h$ | 1.025 | 1.015 | 1.440 | 1.648 | 1.792 | 1.822 | 2.066 | 1.682 | 1.794 | 1.831 | 2.104 | ns |
| | GCLK PLL | $t_{su}$ | 0.992 | 1.013 | 1.646 | 1.862 | 1.976 | 1.860 | 1.804 | 1.870 | 1.998 | 1.880 | 1.856 | ns |
| | | $t_h$ | -0.741 | -0.746 | -1.246 | -1.412 | -1.475 | -1.388 | -1.322 | -1.411 | -1.486 | -1.398 | -1.371 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -0.910 | -0.883 | -1.252 | -1.441 | -1.559 | -1.604 | -1.843 | -1.465 | -1.551 | -1.605 | -1.881 | ns |
| | | $t_h$ | 1.025 | 1.015 | 1.440 | 1.648 | 1.792 | 1.822 | 2.066 | 1.682 | 1.794 | 1.831 | 2.104 | ns |
| | GCLK PLL | $t_{su}$ | 0.992 | 1.013 | 1.646 | 1.862 | 1.976 | 1.860 | 1.804 | 1.870 | 1.998 | 1.880 | 1.856 | ns |
| | | $t_h$ | -0.741 | -0.746 | -1.246 | -1.412 | -1.475 | -1.388 | -1.322 | -1.411 | -1.486 | -1.398 | -1.371 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -0.916 | -0.894 | -1.249 | -1.442 | -1.562 | -1.607 | -1.846 | -1.464 | -1.556 | -1.610 | -1.886 | ns |
| | | $t_h$ | 1.031 | 1.026 | 1.437 | 1.649 | 1.795 | 1.825 | 2.069 | 1.681 | 1.799 | 1.836 | 2.109 | ns |
| | GCLK PLL | $t_{su}$ | 0.986 | 1.002 | 1.649 | 1.861 | 1.973 | 1.857 | 1.801 | 1.871 | 1.993 | 1.875 | 1.851 | ns |
| | | $t_h$ | -0.735 | -0.735 | -1.249 | -1.411 | -1.472 | -1.385 | -1.319 | -1.412 | -1.481 | -1.393 | -1.366 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -0.916 | -0.894 | -1.249 | -1.442 | -1.562 | -1.607 | -1.846 | -1.464 | -1.556 | -1.610 | -1.886 | ns |
| | | $t_h$ | 1.031 | 1.026 | 1.437 | 1.649 | 1.795 | 1.825 | 2.069 | 1.681 | 1.799 | 1.836 | 2.109 | ns |
| | GCLK PLL | $t_{su}$ | 0.986 | 1.002 | 1.649 | 1.861 | 1.973 | 1.857 | 1.801 | 1.871 | 1.993 | 1.875 | 1.851 | ns |
| | | $t_h$ | -0.735 | -0.735 | -1.249 | -1.411 | -1.472 | -1.385 | -1.319 | -1.412 | -1.481 | -1.393 | -1.366 | ns |
| 2.5 V | GCLK | $t_{su}$ | -0.904 | -0.887 | -1.258 | -1.455 | -1.577 | -1.622 | -1.861 | -1.473 | -1.566 | -1.620 | -1.896 | ns |
| | | $t_h$ | 1.019 | 1.019 | 1.446 | 1.662 | 1.810 | 1.840 | 2.084 | 1.690 | 1.809 | 1.846 | 2.119 | ns |
| | GCLK PLL | $t_{su}$ | 0.998 | 1.009 | 1.640 | 1.848 | 1.958 | 1.842 | 1.786 | 1.862 | 1.983 | 1.865 | 1.841 | ns |
| | | $t_h$ | -0.747 | -0.742 | -1.240 | -1.398 | -1.457 | -1.370 | -1.304 | -1.403 | -1.471 | -1.383 | -1.356 | ns |
| 1.8 V | GCLK | $t_{su}$ | -0.873 | -0.918 | -1.298 | -1.402 | -1.575 | -1.530 | -1.859 | -1.402 | -1.567 | -1.526 | -1.897 | ns |
| | | $t_h$ | 0.990 | 1.051 | 1.486 | 1.612 | 1.808 | 1.751 | 2.082 | 1.622 | 1.810 | 1.756 | 2.120 | ns |
| | GCLK PLL | $t_{su}$ | 0.968 | 0.977 | 1.600 | 1.815 | 1.960 | 1.844 | 1.788 | 1.829 | 1.982 | 1.864 | 1.840 | ns |
| | | $t_h$ | -0.716 | -0.709 | -1.200 | -1.365 | -1.459 | -1.372 | -1.306 | -1.370 | -1.470 | -1.382 | -1.355 | ns |
| 1.5 V | GCLK | $t_{su}$ | -0.863 | -0.907 | -1.274 | -1.370 | -1.507 | -1.462 | -1.791 | -1.371 | -1.502 | -1.461 | -1.832 | ns |
| | | $t_h$ | 0.980 | 1.040 | 1.462 | 1.580 | 1.740 | 1.683 | 2.014 | 1.591 | 1.745 | 1.691 | 2.055 | ns |
| | GCLK PLL | $t_{su}$ | 0.978 | 0.988 | 1.624 | 1.847 | 2.028 | 1.912 | 1.856 | 1.860 | 2.047 | 1.929 | 1.905 | ns |
| | | $t_h$ | -0.726 | -0.720 | -1.224 | -1.397 | -1.527 | -1.440 | -1.374 | -1.401 | -1.535 | -1.447 | -1.420 | ns |
| 1.2 V | GCLK | $t_{su}$ | -0.803 | -0.854 | -1.195 | -1.269 | -1.348 | -1.303 | -1.632 | -1.275 | -1.347 | -1.306 | -1.677 | ns |
| | | $t_h$ | 0.920 | 0.987 | 1.383 | 1.479 | 1.581 | 1.524 | 1.855 | 1.495 | 1.590 | 1.536 | 1.900 | ns |
| | GCLK PLL | $t_{su}$ | 1.038 | 1.041 | 1.703 | 1.948 | 2.187 | 2.071 | 2.015 | 1.956 | 2.202 | 2.084 | 2.060 | ns |
| | | $t_h$ | -0.786 | -0.773 | -1.303 | -1.498 | -1.686 | -1.599 | -1.533 | -1.497 | -1.690 | -1.602 | -1.575 | ns |

**Table 1–62.** EP3SL110 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -0.847 | -0.828 | -1.172 | -1.346 | -1.357 | -1.402 | -1.641 | -1.361 | -1.349 | -1.403 | -1.679 | ns |
| | | $t_h$ | 0.963 | 0.961 | 1.360 | 1.553 | 1.590 | 1.620 | 1.864 | 1.578 | 1.592 | 1.629 | 1.902 | ns |
| | GCLK PLL | $t_{su}$ | 1.055 | 1.067 | 1.726 | 1.957 | 2.178 | 2.062 | 2.006 | 1.974 | 2.200 | 2.082 | 2.058 | ns |
| | | $t_h$ | -0.803 | -0.799 | -1.326 | -1.507 | -1.677 | -1.590 | -1.524 | -1.515 | -1.688 | -1.600 | -1.573 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -0.847 | -0.828 | -1.172 | -1.346 | -1.357 | -1.402 | -1.641 | -1.361 | -1.349 | -1.403 | -1.679 | ns |
| | | $t_h$ | 0.963 | 0.961 | 1.360 | 1.553 | 1.590 | 1.620 | 1.864 | 1.578 | 1.592 | 1.629 | 1.902 | ns |
| | GCLK PLL | $t_{su}$ | 1.055 | 1.067 | 1.726 | 1.957 | 2.178 | 2.062 | 2.006 | 1.974 | 2.200 | 2.082 | 2.058 | ns |
| | | $t_h$ | -0.803 | -0.799 | -1.326 | -1.507 | -1.677 | -1.590 | -1.524 | -1.515 | -1.688 | -1.600 | -1.573 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -0.777 | -0.819 | -1.157 | -1.244 | -1.346 | -1.300 | -1.630 | -1.246 | -1.343 | -1.300 | -1.672 | ns |
| | | $t_h$ | 0.894 | 0.952 | 1.345 | 1.452 | 1.576 | 1.519 | 1.849 | 1.463 | 1.583 | 1.529 | 1.891 | ns |
| | GCLK PLL | $t_{su}$ | 1.064 | 1.076 | 1.741 | 1.975 | 2.192 | 2.077 | 2.019 | 1.988 | 2.209 | 2.092 | 2.067 | ns |
| | | $t_h$ | -0.812 | -0.808 | -1.341 | -1.527 | -1.693 | -1.606 | -1.541 | -1.531 | -1.700 | -1.611 | -1.586 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -0.777 | -0.819 | -1.157 | -1.244 | -1.346 | -1.300 | -1.630 | -1.246 | -1.343 | -1.300 | -1.672 | ns |
| | | $t_h$ | 0.894 | 0.952 | 1.345 | 1.452 | 1.576 | 1.519 | 1.849 | 1.463 | 1.583 | 1.529 | 1.891 | ns |
| | GCLK PLL | $t_{su}$ | 1.064 | 1.076 | 1.741 | 1.975 | 2.192 | 2.077 | 2.019 | 1.988 | 2.209 | 2.092 | 2.067 | ns |
| | | $t_h$ | -0.812 | -0.808 | -1.341 | -1.527 | -1.693 | -1.606 | -1.541 | -1.531 | -1.700 | -1.611 | -1.586 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -0.763 | -0.807 | -1.144 | -1.234 | -1.328 | -1.282 | -1.612 | -1.235 | -1.326 | -1.283 | -1.655 | ns |
| | | $t_h$ | 0.880 | 0.940 | 1.333 | 1.442 | 1.558 | 1.501 | 1.831 | 1.452 | 1.566 | 1.512 | 1.874 | ns |
| | GCLK PLL | $t_{su}$ | 1.078 | 1.088 | 1.756 | 1.985 | 2.210 | 2.095 | 2.037 | 1.999 | 2.226 | 2.109 | 2.084 | ns |
| | | $t_h$ | -0.826 | -0.820 | -1.355 | -1.537 | -1.711 | -1.624 | -1.559 | -1.542 | -1.717 | -1.628 | -1.603 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.777 | -0.819 | -1.157 | -1.244 | -1.346 | -1.300 | -1.630 | -1.246 | -1.343 | -1.300 | -1.672 | ns |
| | | $t_h$ | 0.894 | 0.952 | 1.345 | 1.452 | 1.576 | 1.519 | 1.849 | 1.463 | 1.583 | 1.529 | 1.891 | ns |
| | GCLK PLL | $t_{su}$ | 1.064 | 1.076 | 1.741 | 1.975 | 2.192 | 2.077 | 2.019 | 1.988 | 2.209 | 2.092 | 2.067 | ns |
| | | $t_h$ | -0.812 | -0.808 | -1.341 | -1.527 | -1.693 | -1.606 | -1.541 | -1.531 | -1.700 | -1.611 | -1.586 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.777 | -0.819 | -1.157 | -1.244 | -1.346 | -1.300 | -1.630 | -1.246 | -1.343 | -1.300 | -1.672 | ns |
| | | $t_h$ | 0.894 | 0.952 | 1.345 | 1.452 | 1.576 | 1.519 | 1.849 | 1.463 | 1.583 | 1.529 | 1.891 | ns |
| | GCLK PLL | $t_{su}$ | 1.064 | 1.076 | 1.741 | 1.975 | 2.192 | 2.077 | 2.019 | 1.988 | 2.209 | 2.092 | 2.067 | ns |
| | | $t_h$ | -0.812 | -0.808 | -1.341 | -1.527 | -1.693 | -1.606 | -1.541 | -1.531 | -1.700 | -1.611 | -1.586 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.763 | -0.807 | -1.144 | -1.234 | -1.328 | -1.282 | -1.612 | -1.235 | -1.326 | -1.283 | -1.655 | ns |
| | | $t_h$ | 0.880 | 0.940 | 1.333 | 1.442 | 1.558 | 1.501 | 1.831 | 1.452 | 1.566 | 1.512 | 1.874 | ns |
| | GCLK PLL | $t_{su}$ | 1.078 | 1.088 | 1.756 | 1.985 | 2.210 | 2.095 | 2.037 | 1.999 | 2.226 | 2.109 | 2.084 | ns |
| | | $t_h$ | -0.826 | -0.820 | -1.355 | -1.537 | -1.711 | -1.624 | -1.559 | -1.542 | -1.717 | -1.628 | -1.603 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.763 | -0.807 | -1.144 | -1.234 | -1.328 | -1.282 | -1.612 | -1.235 | -1.326 | -1.283 | -1.655 | ns |
| | | $t_h$ | 0.880 | 0.940 | 1.333 | 1.442 | 1.558 | 1.501 | 1.831 | 1.452 | 1.566 | 1.512 | 1.874 | ns |
| | GCLK PLL | $t_{su}$ | 1.078 | 1.088 | 1.756 | 1.985 | 2.210 | 2.095 | 2.037 | 1.999 | 2.226 | 2.109 | 2.084 | ns |
| | | $t_h$ | -0.826 | -0.820 | -1.355 | -1.537 | -1.711 | -1.624 | -1.559 | -1.542 | -1.717 | -1.628 | -1.603 | ns |

**Table 1–62.** EP3SL110 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.754 | -0.795 | -1.135 | -1.224 | -1.312 | -1.266 | -1.596 | -1.226 | -1.310 | -1.267 | -1.639 | ns |
| | | $t_h$ | 0.871 | 0.928 | 1.324 | 1.432 | 1.542 | 1.485 | 1.815 | 1.443 | 1.550 | 1.496 | 1.858 | ns |
| | GCLK PLL | $t_{su}$ | 1.087 | 1.100 | 1.765 | 1.995 | 2.226 | 2.111 | 2.053 | 2.008 | 2.242 | 2.125 | 2.100 | ns |
| | | $t_h$ | -0.835 | -0.832 | -1.364 | -1.547 | -1.727 | -1.640 | -1.575 | -1.551 | -1.733 | -1.644 | -1.619 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.754 | -0.795 | -1.135 | -1.224 | -1.312 | -1.266 | -1.596 | -1.226 | -1.310 | -1.267 | -1.639 | ns |
| | | $t_h$ | 0.871 | 0.928 | 1.324 | 1.432 | 1.542 | 1.485 | 1.815 | 1.443 | 1.550 | 1.496 | 1.858 | ns |
| | GCLK PLL | $t_{su}$ | 1.087 | 1.100 | 1.765 | 1.995 | 2.226 | 2.111 | 2.053 | 2.008 | 2.242 | 2.125 | 2.100 | ns |
| | | $t_h$ | -0.835 | -0.832 | -1.364 | -1.547 | -1.727 | -1.640 | -1.575 | -1.551 | -1.733 | -1.644 | -1.619 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -0.916 | -0.894 | -1.249 | -1.442 | -1.562 | -1.607 | -1.846 | -1.464 | -1.556 | -1.610 | -1.886 | ns |
| | | $t_h$ | 1.031 | 1.026 | 1.437 | 1.649 | 1.795 | 1.825 | 2.069 | 1.681 | 1.799 | 1.836 | 2.109 | ns |
| | GCLK PLL | $t_{su}$ | 0.986 | 1.002 | 1.649 | 1.861 | 1.973 | 1.857 | 1.801 | 1.871 | 1.993 | 1.875 | 1.851 | ns |
| | | $t_h$ | -0.735 | -0.735 | -1.249 | -1.411 | -1.472 | -1.385 | -1.319 | -1.412 | -1.481 | -1.393 | -1.366 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | -0.916 | -0.894 | -1.249 | -1.442 | -1.562 | -1.607 | -1.846 | -1.464 | -1.556 | -1.610 | -1.886 | ns |
| | | $t_h$ | 1.031 | 1.026 | 1.437 | 1.649 | 1.795 | 1.825 | 2.069 | 1.681 | 1.799 | 1.836 | 2.109 | ns |
| | GCLK PLL | $t_{su}$ | 0.986 | 1.002 | 1.649 | 1.861 | 1.973 | 1.857 | 1.801 | 1.871 | 1.993 | 1.875 | 1.851 | ns |
| | | $t_h$ | -0.735 | -0.735 | -1.249 | -1.411 | -1.472 | -1.385 | -1.319 | -1.412 | -1.481 | -1.393 | -1.366 | ns |

Table 1–63 lists the EP3SL110 column pins output timing parameters for single-ended I/O standards.

**Table 1–63.** EP3SL110 Column Pins Output Timing Parameters (Part 1 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.439 | 3.439 | 4.768 | 5.145 | 5.638 | 5.507 | 5.801 | 5.145 | 5.638 | 5.507 | 5.801 | ns |
| | | GCLK PLL | $t_{co}$ | 3.829 | 3.829 | 5.344 | 5.778 | 6.326 | 6.168 | 6.550 | 5.778 | 6.326 | 6.168 | 6.550 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.372 | 3.372 | 4.659 | 5.034 | 5.525 | 5.394 | 5.688 | 5.034 | 5.525 | 5.394 | 5.688 | ns |
| | | GCLK PLL | $t_{co}$ | 3.762 | 3.762 | 5.235 | 5.667 | 6.213 | 6.055 | 6.437 | 5.667 | 6.213 | 6.055 | 6.437 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.286 | 3.286 | 4.556 | 4.936 | 5.433 | 5.302 | 5.596 | 4.936 | 5.433 | 5.302 | 5.596 | ns |
| | | GCLK PLL | $t_{co}$ | 3.676 | 3.676 | 5.131 | 5.568 | 6.121 | 5.963 | 6.345 | 5.568 | 6.121 | 5.963 | 6.345 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.279 | 3.279 | 4.539 | 4.908 | 5.392 | 5.261 | 5.555 | 4.908 | 5.392 | 5.261 | 5.555 | ns |
| | | GCLK PLL | $t_{co}$ | 3.669 | 3.669 | 5.114 | 5.540 | 6.080 | 5.922 | 6.304 | 5.540 | 6.080 | 5.922 | 6.304 | ns |


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**Table 1–63.** EP3SL110 Column Pins Output Timing Parameters (Part 2 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.445 | 3.445 | 4.773 | 5.150 | 5.645 | 5.514 | 5.808 | 5.150 | 5.645 | 5.514 | 5.808 | ns |
| | | GCLK PLL | $t_{co}$ | 3.835 | 3.835 | 5.348 | 5.783 | 6.333 | 6.175 | 6.557 | 5.783 | 6.333 | 6.175 | 6.557 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.290 | 3.290 | 4.566 | 4.953 | 5.444 | 5.313 | 5.607 | 4.953 | 5.444 | 5.313 | 5.607 | ns |
| | | GCLK PLL | $t_{co}$ | 3.680 | 3.680 | 5.141 | 5.585 | 6.132 | 5.974 | 6.356 | 5.585 | 6.132 | 5.974 | 6.356 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.297 | 3.297 | 4.560 | 4.932 | 5.418 | 5.287 | 5.581 | 4.932 | 5.418 | 5.287 | 5.581 | ns |
| | | GCLK PLL | $t_{co}$ | 3.687 | 3.687 | 5.135 | 5.564 | 6.106 | 5.948 | 6.330 | 5.564 | 6.106 | 5.948 | 6.330 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.281 | 3.281 | 4.537 | 4.906 | 5.389 | 5.258 | 5.552 | 4.906 | 5.389 | 5.258 | 5.552 | ns |
| | | GCLK PLL | $t_{co}$ | 3.671 | 3.671 | 5.113 | 5.539 | 6.077 | 5.919 | 6.301 | 5.539 | 6.077 | 5.919 | 6.301 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.403 | 3.403 | 4.735 | 5.114 | 5.605 | 5.474 | 5.768 | 5.114 | 5.605 | 5.474 | 5.768 | ns |
| | | GCLK PLL | $t_{co}$ | 3.793 | 3.793 | 5.311 | 5.746 | 6.293 | 6.135 | 6.517 | 5.746 | 6.293 | 6.135 | 6.517 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.292 | 3.292 | 4.605 | 4.980 | 5.467 | 5.337 | 5.629 | 4.980 | 5.467 | 5.337 | 5.629 | ns |
| | | GCLK PLL | $t_{co}$ | 3.682 | 3.682 | 5.181 | 5.612 | 6.156 | 5.999 | 6.379 | 5.612 | 6.156 | 5.999 | 6.379 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.256 | 3.256 | 4.542 | 4.911 | 5.393 | 5.263 | 5.556 | 4.911 | 5.393 | 5.263 | 5.556 | ns |
| | | GCLK PLL | $t_{co}$ | 3.646 | 3.646 | 5.118 | 5.543 | 6.082 | 5.925 | 6.305 | 5.543 | 6.082 | 5.925 | 6.305 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.238 | 3.238 | 4.513 | 4.883 | 5.365 | 5.234 | 5.528 | 4.883 | 5.365 | 5.234 | 5.528 | ns |
| | | GCLK PLL | $t_{co}$ | 3.628 | 3.628 | 5.089 | 5.515 | 6.053 | 5.895 | 6.277 | 5.515 | 6.053 | 5.895 | 6.277 | ns |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.317 | 3.317 | 4.639 | 5.013 | 5.502 | 5.372 | 5.664 | 5.013 | 5.502 | 5.372 | 5.664 | ns |
| | | GCLK PLL | $t_{co}$ | 3.707 | 3.707 | 5.215 | 5.646 | 6.191 | 6.034 | 6.414 | 5.646 | 6.191 | 6.034 | 6.414 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.238 | 3.238 | 4.516 | 4.884 | 5.367 | 5.237 | 5.529 | 4.884 | 5.367 | 5.237 | 5.529 | ns |
| | | GCLK PLL | $t_{co}$ | 3.628 | 3.628 | 5.091 | 5.517 | 6.056 | 5.899 | 6.279 | 5.517 | 6.056 | 5.899 | 6.279 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.233 | 3.233 | 4.508 | 4.877 | 5.359 | 5.228 | 5.522 | 4.877 | 5.359 | 5.228 | 5.522 | ns |
| | | GCLK PLL | $t_{co}$ | 3.623 | 3.623 | 5.084 | 5.510 | 6.047 | 5.889 | 6.271 | 5.510 | 6.047 | 5.889 | 6.271 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.224 | 3.224 | 4.494 | 4.862 | 5.344 | 5.213 | 5.507 | 4.862 | 5.344 | 5.213 | 5.507 | ns |
| | | GCLK PLL | $t_{co}$ | 3.614 | 3.614 | 5.070 | 5.495 | 6.032 | 5.874 | 6.256 | 5.495 | 6.032 | 5.874 | 6.256 | ns |

**Table 1–63.** EP3SL110 Column Pins Output Timing Parameters (Part 3 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.439 | 3.439 | 4.846 | 5.240 | 5.749 | 5.619 | 5.912 | 5.240 | 5.749 | 5.619 | 5.912 | ns |
| | | GCLK PLL | $t_{co}$ | 3.829 | 3.829 | 5.422 | 5.873 | 6.438 | 6.281 | 6.661 | 5.873 | 6.438 | 6.281 | 6.661 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.339 | 3.339 | 4.727 | 5.114 | 5.617 | 5.487 | 5.779 | 5.114 | 5.617 | 5.487 | 5.779 | ns |
| | | GCLK PLL | $t_{co}$ | 3.729 | 3.729 | 5.303 | 5.747 | 6.306 | 6.149 | 6.529 | 5.747 | 6.306 | 6.149 | 6.529 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.295 | 3.295 | 4.640 | 5.024 | 5.522 | 5.391 | 5.685 | 5.024 | 5.522 | 5.391 | 5.685 | ns |
| | | GCLK PLL | $t_{co}$ | 3.685 | 3.685 | 5.216 | 5.656 | 6.210 | 6.052 | 6.434 | 5.656 | 6.210 | 6.052 | 6.434 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.257 | 3.257 | 4.601 | 4.981 | 5.479 | 5.348 | 5.642 | 4.981 | 5.479 | 5.348 | 5.642 | ns |
| | | GCLK PLL | $t_{co}$ | 3.647 | 3.647 | 5.177 | 5.614 | 6.167 | 6.009 | 6.391 | 5.614 | 6.167 | 6.009 | 6.391 | ns |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.630 | 3.630 | 5.168 | 5.600 | 6.154 | 6.023 | 6.317 | 5.600 | 6.154 | 6.023 | 6.317 | ns |
| | | GCLK PLL | $t_{co}$ | 4.020 | 4.020 | 5.743 | 6.233 | 6.842 | 6.684 | 7.066 | 6.233 | 6.842 | 6.684 | 7.066 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.449 | 3.449 | 4.889 | 5.291 | 5.806 | 5.676 | 5.968 | 5.291 | 5.806 | 5.676 | 5.968 | ns |
| | | GCLK PLL | $t_{co}$ | 3.839 | 3.839 | 5.464 | 5.924 | 6.495 | 6.338 | 6.718 | 5.924 | 6.495 | 6.338 | 6.718 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.367 | 3.367 | 4.782 | 5.176 | 5.696 | 5.565 | 5.859 | 5.176 | 5.696 | 5.565 | 5.859 | ns |
| | | GCLK PLL | $t_{co}$ | 3.757 | 3.757 | 5.357 | 5.809 | 6.384 | 6.226 | 6.608 | 5.809 | 6.384 | 6.226 | 6.608 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.347 | 3.347 | 4.723 | 5.123 | 5.630 | 5.499 | 5.793 | 5.123 | 5.630 | 5.499 | 5.793 | ns |
| | | GCLK PLL | $t_{co}$ | 3.737 | 3.737 | 5.299 | 5.755 | 6.318 | 6.160 | 6.542 | 5.755 | 6.318 | 6.160 | 6.542 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.284 | 3.284 | 4.662 | 5.048 | 5.549 | 5.418 | 5.712 | 5.048 | 5.549 | 5.418 | 5.712 | ns |
| | | GCLK PLL | $t_{co}$ | 3.674 | 3.674 | 5.238 | 5.680 | 6.237 | 6.079 | 6.461 | 5.680 | 6.237 | 6.079 | 6.461 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.266 | 3.266 | 4.642 | 5.026 | 5.526 | 5.395 | 5.689 | 5.026 | 5.526 | 5.395 | 5.689 | ns |
| | | GCLK PLL | $t_{co}$ | 3.656 | 3.656 | 5.217 | 5.659 | 6.214 | 6.056 | 6.438 | 5.659 | 6.214 | 6.056 | 6.438 | ns |

**Table 1–63.** EP3SL110 Column Pins Output Timing Parameters (Part 4 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.576 | 3.576 | 5.096 | 5.533 | 6.092 | 5.961 | 6.255 | 5.533 | 6.092 | 5.961 | 6.255 | ns |
| | | GCLK PLL | $t_{co}$ | 3.966 | 3.966 | 5.672 | 6.165 | 6.780 | 6.622 | 7.004 | 6.165 | 6.780 | 6.622 | 7.004 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.364 | 3.364 | 4.777 | 5.176 | 5.700 | 5.569 | 5.863 | 5.176 | 5.700 | 5.569 | 5.863 | ns |
| | | GCLK PLL | $t_{co}$ | 3.754 | 3.754 | 5.353 | 5.809 | 6.388 | 6.230 | 6.612 | 5.809 | 6.388 | 6.230 | 6.612 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.339 | 3.339 | 4.710 | 5.116 | 5.633 | 5.502 | 5.796 | 5.116 | 5.633 | 5.502 | 5.796 | ns |
| | | GCLK PLL | $t_{co}$ | 3.729 | 3.729 | 5.286 | 5.749 | 6.321 | 6.163 | 6.545 | 5.749 | 6.321 | 6.163 | 6.545 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.328 | 3.328 | 4.693 | 5.091 | 5.613 | 5.482 | 5.776 | 5.091 | 5.613 | 5.482 | 5.776 | ns |
| | | GCLK PLL | $t_{co}$ | 3.718 | 3.718 | 5.269 | 5.724 | 6.301 | 6.143 | 6.525 | 5.724 | 6.301 | 6.143 | 6.525 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.273 | 3.273 | 4.655 | 5.041 | 5.543 | 5.412 | 5.706 | 5.041 | 5.543 | 5.412 | 5.706 | ns |
| | | GCLK PLL | $t_{co}$ | 3.663 | 3.663 | 5.231 | 5.673 | 6.231 | 6.073 | 6.455 | 5.673 | 6.231 | 6.073 | 6.455 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.268 | 3.268 | 4.639 | 5.029 | 5.532 | 5.401 | 5.695 | 5.029 | 5.532 | 5.401 | 5.695 | ns |
| | | GCLK PLL | $t_{co}$ | 3.658 | 3.658 | 5.214 | 5.662 | 6.220 | 6.062 | 6.444 | 5.662 | 6.220 | 6.062 | 6.444 | ns |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.492 | 3.492 | 5.022 | 5.468 | 6.036 | 5.905 | 6.199 | 5.468 | 6.036 | 5.905 | 6.199 | ns |
| | | GCLK PLL | $t_{co}$ | 3.882 | 3.882 | 5.598 | 6.101 | 6.724 | 6.566 | 6.948 | 6.101 | 6.724 | 6.566 | 6.948 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.369 | 3.369 | 4.797 | 5.207 | 5.750 | 5.619 | 5.913 | 5.207 | 5.750 | 5.619 | 5.913 | ns |
| | | GCLK PLL | $t_{co}$ | 3.759 | 3.759 | 5.372 | 5.839 | 6.438 | 6.280 | 6.662 | 5.839 | 6.438 | 6.280 | 6.662 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.331 | 3.331 | 4.704 | 5.117 | 5.637 | 5.506 | 5.800 | 5.117 | 5.637 | 5.506 | 5.800 | ns |
| | | GCLK PLL | $t_{co}$ | 3.721 | 3.721 | 5.280 | 5.750 | 6.325 | 6.167 | 6.549 | 5.750 | 6.325 | 6.167 | 6.549 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.284 | 3.284 | 4.676 | 5.068 | 5.581 | 5.450 | 5.744 | 5.068 | 5.581 | 5.450 | 5.744 | ns |
| | | GCLK PLL | $t_{co}$ | 3.674 | 3.674 | 5.252 | 5.701 | 6.269 | 6.111 | 6.493 | 5.701 | 6.269 | 6.111 | 6.493 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.284 | 3.284 | 4.633 | 5.016 | 5.512 | 5.381 | 5.675 | 5.016 | 5.512 | 5.381 | 5.675 | ns |
| | | GCLK PLL | $t_{co}$ | 3.674 | 3.674 | 5.209 | 5.648 | 6.200 | 6.042 | 6.424 | 5.648 | 6.200 | 6.042 | 6.424 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.281 | 3.281 | 4.630 | 5.012 | 5.508 | 5.377 | 5.671 | 5.012 | 5.508 | 5.377 | 5.671 | ns |
| | | GCLK PLL | $t_{co}$ | 3.671 | 3.671 | 5.206 | 5.645 | 6.196 | 6.038 | 6.420 | 5.645 | 6.196 | 6.038 | 6.420 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.279 | 3.279 | 4.630 | 5.013 | 5.509 | 5.378 | 5.672 | 5.013 | 5.509 | 5.378 | 5.672 | ns |
| | | GCLK PLL | $t_{co}$ | 3.669 | 3.669 | 5.206 | 5.646 | 6.197 | 6.039 | 6.421 | 5.646 | 6.197 | 6.039 | 6.421 | ns |

**Table 1–63.** EP3SL110 Column Pins Output Timing Parameters (Part 5 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.270 | 3.270 | 4.616 | 4.998 | 5.494 | 5.363 | 5.657 | 4.998 | 5.494 | 5.363 | 5.657 | ns |
| | | GCLK PLL | $t_{co}$ | 3.660 | 3.660 | 5.191 | 5.630 | 6.182 | 6.024 | 6.406 | 5.630 | 6.182 | 6.024 | 6.406 | ns |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.291 | 3.291 | 4.645 | 5.030 | 5.528 | 5.397 | 5.691 | 5.030 | 5.528 | 5.397 | 5.691 | ns |
| | | GCLK PLL | $t_{co}$ | 3.681 | 3.681 | 5.221 | 5.662 | 6.216 | 6.058 | 6.440 | 5.662 | 6.216 | 6.058 | 6.440 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.287 | 3.287 | 4.643 | 5.028 | 5.526 | 5.395 | 5.689 | 5.028 | 5.526 | 5.395 | 5.689 | ns |
| | | GCLK PLL | $t_{co}$ | 3.677 | 3.677 | 5.219 | 5.660 | 6.214 | 6.056 | 6.438 | 5.660 | 6.214 | 6.056 | 6.438 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.276 | 3.276 | 4.633 | 5.018 | 5.517 | 5.386 | 5.680 | 5.018 | 5.517 | 5.386 | 5.680 | ns |
| | | GCLK PLL | $t_{co}$ | 3.666 | 3.666 | 5.209 | 5.651 | 6.205 | 6.047 | 6.429 | 5.651 | 6.205 | 6.047 | 6.429 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.265 | 3.265 | 4.621 | 5.005 | 5.504 | 5.373 | 5.667 | 5.005 | 5.504 | 5.373 | 5.667 | ns |
| | | GCLK PLL | $t_{co}$ | 3.655 | 3.655 | 5.196 | 5.638 | 6.192 | 6.034 | 6.416 | 5.638 | 6.192 | 6.034 | 6.416 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.265 | 3.265 | 4.620 | 5.005 | 5.504 | 5.373 | 5.667 | 5.005 | 5.504 | 5.373 | 5.667 | ns |
| | | GCLK PLL | $t_{co}$ | 3.655 | 3.655 | 5.196 | 5.638 | 6.192 | 6.034 | 6.416 | 5.638 | 6.192 | 6.034 | 6.416 | ns |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.271 | 3.271 | 4.619 | 5.002 | 5.499 | 5.368 | 5.662 | 5.002 | 5.499 | 5.368 | 5.662 | ns |
| | | GCLK PLL | $t_{co}$ | 3.661 | 3.661 | 5.195 | 5.635 | 6.187 | 6.029 | 6.411 | 5.635 | 6.187 | 6.029 | 6.411 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.274 | 3.274 | 4.627 | 5.012 | 5.511 | 5.380 | 5.674 | 5.012 | 5.511 | 5.380 | 5.674 | ns |
| | | GCLK PLL | $t_{co}$ | 3.664 | 3.664 | 5.203 | 5.644 | 6.199 | 6.041 | 6.423 | 5.644 | 6.199 | 6.041 | 6.423 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.295 | 3.295 | 4.655 | 5.041 | 5.541 | 5.410 | 5.704 | 5.041 | 5.541 | 5.410 | 5.704 | ns |
| | | GCLK PLL | $t_{co}$ | 3.685 | 3.685 | 5.230 | 5.674 | 6.229 | 6.071 | 6.453 | 5.674 | 6.229 | 6.071 | 6.453 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.281 | 3.281 | 4.644 | 5.031 | 5.532 | 5.401 | 5.695 | 5.031 | 5.532 | 5.401 | 5.695 | ns |
| | | GCLK PLL | $t_{co}$ | 3.671 | 3.671 | 5.220 | 5.664 | 6.220 | 6.062 | 6.444 | 5.664 | 6.220 | 6.062 | 6.444 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.270 | 3.270 | 4.631 | 5.017 | 5.518 | 5.387 | 5.681 | 5.017 | 5.518 | 5.387 | 5.681 | ns |
| | | GCLK PLL | $t_{co}$ | 3.660 | 3.660 | 5.206 | 5.650 | 6.206 | 6.048 | 6.430 | 5.650 | 6.206 | 6.048 | 6.430 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.269 | 3.269 | 4.634 | 5.021 | 5.522 | 5.391 | 5.685 | 5.021 | 5.522 | 5.391 | 5.685 | ns |
| | | GCLK PLL | $t_{co}$ | 3.659 | 3.659 | 5.209 | 5.653 | 6.210 | 6.052 | 6.434 | 5.653 | 6.210 | 6.052 | 6.434 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.266 | 3.266 | 4.628 | 5.015 | 5.516 | 5.385 | 5.679 | 5.015 | 5.516 | 5.385 | 5.679 | ns |
| | | GCLK PLL | $t_{co}$ | 3.656 | 3.656 | 5.204 | 5.648 | 6.204 | 6.046 | 6.428 | 5.648 | 6.204 | 6.046 | 6.428 | ns |

**Table 1–63.** EP3SL110 Column Pins Output Timing Parameters (Part 6 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-15 CLASS II | 8mA | GCLK | $t_{co}$ | 3.268 | 3.268 | 4.617 | 5.001 | 5.499 | 5.368 | 5.662 | 5.001 | 5.499 | 5.368 | 5.662 | ns |
| | | GCLK PLL | $t_{co}$ | 3.658 | 3.658 | 5.193 | 5.634 | 6.187 | 6.029 | 6.411 | 5.634 | 6.187 | 6.029 | 6.411 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.271 | 3.271 | 4.624 | 5.010 | 5.510 | 5.379 | 5.673 | 5.010 | 5.510 | 5.379 | 5.673 | ns |
| | | GCLK PLL | $t_{co}$ | 3.661 | 3.661 | 5.200 | 5.643 | 6.198 | 6.040 | 6.422 | 5.643 | 6.198 | 6.040 | 6.422 | ns |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.278 | 3.278 | 4.619 | 5.001 | 5.497 | 5.366 | 5.660 | 5.001 | 5.497 | 5.366 | 5.660 | ns |
| | | GCLK PLL | $t_{co}$ | 3.668 | 3.668 | 5.195 | 5.634 | 6.185 | 6.027 | 6.409 | 5.634 | 6.185 | 6.027 | 6.409 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.271 | 3.271 | 4.617 | 5.000 | 5.496 | 5.365 | 5.659 | 5.000 | 5.496 | 5.365 | 5.659 | ns |
| | | GCLK PLL | $t_{co}$ | 3.661 | 3.661 | 5.193 | 5.632 | 6.184 | 6.026 | 6.408 | 5.632 | 6.184 | 6.026 | 6.408 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.263 | 3.263 | 4.610 | 4.992 | 5.489 | 5.358 | 5.652 | 4.992 | 5.489 | 5.358 | 5.652 | ns |
| | | GCLK PLL | $t_{co}$ | 3.653 | 3.653 | 5.185 | 5.625 | 6.177 | 6.019 | 6.401 | 5.625 | 6.177 | 6.019 | 6.401 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.266 | 3.266 | 4.613 | 4.996 | 5.493 | 5.362 | 5.656 | 4.996 | 5.493 | 5.362 | 5.656 | ns |
| | | GCLK PLL | $t_{co}$ | 3.656 | 3.656 | 5.188 | 5.628 | 6.181 | 6.023 | 6.405 | 5.628 | 6.181 | 6.023 | 6.405 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.263 | 3.263 | 4.615 | 4.999 | 5.497 | 5.366 | 5.660 | 4.999 | 5.497 | 5.366 | 5.660 | ns |
| | | GCLK PLL | $t_{co}$ | 3.653 | 3.653 | 5.191 | 5.632 | 6.185 | 6.027 | 6.409 | 5.632 | 6.185 | 6.027 | 6.409 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.271 | 3.271 | 4.614 | 4.997 | 5.493 | 5.362 | 5.656 | 4.997 | 5.493 | 5.362 | 5.656 | ns |
| | | GCLK PLL | $t_{co}$ | 3.661 | 3.661 | 5.190 | 5.629 | 6.181 | 6.023 | 6.405 | 5.629 | 6.181 | 6.023 | 6.405 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.283 | 3.283 | 4.628 | 5.011 | 5.508 | 5.377 | 5.671 | 5.011 | 5.508 | 5.377 | 5.671 | ns |
| | | GCLK PLL | $t_{co}$ | 3.673 | 3.673 | 5.203 | 5.644 | 6.196 | 6.038 | 6.420 | 5.644 | 6.196 | 6.038 | 6.420 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.279 | 3.279 | 4.629 | 5.013 | 5.511 | 5.380 | 5.674 | 5.013 | 5.511 | 5.380 | 5.674 | ns |
| | | GCLK PLL | $t_{co}$ | 3.669 | 3.669 | 5.204 | 5.645 | 6.199 | 6.041 | 6.423 | 5.645 | 6.199 | 6.041 | 6.423 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.275 | 3.275 | 4.624 | 5.008 | 5.506 | 5.375 | 5.669 | 5.008 | 5.506 | 5.375 | 5.669 | ns |
| | | GCLK PLL | $t_{co}$ | 3.665 | 3.665 | 5.200 | 5.641 | 6.194 | 6.036 | 6.418 | 5.641 | 6.194 | 6.036 | 6.418 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.268 | 3.268 | 4.617 | 5.001 | 5.499 | 5.368 | 5.662 | 5.001 | 5.499 | 5.368 | 5.662 | ns |
| | | GCLK PLL | $t_{co}$ | 3.658 | 3.658 | 5.193 | 5.634 | 6.187 | 6.029 | 6.411 | 5.634 | 6.187 | 6.029 | 6.411 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.269 | 3.269 | 4.624 | 5.009 | 5.509 | 5.378 | 5.672 | 5.009 | 5.509 | 5.378 | 5.672 | ns |
| | | GCLK PLL | $t_{co}$ | 3.659 | 3.659 | 5.200 | 5.642 | 6.197 | 6.039 | 6.421 | 5.642 | 6.197 | 6.039 | 6.421 | ns |

**Table 1–63.** EP3SL110 Column Pins Output Timing Parameters (Part 7 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.267 | 3.267 | 4.605 | 4.987 | 5.483 | 5.352 | 5.646 | 4.987 | 5.483 | 5.352 | 5.646 | ns |
| | | GCLK PLL | $t_{co}$ | 3.657 | 3.657 | 5.181 | 5.620 | 6.171 | 6.013 | 6.395 | 5.620 | 6.171 | 6.013 | 6.395 | ns |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.286 | 3.286 | 4.642 | 5.028 | 5.529 | 5.398 | 5.692 | 5.028 | 5.529 | 5.398 | 5.692 | ns |
| | | GCLK PLL | $t_{co}$ | 3.676 | 3.676 | 5.217 | 5.661 | 6.217 | 6.059 | 6.441 | 5.661 | 6.217 | 6.059 | 6.441 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.278 | 3.278 | 4.633 | 5.019 | 5.520 | 5.389 | 5.683 | 5.019 | 5.520 | 5.389 | 5.683 | ns |
| | | GCLK PLL | $t_{co}$ | 3.668 | 3.668 | 5.208 | 5.652 | 6.208 | 6.050 | 6.432 | 5.652 | 6.208 | 6.050 | 6.432 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.279 | 3.279 | 4.640 | 5.028 | 5.529 | 5.398 | 5.692 | 5.028 | 5.529 | 5.398 | 5.692 | ns |
| | | GCLK PLL | $t_{co}$ | 3.669 | 3.669 | 5.216 | 5.660 | 6.217 | 6.059 | 6.441 | 5.660 | 6.217 | 6.059 | 6.441 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.268 | 3.268 | 4.627 | 5.014 | 5.515 | 5.384 | 5.678 | 5.014 | 5.515 | 5.384 | 5.678 | ns |
| | | GCLK PLL | $t_{co}$ | 3.658 | 3.658 | 5.203 | 5.647 | 6.203 | 6.045 | 6.427 | 5.647 | 6.203 | 6.045 | 6.427 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.268 | 3.268 | 4.627 | 5.014 | 5.516 | 5.385 | 5.679 | 5.014 | 5.516 | 5.385 | 5.679 | ns |
| | | GCLK PLL | $t_{co}$ | 3.658 | 3.658 | 5.203 | 5.647 | 6.204 | 6.046 | 6.428 | 5.647 | 6.204 | 6.046 | 6.428 | ns |
| 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.289 | 3.289 | 4.643 | 5.029 | 5.529 | 5.398 | 5.692 | 5.029 | 5.529 | 5.398 | 5.692 | ns |
| | | GCLK PLL | $t_{co}$ | 3.679 | 3.679 | 5.219 | 5.662 | 6.217 | 6.059 | 6.441 | 5.662 | 6.217 | 6.059 | 6.441 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.392 | 3.392 | 4.688 | 5.063 | 5.554 | 5.423 | 5.717 | 5.063 | 5.554 | 5.423 | 5.717 | ns |
| | | GCLK PLL | $t_{co}$ | 3.782 | 3.782 | 5.264 | 5.696 | 6.242 | 6.084 | 6.466 | 5.696 | 6.242 | 6.084 | 6.466 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.392 | 3.392 | 4.688 | 5.063 | 5.554 | 5.423 | 5.717 | 5.063 | 5.554 | 5.423 | 5.717 | ns |
| | | GCLK PLL | $t_{co}$ | 3.782 | 3.782 | 5.264 | 5.696 | 6.242 | 6.084 | 6.466 | 5.696 | 6.242 | 6.084 | 6.466 | ns |

Table 1–64 lists the EP3SL110 row pins output timing parameters for single-ended I/O standards.

**Table 1–64.** EP3SL110 Row Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.182 | 3.481 | 4.833 | 5.216 | 5.678 | 5.579 | 5.814 | 5.256 | 5.802 | 5.703 | 5.896 | ns |
| | | GCLK PLL | $t_{co}$ | 1.457 | 1.650 | 2.051 | 2.136 | 2.329 | 2.349 | 2.337 | 2.239 | 2.435 | 2.454 | 2.331 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.116 | 3.376 | 4.703 | 5.078 | 5.533 | 5.434 | 5.669 | 5.143 | 5.653 | 5.554 | 5.747 | ns |
| | | GCLK PLL | $t_{co}$ | 1.364 | 1.545 | 1.921 | 1.998 | 2.184 | 2.204 | 2.192 | 2.098 | 2.286 | 2.305 | 2.182 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.037 | 3.270 | 4.584 | 4.955 | 5.405 | 5.306 | 5.541 | 5.044 | 5.521 | 5.422 | 5.615 | ns |
| | | GCLK PLL | $t_{co}$ | 1.265 | 1.439 | 1.802 | 1.875 | 2.056 | 2.076 | 2.064 | 1.971 | 2.154 | 2.173 | 2.050 | ns |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.184 | 3.485 | 4.841 | 5.221 | 5.682 | 5.583 | 5.818 | 5.264 | 5.806 | 5.707 | 5.900 | ns |
| | | GCLK PLL | $t_{co}$ | 1.467 | 1.654 | 2.059 | 2.141 | 2.333 | 2.353 | 2.341 | 2.245 | 2.439 | 2.458 | 2.335 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.041 | 3.276 | 4.590 | 4.961 | 5.411 | 5.312 | 5.548 | 5.056 | 5.528 | 5.429 | 5.622 | ns |
| | | GCLK PLL | $t_{co}$ | 1.269 | 1.445 | 1.808 | 1.881 | 2.062 | 2.082 | 2.070 | 1.977 | 2.161 | 2.180 | 2.057 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.143 | 3.427 | 4.785 | 5.169 | 5.634 | 5.535 | 5.770 | 5.224 | 5.760 | 5.661 | 5.854 | ns |
| | | GCLK PLL | $t_{co}$ | 1.411 | 1.596 | 2.003 | 2.089 | 2.285 | 2.305 | 2.293 | 2.196 | 2.393 | 2.412 | 2.289 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.042 | 3.300 | 4.632 | 5.010 | 5.470 | 5.371 | 5.606 | 5.082 | 5.596 | 5.496 | 5.689 | ns |
| | | GCLK PLL | $t_{co}$ | 1.286 | 1.469 | 1.850 | 1.930 | 2.121 | 2.141 | 2.129 | 2.034 | 2.229 | 2.247 | 2.124 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.005 | 3.249 | 4.550 | 4.927 | 5.382 | 5.283 | 5.518 | 5.014 | 5.503 | 5.403 | 5.596 | ns |
| | | GCLK PLL | $t_{co}$ | 1.247 | 1.418 | 1.768 | 1.847 | 2.033 | 2.053 | 2.041 | 1.948 | 2.136 | 2.154 | 2.031 | ns |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.064 | 3.346 | 4.679 | 5.062 | 5.524 | 5.425 | 5.660 | 5.115 | 5.649 | 5.549 | 5.742 | ns |
| | | GCLK PLL | $t_{co}$ | 1.325 | 1.515 | 1.897 | 1.982 | 2.175 | 2.195 | 2.183 | 2.088 | 2.282 | 2.300 | 2.177 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.992 | 3.227 | 4.515 | 4.888 | 5.343 | 5.244 | 5.479 | 4.984 | 5.463 | 5.363 | 5.556 | ns |
| | | GCLK PLL | $t_{co}$ | 1.225 | 1.396 | 1.733 | 1.808 | 1.994 | 2.014 | 2.002 | 1.908 | 2.096 | 2.114 | 1.991 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.169 | 3.463 | 4.917 | 5.323 | 5.806 | 5.707 | 5.942 | 5.356 | 5.939 | 5.839 | 6.032 | ns |
| | | GCLK PLL | $t_{co}$ | 1.437 | 1.632 | 2.135 | 2.243 | 2.457 | 2.477 | 2.465 | 2.356 | 2.572 | 2.590 | 2.467 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.084 | 3.365 | 4.762 | 5.160 | 5.636 | 5.537 | 5.772 | 5.219 | 5.765 | 5.665 | 5.858 | ns |
| | | GCLK PLL | $t_{co}$ | 1.327 | 1.534 | 1.980 | 2.080 | 2.287 | 2.307 | 2.295 | 2.189 | 2.398 | 2.416 | 2.293 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.027 | 3.288 | 4.651 | 5.041 | 5.510 | 5.411 | 5.646 | 5.130 | 5.635 | 5.535 | 5.728 | ns |
| | | GCLK PLL | $t_{co}$ | 1.281 | 1.457 | 1.869 | 1.961 | 2.161 | 2.181 | 2.169 | 2.066 | 2.268 | 2.286 | 2.163 | ns |

**Table 1–64.** EP3SL110 Row Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.438 | 3.706 | 5.298 | 5.747 | 6.303 | 6.177 | 6.439 | 5.888 | 6.445 | 6.318 | 6.538 | ns |
| | | GCLK PLL | $t_{co}$ | 1.670 | 1.879 | 2.521 | 2.672 | 2.932 | 2.952 | 2.937 | 2.793 | 3.056 | 3.075 | 2.949 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.213 | 3.504 | 4.971 | 5.378 | 5.898 | 5.772 | 6.034 | 5.523 | 6.039 | 5.911 | 6.131 | ns |
| | | GCLK PLL | $t_{co}$ | 1.445 | 1.677 | 2.194 | 2.303 | 2.527 | 2.547 | 2.532 | 2.428 | 2.650 | 2.668 | 2.542 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.148 | 3.402 | 4.818 | 5.228 | 5.739 | 5.613 | 5.875 | 5.355 | 5.866 | 5.739 | 5.959 | ns |
| | | GCLK PLL | $t_{co}$ | 1.380 | 1.575 | 2.041 | 2.153 | 2.368 | 2.388 | 2.373 | 2.260 | 2.477 | 2.496 | 2.370 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.088 | 3.328 | 4.741 | 5.134 | 5.642 | 5.516 | 5.778 | 5.260 | 5.772 | 5.645 | 5.865 | ns |
| | | GCLK PLL | $t_{co}$ | 1.320 | 1.501 | 1.964 | 2.059 | 2.271 | 2.291 | 2.276 | 2.165 | 2.383 | 2.402 | 2.276 | ns |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.349 | 3.624 | 5.208 | 5.660 | 6.231 | 6.105 | 6.367 | 5.795 | 6.369 | 6.242 | 6.462 | ns |
| | | GCLK PLL | $t_{co}$ | 1.581 | 1.797 | 2.431 | 2.585 | 2.860 | 2.880 | 2.865 | 2.700 | 2.980 | 2.999 | 2.873 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.107 | 3.366 | 4.803 | 5.223 | 5.740 | 5.614 | 5.876 | 5.349 | 5.865 | 5.738 | 5.958 | ns |
| | | GCLK PLL | $t_{co}$ | 1.339 | 1.539 | 2.026 | 2.148 | 2.369 | 2.389 | 2.374 | 2.254 | 2.476 | 2.495 | 2.369 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.080 | 3.319 | 4.730 | 5.127 | 5.634 | 5.508 | 5.770 | 5.251 | 5.760 | 5.633 | 5.853 | ns |
| | | GCLK PLL | $t_{co}$ | 1.312 | 1.492 | 1.953 | 2.052 | 2.263 | 2.283 | 2.268 | 2.156 | 2.371 | 2.390 | 2.264 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.071 | 3.310 | 4.708 | 5.109 | 5.615 | 5.489 | 5.751 | 5.233 | 5.738 | 5.611 | 5.831 | ns |
| | | GCLK PLL | $t_{co}$ | 1.303 | 1.483 | 1.931 | 2.034 | 2.244 | 2.264 | 2.249 | 2.138 | 2.349 | 2.368 | 2.242 | ns |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.292 | 3.549 | 5.118 | 5.574 | 6.156 | 6.030 | 6.292 | 5.707 | 6.285 | 6.158 | 6.378 | ns |
| | | GCLK PLL | $t_{co}$ | 1.524 | 1.722 | 2.341 | 2.499 | 2.785 | 2.805 | 2.790 | 2.612 | 2.896 | 2.915 | 2.789 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.112 | 3.360 | 4.825 | 5.251 | 5.781 | 5.655 | 5.917 | 5.374 | 5.907 | 5.780 | 6.000 | ns |
| | | GCLK PLL | $t_{co}$ | 1.344 | 1.533 | 2.048 | 2.176 | 2.410 | 2.430 | 2.415 | 2.279 | 2.518 | 2.537 | 2.411 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.031 | 3.274 | 4.629 | 5.013 | 5.478 | 5.379 | 5.616 | 5.117 | 5.597 | 5.498 | 5.692 | ns |
| | | GCLK PLL | $t_{co}$ | 1.266 | 1.443 | 1.847 | 1.933 | 2.129 | 2.149 | 2.137 | 2.033 | 2.230 | 2.249 | 2.126 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.026 | 3.262 | 4.621 | 5.005 | 5.476 | 5.371 | 5.614 | 5.116 | 5.596 | 5.491 | 5.691 | ns |
| | | GCLK PLL | $t_{co}$ | 1.254 | 1.431 | 1.839 | 1.925 | 2.121 | 2.141 | 2.129 | 2.025 | 2.223 | 2.242 | 2.119 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.017 | 3.244 | 4.596 | 4.980 | 5.459 | 5.344 | 5.597 | 5.099 | 5.578 | 5.464 | 5.673 | ns |
| | | GCLK PLL | $t_{co}$ | 1.238 | 1.413 | 1.814 | 1.900 | 2.094 | 2.114 | 2.102 | 1.999 | 2.196 | 2.215 | 2.092 | ns |

**Table 1–64.** EP3SL110 Row Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.049 | 3.284 | 4.636 | 5.022 | 5.516 | 5.390 | 5.652 | 5.141 | 5.635 | 5.508 | 5.728 | ns |
| | | GCLK PLL | $t_{co}$ | 1.281 | 1.457 | 1.859 | 1.947 | 2.145 | 2.165 | 2.150 | 2.046 | 2.246 | 2.265 | 2.139 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.034 | 3.270 | 4.633 | 5.020 | 5.514 | 5.388 | 5.650 | 5.139 | 5.633 | 5.506 | 5.726 | ns |
| | | GCLK PLL | $t_{co}$ | 1.266 | 1.443 | 1.856 | 1.945 | 2.143 | 2.163 | 2.148 | 2.044 | 2.244 | 2.263 | 2.137 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.023 | 3.258 | 4.616 | 5.003 | 5.497 | 5.371 | 5.633 | 5.122 | 5.617 | 5.490 | 5.710 | ns |
| | | GCLK PLL | $t_{co}$ | 1.255 | 1.431 | 1.839 | 1.928 | 2.126 | 2.146 | 2.131 | 2.027 | 2.228 | 2.247 | 2.121 | ns |
| | 10mA | GCLK | $t_{co}$ | 2.999 | 3.235 | 4.600 | 4.987 | 5.482 | 5.356 | 5.618 | 5.107 | 5.602 | 5.475 | 5.695 | ns |
| | | GCLK PLL | $t_{co}$ | 1.231 | 1.408 | 1.823 | 1.912 | 2.111 | 2.131 | 2.116 | 2.012 | 2.213 | 2.232 | 2.106 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.999 | 3.234 | 4.599 | 4.986 | 5.481 | 5.355 | 5.617 | 5.106 | 5.601 | 5.474 | 5.694 | ns |
| | | GCLK PLL | $t_{co}$ | 1.231 | 1.407 | 1.822 | 1.911 | 2.110 | 2.130 | 2.116 | 2.011 | 2.212 | 2.231 | 2.106 | ns |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.009 | 3.243 | 4.597 | 4.982 | 5.475 | 5.349 | 5.611 | 5.101 | 5.594 | 5.467 | 5.687 | ns |
| | | GCLK PLL | $t_{co}$ | 1.241 | 1.416 | 1.820 | 1.907 | 2.104 | 2.124 | 2.111 | 2.006 | 2.205 | 2.224 | 2.100 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.004 | 3.238 | 4.596 | 4.983 | 5.477 | 5.351 | 5.613 | 5.103 | 5.598 | 5.471 | 5.691 | ns |
| | | GCLK PLL | $t_{co}$ | 1.235 | 1.411 | 1.819 | 1.908 | 2.106 | 2.126 | 2.121 | 2.008 | 2.209 | 2.228 | 2.111 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.045 | 3.280 | 4.647 | 5.036 | 5.533 | 5.407 | 5.669 | 5.154 | 5.651 | 5.524 | 5.744 | ns |
| | | GCLK PLL | $t_{co}$ | 1.277 | 1.453 | 1.870 | 1.961 | 2.162 | 2.182 | 2.167 | 2.059 | 2.262 | 2.281 | 2.155 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.022 | 3.258 | 4.629 | 5.019 | 5.516 | 5.390 | 5.652 | 5.138 | 5.635 | 5.508 | 5.728 | ns |
| | | GCLK PLL | $t_{co}$ | 1.254 | 1.431 | 1.852 | 1.944 | 2.145 | 2.165 | 2.150 | 2.043 | 2.246 | 2.265 | 2.139 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.005 | 3.241 | 4.612 | 5.001 | 5.498 | 5.372 | 5.634 | 5.120 | 5.618 | 5.491 | 5.711 | ns |
| | | GCLK PLL | $t_{co}$ | 1.237 | 1.414 | 1.835 | 1.926 | 2.127 | 2.147 | 2.132 | 2.025 | 2.229 | 2.248 | 2.122 | ns |

**Table 1–64.** EP3SL110 Row Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.024 | 3.256 | 4.603 | 4.987 | 5.478 | 5.352 | 5.614 | 5.105 | 5.597 | 5.470 | 5.690 | ns |
| | | GCLK PLL | $t_{co}$ | 1.256 | 1.429 | 1.826 | 1.912 | 2.107 | 2.127 | 2.112 | 2.010 | 2.208 | 2.227 | 2.101 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.012 | 3.244 | 4.594 | 4.979 | 5.470 | 5.344 | 5.606 | 5.097 | 5.590 | 5.463 | 5.683 | ns |
| | | GCLK PLL | $t_{co}$ | 1.244 | 1.417 | 1.817 | 1.904 | 2.099 | 2.119 | 2.108 | 2.002 | 2.201 | 2.220 | 2.097 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.999 | 3.232 | 4.585 | 4.970 | 5.462 | 5.336 | 5.598 | 5.089 | 5.582 | 5.455 | 5.675 | ns |
| | | GCLK PLL | $t_{co}$ | 1.231 | 1.405 | 1.808 | 1.895 | 2.091 | 2.111 | 2.101 | 1.994 | 2.193 | 2.212 | 2.090 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.001 | 3.234 | 4.588 | 4.973 | 5.465 | 5.339 | 5.601 | 5.092 | 5.585 | 5.458 | 5.678 | ns |
| | | GCLK PLL | $t_{co}$ | 1.233 | 1.407 | 1.811 | 1.898 | 2.094 | 2.114 | 2.105 | 1.997 | 2.196 | 2.215 | 2.093 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.994 | 3.229 | 4.586 | 4.972 | 5.465 | 5.339 | 5.601 | 5.092 | 5.586 | 5.459 | 5.679 | ns |
| | | GCLK PLL | $t_{co}$ | 1.226 | 1.402 | 1.809 | 1.897 | 2.094 | 2.114 | 2.108 | 1.997 | 2.197 | 2.216 | 2.098 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.001 | 3.234 | 4.581 | 4.964 | 5.457 | 5.330 | 5.595 | 5.083 | 5.575 | 5.448 | 5.670 | ns |
| | | GCLK PLL | $t_{co}$ | 1.232 | 1.406 | 1.804 | 1.889 | 2.085 | 2.105 | 2.104 | 1.988 | 2.186 | 2.205 | 2.092 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.031 | 3.263 | 4.614 | 5.000 | 5.493 | 5.367 | 5.629 | 5.117 | 5.611 | 5.484 | 5.704 | ns |
| | | GCLK PLL | $t_{co}$ | 1.263 | 1.436 | 1.837 | 1.925 | 2.122 | 2.142 | 2.127 | 2.022 | 2.222 | 2.241 | 2.115 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.019 | 3.253 | 4.610 | 4.996 | 5.489 | 5.363 | 5.625 | 5.114 | 5.608 | 5.481 | 5.701 | ns |
| | | GCLK PLL | $t_{co}$ | 1.251 | 1.426 | 1.833 | 1.921 | 2.118 | 2.138 | 2.123 | 2.019 | 2.219 | 2.238 | 2.112 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.015 | 3.248 | 4.604 | 4.990 | 5.483 | 5.357 | 5.619 | 5.108 | 5.602 | 5.475 | 5.695 | ns |
| | | GCLK PLL | $t_{co}$ | 1.247 | 1.421 | 1.827 | 1.915 | 2.112 | 2.132 | 2.117 | 2.013 | 2.213 | 2.232 | 2.106 | ns |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.030 | 3.262 | 4.625 | 5.014 | 5.511 | 5.385 | 5.647 | 5.131 | 5.628 | 5.501 | 5.721 | ns |
| | | GCLK PLL | $t_{co}$ | 1.262 | 1.435 | 1.848 | 1.939 | 2.140 | 2.160 | 2.145 | 2.036 | 2.239 | 2.258 | 2.132 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.018 | 3.250 | 4.614 | 5.002 | 5.499 | 5.373 | 5.635 | 5.120 | 5.617 | 5.490 | 5.710 | ns |
| | | GCLK PLL | $t_{co}$ | 1.250 | 1.423 | 1.837 | 1.927 | 2.128 | 2.148 | 2.133 | 2.025 | 2.228 | 2.247 | 2.121 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.014 | 3.248 | 4.618 | 5.007 | 5.505 | 5.379 | 5.641 | 5.126 | 5.624 | 5.497 | 5.717 | ns |
| | | GCLK PLL | $t_{co}$ | 1.246 | 1.421 | 1.841 | 1.932 | 2.134 | 2.154 | 2.139 | 2.031 | 2.235 | 2.254 | 2.128 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.137 | 3.357 | 4.654 | 5.031 | 5.518 | 5.390 | 5.656 | 5.165 | 5.639 | 5.511 | 5.734 | ns |
| | | GCLK PLL | $t_{co}$ | 1.351 | 1.526 | 1.872 | 1.951 | 2.138 | 2.158 | 2.146 | 2.051 | 2.242 | 2.261 | 2.138 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.137 | 3.357 | 4.654 | 5.031 | 5.518 | 5.390 | 5.656 | 5.165 | 5.639 | 5.511 | 5.734 | ns |
| | | GCLK PLL | $t_{co}$ | 1.351 | 1.526 | 1.872 | 1.951 | 2.138 | 2.158 | 2.146 | 2.051 | 2.242 | 2.261 | 2.138 | ns |


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Table 1–65 through Table 1–70 list the maximum I/O timing parameters for EP3SL110 devices for differential I/O standards.

Table 1–65 lists the EP3SL110 column pins input timing parameters for differential I/O standards.

**Table 1–65.** EP3SL110 Column Pins Input Timing Parameters (Part 1 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -0.978 | -1.006 | -1.151 | -1.135 | -1.286 | -1.233 | -1.594 | -1.098 | -1.339 | -1.193 | -1.632 | ns |
| | | $t_h$ | 1.104 | 1.152 | 1.371 | 1.387 | 1.564 | 1.502 | 1.860 | 1.361 | 1.634 | 1.471 | 1.898 | ns |
| | GCLK PLL | $t_{su}$ | 0.967 | 1.001 | 1.885 | 2.230 | 2.404 | 2.293 | 2.197 | 2.284 | 2.556 | 2.353 | 2.249 | ns |
| | | $t_h$ | -0.707 | -0.719 | -1.450 | -1.735 | -1.855 | -1.769 | -1.669 | -1.780 | -1.984 | -1.818 | -1.718 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -0.978 | -1.006 | -1.151 | -1.135 | -1.286 | -1.233 | -1.594 | -1.098 | -1.339 | -1.193 | -1.632 | ns |
| | | $t_h$ | 1.104 | 1.152 | 1.371 | 1.387 | 1.564 | 1.502 | 1.860 | 1.361 | 1.634 | 1.471 | 1.898 | ns |
| | GCLK PLL | $t_{su}$ | 0.967 | 1.001 | 1.885 | 2.230 | 2.404 | 2.293 | 2.197 | 2.284 | 2.556 | 2.353 | 2.249 | ns |
| | | $t_h$ | -0.707 | -0.719 | -1.450 | -1.735 | -1.855 | -1.769 | -1.669 | -1.780 | -1.984 | -1.818 | -1.718 | ns |
| RSDS | GCLK | $t_{su}$ | -0.978 | -1.006 | -1.151 | -1.135 | -1.286 | -1.233 | -1.594 | -1.098 | -1.339 | -1.193 | -1.632 | ns |
| | | $t_h$ | 1.104 | 1.152 | 1.371 | 1.387 | 1.564 | 1.502 | 1.860 | 1.361 | 1.634 | 1.471 | 1.898 | ns |
| | GCLK PLL | $t_{su}$ | 0.967 | 1.001 | 1.885 | 2.230 | 2.404 | 2.293 | 2.197 | 2.284 | 2.556 | 2.353 | 2.249 | ns |
| | | $t_h$ | -0.707 | -0.719 | -1.450 | -1.735 | -1.855 | -1.769 | -1.669 | -1.780 | -1.984 | -1.818 | -1.718 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.794 | -0.829 | -1.228 | -1.334 | -1.445 | -1.387 | -1.743 | -1.333 | -1.443 | -1.391 | -1.786 | ns |
| | | $t_h$ | 0.913 | 0.967 | 1.416 | 1.546 | 1.677 | 1.610 | 1.964 | 1.554 | 1.684 | 1.621 | 2.007 | ns |
| | GCLK PLL | $t_{su}$ | 1.151 | 1.178 | 1.808 | 2.031 | 2.245 | 2.139 | 2.048 | 2.049 | 2.266 | 2.155 | 2.095 | ns |
| | | $t_h$ | -0.898 | -0.904 | -1.405 | -1.576 | -1.742 | -1.661 | -1.565 | -1.587 | -1.753 | -1.668 | -1.609 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.794 | -0.829 | -1.228 | -1.334 | -1.445 | -1.387 | -1.743 | -1.333 | -1.443 | -1.391 | -1.786 | ns |
| | | $t_h$ | 0.913 | 0.967 | 1.416 | 1.546 | 1.677 | 1.610 | 1.964 | 1.554 | 1.684 | 1.621 | 2.007 | ns |
| | GCLK PLL | $t_{su}$ | 1.151 | 1.178 | 1.808 | 2.031 | 2.245 | 2.139 | 2.048 | 2.049 | 2.266 | 2.155 | 2.095 | ns |
| | | $t_h$ | -0.898 | -0.904 | -1.405 | -1.576 | -1.742 | -1.661 | -1.565 | -1.587 | -1.753 | -1.668 | -1.609 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.802 | -0.841 | -1.238 | -1.345 | -1.461 | -1.403 | -1.759 | -1.344 | -1.458 | -1.406 | -1.801 | ns |
| | | $t_h$ | 0.921 | 0.979 | 1.426 | 1.557 | 1.693 | 1.626 | 1.980 | 1.565 | 1.699 | 1.636 | 2.022 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.166 | 1.798 | 2.020 | 2.229 | 2.123 | 2.032 | 2.038 | 2.251 | 2.140 | 2.080 | ns |
| | | $t_h$ | -0.890 | -0.892 | -1.395 | -1.565 | -1.726 | -1.645 | -1.549 | -1.576 | -1.738 | -1.653 | -1.594 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.802 | -0.841 | -1.238 | -1.345 | -1.461 | -1.403 | -1.759 | -1.344 | -1.458 | -1.406 | -1.801 | ns |
| | | $t_h$ | 0.921 | 0.979 | 1.426 | 1.557 | 1.693 | 1.626 | 1.980 | 1.565 | 1.699 | 1.636 | 2.022 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.166 | 1.798 | 2.020 | 2.229 | 2.123 | 2.032 | 2.038 | 2.251 | 2.140 | 2.080 | ns |
| | | $t_h$ | -0.890 | -0.892 | -1.395 | -1.565 | -1.726 | -1.645 | -1.549 | -1.576 | -1.738 | -1.653 | -1.594 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.814 | -0.852 | -1.247 | -1.356 | -1.480 | -1.422 | -1.778 | -1.355 | -1.476 | -1.424 | -1.819 | ns |
| | | $t_h$ | 0.933 | 0.990 | 1.436 | 1.568 | 1.712 | 1.645 | 1.999 | 1.576 | 1.717 | 1.654 | 2.040 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.155 | 1.789 | 2.009 | 2.210 | 2.104 | 2.013 | 2.027 | 2.233 | 2.122 | 2.062 | ns |
| | | $t_h$ | -0.878 | -0.881 | -1.385 | -1.554 | -1.707 | -1.626 | -1.530 | -1.565 | -1.720 | -1.635 | -1.576 | ns |

**Table 1–65.** EP3SL110 Column Pins Input Timing Parameters (Part 2 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.814 | -0.852 | -1.247 | -1.356 | -1.480 | -1.422 | -1.778 | -1.355 | -1.476 | -1.424 | -1.819 | ns |
| | | $t_h$ | 0.933 | 0.990 | 1.436 | 1.568 | 1.712 | 1.645 | 1.999 | 1.576 | 1.717 | 1.654 | 2.040 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.155 | 1.789 | 2.009 | 2.210 | 2.104 | 2.013 | 2.027 | 2.233 | 2.122 | 2.062 | ns |
| | | $t_h$ | -0.878 | -0.881 | -1.385 | -1.554 | -1.707 | -1.626 | -1.530 | -1.565 | -1.720 | -1.635 | -1.576 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.802 | -0.841 | -1.238 | -1.345 | -1.461 | -1.403 | -1.759 | -1.344 | -1.458 | -1.406 | -1.801 | ns |
| | | $t_h$ | 0.921 | 0.979 | 1.426 | 1.557 | 1.693 | 1.626 | 1.980 | 1.565 | 1.699 | 1.636 | 2.022 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.166 | 1.798 | 2.020 | 2.229 | 2.123 | 2.032 | 2.038 | 2.251 | 2.140 | 2.080 | ns |
| | | $t_h$ | -0.890 | -0.892 | -1.395 | -1.565 | -1.726 | -1.645 | -1.549 | -1.576 | -1.738 | -1.653 | -1.594 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.802 | -0.841 | -1.238 | -1.345 | -1.461 | -1.403 | -1.759 | -1.344 | -1.458 | -1.406 | -1.801 | ns |
| | | $t_h$ | 0.921 | 0.979 | 1.426 | 1.557 | 1.693 | 1.626 | 1.980 | 1.565 | 1.699 | 1.636 | 2.022 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.166 | 1.798 | 2.020 | 2.229 | 2.123 | 2.032 | 2.038 | 2.251 | 2.140 | 2.080 | ns |
| | | $t_h$ | -0.890 | -0.892 | -1.395 | -1.565 | -1.726 | -1.645 | -1.549 | -1.576 | -1.738 | -1.653 | -1.594 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -0.814 | -0.852 | -1.247 | -1.356 | -1.480 | -1.422 | -1.778 | -1.355 | -1.476 | -1.424 | -1.819 | ns |
| | | $t_h$ | 0.933 | 0.990 | 1.436 | 1.568 | 1.712 | 1.645 | 1.999 | 1.576 | 1.717 | 1.654 | 2.040 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.155 | 1.789 | 2.009 | 2.210 | 2.104 | 2.013 | 2.027 | 2.233 | 2.122 | 2.062 | ns |
| | | $t_h$ | -0.878 | -0.881 | -1.385 | -1.554 | -1.707 | -1.626 | -1.530 | -1.565 | -1.720 | -1.635 | -1.576 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -0.814 | -0.852 | -1.247 | -1.356 | -1.480 | -1.422 | -1.778 | -1.355 | -1.476 | -1.424 | -1.819 | ns |
| | | $t_h$ | 0.933 | 0.990 | 1.436 | 1.568 | 1.712 | 1.645 | 1.999 | 1.576 | 1.717 | 1.654 | 2.040 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.155 | 1.789 | 2.009 | 2.210 | 2.104 | 2.013 | 2.027 | 2.233 | 2.122 | 2.062 | ns |
| | | $t_h$ | -0.878 | -0.881 | -1.385 | -1.554 | -1.707 | -1.626 | -1.530 | -1.565 | -1.720 | -1.635 | -1.576 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.821 | -0.858 | -1.259 | -1.361 | -1.480 | -1.424 | -1.777 | -1.359 | -1.471 | -1.422 | -1.815 | ns |
| | | $t_h$ | 0.940 | 0.996 | 1.449 | 1.576 | 1.715 | 1.648 | 2.003 | 1.583 | 1.717 | 1.653 | 2.041 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.149 | 1.777 | 2.004 | 2.210 | 2.102 | 2.014 | 2.023 | 2.238 | 2.124 | 2.066 | ns |
| | | $t_h$ | -0.871 | -0.875 | -1.372 | -1.546 | -1.704 | -1.623 | -1.526 | -1.558 | -1.720 | -1.636 | -1.575 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.821 | -0.858 | -1.259 | -1.361 | -1.480 | -1.424 | -1.777 | -1.359 | -1.471 | -1.422 | -1.815 | ns |
| | | $t_h$ | 0.940 | 0.996 | 1.449 | 1.576 | 1.715 | 1.648 | 2.003 | 1.583 | 1.717 | 1.653 | 2.041 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.149 | 1.777 | 2.004 | 2.210 | 2.102 | 2.014 | 2.023 | 2.238 | 2.124 | 2.066 | ns |
| | | $t_h$ | -0.871 | -0.875 | -1.372 | -1.546 | -1.704 | -1.623 | -1.526 | -1.558 | -1.720 | -1.636 | -1.575 | ns |

Table 1–66 lists the EP3SL110 parameters for differential I/O standards.

**Table 1–66.** EP3SL110 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -0.919 | -0.950 | -1.021 | -0.981 | -1.115 | -1.070 | -1.404 | -0.940 | -1.066 | -1.023 | -1.442 | ns |
| | | $t_h$ | 1.043 | 1.092 | 1.245 | 1.237 | 1.395 | 1.339 | 1.672 | 1.207 | 1.358 | 1.303 | 1.711 | ns |
| | GCLK PLL | $t_{su}$ | 0.959 | 0.987 | 1.949 | 2.324 | 2.527 | 2.403 | 2.334 | 2.384 | 2.597 | 2.470 | 2.387 | ns |
| | | $t_h$ | -0.698 | -0.708 | -1.513 | -1.828 | -1.977 | -1.881 | -1.804 | -1.875 | -2.032 | -1.933 | -1.853 | ns |


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**Table 1–66.** EP3SL110 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| MINI-LVDS | GCLK | $t_{su}$ | -0.919 | -0.950 | -1.021 | -0.981 | -1.115 | -1.070 | -1.404 | -0.940 | -1.066 | -1.023 | -1.442 | ns |
| | | $t_h$ | 1.043 | 1.092 | 1.245 | 1.237 | 1.395 | 1.339 | 1.672 | 1.207 | 1.358 | 1.303 | 1.711 | ns |
| | GCLK PLL | $t_{su}$ | 0.959 | 0.987 | 1.949 | 2.324 | 2.527 | 2.403 | 2.334 | 2.384 | 2.597 | 2.470 | 2.387 | ns |
| | | $t_h$ | -0.698 | -0.708 | -1.513 | -1.828 | -1.977 | -1.881 | -1.804 | -1.875 | -2.032 | -1.933 | -1.853 | ns |
| RSDS | GCLK | $t_{su}$ | -0.919 | -0.950 | -1.021 | -0.981 | -1.115 | -1.070 | -1.404 | -0.940 | -1.066 | -1.023 | -1.442 | ns |
| | | $t_h$ | 1.043 | 1.092 | 1.245 | 1.237 | 1.395 | 1.339 | 1.672 | 1.207 | 1.358 | 1.303 | 1.711 | ns |
| | GCLK PLL | $t_{su}$ | 0.959 | 0.987 | 1.949 | 2.324 | 2.527 | 2.403 | 2.334 | 2.384 | 2.597 | 2.470 | 2.387 | ns |
| | | $t_h$ | -0.698 | -0.708 | -1.513 | -1.828 | -1.977 | -1.881 | -1.804 | -1.875 | -2.032 | -1.933 | -1.853 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.724 | -0.765 | -1.113 | -1.210 | -1.304 | -1.254 | -1.583 | -1.211 | -1.303 | -1.255 | -1.626 | ns |
| | | $t_h$ | 0.841 | 0.898 | 1.302 | 1.420 | 1.535 | 1.474 | 1.802 | 1.429 | 1.543 | 1.483 | 1.846 | ns |
| | GCLK PLL | $t_{su}$ | 1.154 | 1.172 | 1.862 | 2.100 | 2.338 | 2.219 | 2.155 | 2.117 | 2.360 | 2.238 | 2.203 | ns |
| | | $t_h$ | -0.900 | -0.902 | -1.458 | -1.649 | -1.837 | -1.746 | -1.674 | -1.657 | -1.847 | -1.753 | -1.718 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.724 | -0.765 | -1.113 | -1.210 | -1.304 | -1.254 | -1.583 | -1.211 | -1.303 | -1.255 | -1.626 | ns |
| | | $t_h$ | 0.841 | 0.898 | 1.302 | 1.420 | 1.535 | 1.474 | 1.802 | 1.429 | 1.543 | 1.483 | 1.846 | ns |
| | GCLK PLL | $t_{su}$ | 1.154 | 1.172 | 1.862 | 2.100 | 2.338 | 2.219 | 2.155 | 2.117 | 2.360 | 2.238 | 2.203 | ns |
| | | $t_h$ | -0.900 | -0.902 | -1.458 | -1.649 | -1.837 | -1.746 | -1.674 | -1.657 | -1.847 | -1.753 | -1.718 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.733 | -0.777 | -1.122 | -1.220 | -1.320 | -1.270 | -1.599 | -1.220 | -1.319 | -1.271 | -1.642 | ns |
| | | $t_h$ | 0.850 | 0.910 | 1.311 | 1.430 | 1.551 | 1.490 | 1.818 | 1.438 | 1.559 | 1.499 | 1.862 | ns |
| | GCLK PLL | $t_{su}$ | 1.145 | 1.160 | 1.853 | 2.090 | 2.322 | 2.203 | 2.139 | 2.108 | 2.344 | 2.222 | 2.187 | ns |
| | | $t_h$ | -0.891 | -0.890 | -1.449 | -1.639 | -1.821 | -1.730 | -1.658 | -1.648 | -1.831 | -1.737 | -1.702 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.733 | -0.777 | -1.122 | -1.220 | -1.320 | -1.270 | -1.599 | -1.220 | -1.319 | -1.271 | -1.642 | ns |
| | | $t_h$ | 0.850 | 0.910 | 1.311 | 1.430 | 1.551 | 1.490 | 1.818 | 1.438 | 1.559 | 1.499 | 1.862 | ns |
| | GCLK PLL | $t_{su}$ | 1.145 | 1.160 | 1.853 | 2.090 | 2.322 | 2.203 | 2.139 | 2.108 | 2.344 | 2.222 | 2.187 | ns |
| | | $t_h$ | -0.891 | -0.890 | -1.449 | -1.639 | -1.821 | -1.730 | -1.658 | -1.648 | -1.831 | -1.737 | -1.702 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.747 | -0.789 | -1.131 | -1.230 | -1.338 | -1.288 | -1.617 | -1.231 | -1.336 | -1.288 | -1.659 | ns |
| | | $t_h$ | 0.864 | 0.922 | 1.321 | 1.440 | 1.569 | 1.508 | 1.836 | 1.449 | 1.576 | 1.516 | 1.879 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.148 | 1.840 | 2.080 | 2.304 | 2.185 | 2.121 | 2.097 | 2.327 | 2.205 | 2.170 | ns |
| | | $t_h$ | -0.877 | -0.878 | -1.437 | -1.629 | -1.803 | -1.712 | -1.640 | -1.637 | -1.814 | -1.720 | -1.685 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.747 | -0.789 | -1.131 | -1.230 | -1.338 | -1.288 | -1.617 | -1.231 | -1.336 | -1.288 | -1.659 | ns |
| | | $t_h$ | 0.864 | 0.922 | 1.321 | 1.440 | 1.569 | 1.508 | 1.836 | 1.449 | 1.576 | 1.516 | 1.879 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.148 | 1.840 | 2.080 | 2.304 | 2.185 | 2.121 | 2.097 | 2.327 | 2.205 | 2.170 | ns |
| | | $t_h$ | -0.877 | -0.878 | -1.437 | -1.629 | -1.803 | -1.712 | -1.640 | -1.637 | -1.814 | -1.720 | -1.685 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.733 | -0.777 | -1.122 | -1.220 | -1.320 | -1.270 | -1.599 | -1.220 | -1.319 | -1.271 | -1.642 | ns |
| | | $t_h$ | 0.850 | 0.910 | 1.311 | 1.430 | 1.551 | 1.490 | 1.818 | 1.438 | 1.559 | 1.499 | 1.862 | ns |
| | GCLK PLL | $t_{su}$ | 1.145 | 1.160 | 1.853 | 2.090 | 2.322 | 2.203 | 2.139 | 2.108 | 2.344 | 2.222 | 2.187 | ns |
| | | $t_h$ | -0.891 | -0.890 | -1.449 | -1.639 | -1.821 | -1.730 | -1.658 | -1.648 | -1.831 | -1.737 | -1.702 | ns |

**Table 1–66.** EP3SL110 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.733 | -0.777 | -1.122 | -1.220 | -1.320 | -1.270 | -1.599 | -1.220 | -1.319 | -1.271 | -1.642 | ns |
| | | $t_h$ | 0.850 | 0.910 | 1.311 | 1.430 | 1.551 | 1.490 | 1.818 | 1.438 | 1.559 | 1.499 | 1.862 | ns |
| | GCLK PLL | $t_{su}$ | 1.145 | 1.160 | 1.853 | 2.090 | 2.322 | 2.203 | 2.139 | 2.108 | 2.344 | 2.222 | 2.187 | ns |
| | | $t_h$ | -0.891 | -0.890 | -1.449 | -1.639 | -1.821 | -1.730 | -1.658 | -1.648 | -1.831 | -1.737 | -1.702 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -0.747 | -0.789 | -1.131 | -1.230 | -1.338 | -1.288 | -1.617 | -1.231 | -1.336 | -1.288 | -1.659 | ns |
| | | $t_h$ | 0.864 | 0.922 | 1.321 | 1.440 | 1.569 | 1.508 | 1.836 | 1.449 | 1.576 | 1.516 | 1.879 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.148 | 1.840 | 2.080 | 2.304 | 2.185 | 2.121 | 2.097 | 2.327 | 2.205 | 2.170 | ns |
| | | $t_h$ | -0.877 | -0.878 | -1.437 | -1.629 | -1.803 | -1.712 | -1.640 | -1.637 | -1.814 | -1.720 | -1.685 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -0.747 | -0.789 | -1.131 | -1.230 | -1.338 | -1.288 | -1.617 | -1.231 | -1.336 | -1.288 | -1.659 | ns |
| | | $t_h$ | 0.864 | 0.922 | 1.321 | 1.440 | 1.569 | 1.508 | 1.836 | 1.449 | 1.576 | 1.516 | 1.879 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.148 | 1.840 | 2.080 | 2.304 | 2.185 | 2.121 | 2.097 | 2.327 | 2.205 | 2.170 | ns |
| | | $t_h$ | -0.877 | -0.878 | -1.437 | -1.629 | -1.803 | -1.712 | -1.640 | -1.637 | -1.814 | -1.720 | -1.685 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.756 | -0.798 | -1.145 | -1.241 | -1.345 | -1.296 | -1.623 | -1.238 | -1.337 | -1.291 | -1.661 | ns |
| | | $t_h$ | 0.873 | 0.931 | 1.336 | 1.454 | 1.579 | 1.518 | 1.847 | 1.459 | 1.582 | 1.521 | 1.886 | ns |
| | GCLK PLL | $t_{su}$ | 1.122 | 1.139 | 1.825 | 2.064 | 2.293 | 2.173 | 2.110 | 2.086 | 2.321 | 2.197 | 2.163 | ns |
| | | $t_h$ | -0.868 | -0.869 | -1.422 | -1.611 | -1.789 | -1.698 | -1.625 | -1.623 | -1.805 | -1.711 | -1.674 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.756 | -0.798 | -1.145 | -1.241 | -1.345 | -1.296 | -1.623 | -1.238 | -1.337 | -1.291 | -1.661 | ns |
| | | $t_h$ | 0.873 | 0.931 | 1.336 | 1.454 | 1.579 | 1.518 | 1.847 | 1.459 | 1.582 | 1.521 | 1.886 | ns |
| | GCLK PLL | $t_{su}$ | 1.122 | 1.139 | 1.825 | 2.064 | 2.293 | 2.173 | 2.110 | 2.086 | 2.321 | 2.197 | 2.163 | ns |
| | | $t_h$ | -0.868 | -0.869 | -1.422 | -1.611 | -1.789 | -1.698 | -1.625 | -1.623 | -1.805 | -1.711 | -1.674 | ns |

Table 1–67 lists the EP3SL110 column pins output timing parameters for differential I/O standards.

**Table 1–67.** EP3SL110 Column Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.100 | 3.330 | 4.687 | 5.079 | 5.586 | 5.447 | 5.731 | 5.200 | 5.706 | 5.570 | 5.803 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.480 | 1.885 | 1.978 | 2.188 | 2.199 | 2.226 | 2.081 | 2.293 | 2.303 | 2.211 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.096 | 3.333 | 4.734 | 5.134 | 5.648 | 5.509 | 5.793 | 5.259 | 5.772 | 5.636 | 5.869 | ns |
| | | GCLK PLL | $t_{co}$ | 1.304 | 1.483 | 1.932 | 2.033 | 2.250 | 2.261 | 2.288 | 2.140 | 2.359 | 2.369 | 2.277 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.100 | 3.330 | 4.687 | 5.079 | 5.586 | 5.447 | 5.731 | 5.200 | 5.706 | 5.570 | 5.803 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.480 | 1.885 | 1.978 | 2.188 | 2.199 | 2.226 | 2.081 | 2.293 | 2.303 | 2.211 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.096 | 3.333 | 4.734 | 5.134 | 5.648 | 5.509 | 5.793 | 5.259 | 5.772 | 5.636 | 5.869 | ns |
| | | GCLK PLL | $t_{co}$ | 1.304 | 1.483 | 1.932 | 2.033 | 2.250 | 2.261 | 2.288 | 2.140 | 2.359 | 2.369 | 2.277 | ns |


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**Table 1–67.** EP3SL110 Column Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.100 | 3.330 | 4.687 | 5.079 | 5.586 | 5.447 | 5.731 | 5.200 | 5.706 | 5.570 | 5.803 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.480 | 1.885 | 1.978 | 2.188 | 2.199 | 2.226 | 2.081 | 2.293 | 2.303 | 2.211 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.096 | 3.333 | 4.734 | 5.134 | 5.648 | 5.509 | 5.793 | 5.259 | 5.772 | 5.636 | 5.869 | ns |
| | | GCLK PLL | $t_{co}$ | 1.304 | 1.483 | 1.932 | 2.033 | 2.250 | 2.261 | 2.288 | 2.140 | 2.359 | 2.369 | 2.277 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.127 | 3.363 | 4.758 | 5.157 | 5.670 | 5.531 | 5.815 | 5.280 | 5.792 | 5.656 | 5.889 | ns |
| | | GCLK PLL | $t_{co}$ | 1.335 | 1.513 | 1.956 | 2.056 | 2.272 | 2.283 | 2.310 | 2.161 | 2.379 | 2.389 | 2.297 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.117 | 3.353 | 4.748 | 5.146 | 5.660 | 5.521 | 5.805 | 5.269 | 5.782 | 5.646 | 5.879 | ns |
| | | GCLK PLL | $t_{co}$ | 1.325 | 1.503 | 1.946 | 2.045 | 2.262 | 2.273 | 2.300 | 2.150 | 2.369 | 2.379 | 2.287 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.117 | 3.353 | 4.751 | 5.150 | 5.664 | 5.525 | 5.809 | 5.274 | 5.787 | 5.651 | 5.884 | ns |
| | | GCLK PLL | $t_{co}$ | 1.325 | 1.503 | 1.949 | 2.049 | 2.266 | 2.277 | 2.304 | 2.155 | 2.374 | 2.384 | 2.292 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.110 | 3.347 | 4.744 | 5.144 | 5.658 | 5.519 | 5.803 | 5.267 | 5.781 | 5.645 | 5.878 | ns |
| | | GCLK PLL | $t_{co}$ | 1.318 | 1.497 | 1.942 | 2.043 | 2.260 | 2.271 | 2.298 | 2.148 | 2.368 | 2.378 | 2.286 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.109 | 3.345 | 4.741 | 5.141 | 5.655 | 5.516 | 5.800 | 5.264 | 5.777 | 5.641 | 5.874 | ns |
| | | GCLK PLL | $t_{co}$ | 1.317 | 1.495 | 1.939 | 2.040 | 2.257 | 2.268 | 2.295 | 2.145 | 2.364 | 2.374 | 2.282 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.131 | 3.367 | 4.762 | 5.161 | 5.674 | 5.535 | 5.819 | 5.284 | 5.797 | 5.661 | 5.894 | ns |
| | | GCLK PLL | $t_{co}$ | 1.339 | 1.517 | 1.960 | 2.060 | 2.276 | 2.287 | 2.314 | 2.165 | 2.384 | 2.394 | 2.302 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.121 | 3.356 | 4.741 | 5.138 | 5.649 | 5.510 | 5.794 | 5.260 | 5.770 | 5.634 | 5.867 | ns |
| | | GCLK PLL | $t_{co}$ | 1.329 | 1.506 | 1.939 | 2.037 | 2.251 | 2.262 | 2.289 | 2.141 | 2.357 | 2.367 | 2.275 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.116 | 3.352 | 4.741 | 5.138 | 5.650 | 5.511 | 5.795 | 5.261 | 5.772 | 5.636 | 5.869 | ns |
| | | GCLK PLL | $t_{co}$ | 1.324 | 1.502 | 1.939 | 2.037 | 2.252 | 2.263 | 2.290 | 2.142 | 2.359 | 2.369 | 2.277 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.114 | 3.350 | 4.740 | 5.137 | 5.648 | 5.509 | 5.793 | 5.260 | 5.771 | 5.635 | 5.868 | ns |
| | | GCLK PLL | $t_{co}$ | 1.322 | 1.500 | 1.938 | 2.036 | 2.250 | 2.261 | 2.288 | 2.141 | 2.358 | 2.368 | 2.276 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.106 | 3.341 | 4.730 | 5.127 | 5.639 | 5.500 | 5.784 | 5.250 | 5.761 | 5.625 | 5.858 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.491 | 1.928 | 2.026 | 2.241 | 2.252 | 2.279 | 2.131 | 2.348 | 2.358 | 2.266 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.107 | 3.343 | 4.736 | 5.134 | 5.647 | 5.508 | 5.792 | 5.258 | 5.770 | 5.634 | 5.867 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.493 | 1.934 | 2.033 | 2.249 | 2.260 | 2.287 | 2.139 | 2.357 | 2.367 | 2.275 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.106 | 3.340 | 4.719 | 5.115 | 5.625 | 5.486 | 5.770 | 5.237 | 5.746 | 5.610 | 5.843 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.490 | 1.917 | 2.014 | 2.227 | 2.238 | 2.265 | 2.118 | 2.333 | 2.343 | 2.251 | ns |

**Table 1–67.** EP3SL110 Column Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.118 | 3.353 | 4.737 | 5.133 | 5.643 | 5.504 | 5.788 | 5.256 | 5.765 | 5.629 | 5.862 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.503 | 1.935 | 2.032 | 2.245 | 2.256 | 2.283 | 2.137 | 2.352 | 2.362 | 2.270 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.114 | 3.350 | 4.738 | 5.135 | 5.647 | 5.508 | 5.792 | 5.258 | 5.769 | 5.633 | 5.866 | ns |
| | | GCLK PLL | $t_{co}$ | 1.322 | 1.500 | 1.936 | 2.034 | 2.249 | 2.260 | 2.287 | 2.139 | 2.356 | 2.366 | 2.274 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.104 | 3.339 | 4.727 | 5.124 | 5.635 | 5.496 | 5.780 | 5.247 | 5.757 | 5.621 | 5.854 | ns |
| | | GCLK PLL | $t_{co}$ | 1.312 | 1.489 | 1.925 | 2.023 | 2.237 | 2.248 | 2.275 | 2.128 | 2.344 | 2.354 | 2.262 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.102 | 3.337 | 4.725 | 5.121 | 5.633 | 5.494 | 5.778 | 5.245 | 5.755 | 5.619 | 5.852 | ns |
| | | GCLK PLL | $t_{co}$ | 1.310 | 1.487 | 1.923 | 2.020 | 2.235 | 2.246 | 2.273 | 2.126 | 2.342 | 2.352 | 2.260 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.102 | 3.338 | 4.728 | 5.126 | 5.638 | 5.499 | 5.783 | 5.249 | 5.761 | 5.625 | 5.858 | ns |
| | | GCLK PLL | $t_{co}$ | 1.310 | 1.488 | 1.926 | 2.025 | 2.240 | 2.251 | 2.278 | 2.130 | 2.348 | 2.358 | 2.266 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.106 | 3.341 | 4.725 | 5.121 | 5.632 | 5.493 | 5.777 | 5.244 | 5.754 | 5.618 | 5.851 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.491 | 1.923 | 2.020 | 2.234 | 2.245 | 2.272 | 2.125 | 2.341 | 2.351 | 2.259 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.132 | 3.370 | 4.770 | 5.169 | 5.682 | 5.543 | 5.827 | 5.292 | 5.804 | 5.668 | 5.901 | ns |
| | | GCLK PLL | $t_{co}$ | 1.340 | 1.520 | 1.968 | 2.068 | 2.284 | 2.295 | 2.322 | 2.173 | 2.391 | 2.401 | 2.309 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.118 | 3.356 | 4.758 | 5.158 | 5.672 | 5.533 | 5.817 | 5.282 | 5.795 | 5.659 | 5.892 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.506 | 1.956 | 2.057 | 2.274 | 2.285 | 2.312 | 2.163 | 2.382 | 2.392 | 2.300 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.106 | 3.343 | 4.741 | 5.140 | 5.654 | 5.515 | 5.799 | 5.264 | 5.777 | 5.641 | 5.874 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.493 | 1.939 | 2.039 | 2.256 | 2.267 | 2.294 | 2.145 | 2.364 | 2.374 | 2.282 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.106 | 3.343 | 4.744 | 5.144 | 5.658 | 5.519 | 5.803 | 5.268 | 5.782 | 5.646 | 5.879 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.493 | 1.942 | 2.043 | 2.260 | 2.271 | 2.298 | 2.149 | 2.369 | 2.379 | 2.287 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.102 | 3.339 | 4.737 | 5.136 | 5.651 | 5.512 | 5.796 | 5.261 | 5.774 | 5.638 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.310 | 1.489 | 1.935 | 2.035 | 2.253 | 2.264 | 2.291 | 2.142 | 2.361 | 2.371 | 2.279 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.106 | 3.341 | 4.730 | 5.127 | 5.639 | 5.500 | 5.784 | 5.250 | 5.761 | 5.625 | 5.858 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.491 | 1.928 | 2.026 | 2.241 | 2.252 | 2.279 | 2.131 | 2.348 | 2.358 | 2.266 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.107 | 3.343 | 4.738 | 5.137 | 5.650 | 5.511 | 5.795 | 5.260 | 5.773 | 5.637 | 5.870 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.493 | 1.936 | 2.036 | 2.252 | 2.263 | 2.290 | 2.141 | 2.360 | 2.370 | 2.278 | ns |


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**Table 1–67.** EP3SL110 Column Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.135 | 3.373 | 4.769 | 5.167 | 5.680 | 5.541 | 5.825 | 5.291 | 5.802 | 5.666 | 5.899 | ns |
| | | GCLK PLL | $t_{co}$ | 1.343 | 1.523 | 1.967 | 2.066 | 2.282 | 2.293 | 2.320 | 2.172 | 2.389 | 2.399 | 2.307 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.124 | 3.361 | 4.757 | 5.155 | 5.668 | 5.529 | 5.813 | 5.279 | 5.790 | 5.654 | 5.887 | ns |
| | | GCLK PLL | $t_{co}$ | 1.332 | 1.511 | 1.955 | 2.054 | 2.270 | 2.281 | 2.308 | 2.160 | 2.377 | 2.387 | 2.295 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.119 | 3.357 | 4.757 | 5.156 | 5.669 | 5.530 | 5.814 | 5.280 | 5.792 | 5.656 | 5.889 | ns |
| | | GCLK PLL | $t_{co}$ | 1.327 | 1.507 | 1.955 | 2.055 | 2.271 | 2.282 | 2.309 | 2.161 | 2.379 | 2.389 | 2.297 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.105 | 3.342 | 4.739 | 5.137 | 5.650 | 5.511 | 5.795 | 5.261 | 5.774 | 5.638 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.313 | 1.492 | 1.937 | 2.036 | 2.252 | 2.263 | 2.290 | 2.142 | 2.361 | 2.371 | 2.279 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.103 | 3.340 | 4.737 | 5.135 | 5.648 | 5.509 | 5.793 | 5.259 | 5.771 | 5.635 | 5.868 | ns |
| | | GCLK PLL | $t_{co}$ | 1.311 | 1.490 | 1.935 | 2.034 | 2.250 | 2.261 | 2.288 | 2.140 | 2.358 | 2.368 | 2.276 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.107 | 3.342 | 4.729 | 5.125 | 5.636 | 5.497 | 5.781 | 5.248 | 5.758 | 5.622 | 5.855 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.492 | 1.927 | 2.024 | 2.238 | 2.249 | 2.276 | 2.129 | 2.345 | 2.355 | 2.263 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.107 | 3.343 | 4.737 | 5.135 | 5.648 | 5.509 | 5.793 | 5.259 | 5.771 | 5.635 | 5.868 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.493 | 1.935 | 2.034 | 2.250 | 2.261 | 2.288 | 2.140 | 2.358 | 2.368 | 2.276 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.123 | 3.360 | 4.753 | 5.150 | 5.662 | 5.523 | 5.807 | 5.274 | 5.784 | 5.648 | 5.881 | ns |
| | | GCLK PLL | $t_{co}$ | 1.331 | 1.510 | 1.951 | 2.049 | 2.264 | 2.275 | 2.302 | 2.155 | 2.371 | 2.381 | 2.289 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.123 | 3.360 | 4.753 | 5.150 | 5.662 | 5.523 | 5.807 | 5.274 | 5.784 | 5.648 | 5.881 | ns |
| | | GCLK PLL | $t_{co}$ | 1.331 | 1.510 | 1.951 | 2.049 | 2.264 | 2.275 | 2.302 | 2.155 | 2.371 | 2.381 | 2.289 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.113 | 3.350 | 4.743 | 5.140 | 5.652 | 5.513 | 5.797 | 5.264 | 5.775 | 5.639 | 5.872 | ns |
| | | GCLK PLL | $t_{co}$ | 1.321 | 1.500 | 1.941 | 2.039 | 2.254 | 2.265 | 2.292 | 2.145 | 2.362 | 2.372 | 2.280 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.106 | 3.342 | 4.729 | 5.125 | 5.636 | 5.497 | 5.781 | 5.248 | 5.758 | 5.622 | 5.855 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.492 | 1.927 | 2.024 | 2.238 | 2.249 | 2.276 | 2.129 | 2.345 | 2.355 | 2.263 | ns |

Table 1–68 lists the EP3SL110 row pins output timing parameters for differential I/O standards.

**Table 1–68.** EP3SL110 Row Pins Output Timing Parameters (Part 1 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | — | GCLK | $t_{co}$ | 2.711 | 2.894 | 4.033 | 4.387 | 4.843 | 4.717 | 4.978 | 4.486 | 4.943 | 4.816 | 5.035 | ns |
| | | GCLK PLL | $t_{co}$ | 0.934 | 1.059 | 1.248 | 1.300 | 1.459 | 1.480 | 1.491 | 1.379 | 1.542 | 1.561 | 1.459 | ns |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.106 | 3.342 | 4.709 | 5.107 | 5.611 | 5.475 | 5.730 | 5.229 | 5.736 | 5.599 | 5.802 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.503 | 1.919 | 2.016 | 2.222 | 2.235 | 2.238 | 2.120 | 2.330 | 2.340 | 2.222 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.088 | 3.332 | 4.747 | 5.153 | 5.665 | 5.529 | 5.784 | 5.280 | 5.797 | 5.660 | 5.863 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.493 | 1.957 | 2.062 | 2.276 | 2.289 | 2.292 | 2.171 | 2.391 | 2.401 | 2.283 | ns |
| MINI-LVDS | — | GCLK | $t_{co}$ | 2.711 | 2.894 | 4.033 | 4.387 | 4.843 | 4.717 | 4.978 | 4.486 | 4.943 | 4.816 | 5.035 | ns |
| | | GCLK PLL | $t_{co}$ | 0.934 | 1.059 | 1.248 | 1.300 | 1.459 | 1.480 | 1.491 | 1.379 | 1.542 | 1.561 | 1.459 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.106 | 3.342 | 4.709 | 5.107 | 5.611 | 5.475 | 5.730 | 5.229 | 5.736 | 5.599 | 5.802 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.503 | 1.919 | 2.016 | 2.222 | 2.235 | 2.238 | 2.120 | 2.330 | 2.340 | 2.222 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.088 | 3.332 | 4.747 | 5.153 | 5.665 | 5.529 | 5.784 | 5.280 | 5.797 | 5.660 | 5.863 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.493 | 1.957 | 2.062 | 2.276 | 2.289 | 2.292 | 2.171 | 2.391 | 2.401 | 2.283 | ns |
| RSDS | — | GCLK | $t_{co}$ | 2.711 | 2.894 | 4.033 | 4.387 | 4.843 | 4.717 | 4.978 | 4.486 | 4.943 | 4.816 | 5.035 | ns |
| | | GCLK PLL | $t_{co}$ | 0.934 | 1.059 | 1.248 | 1.300 | 1.459 | 1.480 | 1.491 | 1.379 | 1.542 | 1.561 | 1.459 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.106 | 3.342 | 4.709 | 5.107 | 5.611 | 5.475 | 5.730 | 5.229 | 5.736 | 5.599 | 5.802 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.503 | 1.919 | 2.016 | 2.222 | 2.235 | 2.238 | 2.120 | 2.330 | 2.340 | 2.222 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.088 | 3.332 | 4.747 | 5.153 | 5.665 | 5.529 | 5.784 | 5.280 | 5.797 | 5.660 | 5.863 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.493 | 1.957 | 2.062 | 2.276 | 2.289 | 2.292 | 2.171 | 2.391 | 2.401 | 2.283 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.132 | 3.375 | 4.783 | 5.187 | 5.698 | 5.562 | 5.817 | 5.313 | 5.826 | 5.689 | 5.892 | ns |
| | | GCLK PLL | $t_{co}$ | 1.352 | 1.536 | 1.993 | 2.096 | 2.309 | 2.322 | 2.325 | 2.204 | 2.420 | 2.430 | 2.312 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.118 | 3.361 | 4.770 | 5.174 | 5.685 | 5.549 | 5.804 | 5.299 | 5.813 | 5.676 | 5.879 | ns |
| | | GCLK PLL | $t_{co}$ | 1.338 | 1.522 | 1.980 | 2.083 | 2.296 | 2.309 | 2.312 | 2.190 | 2.407 | 2.417 | 2.299 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.114 | 3.357 | 4.768 | 5.174 | 5.686 | 5.550 | 5.805 | 5.299 | 5.815 | 5.678 | 5.881 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.518 | 1.978 | 2.083 | 2.297 | 2.310 | 2.313 | 2.190 | 2.409 | 2.419 | 2.301 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.130 | 3.372 | 4.769 | 5.171 | 5.680 | 5.544 | 5.799 | 5.296 | 5.808 | 5.671 | 5.874 | ns |
| | | GCLK PLL | $t_{co}$ | 1.350 | 1.533 | 1.979 | 2.080 | 2.291 | 2.304 | 2.307 | 2.187 | 2.402 | 2.412 | 2.294 | ns |

**Table 1–68.** EP3SL110 Row Pins Output Timing Parameters (Part 2 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.119 | 3.362 | 4.765 | 5.167 | 5.677 | 5.541 | 5.796 | 5.293 | 5.805 | 5.668 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.339 | 1.523 | 1.975 | 2.076 | 2.288 | 2.301 | 2.304 | 2.184 | 2.399 | 2.409 | 2.291 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.116 | 3.359 | 4.763 | 5.165 | 5.675 | 5.539 | 5.794 | 5.291 | 5.804 | 5.667 | 5.870 | ns |
| | | GCLK PLL | $t_{co}$ | 1.336 | 1.520 | 1.973 | 2.074 | 2.286 | 2.299 | 2.302 | 2.182 | 2.398 | 2.408 | 2.290 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.127 | 3.369 | 4.764 | 5.166 | 5.674 | 5.538 | 5.793 | 5.291 | 5.802 | 5.665 | 5.868 | ns |
| | | GCLK PLL | $t_{co}$ | 1.347 | 1.530 | 1.974 | 2.075 | 2.285 | 2.298 | 2.301 | 2.182 | 2.396 | 2.406 | 2.288 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.117 | 3.360 | 4.762 | 5.164 | 5.673 | 5.537 | 5.792 | 5.290 | 5.802 | 5.665 | 5.868 | ns |
| | | GCLK PLL | $t_{co}$ | 1.337 | 1.521 | 1.972 | 2.073 | 2.284 | 2.297 | 2.300 | 2.181 | 2.396 | 2.406 | 2.288 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.103 | 3.346 | 4.747 | 5.149 | 5.659 | 5.523 | 5.778 | 5.275 | 5.787 | 5.650 | 5.853 | ns |
| | | GCLK PLL | $t_{co}$ | 1.323 | 1.507 | 1.957 | 2.058 | 2.270 | 2.283 | 2.286 | 2.166 | 2.381 | 2.391 | 2.273 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 10mA | GCLK | $t_{co}$ | 3.100 | 3.342 | 4.743 | 5.145 | 5.655 | 5.519 | 5.774 | 5.271 | 5.783 | 5.646 | 5.849 | ns |
| | | GCLK PLL | $t_{co}$ | 1.320 | 1.503 | 1.953 | 2.054 | 2.266 | 2.279 | 2.282 | 2.162 | 2.377 | 2.387 | 2.269 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 12mA | GCLK | $t_{co}$ | 3.097 | 3.340 | 4.744 | 5.148 | 5.658 | 5.522 | 5.777 | 5.274 | 5.787 | 5.650 | 5.853 | ns |
| | | GCLK PLL | $t_{co}$ | 1.317 | 1.501 | 1.954 | 2.057 | 2.269 | 2.282 | 2.285 | 2.165 | 2.381 | 2.391 | 2.273 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.098 | 3.340 | 4.734 | 5.136 | 5.645 | 5.509 | 5.764 | 5.261 | 5.773 | 5.636 | 5.839 | ns |
| | | GCLK PLL | $t_{co}$ | 1.318 | 1.501 | 1.944 | 2.045 | 2.256 | 2.269 | 2.272 | 2.152 | 2.367 | 2.377 | 2.259 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.147 | 3.393 | 4.805 | 5.209 | 5.721 | 5.585 | 5.840 | 5.335 | 5.849 | 5.712 | 5.915 | ns |
| | | GCLK PLL | $t_{co}$ | 1.367 | 1.554 | 2.015 | 2.118 | 2.332 | 2.345 | 2.348 | 2.226 | 2.443 | 2.453 | 2.335 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.123 | 3.369 | 4.787 | 5.192 | 5.704 | 5.568 | 5.823 | 5.318 | 5.834 | 5.697 | 5.900 | ns |
| | | GCLK PLL | $t_{co}$ | 1.343 | 1.530 | 1.997 | 2.101 | 2.315 | 2.328 | 2.331 | 2.209 | 2.428 | 2.438 | 2.320 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.106 | 3.350 | 4.765 | 5.170 | 5.682 | 5.546 | 5.801 | 5.296 | 5.812 | 5.675 | 5.878 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.511 | 1.975 | 2.079 | 2.293 | 2.306 | 2.309 | 2.187 | 2.406 | 2.416 | 2.298 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.151 | 3.396 | 4.805 | 5.209 | 5.720 | 5.584 | 5.839 | 5.335 | 5.849 | 5.712 | 5.915 | ns |
| | | GCLK PLL | $t_{co}$ | 1.371 | 1.557 | 2.015 | 2.118 | 2.331 | 2.344 | 2.347 | 2.226 | 2.443 | 2.453 | 2.335 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 6mA | GCLK | $t_{co}$ | 3.136 | 3.381 | 4.791 | 5.194 | 5.705 | 5.569 | 5.824 | 5.320 | 5.834 | 5.697 | 5.900 | ns |
| | | GCLK PLL | $t_{co}$ | 1.356 | 1.542 | 2.001 | 2.103 | 2.316 | 2.329 | 2.332 | 2.211 | 2.428 | 2.438 | 2.320 | ns |

**Table 1–68.** EP3SL110 Row Pins Output Timing Parameters (Part 3 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.125 | 3.370 | 4.786 | 5.191 | 5.702 | 5.566 | 5.821 | 5.317 | 5.832 | 5.695 | 5.898 | ns |
| | | GCLK PLL | $t_{co}$ | 1.345 | 1.531 | 1.996 | 2.100 | 2.313 | 2.326 | 2.329 | 2.208 | 2.426 | 2.436 | 2.318 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 10mA | GCLK | $t_{co}$ | 3.105 | 3.350 | 4.763 | 5.167 | 5.679 | 5.543 | 5.798 | 5.294 | 5.808 | 5.671 | 5.874 | ns |
| | | GCLK PLL | $t_{co}$ | 1.325 | 1.511 | 1.973 | 2.076 | 2.290 | 2.303 | 2.306 | 2.185 | 2.402 | 2.412 | 2.294 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 12mA | GCLK | $t_{co}$ | 3.102 | 3.346 | 4.759 | 5.164 | 5.675 | 5.539 | 5.794 | 5.290 | 5.805 | 5.668 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.322 | 1.507 | 1.969 | 2.073 | 2.286 | 2.299 | 2.302 | 2.181 | 2.399 | 2.409 | 2.291 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.107 | 3.350 | 4.750 | 5.152 | 5.661 | 5.525 | 5.780 | 5.277 | 5.789 | 5.652 | 5.855 | ns |
| | | GCLK PLL | $t_{co}$ | 1.327 | 1.511 | 1.960 | 2.061 | 2.272 | 2.285 | 2.288 | 2.168 | 2.383 | 2.393 | 2.275 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.100 | 3.343 | 4.749 | 5.153 | 5.664 | 5.528 | 5.783 | 5.280 | 5.794 | 5.657 | 5.860 | ns |
| | | GCLK PLL | $t_{co}$ | 1.320 | 1.504 | 1.959 | 2.062 | 2.275 | 2.288 | 2.291 | 2.171 | 2.388 | 2.398 | 2.280 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.138 | 3.382 | 4.787 | 5.190 | 5.700 | 5.564 | 5.819 | 5.316 | 5.829 | 5.692 | 5.895 | ns |
| | | GCLK PLL | $t_{co}$ | 1.358 | 1.543 | 1.997 | 2.099 | 2.311 | 2.324 | 2.327 | 2.207 | 2.423 | 2.433 | 2.315 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 12mA | GCLK | $t_{co}$ | 3.120 | 3.365 | 4.772 | 5.175 | 5.685 | 5.549 | 5.804 | 5.301 | 5.814 | 5.677 | 5.880 | ns |
| | | GCLK PLL | $t_{co}$ | 1.340 | 1.526 | 1.982 | 2.084 | 2.296 | 2.309 | 2.312 | 2.192 | 2.408 | 2.418 | 2.300 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.106 | 3.349 | 4.749 | 5.151 | 5.660 | 5.524 | 5.779 | 5.277 | 5.789 | 5.652 | 5.855 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.510 | 1.959 | 2.060 | 2.271 | 2.284 | 2.287 | 2.168 | 2.383 | 2.393 | 2.275 | ns |

Table 1–69 and Table 1–70 list the EP3SL110 regional clock (RCLK) adder values that must be added to the GCLK values. Use these adder values to determine I/O timing when the I/O pin is driven using the regional clock. This applies to all I/O standards supported by Stratix III devices.

Table 1–69 lists the EP3SL110 column pin delay adders when using the regional clock.

**Table 1–69.** EP3SL110 Column Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.186 | 0.171 | 0.245 | 0.255 | 0.268 | 0.261 | 0.393 | 0.248 | 0.277 | 0.267 | 0.364 | ns |
| RCLK PLL input adder | 2.391 | 2.371 | 3.577 | 4.036 | 4.418 | 4.225 | 4.574 | 4.044 | 4.442 | 4.246 | 4.635 | ns |
| RCLK output adder | -0.374 | -0.162 | -0.226 | -0.233 | -0.244 | -0.239 | -0.367 | -0.111 | -0.123 | -0.116 | -0.296 | ns |
| RCLK PLL output adder | -2.001 | -1.786 | -2.669 | -2.844 | -2.996 | -2.879 | -2.722 | -2.699 | -3.067 | -2.798 | -2.773 | ns |


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Table 1–70 lists the EP3SL110 row pin delay adders when using the regional clock.

**Table 1–70.** EP3SL110 Row Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.086 | 0.109 | 0.158 | 0.16 | 0.161 | 0.159 | 0.281 | 0.137 | 0.153 | 0.153 | 0.285 | ns |
| RCLK PLL input adder | 0.075 | 0.075 | 0.117 | 0.123 | 0.129 | 0.125 | 0.222 | 0.113 | 0.118 | 0.114 | 0.226 | ns |
| RCLK output adder | -0.072 | -0.097 | -0.137 | -0.135 | -0.116 | -0.134 | -0.24 | -0.11 | -0.104 | -0.124 | -0.244 | ns |
| RCLK PLL output adder | -0.063 | -0.065 | -0.097 | -0.1 | -0.104 | -0.101 | -0.198 | -0.088 | -0.09 | -0.088 | -0.201 | ns |

## EP3SL150 I/O Timing Parameters

Table 1–71 through Table 1–74 list the maximum I/O timing parameters for EP3SL150 devices for single-ended I/O standards.

Table 1–71 lists the EP3SL150 column pins input timing parameters for single-ended I/O standards.

**Table 1–71.** EP3SL150 Column Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -0.986 | -0.964 | -1.402 | -1.558 | -1.797 | -1.778 | -2.106 | -1.558 | -1.797 | -1.778 | -2.106 | ns |
| | | $t_h$ | 1.119 | 1.093 | 1.584 | 1.767 | 2.027 | 1.996 | 2.327 | 1.767 | 2.027 | 1.996 | 2.327 | ns |
| | GCLK PLL | $t_{su}$ | -1.278 | -1.221 | -1.771 | -1.984 | -2.197 | -2.123 | -2.542 | -1.984 | -2.197 | -2.123 | -2.542 | ns |
| | | $t_h$ | 1.556 | 1.499 | 2.175 | 2.439 | 2.697 | 2.598 | 3.034 | 2.439 | 2.697 | 2.598 | 3.034 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -0.986 | -0.964 | -1.402 | -1.558 | -1.797 | -1.778 | -2.106 | -1.558 | -1.797 | -1.778 | -2.106 | ns |
| | | $t_h$ | 1.119 | 1.093 | 1.584 | 1.767 | 2.027 | 1.996 | 2.327 | 1.767 | 2.027 | 1.996 | 2.327 | ns |
| | GCLK PLL | $t_{su}$ | -1.278 | -1.221 | -1.771 | -1.984 | -2.197 | -2.123 | -2.542 | -1.984 | -2.197 | -2.123 | -2.542 | ns |
| | | $t_h$ | 1.556 | 1.499 | 2.175 | 2.439 | 2.697 | 2.598 | 3.034 | 2.439 | 2.697 | 2.598 | 3.034 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -0.997 | -0.975 | -1.401 | -1.560 | -1.796 | -1.777 | -2.105 | -1.560 | -1.796 | -1.777 | -2.105 | ns |
| | | $t_h$ | 1.130 | 1.104 | 1.583 | 1.769 | 2.026 | 1.995 | 2.326 | 1.769 | 2.026 | 1.995 | 2.326 | ns |
| | GCLK PLL | $t_{su}$ | -1.289 | -1.232 | -1.770 | -1.986 | -2.196 | -2.122 | -2.541 | -1.986 | -2.196 | -2.122 | -2.541 | ns |
| | | $t_h$ | 1.567 | 1.510 | 2.174 | 2.441 | 2.696 | 2.597 | 3.033 | 2.441 | 2.696 | 2.597 | 3.033 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -0.997 | -0.975 | -1.401 | -1.560 | -1.796 | -1.777 | -2.105 | -1.560 | -1.796 | -1.777 | -2.105 | ns |
| | | $t_h$ | 1.130 | 1.104 | 1.583 | 1.769 | 2.026 | 1.995 | 2.326 | 1.769 | 2.026 | 1.995 | 2.326 | ns |
| | GCLK PLL | $t_{su}$ | -1.289 | -1.232 | -1.770 | -1.986 | -2.196 | -2.122 | -2.541 | -1.986 | -2.196 | -2.122 | -2.541 | ns |
| | | $t_h$ | 1.567 | 1.510 | 2.174 | 2.441 | 2.696 | 2.597 | 3.033 | 2.441 | 2.696 | 2.597 | 3.033 | ns |
| 2.5 V | GCLK | $t_{su}$ | -0.992 | -0.970 | -1.410 | -1.572 | -1.815 | -1.796 | -2.124 | -1.572 | -1.815 | -1.796 | -2.124 | ns |
| | | $t_h$ | 1.125 | 1.099 | 1.592 | 1.781 | 2.045 | 2.014 | 2.345 | 1.781 | 2.045 | 2.014 | 2.345 | ns |
| | GCLK PLL | $t_{su}$ | -1.284 | -1.227 | -1.779 | -1.998 | -2.215 | -2.141 | -2.560 | -1.998 | -2.215 | -2.141 | -2.560 | ns |
| | | $t_h$ | 1.562 | 1.505 | 2.183 | 2.453 | 2.715 | 2.616 | 3.052 | 2.453 | 2.715 | 2.616 | 3.052 | ns |

**Table 1–71.** EP3SL150 Column Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | GCLK | $t_{su}$ | -1.014 | -0.992 | -1.450 | -1.608 | -1.813 | -1.794 | -2.122 | -1.608 | -1.813 | -1.794 | -2.122 | ns |
| | | $t_h$ | 1.149 | 1.123 | 1.632 | 1.817 | 2.043 | 2.012 | 2.343 | 1.817 | 2.043 | 2.012 | 2.343 | ns |
| | GCLK PLL | $t_{su}$ | -1.306 | -1.249 | -1.819 | -2.034 | -2.213 | -2.139 | -2.558 | -2.034 | -2.213 | -2.139 | -2.558 | ns |
| | | $t_h$ | 1.586 | 1.529 | 2.223 | 2.489 | 2.713 | 2.614 | 3.050 | 2.489 | 2.713 | 2.614 | 3.050 | ns |
| 1.5 V | GCLK | $t_{su}$ | -1.004 | -0.982 | -1.427 | -1.576 | -1.743 | -1.724 | -2.052 | -1.576 | -1.743 | -1.724 | -2.052 | ns |
| | | $t_h$ | 1.139 | 1.113 | 1.609 | 1.785 | 1.973 | 1.942 | 2.273 | 1.785 | 1.973 | 1.942 | 2.273 | ns |
| | GCLK PLL | $t_{su}$ | -1.296 | -1.239 | -1.796 | -2.002 | -2.143 | -2.069 | -2.488 | -2.002 | -2.143 | -2.069 | -2.488 | ns |
| | | $t_h$ | 1.576 | 1.519 | 2.200 | 2.457 | 2.643 | 2.544 | 2.980 | 2.457 | 2.643 | 2.544 | 2.980 | ns |
| 1.2 V | GCLK | $t_{su}$ | -0.952 | -0.930 | -1.350 | -1.477 | -1.587 | -1.568 | -1.896 | -1.477 | -1.587 | -1.568 | -1.896 | ns |
| | | $t_h$ | 1.087 | 1.061 | 1.532 | 1.686 | 1.817 | 1.786 | 2.117 | 1.686 | 1.817 | 1.786 | 2.117 | ns |
| | GCLK PLL | $t_{su}$ | -1.244 | -1.187 | -1.719 | -1.903 | -1.987 | -1.913 | -2.332 | -1.903 | -1.987 | -1.913 | -2.332 | ns |
| | | $t_h$ | 1.524 | 1.467 | 2.123 | 2.358 | 2.487 | 2.388 | 2.824 | 2.358 | 2.487 | 2.388 | 2.824 | ns |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -0.923 | -0.901 | -1.322 | -1.461 | -1.589 | -1.570 | -1.898 | -1.461 | -1.589 | -1.570 | -1.898 | ns |
| | | $t_h$ | 1.058 | 1.032 | 1.504 | 1.670 | 1.819 | 1.788 | 2.119 | 1.670 | 1.819 | 1.788 | 2.119 | ns |
| | GCLK PLL | $t_{su}$ | -1.215 | -1.158 | -1.691 | -1.887 | -1.989 | -1.915 | -2.334 | -1.887 | -1.989 | -1.915 | -2.334 | ns |
| | | $t_h$ | 1.495 | 1.438 | 2.095 | 2.342 | 2.489 | 2.390 | 2.826 | 2.342 | 2.489 | 2.390 | 2.826 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -0.923 | -0.901 | -1.322 | -1.461 | -1.589 | -1.570 | -1.898 | -1.461 | -1.589 | -1.570 | -1.898 | ns |
| | | $t_h$ | 1.058 | 1.032 | 1.504 | 1.670 | 1.819 | 1.788 | 2.119 | 1.670 | 1.819 | 1.788 | 2.119 | ns |
| | GCLK PLL | $t_{su}$ | -1.215 | -1.158 | -1.691 | -1.887 | -1.989 | -1.915 | -2.334 | -1.887 | -1.989 | -1.915 | -2.334 | ns |
| | | $t_h$ | 1.495 | 1.438 | 2.095 | 2.342 | 2.489 | 2.390 | 2.826 | 2.342 | 2.489 | 2.390 | 2.826 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -0.917 | -0.895 | -1.309 | -1.453 | -1.586 | -1.565 | -1.896 | -1.453 | -1.586 | -1.565 | -1.896 | ns |
| | | $t_h$ | 1.052 | 1.026 | 1.491 | 1.659 | 1.813 | 1.782 | 2.112 | 1.659 | 1.813 | 1.782 | 2.112 | ns |
| | GCLK PLL | $t_{su}$ | -1.209 | -1.152 | -1.678 | -1.879 | -1.986 | -1.910 | -2.332 | -1.879 | -1.986 | -1.910 | -2.332 | ns |
| | | $t_h$ | 1.489 | 1.432 | 2.082 | 2.331 | 2.483 | 2.384 | 2.819 | 2.331 | 2.483 | 2.384 | 2.819 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -0.917 | -0.895 | -1.309 | -1.453 | -1.586 | -1.565 | -1.896 | -1.453 | -1.586 | -1.565 | -1.896 | ns |
| | | $t_h$ | 1.052 | 1.026 | 1.491 | 1.659 | 1.813 | 1.782 | 2.112 | 1.659 | 1.813 | 1.782 | 2.112 | ns |
| | GCLK PLL | $t_{su}$ | -1.209 | -1.152 | -1.678 | -1.879 | -1.986 | -1.910 | -2.332 | -1.879 | -1.986 | -1.910 | -2.332 | ns |
| | | $t_h$ | 1.489 | 1.432 | 2.082 | 2.331 | 2.483 | 2.384 | 2.819 | 2.331 | 2.483 | 2.384 | 2.819 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -0.906 | -0.884 | -1.298 | -1.442 | -1.567 | -1.546 | -1.877 | -1.442 | -1.567 | -1.546 | -1.877 | ns |
| | | $t_h$ | 1.041 | 1.015 | 1.479 | 1.648 | 1.794 | 1.763 | 2.093 | 1.648 | 1.794 | 1.763 | 2.093 | ns |
| | GCLK PLL | $t_{su}$ | -1.198 | -1.141 | -1.667 | -1.868 | -1.967 | -1.891 | -2.313 | -1.868 | -1.967 | -1.891 | -2.313 | ns |
| | | $t_h$ | 1.478 | 1.421 | 2.070 | 2.320 | 2.464 | 2.365 | 2.800 | 2.320 | 2.464 | 2.365 | 2.800 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.906 | -0.884 | -1.298 | -1.442 | -1.567 | -1.546 | -1.877 | -1.442 | -1.567 | -1.546 | -1.877 | ns |
| | | $t_h$ | 1.041 | 1.015 | 1.479 | 1.648 | 1.794 | 1.763 | 2.093 | 1.648 | 1.794 | 1.763 | 2.093 | ns |
| | GCLK PLL | $t_{su}$ | -1.198 | -1.141 | -1.667 | -1.868 | -1.967 | -1.891 | -2.313 | -1.868 | -1.967 | -1.891 | -2.313 | ns |
| | | $t_h$ | 1.478 | 1.421 | 2.070 | 2.320 | 2.464 | 2.365 | 2.800 | 2.320 | 2.464 | 2.365 | 2.800 | ns |

**Table 1–71.** EP3SL150 Column Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.917 | -0.895 | -1.309 | -1.453 | -1.586 | -1.565 | -1.896 | -1.453 | -1.586 | -1.565 | -1.896 | ns |
| | | $t_h$ | 1.052 | 1.026 | 1.491 | 1.659 | 1.813 | 1.782 | 2.112 | 1.659 | 1.813 | 1.782 | 2.112 | ns |
| | GCLK PLL | $t_{su}$ | -1.209 | -1.152 | -1.678 | -1.879 | -1.986 | -1.910 | -2.332 | -1.879 | -1.986 | -1.910 | -2.332 | ns |
| | | $t_h$ | 1.489 | 1.432 | 2.082 | 2.331 | 2.483 | 2.384 | 2.819 | 2.331 | 2.483 | 2.384 | 2.819 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.917 | -0.895 | -1.309 | -1.453 | -1.586 | -1.565 | -1.896 | -1.453 | -1.586 | -1.565 | -1.896 | ns |
| | | $t_h$ | 1.052 | 1.026 | 1.491 | 1.659 | 1.813 | 1.782 | 2.112 | 1.659 | 1.813 | 1.782 | 2.112 | ns |
| | GCLK PLL | $t_{su}$ | -1.209 | -1.152 | -1.678 | -1.879 | -1.986 | -1.910 | -2.332 | -1.879 | -1.986 | -1.910 | -2.332 | ns |
| | | $t_h$ | 1.489 | 1.432 | 2.082 | 2.331 | 2.483 | 2.384 | 2.819 | 2.331 | 2.483 | 2.384 | 2.819 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.906 | -0.884 | -1.298 | -1.442 | -1.567 | -1.546 | -1.877 | -1.442 | -1.567 | -1.546 | -1.877 | ns |
| | | $t_h$ | 1.041 | 1.015 | 1.479 | 1.648 | 1.794 | 1.763 | 2.093 | 1.648 | 1.794 | 1.763 | 2.093 | ns |
| | GCLK PLL | $t_{su}$ | -1.198 | -1.141 | -1.667 | -1.868 | -1.967 | -1.891 | -2.313 | -1.868 | -1.967 | -1.891 | -2.313 | ns |
| | | $t_h$ | 1.478 | 1.421 | 2.070 | 2.320 | 2.464 | 2.365 | 2.800 | 2.320 | 2.464 | 2.365 | 2.800 | ns |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.906 | -0.884 | -1.298 | -1.442 | -1.567 | -1.546 | -1.877 | -1.442 | -1.567 | -1.546 | -1.877 | ns |
| | | $t_h$ | 1.041 | 1.015 | 1.479 | 1.648 | 1.794 | 1.763 | 2.093 | 1.648 | 1.794 | 1.763 | 2.093 | ns |
| | GCLK PLL | $t_{su}$ | -1.198 | -1.141 | -1.667 | -1.868 | -1.967 | -1.891 | -2.313 | -1.868 | -1.967 | -1.891 | -2.313 | ns |
| | | $t_h$ | 1.478 | 1.421 | 2.070 | 2.320 | 2.464 | 2.365 | 2.800 | 2.320 | 2.464 | 2.365 | 2.800 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.894 | -0.872 | -1.288 | -1.431 | -1.551 | -1.530 | -1.861 | -1.431 | -1.551 | -1.530 | -1.861 | ns |
| | | $t_h$ | 1.029 | 1.003 | 1.469 | 1.637 | 1.778 | 1.747 | 2.077 | 1.637 | 1.778 | 1.747 | 2.077 | ns |
| | GCLK PLL | $t_{su}$ | -1.186 | -1.129 | -1.657 | -1.857 | -1.951 | -1.875 | -2.297 | -1.857 | -1.951 | -1.875 | -2.297 | ns |
| | | $t_h$ | 1.466 | 1.409 | 2.060 | 2.309 | 2.448 | 2.349 | 2.784 | 2.309 | 2.448 | 2.349 | 2.784 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -0.894 | -0.872 | -1.288 | -1.431 | -1.551 | -1.530 | -1.861 | -1.431 | -1.551 | -1.530 | -1.861 | ns |
| | | $t_h$ | 1.029 | 1.003 | 1.469 | 1.637 | 1.778 | 1.747 | 2.077 | 1.637 | 1.778 | 1.747 | 2.077 | ns |
| | GCLK PLL | $t_{su}$ | -1.186 | -1.129 | -1.657 | -1.857 | -1.951 | -1.875 | -2.297 | -1.857 | -1.951 | -1.875 | -2.297 | ns |
| | | $t_h$ | 1.466 | 1.409 | 2.060 | 2.309 | 2.448 | 2.349 | 2.784 | 2.309 | 2.448 | 2.349 | 2.784 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | -0.997 | -0.975 | -1.401 | -1.560 | -1.796 | -1.777 | -2.105 | -1.560 | -1.796 | -1.777 | -2.105 | ns |
| | | $t_h$ | 1.130 | 1.104 | 1.583 | 1.769 | 2.026 | 1.995 | 2.326 | 1.769 | 2.026 | 1.995 | 2.326 | ns |
| | GCLK PLL | $t_{su}$ | -1.289 | -1.232 | -1.770 | -1.986 | -2.196 | -2.122 | -2.541 | -1.986 | -2.196 | -2.122 | -2.541 | ns |
| | | $t_h$ | 1.567 | 1.510 | 2.174 | 2.441 | 2.696 | 2.597 | 3.033 | 2.441 | 2.696 | 2.597 | 3.033 | ns |

Table 1–72 lists the EP3SL150 row pins input timing parameters for single-ended I/O standards.

**Table 1–72.** EP3SL150 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -0.925 | -0.964 | -1.360 | -1.470 | -1.682 | -1.633 | -1.954 | -1.480 | -1.679 | -1.634 | -1.993 | ns |
| | | $t_h$ | 1.040 | 1.094 | 1.544 | 1.677 | 1.910 | 1.851 | 2.173 | 1.698 | 1.917 | 1.860 | 2.212 | ns |
| | GCLK PLL | $t_{su}$ | 0.988 | 1.009 | 1.642 | 1.858 | 1.971 | 1.855 | 1.796 | 1.865 | 1.993 | 1.875 | 1.848 | ns |
| | | $t_h$ | -0.737 | -0.741 | -1.241 | -1.407 | -1.471 | -1.383 | -1.314 | -1.407 | -1.482 | -1.393 | -1.363 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -0.925 | -0.964 | -1.360 | -1.470 | -1.682 | -1.633 | -1.954 | -1.480 | -1.679 | -1.634 | -1.993 | ns |
| | | $t_h$ | 1.040 | 1.094 | 1.544 | 1.677 | 1.910 | 1.851 | 2.173 | 1.698 | 1.917 | 1.860 | 2.212 | ns |
| | GCLK PLL | $t_{su}$ | 0.988 | 1.009 | 1.642 | 1.858 | 1.971 | 1.855 | 1.796 | 1.865 | 1.993 | 1.875 | 1.848 | ns |
| | | $t_h$ | -0.737 | -0.741 | -1.241 | -1.407 | -1.471 | -1.383 | -1.314 | -1.407 | -1.482 | -1.393 | -1.363 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -0.931 | -0.975 | -1.357 | -1.471 | -1.685 | -1.636 | -1.957 | -1.479 | -1.684 | -1.639 | -1.998 | ns |
| | | $t_h$ | 1.046 | 1.105 | 1.541 | 1.678 | 1.913 | 1.854 | 2.176 | 1.697 | 1.922 | 1.865 | 2.217 | ns |
| | GCLK PLL | $t_{su}$ | 0.982 | 0.998 | 1.645 | 1.857 | 1.968 | 1.852 | 1.793 | 1.866 | 1.988 | 1.870 | 1.843 | ns |
| | | $t_h$ | -0.731 | -0.730 | -1.244 | -1.406 | -1.468 | -1.380 | -1.311 | -1.408 | -1.477 | -1.388 | -1.358 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -0.931 | -0.975 | -1.357 | -1.471 | -1.685 | -1.636 | -1.957 | -1.479 | -1.684 | -1.639 | -1.998 | ns |
| | | $t_h$ | 1.046 | 1.105 | 1.541 | 1.678 | 1.913 | 1.854 | 2.176 | 1.697 | 1.922 | 1.865 | 2.217 | ns |
| | GCLK PLL | $t_{su}$ | 0.982 | 0.998 | 1.645 | 1.857 | 1.968 | 1.852 | 1.793 | 1.866 | 1.988 | 1.870 | 1.843 | ns |
| | | $t_h$ | -0.731 | -0.730 | -1.244 | -1.406 | -1.468 | -1.380 | -1.311 | -1.408 | -1.477 | -1.388 | -1.358 | ns |
| 2.5 V | GCLK | $t_{su}$ | -0.919 | -0.968 | -1.366 | -1.484 | -1.700 | -1.651 | -1.972 | -1.488 | -1.694 | -1.649 | -2.008 | ns |
| | | $t_h$ | 1.034 | 1.098 | 1.550 | 1.691 | 1.928 | 1.869 | 2.191 | 1.706 | 1.932 | 1.875 | 2.227 | ns |
| | GCLK PLL | $t_{su}$ | 0.994 | 1.005 | 1.636 | 1.844 | 1.953 | 1.837 | 1.778 | 1.857 | 1.978 | 1.860 | 1.833 | ns |
| | | $t_h$ | -0.743 | -0.737 | -1.235 | -1.393 | -1.453 | -1.365 | -1.296 | -1.399 | -1.467 | -1.378 | -1.348 | ns |
| 1.8 V | GCLK | $t_{su}$ | -0.949 | -1.000 | -1.406 | -1.530 | -1.590 | -1.662 | -1.875 | -1.521 | -1.582 | -1.663 | -1.913 | ns |
| | | $t_h$ | 1.065 | 1.131 | 1.590 | 1.738 | 1.824 | 1.880 | 2.098 | 1.739 | 1.826 | 1.889 | 2.137 | ns |
| | GCLK PLL | $t_{su}$ | 0.964 | 0.966 | 1.589 | 1.806 | 1.955 | 1.835 | 1.780 | 1.824 | 1.977 | 1.854 | 1.832 | ns |
| | | $t_h$ | -0.712 | -0.698 | -1.190 | -1.356 | -1.455 | -1.362 | -1.298 | -1.366 | -1.466 | -1.372 | -1.347 | ns |
| 1.5 V | GCLK | $t_{su}$ | -0.939 | -0.989 | -1.382 | -1.498 | -1.522 | -1.594 | -1.807 | -1.490 | -1.517 | -1.598 | -1.848 | ns |
| | | $t_h$ | 1.055 | 1.120 | 1.566 | 1.706 | 1.756 | 1.812 | 2.030 | 1.708 | 1.761 | 1.824 | 2.072 | ns |
| | GCLK PLL | $t_{su}$ | 0.974 | 0.977 | 1.613 | 1.838 | 2.023 | 1.903 | 1.848 | 1.855 | 2.042 | 1.919 | 1.897 | ns |
| | | $t_h$ | -0.722 | -0.709 | -1.214 | -1.388 | -1.523 | -1.430 | -1.366 | -1.397 | -1.531 | -1.437 | -1.412 | ns |
| 1.2 V | GCLK | $t_{su}$ | -0.879 | -0.936 | -1.303 | -1.397 | -1.363 | -1.435 | -1.648 | -1.394 | -1.362 | -1.443 | -1.693 | ns |
| | | $t_h$ | 0.995 | 1.067 | 1.487 | 1.605 | 1.597 | 1.653 | 1.871 | 1.612 | 1.606 | 1.669 | 1.917 | ns |
| | GCLK PLL | $t_{su}$ | 1.034 | 1.030 | 1.692 | 1.939 | 2.182 | 2.062 | 2.007 | 1.951 | 2.197 | 2.074 | 2.052 | ns |
| | | $t_h$ | -0.782 | -0.762 | -1.293 | -1.489 | -1.682 | -1.589 | -1.525 | -1.493 | -1.686 | -1.592 | -1.567 | ns |

**Table 1–72.** EP3SL150 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -0.862 | -0.910 | -1.280 | -1.375 | -1.480 | -1.431 | -1.752 | -1.376 | -1.477 | -1.432 | -1.791 | ns |
| | | $t_h$ | 0.978 | 1.041 | 1.464 | 1.582 | 1.708 | 1.649 | 1.971 | 1.594 | 1.715 | 1.658 | 2.010 | ns |
| | GCLK PLL | $t_{su}$ | 1.051 | 1.063 | 1.722 | 1.953 | 2.173 | 2.057 | 1.998 | 1.969 | 2.195 | 2.077 | 2.050 | ns |
| | | $t_h$ | -0.799 | -0.794 | -1.321 | -1.502 | -1.673 | -1.585 | -1.516 | -1.511 | -1.684 | -1.595 | -1.565 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -0.862 | -0.910 | -1.280 | -1.375 | -1.480 | -1.431 | -1.752 | -1.376 | -1.477 | -1.432 | -1.791 | ns |
| | | $t_h$ | 0.978 | 1.041 | 1.464 | 1.582 | 1.708 | 1.649 | 1.971 | 1.594 | 1.715 | 1.658 | 2.010 | ns |
| | GCLK PLL | $t_{su}$ | 1.051 | 1.063 | 1.722 | 1.953 | 2.173 | 2.057 | 1.998 | 1.969 | 2.195 | 2.077 | 2.050 | ns |
| | | $t_h$ | -0.799 | -0.794 | -1.321 | -1.502 | -1.673 | -1.585 | -1.516 | -1.511 | -1.684 | -1.595 | -1.565 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -0.853 | -0.901 | -1.265 | -1.370 | -1.361 | -1.429 | -1.646 | -1.362 | -1.358 | -1.435 | -1.688 | ns |
| | | $t_h$ | 0.969 | 1.032 | 1.449 | 1.576 | 1.592 | 1.646 | 1.865 | 1.578 | 1.599 | 1.660 | 1.908 | ns |
| | GCLK PLL | $t_{su}$ | 1.060 | 1.065 | 1.730 | 1.966 | 2.187 | 2.068 | 2.011 | 1.983 | 2.204 | 2.082 | 2.059 | ns |
| | | $t_h$ | -0.808 | -0.797 | -1.331 | -1.518 | -1.689 | -1.596 | -1.533 | -1.527 | -1.696 | -1.601 | -1.578 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -0.853 | -0.901 | -1.265 | -1.370 | -1.361 | -1.429 | -1.646 | -1.362 | -1.358 | -1.435 | -1.688 | ns |
| | | $t_h$ | 0.969 | 1.032 | 1.449 | 1.576 | 1.592 | 1.646 | 1.865 | 1.578 | 1.599 | 1.660 | 1.908 | ns |
| | GCLK PLL | $t_{su}$ | 1.060 | 1.065 | 1.730 | 1.966 | 2.187 | 2.068 | 2.011 | 1.983 | 2.204 | 2.082 | 2.059 | ns |
| | | $t_h$ | -0.808 | -0.797 | -1.331 | -1.518 | -1.689 | -1.596 | -1.533 | -1.527 | -1.696 | -1.601 | -1.578 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -0.839 | -0.889 | -1.250 | -1.360 | -1.343 | -1.411 | -1.628 | -1.351 | -1.341 | -1.418 | -1.671 | ns |
| | | $t_h$ | 0.955 | 1.020 | 1.435 | 1.566 | 1.574 | 1.628 | 1.847 | 1.567 | 1.582 | 1.643 | 1.891 | ns |
| | GCLK PLL | $t_{su}$ | 1.074 | 1.077 | 1.745 | 1.976 | 2.205 | 2.086 | 2.029 | 1.994 | 2.221 | 2.099 | 2.076 | ns |
| | | $t_h$ | -0.822 | -0.809 | -1.345 | -1.528 | -1.707 | -1.614 | -1.551 | -1.538 | -1.713 | -1.618 | -1.595 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.853 | -0.901 | -1.265 | -1.370 | -1.361 | -1.429 | -1.646 | -1.362 | -1.358 | -1.435 | -1.688 | ns |
| | | $t_h$ | 0.969 | 1.032 | 1.449 | 1.576 | 1.592 | 1.646 | 1.865 | 1.578 | 1.599 | 1.660 | 1.908 | ns |
| | GCLK PLL | $t_{su}$ | 1.060 | 1.065 | 1.730 | 1.966 | 2.187 | 2.068 | 2.011 | 1.983 | 2.204 | 2.082 | 2.059 | ns |
| | | $t_h$ | -0.808 | -0.797 | -1.331 | -1.518 | -1.689 | -1.596 | -1.533 | -1.527 | -1.696 | -1.601 | -1.578 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.853 | -0.901 | -1.265 | -1.370 | -1.361 | -1.429 | -1.646 | -1.362 | -1.358 | -1.435 | -1.688 | ns |
| | | $t_h$ | 0.969 | 1.032 | 1.449 | 1.576 | 1.592 | 1.646 | 1.865 | 1.578 | 1.599 | 1.660 | 1.908 | ns |
| | GCLK PLL | $t_{su}$ | 1.060 | 1.065 | 1.730 | 1.966 | 2.187 | 2.068 | 2.011 | 1.983 | 2.204 | 2.082 | 2.059 | ns |
| | | $t_h$ | -0.808 | -0.797 | -1.331 | -1.518 | -1.689 | -1.596 | -1.533 | -1.527 | -1.696 | -1.601 | -1.578 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.839 | -0.889 | -1.250 | -1.360 | -1.343 | -1.411 | -1.628 | -1.351 | -1.341 | -1.418 | -1.671 | ns |
| | | $t_h$ | 0.955 | 1.020 | 1.435 | 1.566 | 1.574 | 1.628 | 1.847 | 1.567 | 1.582 | 1.643 | 1.891 | ns |
| | GCLK PLL | $t_{su}$ | 1.074 | 1.077 | 1.745 | 1.976 | 2.205 | 2.086 | 2.029 | 1.994 | 2.221 | 2.099 | 2.076 | ns |
| | | $t_h$ | -0.822 | -0.809 | -1.345 | -1.528 | -1.707 | -1.614 | -1.551 | -1.538 | -1.713 | -1.618 | -1.595 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.839 | -0.889 | -1.250 | -1.360 | -1.343 | -1.411 | -1.628 | -1.351 | -1.341 | -1.418 | -1.671 | ns |
| | | $t_h$ | 0.955 | 1.020 | 1.435 | 1.566 | 1.574 | 1.628 | 1.847 | 1.567 | 1.582 | 1.643 | 1.891 | ns |
| | GCLK PLL | $t_{su}$ | 1.074 | 1.077 | 1.745 | 1.976 | 2.205 | 2.086 | 2.029 | 1.994 | 2.221 | 2.099 | 2.076 | ns |
| | | $t_h$ | -0.822 | -0.809 | -1.345 | -1.528 | -1.707 | -1.614 | -1.551 | -1.538 | -1.713 | -1.618 | -1.595 | ns |

**Table 1–72.** EP3SL150 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.830 | -0.877 | -1.241 | -1.350 | -1.327 | -1.395 | -1.612 | -1.342 | -1.325 | -1.402 | -1.655 | ns |
| | | $t_h$ | 0.946 | 1.008 | 1.426 | 1.556 | 1.558 | 1.612 | 1.831 | 1.558 | 1.566 | 1.627 | 1.875 | ns |
| | GCLK PLL | $t_{su}$ | 1.083 | 1.089 | 1.754 | 1.986 | 2.221 | 2.102 | 2.045 | 2.003 | 2.237 | 2.115 | 2.092 | ns |
| | | $t_h$ | -0.831 | -0.821 | -1.354 | -1.538 | -1.723 | -1.630 | -1.567 | -1.547 | -1.729 | -1.634 | -1.611 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.830 | -0.877 | -1.241 | -1.350 | -1.327 | -1.395 | -1.612 | -1.342 | -1.325 | -1.402 | -1.655 | ns |
| | | $t_h$ | 0.946 | 1.008 | 1.426 | 1.556 | 1.558 | 1.612 | 1.831 | 1.558 | 1.566 | 1.627 | 1.875 | ns |
| | GCLK PLL | $t_{su}$ | 1.083 | 1.089 | 1.754 | 1.986 | 2.221 | 2.102 | 2.045 | 2.003 | 2.237 | 2.115 | 2.092 | ns |
| | | $t_h$ | -0.831 | -0.821 | -1.354 | -1.538 | -1.723 | -1.630 | -1.567 | -1.547 | -1.729 | -1.634 | -1.611 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -0.931 | -0.975 | -1.357 | -1.471 | -1.685 | -1.636 | -1.957 | -1.479 | -1.684 | -1.639 | -1.998 | ns |
| | | $t_h$ | 1.046 | 1.105 | 1.541 | 1.678 | 1.913 | 1.854 | 2.176 | 1.697 | 1.922 | 1.865 | 2.217 | ns |
| | GCLK PLL | $t_{su}$ | 0.982 | 0.998 | 1.645 | 1.857 | 1.968 | 1.852 | 1.793 | 1.866 | 1.988 | 1.870 | 1.843 | ns |
| | | $t_h$ | -0.731 | -0.730 | -1.244 | -1.406 | -1.468 | -1.380 | -1.311 | -1.408 | -1.477 | -1.388 | -1.358 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | -0.931 | -0.975 | -1.357 | -1.471 | -1.685 | -1.636 | -1.957 | -1.479 | -1.684 | -1.639 | -1.998 | ns |
| | | $t_h$ | 1.046 | 1.105 | 1.541 | 1.678 | 1.913 | 1.854 | 2.176 | 1.697 | 1.922 | 1.865 | 2.217 | ns |
| | GCLK PLL | $t_{su}$ | 0.982 | 0.998 | 1.645 | 1.857 | 1.968 | 1.852 | 1.793 | 1.866 | 1.988 | 1.870 | 1.843 | ns |
| | | $t_h$ | -0.731 | -0.730 | -1.244 | -1.406 | -1.468 | -1.380 | -1.311 | -1.408 | -1.477 | -1.388 | -1.358 | ns |

Table 1–73 lists the EP3SL150 column pins output timing parameters for single-ended I/O standards.

**Table 1–73.** EP3SL150 Column Pins Output Timing Parameters (Part 1 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.422 | 3.439 | 4.768 | 5.127 | 5.625 | 5.473 | 5.808 | 5.127 | 5.625 | 5.473 | 5.808 | ns |
| | | GCLK PLL | $t_{co}$ | 3.898 | 3.841 | 5.355 | 5.880 | 6.341 | 6.161 | 6.543 | 5.880 | 6.341 | 6.161 | 6.543 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.355 | 3.372 | 4.659 | 5.016 | 5.512 | 5.360 | 5.695 | 5.016 | 5.512 | 5.360 | 5.695 | ns |
| | | GCLK PLL | $t_{co}$ | 3.781 | 3.774 | 5.246 | 5.718 | 6.228 | 6.048 | 6.430 | 5.718 | 6.228 | 6.048 | 6.430 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.269 | 3.286 | 4.555 | 4.918 | 5.420 | 5.268 | 5.603 | 4.918 | 5.420 | 5.268 | 5.603 | ns |
| | | GCLK PLL | $t_{co}$ | 3.692 | 3.688 | 5.142 | 5.583 | 6.136 | 5.956 | 6.338 | 5.583 | 6.136 | 5.956 | 6.338 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.262 | 3.279 | 4.538 | 4.890 | 5.379 | 5.227 | 5.562 | 4.890 | 5.379 | 5.227 | 5.562 | ns |
| | | GCLK PLL | $t_{co}$ | 3.685 | 3.681 | 5.125 | 5.555 | 6.095 | 5.915 | 6.297 | 5.555 | 6.095 | 5.915 | 6.297 | ns |


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**Table 1–73.** EP3SL150 Column Pins Output Timing Parameters (Part 2 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.428 | 3.445 | 4.772 | 5.132 | 5.632 | 5.480 | 5.815 | 5.132 | 5.632 | 5.480 | 5.815 | ns |
| | | GCLK PLL | $t_{co}$ | 3.901 | 3.847 | 5.359 | 5.892 | 6.348 | 6.168 | 6.550 | 5.892 | 6.348 | 6.168 | 6.550 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.273 | 3.290 | 4.565 | 4.935 | 5.431 | 5.279 | 5.614 | 4.935 | 5.431 | 5.279 | 5.614 | ns |
| | | GCLK PLL | $t_{co}$ | 3.701 | 3.692 | 5.152 | 5.600 | 6.147 | 5.967 | 6.349 | 5.600 | 6.147 | 5.967 | 6.349 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.280 | 3.297 | 4.559 | 4.914 | 5.405 | 5.253 | 5.588 | 4.914 | 5.405 | 5.253 | 5.588 | ns |
| | | GCLK PLL | $t_{co}$ | 3.703 | 3.699 | 5.146 | 5.579 | 6.121 | 5.941 | 6.323 | 5.579 | 6.121 | 5.941 | 6.323 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.264 | 3.281 | 4.537 | 4.888 | 5.376 | 5.224 | 5.559 | 4.888 | 5.376 | 5.224 | 5.559 | ns |
| | | GCLK PLL | $t_{co}$ | 3.687 | 3.683 | 5.124 | 5.553 | 6.092 | 5.912 | 6.294 | 5.553 | 6.092 | 5.912 | 6.294 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.386 | 3.403 | 4.735 | 5.096 | 5.592 | 5.440 | 5.775 | 5.096 | 5.592 | 5.440 | 5.775 | ns |
| | | GCLK PLL | $t_{co}$ | 3.843 | 3.805 | 5.322 | 5.831 | 6.308 | 6.128 | 6.510 | 5.831 | 6.308 | 6.128 | 6.510 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.275 | 3.292 | 4.605 | 4.962 | 5.455 | 5.303 | 5.637 | 4.962 | 5.455 | 5.303 | 5.637 | ns |
| | | GCLK PLL | $t_{co}$ | 3.713 | 3.694 | 5.192 | 5.659 | 6.170 | 5.991 | 6.371 | 5.659 | 6.170 | 5.991 | 6.371 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.239 | 3.256 | 4.542 | 4.893 | 5.381 | 5.229 | 5.563 | 4.893 | 5.381 | 5.229 | 5.563 | ns |
| | | GCLK PLL | $t_{co}$ | 3.662 | 3.658 | 5.129 | 5.560 | 6.096 | 5.917 | 6.298 | 5.560 | 6.096 | 5.917 | 6.298 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.221 | 3.238 | 4.513 | 4.865 | 5.352 | 5.200 | 5.535 | 4.865 | 5.352 | 5.200 | 5.535 | ns |
| | | GCLK PLL | $t_{co}$ | 3.644 | 3.640 | 5.100 | 5.530 | 6.070 | 5.888 | 6.270 | 5.530 | 6.070 | 5.888 | 6.270 | ns |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.300 | 3.317 | 4.639 | 4.995 | 5.490 | 5.338 | 5.672 | 4.995 | 5.490 | 5.338 | 5.672 | ns |
| | | GCLK PLL | $t_{co}$ | 3.751 | 3.719 | 5.226 | 5.712 | 6.205 | 6.026 | 6.406 | 5.712 | 6.205 | 6.026 | 6.406 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.221 | 3.238 | 4.515 | 4.866 | 5.355 | 5.203 | 5.537 | 4.866 | 5.355 | 5.203 | 5.537 | ns |
| | | GCLK PLL | $t_{co}$ | 3.644 | 3.640 | 5.102 | 5.531 | 6.083 | 5.891 | 6.271 | 5.531 | 6.083 | 5.891 | 6.271 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.216 | 3.233 | 4.508 | 4.859 | 5.346 | 5.194 | 5.529 | 4.859 | 5.346 | 5.194 | 5.529 | ns |
| | | GCLK PLL | $t_{co}$ | 3.639 | 3.635 | 5.095 | 5.524 | 6.062 | 5.882 | 6.264 | 5.524 | 6.062 | 5.882 | 6.264 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.207 | 3.224 | 4.494 | 4.844 | 5.331 | 5.179 | 5.514 | 4.844 | 5.331 | 5.179 | 5.514 | ns |
| | | GCLK PLL | $t_{co}$ | 3.630 | 3.626 | 5.081 | 5.509 | 6.057 | 5.867 | 6.249 | 5.509 | 6.057 | 5.867 | 6.249 | ns |

**Table 1–73.** EP3SL150 Column Pins Output Timing Parameters (Part 3 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.422 | 3.439 | 4.846 | 5.222 | 5.737 | 5.585 | 5.919 | 5.222 | 5.737 | 5.585 | 5.919 | ns |
| | | GCLK PLL | $t_{co}$ | 3.898 | 3.841 | 5.433 | 5.991 | 6.452 | 6.273 | 6.654 | 5.991 | 6.452 | 6.273 | 6.654 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.322 | 3.339 | 4.727 | 5.096 | 5.605 | 5.453 | 5.787 | 5.096 | 5.605 | 5.453 | 5.787 | ns |
| | | GCLK PLL | $t_{co}$ | 3.773 | 3.741 | 5.314 | 5.807 | 6.320 | 6.141 | 6.521 | 5.807 | 6.320 | 6.141 | 6.521 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.278 | 3.295 | 4.640 | 5.006 | 5.509 | 5.357 | 5.692 | 5.006 | 5.509 | 5.357 | 5.692 | ns |
| | | GCLK PLL | $t_{co}$ | 3.701 | 3.697 | 5.227 | 5.671 | 6.225 | 6.045 | 6.427 | 5.671 | 6.225 | 6.045 | 6.427 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.240 | 3.257 | 4.601 | 4.963 | 5.466 | 5.314 | 5.649 | 4.963 | 5.466 | 5.314 | 5.649 | ns |
| | | GCLK PLL | $t_{co}$ | 3.663 | 3.659 | 5.188 | 5.628 | 6.182 | 6.002 | 6.384 | 5.628 | 6.182 | 6.002 | 6.384 | ns |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.613 | 3.630 | 5.167 | 5.582 | 6.141 | 5.989 | 6.324 | 5.582 | 6.141 | 5.989 | 6.324 | ns |
| | | GCLK PLL | $t_{co}$ | 4.161 | 4.032 | 5.754 | 6.474 | 6.857 | 6.677 | 7.059 | 6.474 | 6.857 | 6.677 | 7.059 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.432 | 3.449 | 4.888 | 5.273 | 5.794 | 5.642 | 5.976 | 5.273 | 5.794 | 5.642 | 5.976 | ns |
| | | GCLK PLL | $t_{co}$ | 3.920 | 3.851 | 5.475 | 6.068 | 6.509 | 6.330 | 6.710 | 6.068 | 6.509 | 6.330 | 6.710 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.350 | 3.367 | 4.781 | 5.158 | 5.683 | 5.531 | 5.866 | 5.158 | 5.683 | 5.531 | 5.866 | ns |
| | | GCLK PLL | $t_{co}$ | 3.802 | 3.769 | 5.368 | 5.878 | 6.399 | 6.219 | 6.601 | 5.878 | 6.399 | 6.219 | 6.601 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.330 | 3.347 | 4.723 | 5.105 | 5.617 | 5.465 | 5.800 | 5.105 | 5.617 | 5.465 | 5.800 | ns |
| | | GCLK PLL | $t_{co}$ | 3.753 | 3.749 | 5.310 | 5.780 | 6.333 | 6.153 | 6.535 | 5.780 | 6.333 | 6.153 | 6.535 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.267 | 3.284 | 4.662 | 5.030 | 5.536 | 5.384 | 5.719 | 5.030 | 5.536 | 5.384 | 5.719 | ns |
| | | GCLK PLL | $t_{co}$ | 3.690 | 3.686 | 5.249 | 5.695 | 6.252 | 6.072 | 6.454 | 5.695 | 6.252 | 6.072 | 6.454 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.249 | 3.266 | 4.641 | 5.008 | 5.513 | 5.361 | 5.696 | 5.008 | 5.513 | 5.361 | 5.696 | ns |
| | | GCLK PLL | $t_{co}$ | 3.672 | 3.668 | 5.228 | 5.673 | 6.229 | 6.049 | 6.431 | 5.673 | 6.229 | 6.049 | 6.431 | ns |


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**Table 1–73.** EP3SL150 Column Pins Output Timing Parameters (Part 4 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.559 | 3.576 | 5.096 | 5.515 | 6.079 | 5.927 | 6.262 | 5.515 | 6.079 | 5.927 | 6.262 | ns |
| | | GCLK PLL | $t_{co}$ | 4.069 | 3.978 | 5.683 | 6.384 | 6.795 | 6.615 | 6.997 | 6.384 | 6.795 | 6.615 | 6.997 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.347 | 3.364 | 4.777 | 5.158 | 5.687 | 5.535 | 5.870 | 5.158 | 5.687 | 5.535 | 5.870 | ns |
| | | GCLK PLL | $t_{co}$ | 3.786 | 3.766 | 5.364 | 5.871 | 6.403 | 6.223 | 6.605 | 5.871 | 6.403 | 6.223 | 6.605 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.322 | 3.339 | 4.710 | 5.098 | 5.620 | 5.468 | 5.803 | 5.098 | 5.620 | 5.468 | 5.803 | ns |
| | | GCLK PLL | $t_{co}$ | 3.745 | 3.741 | 5.297 | 5.763 | 6.336 | 6.156 | 6.538 | 5.763 | 6.336 | 6.156 | 6.538 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.311 | 3.328 | 4.693 | 5.073 | 5.600 | 5.448 | 5.783 | 5.073 | 5.600 | 5.448 | 5.783 | ns |
| | | GCLK PLL | $t_{co}$ | 3.734 | 3.730 | 5.280 | 5.742 | 6.316 | 6.136 | 6.518 | 5.742 | 6.316 | 6.136 | 6.518 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.256 | 3.273 | 4.655 | 5.023 | 5.530 | 5.378 | 5.713 | 5.023 | 5.530 | 5.378 | 5.713 | ns |
| | | GCLK PLL | $t_{co}$ | 3.679 | 3.675 | 5.242 | 5.688 | 6.246 | 6.066 | 6.448 | 5.688 | 6.246 | 6.066 | 6.448 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.251 | 3.268 | 4.638 | 5.011 | 5.519 | 5.367 | 5.702 | 5.011 | 5.519 | 5.367 | 5.702 | ns |
| | | GCLK PLL | $t_{co}$ | 3.674 | 3.670 | 5.225 | 5.676 | 6.235 | 6.055 | 6.437 | 5.676 | 6.235 | 6.055 | 6.437 | ns |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.475 | 3.492 | 5.022 | 5.450 | 6.023 | 5.871 | 6.206 | 5.450 | 6.023 | 5.871 | 6.206 | ns |
| | | GCLK PLL | $t_{co}$ | 3.959 | 3.894 | 5.609 | 6.283 | 6.739 | 6.559 | 6.941 | 6.283 | 6.739 | 6.559 | 6.941 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.352 | 3.369 | 4.796 | 5.189 | 5.737 | 5.585 | 5.920 | 5.189 | 5.737 | 5.585 | 5.920 | ns |
| | | GCLK PLL | $t_{co}$ | 3.786 | 3.771 | 5.383 | 5.902 | 6.453 | 6.273 | 6.655 | 5.902 | 6.453 | 6.273 | 6.655 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.314 | 3.331 | 4.704 | 5.099 | 5.624 | 5.472 | 5.807 | 5.099 | 5.624 | 5.472 | 5.807 | ns |
| | | GCLK PLL | $t_{co}$ | 3.737 | 3.733 | 5.291 | 5.764 | 6.340 | 6.160 | 6.542 | 5.764 | 6.340 | 6.160 | 6.542 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.267 | 3.284 | 4.676 | 5.050 | 5.568 | 5.416 | 5.751 | 5.050 | 5.568 | 5.416 | 5.751 | ns |
| | | GCLK PLL | $t_{co}$ | 3.690 | 3.686 | 5.263 | 5.715 | 6.284 | 6.104 | 6.486 | 5.715 | 6.284 | 6.104 | 6.486 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.267 | 3.284 | 4.633 | 4.998 | 5.499 | 5.347 | 5.682 | 4.998 | 5.499 | 5.347 | 5.682 | ns |
| | | GCLK PLL | $t_{co}$ | 3.690 | 3.686 | 5.220 | 5.663 | 6.215 | 6.035 | 6.417 | 5.663 | 6.215 | 6.035 | 6.417 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.264 | 3.281 | 4.630 | 4.994 | 5.495 | 5.343 | 5.678 | 4.994 | 5.495 | 5.343 | 5.678 | ns |
| | | GCLK PLL | $t_{co}$ | 3.687 | 3.683 | 5.217 | 5.659 | 6.211 | 6.031 | 6.413 | 5.659 | 6.211 | 6.031 | 6.413 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.262 | 3.279 | 4.630 | 4.995 | 5.496 | 5.344 | 5.679 | 4.995 | 5.496 | 5.344 | 5.679 | ns |
| | | GCLK PLL | $t_{co}$ | 3.685 | 3.681 | 5.217 | 5.660 | 6.212 | 6.032 | 6.414 | 5.660 | 6.212 | 6.032 | 6.414 | ns |

**Table 1–73.** EP3SL150 Column Pins Output Timing Parameters (Part 5 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.253 | 3.270 | 4.615 | 4.980 | 5.481 | 5.329 | 5.664 | 4.980 | 5.481 | 5.329 | 5.664 | ns |
| | | GCLK PLL | $t_{co}$ | 3.676 | 3.672 | 5.202 | 5.645 | 6.197 | 6.017 | 6.399 | 5.645 | 6.197 | 6.017 | 6.399 | ns |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.274 | 3.291 | 4.645 | 5.012 | 5.515 | 5.363 | 5.698 | 5.012 | 5.515 | 5.363 | 5.698 | ns |
| | | GCLK PLL | $t_{co}$ | 3.697 | 3.693 | 5.232 | 5.677 | 6.231 | 6.051 | 6.433 | 5.677 | 6.231 | 6.051 | 6.433 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.270 | 3.287 | 4.643 | 5.010 | 5.513 | 5.361 | 5.696 | 5.010 | 5.513 | 5.361 | 5.696 | ns |
| | | GCLK PLL | $t_{co}$ | 3.693 | 3.689 | 5.230 | 5.675 | 6.229 | 6.049 | 6.431 | 5.675 | 6.229 | 6.049 | 6.431 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.259 | 3.276 | 4.633 | 5.000 | 5.504 | 5.352 | 5.687 | 5.000 | 5.504 | 5.352 | 5.687 | ns |
| | | GCLK PLL | $t_{co}$ | 3.682 | 3.678 | 5.220 | 5.665 | 6.220 | 6.040 | 6.422 | 5.665 | 6.220 | 6.040 | 6.422 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.248 | 3.265 | 4.620 | 4.987 | 5.491 | 5.339 | 5.674 | 4.987 | 5.491 | 5.339 | 5.674 | ns |
| | | GCLK PLL | $t_{co}$ | 3.671 | 3.667 | 5.207 | 5.652 | 6.207 | 6.027 | 6.409 | 5.652 | 6.207 | 6.027 | 6.409 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.248 | 3.265 | 4.620 | 4.987 | 5.491 | 5.339 | 5.674 | 4.987 | 5.491 | 5.339 | 5.674 | ns |
| | | GCLK PLL | $t_{co}$ | 3.671 | 3.667 | 5.207 | 5.652 | 6.207 | 6.027 | 6.409 | 5.652 | 6.207 | 6.027 | 6.409 | ns |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.254 | 3.271 | 4.619 | 4.984 | 5.486 | 5.334 | 5.669 | 4.984 | 5.486 | 5.334 | 5.669 | ns |
| | | GCLK PLL | $t_{co}$ | 3.677 | 3.673 | 5.206 | 5.649 | 6.202 | 6.022 | 6.404 | 5.649 | 6.202 | 6.022 | 6.404 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.257 | 3.274 | 4.627 | 4.994 | 5.498 | 5.346 | 5.681 | 4.994 | 5.498 | 5.346 | 5.681 | ns |
| | | GCLK PLL | $t_{co}$ | 3.680 | 3.676 | 5.214 | 5.659 | 6.214 | 6.034 | 6.416 | 5.659 | 6.214 | 6.034 | 6.416 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.278 | 3.295 | 4.654 | 5.023 | 5.528 | 5.376 | 5.711 | 5.023 | 5.528 | 5.376 | 5.711 | ns |
| | | GCLK PLL | $t_{co}$ | 3.701 | 3.697 | 5.241 | 5.688 | 6.244 | 6.064 | 6.446 | 5.688 | 6.244 | 6.064 | 6.446 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.264 | 3.281 | 4.644 | 5.013 | 5.519 | 5.367 | 5.702 | 5.013 | 5.519 | 5.367 | 5.702 | ns |
| | | GCLK PLL | $t_{co}$ | 3.687 | 3.683 | 5.231 | 5.678 | 6.235 | 6.055 | 6.437 | 5.678 | 6.235 | 6.055 | 6.437 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.253 | 3.270 | 4.630 | 4.999 | 5.505 | 5.353 | 5.688 | 4.999 | 5.505 | 5.353 | 5.688 | ns |
| | | GCLK PLL | $t_{co}$ | 3.676 | 3.672 | 5.217 | 5.664 | 6.221 | 6.041 | 6.423 | 5.664 | 6.221 | 6.041 | 6.423 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.252 | 3.269 | 4.633 | 5.003 | 5.509 | 5.357 | 5.692 | 5.003 | 5.509 | 5.357 | 5.692 | ns |
| | | GCLK PLL | $t_{co}$ | 3.675 | 3.671 | 5.220 | 5.668 | 6.225 | 6.045 | 6.427 | 5.668 | 6.225 | 6.045 | 6.427 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.249 | 3.266 | 4.628 | 4.997 | 5.503 | 5.351 | 5.686 | 4.997 | 5.503 | 5.351 | 5.686 | ns |
| | | GCLK PLL | $t_{co}$ | 3.672 | 3.668 | 5.215 | 5.662 | 6.219 | 6.039 | 6.421 | 5.662 | 6.219 | 6.039 | 6.421 | ns |

**Table 1–73.** EP3SL150 Column Pins Output Timing Parameters (Part 6 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-15 CLASS II | 8mA | GCLK | $t_{co}$ | 3.251 | 3.268 | 4.617 | 4.983 | 5.486 | 5.334 | 5.669 | 4.983 | 5.486 | 5.334 | 5.669 | ns |
| | | GCLK PLL | $t_{co}$ | 3.674 | 3.670 | 5.204 | 5.648 | 6.202 | 6.022 | 6.404 | 5.648 | 6.202 | 6.022 | 6.404 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.254 | 3.271 | 4.624 | 4.992 | 5.497 | 5.345 | 5.680 | 4.992 | 5.497 | 5.345 | 5.680 | ns |
| | | GCLK PLL | $t_{co}$ | 3.677 | 3.673 | 5.211 | 5.657 | 6.213 | 6.033 | 6.415 | 5.657 | 6.213 | 6.033 | 6.415 | ns |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.261 | 3.278 | 4.619 | 4.983 | 5.484 | 5.332 | 5.667 | 4.983 | 5.484 | 5.332 | 5.667 | ns |
| | | GCLK PLL | $t_{co}$ | 3.684 | 3.680 | 5.206 | 5.648 | 6.200 | 6.020 | 6.402 | 5.648 | 6.200 | 6.020 | 6.402 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.254 | 3.271 | 4.617 | 4.982 | 5.483 | 5.331 | 5.666 | 4.982 | 5.483 | 5.331 | 5.666 | ns |
| | | GCLK PLL | $t_{co}$ | 3.677 | 3.673 | 5.204 | 5.647 | 6.199 | 6.019 | 6.401 | 5.647 | 6.199 | 6.019 | 6.401 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.246 | 3.263 | 4.609 | 4.974 | 5.476 | 5.324 | 5.659 | 4.974 | 5.476 | 5.324 | 5.659 | ns |
| | | GCLK PLL | $t_{co}$ | 3.669 | 3.665 | 5.196 | 5.639 | 6.192 | 6.012 | 6.394 | 5.639 | 6.192 | 6.012 | 6.394 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.249 | 3.266 | 4.612 | 4.978 | 5.480 | 5.328 | 5.663 | 4.978 | 5.480 | 5.328 | 5.663 | ns |
| | | GCLK PLL | $t_{co}$ | 3.672 | 3.668 | 5.199 | 5.643 | 6.196 | 6.016 | 6.398 | 5.643 | 6.196 | 6.016 | 6.398 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.246 | 3.263 | 4.615 | 4.981 | 5.484 | 5.332 | 5.667 | 4.981 | 5.484 | 5.332 | 5.667 | ns |
| | | GCLK PLL | $t_{co}$ | 3.669 | 3.665 | 5.202 | 5.646 | 6.200 | 6.020 | 6.402 | 5.646 | 6.200 | 6.020 | 6.402 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.254 | 3.271 | 4.614 | 4.979 | 5.480 | 5.328 | 5.663 | 4.979 | 5.480 | 5.328 | 5.663 | ns |
| | | GCLK PLL | $t_{co}$ | 3.677 | 3.673 | 5.201 | 5.644 | 6.196 | 6.016 | 6.398 | 5.644 | 6.196 | 6.016 | 6.398 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.266 | 3.283 | 4.627 | 4.993 | 5.495 | 5.343 | 5.678 | 4.993 | 5.495 | 5.343 | 5.678 | ns |
| | | GCLK PLL | $t_{co}$ | 3.689 | 3.685 | 5.214 | 5.658 | 6.211 | 6.031 | 6.413 | 5.658 | 6.211 | 6.031 | 6.413 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.262 | 3.279 | 4.628 | 4.995 | 5.498 | 5.346 | 5.681 | 4.995 | 5.498 | 5.346 | 5.681 | ns |
| | | GCLK PLL | $t_{co}$ | 3.685 | 3.681 | 5.215 | 5.660 | 6.214 | 6.034 | 6.416 | 5.660 | 6.214 | 6.034 | 6.416 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.258 | 3.275 | 4.624 | 4.990 | 5.493 | 5.341 | 5.676 | 4.990 | 5.493 | 5.341 | 5.676 | ns |
| | | GCLK PLL | $t_{co}$ | 3.681 | 3.677 | 5.211 | 5.655 | 6.209 | 6.029 | 6.411 | 5.655 | 6.209 | 6.029 | 6.411 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.251 | 3.268 | 4.617 | 4.983 | 5.486 | 5.334 | 5.669 | 4.983 | 5.486 | 5.334 | 5.669 | ns |
| | | GCLK PLL | $t_{co}$ | 3.674 | 3.670 | 5.204 | 5.648 | 6.202 | 6.022 | 6.404 | 5.648 | 6.202 | 6.022 | 6.404 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.252 | 3.269 | 4.624 | 4.991 | 5.496 | 5.344 | 5.679 | 4.991 | 5.496 | 5.344 | 5.679 | ns |
| | | GCLK PLL | $t_{co}$ | 3.675 | 3.671 | 5.211 | 5.656 | 6.212 | 6.032 | 6.414 | 5.656 | 6.212 | 6.032 | 6.414 | ns |

**Table 1–73.** EP3SL150 Column Pins Output Timing Parameters (Part 7 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.250 | 3.267 | 4.605 | 4.969 | 5.470 | 5.318 | 5.653 | 4.969 | 5.470 | 5.318 | 5.653 | ns |
| | | GCLK PLL | $t_{co}$ | 3.673 | 3.669 | 5.192 | 5.634 | 6.186 | 6.006 | 6.388 | 5.634 | 6.186 | 6.006 | 6.388 | ns |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.269 | 3.286 | 4.641 | 5.010 | 5.516 | 5.364 | 5.699 | 5.010 | 5.516 | 5.364 | 5.699 | ns |
| | | GCLK PLL | $t_{co}$ | 3.692 | 3.688 | 5.228 | 5.675 | 6.232 | 6.052 | 6.434 | 5.675 | 6.232 | 6.052 | 6.434 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.261 | 3.278 | 4.632 | 5.001 | 5.507 | 5.355 | 5.690 | 5.001 | 5.507 | 5.355 | 5.690 | ns |
| | | GCLK PLL | $t_{co}$ | 3.684 | 3.680 | 5.219 | 5.666 | 6.223 | 6.043 | 6.425 | 5.666 | 6.223 | 6.043 | 6.425 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.262 | 3.279 | 4.640 | 5.010 | 5.516 | 5.364 | 5.699 | 5.010 | 5.516 | 5.364 | 5.699 | ns |
| | | GCLK PLL | $t_{co}$ | 3.685 | 3.681 | 5.227 | 5.675 | 6.232 | 6.052 | 6.434 | 5.675 | 6.232 | 6.052 | 6.434 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.251 | 3.268 | 4.627 | 4.996 | 5.502 | 5.350 | 5.685 | 4.996 | 5.502 | 5.350 | 5.685 | ns |
| | | GCLK PLL | $t_{co}$ | 3.674 | 3.670 | 5.214 | 5.661 | 6.218 | 6.038 | 6.420 | 5.661 | 6.218 | 6.038 | 6.420 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.251 | 3.268 | 4.627 | 4.996 | 5.503 | 5.351 | 5.686 | 4.996 | 5.503 | 5.351 | 5.686 | ns |
| | | GCLK PLL | $t_{co}$ | 3.674 | 3.670 | 5.214 | 5.661 | 6.219 | 6.039 | 6.421 | 5.661 | 6.219 | 6.039 | 6.421 | ns |
| 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.272 | 3.289 | 4.643 | 5.011 | 5.516 | 5.364 | 5.699 | 5.011 | 5.516 | 5.364 | 5.699 | ns |
| | | GCLK PLL | $t_{co}$ | 3.695 | 3.691 | 5.230 | 5.676 | 6.233 | 6.052 | 6.434 | 5.676 | 6.233 | 6.052 | 6.434 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.375 | 3.392 | 4.688 | 5.045 | 5.541 | 5.389 | 5.724 | 5.045 | 5.541 | 5.389 | 5.724 | ns |
| | | GCLK PLL | $t_{co}$ | 3.798 | 3.794 | 5.275 | 5.710 | 6.264 | 6.077 | 6.459 | 5.710 | 6.264 | 6.077 | 6.459 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.375 | 3.392 | 4.688 | 5.045 | 5.541 | 5.389 | 5.724 | 5.045 | 5.541 | 5.389 | 5.724 | ns |
| | | GCLK PLL | $t_{co}$ | 3.798 | 3.794 | 5.275 | 5.710 | 6.264 | 6.077 | 6.459 | 5.710 | 6.264 | 6.077 | 6.459 | ns |


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Table 1–74 lists the EP3SL150 row pins output timing parameters for single-ended I/O standards.

**Table 1–74.** EP3SL150 Row Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.214 | 3.466 | 4.819 | 5.204 | 5.693 | 5.566 | 5.831 | 5.325 | 5.817 | 5.689 | 5.913 | ns |
| | | GCLK PLL | $t_{co}$ | 1.420 | 1.606 | 1.985 | 2.065 | 2.256 | 2.277 | 2.285 | 2.167 | 2.360 | 2.380 | 2.277 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.121 | 3.361 | 4.689 | 5.066 | 5.548 | 5.421 | 5.686 | 5.184 | 5.668 | 5.540 | 5.764 | ns |
| | | GCLK PLL | $t_{co}$ | 1.354 | 1.535 | 1.875 | 1.954 | 2.142 | 2.163 | 2.171 | 2.054 | 2.245 | 2.265 | 2.162 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.042 | 3.271 | 4.570 | 4.943 | 5.420 | 5.293 | 5.558 | 5.057 | 5.536 | 5.408 | 5.632 | ns |
| | | GCLK PLL | $t_{co}$ | 1.275 | 1.446 | 1.769 | 1.854 | 2.046 | 2.067 | 2.075 | 1.955 | 2.145 | 2.165 | 2.062 | ns |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.224 | 3.470 | 4.827 | 5.209 | 5.697 | 5.570 | 5.835 | 5.331 | 5.821 | 5.693 | 5.917 | ns |
| | | GCLK PLL | $t_{co}$ | 1.422 | 1.613 | 1.989 | 2.071 | 2.265 | 2.286 | 2.294 | 2.175 | 2.372 | 2.392 | 2.289 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.046 | 3.275 | 4.576 | 4.949 | 5.427 | 5.301 | 5.564 | 5.063 | 5.543 | 5.417 | 5.639 | ns |
| | | GCLK PLL | $t_{co}$ | 1.279 | 1.450 | 1.780 | 1.869 | 2.056 | 2.077 | 2.085 | 1.967 | 2.154 | 2.174 | 2.071 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.168 | 3.412 | 4.771 | 5.157 | 5.649 | 5.522 | 5.787 | 5.282 | 5.775 | 5.647 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.381 | 1.567 | 1.952 | 2.034 | 2.222 | 2.243 | 2.251 | 2.135 | 2.326 | 2.346 | 2.243 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.047 | 3.285 | 4.618 | 4.998 | 5.485 | 5.358 | 5.623 | 5.120 | 5.611 | 5.482 | 5.706 | ns |
| | | GCLK PLL | $t_{co}$ | 1.280 | 1.455 | 1.815 | 1.892 | 2.077 | 2.098 | 2.106 | 1.993 | 2.181 | 2.200 | 2.097 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.010 | 3.242 | 4.536 | 4.915 | 5.397 | 5.270 | 5.535 | 5.034 | 5.518 | 5.389 | 5.613 | ns |
| | | GCLK PLL | $t_{co}$ | 1.243 | 1.417 | 1.755 | 1.827 | 2.007 | 2.028 | 2.036 | 1.925 | 2.107 | 2.127 | 2.024 | ns |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.082 | 3.331 | 4.665 | 5.050 | 5.539 | 5.412 | 5.677 | 5.174 | 5.664 | 5.535 | 5.759 | ns |
| | | GCLK PLL | $t_{co}$ | 1.302 | 1.479 | 1.850 | 1.927 | 2.113 | 2.134 | 2.142 | 2.026 | 2.217 | 2.236 | 2.133 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.997 | 3.226 | 4.502 | 4.876 | 5.358 | 5.231 | 5.496 | 4.994 | 5.478 | 5.349 | 5.573 | ns |
| | | GCLK PLL | $t_{co}$ | 1.230 | 1.401 | 1.727 | 1.798 | 1.979 | 2.000 | 2.008 | 1.895 | 2.079 | 2.098 | 1.995 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.194 | 3.448 | 4.903 | 5.311 | 5.821 | 5.694 | 5.959 | 5.442 | 5.954 | 5.825 | 6.049 | ns |
| | | GCLK PLL | $t_{co}$ | 1.407 | 1.604 | 2.060 | 2.160 | 2.367 | 2.388 | 2.396 | 2.267 | 2.478 | 2.498 | 2.395 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.089 | 3.350 | 4.748 | 5.148 | 5.651 | 5.524 | 5.789 | 5.275 | 5.780 | 5.651 | 5.875 | ns |
| | | GCLK PLL | $t_{co}$ | 1.322 | 1.501 | 1.936 | 2.025 | 2.225 | 2.246 | 2.254 | 2.130 | 2.334 | 2.353 | 2.250 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.038 | 3.282 | 4.637 | 5.029 | 5.525 | 5.398 | 5.663 | 5.152 | 5.650 | 5.521 | 5.745 | ns |
| | | GCLK PLL | $t_{co}$ | 1.265 | 1.457 | 1.852 | 1.939 | 2.134 | 2.155 | 2.163 | 2.041 | 2.239 | 2.259 | 2.156 | ns |

**Table 1–74.** EP3SL150 Row Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.431 | 3.699 | 5.291 | 5.740 | 6.296 | 6.169 | 6.434 | 5.882 | 6.438 | 6.310 | 6.534 | ns |
| | | GCLK PLL | $t_{co}$ | 1.655 | 1.850 | 2.491 | 2.527 | 2.770 | 2.796 | 2.799 | 2.776 | 2.888 | 2.913 | 2.805 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.206 | 3.497 | 4.964 | 5.371 | 5.891 | 5.764 | 6.029 | 5.517 | 6.032 | 5.903 | 6.127 | ns |
| | | GCLK PLL | $t_{co}$ | 1.430 | 1.648 | 2.164 | 2.201 | 2.410 | 2.436 | 2.439 | 2.411 | 2.527 | 2.551 | 2.443 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.141 | 3.395 | 4.811 | 5.221 | 5.732 | 5.605 | 5.870 | 5.349 | 5.859 | 5.731 | 5.955 | ns |
| | | GCLK PLL | $t_{co}$ | 1.365 | 1.546 | 2.011 | 2.096 | 2.310 | 2.336 | 2.339 | 2.243 | 2.421 | 2.446 | 2.338 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.081 | 3.321 | 4.734 | 5.127 | 5.635 | 5.508 | 5.773 | 5.254 | 5.765 | 5.637 | 5.861 | ns |
| | | GCLK PLL | $t_{co}$ | 1.327 | 1.508 | 1.937 | 2.043 | 2.244 | 2.270 | 2.273 | 2.148 | 2.349 | 2.374 | 2.266 | ns |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.342 | 3.617 | 5.201 | 5.653 | 6.224 | 6.097 | 6.362 | 5.789 | 6.362 | 6.234 | 6.458 | ns |
| | | GCLK PLL | $t_{co}$ | 1.566 | 1.768 | 2.401 | 2.454 | 2.707 | 2.733 | 2.736 | 2.683 | 2.823 | 2.848 | 2.740 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.100 | 3.359 | 4.796 | 5.216 | 5.733 | 5.606 | 5.871 | 5.343 | 5.858 | 5.730 | 5.954 | ns |
| | | GCLK PLL | $t_{co}$ | 1.343 | 1.525 | 1.996 | 2.096 | 2.313 | 2.339 | 2.342 | 2.237 | 2.422 | 2.447 | 2.339 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.073 | 3.312 | 4.723 | 5.120 | 5.627 | 5.502 | 5.765 | 5.245 | 5.753 | 5.625 | 5.849 | ns |
| | | GCLK PLL | $t_{co}$ | 1.316 | 1.499 | 1.923 | 2.035 | 2.244 | 2.270 | 2.273 | 2.139 | 2.349 | 2.374 | 2.266 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.064 | 3.303 | 4.701 | 5.102 | 5.608 | 5.483 | 5.746 | 5.227 | 5.731 | 5.606 | 5.827 | ns |
| | | GCLK PLL | $t_{co}$ | 1.297 | 1.488 | 1.905 | 2.010 | 2.225 | 2.251 | 2.254 | 2.121 | 2.330 | 2.355 | 2.247 | ns |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.285 | 3.542 | 5.111 | 5.567 | 6.149 | 6.022 | 6.287 | 5.701 | 6.278 | 6.150 | 6.374 | ns |
| | | GCLK PLL | $t_{co}$ | 1.509 | 1.693 | 2.311 | 2.386 | 2.646 | 2.672 | 2.675 | 2.595 | 2.754 | 2.779 | 2.671 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.105 | 3.353 | 4.818 | 5.244 | 5.774 | 5.647 | 5.912 | 5.368 | 5.900 | 5.772 | 5.996 | ns |
| | | GCLK PLL | $t_{co}$ | 1.348 | 1.529 | 2.018 | 2.124 | 2.361 | 2.387 | 2.390 | 2.262 | 2.466 | 2.491 | 2.383 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.036 | 3.270 | 4.620 | 5.004 | 5.495 | 5.369 | 5.631 | 5.123 | 5.614 | 5.488 | 5.708 | ns |
| | | GCLK PLL | $t_{co}$ | 1.269 | 1.445 | 1.845 | 1.930 | 2.124 | 2.145 | 2.153 | 2.028 | 2.225 | 2.245 | 2.142 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.031 | 3.266 | 4.617 | 5.002 | 5.493 | 5.367 | 5.628 | 5.122 | 5.613 | 5.487 | 5.706 | ns |
| | | GCLK PLL | $t_{co}$ | 1.264 | 1.441 | 1.842 | 1.928 | 2.122 | 2.143 | 2.151 | 2.027 | 2.224 | 2.244 | 2.141 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.022 | 3.255 | 4.602 | 4.986 | 5.476 | 5.350 | 5.611 | 5.105 | 5.595 | 5.469 | 5.688 | ns |
| | | GCLK PLL | $t_{co}$ | 1.255 | 1.430 | 1.827 | 1.912 | 2.105 | 2.126 | 2.134 | 2.010 | 2.206 | 2.226 | 2.123 | ns |


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**Table 1–74.** EP3SL150 Row Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.042 | 3.277 | 4.629 | 5.031 | 5.512 | 5.397 | 5.647 | 5.135 | 5.631 | 5.516 | 5.724 | ns |
| | | GCLK PLL | $t_{co}$ | 1.276 | 1.452 | 1.856 | 1.947 | 2.139 | 2.165 | 2.168 | 2.041 | 2.240 | 2.265 | 2.157 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.027 | 3.263 | 4.626 | 5.030 | 5.511 | 5.396 | 5.646 | 5.133 | 5.629 | 5.514 | 5.722 | ns |
| | | GCLK PLL | $t_{co}$ | 1.271 | 1.447 | 1.854 | 1.946 | 2.138 | 2.164 | 2.167 | 2.039 | 2.238 | 2.263 | 2.155 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.016 | 3.251 | 4.609 | 5.020 | 5.501 | 5.386 | 5.636 | 5.116 | 5.620 | 5.505 | 5.713 | ns |
| | | GCLK PLL | $t_{co}$ | 1.260 | 1.436 | 1.844 | 1.936 | 2.128 | 2.154 | 2.157 | 2.030 | 2.229 | 2.254 | 2.146 | ns |
| | 10mA | GCLK | $t_{co}$ | 2.992 | 3.228 | 4.593 | 5.007 | 5.488 | 5.373 | 5.623 | 5.101 | 5.608 | 5.493 | 5.701 | ns |
| | | GCLK PLL | $t_{co}$ | 1.249 | 1.425 | 1.831 | 1.923 | 2.115 | 2.141 | 2.144 | 2.018 | 2.217 | 2.242 | 2.134 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.992 | 3.227 | 4.592 | 5.007 | 5.488 | 5.373 | 5.623 | 5.100 | 5.608 | 5.493 | 5.701 | ns |
| | | GCLK PLL | $t_{co}$ | 1.249 | 1.424 | 1.831 | 1.923 | 2.115 | 2.141 | 2.144 | 2.017 | 2.217 | 2.242 | 2.134 | ns |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.002 | 3.236 | 4.590 | 5.004 | 5.483 | 5.368 | 5.618 | 5.095 | 5.602 | 5.487 | 5.695 | ns |
| | | GCLK PLL | $t_{co}$ | 1.257 | 1.431 | 1.830 | 1.920 | 2.110 | 2.136 | 2.139 | 2.013 | 2.211 | 2.236 | 2.128 | ns |
| | 16mA | GCLK | $t_{co}$ | 2.996 | 3.231 | 4.589 | 5.012 | 5.493 | 5.378 | 5.628 | 5.097 | 5.613 | 5.498 | 5.706 | ns |
| | | GCLK PLL | $t_{co}$ | 1.258 | 1.434 | 1.836 | 1.928 | 2.120 | 2.146 | 2.149 | 2.022 | 2.222 | 2.247 | 2.139 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.038 | 3.273 | 4.640 | 5.042 | 5.526 | 5.410 | 5.664 | 5.148 | 5.644 | 5.528 | 5.740 | ns |
| | | GCLK PLL | $t_{co}$ | 1.279 | 1.455 | 1.865 | 1.958 | 2.152 | 2.178 | 2.181 | 2.051 | 2.252 | 2.277 | 2.169 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.015 | 3.251 | 4.622 | 5.032 | 5.515 | 5.400 | 5.650 | 5.132 | 5.634 | 5.519 | 5.727 | ns |
| | | GCLK PLL | $t_{co}$ | 1.265 | 1.441 | 1.854 | 1.948 | 2.142 | 2.168 | 2.171 | 2.042 | 2.243 | 2.268 | 2.160 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.998 | 3.234 | 4.605 | 5.019 | 5.502 | 5.387 | 5.637 | 5.114 | 5.621 | 5.506 | 5.714 | ns |
| | | GCLK PLL | $t_{co}$ | 1.254 | 1.429 | 1.841 | 1.935 | 2.129 | 2.155 | 2.158 | 2.029 | 2.230 | 2.255 | 2.147 | ns |

**Table 1–74.** EP3SL150 Row Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.017 | 3.249 | 4.596 | 5.002 | 5.481 | 5.366 | 5.616 | 5.099 | 5.599 | 5.484 | 5.692 | ns |
| | | GCLK PLL | $t_{co}$ | 1.264 | 1.437 | 1.829 | 1.918 | 2.108 | 2.134 | 2.137 | 2.012 | 2.208 | 2.233 | 2.125 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.005 | 3.237 | 4.587 | 5.001 | 5.480 | 5.365 | 5.615 | 5.091 | 5.599 | 5.484 | 5.692 | ns |
| | | GCLK PLL | $t_{co}$ | 1.257 | 1.431 | 1.827 | 1.917 | 2.107 | 2.133 | 2.136 | 2.011 | 2.208 | 2.233 | 2.125 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.992 | 3.225 | 4.578 | 4.994 | 5.473 | 5.358 | 5.608 | 5.083 | 5.592 | 5.477 | 5.685 | ns |
| | | GCLK PLL | $t_{co}$ | 1.248 | 1.423 | 1.820 | 1.910 | 2.100 | 2.126 | 2.129 | 2.004 | 2.201 | 2.226 | 2.118 | ns |
| | 10mA | GCLK | $t_{co}$ | 2.994 | 3.227 | 4.581 | 4.997 | 5.477 | 5.362 | 5.612 | 5.086 | 5.595 | 5.480 | 5.688 | ns |
| | | GCLK PLL | $t_{co}$ | 1.251 | 1.425 | 1.823 | 1.913 | 2.104 | 2.130 | 2.133 | 2.007 | 2.204 | 2.229 | 2.121 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.987 | 3.222 | 4.579 | 5.000 | 5.480 | 5.365 | 5.615 | 5.086 | 5.600 | 5.485 | 5.693 | ns |
| | | GCLK PLL | $t_{co}$ | 1.247 | 1.422 | 1.825 | 1.916 | 2.107 | 2.133 | 2.136 | 2.010 | 2.209 | 2.234 | 2.126 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 2.993 | 3.226 | 4.574 | 4.997 | 5.476 | 5.361 | 5.611 | 5.077 | 5.594 | 5.479 | 5.687 | ns |
| | | GCLK PLL | $t_{co}$ | 1.255 | 1.430 | 1.823 | 1.913 | 2.103 | 2.129 | 2.132 | 2.006 | 2.203 | 2.228 | 2.120 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.024 | 3.256 | 4.607 | 5.012 | 5.492 | 5.377 | 5.627 | 5.111 | 5.610 | 5.495 | 5.703 | ns |
| | | GCLK PLL | $t_{co}$ | 1.270 | 1.443 | 1.838 | 1.928 | 2.119 | 2.145 | 2.148 | 2.021 | 2.219 | 2.244 | 2.136 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.012 | 3.246 | 4.603 | 5.014 | 5.494 | 5.379 | 5.629 | 5.108 | 5.613 | 5.498 | 5.706 | ns |
| | | GCLK PLL | $t_{co}$ | 1.264 | 1.438 | 1.839 | 1.930 | 2.121 | 2.147 | 2.150 | 2.023 | 2.222 | 2.247 | 2.139 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.008 | 3.241 | 4.597 | 5.009 | 5.489 | 5.374 | 5.624 | 5.102 | 5.607 | 5.492 | 5.700 | ns |
| | | GCLK PLL | $t_{co}$ | 1.260 | 1.434 | 1.834 | 1.925 | 2.116 | 2.142 | 2.145 | 2.018 | 2.216 | 2.241 | 2.133 | ns |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.023 | 3.255 | 4.618 | 5.028 | 5.511 | 5.396 | 5.646 | 5.125 | 5.629 | 5.514 | 5.722 | ns |
| | | GCLK PLL | $t_{co}$ | 1.272 | 1.445 | 1.851 | 1.944 | 2.138 | 2.164 | 2.167 | 2.037 | 2.238 | 2.263 | 2.155 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.011 | 3.243 | 4.607 | 5.019 | 5.502 | 5.387 | 5.637 | 5.114 | 5.620 | 5.505 | 5.713 | ns |
| | | GCLK PLL | $t_{co}$ | 1.263 | 1.437 | 1.842 | 1.935 | 2.129 | 2.155 | 2.158 | 2.028 | 2.229 | 2.254 | 2.146 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.007 | 3.241 | 4.611 | 5.027 | 5.511 | 5.396 | 5.646 | 5.120 | 5.630 | 5.515 | 5.723 | ns |
| | | GCLK PLL | $t_{co}$ | 1.262 | 1.437 | 1.849 | 1.943 | 2.138 | 2.164 | 2.167 | 2.037 | 2.239 | 2.264 | 2.156 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.142 | 3.376 | 4.672 | 5.050 | 5.535 | 5.409 | 5.670 | 5.171 | 5.656 | 5.530 | 5.749 | ns |
| | | GCLK PLL | $t_{co}$ | 1.375 | 1.551 | 1.897 | 1.976 | 2.164 | 2.185 | 2.193 | 2.076 | 2.267 | 2.287 | 2.184 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.142 | 3.376 | 4.672 | 5.050 | 5.535 | 5.409 | 5.670 | 5.171 | 5.656 | 5.530 | 5.749 | ns |
| | | GCLK PLL | $t_{co}$ | 1.375 | 1.551 | 1.897 | 1.976 | 2.164 | 2.185 | 2.193 | 2.076 | 2.267 | 2.287 | 2.184 | ns |


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Table 1–75 through Table 1–75 list the maximum I/O timing parameters for EP3SL150 devices for differential I/O standards.

Table 1–75 lists the EP3SL150 column pins input timing parameters for differential I/O standards.

**Table 1–75.** EP3SL150 Column Pins Input Timing Parameters (Part 1 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -0.978 | -1.006 | -1.151 | -1.135 | -1.286 | -1.233 | -1.594 | -1.098 | -1.339 | -1.193 | -1.632 | ns |
| | | $t_h$ | 1.104 | 1.152 | 1.371 | 1.387 | 1.564 | 1.502 | 1.860 | 1.361 | 1.634 | 1.471 | 1.898 | ns |
| | GCLK PLL | $t_{su}$ | 0.967 | 1.001 | 1.885 | 2.230 | 2.404 | 2.293 | 2.197 | 2.284 | 2.556 | 2.353 | 2.249 | ns |
| | | $t_h$ | -0.707 | -0.719 | -1.450 | -1.735 | -1.855 | -1.769 | -1.669 | -1.780 | -1.984 | -1.818 | -1.718 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -0.978 | -1.006 | -1.151 | -1.135 | -1.286 | -1.233 | -1.594 | -1.098 | -1.339 | -1.193 | -1.632 | ns |
| | | $t_h$ | 1.104 | 1.152 | 1.371 | 1.387 | 1.564 | 1.502 | 1.860 | 1.361 | 1.634 | 1.471 | 1.898 | ns |
| | GCLK PLL | $t_{su}$ | 0.967 | 1.001 | 1.885 | 2.230 | 2.404 | 2.293 | 2.197 | 2.284 | 2.556 | 2.353 | 2.249 | ns |
| | | $t_h$ | -0.707 | -0.719 | -1.450 | -1.735 | -1.855 | -1.769 | -1.669 | -1.780 | -1.984 | -1.818 | -1.718 | ns |
| RSDS | GCLK | $t_{su}$ | -0.978 | -1.006 | -1.151 | -1.135 | -1.286 | -1.233 | -1.594 | -1.098 | -1.339 | -1.193 | -1.632 | ns |
| | | $t_h$ | 1.104 | 1.152 | 1.371 | 1.387 | 1.564 | 1.502 | 1.860 | 1.361 | 1.634 | 1.471 | 1.898 | ns |
| | GCLK PLL | $t_{su}$ | 0.967 | 1.001 | 1.885 | 2.230 | 2.404 | 2.293 | 2.197 | 2.284 | 2.556 | 2.353 | 2.249 | ns |
| | | $t_h$ | -0.707 | -0.719 | -1.450 | -1.735 | -1.855 | -1.769 | -1.669 | -1.780 | -1.984 | -1.818 | -1.718 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.794 | -0.829 | -1.228 | -1.334 | -1.445 | -1.387 | -1.743 | -1.333 | -1.443 | -1.391 | -1.786 | ns |
| | | $t_h$ | 0.913 | 0.967 | 1.416 | 1.546 | 1.677 | 1.610 | 1.964 | 1.554 | 1.684 | 1.621 | 2.007 | ns |
| | GCLK PLL | $t_{su}$ | 1.151 | 1.178 | 1.808 | 2.031 | 2.245 | 2.139 | 2.048 | 2.049 | 2.266 | 2.155 | 2.095 | ns |
| | | $t_h$ | -0.898 | -0.904 | -1.405 | -1.576 | -1.742 | -1.661 | -1.565 | -1.587 | -1.753 | -1.668 | -1.609 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.794 | -0.829 | -1.228 | -1.334 | -1.445 | -1.387 | -1.743 | -1.333 | -1.443 | -1.391 | -1.786 | ns |
| | | $t_h$ | 0.913 | 0.967 | 1.416 | 1.546 | 1.677 | 1.610 | 1.964 | 1.554 | 1.684 | 1.621 | 2.007 | ns |
| | GCLK PLL | $t_{su}$ | 1.151 | 1.178 | 1.808 | 2.031 | 2.245 | 2.139 | 2.048 | 2.049 | 2.266 | 2.155 | 2.095 | ns |
| | | $t_h$ | -0.898 | -0.904 | -1.405 | -1.576 | -1.742 | -1.661 | -1.565 | -1.587 | -1.753 | -1.668 | -1.609 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.802 | -0.841 | -1.238 | -1.345 | -1.461 | -1.403 | -1.759 | -1.344 | -1.458 | -1.406 | -1.801 | ns |
| | | $t_h$ | 0.921 | 0.979 | 1.426 | 1.557 | 1.693 | 1.626 | 1.980 | 1.565 | 1.699 | 1.636 | 2.022 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.166 | 1.798 | 2.020 | 2.229 | 2.123 | 2.032 | 2.038 | 2.251 | 2.140 | 2.080 | ns |
| | | $t_h$ | -0.890 | -0.892 | -1.395 | -1.565 | -1.726 | -1.645 | -1.549 | -1.576 | -1.738 | -1.653 | -1.594 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.802 | -0.841 | -1.238 | -1.345 | -1.461 | -1.403 | -1.759 | -1.344 | -1.458 | -1.406 | -1.801 | ns |
| | | $t_h$ | 0.921 | 0.979 | 1.426 | 1.557 | 1.693 | 1.626 | 1.980 | 1.565 | 1.699 | 1.636 | 2.022 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.166 | 1.798 | 2.020 | 2.229 | 2.123 | 2.032 | 2.038 | 2.251 | 2.140 | 2.080 | ns |
| | | $t_h$ | -0.890 | -0.892 | -1.395 | -1.565 | -1.726 | -1.645 | -1.549 | -1.576 | -1.738 | -1.653 | -1.594 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.814 | -0.852 | -1.247 | -1.356 | -1.480 | -1.422 | -1.778 | -1.355 | -1.476 | -1.424 | -1.819 | ns |
| | | $t_h$ | 0.933 | 0.990 | 1.436 | 1.568 | 1.712 | 1.645 | 1.999 | 1.576 | 1.717 | 1.654 | 2.040 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.155 | 1.789 | 2.009 | 2.210 | 2.104 | 2.013 | 2.027 | 2.233 | 2.122 | 2.062 | ns |
| | | $t_h$ | -0.878 | -0.881 | -1.385 | -1.554 | -1.707 | -1.626 | -1.530 | -1.565 | -1.720 | -1.635 | -1.576 | ns |

**Table 1–75.** EP3SL150 Column Pins Input Timing Parameters (Part 2 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.814 | -0.852 | -1.247 | -1.356 | -1.480 | -1.422 | -1.778 | -1.355 | -1.476 | -1.424 | -1.819 | ns |
| | | $t_h$ | 0.933 | 0.990 | 1.436 | 1.568 | 1.712 | 1.645 | 1.999 | 1.576 | 1.717 | 1.654 | 2.040 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.155 | 1.789 | 2.009 | 2.210 | 2.104 | 2.013 | 2.027 | 2.233 | 2.122 | 2.062 | ns |
| | | $t_h$ | -0.878 | -0.881 | -1.385 | -1.554 | -1.707 | -1.626 | -1.530 | -1.565 | -1.720 | -1.635 | -1.576 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.802 | -0.841 | -1.238 | -1.345 | -1.461 | -1.403 | -1.759 | -1.344 | -1.458 | -1.406 | -1.801 | ns |
| | | $t_h$ | 0.921 | 0.979 | 1.426 | 1.557 | 1.693 | 1.626 | 1.980 | 1.565 | 1.699 | 1.636 | 2.022 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.166 | 1.798 | 2.020 | 2.229 | 2.123 | 2.032 | 2.038 | 2.251 | 2.140 | 2.080 | ns |
| | | $t_h$ | -0.890 | -0.892 | -1.395 | -1.565 | -1.726 | -1.645 | -1.549 | -1.576 | -1.738 | -1.653 | -1.594 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.802 | -0.841 | -1.238 | -1.345 | -1.461 | -1.403 | -1.759 | -1.344 | -1.458 | -1.406 | -1.801 | ns |
| | | $t_h$ | 0.921 | 0.979 | 1.426 | 1.557 | 1.693 | 1.626 | 1.980 | 1.565 | 1.699 | 1.636 | 2.022 | ns |
| | GCLK PLL | $t_{su}$ | 1.143 | 1.166 | 1.798 | 2.020 | 2.229 | 2.123 | 2.032 | 2.038 | 2.251 | 2.140 | 2.080 | ns |
| | | $t_h$ | -0.890 | -0.892 | -1.395 | -1.565 | -1.726 | -1.645 | -1.549 | -1.576 | -1.738 | -1.653 | -1.594 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -0.814 | -0.852 | -1.247 | -1.356 | -1.480 | -1.422 | -1.778 | -1.355 | -1.476 | -1.424 | -1.819 | ns |
| | | $t_h$ | 0.933 | 0.990 | 1.436 | 1.568 | 1.712 | 1.645 | 1.999 | 1.576 | 1.717 | 1.654 | 2.040 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.155 | 1.789 | 2.009 | 2.210 | 2.104 | 2.013 | 2.027 | 2.233 | 2.122 | 2.062 | ns |
| | | $t_h$ | -0.878 | -0.881 | -1.385 | -1.554 | -1.707 | -1.626 | -1.530 | -1.565 | -1.720 | -1.635 | -1.576 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -0.814 | -0.852 | -1.247 | -1.356 | -1.480 | -1.422 | -1.778 | -1.355 | -1.476 | -1.424 | -1.819 | ns |
| | | $t_h$ | 0.933 | 0.990 | 1.436 | 1.568 | 1.712 | 1.645 | 1.999 | 1.576 | 1.717 | 1.654 | 2.040 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.155 | 1.789 | 2.009 | 2.210 | 2.104 | 2.013 | 2.027 | 2.233 | 2.122 | 2.062 | ns |
| | | $t_h$ | -0.878 | -0.881 | -1.385 | -1.554 | -1.707 | -1.626 | -1.530 | -1.565 | -1.720 | -1.635 | -1.576 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.821 | -0.858 | -1.259 | -1.361 | -1.480 | -1.424 | -1.777 | -1.359 | -1.471 | -1.422 | -1.815 | ns |
| | | $t_h$ | 0.940 | 0.996 | 1.449 | 1.576 | 1.715 | 1.648 | 2.003 | 1.583 | 1.717 | 1.653 | 2.041 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.149 | 1.777 | 2.004 | 2.210 | 2.102 | 2.014 | 2.023 | 2.238 | 2.124 | 2.066 | ns |
| | | $t_h$ | -0.871 | -0.875 | -1.372 | -1.546 | -1.704 | -1.623 | -1.526 | -1.558 | -1.720 | -1.636 | -1.575 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.821 | -0.858 | -1.259 | -1.361 | -1.480 | -1.424 | -1.777 | -1.359 | -1.471 | -1.422 | -1.815 | ns |
| | | $t_h$ | 0.940 | 0.996 | 1.449 | 1.576 | 1.715 | 1.648 | 2.003 | 1.583 | 1.717 | 1.653 | 2.041 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.149 | 1.777 | 2.004 | 2.210 | 2.102 | 2.014 | 2.023 | 2.238 | 2.124 | 2.066 | ns |
| | | $t_h$ | -0.871 | -0.875 | -1.372 | -1.546 | -1.704 | -1.623 | -1.526 | -1.558 | -1.720 | -1.636 | -1.575 | ns |


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Table 1–76 lists the EP3SL150 row pins input timing parameters for differential I/O standards.

**Table 1–76.** EP3SL150 Row Pins Input Timing Parameters (Part 1 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -0.919 | -0.950 | -1.021 | -0.981 | -1.115 | -1.070 | -1.404 | -0.940 | -1.066 | -1.023 | -1.442 | ns |
| | | $t_h$ | 1.043 | 1.092 | 1.245 | 1.237 | 1.395 | 1.339 | 1.672 | 1.207 | 1.358 | 1.303 | 1.711 | ns |
| | GCLK PLL | $t_{su}$ | 0.959 | 0.987 | 1.949 | 2.324 | 2.527 | 2.403 | 2.334 | 2.384 | 2.597 | 2.470 | 2.387 | ns |
| | | $t_h$ | -0.698 | -0.708 | -1.513 | -1.828 | -1.977 | -1.881 | -1.804 | -1.875 | -2.032 | -1.933 | -1.853 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -0.919 | -0.950 | -1.021 | -0.981 | -1.115 | -1.070 | -1.404 | -0.940 | -1.066 | -1.023 | -1.442 | ns |
| | | $t_h$ | 1.043 | 1.092 | 1.245 | 1.237 | 1.395 | 1.339 | 1.672 | 1.207 | 1.358 | 1.303 | 1.711 | ns |
| | GCLK PLL | $t_{su}$ | 0.959 | 0.987 | 1.949 | 2.324 | 2.527 | 2.403 | 2.334 | 2.384 | 2.597 | 2.470 | 2.387 | ns |
| | | $t_h$ | -0.698 | -0.708 | -1.513 | -1.828 | -1.977 | -1.881 | -1.804 | -1.875 | -2.032 | -1.933 | -1.853 | ns |
| RSDS | GCLK | $t_{su}$ | -0.919 | -0.950 | -1.021 | -0.981 | -1.115 | -1.070 | -1.404 | -0.940 | -1.066 | -1.023 | -1.442 | ns |
| | | $t_h$ | 1.043 | 1.092 | 1.245 | 1.237 | 1.395 | 1.339 | 1.672 | 1.207 | 1.358 | 1.303 | 1.711 | ns |
| | GCLK PLL | $t_{su}$ | 0.959 | 0.987 | 1.949 | 2.324 | 2.527 | 2.403 | 2.334 | 2.384 | 2.597 | 2.470 | 2.387 | ns |
| | | $t_h$ | -0.698 | -0.708 | -1.513 | -1.828 | -1.977 | -1.881 | -1.804 | -1.875 | -2.032 | -1.933 | -1.853 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.724 | -0.765 | -1.113 | -1.210 | -1.304 | -1.254 | -1.583 | -1.211 | -1.303 | -1.255 | -1.626 | ns |
| | | $t_h$ | 0.841 | 0.898 | 1.302 | 1.420 | 1.535 | 1.474 | 1.802 | 1.429 | 1.543 | 1.483 | 1.846 | ns |
| | GCLK PLL | $t_{su}$ | 1.154 | 1.172 | 1.862 | 2.100 | 2.338 | 2.219 | 2.155 | 2.117 | 2.360 | 2.238 | 2.203 | ns |
| | | $t_h$ | -0.900 | -0.902 | -1.458 | -1.649 | -1.837 | -1.746 | -1.674 | -1.657 | -1.847 | -1.753 | -1.718 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.724 | -0.765 | -1.113 | -1.210 | -1.304 | -1.254 | -1.583 | -1.211 | -1.303 | -1.255 | -1.626 | ns |
| | | $t_h$ | 0.841 | 0.898 | 1.302 | 1.420 | 1.535 | 1.474 | 1.802 | 1.429 | 1.543 | 1.483 | 1.846 | ns |
| | GCLK PLL | $t_{su}$ | 1.154 | 1.172 | 1.862 | 2.100 | 2.338 | 2.219 | 2.155 | 2.117 | 2.360 | 2.238 | 2.203 | ns |
| | | $t_h$ | -0.900 | -0.902 | -1.458 | -1.649 | -1.837 | -1.746 | -1.674 | -1.657 | -1.847 | -1.753 | -1.718 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.733 | -0.777 | -1.122 | -1.220 | -1.320 | -1.270 | -1.599 | -1.220 | -1.319 | -1.271 | -1.642 | ns |
| | | $t_h$ | 0.850 | 0.910 | 1.311 | 1.430 | 1.551 | 1.490 | 1.818 | 1.438 | 1.559 | 1.499 | 1.862 | ns |
| | GCLK PLL | $t_{su}$ | 1.145 | 1.160 | 1.853 | 2.090 | 2.322 | 2.203 | 2.139 | 2.108 | 2.344 | 2.222 | 2.187 | ns |
| | | $t_h$ | -0.891 | -0.890 | -1.449 | -1.639 | -1.821 | -1.730 | -1.658 | -1.648 | -1.831 | -1.737 | -1.702 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.733 | -0.777 | -1.122 | -1.220 | -1.320 | -1.270 | -1.599 | -1.220 | -1.319 | -1.271 | -1.642 | ns |
| | | $t_h$ | 0.850 | 0.910 | 1.311 | 1.430 | 1.551 | 1.490 | 1.818 | 1.438 | 1.559 | 1.499 | 1.862 | ns |
| | GCLK PLL | $t_{su}$ | 1.145 | 1.160 | 1.853 | 2.090 | 2.322 | 2.203 | 2.139 | 2.108 | 2.344 | 2.222 | 2.187 | ns |
| | | $t_h$ | -0.891 | -0.890 | -1.449 | -1.639 | -1.821 | -1.730 | -1.658 | -1.648 | -1.831 | -1.737 | -1.702 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.747 | -0.789 | -1.131 | -1.230 | -1.338 | -1.288 | -1.617 | -1.231 | -1.336 | -1.288 | -1.659 | ns |
| | | $t_h$ | 0.864 | 0.922 | 1.321 | 1.440 | 1.569 | 1.508 | 1.836 | 1.449 | 1.576 | 1.516 | 1.879 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.148 | 1.840 | 2.080 | 2.304 | 2.185 | 2.121 | 2.097 | 2.327 | 2.205 | 2.170 | ns |
| | | $t_h$ | -0.877 | -0.878 | -1.437 | -1.629 | -1.803 | -1.712 | -1.640 | -1.637 | -1.814 | -1.720 | -1.685 | ns |

**Table 1–76.** EP3SL150 Row Pins Input Timing Parameters (Part 2 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.747 | -0.789 | -1.131 | -1.230 | -1.338 | -1.288 | -1.617 | -1.231 | -1.336 | -1.288 | -1.659 | ns |
| | | $t_h$ | 0.864 | 0.922 | 1.321 | 1.440 | 1.569 | 1.508 | 1.836 | 1.449 | 1.576 | 1.516 | 1.879 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.148 | 1.840 | 2.080 | 2.304 | 2.185 | 2.121 | 2.097 | 2.327 | 2.205 | 2.170 | ns |
| | | $t_h$ | -0.877 | -0.878 | -1.437 | -1.629 | -1.803 | -1.712 | -1.640 | -1.637 | -1.814 | -1.720 | -1.685 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.733 | -0.777 | -1.122 | -1.220 | -1.320 | -1.270 | -1.599 | -1.220 | -1.319 | -1.271 | -1.642 | ns |
| | | $t_h$ | 0.850 | 0.910 | 1.311 | 1.430 | 1.551 | 1.490 | 1.818 | 1.438 | 1.559 | 1.499 | 1.862 | ns |
| | GCLK PLL | $t_{su}$ | 1.145 | 1.160 | 1.853 | 2.090 | 2.322 | 2.203 | 2.139 | 2.108 | 2.344 | 2.222 | 2.187 | ns |
| | | $t_h$ | -0.891 | -0.890 | -1.449 | -1.639 | -1.821 | -1.730 | -1.658 | -1.648 | -1.831 | -1.737 | -1.702 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.733 | -0.777 | -1.122 | -1.220 | -1.320 | -1.270 | -1.599 | -1.220 | -1.319 | -1.271 | -1.642 | ns |
| | | $t_h$ | 0.850 | 0.910 | 1.311 | 1.430 | 1.551 | 1.490 | 1.818 | 1.438 | 1.559 | 1.499 | 1.862 | ns |
| | GCLK PLL | $t_{su}$ | 1.145 | 1.160 | 1.853 | 2.090 | 2.322 | 2.203 | 2.139 | 2.108 | 2.344 | 2.222 | 2.187 | ns |
| | | $t_h$ | -0.891 | -0.890 | -1.449 | -1.639 | -1.821 | -1.730 | -1.658 | -1.648 | -1.831 | -1.737 | -1.702 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -0.747 | -0.789 | -1.131 | -1.230 | -1.338 | -1.288 | -1.617 | -1.231 | -1.336 | -1.288 | -1.659 | ns |
| | | $t_h$ | 0.864 | 0.922 | 1.321 | 1.440 | 1.569 | 1.508 | 1.836 | 1.449 | 1.576 | 1.516 | 1.879 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.148 | 1.840 | 2.080 | 2.304 | 2.185 | 2.121 | 2.097 | 2.327 | 2.205 | 2.170 | ns |
| | | $t_h$ | -0.877 | -0.878 | -1.437 | -1.629 | -1.803 | -1.712 | -1.640 | -1.637 | -1.814 | -1.720 | -1.685 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -0.747 | -0.789 | -1.131 | -1.230 | -1.338 | -1.288 | -1.617 | -1.231 | -1.336 | -1.288 | -1.659 | ns |
| | | $t_h$ | 0.864 | 0.922 | 1.321 | 1.440 | 1.569 | 1.508 | 1.836 | 1.449 | 1.576 | 1.516 | 1.879 | ns |
| | GCLK PLL | $t_{su}$ | 1.131 | 1.148 | 1.840 | 2.080 | 2.304 | 2.185 | 2.121 | 2.097 | 2.327 | 2.205 | 2.170 | ns |
| | | $t_h$ | -0.877 | -0.878 | -1.437 | -1.629 | -1.803 | -1.712 | -1.640 | -1.637 | -1.814 | -1.720 | -1.685 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.756 | -0.798 | -1.145 | -1.241 | -1.345 | -1.296 | -1.623 | -1.238 | -1.337 | -1.291 | -1.661 | ns |
| | | $t_h$ | 0.873 | 0.931 | 1.336 | 1.454 | 1.579 | 1.518 | 1.847 | 1.459 | 1.582 | 1.521 | 1.886 | ns |
| | GCLK PLL | $t_{su}$ | 1.122 | 1.139 | 1.825 | 2.064 | 2.293 | 2.173 | 2.110 | 2.086 | 2.321 | 2.197 | 2.163 | ns |
| | | $t_h$ | -0.868 | -0.869 | -1.422 | -1.611 | -1.789 | -1.698 | -1.625 | -1.623 | -1.805 | -1.711 | -1.674 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.756 | -0.798 | -1.145 | -1.241 | -1.345 | -1.296 | -1.623 | -1.238 | -1.337 | -1.291 | -1.661 | ns |
| | | $t_h$ | 0.873 | 0.931 | 1.336 | 1.454 | 1.579 | 1.518 | 1.847 | 1.459 | 1.582 | 1.521 | 1.886 | ns |
| | GCLK PLL | $t_{su}$ | 1.122 | 1.139 | 1.825 | 2.064 | 2.293 | 2.173 | 2.110 | 2.086 | 2.321 | 2.197 | 2.163 | ns |
| | | $t_h$ | -0.868 | -0.869 | -1.422 | -1.611 | -1.789 | -1.698 | -1.625 | -1.623 | -1.805 | -1.711 | -1.674 | ns |

Table 1–77 lists the EP3SL150 column pins output timing parameters for differential I/O standards.

**Table 1–77.** EP3SL150 Column Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.100 | 3.330 | 4.687 | 5.079 | 5.586 | 5.447 | 5.731 | 5.200 | 5.706 | 5.570 | 5.803 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.480 | 1.885 | 1.978 | 2.188 | 2.199 | 2.226 | 2.081 | 2.293 | 2.303 | 2.211 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.096 | 3.333 | 4.734 | 5.134 | 5.648 | 5.509 | 5.793 | 5.259 | 5.772 | 5.636 | 5.869 | ns |
| | | GCLK PLL | $t_{co}$ | 1.304 | 1.483 | 1.932 | 2.033 | 2.250 | 2.261 | 2.288 | 2.140 | 2.359 | 2.369 | 2.277 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.100 | 3.330 | 4.687 | 5.079 | 5.586 | 5.447 | 5.731 | 5.200 | 5.706 | 5.570 | 5.803 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.480 | 1.885 | 1.978 | 2.188 | 2.199 | 2.226 | 2.081 | 2.293 | 2.303 | 2.211 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.096 | 3.333 | 4.734 | 5.134 | 5.648 | 5.509 | 5.793 | 5.259 | 5.772 | 5.636 | 5.869 | ns |
| | | GCLK PLL | $t_{co}$ | 1.304 | 1.483 | 1.932 | 2.033 | 2.250 | 2.261 | 2.288 | 2.140 | 2.359 | 2.369 | 2.277 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.100 | 3.330 | 4.687 | 5.079 | 5.586 | 5.447 | 5.731 | 5.200 | 5.706 | 5.570 | 5.803 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.480 | 1.885 | 1.978 | 2.188 | 2.199 | 2.226 | 2.081 | 2.293 | 2.303 | 2.211 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.096 | 3.333 | 4.734 | 5.134 | 5.648 | 5.509 | 5.793 | 5.259 | 5.772 | 5.636 | 5.869 | ns |
| | | GCLK PLL | $t_{co}$ | 1.304 | 1.483 | 1.932 | 2.033 | 2.250 | 2.261 | 2.288 | 2.140 | 2.359 | 2.369 | 2.277 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.127 | 3.363 | 4.758 | 5.157 | 5.670 | 5.531 | 5.815 | 5.280 | 5.792 | 5.656 | 5.889 | ns |
| | | GCLK PLL | $t_{co}$ | 1.335 | 1.513 | 1.956 | 2.056 | 2.272 | 2.283 | 2.310 | 2.161 | 2.379 | 2.389 | 2.297 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.117 | 3.353 | 4.748 | 5.146 | 5.660 | 5.521 | 5.805 | 5.269 | 5.782 | 5.646 | 5.879 | ns |
| | | GCLK PLL | $t_{co}$ | 1.325 | 1.503 | 1.946 | 2.045 | 2.262 | 2.273 | 2.300 | 2.150 | 2.369 | 2.379 | 2.287 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.117 | 3.353 | 4.751 | 5.150 | 5.664 | 5.525 | 5.809 | 5.274 | 5.787 | 5.651 | 5.884 | ns |
| | | GCLK PLL | $t_{co}$ | 1.325 | 1.503 | 1.949 | 2.049 | 2.266 | 2.277 | 2.304 | 2.155 | 2.374 | 2.384 | 2.292 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.110 | 3.347 | 4.744 | 5.144 | 5.658 | 5.519 | 5.803 | 5.267 | 5.781 | 5.645 | 5.878 | ns |
| | | GCLK PLL | $t_{co}$ | 1.318 | 1.497 | 1.942 | 2.043 | 2.260 | 2.271 | 2.298 | 2.148 | 2.368 | 2.378 | 2.286 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.109 | 3.345 | 4.741 | 5.141 | 5.655 | 5.516 | 5.800 | 5.264 | 5.777 | 5.641 | 5.874 | ns |
| | | GCLK PLL | $t_{co}$ | 1.317 | 1.495 | 1.939 | 2.040 | 2.257 | 2.268 | 2.295 | 2.145 | 2.364 | 2.374 | 2.282 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.131 | 3.367 | 4.762 | 5.161 | 5.674 | 5.535 | 5.819 | 5.284 | 5.797 | 5.661 | 5.894 | ns |
| | | GCLK PLL | $t_{co}$ | 1.339 | 1.517 | 1.960 | 2.060 | 2.276 | 2.287 | 2.314 | 2.165 | 2.384 | 2.394 | 2.302 | ns |

**Table 1–77.** EP3SL150 Column Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.121 | 3.356 | 4.741 | 5.138 | 5.649 | 5.510 | 5.794 | 5.260 | 5.770 | 5.634 | 5.867 | ns |
| | | GCLK PLL | $t_{co}$ | 1.329 | 1.506 | 1.939 | 2.037 | 2.251 | 2.262 | 2.289 | 2.141 | 2.357 | 2.367 | 2.275 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.116 | 3.352 | 4.741 | 5.138 | 5.650 | 5.511 | 5.795 | 5.261 | 5.772 | 5.636 | 5.869 | ns |
| | | GCLK PLL | $t_{co}$ | 1.324 | 1.502 | 1.939 | 2.037 | 2.252 | 2.263 | 2.290 | 2.142 | 2.359 | 2.369 | 2.277 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.114 | 3.350 | 4.740 | 5.137 | 5.648 | 5.509 | 5.793 | 5.260 | 5.771 | 5.635 | 5.868 | ns |
| | | GCLK PLL | $t_{co}$ | 1.322 | 1.500 | 1.938 | 2.036 | 2.250 | 2.261 | 2.288 | 2.141 | 2.358 | 2.368 | 2.276 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.106 | 3.341 | 4.730 | 5.127 | 5.639 | 5.500 | 5.784 | 5.250 | 5.761 | 5.625 | 5.858 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.491 | 1.928 | 2.026 | 2.241 | 2.252 | 2.279 | 2.131 | 2.348 | 2.358 | 2.266 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.107 | 3.343 | 4.736 | 5.134 | 5.647 | 5.508 | 5.792 | 5.258 | 5.770 | 5.634 | 5.867 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.493 | 1.934 | 2.033 | 2.249 | 2.260 | 2.287 | 2.139 | 2.357 | 2.367 | 2.275 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.106 | 3.340 | 4.719 | 5.115 | 5.625 | 5.486 | 5.770 | 5.237 | 5.746 | 5.610 | 5.843 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.490 | 1.917 | 2.014 | 2.227 | 2.238 | 2.265 | 2.118 | 2.333 | 2.343 | 2.251 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.118 | 3.353 | 4.737 | 5.133 | 5.643 | 5.504 | 5.788 | 5.256 | 5.765 | 5.629 | 5.862 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.503 | 1.935 | 2.032 | 2.245 | 2.256 | 2.283 | 2.137 | 2.352 | 2.362 | 2.270 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.114 | 3.350 | 4.738 | 5.135 | 5.647 | 5.508 | 5.792 | 5.258 | 5.769 | 5.633 | 5.866 | ns |
| | | GCLK PLL | $t_{co}$ | 1.322 | 1.500 | 1.936 | 2.034 | 2.249 | 2.260 | 2.287 | 2.139 | 2.356 | 2.366 | 2.274 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.104 | 3.339 | 4.727 | 5.124 | 5.635 | 5.496 | 5.780 | 5.247 | 5.757 | 5.621 | 5.854 | ns |
| | | GCLK PLL | $t_{co}$ | 1.312 | 1.489 | 1.925 | 2.023 | 2.237 | 2.248 | 2.275 | 2.128 | 2.344 | 2.354 | 2.262 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.102 | 3.337 | 4.725 | 5.121 | 5.633 | 5.494 | 5.778 | 5.245 | 5.755 | 5.619 | 5.852 | ns |
| | | GCLK PLL | $t_{co}$ | 1.310 | 1.487 | 1.923 | 2.020 | 2.235 | 2.246 | 2.273 | 2.126 | 2.342 | 2.352 | 2.260 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.102 | 3.338 | 4.728 | 5.126 | 5.638 | 5.499 | 5.783 | 5.249 | 5.761 | 5.625 | 5.858 | ns |
| | | GCLK PLL | $t_{co}$ | 1.310 | 1.488 | 1.926 | 2.025 | 2.240 | 2.251 | 2.278 | 2.130 | 2.348 | 2.358 | 2.266 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.106 | 3.341 | 4.725 | 5.121 | 5.632 | 5.493 | 5.777 | 5.244 | 5.754 | 5.618 | 5.851 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.491 | 1.923 | 2.020 | 2.234 | 2.245 | 2.272 | 2.125 | 2.341 | 2.351 | 2.259 | ns |


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**Table 1–77.** EP3SL150 Column Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.132 | 3.370 | 4.770 | 5.169 | 5.682 | 5.543 | 5.827 | 5.292 | 5.804 | 5.668 | 5.901 | ns |
| | | GCLK PLL | $t_{co}$ | 1.340 | 1.520 | 1.968 | 2.068 | 2.284 | 2.295 | 2.322 | 2.173 | 2.391 | 2.401 | 2.309 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.118 | 3.356 | 4.758 | 5.158 | 5.672 | 5.533 | 5.817 | 5.282 | 5.795 | 5.659 | 5.892 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.506 | 1.956 | 2.057 | 2.274 | 2.285 | 2.312 | 2.163 | 2.382 | 2.392 | 2.300 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.106 | 3.343 | 4.741 | 5.140 | 5.654 | 5.515 | 5.799 | 5.264 | 5.777 | 5.641 | 5.874 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.493 | 1.939 | 2.039 | 2.256 | 2.267 | 2.294 | 2.145 | 2.364 | 2.374 | 2.282 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.106 | 3.343 | 4.744 | 5.144 | 5.658 | 5.519 | 5.803 | 5.268 | 5.782 | 5.646 | 5.879 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.493 | 1.942 | 2.043 | 2.260 | 2.271 | 2.298 | 2.149 | 2.369 | 2.379 | 2.287 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.102 | 3.339 | 4.737 | 5.136 | 5.651 | 5.512 | 5.796 | 5.261 | 5.774 | 5.638 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.310 | 1.489 | 1.935 | 2.035 | 2.253 | 2.264 | 2.291 | 2.142 | 2.361 | 2.371 | 2.279 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.106 | 3.341 | 4.730 | 5.127 | 5.639 | 5.500 | 5.784 | 5.250 | 5.761 | 5.625 | 5.858 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.491 | 1.928 | 2.026 | 2.241 | 2.252 | 2.279 | 2.131 | 2.348 | 2.358 | 2.266 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.107 | 3.343 | 4.738 | 5.137 | 5.650 | 5.511 | 5.795 | 5.260 | 5.773 | 5.637 | 5.870 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.493 | 1.936 | 2.036 | 2.252 | 2.263 | 2.290 | 2.141 | 2.360 | 2.370 | 2.278 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.135 | 3.373 | 4.769 | 5.167 | 5.680 | 5.541 | 5.825 | 5.291 | 5.802 | 5.666 | 5.899 | ns |
| | | GCLK PLL | $t_{co}$ | 1.343 | 1.523 | 1.967 | 2.066 | 2.282 | 2.293 | 2.320 | 2.172 | 2.389 | 2.399 | 2.307 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.124 | 3.361 | 4.757 | 5.155 | 5.668 | 5.529 | 5.813 | 5.279 | 5.790 | 5.654 | 5.887 | ns |
| | | GCLK PLL | $t_{co}$ | 1.332 | 1.511 | 1.955 | 2.054 | 2.270 | 2.281 | 2.308 | 2.160 | 2.377 | 2.387 | 2.295 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.119 | 3.357 | 4.757 | 5.156 | 5.669 | 5.530 | 5.814 | 5.280 | 5.792 | 5.656 | 5.889 | ns |
| | | GCLK PLL | $t_{co}$ | 1.327 | 1.507 | 1.955 | 2.055 | 2.271 | 2.282 | 2.309 | 2.161 | 2.379 | 2.389 | 2.297 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.105 | 3.342 | 4.739 | 5.137 | 5.650 | 5.511 | 5.795 | 5.261 | 5.774 | 5.638 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.313 | 1.492 | 1.937 | 2.036 | 2.252 | 2.263 | 2.290 | 2.142 | 2.361 | 2.371 | 2.279 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.103 | 3.340 | 4.737 | 5.135 | 5.648 | 5.509 | 5.793 | 5.259 | 5.771 | 5.635 | 5.868 | ns |
| | | GCLK PLL | $t_{co}$ | 1.311 | 1.490 | 1.935 | 2.034 | 2.250 | 2.261 | 2.288 | 2.140 | 2.358 | 2.368 | 2.276 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.107 | 3.342 | 4.729 | 5.125 | 5.636 | 5.497 | 5.781 | 5.248 | 5.758 | 5.622 | 5.855 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.492 | 1.927 | 2.024 | 2.238 | 2.249 | 2.276 | 2.129 | 2.345 | 2.355 | 2.263 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.107 | 3.343 | 4.737 | 5.135 | 5.648 | 5.509 | 5.793 | 5.259 | 5.771 | 5.635 | 5.868 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.493 | 1.935 | 2.034 | 2.250 | 2.261 | 2.288 | 2.140 | 2.358 | 2.368 | 2.276 | ns |

**Table 1–77.** EP3SL150 Column Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.123 | 3.360 | 4.753 | 5.150 | 5.662 | 5.523 | 5.807 | 5.274 | 5.784 | 5.648 | 5.881 | ns |
| | | GCLK PLL | $t_{co}$ | 1.331 | 1.510 | 1.951 | 2.049 | 2.264 | 2.275 | 2.302 | 2.155 | 2.371 | 2.381 | 2.289 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.123 | 3.360 | 4.753 | 5.150 | 5.662 | 5.523 | 5.807 | 5.274 | 5.784 | 5.648 | 5.881 | ns |
| | | GCLK PLL | $t_{co}$ | 1.331 | 1.510 | 1.951 | 2.049 | 2.264 | 2.275 | 2.302 | 2.155 | 2.371 | 2.381 | 2.289 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.113 | 3.350 | 4.743 | 5.140 | 5.652 | 5.513 | 5.797 | 5.264 | 5.775 | 5.639 | 5.872 | ns |
| | | GCLK PLL | $t_{co}$ | 1.321 | 1.500 | 1.941 | 2.039 | 2.254 | 2.265 | 2.292 | 2.145 | 2.362 | 2.372 | 2.280 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.106 | 3.342 | 4.729 | 5.125 | 5.636 | 5.497 | 5.781 | 5.248 | 5.758 | 5.622 | 5.855 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.492 | 1.927 | 2.024 | 2.238 | 2.249 | 2.276 | 2.129 | 2.345 | 2.355 | 2.263 | ns |


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Table 1–78 lists the EP3SL150 row pins output timing parameters for differential I/O standards.

**Table 1–78.** EP3SL150 Row Pins Output Timing Parameters (Part 1 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | — | GCLK | $t_{co}$ | 2.711 | 2.894 | 4.033 | 4.387 | 4.843 | 4.717 | 4.978 | 4.486 | 4.943 | 4.816 | 5.035 | ns |
| | | GCLK PLL | $t_{co}$ | 0.934 | 1.059 | 1.248 | 1.300 | 1.459 | 1.480 | 1.491 | 1.379 | 1.542 | 1.561 | 1.459 | ns |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.106 | 3.342 | 4.709 | 5.107 | 5.611 | 5.475 | 5.730 | 5.229 | 5.736 | 5.599 | 5.802 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.503 | 1.919 | 2.016 | 2.222 | 2.235 | 2.238 | 2.120 | 2.330 | 2.340 | 2.222 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.088 | 3.332 | 4.747 | 5.153 | 5.665 | 5.529 | 5.784 | 5.280 | 5.797 | 5.660 | 5.863 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.493 | 1.957 | 2.062 | 2.276 | 2.289 | 2.292 | 2.171 | 2.391 | 2.401 | 2.283 | ns |
| MINI-LVDS | — | GCLK | $t_{co}$ | 2.711 | 2.894 | 4.033 | 4.387 | 4.843 | 4.717 | 4.978 | 4.486 | 4.943 | 4.816 | 5.035 | ns |
| | | GCLK PLL | $t_{co}$ | 0.934 | 1.059 | 1.248 | 1.300 | 1.459 | 1.480 | 1.491 | 1.379 | 1.542 | 1.561 | 1.459 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.106 | 3.342 | 4.709 | 5.107 | 5.611 | 5.475 | 5.730 | 5.229 | 5.736 | 5.599 | 5.802 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.503 | 1.919 | 2.016 | 2.222 | 2.235 | 2.238 | 2.120 | 2.330 | 2.340 | 2.222 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.088 | 3.332 | 4.747 | 5.153 | 5.665 | 5.529 | 5.784 | 5.280 | 5.797 | 5.660 | 5.863 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.493 | 1.957 | 2.062 | 2.276 | 2.289 | 2.292 | 2.171 | 2.391 | 2.401 | 2.283 | ns |
| RSDS | — | GCLK | $t_{co}$ | 2.711 | 2.894 | 4.033 | 4.387 | 4.843 | 4.717 | 4.978 | 4.486 | 4.943 | 4.816 | 5.035 | ns |
| | | GCLK PLL | $t_{co}$ | 0.934 | 1.059 | 1.248 | 1.300 | 1.459 | 1.480 | 1.491 | 1.379 | 1.542 | 1.561 | 1.459 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.106 | 3.342 | 4.709 | 5.107 | 5.611 | 5.475 | 5.730 | 5.229 | 5.736 | 5.599 | 5.802 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.503 | 1.919 | 2.016 | 2.222 | 2.235 | 2.238 | 2.120 | 2.330 | 2.340 | 2.222 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.088 | 3.332 | 4.747 | 5.153 | 5.665 | 5.529 | 5.784 | 5.280 | 5.797 | 5.660 | 5.863 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.493 | 1.957 | 2.062 | 2.276 | 2.289 | 2.292 | 2.171 | 2.391 | 2.401 | 2.283 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.132 | 3.375 | 4.783 | 5.187 | 5.698 | 5.562 | 5.817 | 5.313 | 5.826 | 5.689 | 5.892 | ns |
| | | GCLK PLL | $t_{co}$ | 1.352 | 1.536 | 1.993 | 2.096 | 2.309 | 2.322 | 2.325 | 2.204 | 2.420 | 2.430 | 2.312 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.118 | 3.361 | 4.770 | 5.174 | 5.685 | 5.549 | 5.804 | 5.299 | 5.813 | 5.676 | 5.879 | ns |
| | | GCLK PLL | $t_{co}$ | 1.338 | 1.522 | 1.980 | 2.083 | 2.296 | 2.309 | 2.312 | 2.190 | 2.407 | 2.417 | 2.299 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.114 | 3.357 | 4.768 | 5.174 | 5.686 | 5.550 | 5.805 | 5.299 | 5.815 | 5.678 | 5.881 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.518 | 1.978 | 2.083 | 2.297 | 2.310 | 2.313 | 2.190 | 2.409 | 2.419 | 2.301 | ns |

**Table 1–78.** EP3SL150 Row Pins Output Timing Parameters (Part 2 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.130 | 3.372 | 4.769 | 5.171 | 5.680 | 5.544 | 5.799 | 5.296 | 5.808 | 5.671 | 5.874 | ns |
| | | GCLK PLL | $t_{co}$ | 1.350 | 1.533 | 1.979 | 2.080 | 2.291 | 2.304 | 2.307 | 2.187 | 2.402 | 2.412 | 2.294 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.119 | 3.362 | 4.765 | 5.167 | 5.677 | 5.541 | 5.796 | 5.293 | 5.805 | 5.668 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.339 | 1.523 | 1.975 | 2.076 | 2.288 | 2.301 | 2.304 | 2.184 | 2.399 | 2.409 | 2.291 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.116 | 3.359 | 4.763 | 5.165 | 5.675 | 5.539 | 5.794 | 5.291 | 5.804 | 5.667 | 5.870 | ns |
| | | GCLK PLL | $t_{co}$ | 1.336 | 1.520 | 1.973 | 2.074 | 2.286 | 2.299 | 2.302 | 2.182 | 2.398 | 2.408 | 2.290 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.127 | 3.369 | 4.764 | 5.166 | 5.674 | 5.538 | 5.793 | 5.291 | 5.802 | 5.665 | 5.868 | ns |
| | | GCLK PLL | $t_{co}$ | 1.347 | 1.530 | 1.974 | 2.075 | 2.285 | 2.298 | 2.301 | 2.182 | 2.396 | 2.406 | 2.288 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.117 | 3.360 | 4.762 | 5.164 | 5.673 | 5.537 | 5.792 | 5.290 | 5.802 | 5.665 | 5.868 | ns |
| | | GCLK PLL | $t_{co}$ | 1.337 | 1.521 | 1.972 | 2.073 | 2.284 | 2.297 | 2.300 | 2.181 | 2.396 | 2.406 | 2.288 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.103 | 3.346 | 4.747 | 5.149 | 5.659 | 5.523 | 5.778 | 5.275 | 5.787 | 5.650 | 5.853 | ns |
| | | GCLK PLL | $t_{co}$ | 1.323 | 1.507 | 1.957 | 2.058 | 2.270 | 2.283 | 2.286 | 2.166 | 2.381 | 2.391 | 2.273 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.100 | 3.342 | 4.743 | 5.145 | 5.655 | 5.519 | 5.774 | 5.271 | 5.783 | 5.646 | 5.849 | ns |
| | | GCLK PLL | $t_{co}$ | 1.320 | 1.503 | 1.953 | 2.054 | 2.266 | 2.279 | 2.282 | 2.162 | 2.377 | 2.387 | 2.269 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.097 | 3.340 | 4.744 | 5.148 | 5.658 | 5.522 | 5.777 | 5.274 | 5.787 | 5.650 | 5.853 | ns |
| | | GCLK PLL | $t_{co}$ | 1.317 | 1.501 | 1.954 | 2.057 | 2.269 | 2.282 | 2.285 | 2.165 | 2.381 | 2.391 | 2.273 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.098 | 3.340 | 4.734 | 5.136 | 5.645 | 5.509 | 5.764 | 5.261 | 5.773 | 5.636 | 5.839 | ns |
| | | GCLK PLL | $t_{co}$ | 1.318 | 1.501 | 1.944 | 2.045 | 2.256 | 2.269 | 2.272 | 2.152 | 2.367 | 2.377 | 2.259 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.147 | 3.393 | 4.805 | 5.209 | 5.721 | 5.585 | 5.840 | 5.335 | 5.849 | 5.712 | 5.915 | ns |
| | | GCLK PLL | $t_{co}$ | 1.367 | 1.554 | 2.015 | 2.118 | 2.332 | 2.345 | 2.348 | 2.226 | 2.443 | 2.453 | 2.335 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.123 | 3.369 | 4.787 | 5.192 | 5.704 | 5.568 | 5.823 | 5.318 | 5.834 | 5.697 | 5.900 | ns |
| | | GCLK PLL | $t_{co}$ | 1.343 | 1.530 | 1.997 | 2.101 | 2.315 | 2.328 | 2.331 | 2.209 | 2.428 | 2.438 | 2.320 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.106 | 3.350 | 4.765 | 5.170 | 5.682 | 5.546 | 5.801 | 5.296 | 5.812 | 5.675 | 5.878 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.511 | 1.975 | 2.079 | 2.293 | 2.306 | 2.309 | 2.187 | 2.406 | 2.416 | 2.298 | ns |


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**Table 1–78.** EP3SL150 Row Pins Output Timing Parameters (Part 3 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.151 | 3.396 | 4.805 | 5.209 | 5.720 | 5.584 | 5.839 | 5.335 | 5.849 | 5.712 | 5.915 | ns |
| | | GCLK PLL | $t_{co}$ | 1.371 | 1.557 | 2.015 | 2.118 | 2.331 | 2.344 | 2.347 | 2.226 | 2.443 | 2.453 | 2.335 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.136 | 3.381 | 4.791 | 5.194 | 5.705 | 5.569 | 5.824 | 5.320 | 5.834 | 5.697 | 5.900 | ns |
| | | GCLK PLL | $t_{co}$ | 1.356 | 1.542 | 2.001 | 2.103 | 2.316 | 2.329 | 2.332 | 2.211 | 2.428 | 2.438 | 2.320 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.125 | 3.370 | 4.786 | 5.191 | 5.702 | 5.566 | 5.821 | 5.317 | 5.832 | 5.695 | 5.898 | ns |
| | | GCLK PLL | $t_{co}$ | 1.345 | 1.531 | 1.996 | 2.100 | 2.313 | 2.326 | 2.329 | 2.208 | 2.426 | 2.436 | 2.318 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.105 | 3.350 | 4.763 | 5.167 | 5.679 | 5.543 | 5.798 | 5.294 | 5.808 | 5.671 | 5.874 | ns |
| | | GCLK PLL | $t_{co}$ | 1.325 | 1.511 | 1.973 | 2.076 | 2.290 | 2.303 | 2.306 | 2.185 | 2.402 | 2.412 | 2.294 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.102 | 3.346 | 4.759 | 5.164 | 5.675 | 5.539 | 5.794 | 5.290 | 5.805 | 5.668 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.322 | 1.507 | 1.969 | 2.073 | 2.286 | 2.299 | 2.302 | 2.181 | 2.399 | 2.409 | 2.291 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.107 | 3.350 | 4.750 | 5.152 | 5.661 | 5.525 | 5.780 | 5.277 | 5.789 | 5.652 | 5.855 | ns |
| | | GCLK PLL | $t_{co}$ | 1.327 | 1.511 | 1.960 | 2.061 | 2.272 | 2.285 | 2.288 | 2.168 | 2.383 | 2.393 | 2.275 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.100 | 3.343 | 4.749 | 5.153 | 5.664 | 5.528 | 5.783 | 5.280 | 5.794 | 5.657 | 5.860 | ns |
| | | GCLK PLL | $t_{co}$ | 1.320 | 1.504 | 1.959 | 2.062 | 2.275 | 2.288 | 2.291 | 2.171 | 2.388 | 2.398 | 2.280 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.138 | 3.382 | 4.787 | 5.190 | 5.700 | 5.564 | 5.819 | 5.316 | 5.829 | 5.692 | 5.895 | ns |
| | | GCLK PLL | $t_{co}$ | 1.358 | 1.543 | 1.997 | 2.099 | 2.311 | 2.324 | 2.327 | 2.207 | 2.423 | 2.433 | 2.315 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.120 | 3.365 | 4.772 | 5.175 | 5.685 | 5.549 | 5.804 | 5.301 | 5.814 | 5.677 | 5.880 | ns |
| | | GCLK PLL | $t_{co}$ | 1.340 | 1.526 | 1.982 | 2.084 | 2.296 | 2.309 | 2.312 | 2.192 | 2.408 | 2.418 | 2.300 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.106 | 3.349 | 4.749 | 5.151 | 5.660 | 5.524 | 5.779 | 5.277 | 5.789 | 5.652 | 5.855 | ns |
| | | GCLK PLL | $t_{co}$ | 1.326 | 1.510 | 1.959 | 2.060 | 2.271 | 2.284 | 2.287 | 2.168 | 2.383 | 2.393 | 2.275 | ns |

Table 1–79 and Table 1–80 list the EP3SL150 regional clock (RCLK) adder values that must be added to the GCLK values. Use these adder values to determine I/O timing when the I/O pin is driven using the regional clock. This applies to all I/O standards supported by Stratix III devices.

Table 1–79 lists the EP3SL150 column pin delay adders when using the regional clock.

**Table 1–79.** EP3SL150 Column Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.198 | 0.152 | 0.22 | 0.258 | 0.27 | 0.262 | 0.393 | 0.244 | 0.271 | 0.261 | 0.495 | ns |
| RCLK PLL input adder | 2.453 | 2.426 | 3.654 | 4.098 | 4.422 | 4.224 | 4.664 | 4.106 | 4.447 | 4.101 | 4.707 | ns |
| RCLK output adder | -0.374 | -0.152 | -0.216 | -0.232 | -0.248 | -0.227 | -0.367 | -0.11 | -0.127 | -0.106 | -0.303 | ns |
| RCLK PLL output adder | -2.017 | -1.798 | -2.68 | -2.859 | -3.011 | -2.872 | -2.715 | -2.714 | -3.082 | -2.791 | -2.766 | ns |

Table 1–80 lists the EP3SL150 row pin delay adders when using the regional clock.

**Table 1–80.** EP3SL150 Row Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.107 | 0.115 | 0.164 | 0.165 | 0.167 | 0.165 | 0.285 | 0.158 | 0.159 | 0.158 | 0.29 | ns |
| RCLK PLL input adder | 0.074 | 0.075 | 0.116 | 0.123 | 0.129 | 0.126 | 0.218 | 0.114 | 0.118 | 0.114 | 0.223 | ns |
| RCLK output adder | -0.093 | -0.103 | -0.137 | -0.136 | -0.133 | -0.134 | -0.257 | -0.125 | -0.121 | -0.122 | -0.261 | ns |
| RCLK PLL output adder | -0.063 | -0.065 | -0.097 | -0.102 | -0.103 | -0.102 | -0.198 | -0.088 | -0.089 | -0.088 | -0.202 | ns |

## EP3SL200 I/O Timing Parameters

Table 1–81 through Table 1–84 list the maximum I/O timing parameters for EP3SL200 devices for single-ended I/O standards.

Table 1–81 lists the EP3SL200 column pins input timing parameters for single-ended I/O standards.

**Table 1–81.** EP3SL200 Column Pins Input Timing Parameters (Part 1 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -1.137 | -1.173 | -1.810 | -1.775 | -2.002 | -1.934 | -2.482 | -1.775 | -2.002 | -1.934 | -2.482 | ns |
| | | $t_h$ | 1.285 | 1.319 | 2.032 | 2.008 | 2.259 | 2.177 | 2.724 | 2.008 | 2.259 | 2.177 | 2.724 | ns |
| | GCLK PLL | $t_{su}$ | -1.465 | -1.465 | -2.238 | -2.271 | -2.558 | -2.477 | -2.997 | -2.271 | -2.558 | -2.477 | -2.997 | ns |
| | | $t_h$ | 1.778 | 1.778 | 2.727 | 2.776 | 3.113 | 3.000 | 3.543 | 2.776 | 3.113 | 3.000 | 3.543 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -1.137 | -1.173 | -1.810 | -1.775 | -2.002 | -1.934 | -2.482 | -1.775 | -2.002 | -1.934 | -2.482 | ns |
| | | $t_h$ | 1.285 | 1.319 | 2.032 | 2.008 | 2.259 | 2.177 | 2.724 | 2.008 | 2.259 | 2.177 | 2.724 | ns |
| | GCLK PLL | $t_{su}$ | -1.465 | -1.465 | -2.238 | -2.271 | -2.558 | -2.477 | -2.997 | -2.271 | -2.558 | -2.477 | -2.997 | ns |
| | | $t_h$ | 1.778 | 1.778 | 2.727 | 2.776 | 3.113 | 3.000 | 3.543 | 2.776 | 3.113 | 3.000 | 3.543 | ns |


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**Table 1–81.** EP3SL200 Column Pins Input Timing Parameters (Part 2 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -1.148 | -1.184 | -1.809 | -1.777 | -2.001 | -1.933 | -2.481 | -1.777 | -2.001 | -1.933 | -2.481 | ns |
| | | $t_h$ | 1.296 | 1.330 | 2.031 | 2.010 | 2.258 | 2.176 | 2.723 | 2.010 | 2.258 | 2.176 | 2.723 | ns |
| | GCLK PLL | $t_{su}$ | -1.476 | -1.476 | -2.237 | -2.273 | -2.557 | -2.476 | -2.996 | -2.273 | -2.557 | -2.476 | -2.996 | ns |
| | | $t_h$ | 1.789 | 1.789 | 2.726 | 2.778 | 3.112 | 2.999 | 3.542 | 2.778 | 3.112 | 2.999 | 3.542 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -1.148 | -1.184 | -1.809 | -1.777 | -2.001 | -1.933 | -2.481 | -1.777 | -2.001 | -1.933 | -2.481 | ns |
| | | $t_h$ | 1.296 | 1.330 | 2.031 | 2.010 | 2.258 | 2.176 | 2.723 | 2.010 | 2.258 | 2.176 | 2.723 | ns |
| | GCLK PLL | $t_{su}$ | -1.476 | -1.476 | -2.237 | -2.273 | -2.557 | -2.476 | -2.996 | -2.273 | -2.557 | -2.476 | -2.996 | ns |
| | | $t_h$ | 1.789 | 1.789 | 2.726 | 2.778 | 3.112 | 2.999 | 3.542 | 2.778 | 3.112 | 2.999 | 3.542 | ns |
| 2.5 V | GCLK | $t_{su}$ | -1.143 | -1.179 | -1.818 | -1.789 | -2.020 | -1.952 | -2.500 | -1.789 | -2.020 | -1.952 | -2.500 | ns |
| | | $t_h$ | 1.291 | 1.325 | 2.040 | 2.022 | 2.277 | 2.195 | 2.742 | 2.022 | 2.277 | 2.195 | 2.742 | ns |
| | GCLK PLL | $t_{su}$ | -1.471 | -1.471 | -2.246 | -2.285 | -2.576 | -2.495 | -3.015 | -2.285 | -2.576 | -2.495 | -3.015 | ns |
| | | $t_h$ | 1.784 | 1.784 | 2.735 | 2.790 | 3.131 | 3.018 | 3.561 | 2.790 | 3.131 | 3.018 | 3.561 | ns |
| 1.8 V | GCLK | $t_{su}$ | -1.163 | -1.201 | -1.858 | -1.825 | -2.018 | -1.950 | -2.498 | -1.825 | -2.018 | -1.950 | -2.498 | ns |
| | | $t_h$ | 1.313 | 1.349 | 2.080 | 2.058 | 2.275 | 2.193 | 2.740 | 2.058 | 2.275 | 2.193 | 2.740 | ns |
| | GCLK PLL | $t_{su}$ | -1.493 | -1.493 | -2.286 | -2.321 | -2.574 | -2.493 | -3.013 | -2.321 | -2.574 | -2.493 | -3.013 | ns |
| | | $t_h$ | 1.808 | 1.808 | 2.775 | 2.826 | 3.129 | 3.016 | 3.559 | 2.826 | 3.129 | 3.016 | 3.559 | ns |
| 1.5 V | GCLK | $t_{su}$ | -1.153 | -1.191 | -1.835 | -1.793 | -1.948 | -1.880 | -2.428 | -1.793 | -1.948 | -1.880 | -2.428 | ns |
| | | $t_h$ | 1.303 | 1.339 | 2.057 | 2.026 | 2.205 | 2.123 | 2.670 | 2.026 | 2.205 | 2.123 | 2.670 | ns |
| | GCLK PLL | $t_{su}$ | -1.483 | -1.483 | -2.263 | -2.289 | -2.504 | -2.423 | -2.943 | -2.289 | -2.504 | -2.423 | -2.943 | ns |
| | | $t_h$ | 1.798 | 1.798 | 2.752 | 2.794 | 3.059 | 2.946 | 3.489 | 2.794 | 3.059 | 2.946 | 3.489 | ns |
| 1.2 V | GCLK | $t_{su}$ | -1.101 | -1.139 | -1.758 | -1.694 | -1.792 | -1.724 | -2.272 | -1.694 | -1.792 | -1.724 | -2.272 | ns |
| | | $t_h$ | 1.251 | 1.287 | 1.980 | 1.927 | 2.049 | 1.967 | 2.514 | 1.927 | 2.049 | 1.967 | 2.514 | ns |
| | GCLK PLL | $t_{su}$ | -1.431 | -1.431 | -2.186 | -2.190 | -2.348 | -2.267 | -2.787 | -2.190 | -2.348 | -2.267 | -2.787 | ns |
| | | $t_h$ | 1.746 | 1.746 | 2.675 | 2.695 | 2.903 | 2.790 | 3.333 | 2.695 | 2.903 | 2.790 | 3.333 | ns |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -1.072 | -1.110 | -1.730 | -1.678 | -1.794 | -1.726 | -2.274 | -1.678 | -1.794 | -1.726 | -2.274 | ns |
| | | $t_h$ | 1.222 | 1.258 | 1.952 | 1.911 | 2.051 | 1.969 | 2.516 | 1.911 | 2.051 | 1.969 | 2.516 | ns |
| | GCLK PLL | $t_{su}$ | -1.402 | -1.402 | -2.158 | -2.174 | -2.350 | -2.269 | -2.789 | -2.174 | -2.350 | -2.269 | -2.789 | ns |
| | | $t_h$ | 1.717 | 1.717 | 2.647 | 2.679 | 2.905 | 2.792 | 3.335 | 2.679 | 2.905 | 2.792 | 3.335 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -1.072 | -1.110 | -1.730 | -1.678 | -1.794 | -1.726 | -2.274 | -1.678 | -1.794 | -1.726 | -2.274 | ns |
| | | $t_h$ | 1.222 | 1.258 | 1.952 | 1.911 | 2.051 | 1.969 | 2.516 | 1.911 | 2.051 | 1.969 | 2.516 | ns |
| | GCLK PLL | $t_{su}$ | -1.402 | -1.402 | -2.158 | -2.174 | -2.350 | -2.269 | -2.789 | -2.174 | -2.350 | -2.269 | -2.789 | ns |
| | | $t_h$ | 1.717 | 1.717 | 2.647 | 2.679 | 2.905 | 2.792 | 3.335 | 2.679 | 2.905 | 2.792 | 3.335 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -1.066 | -1.104 | -1.717 | -1.673 | -1.794 | -1.724 | -2.272 | -1.673 | -1.794 | -1.724 | -2.272 | ns |
| | | $t_h$ | 1.216 | 1.252 | 1.939 | 1.903 | 2.048 | 1.966 | 2.509 | 1.903 | 2.048 | 1.966 | 2.509 | ns |
| | GCLK PLL | $t_{su}$ | -1.396 | -1.396 | -2.145 | -2.166 | -2.347 | -2.264 | -2.787 | -2.166 | -2.347 | -2.264 | -2.787 | ns |
| | | $t_h$ | 1.711 | 1.711 | 2.634 | 2.668 | 2.899 | 2.786 | 3.328 | 2.668 | 2.899 | 2.786 | 3.328 | ns |

**Table 1–81.** EP3SL200 Column Pins Input Timing Parameters (Part 3 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -1.066 | -1.104 | -1.717 | -1.673 | -1.794 | -1.724 | -2.272 | -1.673 | -1.794 | -1.724 | -2.272 | ns |
| | | $t_h$ | 1.216 | 1.252 | 1.939 | 1.903 | 2.048 | 1.966 | 2.509 | 1.903 | 2.048 | 1.966 | 2.509 | ns |
| | GCLK PLL | $t_{su}$ | -1.396 | -1.396 | -2.145 | -2.166 | -2.347 | -2.264 | -2.787 | -2.166 | -2.347 | -2.264 | -2.787 | ns |
| | | $t_h$ | 1.711 | 1.711 | 2.634 | 2.668 | 2.899 | 2.786 | 3.328 | 2.668 | 2.899 | 2.786 | 3.328 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -1.055 | -1.093 | -1.706 | -1.662 | -1.775 | -1.705 | -2.253 | -1.662 | -1.775 | -1.705 | -2.253 | ns |
| | | $t_h$ | 1.205 | 1.241 | 1.927 | 1.892 | 2.029 | 1.947 | 2.490 | 1.892 | 2.029 | 1.947 | 2.490 | ns |
| | GCLK PLL | $t_{su}$ | -1.385 | -1.385 | -2.134 | -2.155 | -2.328 | -2.245 | -2.768 | -2.155 | -2.328 | -2.245 | -2.768 | ns |
| | | $t_h$ | 1.700 | 1.700 | 2.622 | 2.657 | 2.880 | 2.767 | 3.309 | 2.657 | 2.880 | 2.767 | 3.309 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -1.055 | -1.093 | -1.706 | -1.662 | -1.775 | -1.705 | -2.253 | -1.662 | -1.775 | -1.705 | -2.253 | ns |
| | | $t_h$ | 1.205 | 1.241 | 1.927 | 1.892 | 2.029 | 1.947 | 2.490 | 1.892 | 2.029 | 1.947 | 2.490 | ns |
| | GCLK PLL | $t_{su}$ | -1.385 | -1.385 | -2.134 | -2.155 | -2.328 | -2.245 | -2.768 | -2.155 | -2.328 | -2.245 | -2.768 | ns |
| | | $t_h$ | 1.700 | 1.700 | 2.622 | 2.657 | 2.880 | 2.767 | 3.309 | 2.657 | 2.880 | 2.767 | 3.309 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -1.066 | -1.104 | -1.717 | -1.673 | -1.794 | -1.724 | -2.272 | -1.673 | -1.794 | -1.724 | -2.272 | ns |
| | | $t_h$ | 1.216 | 1.252 | 1.939 | 1.903 | 2.048 | 1.966 | 2.509 | 1.903 | 2.048 | 1.966 | 2.509 | ns |
| | GCLK PLL | $t_{su}$ | -1.396 | -1.396 | -2.145 | -2.166 | -2.347 | -2.264 | -2.787 | -2.166 | -2.347 | -2.264 | -2.787 | ns |
| | | $t_h$ | 1.711 | 1.711 | 2.634 | 2.668 | 2.899 | 2.786 | 3.328 | 2.668 | 2.899 | 2.786 | 3.328 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -1.066 | -1.104 | -1.717 | -1.673 | -1.794 | -1.724 | -2.272 | -1.673 | -1.794 | -1.724 | -2.272 | ns |
| | | $t_h$ | 1.216 | 1.252 | 1.939 | 1.903 | 2.048 | 1.966 | 2.509 | 1.903 | 2.048 | 1.966 | 2.509 | ns |
| | GCLK PLL | $t_{su}$ | -1.396 | -1.396 | -2.145 | -2.166 | -2.347 | -2.264 | -2.787 | -2.166 | -2.347 | -2.264 | -2.787 | ns |
| | | $t_h$ | 1.711 | 1.711 | 2.634 | 2.668 | 2.899 | 2.786 | 3.328 | 2.668 | 2.899 | 2.786 | 3.328 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -1.055 | -1.093 | -1.706 | -1.662 | -1.775 | -1.705 | -2.253 | -1.662 | -1.775 | -1.705 | -2.253 | ns |
| | | $t_h$ | 1.205 | 1.241 | 1.927 | 1.892 | 2.029 | 1.947 | 2.490 | 1.892 | 2.029 | 1.947 | 2.490 | ns |
| | GCLK PLL | $t_{su}$ | -1.385 | -1.385 | -2.134 | -2.155 | -2.328 | -2.245 | -2.768 | -2.155 | -2.328 | -2.245 | -2.768 | ns |
| | | $t_h$ | 1.700 | 1.700 | 2.622 | 2.657 | 2.880 | 2.767 | 3.309 | 2.657 | 2.880 | 2.767 | 3.309 | ns |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -1.055 | -1.093 | -1.706 | -1.662 | -1.775 | -1.705 | -2.253 | -1.662 | -1.775 | -1.705 | -2.253 | ns |
| | | $t_h$ | 1.205 | 1.241 | 1.927 | 1.892 | 2.029 | 1.947 | 2.490 | 1.892 | 2.029 | 1.947 | 2.490 | ns |
| | GCLK PLL | $t_{su}$ | -1.385 | -1.385 | -2.134 | -2.155 | -2.328 | -2.245 | -2.768 | -2.155 | -2.328 | -2.245 | -2.768 | ns |
| | | $t_h$ | 1.700 | 1.700 | 2.622 | 2.657 | 2.880 | 2.767 | 3.309 | 2.657 | 2.880 | 2.767 | 3.309 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -1.043 | -1.081 | -1.696 | -1.651 | -1.759 | -1.689 | -2.237 | -1.651 | -1.759 | -1.689 | -2.237 | ns |
| | | $t_h$ | 1.193 | 1.229 | 1.917 | 1.881 | 2.013 | 1.931 | 2.474 | 1.881 | 2.013 | 1.931 | 2.474 | ns |
| | GCLK PLL | $t_{su}$ | -1.373 | -1.373 | -2.124 | -2.144 | -2.312 | -2.229 | -2.752 | -2.144 | -2.312 | -2.229 | -2.752 | ns |
| | | $t_h$ | 1.688 | 1.688 | 2.612 | 2.646 | 2.864 | 2.751 | 3.293 | 2.646 | 2.864 | 2.751 | 3.293 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -1.043 | -1.081 | -1.696 | -1.651 | -1.759 | -1.689 | -2.237 | -1.651 | -1.759 | -1.689 | -2.237 | ns |
| | | $t_h$ | 1.193 | 1.229 | 1.917 | 1.881 | 2.013 | 1.931 | 2.474 | 1.881 | 2.013 | 1.931 | 2.474 | ns |
| | GCLK PLL | $t_{su}$ | -1.373 | -1.373 | -2.124 | -2.144 | -2.312 | -2.229 | -2.752 | -2.144 | -2.312 | -2.229 | -2.752 | ns |
| | | $t_h$ | 1.688 | 1.688 | 2.612 | 2.646 | 2.864 | 2.751 | 3.293 | 2.646 | 2.864 | 2.751 | 3.293 | ns |

**Table 1–81.** EP3SL200 Column Pins Input Timing Parameters (Part 4 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V PCI-X | GCLK | $t_{su}$ | -1.148 | -1.184 | -1.809 | -1.777 | -2.001 | -1.933 | -2.481 | -1.777 | -2.001 | -1.933 | -2.481 | ns |
| | | $t_h$ | 1.296 | 1.330 | 2.031 | 2.010 | 2.258 | 2.176 | 2.723 | 2.010 | 2.258 | 2.176 | 2.723 | ns |
| | GCLK PLL | $t_{su}$ | -1.476 | -1.476 | -2.237 | -2.273 | -2.557 | -2.476 | -2.996 | -2.273 | -2.557 | -2.476 | -2.996 | ns |
| | | $t_h$ | 1.789 | 1.789 | 2.726 | 2.778 | 3.112 | 2.999 | 3.542 | 2.778 | 3.112 | 2.999 | 3.542 | ns |

Table 1–82 lists the EP3SL200 row pins input timing parameters for single-ended I/O standards.

**Table 1–82.** EP3SL200 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -1.298 | -1.321 | -1.972 | -1.978 | -2.368 | -2.291 | -2.712 | -2.132 | -2.388 | -2.291 | -2.712 | ns |
| | | $t_h$ | 1.432 | 1.473 | 1.671 | 1.862 | 1.969 | 1.850 | 1.775 | 1.751 | 1.869 | 1.850 | 1.775 | ns |
| | GCLK PLL | $t_{su}$ | 0.915 | 0.938 | 2.210 | 2.223 | 2.633 | 2.541 | 2.966 | 2.384 | 2.665 | 2.541 | 2.966 | ns |
| | | $t_h$ | -0.638 | -0.643 | -1.972 | -1.978 | -2.368 | -2.291 | -2.712 | -2.132 | -2.388 | -2.291 | -2.712 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -1.298 | -1.321 | -1.972 | -1.978 | -2.368 | -2.291 | -2.712 | -2.132 | -2.388 | -2.291 | -2.712 | ns |
| | | $t_h$ | 1.432 | 1.473 | 1.671 | 1.862 | 1.969 | 1.850 | 1.775 | 1.751 | 1.869 | 1.850 | 1.775 | ns |
| | GCLK PLL | $t_{su}$ | 0.915 | 0.938 | 2.210 | 2.223 | 2.633 | 2.541 | 2.966 | 2.384 | 2.665 | 2.541 | 2.966 | ns |
| | | $t_h$ | -0.638 | -0.643 | -1.969 | -1.979 | -2.371 | -2.294 | -2.715 | -2.131 | -2.393 | -2.294 | -2.715 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -1.304 | -1.332 | 2.207 | 2.224 | 2.636 | 2.544 | 2.969 | 2.383 | 2.670 | 2.544 | 2.969 | ns |
| | | $t_h$ | 1.438 | 1.484 | -1.969 | -1.979 | -2.371 | -2.294 | -2.715 | -2.131 | -2.393 | -2.294 | -2.715 | ns |
| | GCLK PLL | $t_{su}$ | 0.909 | 0.927 | 1.674 | 1.861 | 1.966 | 1.847 | 1.772 | 1.752 | 1.864 | 1.847 | 1.772 | ns |
| | | $t_h$ | -0.632 | -0.632 | 2.207 | 2.224 | 2.636 | 2.544 | 2.969 | 2.383 | 2.670 | 2.544 | 2.969 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -1.304 | -1.332 | 2.216 | 2.237 | 2.651 | 2.559 | 2.984 | 2.392 | 2.680 | 2.559 | 2.984 | ns |
| | | $t_h$ | 1.438 | 1.484 | -1.978 | -1.992 | -2.386 | -2.309 | -2.730 | -2.140 | -2.403 | -2.309 | -2.730 | ns |
| | GCLK PLL | $t_{su}$ | 0.909 | 0.927 | 1.665 | 1.848 | 1.951 | 1.832 | 1.757 | 1.743 | 1.854 | 1.832 | 1.757 | ns |
| | | $t_h$ | -0.632 | -0.632 | 2.216 | 2.237 | 2.651 | 2.559 | 2.984 | 2.392 | 2.680 | 2.559 | 2.984 | ns |
| 2.5 V | GCLK | $t_{su}$ | -1.292 | -1.325 | 1.625 | 1.722 | 1.945 | 1.834 | 1.742 | 1.710 | 1.853 | 1.834 | 1.742 | ns |
| | | $t_h$ | 1.426 | 1.477 | 2.254 | 2.297 | 2.649 | 2.557 | 2.982 | 2.425 | 2.681 | 2.557 | 2.982 | ns |
| | GCLK PLL | $t_{su}$ | 0.921 | 0.934 | -2.017 | -2.051 | -2.384 | -2.307 | -2.728 | -2.173 | -2.404 | -2.307 | -2.728 | ns |
| | | $t_h$ | -0.644 | -0.639 | 1.625 | 1.722 | 1.945 | 1.834 | 1.742 | 1.710 | 1.853 | 1.834 | 1.742 | ns |
| 1.8 V | GCLK | $t_{su}$ | -1.322 | -1.354 | 1.649 | 1.754 | 2.013 | 1.902 | 1.810 | 1.741 | 1.918 | 1.902 | 1.810 | ns |
| | | $t_h$ | 0.891 | 0.902 | 2.230 | 2.265 | 2.581 | 2.489 | 2.914 | 2.394 | 2.616 | 2.489 | 2.914 | ns |
| | GCLK PLL | $t_{su}$ | 1.457 | 1.507 | -1.993 | -2.019 | -2.316 | -2.239 | -2.660 | -2.142 | -2.339 | -2.239 | -2.660 | ns |
| | | $t_h$ | -1.312 | -1.343 | 1.728 | 1.855 | 2.172 | 2.061 | 1.969 | 1.837 | 2.073 | 2.061 | 1.969 | ns |

**Table 1–82.** EP3SL200 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5 V | GCLK | $t_{su}$ | 0.901 | 0.913 | 2.151 | 2.164 | 2.422 | 2.330 | 2.755 | 2.298 | 2.461 | 2.330 | 2.755 | ns |
| | | $t_h$ | 1.447 | 1.496 | -1.914 | -1.918 | -2.157 | -2.080 | -2.501 | -2.046 | -2.184 | -2.080 | -2.501 | ns |
| | GCLK PLL | $t_{su}$ | -1.252 | -1.290 | 1.751 | 1.957 | 2.171 | 2.052 | 1.977 | 1.855 | 2.071 | 2.052 | 1.977 | ns |
| | | $t_h$ | 0.961 | 0.966 | 2.130 | 2.128 | 2.431 | 2.339 | 2.764 | 2.280 | 2.463 | 2.339 | 2.764 | ns |
| 1.2 V | GCLK | $t_{su}$ | 1.387 | 1.443 | -1.876 | -1.893 | -2.152 | -2.074 | -2.497 | -2.014 | -2.177 | -2.074 | -2.497 | ns |
| | | $t_h$ | -1.235 | -1.266 | 1.766 | -1.893 | -2.152 | -2.074 | -2.497 | -2.014 | -2.177 | -2.074 | -2.497 | ns |
| | GCLK PLL | $t_{su}$ | 0.978 | 0.992 | 2.113 | 2.137 | 2.415 | 2.323 | 2.747 | 2.264 | 2.451 | 2.323 | 2.747 | ns |
| | | $t_h$ | 1.370 | 1.419 | -1.876 | 1.882 | 2.174 | 2.064 | 1.973 | 1.869 | 2.080 | 2.064 | 1.973 | ns |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -1.235 | -1.266 | 1.766 | 1.882 | 2.174 | 2.064 | 1.973 | 1.869 | 2.080 | 2.064 | 1.973 | ns |
| | | $t_h$ | 0.978 | 0.992 | 2.113 | -1.387 | -1.620 | -1.542 | -1.441 | -1.361 | -1.518 | -1.542 | -1.441 | ns |
| | GCLK PLL | $t_{su}$ | 1.370 | 1.419 | -1.876 | -1.893 | -2.152 | -2.074 | -2.497 | -2.014 | -2.177 | -2.074 | -2.497 | ns |
| | | $t_h$ | -1.226 | -1.255 | 1.766 | 2.137 | 2.415 | 2.323 | 2.747 | 2.264 | 2.451 | 2.323 | 2.747 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | 0.987 | 1.001 | 2.113 | 1.882 | 2.174 | 2.064 | 1.973 | 1.869 | 2.080 | 2.064 | 1.973 | ns |
| | | $t_h$ | 1.361 | 1.408 | -1.876 | -1.387 | -1.620 | -1.542 | -1.441 | -1.361 | -1.518 | -1.542 | -1.441 | ns |
| | GCLK PLL | $t_{su}$ | -1.226 | -1.255 | -1.302 | -1.883 | -2.134 | -2.056 | -2.479 | -2.003 | -2.160 | -2.056 | -2.479 | ns |
| | | $t_h$ | 0.987 | 1.001 | -1.863 | 2.127 | 2.397 | 2.305 | 2.729 | 2.253 | 2.434 | 2.305 | 2.729 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | 1.361 | 1.408 | 2.101 | 1.892 | 2.192 | 2.082 | 1.991 | 1.880 | 2.097 | 2.082 | 1.991 | ns |
| | | $t_h$ | -1.212 | -1.243 | 1.766 | 1.892 | 2.192 | 2.082 | 1.991 | 1.880 | 2.097 | 2.082 | 1.991 | ns |
| | GCLK PLL | $t_{su}$ | 1.001 | 1.013 | 2.113 | -1.397 | -1.638 | -1.560 | -1.459 | -1.372 | -1.535 | -1.560 | -1.459 | ns |
| | | $t_h$ | 1.347 | 1.396 | -1.876 | -1.883 | -2.134 | -2.056 | -2.479 | -2.003 | -2.160 | -2.056 | -2.479 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -1.226 | -1.255 | 1.766 | -1.387 | -1.620 | -1.542 | -1.441 | -1.361 | -1.518 | -1.542 | -1.441 | ns |
| | | $t_h$ | 0.987 | 1.001 | 2.113 | -1.893 | -2.152 | -2.074 | -2.497 | -2.014 | -2.177 | -2.074 | -2.497 | ns |
| | GCLK PLL | $t_{su}$ | 1.361 | 1.408 | -1.876 | 2.137 | 2.415 | 2.323 | 2.747 | 2.264 | 2.451 | 2.323 | 2.747 | ns |
| | | $t_h$ | -1.226 | -1.255 | -1.302 | 1.882 | 2.174 | 2.064 | 1.973 | 1.869 | 2.080 | 2.064 | 1.973 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | 0.987 | 1.001 | -1.863 | -1.387 | -1.620 | -1.542 | -1.441 | -1.361 | -1.518 | -1.542 | -1.441 | ns |
| | | $t_h$ | 1.361 | 1.408 | 2.101 | -1.893 | -2.152 | -2.074 | -2.497 | -2.014 | -2.177 | -2.074 | -2.497 | ns |
| | GCLK PLL | $t_{su}$ | -1.212 | -1.243 | 1.781 | 2.137 | 2.415 | 2.323 | 2.747 | 2.264 | 2.451 | 2.323 | 2.747 | ns |
| | | $t_h$ | 1.001 | 1.013 | -1.302 | 1.882 | 2.174 | 2.064 | 1.973 | 1.869 | 2.080 | 2.064 | 1.973 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | 1.347 | 1.396 | -1.863 | -1.387 | -1.620 | -1.542 | -1.441 | -1.361 | -1.518 | -1.542 | -1.441 | ns |
| | | $t_h$ | -1.212 | -1.243 | -1.311 | 1.892 | 2.192 | 2.082 | 1.991 | 1.880 | 2.097 | 2.082 | 1.991 | ns |
| | GCLK PLL | $t_{su}$ | 1.001 | 1.013 | -1.854 | -1.397 | -1.638 | -1.560 | -1.459 | -1.372 | -1.535 | -1.560 | -1.459 | ns |
| | | $t_h$ | 1.347 | 1.396 | 2.092 | -1.883 | -2.134 | -2.056 | -2.479 | -2.003 | -2.160 | -2.056 | -2.479 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -1.203 | -1.231 | 1.790 | 2.127 | 2.397 | 2.305 | 2.729 | 2.253 | 2.434 | 2.305 | 2.729 | ns |
| | | $t_h$ | 1.010 | 1.025 | -1.311 | 1.892 | 2.192 | 2.082 | 1.991 | 1.880 | 2.097 | 2.082 | 1.991 | ns |
| | GCLK PLL | $t_{su}$ | 1.338 | 1.384 | -1.854 | -1.397 | -1.638 | -1.560 | -1.459 | -1.372 | -1.535 | -1.560 | -1.459 | ns |
| | | $t_h$ | -1.203 | -1.231 | -1.311 | 1.902 | 2.208 | 2.098 | 2.007 | 1.889 | 2.113 | 2.098 | 2.007 | ns |

**Table 1–82.** EP3SL200 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | 1.010 | 1.025 | -1.969 | -1.407 | -1.654 | -1.576 | -1.475 | -1.381 | -1.551 | -1.576 | -1.475 | ns |
| | | $t_h$ | 1.338 | 1.384 | 1.674 | -1.873 | -2.118 | -2.040 | -2.463 | -1.994 | -2.144 | -2.040 | -2.463 | ns |
| | GCLK PLL | $t_{su}$ | -1.304 | -1.332 | 2.207 | 2.117 | 2.381 | 2.289 | 2.713 | 2.244 | 2.418 | 2.289 | 2.713 | ns |
| | | $t_h$ | 1.438 | 1.484 | -1.969 | 1.902 | 2.208 | 2.098 | 2.007 | 1.889 | 2.113 | 2.098 | 2.007 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | 0.909 | 0.927 | 1.674 | -1.407 | -1.654 | -1.576 | -1.475 | -1.381 | -1.551 | -1.576 | -1.475 | ns |
| | | $t_h$ | -0.632 | -0.632 | 2.207 | -1.873 | -2.118 | -2.040 | -2.463 | -1.994 | -2.144 | -2.040 | -2.463 | ns |
| | GCLK PLL | $t_{su}$ | -1.304 | -1.332 | 2.207 | 2.117 | 2.381 | 2.289 | 2.713 | 2.244 | 2.418 | 2.289 | 2.713 | ns |
| | | $t_h$ | 1.438 | 1.484 | 2.207 | 1.902 | 2.208 | 2.098 | 2.007 | 1.889 | 2.113 | 2.098 | 2.007 | ns |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | 0.909 | 0.927 | 2.207 | -1.407 | -1.654 | -1.576 | -1.475 | -1.381 | -1.551 | -1.576 | -1.475 | ns |
| | | $t_h$ | -0.632 | -0.632 | 2.207 | -1.873 | -2.118 | -2.040 | -2.463 | -1.994 | -2.144 | -2.040 | -2.463 | ns |
| | GCLK PLL | $t_{su}$ | -1.298 | -1.321 | -1.972 | -1.978 | -2.368 | -2.291 | -2.712 | -2.132 | -2.388 | -2.291 | -2.712 | ns |
| | | $t_h$ | 1.432 | 1.473 | 1.671 | 1.862 | 1.969 | 1.850 | 1.775 | 1.751 | 1.869 | 1.850 | 1.775 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | 0.915 | 0.938 | 2.210 | 2.223 | 2.633 | 2.541 | 2.966 | 2.384 | 2.665 | 2.541 | 2.966 | ns |
| | | $t_h$ | -0.638 | -0.643 | -1.972 | -1.978 | -2.368 | -2.291 | -2.712 | -2.132 | -2.388 | -2.291 | -2.712 | ns |
| | GCLK PLL | $t_{su}$ | -1.298 | -1.321 | -1.972 | -1.978 | -2.368 | -2.291 | -2.712 | -2.132 | -2.388 | -2.291 | -2.712 | ns |
| | | $t_h$ | 1.432 | 1.473 | 1.671 | 1.862 | 1.969 | 1.850 | 1.775 | 1.751 | 1.869 | 1.850 | 1.775 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | 0.915 | 0.938 | 2.210 | 2.223 | 2.633 | 2.541 | 2.966 | 2.384 | 2.665 | 2.541 | 2.966 | ns |
| | | $t_h$ | -0.638 | -0.643 | -1.969 | -1.979 | -2.371 | -2.294 | -2.715 | -2.131 | -2.393 | -2.294 | -2.715 | ns |
| | GCLK PLL | $t_{su}$ | -1.304 | -1.332 | 2.207 | 2.224 | 2.636 | 2.544 | 2.969 | 2.383 | 2.670 | 2.544 | 2.969 | ns |
| | | $t_h$ | 1.438 | 1.484 | -1.969 | -1.979 | -2.371 | -2.294 | -2.715 | -2.131 | -2.393 | -2.294 | -2.715 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | 0.909 | 0.927 | 1.674 | 1.861 | 1.966 | 1.847 | 1.772 | 1.752 | 1.864 | 1.847 | 1.772 | ns |
| | | $t_h$ | -0.632 | -0.632 | 2.207 | 2.224 | 2.636 | 2.544 | 2.969 | 2.383 | 2.670 | 2.544 | 2.969 | ns |
| | GCLK PLL | $t_{su}$ | -1.304 | -1.332 | 2.216 | 2.237 | 2.651 | 2.559 | 2.984 | 2.392 | 2.680 | 2.559 | 2.984 | ns |
| | | $t_h$ | 1.438 | 1.484 | -1.978 | -1.992 | -2.386 | -2.309 | -2.730 | -2.140 | -2.403 | -2.309 | -2.730 | ns |

Table 1–83 lists the EP3SL200 column pins output timing parameters for single-ended I/O standards.

**Table 1–83.** EP3SL200 Column Pins Output Timing Parameters (Part 1 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.677 | 3.677 | 5.302 | 5.492 | 5.997 | 5.854 | 6.259 | 5.492 | 5.997 | 5.854 | 6.259 | ns |
| | | GCLK PLL | $t_{co}$ | 4.076 | 4.076 | 5.937 | 6.132 | 6.701 | 6.529 | 7.016 | 6.132 | 6.701 | 6.529 | 7.016 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.610 | 3.610 | 5.193 | 5.381 | 5.884 | 5.741 | 6.146 | 5.381 | 5.884 | 5.741 | 6.146 | ns |
| | | GCLK PLL | $t_{co}$ | 4.009 | 4.009 | 5.828 | 6.021 | 6.588 | 6.416 | 6.903 | 6.021 | 6.588 | 6.416 | 6.903 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.524 | 3.524 | 5.089 | 5.282 | 5.792 | 5.649 | 6.054 | 5.282 | 5.792 | 5.649 | 6.054 | ns |
| | | GCLK PLL | $t_{co}$ | 3.923 | 3.923 | 5.724 | 5.922 | 6.496 | 6.324 | 6.811 | 5.922 | 6.496 | 6.324 | 6.811 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.517 | 3.517 | 5.072 | 5.254 | 5.751 | 5.608 | 6.013 | 5.254 | 5.751 | 5.608 | 6.013 | ns |
| | | GCLK PLL | $t_{co}$ | 3.916 | 3.916 | 5.707 | 5.894 | 6.455 | 6.283 | 6.770 | 5.894 | 6.455 | 6.283 | 6.770 | ns |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.683 | 3.683 | 5.306 | 5.497 | 6.004 | 5.861 | 6.266 | 5.497 | 6.004 | 5.861 | 6.266 | ns |
| | | GCLK PLL | $t_{co}$ | 4.082 | 4.082 | 5.941 | 6.137 | 6.708 | 6.536 | 7.023 | 6.137 | 6.708 | 6.536 | 7.023 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.528 | 3.528 | 5.099 | 5.299 | 5.803 | 5.660 | 6.065 | 5.299 | 5.803 | 5.660 | 6.065 | ns |
| | | GCLK PLL | $t_{co}$ | 3.927 | 3.927 | 5.734 | 5.939 | 6.507 | 6.335 | 6.822 | 5.939 | 6.507 | 6.335 | 6.822 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.535 | 3.535 | 5.093 | 5.278 | 5.777 | 5.634 | 6.039 | 5.278 | 5.777 | 5.634 | 6.039 | ns |
| | | GCLK PLL | $t_{co}$ | 3.934 | 3.934 | 5.728 | 5.918 | 6.481 | 6.309 | 6.796 | 5.918 | 6.481 | 6.309 | 6.796 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.519 | 3.519 | 5.071 | 5.253 | 5.748 | 5.605 | 6.010 | 5.253 | 5.748 | 5.605 | 6.010 | ns |
| | | GCLK PLL | $t_{co}$ | 3.918 | 3.918 | 5.706 | 5.893 | 6.452 | 6.280 | 6.767 | 5.893 | 6.452 | 6.280 | 6.767 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.641 | 3.641 | 5.269 | 5.460 | 5.964 | 5.821 | 6.226 | 5.460 | 5.964 | 5.821 | 6.226 | ns |
| | | GCLK PLL | $t_{co}$ | 4.040 | 4.040 | 5.904 | 6.100 | 6.668 | 6.496 | 6.983 | 6.100 | 6.668 | 6.496 | 6.983 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.530 | 3.530 | 5.139 | 5.326 | 5.826 | 5.684 | 6.088 | 5.326 | 5.826 | 5.684 | 6.088 | ns |
| | | GCLK PLL | $t_{co}$ | 3.929 | 3.929 | 5.774 | 5.966 | 6.531 | 6.360 | 6.845 | 5.966 | 6.531 | 6.360 | 6.845 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.494 | 3.494 | 5.076 | 5.257 | 5.752 | 5.610 | 6.014 | 5.257 | 5.752 | 5.610 | 6.014 | ns |
| | | GCLK PLL | $t_{co}$ | 3.893 | 3.893 | 5.711 | 5.897 | 6.457 | 6.286 | 6.771 | 5.897 | 6.457 | 6.286 | 6.771 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.476 | 3.476 | 5.047 | 5.229 | 5.724 | 5.581 | 5.986 | 5.229 | 5.724 | 5.581 | 5.986 | ns |
| | | GCLK PLL | $t_{co}$ | 3.875 | 3.875 | 5.682 | 5.869 | 6.428 | 6.256 | 6.743 | 5.869 | 6.428 | 6.256 | 6.743 | ns |

**Table 1–83.** EP3SL200 Column Pins Output Timing Parameters (Part 2 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.555 | 3.555 | 5.173 | 5.360 | 5.861 | 5.719 | 6.123 | 5.360 | 5.861 | 5.719 | 6.123 | ns |
| | | GCLK PLL | $t_{co}$ | 3.954 | 3.954 | 5.808 | 6.000 | 6.566 | 6.395 | 6.880 | 6.000 | 6.566 | 6.395 | 6.880 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.476 | 3.476 | 5.049 | 5.231 | 5.726 | 5.584 | 5.988 | 5.231 | 5.726 | 5.584 | 5.988 | ns |
| | | GCLK PLL | $t_{co}$ | 3.875 | 3.875 | 5.684 | 5.871 | 6.431 | 6.260 | 6.745 | 5.871 | 6.431 | 6.260 | 6.745 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.471 | 3.471 | 5.042 | 5.224 | 5.718 | 5.575 | 5.980 | 5.224 | 5.718 | 5.575 | 5.980 | ns |
| | | GCLK PLL | $t_{co}$ | 3.870 | 3.870 | 5.677 | 5.864 | 6.422 | 6.250 | 6.737 | 5.864 | 6.422 | 6.250 | 6.737 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.462 | 3.462 | 5.028 | 5.209 | 5.703 | 5.560 | 5.965 | 5.209 | 5.703 | 5.560 | 5.965 | ns |
| | | GCLK PLL | $t_{co}$ | 3.861 | 3.861 | 5.663 | 5.849 | 6.407 | 6.235 | 6.722 | 5.849 | 6.407 | 6.235 | 6.722 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.677 | 3.677 | 5.380 | 5.587 | 6.108 | 5.966 | 6.370 | 5.587 | 6.108 | 5.966 | 6.370 | ns |
| | | GCLK PLL | $t_{co}$ | 4.076 | 4.076 | 6.015 | 6.227 | 6.813 | 6.642 | 7.127 | 6.227 | 6.813 | 6.642 | 7.127 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.577 | 3.577 | 5.261 | 5.461 | 5.976 | 5.834 | 6.238 | 5.461 | 5.976 | 5.834 | 6.238 | ns |
| | | GCLK PLL | $t_{co}$ | 3.976 | 3.976 | 5.896 | 6.101 | 6.681 | 6.510 | 6.995 | 6.101 | 6.681 | 6.510 | 6.995 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.533 | 3.533 | 5.174 | 5.370 | 5.881 | 5.738 | 6.143 | 5.370 | 5.881 | 5.738 | 6.143 | ns |
| | | GCLK PLL | $t_{co}$ | 3.932 | 3.932 | 5.809 | 6.010 | 6.585 | 6.413 | 6.900 | 6.010 | 6.585 | 6.413 | 6.900 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.495 | 3.495 | 5.135 | 5.328 | 5.838 | 5.695 | 6.100 | 5.328 | 5.838 | 5.695 | 6.100 | ns |
| | | GCLK PLL | $t_{co}$ | 3.894 | 3.894 | 5.770 | 5.968 | 6.542 | 6.370 | 6.857 | 5.968 | 6.542 | 6.370 | 6.857 | ns |

**Table 1–83.** EP3SL200 Column Pins Output Timing Parameters (Part 3 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.868 | 3.868 | 5.701 | 5.947 | 6.513 | 6.370 | 6.775 | 5.947 | 6.513 | 6.370 | 6.775 | ns |
| | | GCLK PLL | $t_{co}$ | 4.267 | 4.267 | 6.336 | 6.587 | 7.217 | 7.045 | 7.532 | 6.587 | 7.217 | 7.045 | 7.532 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.687 | 3.687 | 5.422 | 5.638 | 6.165 | 6.023 | 6.427 | 5.638 | 6.165 | 6.023 | 6.427 | ns |
| | | GCLK PLL | $t_{co}$ | 4.086 | 4.086 | 6.057 | 6.278 | 6.870 | 6.699 | 7.184 | 6.278 | 6.870 | 6.699 | 7.184 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.605 | 3.605 | 5.315 | 5.523 | 6.055 | 5.912 | 6.317 | 5.523 | 6.055 | 5.912 | 6.317 | ns |
| | | GCLK PLL | $t_{co}$ | 4.004 | 4.004 | 5.950 | 6.163 | 6.759 | 6.587 | 7.074 | 6.163 | 6.759 | 6.587 | 7.074 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.585 | 3.585 | 5.257 | 5.469 | 5.989 | 5.846 | 6.251 | 5.469 | 5.989 | 5.846 | 6.251 | ns |
| | | GCLK PLL | $t_{co}$ | 3.984 | 3.984 | 5.892 | 6.109 | 6.693 | 6.521 | 7.008 | 6.109 | 6.693 | 6.521 | 7.008 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.522 | 3.522 | 5.196 | 5.394 | 5.908 | 5.765 | 6.170 | 5.394 | 5.908 | 5.765 | 6.170 | ns |
| | | GCLK PLL | $t_{co}$ | 3.921 | 3.921 | 5.831 | 6.034 | 6.612 | 6.440 | 6.927 | 6.034 | 6.612 | 6.440 | 6.927 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.504 | 3.504 | 5.175 | 5.373 | 5.885 | 5.742 | 6.147 | 5.373 | 5.885 | 5.742 | 6.147 | ns |
| | | GCLK PLL | $t_{co}$ | 3.903 | 3.903 | 5.810 | 6.013 | 6.589 | 6.417 | 6.904 | 6.013 | 6.589 | 6.417 | 6.904 | ns |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.814 | 3.814 | 5.630 | 5.879 | 6.451 | 6.308 | 6.713 | 5.879 | 6.451 | 6.308 | 6.713 | ns |
| | | GCLK PLL | $t_{co}$ | 4.213 | 4.213 | 6.265 | 6.519 | 7.155 | 6.983 | 7.470 | 6.519 | 7.155 | 6.983 | 7.470 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.602 | 3.602 | 5.311 | 5.523 | 6.059 | 5.916 | 6.321 | 5.523 | 6.059 | 5.916 | 6.321 | ns |
| | | GCLK PLL | $t_{co}$ | 4.001 | 4.001 | 5.946 | 6.163 | 6.763 | 6.591 | 7.078 | 6.163 | 6.763 | 6.591 | 7.078 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.577 | 3.577 | 5.244 | 5.463 | 5.992 | 5.849 | 6.254 | 5.463 | 5.992 | 5.849 | 6.254 | ns |
| | | GCLK PLL | $t_{co}$ | 3.976 | 3.976 | 5.879 | 6.103 | 6.696 | 6.524 | 7.011 | 6.103 | 6.696 | 6.524 | 7.011 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.566 | 3.566 | 5.227 | 5.438 | 5.972 | 5.829 | 6.234 | 5.438 | 5.972 | 5.829 | 6.234 | ns |
| | | GCLK PLL | $t_{co}$ | 3.965 | 3.965 | 5.862 | 6.078 | 6.676 | 6.504 | 6.991 | 6.078 | 6.676 | 6.504 | 6.991 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.511 | 3.511 | 5.189 | 5.387 | 5.902 | 5.759 | 6.164 | 5.387 | 5.902 | 5.759 | 6.164 | ns |
| | | GCLK PLL | $t_{co}$ | 3.910 | 3.910 | 5.824 | 6.027 | 6.606 | 6.434 | 6.921 | 6.027 | 6.606 | 6.434 | 6.921 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.506 | 3.506 | 5.172 | 5.376 | 5.891 | 5.748 | 6.153 | 5.376 | 5.891 | 5.748 | 6.153 | ns |
| | | GCLK PLL | $t_{co}$ | 3.905 | 3.905 | 5.807 | 6.016 | 6.595 | 6.423 | 6.910 | 6.016 | 6.595 | 6.423 | 6.910 | ns |


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**Table 1–83.** EP3SL200 Column Pins Output Timing Parameters (Part 4 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.730 | 3.730 | 5.556 | 5.815 | 6.395 | 6.252 | 6.657 | 5.815 | 6.395 | 6.252 | 6.657 | ns |
| | | GCLK PLL | $t_{co}$ | 4.129 | 4.129 | 6.191 | 6.455 | 7.099 | 6.927 | 7.414 | 6.455 | 7.099 | 6.927 | 7.414 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.607 | 3.607 | 5.330 | 5.553 | 6.109 | 5.966 | 6.371 | 5.553 | 6.109 | 5.966 | 6.371 | ns |
| | | GCLK PLL | $t_{co}$ | 4.006 | 4.006 | 5.965 | 6.193 | 6.813 | 6.641 | 7.128 | 6.193 | 6.813 | 6.641 | 7.128 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.569 | 3.569 | 5.238 | 5.464 | 5.996 | 5.853 | 6.258 | 5.464 | 5.996 | 5.853 | 6.258 | ns |
| | | GCLK PLL | $t_{co}$ | 3.968 | 3.968 | 5.873 | 6.104 | 6.700 | 6.528 | 7.015 | 6.104 | 6.700 | 6.528 | 7.015 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.522 | 3.522 | 5.210 | 5.415 | 5.940 | 5.797 | 6.202 | 5.415 | 5.940 | 5.797 | 6.202 | ns |
| | | GCLK PLL | $t_{co}$ | 3.921 | 3.921 | 5.845 | 6.055 | 6.644 | 6.472 | 6.959 | 6.055 | 6.644 | 6.472 | 6.959 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.522 | 3.522 | 5.167 | 5.362 | 5.871 | 5.728 | 6.133 | 5.362 | 5.871 | 5.728 | 6.133 | ns |
| | | GCLK PLL | $t_{co}$ | 3.921 | 3.921 | 5.802 | 6.002 | 6.575 | 6.403 | 6.890 | 6.002 | 6.575 | 6.403 | 6.890 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.519 | 3.519 | 5.164 | 5.359 | 5.867 | 5.724 | 6.129 | 5.359 | 5.867 | 5.724 | 6.129 | ns |
| | | GCLK PLL | $t_{co}$ | 3.918 | 3.918 | 5.799 | 5.999 | 6.571 | 6.399 | 6.886 | 5.999 | 6.571 | 6.399 | 6.886 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.517 | 3.517 | 5.164 | 5.360 | 5.868 | 5.725 | 6.130 | 5.360 | 5.868 | 5.725 | 6.130 | ns |
| | | GCLK PLL | $t_{co}$ | 3.916 | 3.916 | 5.799 | 6.000 | 6.572 | 6.400 | 6.887 | 6.000 | 6.572 | 6.400 | 6.887 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.508 | 3.508 | 5.149 | 5.344 | 5.853 | 5.710 | 6.115 | 5.344 | 5.853 | 5.710 | 6.115 | ns |
| | | GCLK PLL | $t_{co}$ | 3.907 | 3.907 | 5.784 | 5.984 | 6.557 | 6.385 | 6.872 | 5.984 | 6.557 | 6.385 | 6.872 | ns |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.529 | 3.529 | 5.179 | 5.376 | 5.887 | 5.744 | 6.149 | 5.376 | 5.887 | 5.744 | 6.149 | ns |
| | | GCLK PLL | $t_{co}$ | 3.928 | 3.928 | 5.814 | 6.016 | 6.591 | 6.419 | 6.906 | 6.016 | 6.591 | 6.419 | 6.906 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.525 | 3.525 | 5.177 | 5.374 | 5.885 | 5.742 | 6.147 | 5.374 | 5.885 | 5.742 | 6.147 | ns |
| | | GCLK PLL | $t_{co}$ | 3.924 | 3.924 | 5.812 | 6.014 | 6.589 | 6.417 | 6.904 | 6.014 | 6.589 | 6.417 | 6.904 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.514 | 3.514 | 5.167 | 5.365 | 5.876 | 5.733 | 6.138 | 5.365 | 5.876 | 5.733 | 6.138 | ns |
| | | GCLK PLL | $t_{co}$ | 3.913 | 3.913 | 5.802 | 6.005 | 6.580 | 6.408 | 6.895 | 6.005 | 6.580 | 6.408 | 6.895 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.503 | 3.503 | 5.154 | 5.352 | 5.863 | 5.720 | 6.125 | 5.352 | 5.863 | 5.720 | 6.125 | ns |
| | | GCLK PLL | $t_{co}$ | 3.902 | 3.902 | 5.789 | 5.992 | 6.567 | 6.395 | 6.882 | 5.992 | 6.567 | 6.395 | 6.882 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.503 | 3.503 | 5.154 | 5.352 | 5.863 | 5.720 | 6.125 | 5.352 | 5.863 | 5.720 | 6.125 | ns |
| | | GCLK PLL | $t_{co}$ | 3.902 | 3.902 | 5.789 | 5.992 | 6.567 | 6.395 | 6.882 | 5.992 | 6.567 | 6.395 | 6.882 | ns |

**Table 1–83.** EP3SL200 Column Pins Output Timing Parameters (Part 5 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.509 | 3.509 | 5.153 | 5.349 | 5.858 | 5.715 | 6.120 | 5.349 | 5.858 | 5.715 | 6.120 | ns |
| | | GCLK PLL | $t_{co}$ | 3.908 | 3.908 | 5.788 | 5.989 | 6.562 | 6.390 | 6.877 | 5.989 | 6.562 | 6.390 | 6.877 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.512 | 3.512 | 5.161 | 5.358 | 5.870 | 5.727 | 6.132 | 5.358 | 5.870 | 5.727 | 6.132 | ns |
| | | GCLK PLL | $t_{co}$ | 3.911 | 3.911 | 5.796 | 5.998 | 6.574 | 6.402 | 6.889 | 5.998 | 6.574 | 6.402 | 6.889 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.533 | 3.533 | 5.188 | 5.388 | 5.900 | 5.757 | 6.162 | 5.388 | 5.900 | 5.757 | 6.162 | ns |
| | | GCLK PLL | $t_{co}$ | 3.932 | 3.932 | 5.823 | 6.028 | 6.604 | 6.432 | 6.919 | 6.028 | 6.604 | 6.432 | 6.919 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.519 | 3.519 | 5.178 | 5.378 | 5.891 | 5.748 | 6.153 | 5.378 | 5.891 | 5.748 | 6.153 | ns |
| | | GCLK PLL | $t_{co}$ | 3.918 | 3.918 | 5.813 | 6.018 | 6.595 | 6.423 | 6.910 | 6.018 | 6.595 | 6.423 | 6.910 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.508 | 3.508 | 5.164 | 5.364 | 5.877 | 5.734 | 6.139 | 5.364 | 5.877 | 5.734 | 6.139 | ns |
| | | GCLK PLL | $t_{co}$ | 3.907 | 3.907 | 5.799 | 6.004 | 6.581 | 6.409 | 6.896 | 6.004 | 6.581 | 6.409 | 6.896 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.507 | 3.507 | 5.167 | 5.367 | 5.881 | 5.738 | 6.143 | 5.367 | 5.881 | 5.738 | 6.143 | ns |
| | | GCLK PLL | $t_{co}$ | 3.906 | 3.906 | 5.802 | 6.007 | 6.585 | 6.413 | 6.900 | 6.007 | 6.585 | 6.413 | 6.900 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.504 | 3.504 | 5.162 | 5.362 | 5.875 | 5.732 | 6.137 | 5.362 | 5.875 | 5.732 | 6.137 | ns |
| | | GCLK PLL | $t_{co}$ | 3.903 | 3.903 | 5.797 | 6.002 | 6.579 | 6.407 | 6.894 | 6.002 | 6.579 | 6.407 | 6.894 | ns |
| SSTL-15 CLASS II | 8mA | GCLK | $t_{co}$ | 3.506 | 3.506 | 5.151 | 5.348 | 5.858 | 5.715 | 6.120 | 5.348 | 5.858 | 5.715 | 6.120 | ns |
| | | GCLK PLL | $t_{co}$ | 3.905 | 3.905 | 5.786 | 5.988 | 6.562 | 6.390 | 6.877 | 5.988 | 6.562 | 6.390 | 6.877 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.509 | 3.509 | 5.158 | 5.357 | 5.869 | 5.726 | 6.131 | 5.357 | 5.869 | 5.726 | 6.131 | ns |
| | | GCLK PLL | $t_{co}$ | 3.908 | 3.908 | 5.793 | 5.997 | 6.573 | 6.401 | 6.888 | 5.997 | 6.573 | 6.401 | 6.888 | ns |


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**Table 1–83.** EP3SL200 Column Pins Output Timing Parameters (Part 6 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.516 | 3.516 | 5.153 | 5.348 | 5.856 | 5.713 | 6.118 | 5.348 | 5.856 | 5.713 | 6.118 | ns |
| | | GCLK PLL | $t_{co}$ | 3.915 | 3.915 | 5.788 | 5.988 | 6.560 | 6.388 | 6.875 | 5.988 | 6.560 | 6.388 | 6.875 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.509 | 3.509 | 5.151 | 5.346 | 5.855 | 5.712 | 6.117 | 5.346 | 5.855 | 5.712 | 6.117 | ns |
| | | GCLK PLL | $t_{co}$ | 3.908 | 3.908 | 5.786 | 5.986 | 6.559 | 6.387 | 6.874 | 5.986 | 6.559 | 6.387 | 6.874 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.501 | 3.501 | 5.143 | 5.339 | 5.848 | 5.705 | 6.110 | 5.339 | 5.848 | 5.705 | 6.110 | ns |
| | | GCLK PLL | $t_{co}$ | 3.900 | 3.900 | 5.778 | 5.979 | 6.552 | 6.380 | 6.867 | 5.979 | 6.552 | 6.380 | 6.867 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.504 | 3.504 | 5.146 | 5.342 | 5.852 | 5.709 | 6.114 | 5.342 | 5.852 | 5.709 | 6.114 | ns |
| | | GCLK PLL | $t_{co}$ | 3.903 | 3.903 | 5.781 | 5.982 | 6.556 | 6.384 | 6.871 | 5.982 | 6.556 | 6.384 | 6.871 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.501 | 3.501 | 5.149 | 5.346 | 5.856 | 5.713 | 6.118 | 5.346 | 5.856 | 5.713 | 6.118 | ns |
| | | GCLK PLL | $t_{co}$ | 3.900 | 3.900 | 5.784 | 5.986 | 6.560 | 6.388 | 6.875 | 5.986 | 6.560 | 6.388 | 6.875 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.509 | 3.509 | 5.148 | 5.343 | 5.852 | 5.709 | 6.114 | 5.343 | 5.852 | 5.709 | 6.114 | ns |
| | | GCLK PLL | $t_{co}$ | 3.908 | 3.908 | 5.783 | 5.983 | 6.556 | 6.384 | 6.871 | 5.983 | 6.556 | 6.384 | 6.871 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.521 | 3.521 | 5.161 | 5.358 | 5.867 | 5.724 | 6.129 | 5.358 | 5.867 | 5.724 | 6.129 | ns |
| | | GCLK PLL | $t_{co}$ | 3.920 | 3.920 | 5.796 | 5.998 | 6.571 | 6.399 | 6.886 | 5.998 | 6.571 | 6.399 | 6.886 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.517 | 3.517 | 5.162 | 5.359 | 5.870 | 5.727 | 6.132 | 5.359 | 5.870 | 5.727 | 6.132 | ns |
| | | GCLK PLL | $t_{co}$ | 3.916 | 3.916 | 5.797 | 5.999 | 6.574 | 6.402 | 6.889 | 5.999 | 6.574 | 6.402 | 6.889 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.513 | 3.513 | 5.158 | 5.355 | 5.865 | 5.722 | 6.127 | 5.355 | 5.865 | 5.722 | 6.127 | ns |
| | | GCLK PLL | $t_{co}$ | 3.912 | 3.912 | 5.793 | 5.995 | 6.569 | 6.397 | 6.884 | 5.995 | 6.569 | 6.397 | 6.884 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.506 | 3.506 | 5.151 | 5.348 | 5.858 | 5.715 | 6.120 | 5.348 | 5.858 | 5.715 | 6.120 | ns |
| | | GCLK PLL | $t_{co}$ | 3.905 | 3.905 | 5.786 | 5.988 | 6.562 | 6.390 | 6.877 | 5.988 | 6.562 | 6.390 | 6.877 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.507 | 3.507 | 5.158 | 5.356 | 5.868 | 5.725 | 6.130 | 5.356 | 5.868 | 5.725 | 6.130 | ns |
| | | GCLK PLL | $t_{co}$ | 3.906 | 3.906 | 5.793 | 5.996 | 6.572 | 6.400 | 6.887 | 5.996 | 6.572 | 6.400 | 6.887 | ns |
| 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.505 | 3.505 | 5.139 | 5.334 | 5.842 | 5.699 | 6.104 | 5.334 | 5.842 | 5.699 | 6.104 | ns |
| | | GCLK PLL | $t_{co}$ | 3.904 | 3.904 | 5.774 | 5.974 | 6.546 | 6.374 | 6.861 | 5.974 | 6.546 | 6.374 | 6.861 | ns |

**Table 1–83.** EP3SL200 Column Pins Output Timing Parameters (Part 7 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.524 | 3.524 | 5.175 | 5.375 | 5.888 | 5.745 | 6.150 | 5.375 | 5.888 | 5.745 | 6.150 | ns |
| | | GCLK PLL | $t_{co}$ | 3.923 | 3.923 | 5.810 | 6.015 | 6.592 | 6.420 | 6.907 | 6.015 | 6.592 | 6.420 | 6.907 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.516 | 3.516 | 5.166 | 5.366 | 5.879 | 5.736 | 6.141 | 5.366 | 5.879 | 5.736 | 6.141 | ns |
| | | GCLK PLL | $t_{co}$ | 3.915 | 3.915 | 5.801 | 6.006 | 6.583 | 6.411 | 6.898 | 6.006 | 6.583 | 6.411 | 6.898 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.517 | 3.517 | 5.174 | 5.374 | 5.888 | 5.745 | 6.150 | 5.374 | 5.888 | 5.745 | 6.150 | ns |
| | | GCLK PLL | $t_{co}$ | 3.916 | 3.916 | 5.809 | 6.014 | 6.592 | 6.420 | 6.907 | 6.014 | 6.592 | 6.420 | 6.907 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.506 | 3.506 | 5.161 | 5.361 | 5.874 | 5.731 | 6.136 | 5.361 | 5.874 | 5.731 | 6.136 | ns |
| | | GCLK PLL | $t_{co}$ | 3.905 | 3.905 | 5.796 | 6.001 | 6.578 | 6.406 | 6.893 | 6.001 | 6.578 | 6.406 | 6.893 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.506 | 3.506 | 5.161 | 5.361 | 5.875 | 5.732 | 6.137 | 5.361 | 5.875 | 5.732 | 6.137 | ns |
| | | GCLK PLL | $t_{co}$ | 3.905 | 3.905 | 5.796 | 6.001 | 6.579 | 6.407 | 6.894 | 6.001 | 6.579 | 6.407 | 6.894 | ns |
| 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.527 | 3.527 | 5.177 | 5.376 | 5.888 | 5.745 | 6.150 | 5.376 | 5.888 | 5.745 | 6.150 | ns |
| | | GCLK PLL | $t_{co}$ | 3.926 | 3.926 | 5.812 | 6.016 | 6.592 | 6.420 | 6.907 | 6.016 | 6.592 | 6.420 | 6.907 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.630 | 3.630 | 5.222 | 5.410 | 5.913 | 5.770 | 6.175 | 5.410 | 5.913 | 5.770 | 6.175 | ns |
| | | GCLK PLL | $t_{co}$ | 4.029 | 4.029 | 5.857 | 6.050 | 6.617 | 6.445 | 6.932 | 6.050 | 6.617 | 6.445 | 6.932 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.630 | 3.630 | 5.222 | 5.410 | 5.913 | 5.770 | 6.175 | 5.410 | 5.913 | 5.770 | 6.175 | ns |
| | | GCLK PLL | $t_{co}$ | 4.029 | 4.029 | 5.857 | 6.050 | 6.617 | 6.445 | 6.932 | 6.050 | 6.617 | 6.445 | 6.932 | ns |

Table 1–84 lists the EP3SL200 row pins output timing parameters for single-ended I/O standards.

**Table 1–84.** EP3SL200 Row Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.639 | 3.902 | 5.663 | 5.916 | 6.397 | 6.238 | 6.709 | 6.053 | 6.634 | 6.238 | 6.709 | ns |
| | | GCLK PLL | $t_{co}$ | 1.551 | 1.768 | 2.210 | 2.317 | 2.505 | 2.518 | 2.444 | 2.409 | 2.649 | 2.518 | 2.444 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.548 | 3.813 | 5.533 | 5.778 | 6.283 | 6.124 | 6.565 | 5.912 | 6.485 | 6.124 | 6.565 | ns |
| | | GCLK PLL | $t_{co}$ | 1.468 | 1.663 | 2.080 | 2.179 | 2.361 | 2.374 | 2.300 | 2.268 | 2.500 | 2.374 | 2.300 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.469 | 3.724 | 5.414 | 5.655 | 6.187 | 6.028 | 6.437 | 5.785 | 6.353 | 6.028 | 6.437 | ns |
| | | GCLK PLL | $t_{co}$ | 1.389 | 1.560 | 1.961 | 2.056 | 2.233 | 2.246 | 2.172 | 2.147 | 2.368 | 2.246 | 2.172 | ns |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.649 | 3.906 | 5.671 | 5.921 | 6.406 | 6.247 | 6.714 | 6.059 | 6.639 | 6.247 | 6.714 | ns |
| | | GCLK PLL | $t_{co}$ | 1.561 | 1.772 | 2.218 | 2.322 | 2.510 | 2.523 | 2.449 | 2.415 | 2.654 | 2.523 | 2.449 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.473 | 3.728 | 5.420 | 5.661 | 6.197 | 6.038 | 6.443 | 5.794 | 6.360 | 6.038 | 6.443 | ns |
| | | GCLK PLL | $t_{co}$ | 1.393 | 1.564 | 1.967 | 2.062 | 2.239 | 2.252 | 2.178 | 2.159 | 2.375 | 2.252 | 2.178 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.593 | 3.848 | 5.615 | 5.869 | 6.363 | 6.204 | 6.666 | 6.010 | 6.592 | 6.204 | 6.666 | ns |
| | | GCLK PLL | $t_{co}$ | 1.505 | 1.714 | 2.162 | 2.270 | 2.462 | 2.475 | 2.401 | 2.366 | 2.607 | 2.475 | 2.401 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.474 | 3.733 | 5.463 | 5.710 | 6.218 | 6.059 | 6.502 | 5.848 | 6.428 | 6.059 | 6.502 | ns |
| | | GCLK PLL | $t_{co}$ | 1.394 | 1.587 | 2.010 | 2.111 | 2.298 | 2.311 | 2.237 | 2.204 | 2.443 | 2.311 | 2.237 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.437 | 3.695 | 5.395 | 5.627 | 6.148 | 5.989 | 6.414 | 5.762 | 6.335 | 5.989 | 6.414 | ns |
| | | GCLK PLL | $t_{co}$ | 1.357 | 1.536 | 1.928 | 2.028 | 2.210 | 2.223 | 2.149 | 2.118 | 2.350 | 2.223 | 2.149 | ns |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.507 | 3.767 | 5.510 | 5.762 | 6.254 | 6.095 | 6.555 | 5.902 | 6.481 | 6.095 | 6.555 | ns |
| | | GCLK PLL | $t_{co}$ | 1.419 | 1.633 | 2.057 | 2.163 | 2.351 | 2.364 | 2.290 | 2.258 | 2.496 | 2.364 | 2.290 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.424 | 3.679 | 5.368 | 5.588 | 6.120 | 5.961 | 6.375 | 5.722 | 6.295 | 5.961 | 6.375 | ns |
| | | GCLK PLL | $t_{co}$ | 1.344 | 1.515 | 1.893 | 1.989 | 2.171 | 2.184 | 2.110 | 2.087 | 2.310 | 2.184 | 2.110 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.619 | 3.884 | 5.748 | 6.023 | 6.508 | 6.349 | 6.838 | 6.170 | 6.771 | 6.349 | 6.838 | ns |
| | | GCLK PLL | $t_{co}$ | 1.531 | 1.750 | 2.295 | 2.424 | 2.634 | 2.647 | 2.573 | 2.526 | 2.786 | 2.647 | 2.573 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.516 | 3.785 | 5.593 | 5.860 | 6.366 | 6.207 | 6.668 | 6.003 | 6.597 | 6.207 | 6.668 | ns |
| | | GCLK PLL | $t_{co}$ | 1.436 | 1.651 | 2.140 | 2.261 | 2.464 | 2.477 | 2.403 | 2.359 | 2.612 | 2.477 | 2.403 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.463 | 3.735 | 5.492 | 5.741 | 6.275 | 6.116 | 6.542 | 5.880 | 6.467 | 6.116 | 6.542 | ns |
| | | GCLK PLL | $t_{co}$ | 1.379 | 1.575 | 2.029 | 2.142 | 2.338 | 2.351 | 2.277 | 2.236 | 2.482 | 2.351 | 2.277 | ns |

**Table 1–84.** EP3SL200 Row Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.863 | 4.170 | 6.174 | 6.451 | 7.093 | 6.933 | 7.278 | 6.617 | 7.250 | 6.933 | 7.278 | ns |
| | | GCLK PLL | $t_{co}$ | 1.795 | 2.018 | 2.703 | 2.852 | 3.121 | 3.130 | 3.066 | 2.995 | 3.095 | 3.130 | 3.066 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.638 | 3.968 | 5.848 | 6.083 | 6.688 | 6.528 | 6.873 | 6.252 | 6.844 | 6.528 | 6.873 | ns |
| | | GCLK PLL | $t_{co}$ | 1.570 | 1.816 | 2.377 | 2.484 | 2.716 | 2.725 | 2.661 | 2.630 | 2.734 | 2.725 | 2.661 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.573 | 3.866 | 5.694 | 5.933 | 6.529 | 6.369 | 6.714 | 6.084 | 6.671 | 6.369 | 6.714 | ns |
| | | GCLK PLL | $t_{co}$ | 1.505 | 1.714 | 2.223 | 2.334 | 2.557 | 2.566 | 2.502 | 2.462 | 2.628 | 2.566 | 2.502 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.521 | 3.792 | 5.617 | 5.840 | 6.433 | 6.273 | 6.618 | 5.989 | 6.577 | 6.273 | 6.618 | ns |
| | | GCLK PLL | $t_{co}$ | 1.445 | 1.640 | 2.146 | 2.241 | 2.461 | 2.470 | 2.406 | 2.367 | 2.556 | 2.470 | 2.406 | ns |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.774 | 4.088 | 6.084 | 6.365 | 7.021 | 6.861 | 7.206 | 6.524 | 7.174 | 6.861 | 7.206 | ns |
| | | GCLK PLL | $t_{co}$ | 1.706 | 1.936 | 2.613 | 2.766 | 3.049 | 3.058 | 2.994 | 2.902 | 3.030 | 3.058 | 2.994 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.537 | 3.831 | 5.679 | 5.928 | 6.530 | 6.370 | 6.715 | 6.078 | 6.670 | 6.370 | 6.715 | ns |
| | | GCLK PLL | $t_{co}$ | 1.464 | 1.679 | 2.208 | 2.329 | 2.558 | 2.567 | 2.503 | 2.456 | 2.629 | 2.567 | 2.503 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.510 | 3.783 | 5.606 | 5.832 | 6.424 | 6.264 | 6.609 | 5.980 | 6.565 | 6.264 | 6.609 | ns |
| | | GCLK PLL | $t_{co}$ | 1.437 | 1.631 | 2.135 | 2.233 | 2.452 | 2.461 | 2.397 | 2.358 | 2.556 | 2.461 | 2.397 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.496 | 3.774 | 5.584 | 5.814 | 6.405 | 6.245 | 6.590 | 5.962 | 6.543 | 6.245 | 6.590 | ns |
| | | GCLK PLL | $t_{co}$ | 1.428 | 1.622 | 2.113 | 2.215 | 2.433 | 2.442 | 2.378 | 2.340 | 2.537 | 2.442 | 2.378 | ns |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.717 | 4.013 | 5.994 | 6.279 | 6.946 | 6.786 | 7.131 | 6.436 | 7.090 | 6.786 | 7.131 | ns |
| | | GCLK PLL | $t_{co}$ | 1.649 | 1.861 | 2.523 | 2.680 | 2.974 | 2.983 | 2.919 | 2.814 | 2.961 | 2.983 | 2.919 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.542 | 3.824 | 5.701 | 5.956 | 6.571 | 6.411 | 6.756 | 6.103 | 6.712 | 6.411 | 6.756 | ns |
| | | GCLK PLL | $t_{co}$ | 1.469 | 1.672 | 2.230 | 2.357 | 2.599 | 2.608 | 2.544 | 2.481 | 2.673 | 2.608 | 2.544 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.463 | 3.723 | 5.485 | 5.713 | 6.265 | 6.106 | 6.510 | 5.855 | 6.429 | 6.106 | 6.510 | ns |
| | | GCLK PLL | $t_{co}$ | 1.383 | 1.561 | 2.006 | 2.114 | 2.306 | 2.319 | 2.245 | 2.220 | 2.444 | 2.319 | 2.245 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.458 | 3.719 | 5.482 | 5.705 | 6.263 | 6.104 | 6.502 | 5.854 | 6.422 | 6.104 | 6.502 | ns |
| | | GCLK PLL | $t_{co}$ | 1.378 | 1.555 | 1.999 | 2.106 | 2.298 | 2.311 | 2.237 | 2.219 | 2.437 | 2.311 | 2.237 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.449 | 3.708 | 5.467 | 5.680 | 6.246 | 6.087 | 6.475 | 5.837 | 6.395 | 6.087 | 6.475 | ns |
| | | GCLK PLL | $t_{co}$ | 1.369 | 1.544 | 1.984 | 2.081 | 2.271 | 2.284 | 2.210 | 2.202 | 2.413 | 2.284 | 2.210 | ns |


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**Table 1–84.** EP3SL200 Row Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.474 | 3.748 | 5.512 | 5.727 | 6.306 | 6.146 | 6.491 | 5.870 | 6.440 | 6.146 | 6.491 | ns |
| | | GCLK PLL | $t_{co}$ | 1.406 | 1.596 | 2.041 | 2.128 | 2.334 | 2.343 | 2.279 | 2.248 | 2.447 | 2.343 | 2.279 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.465 | 3.734 | 5.509 | 5.725 | 6.304 | 6.144 | 6.489 | 5.868 | 6.438 | 6.144 | 6.489 | ns |
| | | GCLK PLL | $t_{co}$ | 1.391 | 1.582 | 2.038 | 2.126 | 2.332 | 2.341 | 2.277 | 2.246 | 2.445 | 2.341 | 2.277 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.454 | 3.722 | 5.492 | 5.708 | 6.287 | 6.127 | 6.472 | 5.857 | 6.422 | 6.127 | 6.472 | ns |
| | | GCLK PLL | $t_{co}$ | 1.380 | 1.570 | 2.021 | 2.109 | 2.315 | 2.324 | 2.260 | 2.229 | 2.436 | 2.324 | 2.260 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.443 | 3.699 | 5.476 | 5.692 | 6.272 | 6.112 | 6.457 | 5.845 | 6.407 | 6.112 | 6.457 | ns |
| | | GCLK PLL | $t_{co}$ | 1.363 | 1.547 | 2.005 | 2.093 | 2.300 | 2.309 | 2.245 | 2.214 | 2.424 | 2.309 | 2.245 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.443 | 3.698 | 5.475 | 5.691 | 6.271 | 6.111 | 6.456 | 5.844 | 6.406 | 6.111 | 6.456 | ns |
| | | GCLK PLL | $t_{co}$ | 1.363 | 1.546 | 2.004 | 2.092 | 2.299 | 2.308 | 2.244 | 2.213 | 2.424 | 2.308 | 2.244 | ns |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.451 | 3.707 | 5.473 | 5.687 | 6.265 | 6.105 | 6.450 | 5.840 | 6.399 | 6.105 | 6.450 | ns |
| | | GCLK PLL | $t_{co}$ | 1.371 | 1.555 | 2.002 | 2.088 | 2.293 | 2.302 | 2.238 | 2.208 | 2.418 | 2.302 | 2.238 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.452 | 3.702 | 5.472 | 5.688 | 6.267 | 6.107 | 6.458 | 5.849 | 6.408 | 6.107 | 6.458 | ns |
| | | GCLK PLL | $t_{co}$ | 1.372 | 1.550 | 2.001 | 2.093 | 2.295 | 2.304 | 2.240 | 2.214 | 2.429 | 2.304 | 2.240 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.473 | 3.744 | 5.523 | 5.741 | 6.323 | 6.163 | 6.508 | 5.883 | 6.456 | 6.163 | 6.508 | ns |
| | | GCLK PLL | $t_{co}$ | 1.402 | 1.592 | 2.052 | 2.142 | 2.351 | 2.360 | 2.296 | 2.261 | 2.459 | 2.360 | 2.296 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.459 | 3.722 | 5.505 | 5.724 | 6.306 | 6.146 | 6.491 | 5.869 | 6.440 | 6.146 | 6.491 | ns |
| | | GCLK PLL | $t_{co}$ | 1.379 | 1.570 | 2.034 | 2.125 | 2.334 | 2.343 | 2.279 | 2.245 | 2.450 | 2.343 | 2.279 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.448 | 3.705 | 5.488 | 5.706 | 6.288 | 6.128 | 6.473 | 5.856 | 6.423 | 6.128 | 6.473 | ns |
| | | GCLK PLL | $t_{co}$ | 1.368 | 1.553 | 2.017 | 2.107 | 2.316 | 2.325 | 2.261 | 2.227 | 2.437 | 2.325 | 2.261 | ns |

**Table 1–84.** EP3SL200 Row Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.458 | 3.720 | 5.479 | 5.692 | 6.268 | 6.108 | 6.453 | 5.839 | 6.402 | 6.108 | 6.453 | ns |
| | | GCLK PLL | $t_{co}$ | 1.381 | 1.568 | 2.008 | 2.093 | 2.296 | 2.305 | 2.241 | 2.212 | 2.415 | 2.305 | 2.241 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.451 | 3.708 | 5.470 | 5.684 | 6.260 | 6.100 | 6.445 | 5.838 | 6.395 | 6.100 | 6.445 | ns |
| | | GCLK PLL | $t_{co}$ | 1.371 | 1.556 | 1.999 | 2.085 | 2.288 | 2.297 | 2.233 | 2.204 | 2.415 | 2.297 | 2.233 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.442 | 3.696 | 5.462 | 5.675 | 6.252 | 6.092 | 6.438 | 5.831 | 6.387 | 6.092 | 6.438 | ns |
| | | GCLK PLL | $t_{co}$ | 1.362 | 1.544 | 1.991 | 2.076 | 2.280 | 2.289 | 2.225 | 2.196 | 2.408 | 2.289 | 2.225 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.445 | 3.698 | 5.464 | 5.678 | 6.255 | 6.095 | 6.442 | 5.834 | 6.390 | 6.095 | 6.442 | ns |
| | | GCLK PLL | $t_{co}$ | 1.365 | 1.546 | 1.993 | 2.079 | 2.283 | 2.292 | 2.228 | 2.199 | 2.411 | 2.292 | 2.228 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.441 | 3.693 | 5.462 | 5.677 | 6.255 | 6.095 | 6.445 | 5.837 | 6.395 | 6.095 | 6.445 | ns |
| | | GCLK PLL | $t_{co}$ | 1.361 | 1.541 | 1.991 | 2.081 | 2.283 | 2.292 | 2.228 | 2.202 | 2.416 | 2.292 | 2.228 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.449 | 3.697 | 5.457 | 5.669 | 6.246 | 6.086 | 6.441 | 5.833 | 6.389 | 6.086 | 6.441 | ns |
| | | GCLK PLL | $t_{co}$ | 1.369 | 1.545 | 1.986 | 2.078 | 2.274 | 2.283 | 2.219 | 2.198 | 2.410 | 2.283 | 2.219 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.464 | 3.727 | 5.490 | 5.705 | 6.283 | 6.123 | 6.468 | 5.848 | 6.416 | 6.123 | 6.468 | ns |
| | | GCLK PLL | $t_{co}$ | 1.388 | 1.575 | 2.019 | 2.106 | 2.311 | 2.320 | 2.256 | 2.224 | 2.426 | 2.320 | 2.256 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.458 | 3.717 | 5.486 | 5.701 | 6.279 | 6.119 | 6.464 | 5.850 | 6.413 | 6.119 | 6.464 | ns |
| | | GCLK PLL | $t_{co}$ | 1.378 | 1.565 | 2.015 | 2.102 | 2.307 | 2.316 | 2.252 | 2.221 | 2.429 | 2.316 | 2.252 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.454 | 3.712 | 5.480 | 5.695 | 6.273 | 6.113 | 6.458 | 5.845 | 6.407 | 6.113 | 6.458 | ns |
| | | GCLK PLL | $t_{co}$ | 1.374 | 1.560 | 2.009 | 2.096 | 2.301 | 2.310 | 2.246 | 2.215 | 2.423 | 2.310 | 2.246 | ns |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.466 | 3.726 | 5.501 | 5.719 | 6.301 | 6.141 | 6.486 | 5.864 | 6.433 | 6.141 | 6.486 | ns |
| | | GCLK PLL | $t_{co}$ | 1.387 | 1.574 | 2.030 | 2.120 | 2.329 | 2.338 | 2.274 | 2.238 | 2.445 | 2.338 | 2.274 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.457 | 3.714 | 5.490 | 5.707 | 6.289 | 6.129 | 6.474 | 5.855 | 6.422 | 6.129 | 6.474 | ns |
| | | GCLK PLL | $t_{co}$ | 1.377 | 1.562 | 2.019 | 2.108 | 2.317 | 2.326 | 2.262 | 2.227 | 2.436 | 2.326 | 2.262 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.456 | 3.712 | 5.494 | 5.712 | 6.295 | 6.135 | 6.480 | 5.864 | 6.429 | 6.135 | 6.480 | ns |
| | | GCLK PLL | $t_{co}$ | 1.376 | 1.560 | 2.023 | 2.113 | 2.323 | 2.332 | 2.268 | 2.233 | 2.446 | 2.332 | 2.268 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.569 | 3.829 | 5.537 | 5.731 | 6.305 | 6.146 | 6.519 | 5.903 | 6.453 | 6.146 | 6.519 | ns |
| | | GCLK PLL | $t_{co}$ | 1.489 | 1.665 | 2.054 | 2.132 | 2.315 | 2.328 | 2.267 | 2.268 | 2.474 | 2.328 | 2.267 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.569 | 3.829 | 5.537 | 5.731 | 6.305 | 6.146 | 6.519 | 5.903 | 6.453 | 6.146 | 6.519 | ns |
| | | GCLK PLL | $t_{co}$ | 1.489 | 1.665 | 2.054 | 2.132 | 2.315 | 2.328 | 2.267 | 2.268 | 2.474 | 2.328 | 2.267 | ns |


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Table 1–85 through Table 1–88 list the maximum I/O timing parameters for EP3SL200 devices for differential I/O standards.

Table 1–85 lists the EP3SL200 column pins input timing parameters for differential I/O standards.

**Table 1–85.** EP3SL200 Column Pins Input Timing Parameters (Part 1 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -1.153 | -1.221 | -1.879 | -1.911 | -2.067 | -1.987 | -2.459 | -1.928 | -2.084 | -1.987 | -2.459 | ns |
| | | $t_h$ | 1.289 | 1.376 | 2.114 | 2.150 | 2.330 | 2.237 | 2.711 | 2.177 | 2.355 | 2.237 | 2.711 | ns |
| | GCLK PLL | $t_{su}$ | 1.103 | 1.122 | 1.882 | 1.986 | 2.207 | 2.099 | 2.096 | 1.998 | 2.217 | 2.099 | 2.096 | ns |
| | | $t_h$ | -0.824 | -0.821 | -1.403 | -1.493 | -1.659 | -1.580 | -1.562 | -1.493 | -1.659 | -1.580 | -1.562 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -1.153 | -1.221 | -1.879 | -1.911 | -2.067 | -1.987 | -2.459 | -1.928 | -2.084 | -1.987 | -2.459 | ns |
| | | $t_h$ | 1.289 | 1.376 | 2.114 | 2.150 | 2.330 | 2.237 | 2.711 | 2.177 | 2.355 | 2.237 | 2.711 | ns |
| | GCLK PLL | $t_{su}$ | 1.103 | 1.122 | 1.882 | 1.986 | 2.207 | 2.099 | 2.096 | 1.998 | 2.217 | 2.099 | 2.096 | ns |
| | | $t_h$ | -0.824 | -0.821 | -1.403 | -1.493 | -1.659 | -1.580 | -1.562 | -1.493 | -1.659 | -1.580 | -1.562 | ns |
| RSDS | GCLK | $t_{su}$ | -1.161 | -1.233 | -1.889 | -1.922 | -2.083 | -2.003 | -2.475 | -1.939 | -2.099 | -2.003 | -2.475 | ns |
| | | $t_h$ | 1.297 | 1.388 | 2.124 | 2.161 | 2.346 | 2.253 | 2.727 | 2.188 | 2.370 | 2.253 | 2.727 | ns |
| | GCLK PLL | $t_{su}$ | 1.095 | 1.110 | 1.872 | 1.975 | 2.191 | 2.083 | 2.080 | 1.987 | 2.202 | 2.083 | 2.080 | ns |
| | | $t_h$ | -0.816 | -0.809 | -1.393 | -1.482 | -1.643 | -1.564 | -1.546 | -1.482 | -1.644 | -1.564 | -1.546 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -1.161 | -1.233 | -1.889 | -1.922 | -2.083 | -2.003 | -2.475 | -1.939 | -2.099 | -2.003 | -2.475 | ns |
| | | $t_h$ | 1.297 | 1.388 | 2.124 | 2.161 | 2.346 | 2.253 | 2.727 | 2.188 | 2.370 | 2.253 | 2.727 | ns |
| | GCLK PLL | $t_{su}$ | 1.095 | 1.110 | 1.872 | 1.975 | 2.191 | 2.083 | 2.080 | 1.987 | 2.202 | 2.083 | 2.080 | ns |
| | | $t_h$ | -0.816 | -0.809 | -1.393 | -1.482 | -1.643 | -1.564 | -1.546 | -1.482 | -1.644 | -1.564 | -1.546 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -1.173 | -1.244 | -1.898 | -1.933 | -2.102 | -2.022 | -2.494 | -1.950 | -2.117 | -2.022 | -2.494 | ns |
| | | $t_h$ | 1.309 | 1.399 | 2.133 | 2.172 | 2.365 | 2.272 | 2.746 | 2.199 | 2.388 | 2.272 | 2.746 | ns |
| | GCLK PLL | $t_{su}$ | 1.083 | 1.099 | 1.863 | 1.964 | 2.172 | 2.064 | 2.061 | 1.976 | 2.184 | 2.064 | 2.061 | ns |
| | | $t_h$ | -0.804 | -0.798 | -1.384 | -1.471 | -1.624 | -1.545 | -1.527 | -1.471 | -1.626 | -1.545 | -1.527 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -1.173 | -1.244 | -1.898 | -1.933 | -2.102 | -2.022 | -2.494 | -1.950 | -2.117 | -2.022 | -2.494 | ns |
| | | $t_h$ | 1.309 | 1.399 | 2.133 | 2.172 | 2.365 | 2.272 | 2.746 | 2.199 | 2.388 | 2.272 | 2.746 | ns |
| | GCLK PLL | $t_{su}$ | 1.083 | 1.099 | 1.863 | 1.964 | 2.172 | 2.064 | 2.061 | 1.976 | 2.184 | 2.064 | 2.061 | ns |
| | | $t_h$ | -0.804 | -0.798 | -1.384 | -1.471 | -1.624 | -1.545 | -1.527 | -1.471 | -1.626 | -1.545 | -1.527 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -1.161 | -1.233 | -1.889 | -1.922 | -2.083 | -2.003 | -2.475 | -1.939 | -2.099 | -2.003 | -2.475 | ns |
| | | $t_h$ | 1.297 | 1.388 | 2.124 | 2.161 | 2.346 | 2.253 | 2.727 | 2.188 | 2.370 | 2.253 | 2.727 | ns |
| | GCLK PLL | $t_{su}$ | 1.095 | 1.110 | 1.872 | 1.975 | 2.191 | 2.083 | 2.080 | 1.987 | 2.202 | 2.083 | 2.080 | ns |
| | | $t_h$ | -0.816 | -0.809 | -1.393 | -1.482 | -1.643 | -1.564 | -1.546 | -1.482 | -1.644 | -1.564 | -1.546 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -1.161 | -1.233 | -1.889 | -1.922 | -2.083 | -2.003 | -2.475 | -1.939 | -2.099 | -2.003 | -2.475 | ns |
| | | $t_h$ | 1.297 | 1.388 | 2.124 | 2.161 | 2.346 | 2.253 | 2.727 | 2.188 | 2.370 | 2.253 | 2.727 | ns |
| | GCLK PLL | $t_{su}$ | 1.095 | 1.110 | 1.872 | 1.975 | 2.191 | 2.083 | 2.080 | 1.987 | 2.202 | 2.083 | 2.080 | ns |
| | | $t_h$ | -0.816 | -0.809 | -1.393 | -1.482 | -1.643 | -1.564 | -1.546 | -1.482 | -1.644 | -1.564 | -1.546 | ns |

**Table 1–85.** EP3SL200 Column Pins Input Timing Parameters (Part 2 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -1.173 | -1.244 | -1.898 | -1.933 | -2.102 | -2.022 | -2.494 | -1.950 | -2.117 | -2.022 | -2.494 | ns |
| | | $t_h$ | 1.309 | 1.399 | 2.133 | 2.172 | 2.365 | 2.272 | 2.746 | 2.199 | 2.388 | 2.272 | 2.746 | ns |
| | GCLK PLL | $t_{su}$ | 1.083 | 1.099 | 1.863 | 1.964 | 2.172 | 2.064 | 2.061 | 1.976 | 2.184 | 2.064 | 2.061 | ns |
| | | $t_h$ | -0.804 | -0.798 | -1.384 | -1.471 | -1.624 | -1.545 | -1.527 | -1.471 | -1.626 | -1.545 | -1.527 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -1.173 | -1.244 | -1.898 | -1.933 | -2.102 | -2.022 | -2.494 | -1.950 | -2.117 | -2.022 | -2.494 | ns |
| | | $t_h$ | 1.309 | 1.399 | 2.133 | 2.172 | 2.365 | 2.272 | 2.746 | 2.199 | 2.388 | 2.272 | 2.746 | ns |
| | GCLK PLL | $t_{su}$ | 1.083 | 1.099 | 1.863 | 1.964 | 2.172 | 2.064 | 2.061 | 1.976 | 2.184 | 2.064 | 2.061 | ns |
| | | $t_h$ | -0.804 | -0.798 | -1.384 | -1.471 | -1.624 | -1.545 | -1.527 | -1.471 | -1.626 | -1.545 | -1.527 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -1.180 | -1.250 | -1.910 | -1.938 | -2.102 | -2.024 | -2.493 | -1.954 | -2.112 | -2.024 | -2.493 | ns |
| | | $t_h$ | 1.316 | 1.405 | 2.146 | 2.180 | 2.368 | 2.275 | 2.750 | 2.206 | 2.388 | 2.275 | 2.750 | ns |
| | GCLK PLL | $t_{su}$ | 1.076 | 1.093 | 1.851 | 1.959 | 2.172 | 2.062 | 2.062 | 1.972 | 2.189 | 2.062 | 2.062 | ns |
| | | $t_h$ | -0.797 | -0.792 | -1.371 | -1.463 | -1.621 | -1.542 | -1.523 | -1.464 | -1.626 | -1.542 | -1.523 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -1.180 | -1.250 | -1.910 | -1.938 | -2.102 | -2.024 | -2.493 | -1.954 | -2.112 | -2.024 | -2.493 | ns |
| | | $t_h$ | 1.316 | 1.405 | 2.146 | 2.180 | 2.368 | 2.275 | 2.750 | 2.206 | 2.388 | 2.275 | 2.750 | ns |
| | GCLK PLL | $t_{su}$ | 1.076 | 1.093 | 1.851 | 1.959 | 2.172 | 2.062 | 2.062 | 1.972 | 2.189 | 2.062 | 2.062 | ns |
| | | $t_h$ | -0.797 | -0.792 | -1.371 | -1.463 | -1.621 | -1.542 | -1.523 | -1.464 | -1.626 | -1.542 | -1.523 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -1.153 | -1.221 | -1.879 | -1.911 | -2.067 | -1.987 | -2.459 | -1.928 | -2.084 | -1.987 | -2.459 | ns |
| | | $t_h$ | 1.289 | 1.376 | 2.114 | 2.150 | 2.330 | 2.237 | 2.711 | 2.177 | 2.355 | 2.237 | 2.711 | ns |
| | GCLK PLL | $t_{su}$ | 1.103 | 1.122 | 1.882 | 1.986 | 2.207 | 2.099 | 2.096 | 1.998 | 2.217 | 2.099 | 2.096 | ns |
| | | $t_h$ | -0.824 | -0.821 | -1.403 | -1.493 | -1.659 | -1.580 | -1.562 | -1.493 | -1.659 | -1.580 | -1.562 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -1.153 | -1.221 | -1.879 | -1.911 | -2.067 | -1.987 | -2.459 | -1.928 | -2.084 | -1.987 | -2.459 | ns |
| | | $t_h$ | 1.289 | 1.376 | 2.114 | 2.150 | 2.330 | 2.237 | 2.711 | 2.177 | 2.355 | 2.237 | 2.711 | ns |
| | GCLK PLL | $t_{su}$ | 1.103 | 1.122 | 1.882 | 1.986 | 2.207 | 2.099 | 2.096 | 1.998 | 2.217 | 2.099 | 2.096 | ns |
| | | $t_h$ | -0.824 | -0.821 | -1.403 | -1.493 | -1.659 | -1.580 | -1.562 | -1.493 | -1.659 | -1.580 | -1.562 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -1.161 | -1.233 | -1.889 | -1.922 | -2.083 | -2.003 | -2.475 | -1.939 | -2.099 | -2.003 | -2.475 | ns |
| | | $t_h$ | 1.297 | 1.388 | 2.124 | 2.161 | 2.346 | 2.253 | 2.727 | 2.188 | 2.370 | 2.253 | 2.727 | ns |
| | GCLK PLL | $t_{su}$ | 1.095 | 1.110 | 1.872 | 1.975 | 2.191 | 2.083 | 2.080 | 1.987 | 2.202 | 2.083 | 2.080 | ns |
| | | $t_h$ | -0.816 | -0.809 | -1.393 | -1.482 | -1.643 | -1.564 | -1.546 | -1.482 | -1.644 | -1.564 | -1.546 | ns |

Table 1–86 lists the EP3SL200 row pins input timing parameters for differential I/O standards.

**Table 1–86.** EP3SL200 Row Pins Input Timing Parameters (Part 1 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -1.332 | -1.401 | -1.719 | -1.648 | -1.841 | -1.769 | -2.221 | -1.630 | -1.815 | -1.769 | -2.221 | ns |
| | | $t_h$ | 1.476 | 1.563 | 1.994 | 1.939 | 2.157 | 2.071 | 2.526 | 1.934 | 2.145 | 2.071 | 2.526 | ns |
| | GCLK PLL | $t_{su}$ | 0.869 | 0.886 | 1.991 | 2.205 | 2.405 | 2.282 | 2.297 | 2.252 | 2.458 | 2.282 | 2.297 | ns |
| | | $t_h$ | -0.581 | -0.578 | -1.475 | -1.662 | -1.803 | -1.711 | -1.711 | -1.692 | -1.839 | -1.711 | -1.711 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -1.332 | -1.401 | -1.719 | -1.648 | -1.841 | -1.769 | -2.221 | -1.630 | -1.815 | -1.769 | -2.221 | ns |
| | | $t_h$ | 1.476 | 1.563 | 1.994 | 1.939 | 2.157 | 2.071 | 2.526 | 1.934 | 2.145 | 2.071 | 2.526 | ns |
| | GCLK PLL | $t_{su}$ | 0.869 | 0.886 | 1.991 | 2.205 | 2.405 | 2.282 | 2.297 | 2.252 | 2.458 | 2.282 | 2.297 | ns |
| | | $t_h$ | -0.581 | -0.578 | -1.475 | -1.662 | -1.803 | -1.711 | -1.711 | -1.692 | -1.839 | -1.711 | -1.711 | ns |
| RSDS | GCLK | $t_{su}$ | -1.332 | -1.401 | -1.719 | -1.648 | -1.841 | -1.769 | -2.221 | -1.630 | -1.815 | -1.769 | -2.221 | ns |
| | | $t_h$ | 1.476 | 1.563 | 1.994 | 1.939 | 2.157 | 2.071 | 2.526 | 1.934 | 2.145 | 2.071 | 2.526 | ns |
| | GCLK PLL | $t_{su}$ | 0.869 | 0.886 | 1.991 | 2.205 | 2.405 | 2.282 | 2.297 | 2.252 | 2.458 | 2.282 | 2.297 | ns |
| | | $t_h$ | -0.581 | -0.578 | -1.475 | -1.662 | -1.803 | -1.711 | -1.711 | -1.692 | -1.839 | -1.711 | -1.711 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -1.137 | -1.216 | -1.849 | -1.877 | -2.030 | -1.953 | -2.400 | -1.901 | -2.052 | -1.953 | -2.400 | ns |
| | | $t_h$ | 1.274 | 1.369 | 2.088 | 2.122 | 2.297 | 2.206 | 2.656 | 2.156 | 2.330 | 2.206 | 2.656 | ns |
| | GCLK PLL | $t_{su}$ | 1.064 | 1.071 | 1.866 | 1.981 | 2.216 | 2.098 | 2.118 | 1.985 | 2.221 | 2.098 | 2.118 | ns |
| | | $t_h$ | -0.783 | -0.772 | -1.384 | -1.483 | -1.663 | -1.576 | -1.581 | -1.474 | -1.654 | -1.576 | -1.581 | ns |
| | GCLK | $t_{su}$ | -1.137 | -1.216 | -1.849 | -1.877 | -2.030 | -1.953 | -2.400 | -1.901 | -2.052 | -1.953 | -2.400 | ns |
| | | $t_h$ | 1.274 | 1.369 | 2.088 | 2.122 | 2.297 | 2.206 | 2.656 | 2.156 | 2.330 | 2.206 | 2.656 | ns |
| | GCLK PLL | $t_{su}$ | 1.064 | 1.071 | 1.866 | 1.981 | 2.216 | 2.098 | 2.118 | 1.985 | 2.221 | 2.098 | 2.118 | ns |
| | | $t_h$ | -0.783 | -0.772 | -1.384 | -1.483 | -1.663 | -1.576 | -1.581 | -1.474 | -1.654 | -1.576 | -1.581 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -1.146 | -1.228 | -1.858 | -1.887 | -2.046 | -1.969 | -2.416 | -1.910 | -2.068 | -1.969 | -2.416 | ns |
| | | $t_h$ | 1.283 | 1.381 | 2.097 | 2.132 | 2.313 | 2.222 | 2.672 | 2.165 | 2.346 | 2.222 | 2.672 | ns |
| | GCLK PLL | $t_{su}$ | 1.055 | 1.059 | 1.857 | 1.971 | 2.200 | 2.082 | 2.102 | 1.976 | 2.205 | 2.082 | 2.102 | ns |
| | | $t_h$ | -0.774 | -0.760 | -1.375 | -1.473 | -1.647 | -1.560 | -1.565 | -1.465 | -1.638 | -1.560 | -1.565 | ns |
| | GCLK | $t_{su}$ | -1.146 | -1.228 | -1.858 | -1.887 | -2.046 | -1.969 | -2.416 | -1.910 | -2.068 | -1.969 | -2.416 | ns |
| | | $t_h$ | 1.283 | 1.381 | 2.097 | 2.132 | 2.313 | 2.222 | 2.672 | 2.165 | 2.346 | 2.222 | 2.672 | ns |
| | GCLK PLL | $t_{su}$ | 1.055 | 1.059 | 1.857 | 1.971 | 2.200 | 2.082 | 2.102 | 1.976 | 2.205 | 2.082 | 2.102 | ns |
| | | $t_h$ | -0.774 | -0.760 | -1.375 | -1.473 | -1.647 | -1.560 | -1.565 | -1.465 | -1.638 | -1.560 | -1.565 | ns |

**Table 1–86.** EP3SL200 Row Pins Input Timing Parameters (Part 2 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -1.160 | -1.240 | -1.867 | -1.897 | -2.064 | -1.987 | -2.434 | -1.921 | -2.085 | -1.987 | -2.434 | ns |
| | | $t_h$ | 1.297 | 1.393 | 2.106 | 2.142 | 2.331 | 2.240 | 2.690 | 2.176 | 2.363 | 2.240 | 2.690 | ns |
| | GCLK PLL | $t_{su}$ | 1.041 | 1.047 | 1.844 | 1.961 | 2.182 | 2.064 | 2.084 | 1.965 | 2.188 | 2.064 | 2.084 | ns |
| | | $t_h$ | -0.760 | -0.748 | -1.363 | -1.463 | -1.629 | -1.542 | -1.547 | -1.454 | -1.621 | -1.542 | -1.547 | ns |
| | GCLK | $t_{su}$ | -1.160 | -1.240 | -1.867 | -1.897 | -2.064 | -1.987 | -2.434 | -1.921 | -2.085 | -1.987 | -2.434 | ns |
| | | $t_h$ | 1.297 | 1.393 | 2.106 | 2.142 | 2.331 | 2.240 | 2.690 | 2.176 | 2.363 | 2.240 | 2.690 | ns |
| | GCLK PLL | $t_{su}$ | 1.041 | 1.047 | 1.844 | 1.961 | 2.182 | 2.064 | 2.084 | 1.965 | 2.188 | 2.064 | 2.084 | ns |
| | | $t_h$ | -0.760 | -0.748 | -1.363 | -1.463 | -1.629 | -1.542 | -1.547 | -1.454 | -1.621 | -1.542 | -1.547 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -1.146 | -1.228 | -1.858 | -1.887 | -2.046 | -1.969 | -2.416 | -1.910 | -2.068 | -1.969 | -2.416 | ns |
| | | $t_h$ | 1.283 | 1.381 | 2.097 | 2.132 | 2.313 | 2.222 | 2.672 | 2.165 | 2.346 | 2.222 | 2.672 | ns |
| | GCLK PLL | $t_{su}$ | 1.055 | 1.059 | 1.857 | 1.971 | 2.200 | 2.082 | 2.102 | 1.976 | 2.205 | 2.082 | 2.102 | ns |
| | | $t_h$ | -0.774 | -0.760 | -1.375 | -1.473 | -1.647 | -1.560 | -1.565 | -1.465 | -1.638 | -1.560 | -1.565 | ns |
| | GCLK | $t_{su}$ | -1.146 | -1.228 | -1.858 | -1.887 | -2.046 | -1.969 | -2.416 | -1.910 | -2.068 | -1.969 | -2.416 | ns |
| | | $t_h$ | 1.283 | 1.381 | 2.097 | 2.132 | 2.313 | 2.222 | 2.672 | 2.165 | 2.346 | 2.222 | 2.672 | ns |
| | GCLK PLL | $t_{su}$ | 1.055 | 1.059 | 1.857 | 1.971 | 2.200 | 2.082 | 2.102 | 1.976 | 2.205 | 2.082 | 2.102 | ns |
| | | $t_h$ | -0.774 | -0.760 | -1.375 | -1.473 | -1.647 | -1.560 | -1.565 | -1.465 | -1.638 | -1.560 | -1.565 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -1.160 | -1.240 | -1.867 | -1.897 | -2.064 | -1.987 | -2.434 | -1.921 | -2.085 | -1.987 | -2.434 | ns |
| | | $t_h$ | 1.297 | 1.393 | 2.106 | 2.142 | 2.331 | 2.240 | 2.690 | 2.176 | 2.363 | 2.240 | 2.690 | ns |
| | GCLK PLL | $t_{su}$ | 1.041 | 1.047 | 1.844 | 1.961 | 2.182 | 2.064 | 2.084 | 1.965 | 2.188 | 2.064 | 2.084 | ns |
| | | $t_h$ | -0.760 | -0.748 | -1.363 | -1.463 | -1.629 | -1.542 | -1.547 | -1.454 | -1.621 | -1.542 | -1.547 | ns |
| | GCLK | $t_{su}$ | -1.160 | -1.240 | -1.867 | -1.897 | -2.064 | -1.987 | -2.434 | -1.921 | -2.085 | -1.987 | -2.434 | ns |
| | | $t_h$ | 1.297 | 1.393 | 2.106 | 2.142 | 2.331 | 2.240 | 2.690 | 2.176 | 2.363 | 2.240 | 2.690 | ns |
| | GCLK PLL | $t_{su}$ | 1.041 | 1.047 | 1.844 | 1.961 | 2.182 | 2.064 | 2.084 | 1.965 | 2.188 | 2.064 | 2.084 | ns |
| | | $t_h$ | -0.760 | -0.748 | -1.363 | -1.463 | -1.629 | -1.542 | -1.547 | -1.454 | -1.621 | -1.542 | -1.547 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -1.169 | -1.249 | -1.881 | -1.908 | -2.071 | -1.995 | -2.440 | -1.928 | -2.086 | -1.995 | -2.440 | ns |
| | | $t_h$ | 1.306 | 1.402 | 2.121 | 2.156 | 2.341 | 2.250 | 2.701 | 2.186 | 2.369 | 2.250 | 2.701 | ns |
| | GCLK PLL | $t_{su}$ | 1.032 | 1.038 | 1.829 | 1.945 | 2.171 | 2.052 | 2.073 | 1.954 | 2.182 | 2.052 | 2.073 | ns |
| | | $t_h$ | -0.751 | -0.739 | -1.348 | -1.445 | -1.615 | -1.528 | -1.532 | -1.440 | -1.612 | -1.528 | -1.532 | ns |
| | GCLK | $t_{su}$ | -1.169 | -1.249 | -1.881 | -1.908 | -2.071 | -1.995 | -2.440 | -1.928 | -2.086 | -1.995 | -2.440 | ns |
| | | $t_h$ | 1.306 | 1.402 | 2.121 | 2.156 | 2.341 | 2.250 | 2.701 | 2.186 | 2.369 | 2.250 | 2.701 | ns |
| | GCLK PLL | $t_{su}$ | 1.032 | 1.038 | 1.829 | 1.945 | 2.171 | 2.052 | 2.073 | 1.954 | 2.182 | 2.052 | 2.073 | ns |
| | | $t_h$ | -0.751 | -0.739 | -1.348 | -1.445 | -1.615 | -1.528 | -1.532 | -1.440 | -1.612 | -1.528 | -1.532 | ns |

Table 1–87 lists the EP3SL200 column pins output timing parameters for differential I/O standards.

**Table 1–87.** EP3SL200 Column Pins output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.479 | 3.750 | 5.506 | 5.712 | 6.270 | 6.106 | 6.513 | 5.854 | 6.411 | 6.106 | 6.513 | ns |
| | | GCLK PLL | $t_{co}$ | 3.475 | 3.753 | 5.553 | 5.767 | 6.332 | 6.168 | 6.575 | 5.913 | 6.477 | 6.168 | 6.575 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.479 | 3.750 | 5.506 | 5.712 | 6.270 | 6.106 | 6.513 | 5.854 | 6.411 | 6.106 | 6.513 | ns |
| | | GCLK PLL | $t_{co}$ | 3.475 | 3.753 | 5.553 | 5.767 | 6.332 | 6.168 | 6.575 | 5.913 | 6.477 | 6.168 | 6.575 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.479 | 3.750 | 5.506 | 5.712 | 6.270 | 6.106 | 6.513 | 5.854 | 6.411 | 6.106 | 6.513 | ns |
| | | GCLK PLL | $t_{co}$ | 3.475 | 3.753 | 5.553 | 5.767 | 6.332 | 6.168 | 6.575 | 5.913 | 6.477 | 6.168 | 6.575 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.506 | 3.783 | 5.577 | 5.790 | 6.354 | 6.190 | 6.597 | 5.934 | 6.497 | 6.190 | 6.597 | ns |
| | | GCLK PLL | $t_{co}$ | 3.496 | 3.773 | 5.567 | 5.779 | 6.344 | 6.180 | 6.587 | 5.923 | 6.487 | 6.180 | 6.587 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.496 | 3.773 | 5.570 | 5.783 | 6.348 | 6.184 | 6.591 | 5.928 | 6.492 | 6.184 | 6.591 | ns |
| | | GCLK PLL | $t_{co}$ | 3.489 | 3.767 | 5.563 | 5.777 | 6.342 | 6.178 | 6.585 | 5.921 | 6.486 | 6.178 | 6.585 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.488 | 3.765 | 5.560 | 5.774 | 6.339 | 6.175 | 6.582 | 5.918 | 6.482 | 6.175 | 6.582 | ns |
| | | GCLK PLL | $t_{co}$ | 3.510 | 3.787 | 5.581 | 5.794 | 6.358 | 6.194 | 6.601 | 5.938 | 6.502 | 6.194 | 6.601 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.500 | 3.776 | 5.560 | 5.771 | 6.333 | 6.169 | 6.576 | 5.914 | 6.475 | 6.169 | 6.576 | ns |
| | | GCLK PLL | $t_{co}$ | 3.495 | 3.772 | 5.560 | 5.771 | 6.334 | 6.170 | 6.577 | 5.915 | 6.477 | 6.170 | 6.577 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.493 | 3.770 | 5.559 | 5.770 | 6.332 | 6.168 | 6.575 | 5.914 | 6.476 | 6.168 | 6.575 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.761 | 5.549 | 5.760 | 6.323 | 6.159 | 6.566 | 5.904 | 6.466 | 6.159 | 6.566 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.486 | 3.763 | 5.555 | 5.767 | 6.331 | 6.167 | 6.574 | 5.912 | 6.475 | 6.167 | 6.574 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.760 | 5.538 | 5.748 | 6.309 | 6.145 | 6.552 | 5.891 | 6.451 | 6.145 | 6.552 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.497 | 3.773 | 5.556 | 5.766 | 6.327 | 6.163 | 6.570 | 5.910 | 6.470 | 6.163 | 6.570 | ns |
| | | GCLK PLL | $t_{co}$ | 3.493 | 3.770 | 5.557 | 5.768 | 6.331 | 6.167 | 6.574 | 5.912 | 6.474 | 6.167 | 6.574 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.483 | 3.759 | 5.546 | 5.757 | 6.319 | 6.155 | 6.562 | 5.901 | 6.462 | 6.155 | 6.562 | ns |
| | | GCLK PLL | $t_{co}$ | 3.481 | 3.757 | 5.544 | 5.754 | 6.317 | 6.153 | 6.560 | 5.899 | 6.460 | 6.153 | 6.560 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.481 | 3.758 | 5.547 | 5.759 | 6.322 | 6.158 | 6.565 | 5.903 | 6.466 | 6.158 | 6.565 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.761 | 5.544 | 5.754 | 6.316 | 6.152 | 6.559 | 5.898 | 6.459 | 6.152 | 6.559 | ns |

**Table 1–87.** EP3SL200 Column Pins output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.511 | 3.790 | 5.589 | 5.802 | 6.366 | 6.202 | 6.609 | 5.946 | 6.509 | 6.202 | 6.609 | ns |
| | | GCLK PLL | $t_{co}$ | 3.497 | 3.776 | 5.577 | 5.791 | 6.356 | 6.192 | 6.599 | 5.936 | 6.500 | 6.192 | 6.599 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.485 | 3.763 | 5.560 | 5.773 | 6.338 | 6.174 | 6.581 | 5.918 | 6.482 | 6.174 | 6.581 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.763 | 5.563 | 5.777 | 6.342 | 6.178 | 6.585 | 5.922 | 6.487 | 6.178 | 6.585 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.481 | 3.759 | 5.556 | 5.769 | 6.335 | 6.171 | 6.578 | 5.915 | 6.479 | 6.171 | 6.578 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.761 | 5.549 | 5.760 | 6.323 | 6.159 | 6.566 | 5.904 | 6.466 | 6.159 | 6.566 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.486 | 3.763 | 5.557 | 5.770 | 6.334 | 6.170 | 6.577 | 5.914 | 6.478 | 6.170 | 6.577 | ns |
| | | GCLK PLL | $t_{co}$ | 3.514 | 3.793 | 5.588 | 5.800 | 6.364 | 6.200 | 6.607 | 5.945 | 6.507 | 6.200 | 6.607 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.503 | 3.781 | 5.576 | 5.788 | 6.352 | 6.188 | 6.595 | 5.933 | 6.495 | 6.188 | 6.595 | ns |
| | | GCLK PLL | $t_{co}$ | 3.498 | 3.777 | 5.576 | 5.789 | 6.353 | 6.189 | 6.596 | 5.934 | 6.497 | 6.189 | 6.596 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.484 | 3.762 | 5.558 | 5.770 | 6.334 | 6.170 | 6.577 | 5.915 | 6.479 | 6.170 | 6.577 | ns |
| | | GCLK PLL | $t_{co}$ | 3.482 | 3.760 | 5.556 | 5.768 | 6.332 | 6.168 | 6.575 | 5.913 | 6.476 | 6.168 | 6.575 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.486 | 3.762 | 5.548 | 5.758 | 6.320 | 6.156 | 6.563 | 5.902 | 6.463 | 6.156 | 6.563 | ns |
| | | GCLK PLL | $t_{co}$ | 3.486 | 3.763 | 5.556 | 5.768 | 6.332 | 6.168 | 6.575 | 5.913 | 6.476 | 6.168 | 6.575 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.502 | 3.780 | 5.572 | 5.783 | 6.346 | 6.182 | 6.589 | 5.928 | 6.489 | 6.182 | 6.589 | ns |
| | | GCLK PLL | $t_{co}$ | 3.502 | 3.780 | 5.572 | 5.783 | 6.346 | 6.182 | 6.589 | 5.928 | 6.489 | 6.182 | 6.589 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.492 | 3.770 | 5.562 | 5.773 | 6.336 | 6.172 | 6.579 | 5.918 | 6.480 | 6.172 | 6.579 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.762 | 5.548 | 5.758 | 6.320 | 6.156 | 6.563 | 5.902 | 6.463 | 6.156 | 6.563 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.479 | 3.750 | 5.506 | 5.712 | 6.270 | 6.106 | 6.513 | 5.854 | 6.411 | 6.106 | 6.513 | ns |
| | | GCLK PLL | $t_{co}$ | 3.475 | 3.753 | 5.553 | 5.767 | 6.332 | 6.168 | 6.575 | 5.913 | 6.477 | 6.168 | 6.575 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.479 | 3.750 | 5.506 | 5.712 | 6.270 | 6.106 | 6.513 | 5.854 | 6.411 | 6.106 | 6.513 | ns |
| | | GCLK PLL | $t_{co}$ | 3.475 | 3.753 | 5.553 | 5.767 | 6.332 | 6.168 | 6.575 | 5.913 | 6.477 | 6.168 | 6.575 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.479 | 3.750 | 5.506 | 5.712 | 6.270 | 6.106 | 6.513 | 5.854 | 6.411 | 6.106 | 6.513 | ns |
| | | GCLK PLL | $t_{co}$ | 3.475 | 3.753 | 5.553 | 5.767 | 6.332 | 6.168 | 6.575 | 5.913 | 6.477 | 6.168 | 6.575 | ns |


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**Table 1–87.** EP3SL200 Column Pins output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.506 | 3.783 | 5.577 | 5.790 | 6.354 | 6.190 | 6.597 | 5.934 | 6.497 | 6.190 | 6.597 | ns |
| | | GCLK PLL | $t_{co}$ | 3.496 | 3.773 | 5.567 | 5.779 | 6.344 | 6.180 | 6.587 | 5.923 | 6.487 | 6.180 | 6.587 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.496 | 3.773 | 5.570 | 5.783 | 6.348 | 6.184 | 6.591 | 5.928 | 6.492 | 6.184 | 6.591 | ns |
| | | GCLK PLL | $t_{co}$ | 3.489 | 3.767 | 5.563 | 5.777 | 6.342 | 6.178 | 6.585 | 5.921 | 6.486 | 6.178 | 6.585 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.488 | 3.765 | 5.560 | 5.774 | 6.339 | 6.175 | 6.582 | 5.918 | 6.482 | 6.175 | 6.582 | ns |
| | | GCLK PLL | $t_{co}$ | 3.510 | 3.787 | 5.581 | 5.794 | 6.358 | 6.194 | 6.601 | 5.938 | 6.502 | 6.194 | 6.601 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.500 | 3.776 | 5.560 | 5.771 | 6.333 | 6.169 | 6.576 | 5.914 | 6.475 | 6.169 | 6.576 | ns |
| | | GCLK PLL | $t_{co}$ | 3.495 | 3.772 | 5.560 | 5.771 | 6.334 | 6.170 | 6.577 | 5.915 | 6.477 | 6.170 | 6.577 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.493 | 3.770 | 5.559 | 5.770 | 6.332 | 6.168 | 6.575 | 5.914 | 6.476 | 6.168 | 6.575 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.761 | 5.549 | 5.760 | 6.323 | 6.159 | 6.566 | 5.904 | 6.466 | 6.159 | 6.566 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.486 | 3.763 | 5.555 | 5.767 | 6.331 | 6.167 | 6.574 | 5.912 | 6.475 | 6.167 | 6.574 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.760 | 5.538 | 5.748 | 6.309 | 6.145 | 6.552 | 5.891 | 6.451 | 6.145 | 6.552 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.497 | 3.773 | 5.556 | 5.766 | 6.327 | 6.163 | 6.570 | 5.910 | 6.470 | 6.163 | 6.570 | ns |
| | | GCLK PLL | $t_{co}$ | 3.493 | 3.770 | 5.557 | 5.768 | 6.331 | 6.167 | 6.574 | 5.912 | 6.474 | 6.167 | 6.574 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.483 | 3.759 | 5.546 | 5.757 | 6.319 | 6.155 | 6.562 | 5.901 | 6.462 | 6.155 | 6.562 | ns |
| | | GCLK PLL | $t_{co}$ | 3.481 | 3.757 | 5.544 | 5.754 | 6.317 | 6.153 | 6.560 | 5.899 | 6.460 | 6.153 | 6.560 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.481 | 3.758 | 5.547 | 5.759 | 6.322 | 6.158 | 6.565 | 5.903 | 6.466 | 6.158 | 6.565 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.761 | 5.544 | 5.754 | 6.316 | 6.152 | 6.559 | 5.898 | 6.459 | 6.152 | 6.559 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.511 | 3.790 | 5.589 | 5.802 | 6.366 | 6.202 | 6.609 | 5.946 | 6.509 | 6.202 | 6.609 | ns |
| | | GCLK PLL | $t_{co}$ | 3.497 | 3.776 | 5.577 | 5.791 | 6.356 | 6.192 | 6.599 | 5.936 | 6.500 | 6.192 | 6.599 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.485 | 3.763 | 5.560 | 5.773 | 6.338 | 6.174 | 6.581 | 5.918 | 6.482 | 6.174 | 6.581 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.763 | 5.563 | 5.777 | 6.342 | 6.178 | 6.585 | 5.922 | 6.487 | 6.178 | 6.585 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.481 | 3.759 | 5.556 | 5.769 | 6.335 | 6.171 | 6.578 | 5.915 | 6.479 | 6.171 | 6.578 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.761 | 5.549 | 5.760 | 6.323 | 6.159 | 6.566 | 5.904 | 6.466 | 6.159 | 6.566 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.486 | 3.763 | 5.557 | 5.770 | 6.334 | 6.170 | 6.577 | 5.914 | 6.478 | 6.170 | 6.577 | ns |
| | | GCLK PLL | $t_{co}$ | 3.514 | 3.793 | 5.588 | 5.800 | 6.364 | 6.200 | 6.607 | 5.945 | 6.507 | 6.200 | 6.607 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.503 | 3.781 | 5.576 | 5.788 | 6.352 | 6.188 | 6.595 | 5.933 | 6.495 | 6.188 | 6.595 | ns |
| | | GCLK PLL | $t_{co}$ | 3.498 | 3.777 | 5.576 | 5.789 | 6.353 | 6.189 | 6.596 | 5.934 | 6.497 | 6.189 | 6.596 | ns |

**Table 1–87.** EP3SL200 Column Pins output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.484 | 3.762 | 5.558 | 5.770 | 6.334 | 6.170 | 6.577 | 5.915 | 6.479 | 6.170 | 6.577 | ns |
| | | GCLK PLL | $t_{co}$ | 3.482 | 3.760 | 5.556 | 5.768 | 6.332 | 6.168 | 6.575 | 5.913 | 6.476 | 6.168 | 6.575 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.486 | 3.762 | 5.548 | 5.758 | 6.320 | 6.156 | 6.563 | 5.902 | 6.463 | 6.156 | 6.563 | ns |
| | | GCLK PLL | $t_{co}$ | 3.486 | 3.763 | 5.556 | 5.768 | 6.332 | 6.168 | 6.575 | 5.913 | 6.476 | 6.168 | 6.575 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.502 | 3.780 | 5.572 | 5.783 | 6.346 | 6.182 | 6.589 | 5.928 | 6.489 | 6.182 | 6.589 | ns |
| | | GCLK PLL | $t_{co}$ | 3.502 | 3.780 | 5.572 | 5.783 | 6.346 | 6.182 | 6.589 | 5.928 | 6.489 | 6.182 | 6.589 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.492 | 3.770 | 5.562 | 5.773 | 6.336 | 6.172 | 6.579 | 5.918 | 6.480 | 6.172 | 6.579 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.762 | 5.548 | 5.758 | 6.320 | 6.156 | 6.563 | 5.902 | 6.463 | 6.156 | 6.563 | ns |

Table 1–88 lists the EP3SL200 row pins output timing parameters for differential I/O standards.

**Table 1–88.** EP3SL200 Row Pins Output Timing Parameters (Part 1 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | — | GCLK | $t_{co}$ | 3.152 | 3.376 | 4.936 | 5.115 | 5.637 | 5.478 | 5.865 | 5.239 | 5.762 | 5.478 | 5.865 | ns |
| | | GCLK PLL | $t_{co}$ | 3.536 | 3.812 | 5.604 | 5.814 | 6.381 | 6.214 | 6.593 | 5.962 | 6.531 | 6.214 | 6.593 | ns |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.518 | 3.802 | 5.642 | 5.860 | 6.435 | 6.268 | 6.647 | 6.013 | 6.592 | 6.268 | 6.647 | ns |
| | | GCLK PLL | $t_{co}$ | 3.152 | 3.376 | 4.936 | 5.115 | 5.637 | 5.478 | 5.865 | 5.239 | 5.762 | 5.478 | 5.865 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.536 | 3.812 | 5.604 | 5.814 | 6.381 | 6.214 | 6.593 | 5.962 | 6.531 | 6.214 | 6.593 | ns |
| | | GCLK PLL | $t_{co}$ | 3.518 | 3.802 | 5.642 | 5.860 | 6.435 | 6.268 | 6.647 | 6.013 | 6.592 | 6.268 | 6.647 | ns |
| MINI-LVDS | — | GCLK | $t_{co}$ | 3.152 | 3.376 | 4.936 | 5.115 | 5.637 | 5.478 | 5.865 | 5.239 | 5.762 | 5.478 | 5.865 | ns |
| | | GCLK PLL | $t_{co}$ | 3.536 | 3.812 | 5.604 | 5.814 | 6.381 | 6.214 | 6.593 | 5.962 | 6.531 | 6.214 | 6.593 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.518 | 3.802 | 5.642 | 5.860 | 6.435 | 6.268 | 6.647 | 6.013 | 6.592 | 6.268 | 6.647 | ns |
| | | GCLK PLL | $t_{co}$ | 3.562 | 3.845 | 5.678 | 5.894 | 6.468 | 6.301 | 6.680 | 6.046 | 6.621 | 6.301 | 6.680 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.548 | 3.831 | 5.665 | 5.881 | 6.455 | 6.288 | 6.667 | 6.032 | 6.608 | 6.288 | 6.667 | ns |
| | | GCLK PLL | $t_{co}$ | 3.544 | 3.827 | 5.663 | 5.881 | 6.456 | 6.289 | 6.668 | 6.032 | 6.610 | 6.289 | 6.668 | ns |
| RSDS | — | GCLK | $t_{co}$ | 3.560 | 3.842 | 5.664 | 5.878 | 6.450 | 6.283 | 6.662 | 6.029 | 6.603 | 6.283 | 6.662 | ns |
| | | GCLK PLL | $t_{co}$ | 3.549 | 3.832 | 5.660 | 5.874 | 6.447 | 6.280 | 6.659 | 6.026 | 6.600 | 6.280 | 6.659 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.546 | 3.829 | 5.658 | 5.872 | 6.445 | 6.278 | 6.657 | 6.024 | 6.599 | 6.278 | 6.657 | ns |
| | | GCLK PLL | $t_{co}$ | 3.557 | 3.839 | 5.659 | 5.873 | 6.444 | 6.277 | 6.656 | 6.023 | 6.597 | 6.277 | 6.656 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.547 | 3.830 | 5.657 | 5.871 | 6.443 | 6.276 | 6.655 | 6.023 | 6.597 | 6.276 | 6.655 | ns |
| | | GCLK PLL | $t_{co}$ | 3.533 | 3.816 | 5.642 | 5.856 | 6.429 | 6.262 | 6.641 | 6.008 | 6.582 | 6.262 | 6.641 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.530 | 3.812 | 5.638 | 5.852 | 6.425 | 6.258 | 6.637 | 6.004 | 6.578 | 6.258 | 6.637 | ns |
| | | GCLK PLL | $t_{co}$ | 3.527 | 3.810 | 5.639 | 5.855 | 6.428 | 6.261 | 6.640 | 6.007 | 6.582 | 6.261 | 6.640 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.528 | 3.810 | 5.629 | 5.843 | 6.415 | 6.248 | 6.627 | 5.994 | 6.568 | 6.248 | 6.627 | ns |
| | | GCLK PLL | $t_{co}$ | 3.577 | 3.863 | 5.700 | 5.916 | 6.491 | 6.324 | 6.703 | 6.068 | 6.644 | 6.324 | 6.703 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.553 | 3.839 | 5.682 | 5.899 | 6.474 | 6.307 | 6.686 | 6.051 | 6.629 | 6.307 | 6.686 | ns |
| | | GCLK PLL | $t_{co}$ | 3.535 | 3.820 | 5.660 | 5.877 | 6.452 | 6.285 | 6.664 | 6.029 | 6.607 | 6.285 | 6.664 | ns |

**Table 1–88.** EP3SL200 Row Pins Output Timing Parameters (Part 2 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.581 | 3.866 | 5.700 | 5.916 | 6.490 | 6.323 | 6.702 | 6.068 | 6.644 | 6.323 | 6.702 | ns |
| | | GCLK PLL | $t_{co}$ | 3.566 | 3.851 | 5.686 | 5.901 | 6.475 | 6.308 | 6.687 | 6.053 | 6.629 | 6.308 | 6.687 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.555 | 3.840 | 5.681 | 5.898 | 6.472 | 6.305 | 6.684 | 6.050 | 6.627 | 6.305 | 6.684 | ns |
| | | GCLK PLL | $t_{co}$ | 3.535 | 3.820 | 5.658 | 5.874 | 6.449 | 6.282 | 6.661 | 6.027 | 6.603 | 6.282 | 6.661 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.532 | 3.816 | 5.654 | 5.871 | 6.445 | 6.278 | 6.657 | 6.023 | 6.600 | 6.278 | 6.657 | ns |
| | | GCLK PLL | $t_{co}$ | 3.537 | 3.820 | 5.645 | 5.859 | 6.431 | 6.264 | 6.643 | 6.010 | 6.584 | 6.264 | 6.643 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.530 | 3.813 | 5.644 | 5.860 | 6.434 | 6.267 | 6.646 | 6.013 | 6.589 | 6.267 | 6.646 | ns |
| | | GCLK PLL | $t_{co}$ | 3.568 | 3.852 | 5.682 | 5.897 | 6.470 | 6.303 | 6.682 | 6.049 | 6.624 | 6.303 | 6.682 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.550 | 3.835 | 5.667 | 5.882 | 6.455 | 6.288 | 6.667 | 6.034 | 6.609 | 6.288 | 6.667 | ns |
| | | GCLK PLL | $t_{co}$ | 3.536 | 3.819 | 5.644 | 5.858 | 6.430 | 6.263 | 6.642 | 6.010 | 6.584 | 6.263 | 6.642 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.152 | 3.376 | 4.936 | 5.115 | 5.637 | 5.478 | 5.865 | 5.239 | 5.762 | 5.478 | 5.865 | ns |
| | | GCLK PLL | $t_{co}$ | 3.536 | 3.812 | 5.604 | 5.814 | 6.381 | 6.214 | 6.593 | 5.962 | 6.531 | 6.214 | 6.593 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.518 | 3.802 | 5.642 | 5.860 | 6.435 | 6.268 | 6.647 | 6.013 | 6.592 | 6.268 | 6.647 | ns |
| | | GCLK PLL | $t_{co}$ | 3.152 | 3.376 | 4.936 | 5.115 | 5.637 | 5.478 | 5.865 | 5.239 | 5.762 | 5.478 | 5.865 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.536 | 3.812 | 5.604 | 5.814 | 6.381 | 6.214 | 6.593 | 5.962 | 6.531 | 6.214 | 6.593 | ns |
| | | GCLK PLL | $t_{co}$ | 3.518 | 3.802 | 5.642 | 5.860 | 6.435 | 6.268 | 6.647 | 6.013 | 6.592 | 6.268 | 6.647 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.152 | 3.376 | 4.936 | 5.115 | 5.637 | 5.478 | 5.865 | 5.239 | 5.762 | 5.478 | 5.865 | ns |
| | | GCLK PLL | $t_{co}$ | 3.536 | 3.812 | 5.604 | 5.814 | 6.381 | 6.214 | 6.593 | 5.962 | 6.531 | 6.214 | 6.593 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.518 | 3.802 | 5.642 | 5.860 | 6.435 | 6.268 | 6.647 | 6.013 | 6.592 | 6.268 | 6.647 | ns |
| | | GCLK PLL | $t_{co}$ | 3.562 | 3.845 | 5.678 | 5.894 | 6.468 | 6.301 | 6.680 | 6.046 | 6.621 | 6.301 | 6.680 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.548 | 3.831 | 5.665 | 5.881 | 6.455 | 6.288 | 6.667 | 6.032 | 6.608 | 6.288 | 6.667 | ns |
| | | GCLK PLL | $t_{co}$ | 3.544 | 3.827 | 5.663 | 5.881 | 6.456 | 6.289 | 6.668 | 6.032 | 6.610 | 6.289 | 6.668 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.560 | 3.842 | 5.664 | 5.878 | 6.450 | 6.283 | 6.662 | 6.029 | 6.603 | 6.283 | 6.662 | ns |
| | | GCLK PLL | $t_{co}$ | 3.549 | 3.832 | 5.660 | 5.874 | 6.447 | 6.280 | 6.659 | 6.026 | 6.600 | 6.280 | 6.659 | ns |

**Table 1–88.** EP3SL200 Row Pins Output Timing Parameters (Part 3 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.546 | 3.829 | 5.658 | 5.872 | 6.445 | 6.278 | 6.657 | 6.024 | 6.599 | 6.278 | 6.657 | ns |
| | | GCLK PLL | $t_{co}$ | 3.557 | 3.839 | 5.659 | 5.873 | 6.444 | 6.277 | 6.656 | 6.023 | 6.597 | 6.277 | 6.656 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.547 | 3.830 | 5.657 | 5.871 | 6.443 | 6.276 | 6.655 | 6.023 | 6.597 | 6.276 | 6.655 | ns |
| | | GCLK PLL | $t_{co}$ | 3.533 | 3.816 | 5.642 | 5.856 | 6.429 | 6.262 | 6.641 | 6.008 | 6.582 | 6.262 | 6.641 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.530 | 3.812 | 5.638 | 5.852 | 6.425 | 6.258 | 6.637 | 6.004 | 6.578 | 6.258 | 6.637 | ns |
| | | GCLK PLL | $t_{co}$ | 3.527 | 3.810 | 5.639 | 5.855 | 6.428 | 6.261 | 6.640 | 6.007 | 6.582 | 6.261 | 6.640 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.528 | 3.810 | 5.629 | 5.843 | 6.415 | 6.248 | 6.627 | 5.994 | 6.568 | 6.248 | 6.627 | ns |
| | | GCLK PLL | $t_{co}$ | 3.577 | 3.863 | 5.700 | 5.916 | 6.491 | 6.324 | 6.703 | 6.068 | 6.644 | 6.324 | 6.703 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.553 | 3.839 | 5.682 | 5.899 | 6.474 | 6.307 | 6.686 | 6.051 | 6.629 | 6.307 | 6.686 | ns |
| | | GCLK PLL | $t_{co}$ | 3.535 | 3.820 | 5.660 | 5.877 | 6.452 | 6.285 | 6.664 | 6.029 | 6.607 | 6.285 | 6.664 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.581 | 3.866 | 5.700 | 5.916 | 6.490 | 6.323 | 6.702 | 6.068 | 6.644 | 6.323 | 6.702 | ns |
| | | GCLK PLL | $t_{co}$ | 3.566 | 3.851 | 5.686 | 5.901 | 6.475 | 6.308 | 6.687 | 6.053 | 6.629 | 6.308 | 6.687 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.555 | 3.840 | 5.681 | 5.898 | 6.472 | 6.305 | 6.684 | 6.050 | 6.627 | 6.305 | 6.684 | ns |
| | | GCLK PLL | $t_{co}$ | 3.535 | 3.820 | 5.658 | 5.874 | 6.449 | 6.282 | 6.661 | 6.027 | 6.603 | 6.282 | 6.661 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.532 | 3.816 | 5.654 | 5.871 | 6.445 | 6.278 | 6.657 | 6.023 | 6.600 | 6.278 | 6.657 | ns |
| | | GCLK PLL | $t_{co}$ | 3.537 | 3.820 | 5.645 | 5.859 | 6.431 | 6.264 | 6.643 | 6.010 | 6.584 | 6.264 | 6.643 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.530 | 3.813 | 5.644 | 5.860 | 6.434 | 6.267 | 6.646 | 6.013 | 6.589 | 6.267 | 6.646 | ns |
| | | GCLK PLL | $t_{co}$ | 3.568 | 3.852 | 5.682 | 5.897 | 6.470 | 6.303 | 6.682 | 6.049 | 6.624 | 6.303 | 6.682 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.550 | 3.835 | 5.667 | 5.882 | 6.455 | 6.288 | 6.667 | 6.034 | 6.609 | 6.288 | 6.667 | ns |
| | | GCLK PLL | $t_{co}$ | 3.536 | 3.819 | 5.644 | 5.858 | 6.430 | 6.263 | 6.642 | 6.010 | 6.584 | 6.263 | 6.642 | ns |

Table 1–89 and Table 1–90 list the EP3SL200 regional clock (RCLK) adder values that must be added to the GCLK values. Use these adder values to determine I/O timing when the I/O pin is driven using the regional clock. This applies to all I/O standards supported by Stratix III devices.

Table 1–89 lists the EP3SL200 column pin delay adders when using the regional clock.

**Table 1–89.** EP3SL200 Column Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.204 | 0.235 | 0.378 | 0.378 | 0.403 | 0.392 | 0.509 | 0.387 | 0.411 | 0.392 | 0.509 | ns |
| RCLK PLL input adder | 0.036 | 0.046 | 0.078 | 0.078 | -0.047 | -0.038 | -0.036 | 0.085 | -0.046 | -0.038 | -0.036 | ns |
| RCLK output adder | -0.211 | -0.234 | -0.332 | -0.328 | -0.34 | -0.334 | -0.464 | -0.327 | -0.339 | -0.334 | -0.464 | ns |
| RCLK PLL output adder | 1.904 | 1.965 | 3.193 | 3.323 | 3.688 | 3.496 | 3.804 | 3.351 | 3.716 | 3.496 | 3.804 | ns |

Table 1–90 lists the EP3SL200 row pin delay adders when using the regional clock.

**Table 1–90.** EP3SL200 Row Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.272 | 0.301 | 0.446 | 0.424 | 0.473 | 0.46 | 0.547 | 0.454 | 0.481 | 0.46 | 0.547 | ns |
| RCLK PLL input adder | 0.14 | 0.149 | 0.226 | 0.216 | 0.235 | 0.226 | 0.306 | 0.232 | 0.254 | 0.226 | 0.306 | ns |
| RCLK output adder | -0.278 | -0.306 | -0.418 | -0.434 | -0.486 | -0.472 | -0.592 | -0.464 | -0.493 | -0.472 | -0.592 | ns |
| RCLK PLL output adder | -0.15 | -0.15 | -0.227 | -0.233 | -0.254 | -0.243 | -0.322 | -0.243 | -0.258 | -0.243 | -0.322 | ns |

## EP3SL340 I/O Timing Parameters

Table 1–91 through Table 1–94 list the maximum I/O timing parameters for EP3SL340 devices for single-ended I/O standards.

Table 1–91 lists the EP3SL340 column pins input timing parameters for single-ended I/O standards.

**Table 1–91.** EP3SL340 Column Pins Input Timing Parameters (Part 1 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -1.345 | -1.335 | -2.017 | -2.061 | -2.330 | -2.245 | -2.542 | -2.061 | -2.330 | -2.245 | -2.542 | ns |
| | | $t_h$ | 1.486 | 1.476 | 2.232 | 2.284 | 2.574 | 2.476 | 2.783 | 2.284 | 2.574 | 2.476 | 2.783 | ns |
| | GCLK PLL | $t_{su}$ | -1.691 | -1.691 | -2.554 | -2.585 | -2.890 | -2.799 | -3.373 | -2.585 | -2.890 | -2.799 | -3.373 | ns |
| | | $t_h$ | 1.996 | 1.996 | 3.031 | 3.081 | 3.434 | 3.313 | 3.912 | 3.081 | 3.434 | 3.313 | 3.912 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -1.345 | -1.335 | -2.017 | -2.061 | -2.330 | -2.245 | -2.542 | -2.061 | -2.330 | -2.245 | -2.542 | ns |
| | | $t_h$ | 1.486 | 1.476 | 2.232 | 2.284 | 2.574 | 2.476 | 2.783 | 2.284 | 2.574 | 2.476 | 2.783 | ns |
| | GCLK PLL | $t_{su}$ | -1.691 | -1.691 | -2.554 | -2.585 | -2.890 | -2.799 | -3.373 | -2.585 | -2.890 | -2.799 | -3.373 | ns |
| | | $t_h$ | 1.996 | 1.996 | 3.031 | 3.081 | 3.434 | 3.313 | 3.912 | 3.081 | 3.434 | 3.313 | 3.912 | ns |

**Table 1–91.** EP3SL340 Column Pins Input Timing Parameters (Part 2 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -1.356 | -1.346 | -2.016 | -2.063 | -2.329 | -2.244 | -2.541 | -2.063 | -2.329 | -2.244 | -2.541 | ns |
| | | $t_h$ | 1.497 | 1.487 | 2.231 | 2.286 | 2.573 | 2.475 | 2.782 | 2.286 | 2.573 | 2.475 | 2.782 | ns |
| | GCLK PLL | $t_{su}$ | -1.702 | -1.702 | -2.553 | -2.587 | -2.889 | -2.798 | -3.372 | -2.587 | -2.889 | -2.798 | -3.372 | ns |
| | | $t_h$ | 2.007 | 2.007 | 3.030 | 3.083 | 3.433 | 3.312 | 3.911 | 3.083 | 3.433 | 3.312 | 3.911 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -1.356 | -1.346 | -2.016 | -2.063 | -2.329 | -2.244 | -2.541 | -2.063 | -2.329 | -2.244 | -2.541 | ns |
| | | $t_h$ | 1.497 | 1.487 | 2.231 | 2.286 | 2.573 | 2.475 | 2.782 | 2.286 | 2.573 | 2.475 | 2.782 | ns |
| | GCLK PLL | $t_{su}$ | -1.702 | -1.702 | -2.553 | -2.587 | -2.889 | -2.798 | -3.372 | -2.587 | -2.889 | -2.798 | -3.372 | ns |
| | | $t_h$ | 2.007 | 2.007 | 3.030 | 3.083 | 3.433 | 3.312 | 3.911 | 3.083 | 3.433 | 3.312 | 3.911 | ns |
| 2.5 V | GCLK | $t_{su}$ | -1.351 | -1.341 | -2.025 | -2.075 | -2.348 | -2.263 | -2.560 | -2.075 | -2.348 | -2.263 | -2.560 | ns |
| | | $t_h$ | 1.492 | 1.482 | 2.240 | 2.298 | 2.592 | 2.494 | 2.801 | 2.298 | 2.592 | 2.494 | 2.801 | ns |
| | GCLK PLL | $t_{su}$ | -1.697 | -1.697 | -2.562 | -2.599 | -2.908 | -2.817 | -3.391 | -2.599 | -2.908 | -2.817 | -3.391 | ns |
| | | $t_h$ | 2.002 | 2.002 | 3.039 | 3.095 | 3.452 | 3.331 | 3.930 | 3.095 | 3.452 | 3.331 | 3.930 | ns |
| 1.8 V | GCLK | $t_{su}$ | -1.373 | -1.363 | -2.065 | -2.111 | -2.346 | -2.261 | -2.558 | -2.111 | -2.346 | -2.261 | -2.558 | ns |
| | | $t_h$ | 1.516 | 1.506 | 2.280 | 2.334 | 2.590 | 2.492 | 2.799 | 2.334 | 2.590 | 2.492 | 2.799 | ns |
| | GCLK PLL | $t_{su}$ | -1.719 | -1.719 | -2.602 | -2.635 | -2.906 | -2.815 | -3.389 | -2.635 | -2.906 | -2.815 | -3.389 | ns |
| | | $t_h$ | 2.026 | 2.026 | 3.079 | 3.131 | 3.450 | 3.329 | 3.928 | 3.131 | 3.450 | 3.329 | 3.928 | ns |
| 1.5 V | GCLK | $t_{su}$ | -1.363 | -1.353 | -2.042 | -2.079 | -2.276 | -2.191 | -2.488 | -2.079 | -2.276 | -2.191 | -2.488 | ns |
| | | $t_h$ | 1.506 | 1.496 | 2.257 | 2.302 | 2.520 | 2.422 | 2.729 | 2.302 | 2.520 | 2.422 | 2.729 | ns |
| | GCLK PLL | $t_{su}$ | -1.709 | -1.709 | -2.579 | -2.603 | -2.836 | -2.745 | -3.319 | -2.603 | -2.836 | -2.745 | -3.319 | ns |
| | | $t_h$ | 2.016 | 2.016 | 3.056 | 3.099 | 3.380 | 3.259 | 3.858 | 3.099 | 3.380 | 3.259 | 3.858 | ns |
| 1.2 V | GCLK | $t_{su}$ | -1.311 | -1.301 | -1.965 | -1.980 | -2.120 | -2.035 | -2.332 | -1.980 | -2.120 | -2.035 | -2.332 | ns |
| | | $t_h$ | 1.454 | 1.444 | 2.180 | 2.203 | 2.364 | 2.266 | 2.573 | 2.203 | 2.364 | 2.266 | 2.573 | ns |
| | GCLK PLL | $t_{su}$ | -1.657 | -1.657 | -2.502 | -2.504 | -2.680 | -2.589 | -3.163 | -2.504 | -2.680 | -2.589 | -3.163 | ns |
| | | $t_h$ | 1.964 | 1.964 | 2.979 | 3.000 | 3.224 | 3.103 | 3.702 | 3.000 | 3.224 | 3.103 | 3.702 | ns |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -1.282 | -1.272 | -1.937 | -1.964 | -2.122 | -2.037 | -2.334 | -1.964 | -2.122 | -2.037 | -2.334 | ns |
| | | $t_h$ | 1.425 | 1.415 | 2.152 | 2.187 | 2.366 | 2.268 | 2.575 | 2.187 | 2.366 | 2.268 | 2.575 | ns |
| | GCLK PLL | $t_{su}$ | -1.628 | -1.628 | -2.474 | -2.488 | -2.682 | -2.591 | -3.165 | -2.488 | -2.682 | -2.591 | -3.165 | ns |
| | | $t_h$ | 1.935 | 1.935 | 2.951 | 2.984 | 3.226 | 3.105 | 3.704 | 2.984 | 3.226 | 3.105 | 3.704 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -1.282 | -1.272 | -1.937 | -1.964 | -2.122 | -2.037 | -2.334 | -1.964 | -2.122 | -2.037 | -2.334 | ns |
| | | $t_h$ | 1.425 | 1.415 | 2.152 | 2.187 | 2.366 | 2.268 | 2.575 | 2.187 | 2.366 | 2.268 | 2.575 | ns |
| | GCLK PLL | $t_{su}$ | -1.628 | -1.628 | -2.474 | -2.488 | -2.682 | -2.591 | -3.165 | -2.488 | -2.682 | -2.591 | -3.165 | ns |
| | | $t_h$ | 1.935 | 1.935 | 2.951 | 2.984 | 3.226 | 3.105 | 3.704 | 2.984 | 3.226 | 3.105 | 3.704 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -1.276 | -1.266 | -1.924 | -1.956 | -2.119 | -2.032 | -2.335 | -1.956 | -2.119 | -2.032 | -2.335 | ns |
| | | $t_h$ | 1.419 | 1.409 | 2.139 | 2.176 | 2.360 | 2.262 | 2.571 | 2.176 | 2.360 | 2.262 | 2.571 | ns |
| | GCLK PLL | $t_{su}$ | -1.622 | -1.622 | -2.461 | -2.480 | -2.679 | -2.586 | -3.163 | -2.480 | -2.679 | -2.586 | -3.163 | ns |
| | | $t_h$ | 1.929 | 1.929 | 2.938 | 2.973 | 3.220 | 3.099 | 3.697 | 2.973 | 3.220 | 3.099 | 3.697 | ns |

**Table 1–91.** EP3SL340 Column Pins Input Timing Parameters (Part 3 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -1.397 | -1.354 | -2.096 | -2.121 | -2.299 | -2.366 | -2.766 | -2.321 | -2.476 | -2.366 | -2.766 | ns |
| | | $t_h$ | 1.530 | 1.508 | 2.327 | 2.361 | 2.563 | 2.611 | 3.023 | 2.566 | 2.745 | 2.611 | 3.023 | ns |
| | GCLK PLL | $t_{su}$ | 0.785 | 0.779 | 1.380 | 1.479 | 1.654 | 1.670 | 1.679 | 1.480 | 1.660 | 1.670 | 1.679 | ns |
| | | $t_h$ | -0.510 | -0.485 | -0.912 | -0.992 | -1.113 | -1.156 | -1.144 | -0.982 | -1.107 | -1.156 | -1.144 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -1.397 | -1.354 | -2.096 | -2.121 | -2.299 | -2.366 | -2.766 | -2.321 | -2.476 | -2.366 | -2.766 | ns |
| | | $t_h$ | 1.530 | 1.508 | 2.327 | 2.361 | 2.563 | 2.611 | 3.023 | 2.566 | 2.745 | 2.611 | 3.023 | ns |
| | GCLK PLL | $t_{su}$ | 0.785 | 0.779 | 1.380 | 1.479 | 1.654 | 1.670 | 1.679 | 1.480 | 1.660 | 1.670 | 1.679 | ns |
| | | $t_h$ | -0.510 | -0.485 | -0.912 | -0.992 | -1.113 | -1.156 | -1.144 | -0.982 | -1.107 | -1.156 | -1.144 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -1.397 | -1.354 | -2.096 | -2.121 | -2.299 | -2.366 | -2.766 | -2.321 | -2.476 | -2.366 | -2.766 | ns |
| | | $t_h$ | 1.530 | 1.508 | 2.327 | 2.361 | 2.563 | 2.611 | 3.023 | 2.566 | 2.745 | 2.611 | 3.023 | ns |
| | GCLK PLL | $t_{su}$ | 0.785 | 0.779 | 1.380 | 1.479 | 1.654 | 1.670 | 1.679 | 1.480 | 1.660 | 1.670 | 1.679 | ns |
| | | $t_h$ | -0.510 | -0.485 | -0.912 | -0.992 | -1.113 | -1.156 | -1.144 | -0.982 | -1.107 | -1.156 | -1.144 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -1.397 | -1.354 | -2.096 | -2.121 | -2.299 | -2.366 | -2.766 | -2.321 | -2.476 | -2.366 | -2.766 | ns |
| | | $t_h$ | 1.530 | 1.508 | 2.327 | 2.361 | 2.563 | 2.611 | 3.023 | 2.566 | 2.745 | 2.611 | 3.023 | ns |
| | GCLK PLL | $t_{su}$ | 0.785 | 0.779 | 1.380 | 1.479 | 1.654 | 1.670 | 1.679 | 1.480 | 1.660 | 1.670 | 1.679 | ns |
| | | $t_h$ | -0.510 | -0.485 | -0.912 | -0.992 | -1.113 | -1.156 | -1.144 | -0.982 | -1.107 | -1.156 | -1.144 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -1.397 | -1.354 | -2.096 | -2.121 | -2.299 | -2.366 | -2.766 | -2.321 | -2.476 | -2.366 | -2.766 | ns |
| | | $t_h$ | 1.530 | 1.508 | 2.327 | 2.361 | 2.563 | 2.611 | 3.023 | 2.566 | 2.745 | 2.611 | 3.023 | ns |
| | GCLK PLL | $t_{su}$ | 0.785 | 0.779 | 1.380 | 1.479 | 1.654 | 1.670 | 1.679 | 1.480 | 1.660 | 1.670 | 1.679 | ns |
| | | $t_h$ | -0.510 | -0.485 | -0.912 | -0.992 | -1.113 | -1.156 | -1.144 | -0.982 | -1.107 | -1.156 | -1.144 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -1.397 | -1.354 | -2.096 | -2.121 | -2.299 | -2.366 | -2.766 | -2.321 | -2.476 | -2.366 | -2.766 | ns |
| | | $t_h$ | 1.530 | 1.508 | 2.327 | 2.361 | 2.563 | 2.611 | 3.023 | 2.566 | 2.745 | 2.611 | 3.023 | ns |
| | GCLK PLL | $t_{su}$ | 0.785 | 0.779 | 1.380 | 1.479 | 1.654 | 1.670 | 1.679 | 1.480 | 1.660 | 1.670 | 1.679 | ns |
| | | $t_h$ | -0.510 | -0.485 | -0.912 | -0.992 | -1.113 | -1.156 | -1.144 | -0.982 | -1.107 | -1.156 | -1.144 | ns |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -1.397 | -1.354 | -2.096 | -2.121 | -2.299 | -2.366 | -2.766 | -2.321 | -2.476 | -2.366 | -2.766 | ns |
| | | $t_h$ | 1.530 | 1.508 | 2.327 | 2.361 | 2.563 | 2.611 | 3.023 | 2.566 | 2.745 | 2.611 | 3.023 | ns |
| | GCLK PLL | $t_{su}$ | 0.785 | 0.779 | 1.380 | 1.479 | 1.654 | 1.670 | 1.679 | 1.480 | 1.660 | 1.670 | 1.679 | ns |
| | | $t_h$ | -0.510 | -0.485 | -0.912 | -0.992 | -1.113 | -1.156 | -1.144 | -0.982 | -1.107 | -1.156 | -1.144 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -1.397 | -1.354 | -2.096 | -2.121 | -2.299 | -2.366 | -2.766 | -2.321 | -2.476 | -2.366 | -2.766 | ns |
| | | $t_h$ | 1.530 | 1.508 | 2.327 | 2.361 | 2.563 | 2.611 | 3.023 | 2.566 | 2.745 | 2.611 | 3.023 | ns |
| | GCLK PLL | $t_{su}$ | 0.785 | 0.779 | 1.380 | 1.479 | 1.654 | 1.670 | 1.679 | 1.480 | 1.660 | 1.670 | 1.679 | ns |
| | | $t_h$ | -0.510 | -0.485 | -0.912 | -0.992 | -1.113 | -1.156 | -1.144 | -0.982 | -1.107 | -1.156 | -1.144 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -1.397 | -1.354 | -2.096 | -2.121 | -2.299 | -2.366 | -2.766 | -2.321 | -2.476 | -2.366 | -2.766 | ns |
| | | $t_h$ | 1.530 | 1.508 | 2.327 | 2.361 | 2.563 | 2.611 | 3.023 | 2.566 | 2.745 | 2.611 | 3.023 | ns |
| | GCLK PLL | $t_{su}$ | 0.785 | 0.779 | 1.380 | 1.479 | 1.654 | 1.670 | 1.679 | 1.480 | 1.660 | 1.670 | 1.679 | ns |
| | | $t_h$ | -0.510 | -0.485 | -0.912 | -0.992 | -1.113 | -1.156 | -1.144 | -0.982 | -1.107 | -1.156 | -1.144 | ns |

**Table 1–91.** EP3SL340 Column Pins Input Timing Parameters (Part 4 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V PCI-X | GCLK | $t_{su}$ | -1.356 | -1.346 | -2.016 | -2.063 | -2.329 | -2.244 | -2.541 | -2.063 | -2.329 | -2.244 | -2.541 | ns |
| | | $t_h$ | 1.497 | 1.487 | 2.231 | 2.286 | 2.573 | 2.475 | 2.782 | 2.286 | 2.573 | 2.475 | 2.782 | ns |
| | GCLK PLL | $t_{su}$ | -1.702 | -1.702 | -2.553 | -2.587 | -2.889 | -2.798 | -3.372 | -2.587 | -2.889 | -2.798 | -3.372 | ns |
| | | $t_h$ | 2.007 | 2.007 | 3.030 | 3.083 | 3.433 | 3.312 | 3.911 | 3.083 | 3.433 | 3.312 | 3.911 | ns |

Table 1–92 lists the EP3SL340 row pins input timing parameters for single-ended I/O standards.

**Table 1–92.** EP3SL340 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -1.239 | -1.296 | -1.925 | -1.956 | -2.199 | -2.135 | -2.587 | -1.973 | -2.204 | -2.142 | -2.522 | ns |
| | | $t_h$ | 1.362 | 1.435 | 2.137 | 2.177 | 2.442 | 2.366 | 2.822 | 2.205 | 2.456 | 2.382 | 2.763 | ns |
| | GCLK PLL | $t_{su}$ | 0.879 | 0.945 | 1.670 | 1.687 | 1.786 | 1.680 | 1.689 | 1.689 | 1.807 | 1.695 | 1.746 | ns |
| | | $t_h$ | -0.615 | -0.660 | -1.216 | -1.217 | -1.263 | -1.188 | -1.178 | -1.208 | -1.273 | -1.193 | -1.231 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -1.239 | -1.296 | -1.925 | -1.956 | -2.199 | -2.135 | -2.587 | -1.973 | -2.204 | -2.142 | -2.522 | ns |
| | | $t_h$ | 1.362 | 1.435 | 2.137 | 2.177 | 2.442 | 2.366 | 2.822 | 2.205 | 2.456 | 2.382 | 2.763 | ns |
| | GCLK PLL | $t_{su}$ | 0.879 | 0.945 | 1.670 | 1.687 | 1.786 | 1.680 | 1.689 | 1.689 | 1.807 | 1.695 | 1.746 | ns |
| | | $t_h$ | -0.615 | -0.660 | -1.216 | -1.217 | -1.263 | -1.188 | -1.178 | -1.208 | -1.273 | -1.193 | -1.231 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -1.245 | -1.307 | -1.922 | -1.957 | -2.202 | -2.138 | -2.590 | -1.972 | -2.209 | -2.147 | -2.527 | ns |
| | | $t_h$ | 1.368 | 1.446 | 2.134 | 2.178 | 2.445 | 2.369 | 2.825 | 2.204 | 2.461 | 2.387 | 2.768 | ns |
| | GCLK PLL | $t_{su}$ | 0.873 | 0.934 | 1.673 | 1.686 | 1.783 | 1.677 | 1.686 | 1.690 | 1.802 | 1.690 | 1.741 | ns |
| | | $t_h$ | -0.609 | -0.649 | -1.219 | -1.216 | -1.260 | -1.185 | -1.175 | -1.209 | -1.268 | -1.188 | -1.226 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -1.245 | -1.307 | -1.922 | -1.957 | -2.202 | -2.138 | -2.590 | -1.972 | -2.209 | -2.147 | -2.527 | ns |
| | | $t_h$ | 1.368 | 1.446 | 2.134 | 2.178 | 2.445 | 2.369 | 2.825 | 2.204 | 2.461 | 2.387 | 2.768 | ns |
| | GCLK PLL | $t_{su}$ | 0.873 | 0.934 | 1.673 | 1.686 | 1.783 | 1.677 | 1.686 | 1.690 | 1.802 | 1.690 | 1.741 | ns |
| | | $t_h$ | -0.609 | -0.649 | -1.219 | -1.216 | -1.260 | -1.185 | -1.175 | -1.209 | -1.268 | -1.188 | -1.226 | ns |
| 2.5 V | GCLK | $t_{su}$ | -1.233 | -1.300 | -1.931 | -1.970 | -2.217 | -2.153 | -2.605 | -1.981 | -2.219 | -2.157 | -2.537 | ns |
| | | $t_h$ | 1.356 | 1.439 | 2.143 | 2.191 | 2.460 | 2.384 | 2.840 | 2.213 | 2.471 | 2.397 | 2.778 | ns |
| | GCLK PLL | $t_{su}$ | 0.885 | 0.941 | 1.664 | 1.673 | 1.768 | 1.662 | 1.671 | 1.681 | 1.792 | 1.680 | 1.731 | ns |
| | | $t_h$ | -0.621 | -0.656 | -1.210 | -1.203 | -1.245 | -1.170 | -1.160 | -1.200 | -1.258 | -1.178 | -1.216 | ns |
| 1.8 V | GCLK | $t_{su}$ | -1.251 | -1.343 | -1.980 | -1.995 | -2.204 | -2.138 | -2.582 | -2.003 | -2.208 | -2.153 | -2.621 | ns |
| | | $t_h$ | 1.377 | 1.482 | 2.193 | 2.216 | 2.447 | 2.369 | 2.817 | 2.234 | 2.461 | 2.393 | 2.859 | ns |
| | GCLK PLL | $t_{su}$ | 0.827 | 0.910 | 1.624 | 1.634 | 1.857 | 1.742 | 1.565 | 1.620 | 1.886 | 1.762 | 1.619 | ns |
| | | $t_h$ | -0.562 | -0.624 | -1.170 | -1.164 | -1.330 | -1.246 | -1.060 | -1.140 | -1.347 | -1.255 | -1.107 | ns |

**Table 1–92.** EP3SL340 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5 V | GCLK | $t_{su}$ | -1.241 | -1.332 | -1.956 | -1.963 | -2.136 | -2.070 | -2.514 | -1.972 | -2.143 | -2.088 | -2.556 | ns |
| | | $t_h$ | 1.367 | 1.471 | 2.169 | 2.184 | 2.379 | 2.301 | 2.749 | 2.203 | 2.396 | 2.328 | 2.794 | ns |
| | GCLK PLL | $t_{su}$ | 0.837 | 0.921 | 1.648 | 1.666 | 1.925 | 1.810 | 1.633 | 1.651 | 1.951 | 1.827 | 1.684 | ns |
| | | $t_h$ | -0.572 | -0.635 | -1.194 | -1.196 | -1.398 | -1.314 | -1.128 | -1.171 | -1.412 | -1.320 | -1.172 | ns |
| 1.2 V | GCLK | $t_{su}$ | -1.181 | -1.279 | -1.877 | -1.862 | -1.977 | -1.911 | -2.355 | -1.876 | -1.988 | -1.933 | -2.401 | ns |
| | | $t_h$ | 1.307 | 1.418 | 2.090 | 2.083 | 2.220 | 2.142 | 2.590 | 2.107 | 2.241 | 2.173 | 2.639 | ns |
| | GCLK PLL | $t_{su}$ | 0.897 | 0.974 | 1.727 | 1.767 | 2.084 | 1.969 | 1.792 | 1.747 | 2.106 | 1.982 | 1.839 | ns |
| | | $t_h$ | -0.632 | -0.688 | -1.273 | -1.297 | -1.557 | -1.473 | -1.287 | -1.267 | -1.567 | -1.475 | -1.327 | ns |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -1.176 | -1.242 | -1.845 | -1.861 | -1.997 | -1.933 | -2.385 | -1.869 | -2.002 | -1.940 | -2.320 | ns |
| | | $t_h$ | 1.300 | 1.382 | 2.057 | 2.082 | 2.240 | 2.164 | 2.620 | 2.101 | 2.254 | 2.180 | 2.561 | ns |
| | GCLK PLL | $t_{su}$ | 0.942 | 1.000 | 1.750 | 1.782 | 1.988 | 1.882 | 1.891 | 1.793 | 2.009 | 1.897 | 1.948 | ns |
| | | $t_h$ | -0.677 | -0.714 | -1.296 | -1.312 | -1.465 | -1.390 | -1.380 | -1.312 | -1.475 | -1.395 | -1.433 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -1.176 | -1.242 | -1.845 | -1.861 | -1.997 | -1.933 | -2.385 | -1.869 | -2.002 | -1.940 | -2.320 | ns |
| | | $t_h$ | 1.300 | 1.382 | 2.057 | 2.082 | 2.240 | 2.164 | 2.620 | 2.101 | 2.254 | 2.180 | 2.561 | ns |
| | GCLK PLL | $t_{su}$ | 0.942 | 1.000 | 1.750 | 1.782 | 1.988 | 1.882 | 1.891 | 1.793 | 2.009 | 1.897 | 1.948 | ns |
| | | $t_h$ | -0.677 | -0.714 | -1.296 | -1.312 | -1.465 | -1.390 | -1.380 | -1.312 | -1.475 | -1.395 | -1.433 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -1.155 | -1.244 | -1.839 | -1.835 | -1.972 | -1.905 | -2.351 | -1.844 | -1.981 | -1.925 | -2.394 | ns |
| | | $t_h$ | 1.281 | 1.383 | 2.052 | 2.054 | 2.213 | 2.135 | 2.582 | 2.073 | 2.231 | 2.164 | 2.628 | ns |
| | GCLK PLL | $t_{su}$ | 0.923 | 1.009 | 1.765 | 1.794 | 2.086 | 1.972 | 1.796 | 1.779 | 2.110 | 1.988 | 1.846 | ns |
| | | $t_h$ | -0.658 | -0.723 | -1.311 | -1.326 | -1.562 | -1.478 | -1.295 | -1.301 | -1.574 | -1.482 | -1.338 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -1.155 | -1.244 | -1.839 | -1.835 | -1.972 | -1.905 | -2.351 | -1.844 | -1.981 | -1.925 | -2.394 | ns |
| | | $t_h$ | 1.281 | 1.383 | 2.052 | 2.054 | 2.213 | 2.135 | 2.582 | 2.073 | 2.231 | 2.164 | 2.628 | ns |
| | GCLK PLL | $t_{su}$ | 0.923 | 1.009 | 1.765 | 1.794 | 2.086 | 1.972 | 1.796 | 1.779 | 2.110 | 1.988 | 1.846 | ns |
| | | $t_h$ | -0.658 | -0.723 | -1.311 | -1.326 | -1.562 | -1.478 | -1.295 | -1.301 | -1.574 | -1.482 | -1.338 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -1.141 | -1.232 | -1.824 | -1.825 | -1.954 | -1.887 | -2.333 | -1.833 | -1.964 | -1.908 | -2.377 | ns |
| | | $t_h$ | 1.267 | 1.371 | 2.038 | 2.044 | 2.195 | 2.117 | 2.564 | 2.062 | 2.214 | 2.147 | 2.611 | ns |
| | GCLK PLL | $t_{su}$ | 0.937 | 1.021 | 1.778 | 1.804 | 2.104 | 1.990 | 1.814 | 1.790 | 2.127 | 2.005 | 1.863 | ns |
| | | $t_h$ | -0.672 | -0.735 | -1.323 | -1.336 | -1.580 | -1.496 | -1.313 | -1.312 | -1.591 | -1.499 | -1.355 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -1.155 | -1.244 | -1.839 | -1.835 | -1.972 | -1.905 | -2.351 | -1.844 | -1.981 | -1.925 | -2.394 | ns |
| | | $t_h$ | 1.281 | 1.383 | 2.052 | 2.054 | 2.213 | 2.135 | 2.582 | 2.073 | 2.231 | 2.164 | 2.628 | ns |
| | GCLK PLL | $t_{su}$ | 0.923 | 1.009 | 1.765 | 1.794 | 2.086 | 1.972 | 1.796 | 1.779 | 2.110 | 1.988 | 1.846 | ns |
| | | $t_h$ | -0.658 | -0.723 | -1.311 | -1.326 | -1.562 | -1.478 | -1.295 | -1.301 | -1.574 | -1.482 | -1.338 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -1.155 | -1.244 | -1.839 | -1.835 | -1.972 | -1.905 | -2.351 | -1.844 | -1.981 | -1.925 | -2.394 | ns |
| | | $t_h$ | 1.281 | 1.383 | 2.052 | 2.054 | 2.213 | 2.135 | 2.582 | 2.073 | 2.231 | 2.164 | 2.628 | ns |
| | GCLK PLL | $t_{su}$ | 0.923 | 1.009 | 1.765 | 1.794 | 2.086 | 1.972 | 1.796 | 1.779 | 2.110 | 1.988 | 1.846 | ns |
| | | $t_h$ | -0.658 | -0.723 | -1.311 | -1.326 | -1.562 | -1.478 | -1.295 | -1.301 | -1.574 | -1.482 | -1.338 | ns |

**Table 1–92.** EP3SL340 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -1.141 | -1.232 | -1.824 | -1.825 | -1.954 | -1.887 | -2.333 | -1.833 | -1.964 | -1.908 | -2.377 | ns |
| | | $t_h$ | 1.267 | 1.371 | 2.038 | 2.044 | 2.195 | 2.117 | 2.564 | 2.062 | 2.214 | 2.147 | 2.611 | ns |
| | GCLK PLL | $t_{su}$ | 0.937 | 1.021 | 1.778 | 1.804 | 2.104 | 1.990 | 1.814 | 1.790 | 2.127 | 2.005 | 1.863 | ns |
| | | $t_h$ | -0.672 | -0.735 | -1.323 | -1.336 | -1.580 | -1.496 | -1.313 | -1.312 | -1.591 | -1.499 | -1.355 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -1.141 | -1.232 | -1.824 | -1.825 | -1.954 | -1.887 | -2.333 | -1.833 | -1.964 | -1.908 | -2.377 | ns |
| | | $t_h$ | 1.267 | 1.371 | 2.038 | 2.044 | 2.195 | 2.117 | 2.564 | 2.062 | 2.214 | 2.147 | 2.611 | ns |
| | GCLK PLL | $t_{su}$ | 0.937 | 1.021 | 1.778 | 1.804 | 2.104 | 1.990 | 1.814 | 1.790 | 2.127 | 2.005 | 1.863 | ns |
| | | $t_h$ | -0.672 | -0.735 | -1.323 | -1.336 | -1.580 | -1.496 | -1.313 | -1.312 | -1.591 | -1.499 | -1.355 | ns |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -1.132 | -1.220 | -1.815 | -1.815 | -1.938 | -1.871 | -2.317 | -1.824 | -1.948 | -1.892 | -2.361 | ns |
| | | $t_h$ | 1.258 | 1.359 | 2.029 | 2.034 | 2.179 | 2.101 | 2.548 | 2.053 | 2.198 | 2.131 | 2.595 | ns |
| | GCLK PLL | $t_{su}$ | 0.946 | 1.033 | 1.787 | 1.814 | 2.120 | 2.006 | 1.830 | 1.799 | 2.143 | 2.021 | 1.879 | ns |
| | | $t_h$ | -0.681 | -0.747 | -1.332 | -1.346 | -1.596 | -1.512 | -1.329 | -1.321 | -1.607 | -1.515 | -1.371 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -1.132 | -1.220 | -1.815 | -1.815 | -1.938 | -1.871 | -2.317 | -1.824 | -1.948 | -1.892 | -2.361 | ns |
| | | $t_h$ | 1.258 | 1.359 | 2.029 | 2.034 | 2.179 | 2.101 | 2.548 | 2.053 | 2.198 | 2.131 | 2.595 | ns |
| | GCLK PLL | $t_{su}$ | 0.946 | 1.033 | 1.787 | 1.814 | 2.120 | 2.006 | 1.830 | 1.799 | 2.143 | 2.021 | 1.879 | ns |
| | | $t_h$ | -0.681 | -0.747 | -1.332 | -1.346 | -1.596 | -1.512 | -1.329 | -1.321 | -1.607 | -1.515 | -1.371 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -1.245 | -1.307 | -1.922 | -1.957 | -2.202 | -2.138 | -2.590 | -1.972 | -2.209 | -2.147 | -2.527 | ns |
| | | $t_h$ | 1.368 | 1.446 | 2.134 | 2.178 | 2.445 | 2.369 | 2.825 | 2.204 | 2.461 | 2.387 | 2.768 | ns |
| | GCLK PLL | $t_{su}$ | 0.873 | 0.934 | 1.673 | 1.686 | 1.783 | 1.677 | 1.686 | 1.690 | 1.802 | 1.690 | 1.741 | ns |
| | | $t_h$ | -0.609 | -0.649 | -1.219 | -1.216 | -1.260 | -1.185 | -1.175 | -1.209 | -1.268 | -1.188 | -1.226 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | -1.245 | -1.307 | -1.922 | -1.957 | -2.202 | -2.138 | -2.590 | -1.972 | -2.209 | -2.147 | -2.527 | ns |
| | | $t_h$ | 1.368 | 1.446 | 2.134 | 2.178 | 2.445 | 2.369 | 2.825 | 2.204 | 2.461 | 2.387 | 2.768 | ns |
| | GCLK PLL | $t_{su}$ | 0.873 | 0.934 | 1.673 | 1.686 | 1.783 | 1.677 | 1.686 | 1.690 | 1.802 | 1.690 | 1.741 | ns |
| | | $t_h$ | -0.609 | -0.649 | -1.219 | -1.216 | -1.260 | -1.185 | -1.175 | -1.209 | -1.268 | -1.188 | -1.226 | ns |

Table 1–93 lists the EP3SL340 column pins output timing parameters for single-ended I/O standards.

**Table 1–93.** EP3SL340 Column Pins Output Timing Parameters (Part 1 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.705 | 3.705 | 5.372 | 5.559 | 6.083 | 5.935 | 6.364 | 5.559 | 6.083 | 5.935 | 6.364 | ns |
| | | GCLK PLL | $t_{co}$ | 4.269 | 4.269 | 6.214 | 6.409 | 6.992 | 6.812 | 7.355 | 6.409 | 6.992 | 6.812 | 7.355 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.638 | 3.638 | 5.263 | 5.448 | 5.970 | 5.822 | 6.251 | 5.448 | 5.970 | 5.822 | 6.251 | ns |
| | | GCLK PLL | $t_{co}$ | 4.202 | 4.202 | 6.105 | 6.298 | 6.879 | 6.699 | 7.242 | 6.298 | 6.879 | 6.699 | 7.242 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.552 | 3.552 | 5.160 | 5.350 | 5.878 | 5.730 | 6.159 | 5.350 | 5.878 | 5.730 | 6.159 | ns |
| | | GCLK PLL | $t_{co}$ | 4.116 | 4.116 | 6.001 | 6.200 | 6.789 | 6.609 | 7.152 | 6.200 | 6.789 | 6.609 | 7.152 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.545 | 3.545 | 5.143 | 5.322 | 5.837 | 5.689 | 6.118 | 5.322 | 5.837 | 5.689 | 6.118 | ns |
| | | GCLK PLL | $t_{co}$ | 4.110 | 4.110 | 5.985 | 6.172 | 6.747 | 6.567 | 7.110 | 6.172 | 6.747 | 6.567 | 7.110 | ns |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.711 | 3.711 | 5.377 | 5.564 | 6.090 | 5.942 | 6.371 | 5.564 | 6.090 | 5.942 | 6.371 | ns |
| | | GCLK PLL | $t_{co}$ | 4.275 | 4.275 | 6.218 | 6.414 | 7.000 | 6.820 | 7.363 | 6.414 | 7.000 | 6.820 | 7.363 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.556 | 3.556 | 5.170 | 5.367 | 5.889 | 5.741 | 6.170 | 5.367 | 5.889 | 5.741 | 6.170 | ns |
| | | GCLK PLL | $t_{co}$ | 4.120 | 4.120 | 6.012 | 6.217 | 6.799 | 6.619 | 7.162 | 6.217 | 6.799 | 6.619 | 7.162 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.563 | 3.563 | 5.164 | 5.346 | 5.863 | 5.715 | 6.144 | 5.346 | 5.863 | 5.715 | 6.144 | ns |
| | | GCLK PLL | $t_{co}$ | 4.127 | 4.127 | 6.006 | 6.196 | 6.775 | 6.595 | 7.138 | 6.196 | 6.775 | 6.595 | 7.138 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.547 | 3.547 | 5.141 | 5.320 | 5.834 | 5.686 | 6.115 | 5.320 | 5.834 | 5.686 | 6.115 | ns |
| | | GCLK PLL | $t_{co}$ | 4.111 | 4.111 | 5.983 | 6.171 | 6.746 | 6.566 | 7.109 | 6.171 | 6.746 | 6.566 | 7.109 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.669 | 3.669 | 5.339 | 5.528 | 6.050 | 5.902 | 6.331 | 5.528 | 6.050 | 5.902 | 6.331 | ns |
| | | GCLK PLL | $t_{co}$ | 4.232 | 4.232 | 6.181 | 6.377 | 6.983 | 6.803 | 7.346 | 6.377 | 6.983 | 6.803 | 7.346 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.558 | 3.558 | 5.209 | 5.394 | 5.912 | 5.765 | 6.193 | 5.394 | 5.912 | 5.765 | 6.193 | ns |
| | | GCLK PLL | $t_{co}$ | 4.125 | 4.125 | 6.053 | 6.246 | 6.867 | 6.688 | 7.229 | 6.246 | 6.867 | 6.688 | 7.229 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.522 | 3.522 | 5.146 | 5.325 | 5.838 | 5.691 | 6.119 | 5.325 | 5.838 | 5.691 | 6.119 | ns |
| | | GCLK PLL | $t_{co}$ | 4.087 | 4.087 | 5.987 | 6.174 | 6.803 | 6.624 | 7.165 | 6.174 | 6.803 | 6.624 | 7.165 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.504 | 3.504 | 5.117 | 5.297 | 5.810 | 5.662 | 6.091 | 5.297 | 5.810 | 5.662 | 6.091 | ns |
| | | GCLK PLL | $t_{co}$ | 4.068 | 4.068 | 5.959 | 6.147 | 6.780 | 6.601 | 7.142 | 6.147 | 6.780 | 6.601 | 7.142 | ns |

**Table 1–93.** EP3SL340 Column Pins Output Timing Parameters (Part 2 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.583 | 3.583 | 5.243 | 5.427 | 5.947 | 5.800 | 6.228 | 5.427 | 5.947 | 5.800 | 6.228 | ns |
| | | GCLK PLL | $t_{co}$ | 4.149 | 4.149 | 6.087 | 6.279 | 6.903 | 6.724 | 7.265 | 6.279 | 6.903 | 6.724 | 7.265 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.504 | 3.504 | 5.120 | 5.298 | 5.812 | 5.665 | 6.093 | 5.298 | 5.812 | 5.665 | 6.093 | ns |
| | | GCLK PLL | $t_{co}$ | 4.070 | 4.070 | 5.963 | 6.149 | 6.793 | 6.614 | 7.155 | 6.149 | 6.793 | 6.614 | 7.155 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.499 | 3.499 | 5.112 | 5.291 | 5.804 | 5.656 | 6.085 | 5.291 | 5.804 | 5.656 | 6.085 | ns |
| | | GCLK PLL | $t_{co}$ | 4.063 | 4.063 | 5.955 | 6.142 | 6.761 | 6.581 | 7.124 | 6.142 | 6.761 | 6.581 | 7.124 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.490 | 3.490 | 5.098 | 5.276 | 5.789 | 5.641 | 6.070 | 5.276 | 5.789 | 5.641 | 6.070 | ns |
| | | GCLK PLL | $t_{co}$ | 4.054 | 4.054 | 5.940 | 6.126 | 6.767 | 6.588 | 7.129 | 6.126 | 6.767 | 6.588 | 7.129 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.705 | 3.705 | 5.450 | 5.654 | 6.194 | 6.047 | 6.475 | 5.654 | 6.194 | 6.047 | 6.475 | ns |
| | | GCLK PLL | $t_{co}$ | 4.269 | 4.269 | 6.293 | 6.504 | 7.111 | 6.932 | 7.473 | 6.504 | 7.111 | 6.932 | 7.473 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.605 | 3.605 | 5.331 | 5.528 | 6.062 | 5.915 | 6.343 | 5.528 | 6.062 | 5.915 | 6.343 | ns |
| | | GCLK PLL | $t_{co}$ | 4.172 | 4.172 | 6.174 | 6.379 | 6.987 | 6.808 | 7.349 | 6.379 | 6.987 | 6.808 | 7.349 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.561 | 3.561 | 5.244 | 5.438 | 5.967 | 5.819 | 6.248 | 5.438 | 5.967 | 5.819 | 6.248 | ns |
| | | GCLK PLL | $t_{co}$ | 4.127 | 4.127 | 6.087 | 6.288 | 6.909 | 6.730 | 7.271 | 6.288 | 6.909 | 6.730 | 7.271 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.523 | 3.523 | 5.205 | 5.395 | 5.924 | 5.776 | 6.205 | 5.395 | 5.924 | 5.776 | 6.205 | ns |
| | | GCLK PLL | $t_{co}$ | 4.088 | 4.088 | 6.048 | 6.246 | 6.852 | 6.673 | 7.214 | 6.246 | 6.852 | 6.673 | 7.214 | ns |

**Table 1–93.** EP3SL340 Column Pins Output Timing Parameters (Part 3 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.896 | 3.896 | 5.772 | 6.014 | 6.599 | 6.451 | 6.880 | 6.014 | 6.599 | 6.451 | 6.880 | ns |
| | | GCLK PLL | $t_{co}$ | 4.460 | 4.460 | 6.613 | 6.863 | 7.507 | 7.327 | 7.870 | 6.863 | 7.507 | 7.327 | 7.870 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.715 | 3.715 | 5.493 | 5.705 | 6.251 | 6.104 | 6.532 | 5.705 | 6.251 | 6.104 | 6.532 | ns |
| | | GCLK PLL | $t_{co}$ | 4.282 | 4.282 | 6.336 | 6.556 | 7.177 | 6.998 | 7.539 | 6.556 | 7.177 | 6.998 | 7.539 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.633 | 3.633 | 5.386 | 5.590 | 6.141 | 5.993 | 6.422 | 5.590 | 6.141 | 5.993 | 6.422 | ns |
| | | GCLK PLL | $t_{co}$ | 4.197 | 4.197 | 6.227 | 6.440 | 7.064 | 6.884 | 7.427 | 6.440 | 7.064 | 6.884 | 7.427 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.613 | 3.613 | 5.327 | 5.537 | 6.075 | 5.927 | 6.356 | 5.537 | 6.075 | 5.927 | 6.356 | ns |
| | | GCLK PLL | $t_{co}$ | 4.177 | 4.177 | 6.169 | 6.386 | 6.987 | 6.807 | 7.350 | 6.386 | 6.987 | 6.807 | 7.350 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.550 | 3.550 | 5.266 | 5.462 | 5.994 | 5.846 | 6.275 | 5.462 | 5.994 | 5.846 | 6.275 | ns |
| | | GCLK PLL | $t_{co}$ | 4.114 | 4.114 | 6.109 | 6.312 | 6.918 | 6.738 | 7.281 | 6.312 | 6.918 | 6.738 | 7.281 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.532 | 3.532 | 5.246 | 5.440 | 5.971 | 5.823 | 6.252 | 5.440 | 5.971 | 5.823 | 6.252 | ns |
| | | GCLK PLL | $t_{co}$ | 4.097 | 4.097 | 6.088 | 6.291 | 6.885 | 6.705 | 7.248 | 6.291 | 6.885 | 6.705 | 7.248 | ns |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.842 | 3.842 | 5.700 | 5.947 | 6.537 | 6.389 | 6.818 | 5.947 | 6.537 | 6.389 | 6.818 | ns |
| | | GCLK PLL | $t_{co}$ | 4.406 | 4.406 | 6.542 | 6.796 | 7.452 | 7.272 | 7.815 | 6.796 | 7.452 | 7.272 | 7.815 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.630 | 3.630 | 5.381 | 5.590 | 6.145 | 5.997 | 6.426 | 5.590 | 6.145 | 5.997 | 6.426 | ns |
| | | GCLK PLL | $t_{co}$ | 4.194 | 4.194 | 6.223 | 6.439 | 7.066 | 6.886 | 7.429 | 6.439 | 7.066 | 6.886 | 7.429 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.605 | 3.605 | 5.314 | 5.530 | 6.078 | 5.930 | 6.359 | 5.530 | 6.078 | 5.930 | 6.359 | ns |
| | | GCLK PLL | $t_{co}$ | 4.170 | 4.170 | 6.156 | 6.381 | 6.989 | 6.809 | 7.352 | 6.381 | 6.989 | 6.809 | 7.352 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.594 | 3.594 | 5.297 | 5.505 | 6.058 | 5.910 | 6.339 | 5.505 | 6.058 | 5.910 | 6.339 | ns |
| | | GCLK PLL | $t_{co}$ | 4.158 | 4.158 | 6.140 | 6.356 | 6.972 | 6.792 | 7.335 | 6.356 | 6.972 | 6.792 | 7.335 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.539 | 3.539 | 5.259 | 5.455 | 5.988 | 5.840 | 6.269 | 5.455 | 5.988 | 5.840 | 6.269 | ns |
| | | GCLK PLL | $t_{co}$ | 4.103 | 4.103 | 6.101 | 6.305 | 6.909 | 6.729 | 7.272 | 6.305 | 6.909 | 6.729 | 7.272 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.534 | 3.534 | 5.243 | 5.443 | 5.977 | 5.829 | 6.258 | 5.443 | 5.977 | 5.829 | 6.258 | ns |
| | | GCLK PLL | $t_{co}$ | 4.097 | 4.097 | 6.084 | 6.292 | 6.888 | 6.708 | 7.251 | 6.292 | 6.888 | 6.708 | 7.251 | ns |


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**Table 1–93.** EP3SL340 Column Pins Output Timing Parameters (Part 4 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.758 | 3.758 | 5.626 | 5.882 | 6.481 | 6.333 | 6.762 | 5.882 | 6.481 | 6.333 | 6.762 | ns |
| | | GCLK PLL | $t_{co}$ | 4.322 | 4.322 | 6.468 | 6.731 | 7.392 | 7.212 | 7.755 | 6.731 | 7.392 | 7.212 | 7.755 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.635 | 3.635 | 5.401 | 5.621 | 6.195 | 6.047 | 6.476 | 5.621 | 6.195 | 6.047 | 6.476 | ns |
| | | GCLK PLL | $t_{co}$ | 4.200 | 4.200 | 6.243 | 6.471 | 7.107 | 6.927 | 7.470 | 6.471 | 7.107 | 6.927 | 7.470 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.597 | 3.597 | 5.308 | 5.531 | 6.082 | 5.934 | 6.363 | 5.531 | 6.082 | 5.934 | 6.363 | ns |
| | | GCLK PLL | $t_{co}$ | 4.162 | 4.162 | 6.150 | 6.381 | 6.993 | 6.813 | 7.356 | 6.381 | 6.993 | 6.813 | 7.356 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.550 | 3.550 | 5.280 | 5.482 | 6.026 | 5.878 | 6.307 | 5.482 | 6.026 | 5.878 | 6.307 | ns |
| | | GCLK PLL | $t_{co}$ | 4.113 | 4.113 | 6.121 | 6.331 | 6.946 | 6.766 | 7.309 | 6.331 | 6.946 | 6.766 | 7.309 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.550 | 3.550 | 5.237 | 5.430 | 5.957 | 5.809 | 6.238 | 5.430 | 5.957 | 5.809 | 6.238 | ns |
| | | GCLK PLL | $t_{co}$ | 4.114 | 4.114 | 6.078 | 6.278 | 6.903 | 6.723 | 7.266 | 6.278 | 6.903 | 6.723 | 7.266 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.547 | 3.547 | 5.234 | 5.426 | 5.953 | 5.805 | 6.234 | 5.426 | 5.953 | 5.805 | 6.234 | ns |
| | | GCLK PLL | $t_{co}$ | 4.111 | 4.111 | 6.075 | 6.274 | 6.899 | 6.720 | 7.261 | 6.274 | 6.899 | 6.720 | 7.261 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.545 | 3.545 | 5.234 | 5.427 | 5.954 | 5.806 | 6.235 | 5.427 | 5.954 | 5.806 | 6.235 | ns |
| | | GCLK PLL | $t_{co}$ | 4.110 | 4.110 | 6.075 | 6.275 | 6.899 | 6.719 | 7.262 | 6.275 | 6.899 | 6.719 | 7.262 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.536 | 3.536 | 5.220 | 5.412 | 5.939 | 5.791 | 6.220 | 5.412 | 5.939 | 5.791 | 6.220 | ns |
| | | GCLK PLL | $t_{co}$ | 4.101 | 4.101 | 6.062 | 6.261 | 6.883 | 6.703 | 7.246 | 6.261 | 6.883 | 6.703 | 7.246 | ns |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.557 | 3.557 | 5.249 | 5.444 | 5.973 | 5.825 | 6.254 | 5.444 | 5.973 | 5.825 | 6.254 | ns |
| | | GCLK PLL | $t_{co}$ | 4.121 | 4.121 | 6.090 | 6.292 | 6.923 | 6.744 | 7.285 | 6.292 | 6.923 | 6.744 | 7.285 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.553 | 3.553 | 5.247 | 5.442 | 5.971 | 5.823 | 6.252 | 5.442 | 5.971 | 5.823 | 6.252 | ns |
| | | GCLK PLL | $t_{co}$ | 4.117 | 4.117 | 6.088 | 6.290 | 6.920 | 6.740 | 7.283 | 6.290 | 6.920 | 6.740 | 7.283 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.542 | 3.542 | 5.237 | 5.432 | 5.962 | 5.814 | 6.243 | 5.432 | 5.962 | 5.814 | 6.243 | ns |
| | | GCLK PLL | $t_{co}$ | 4.107 | 4.107 | 6.079 | 6.281 | 6.919 | 6.740 | 7.281 | 6.281 | 6.919 | 6.740 | 7.281 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.531 | 3.531 | 5.225 | 5.419 | 5.949 | 5.801 | 6.230 | 5.419 | 5.949 | 5.801 | 6.230 | ns |
| | | GCLK PLL | $t_{co}$ | 4.095 | 4.095 | 6.066 | 6.268 | 6.894 | 6.715 | 7.256 | 6.268 | 6.894 | 6.715 | 7.256 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.531 | 3.531 | 5.224 | 5.419 | 5.949 | 5.801 | 6.230 | 5.419 | 5.949 | 5.801 | 6.230 | ns |
| | | GCLK PLL | $t_{co}$ | 4.095 | 4.095 | 6.066 | 6.268 | 6.892 | 6.712 | 7.255 | 6.268 | 6.892 | 6.712 | 7.255 | ns |

**Table 1–93.** EP3SL340 Column Pins Output Timing Parameters (Part 5 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.537 | 3.537 | 5.223 | 5.416 | 5.944 | 5.796 | 6.225 | 5.416 | 5.944 | 5.796 | 6.225 | ns |
| | | GCLK PLL | $t_{co}$ | 4.102 | 4.102 | 6.065 | 6.265 | 6.895 | 6.715 | 7.258 | 6.265 | 6.895 | 6.715 | 7.258 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.540 | 3.540 | 5.231 | 5.426 | 5.956 | 5.808 | 6.237 | 5.426 | 5.956 | 5.808 | 6.237 | ns |
| | | GCLK PLL | $t_{co}$ | 4.104 | 4.104 | 6.072 | 6.274 | 6.918 | 6.738 | 7.281 | 6.274 | 6.918 | 6.738 | 7.281 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.561 | 3.561 | 5.259 | 5.455 | 5.986 | 5.838 | 6.267 | 5.455 | 5.986 | 5.838 | 6.267 | ns |
| | | GCLK PLL | $t_{co}$ | 4.124 | 4.124 | 6.100 | 6.303 | 6.937 | 6.757 | 7.300 | 6.303 | 6.937 | 6.757 | 7.300 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.547 | 3.547 | 5.248 | 5.445 | 5.977 | 5.829 | 6.258 | 5.445 | 5.977 | 5.829 | 6.258 | ns |
| | | GCLK PLL | $t_{co}$ | 4.112 | 4.112 | 6.090 | 6.294 | 6.923 | 6.743 | 7.286 | 6.294 | 6.923 | 6.743 | 7.286 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.536 | 3.536 | 5.235 | 5.431 | 5.963 | 5.815 | 6.244 | 5.431 | 5.963 | 5.815 | 6.244 | ns |
| | | GCLK PLL | $t_{co}$ | 4.100 | 4.100 | 6.076 | 6.280 | 6.908 | 6.728 | 7.271 | 6.280 | 6.908 | 6.728 | 7.271 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.535 | 3.535 | 5.238 | 5.435 | 5.967 | 5.819 | 6.248 | 5.435 | 5.967 | 5.819 | 6.248 | ns |
| | | GCLK PLL | $t_{co}$ | 4.099 | 4.099 | 6.078 | 6.283 | 6.905 | 6.726 | 7.268 | 6.283 | 6.905 | 6.726 | 7.268 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.532 | 3.532 | 5.232 | 5.429 | 5.961 | 5.813 | 6.242 | 5.429 | 5.961 | 5.813 | 6.242 | ns |
| | | GCLK PLL | $t_{co}$ | 4.096 | 4.096 | 6.073 | 6.277 | 6.899 | 6.719 | 7.262 | 6.277 | 6.899 | 6.719 | 7.262 | ns |
| SSTL-15 CLASS II | 8mA | GCLK | $t_{co}$ | 3.534 | 3.534 | 5.221 | 5.415 | 5.944 | 5.796 | 6.225 | 5.415 | 5.944 | 5.796 | 6.225 | ns |
| | | GCLK PLL | $t_{co}$ | 4.098 | 4.098 | 6.063 | 6.264 | 6.896 | 6.716 | 7.259 | 6.264 | 6.896 | 6.716 | 7.259 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.537 | 3.537 | 5.228 | 5.424 | 5.955 | 5.807 | 6.236 | 5.424 | 5.955 | 5.807 | 6.236 | ns |
| | | GCLK PLL | $t_{co}$ | 4.101 | 4.101 | 6.070 | 6.272 | 6.920 | 6.740 | 7.283 | 6.272 | 6.920 | 6.740 | 7.283 | ns |


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**Table 1–93.** EP3SL340 Column Pins Output Timing Parameters (Part 6 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.544 | 3.544 | 5.223 | 5.415 | 5.942 | 5.794 | 6.223 | 5.415 | 5.942 | 5.794 | 6.223 | ns |
| | | GCLK PLL | $t_{co}$ | 4.108 | 4.108 | 6.064 | 6.263 | 6.897 | 6.717 | 7.260 | 6.263 | 6.897 | 6.717 | 7.260 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.537 | 3.537 | 5.221 | 5.414 | 5.941 | 5.793 | 6.222 | 5.414 | 5.941 | 5.793 | 6.222 | ns |
| | | GCLK PLL | $t_{co}$ | 4.102 | 4.102 | 6.063 | 6.263 | 6.903 | 6.724 | 7.265 | 6.263 | 6.903 | 6.724 | 7.265 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.529 | 3.529 | 5.214 | 5.406 | 5.934 | 5.786 | 6.215 | 5.406 | 5.934 | 5.786 | 6.215 | ns |
| | | GCLK PLL | $t_{co}$ | 4.094 | 4.094 | 6.055 | 6.255 | 6.885 | 6.706 | 7.247 | 6.255 | 6.885 | 6.706 | 7.247 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.532 | 3.532 | 5.217 | 5.410 | 5.938 | 5.790 | 6.219 | 5.410 | 5.938 | 5.790 | 6.219 | ns |
| | | GCLK PLL | $t_{co}$ | 4.096 | 4.096 | 6.058 | 6.258 | 6.887 | 6.707 | 7.250 | 6.258 | 6.887 | 6.707 | 7.250 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.529 | 3.529 | 5.219 | 5.413 | 5.942 | 5.794 | 6.223 | 5.413 | 5.942 | 5.794 | 6.223 | ns |
| | | GCLK PLL | $t_{co}$ | 4.093 | 4.093 | 6.060 | 6.261 | 6.895 | 6.716 | 7.257 | 6.261 | 6.895 | 6.716 | 7.257 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.537 | 3.537 | 5.218 | 5.411 | 5.938 | 5.790 | 6.219 | 5.411 | 5.938 | 5.790 | 6.219 | ns |
| | | GCLK PLL | $t_{co}$ | 4.101 | 4.101 | 6.059 | 6.259 | 6.898 | 6.718 | 7.261 | 6.259 | 6.898 | 6.718 | 7.261 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.549 | 3.549 | 5.232 | 5.425 | 5.953 | 5.805 | 6.234 | 5.425 | 5.953 | 5.805 | 6.234 | ns |
| | | GCLK PLL | $t_{co}$ | 4.113 | 4.113 | 6.072 | 6.273 | 6.910 | 6.730 | 7.273 | 6.273 | 6.910 | 6.730 | 7.273 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.545 | 3.545 | 5.233 | 5.427 | 5.956 | 5.808 | 6.237 | 5.427 | 5.956 | 5.808 | 6.237 | ns |
| | | GCLK PLL | $t_{co}$ | 4.109 | 4.109 | 6.075 | 6.276 | 6.907 | 6.727 | 7.270 | 6.276 | 6.907 | 6.727 | 7.270 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.541 | 3.541 | 5.228 | 5.422 | 5.951 | 5.803 | 6.232 | 5.422 | 5.951 | 5.803 | 6.232 | ns |
| | | GCLK PLL | $t_{co}$ | 4.105 | 4.105 | 6.070 | 6.271 | 6.902 | 6.722 | 7.265 | 6.271 | 6.902 | 6.722 | 7.265 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.534 | 3.534 | 5.221 | 5.415 | 5.944 | 5.796 | 6.225 | 5.415 | 5.944 | 5.796 | 6.225 | ns |
| | | GCLK PLL | $t_{co}$ | 4.098 | 4.098 | 6.063 | 6.264 | 6.896 | 6.716 | 7.259 | 6.264 | 6.896 | 6.716 | 7.259 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.535 | 3.535 | 5.228 | 5.423 | 5.954 | 5.806 | 6.235 | 5.423 | 5.954 | 5.806 | 6.235 | ns |
| | | GCLK PLL | $t_{co}$ | 4.098 | 4.098 | 6.069 | 6.271 | 6.900 | 6.721 | 7.262 | 6.271 | 6.900 | 6.721 | 7.262 | ns |
| 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.533 | 3.533 | 5.209 | 5.401 | 5.928 | 5.780 | 6.209 | 5.401 | 5.928 | 5.780 | 6.209 | ns |
| | | GCLK PLL | $t_{co}$ | 4.096 | 4.096 | 6.050 | 6.249 | 6.884 | 6.704 | 7.247 | 6.249 | 6.884 | 6.704 | 7.247 | ns |

**Table 1–93.** EP3SL340 Column Pins Output Timing Parameters (Part 7 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.552 | 3.552 | 5.246 | 5.442 | 5.974 | 5.826 | 6.255 | 5.442 | 5.974 | 5.826 | 6.255 | ns |
| | | GCLK PLL | $t_{co}$ | 4.117 | 4.117 | 6.087 | 6.291 | 6.929 | 6.749 | 7.292 | 6.291 | 6.929 | 6.749 | 7.292 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.544 | 3.544 | 5.237 | 5.433 | 5.965 | 5.817 | 6.246 | 5.433 | 5.965 | 5.817 | 6.246 | ns |
| | | GCLK PLL | $t_{co}$ | 4.108 | 4.108 | 6.078 | 6.282 | 6.917 | 6.737 | 7.280 | 6.282 | 6.917 | 6.737 | 7.280 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.545 | 3.545 | 5.244 | 5.442 | 5.974 | 5.826 | 6.255 | 5.442 | 5.974 | 5.826 | 6.255 | ns |
| | | GCLK PLL | $t_{co}$ | 4.108 | 4.108 | 6.085 | 6.290 | 6.920 | 6.740 | 7.283 | 6.290 | 6.920 | 6.740 | 7.283 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.534 | 3.534 | 5.231 | 5.428 | 5.960 | 5.812 | 6.241 | 5.428 | 5.960 | 5.812 | 6.241 | ns |
| | | GCLK PLL | $t_{co}$ | 4.098 | 4.098 | 6.072 | 6.276 | 6.915 | 6.736 | 7.277 | 6.276 | 6.915 | 6.736 | 7.277 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.534 | 3.534 | 5.231 | 5.428 | 5.961 | 5.813 | 6.242 | 5.428 | 5.961 | 5.813 | 6.242 | ns |
| | | GCLK PLL | $t_{co}$ | 4.098 | 4.098 | 6.073 | 6.277 | 6.906 | 6.727 | 7.269 | 6.277 | 6.906 | 6.727 | 7.269 | ns |
| 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.555 | 3.555 | 5.247 | 5.443 | 5.974 | 5.826 | 6.255 | 5.443 | 5.974 | 5.826 | 6.255 | ns |
| | | GCLK PLL | $t_{co}$ | 4.119 | 4.119 | 6.089 | 6.292 | 6.943 | 6.763 | 7.306 | 6.292 | 6.943 | 6.763 | 7.306 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.658 | 3.658 | 5.292 | 5.477 | 5.999 | 5.851 | 6.280 | 5.477 | 5.999 | 5.851 | 6.280 | ns |
| | | GCLK PLL | $t_{co}$ | 4.222 | 4.222 | 6.134 | 6.328 | 6.974 | 6.794 | 7.337 | 6.328 | 6.974 | 6.794 | 7.337 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.658 | 3.658 | 5.292 | 5.477 | 5.999 | 5.851 | 6.280 | 5.477 | 5.999 | 5.851 | 6.280 | ns |
| | | GCLK PLL | $t_{co}$ | 4.222 | 4.222 | 6.134 | 6.328 | 6.974 | 6.794 | 7.337 | 6.328 | 6.974 | 6.794 | 7.337 | ns |

Table 1–94 lists the EP3SL340 row pins output timing parameters for single-ended I/O standards.

**Table 1–94.** EP3SL340 Row Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.479 | 3.781 | 5.469 | 5.657 | 6.238 | 6.095 | 6.481 | 5.741 | 6.370 | 6.120 | 6.565 | ns |
| | | GCLK PLL | $t_{co}$ | 1.562 | 1.782 | 2.243 | 2.285 | 2.559 | 2.570 | 2.578 | 2.386 | 2.666 | 2.671 | 2.594 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.413 | 3.681 | 5.339 | 5.519 | 6.093 | 5.950 | 6.336 | 5.628 | 6.221 | 6.005 | 6.416 | ns |
| | | GCLK PLL | $t_{co}$ | 1.496 | 1.677 | 2.113 | 2.174 | 2.414 | 2.425 | 2.433 | 2.273 | 2.517 | 2.522 | 2.445 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.334 | 3.592 | 5.220 | 5.398 | 5.965 | 5.822 | 6.208 | 5.529 | 6.089 | 5.905 | 6.284 | ns |
| | | GCLK PLL | $t_{co}$ | 1.417 | 1.575 | 1.994 | 2.074 | 2.286 | 2.297 | 2.305 | 2.174 | 2.385 | 2.390 | 2.313 | ns |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.481 | 3.785 | 5.477 | 5.662 | 6.242 | 6.099 | 6.485 | 5.749 | 6.374 | 6.132 | 6.569 | ns |
| | | GCLK PLL | $t_{co}$ | 1.564 | 1.786 | 2.251 | 2.291 | 2.563 | 2.574 | 2.582 | 2.394 | 2.670 | 2.675 | 2.598 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.338 | 3.596 | 5.226 | 5.413 | 5.971 | 5.828 | 6.214 | 5.541 | 6.096 | 5.914 | 6.291 | ns |
| | | GCLK PLL | $t_{co}$ | 1.421 | 1.579 | 2.000 | 2.089 | 2.292 | 2.303 | 2.311 | 2.186 | 2.392 | 2.397 | 2.320 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.440 | 3.727 | 5.421 | 5.610 | 6.194 | 6.051 | 6.437 | 5.709 | 6.328 | 6.086 | 6.523 | ns |
| | | GCLK PLL | $t_{co}$ | 1.523 | 1.728 | 2.195 | 2.254 | 2.515 | 2.526 | 2.534 | 2.354 | 2.624 | 2.629 | 2.552 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.339 | 3.601 | 5.269 | 5.451 | 6.030 | 5.887 | 6.273 | 5.567 | 6.164 | 5.940 | 6.358 | ns |
| | | GCLK PLL | $t_{co}$ | 1.422 | 1.601 | 2.043 | 2.112 | 2.351 | 2.362 | 2.370 | 2.212 | 2.460 | 2.464 | 2.387 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.302 | 3.563 | 5.188 | 5.371 | 5.942 | 5.799 | 6.185 | 5.499 | 6.071 | 5.867 | 6.265 | ns |
| | | GCLK PLL | $t_{co}$ | 1.385 | 1.550 | 1.961 | 2.047 | 2.263 | 2.274 | 2.282 | 2.144 | 2.367 | 2.371 | 2.294 | ns |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.361 | 3.646 | 5.316 | 5.503 | 6.084 | 5.941 | 6.327 | 5.600 | 6.217 | 5.976 | 6.411 | ns |
| | | GCLK PLL | $t_{co}$ | 1.444 | 1.647 | 2.090 | 2.147 | 2.405 | 2.416 | 2.424 | 2.245 | 2.513 | 2.517 | 2.440 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.289 | 3.547 | 5.161 | 5.342 | 5.903 | 5.760 | 6.146 | 5.469 | 6.031 | 5.838 | 6.225 | ns |
| | | GCLK PLL | $t_{co}$ | 1.372 | 1.530 | 1.926 | 2.018 | 2.224 | 2.235 | 2.243 | 2.114 | 2.327 | 2.331 | 2.254 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.466 | 3.763 | 5.554 | 5.764 | 6.366 | 6.223 | 6.609 | 5.841 | 6.507 | 6.238 | 6.701 | ns |
| | | GCLK PLL | $t_{co}$ | 1.549 | 1.764 | 2.328 | 2.380 | 2.687 | 2.698 | 2.706 | 2.486 | 2.803 | 2.807 | 2.730 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.381 | 3.665 | 5.399 | 5.601 | 6.196 | 6.053 | 6.439 | 5.704 | 6.333 | 6.093 | 6.527 | ns |
| | | GCLK PLL | $t_{co}$ | 1.464 | 1.666 | 2.173 | 2.245 | 2.517 | 2.528 | 2.536 | 2.349 | 2.629 | 2.633 | 2.556 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.324 | 3.603 | 5.288 | 5.483 | 6.070 | 5.927 | 6.313 | 5.615 | 6.203 | 5.999 | 6.397 | ns |
| | | GCLK PLL | $t_{co}$ | 1.407 | 1.589 | 2.062 | 2.159 | 2.391 | 2.402 | 2.410 | 2.260 | 2.499 | 2.503 | 2.426 | ns |

**Table 1–94.** EP3SL340 Row Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.692 | 3.942 | 5.817 | 6.193 | 6.841 | 6.698 | 7.084 | 6.248 | 6.991 | 6.682 | 7.186 | ns |
| | | GCLK PLL | $t_{co}$ | 1.785 | 1.925 | 2.574 | 2.860 | 3.162 | 3.173 | 3.192 | 2.985 | 3.287 | 3.292 | 3.203 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.519 | 3.756 | 5.527 | 5.824 | 6.436 | 6.293 | 6.679 | 5.922 | 6.585 | 6.320 | 6.779 | ns |
| | | GCLK PLL | $t_{co}$ | 1.562 | 1.739 | 2.284 | 2.491 | 2.757 | 2.768 | 2.787 | 2.620 | 2.881 | 2.885 | 2.796 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.444 | 3.674 | 5.427 | 5.674 | 6.277 | 6.134 | 6.520 | 5.808 | 6.412 | 6.215 | 6.607 | ns |
| | | GCLK PLL | $t_{co}$ | 1.495 | 1.657 | 2.184 | 2.341 | 2.598 | 2.609 | 2.628 | 2.452 | 2.708 | 2.713 | 2.624 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.426 | 3.654 | 5.370 | 5.595 | 6.180 | 6.037 | 6.423 | 5.752 | 6.318 | 6.143 | 6.513 | ns |
| | | GCLK PLL | $t_{co}$ | 1.469 | 1.637 | 2.127 | 2.259 | 2.501 | 2.512 | 2.531 | 2.361 | 2.614 | 2.619 | 2.530 | ns |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.634 | 3.885 | 5.745 | 6.106 | 6.769 | 6.626 | 7.012 | 6.169 | 6.915 | 6.617 | 7.110 | ns |
| | | GCLK PLL | $t_{co}$ | 1.696 | 1.868 | 2.502 | 2.773 | 3.090 | 3.101 | 3.120 | 2.892 | 3.211 | 3.216 | 3.127 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.442 | 3.671 | 5.423 | 5.669 | 6.278 | 6.135 | 6.521 | 5.805 | 6.411 | 6.216 | 6.606 | ns |
| | | GCLK PLL | $t_{co}$ | 1.485 | 1.654 | 2.180 | 2.336 | 2.599 | 2.610 | 2.629 | 2.446 | 2.707 | 2.712 | 2.623 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.415 | 3.645 | 5.355 | 5.587 | 6.172 | 6.029 | 6.415 | 5.745 | 6.306 | 6.143 | 6.501 | ns |
| | | GCLK PLL | $t_{co}$ | 1.458 | 1.628 | 2.112 | 2.251 | 2.493 | 2.504 | 2.523 | 2.354 | 2.602 | 2.607 | 2.518 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.396 | 3.634 | 5.338 | 5.562 | 6.153 | 6.010 | 6.396 | 5.721 | 6.284 | 6.124 | 6.479 | ns |
| | | GCLK PLL | $t_{co}$ | 1.439 | 1.617 | 2.095 | 2.226 | 2.474 | 2.485 | 2.504 | 2.330 | 2.580 | 2.585 | 2.496 | ns |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.564 | 3.798 | 5.666 | 6.020 | 6.694 | 6.551 | 6.937 | 6.100 | 6.831 | 6.548 | 7.026 | ns |
| | | GCLK PLL | $t_{co}$ | 1.639 | 1.781 | 2.423 | 2.687 | 3.015 | 3.026 | 3.045 | 2.804 | 3.127 | 3.132 | 3.043 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.447 | 3.675 | 5.440 | 5.697 | 6.319 | 6.176 | 6.562 | 5.834 | 6.453 | 6.260 | 6.648 | ns |
| | | GCLK PLL | $t_{co}$ | 1.490 | 1.658 | 2.197 | 2.364 | 2.640 | 2.651 | 2.670 | 2.471 | 2.749 | 2.754 | 2.665 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.328 | 3.591 | 5.278 | 5.474 | 6.038 | 5.895 | 6.281 | 5.602 | 6.165 | 5.985 | 6.360 | ns |
| | | GCLK PLL | $t_{co}$ | 1.411 | 1.575 | 2.039 | 2.150 | 2.359 | 2.370 | 2.378 | 2.247 | 2.461 | 2.466 | 2.389 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.323 | 3.587 | 5.275 | 5.472 | 6.030 | 5.887 | 6.273 | 5.601 | 6.158 | 5.984 | 6.353 | ns |
| | | GCLK PLL | $t_{co}$ | 1.406 | 1.570 | 2.032 | 2.148 | 2.351 | 2.362 | 2.370 | 2.246 | 2.454 | 2.459 | 2.382 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.314 | 3.576 | 5.260 | 5.456 | 6.003 | 5.860 | 6.246 | 5.584 | 6.131 | 5.966 | 6.326 | ns |
| | | GCLK PLL | $t_{co}$ | 1.397 | 1.559 | 2.017 | 2.132 | 2.324 | 2.335 | 2.343 | 2.229 | 2.427 | 2.432 | 2.355 | ns |

**Table 1–94.** EP3SL340 Row Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.375 | 3.598 | 5.289 | 5.499 | 6.054 | 5.911 | 6.297 | 5.651 | 6.181 | 6.034 | 6.376 | ns |
| | | GCLK PLL | $t_{co}$ | 1.418 | 1.581 | 2.046 | 2.163 | 2.375 | 2.386 | 2.405 | 2.260 | 2.477 | 2.482 | 2.393 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.370 | 3.593 | 5.287 | 5.498 | 6.052 | 5.909 | 6.295 | 5.649 | 6.179 | 6.032 | 6.374 | ns |
| | | GCLK PLL | $t_{co}$ | 1.413 | 1.576 | 2.044 | 2.162 | 2.373 | 2.384 | 2.403 | 2.258 | 2.475 | 2.480 | 2.391 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.359 | 3.582 | 5.277 | 5.488 | 6.035 | 5.895 | 6.278 | 5.640 | 6.163 | 6.023 | 6.358 | ns |
| | | GCLK PLL | $t_{co}$ | 1.402 | 1.565 | 2.034 | 2.152 | 2.356 | 2.367 | 2.386 | 2.249 | 2.459 | 2.464 | 2.375 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.348 | 3.571 | 5.264 | 5.475 | 6.020 | 5.882 | 6.263 | 5.628 | 6.148 | 6.011 | 6.343 | ns |
| | | GCLK PLL | $t_{co}$ | 1.391 | 1.554 | 2.021 | 2.139 | 2.341 | 2.352 | 2.371 | 2.237 | 2.444 | 2.449 | 2.360 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.348 | 3.570 | 5.264 | 5.475 | 6.019 | 5.882 | 6.262 | 5.627 | 6.147 | 6.011 | 6.342 | ns |
| | | GCLK PLL | $t_{co}$ | 1.391 | 1.553 | 2.021 | 2.139 | 2.340 | 2.351 | 2.370 | 2.236 | 2.443 | 2.448 | 2.359 | ns |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.356 | 3.577 | 5.263 | 5.472 | 6.013 | 5.877 | 6.256 | 5.623 | 6.140 | 6.005 | 6.335 | ns |
| | | GCLK PLL | $t_{co}$ | 1.399 | 1.560 | 2.020 | 2.136 | 2.334 | 2.345 | 2.364 | 2.232 | 2.436 | 2.441 | 2.352 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.357 | 3.580 | 5.269 | 5.480 | 6.015 | 5.887 | 6.258 | 5.632 | 6.144 | 6.016 | 6.339 | ns |
| | | GCLK PLL | $t_{co}$ | 1.400 | 1.563 | 2.026 | 2.144 | 2.336 | 2.347 | 2.366 | 2.241 | 2.440 | 2.445 | 2.356 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.378 | 3.601 | 5.298 | 5.510 | 6.071 | 5.928 | 6.314 | 5.661 | 6.197 | 6.046 | 6.392 | ns |
| | | GCLK PLL | $t_{co}$ | 1.421 | 1.584 | 2.055 | 2.174 | 2.392 | 2.403 | 2.422 | 2.270 | 2.493 | 2.498 | 2.409 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.364 | 3.587 | 5.287 | 5.500 | 6.054 | 5.911 | 6.297 | 5.652 | 6.181 | 6.037 | 6.376 | ns |
| | | GCLK PLL | $t_{co}$ | 1.407 | 1.570 | 2.044 | 2.164 | 2.375 | 2.386 | 2.405 | 2.261 | 2.477 | 2.482 | 2.393 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.353 | 3.575 | 5.274 | 5.487 | 6.036 | 5.896 | 6.279 | 5.639 | 6.164 | 6.024 | 6.359 | ns |
| | | GCLK PLL | $t_{co}$ | 1.396 | 1.558 | 2.031 | 2.151 | 2.357 | 2.368 | 2.387 | 2.248 | 2.460 | 2.465 | 2.376 | ns |

**Table 1–94.** EP3SL340 Row Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.363 | 3.583 | 5.262 | 5.470 | 6.016 | 5.875 | 6.259 | 5.622 | 6.143 | 6.002 | 6.338 | ns |
| | | GCLK PLL | $t_{co}$ | 1.406 | 1.566 | 2.019 | 2.134 | 2.337 | 2.348 | 2.367 | 2.231 | 2.439 | 2.444 | 2.355 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.356 | 3.577 | 5.260 | 5.469 | 6.008 | 5.874 | 6.251 | 5.621 | 6.136 | 6.002 | 6.331 | ns |
| | | GCLK PLL | $t_{co}$ | 1.399 | 1.560 | 2.017 | 2.133 | 2.329 | 2.340 | 2.359 | 2.230 | 2.432 | 2.437 | 2.348 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.347 | 3.569 | 5.253 | 5.462 | 6.000 | 5.867 | 6.243 | 5.614 | 6.128 | 5.995 | 6.323 | ns |
| | | GCLK PLL | $t_{co}$ | 1.390 | 1.552 | 2.010 | 2.126 | 2.321 | 2.332 | 2.351 | 2.223 | 2.424 | 2.429 | 2.340 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.350 | 3.571 | 5.256 | 5.465 | 6.003 | 5.871 | 6.246 | 5.617 | 6.131 | 5.998 | 6.326 | ns |
| | | GCLK PLL | $t_{co}$ | 1.393 | 1.554 | 2.013 | 2.129 | 2.324 | 2.335 | 2.354 | 2.226 | 2.427 | 2.432 | 2.343 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.346 | 3.568 | 5.258 | 5.468 | 6.003 | 5.874 | 6.246 | 5.620 | 6.132 | 6.003 | 6.327 | ns |
| | | GCLK PLL | $t_{co}$ | 1.389 | 1.551 | 2.015 | 2.132 | 2.324 | 2.335 | 2.354 | 2.229 | 2.428 | 2.433 | 2.344 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.354 | 3.576 | 5.256 | 5.465 | 5.994 | 5.870 | 6.237 | 5.616 | 6.121 | 5.997 | 6.316 | ns |
| | | GCLK PLL | $t_{co}$ | 1.397 | 1.559 | 2.013 | 2.129 | 2.315 | 2.326 | 2.345 | 2.225 | 2.417 | 2.422 | 2.333 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.369 | 3.589 | 5.271 | 5.480 | 6.031 | 5.888 | 6.274 | 5.631 | 6.157 | 6.013 | 6.352 | ns |
| | | GCLK PLL | $t_{co}$ | 1.412 | 1.572 | 2.028 | 2.144 | 2.352 | 2.363 | 2.382 | 2.240 | 2.453 | 2.458 | 2.369 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.363 | 3.584 | 5.272 | 5.482 | 6.027 | 5.888 | 6.270 | 5.633 | 6.154 | 6.016 | 6.349 | ns |
| | | GCLK PLL | $t_{co}$ | 1.406 | 1.567 | 2.029 | 2.146 | 2.348 | 2.359 | 2.378 | 2.242 | 2.450 | 2.455 | 2.366 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.359 | 3.580 | 5.267 | 5.477 | 6.021 | 5.883 | 6.264 | 5.628 | 6.148 | 6.010 | 6.343 | ns |
| | | GCLK PLL | $t_{co}$ | 1.402 | 1.563 | 2.024 | 2.141 | 2.342 | 2.353 | 2.372 | 2.237 | 2.444 | 2.449 | 2.360 | ns |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.371 | 3.591 | 5.284 | 5.496 | 6.049 | 5.906 | 6.292 | 5.647 | 6.174 | 6.032 | 6.369 | ns |
| | | GCLK PLL | $t_{co}$ | 1.414 | 1.574 | 2.041 | 2.160 | 2.370 | 2.381 | 2.400 | 2.256 | 2.470 | 2.475 | 2.386 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.362 | 3.583 | 5.275 | 5.487 | 6.037 | 5.896 | 6.280 | 5.638 | 6.163 | 6.023 | 6.358 | ns |
| | | GCLK PLL | $t_{co}$ | 1.405 | 1.566 | 2.032 | 2.151 | 2.358 | 2.369 | 2.388 | 2.247 | 2.459 | 2.464 | 2.375 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.361 | 3.583 | 5.282 | 5.495 | 6.043 | 5.905 | 6.286 | 5.647 | 6.170 | 6.033 | 6.365 | ns |
| | | GCLK PLL | $t_{co}$ | 1.404 | 1.566 | 2.039 | 2.159 | 2.364 | 2.375 | 2.394 | 2.256 | 2.466 | 2.471 | 2.382 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.434 | 3.697 | 5.330 | 5.520 | 6.047 | 5.904 | 6.299 | 5.650 | 6.177 | 6.027 | 6.372 | ns |
| | | GCLK PLL | $t_{co}$ | 1.517 | 1.680 | 2.087 | 2.196 | 2.378 | 2.386 | 2.387 | 2.295 | 2.482 | 2.493 | 2.401 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.434 | 3.697 | 5.330 | 5.520 | 6.047 | 5.904 | 6.299 | 5.650 | 6.177 | 6.027 | 6.372 | ns |
| | | GCLK PLL | $t_{co}$ | 1.517 | 1.680 | 2.087 | 2.196 | 2.378 | 2.386 | 2.387 | 2.295 | 2.482 | 2.493 | 2.401 | ns |


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Table 1–95 through Table 1–98 list the maximum I/O timing parameters for EP3SL340 devices for differential I/O standards.

Table 1–95 lists the EP3SL340 column pins input timing parameters for differential I/O standards.

**Table 1–95.** EP3SL340 Column Pins Input Timing Parameters (Part 1 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -1.278 | -1.335 | -1.674 | -1.607 | -1.788 | -1.721 | -2.204 | -1.580 | -2.013 | -1.689 | -2.242 | ns |
| | | $t_h$ | 1.414 | 1.489 | 1.926 | 1.873 | 2.080 | 2.002 | 2.485 | 1.857 | 2.327 | 1.981 | 2.527 | ns |
| | GCLK PLL | $t_{su}$ | 0.857 | 0.885 | 1.872 | 2.050 | 2.211 | 2.107 | 1.975 | 2.104 | 2.409 | 2.165 | 2.031 | ns |
| | | $t_h$ | -0.582 | -0.589 | -1.382 | -1.537 | -1.640 | -1.565 | -1.423 | -1.579 | -1.804 | -1.612 | -1.474 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -1.278 | -1.335 | -1.674 | -1.607 | -1.788 | -1.721 | -2.204 | -1.580 | -2.013 | -1.689 | -2.242 | ns |
| | | $t_h$ | 1.414 | 1.489 | 1.926 | 1.873 | 2.080 | 2.002 | 2.485 | 1.857 | 2.327 | 1.981 | 2.527 | ns |
| | GCLK PLL | $t_{su}$ | 0.857 | 0.885 | 1.872 | 2.050 | 2.211 | 2.107 | 1.975 | 2.104 | 2.409 | 2.165 | 2.031 | ns |
| | | $t_h$ | -0.582 | -0.589 | -1.382 | -1.537 | -1.640 | -1.565 | -1.423 | -1.579 | -1.804 | -1.612 | -1.474 | ns |
| RSDS | GCLK | $t_{su}$ | -1.278 | -1.335 | -1.674 | -1.607 | -1.788 | -1.721 | -2.204 | -1.580 | -2.013 | -1.689 | -2.242 | ns |
| | | $t_h$ | 1.414 | 1.489 | 1.926 | 1.873 | 2.080 | 2.002 | 2.485 | 1.857 | 2.327 | 1.981 | 2.527 | ns |
| | GCLK PLL | $t_{su}$ | 0.857 | 0.885 | 1.872 | 2.050 | 2.211 | 2.107 | 1.975 | 2.104 | 2.409 | 2.165 | 2.031 | ns |
| | | $t_h$ | -0.582 | -0.589 | -1.382 | -1.537 | -1.640 | -1.565 | -1.423 | -1.579 | -1.804 | -1.612 | -1.474 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -1.094 | -1.158 | -1.787 | -1.806 | -1.947 | -1.875 | -2.353 | -1.815 | -1.953 | -1.887 | -2.396 | ns |
| | | $t_h$ | 1.223 | 1.304 | 2.006 | 2.032 | 2.193 | 2.110 | 2.589 | 2.050 | 2.208 | 2.131 | 2.636 | ns |
| | GCLK PLL | $t_{su}$ | 1.041 | 1.062 | 1.759 | 1.851 | 2.052 | 1.953 | 1.826 | 1.869 | 2.073 | 1.967 | 1.877 | ns |
| | | $t_h$ | -0.773 | -0.774 | -1.302 | -1.378 | -1.527 | -1.457 | -1.319 | -1.386 | -1.537 | -1.462 | -1.365 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -1.094 | -1.158 | -1.787 | -1.806 | -1.947 | -1.875 | -2.353 | -1.815 | -1.953 | -1.887 | -2.396 | ns |
| | | $t_h$ | 1.223 | 1.304 | 2.006 | 2.032 | 2.193 | 2.110 | 2.589 | 2.050 | 2.208 | 2.131 | 2.636 | ns |
| | GCLK PLL | $t_{su}$ | 1.041 | 1.062 | 1.759 | 1.851 | 2.052 | 1.953 | 1.826 | 1.869 | 2.073 | 1.967 | 1.877 | ns |
| | | $t_h$ | -0.773 | -0.774 | -1.302 | -1.378 | -1.527 | -1.457 | -1.319 | -1.386 | -1.537 | -1.462 | -1.365 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -1.102 | -1.170 | -1.797 | -1.817 | -1.963 | -1.891 | -2.369 | -1.826 | -1.968 | -1.902 | -2.411 | ns |
| | | $t_h$ | 1.231 | 1.316 | 2.016 | 2.043 | 2.209 | 2.126 | 2.605 | 2.061 | 2.223 | 2.146 | 2.651 | ns |
| | GCLK PLL | $t_{su}$ | 1.033 | 1.050 | 1.749 | 1.840 | 2.036 | 1.937 | 1.810 | 1.858 | 2.058 | 1.952 | 1.862 | ns |
| | | $t_h$ | -0.765 | -0.762 | -1.292 | -1.367 | -1.511 | -1.441 | -1.303 | -1.375 | -1.522 | -1.447 | -1.350 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -1.102 | -1.170 | -1.797 | -1.817 | -1.963 | -1.891 | -2.369 | -1.826 | -1.968 | -1.902 | -2.411 | ns |
| | | $t_h$ | 1.231 | 1.316 | 2.016 | 2.043 | 2.209 | 2.126 | 2.605 | 2.061 | 2.223 | 2.146 | 2.651 | ns |
| | GCLK PLL | $t_{su}$ | 1.033 | 1.050 | 1.749 | 1.840 | 2.036 | 1.937 | 1.810 | 1.858 | 2.058 | 1.952 | 1.862 | ns |
| | | $t_h$ | -0.765 | -0.762 | -1.292 | -1.367 | -1.511 | -1.441 | -1.303 | -1.375 | -1.522 | -1.447 | -1.350 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -1.114 | -1.181 | -1.806 | -1.828 | -1.982 | -1.910 | -2.388 | -1.837 | -1.986 | -1.920 | -2.429 | ns |
| | | $t_h$ | 1.243 | 1.327 | 2.025 | 2.054 | 2.228 | 2.145 | 2.624 | 2.072 | 2.241 | 2.164 | 2.669 | ns |
| | GCLK PLL | $t_{su}$ | 1.021 | 1.039 | 1.740 | 1.829 | 2.017 | 1.918 | 1.791 | 1.847 | 2.040 | 1.934 | 1.844 | ns |
| | | $t_h$ | -0.753 | -0.751 | -1.283 | -1.356 | -1.492 | -1.422 | -1.284 | -1.364 | -1.504 | -1.429 | -1.332 | ns |

**Table 1–95.** EP3SL340 Column Pins Input Timing Parameters (Part 2 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -1.114 | -1.181 | -1.806 | -1.828 | -1.982 | -1.910 | -2.388 | -1.837 | -1.986 | -1.920 | -2.429 | ns |
| | | $t_h$ | 1.243 | 1.327 | 2.025 | 2.054 | 2.228 | 2.145 | 2.624 | 2.072 | 2.241 | 2.164 | 2.669 | ns |
| | GCLK PLL | $t_{su}$ | 1.021 | 1.039 | 1.740 | 1.829 | 2.017 | 1.918 | 1.791 | 1.847 | 2.040 | 1.934 | 1.844 | ns |
| | | $t_h$ | -0.753 | -0.751 | -1.283 | -1.356 | -1.492 | -1.422 | -1.284 | -1.364 | -1.504 | -1.429 | -1.332 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -1.102 | -1.170 | -1.797 | -1.817 | -1.963 | -1.891 | -2.369 | -1.826 | -1.968 | -1.902 | -2.411 | ns |
| | | $t_h$ | 1.231 | 1.316 | 2.016 | 2.043 | 2.209 | 2.126 | 2.605 | 2.061 | 2.223 | 2.146 | 2.651 | ns |
| | GCLK PLL | $t_{su}$ | 1.033 | 1.050 | 1.749 | 1.840 | 2.036 | 1.937 | 1.810 | 1.858 | 2.058 | 1.952 | 1.862 | ns |
| | | $t_h$ | -0.765 | -0.762 | -1.292 | -1.367 | -1.511 | -1.441 | -1.303 | -1.375 | -1.522 | -1.447 | -1.350 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -1.102 | -1.170 | -1.797 | -1.817 | -1.963 | -1.891 | -2.369 | -1.826 | -1.968 | -1.902 | -2.411 | ns |
| | | $t_h$ | 1.231 | 1.316 | 2.016 | 2.043 | 2.209 | 2.126 | 2.605 | 2.061 | 2.223 | 2.146 | 2.651 | ns |
| | GCLK PLL | $t_{su}$ | 1.033 | 1.050 | 1.749 | 1.840 | 2.036 | 1.937 | 1.810 | 1.858 | 2.058 | 1.952 | 1.862 | ns |
| | | $t_h$ | -0.765 | -0.762 | -1.292 | -1.367 | -1.511 | -1.441 | -1.303 | -1.375 | -1.522 | -1.447 | -1.350 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -1.114 | -1.181 | -1.806 | -1.828 | -1.982 | -1.910 | -2.388 | -1.837 | -1.986 | -1.920 | -2.429 | ns |
| | | $t_h$ | 1.243 | 1.327 | 2.025 | 2.054 | 2.228 | 2.145 | 2.624 | 2.072 | 2.241 | 2.164 | 2.669 | ns |
| | GCLK PLL | $t_{su}$ | 1.021 | 1.039 | 1.740 | 1.829 | 2.017 | 1.918 | 1.791 | 1.847 | 2.040 | 1.934 | 1.844 | ns |
| | | $t_h$ | -0.753 | -0.751 | -1.283 | -1.356 | -1.492 | -1.422 | -1.284 | -1.364 | -1.504 | -1.429 | -1.332 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -1.114 | -1.181 | -1.806 | -1.828 | -1.982 | -1.910 | -2.388 | -1.837 | -1.986 | -1.920 | -2.429 | ns |
| | | $t_h$ | 1.243 | 1.327 | 2.025 | 2.054 | 2.228 | 2.145 | 2.624 | 2.072 | 2.241 | 2.164 | 2.669 | ns |
| | GCLK PLL | $t_{su}$ | 1.021 | 1.039 | 1.740 | 1.829 | 2.017 | 1.918 | 1.791 | 1.847 | 2.040 | 1.934 | 1.844 | ns |
| | | $t_h$ | -0.753 | -0.751 | -1.283 | -1.356 | -1.492 | -1.422 | -1.284 | -1.364 | -1.504 | -1.429 | -1.332 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -1.121 | -1.187 | -1.818 | -1.833 | -1.982 | -1.912 | -2.387 | -1.841 | -1.981 | -1.918 | -2.425 | ns |
| | | $t_h$ | 1.250 | 1.333 | 2.038 | 2.062 | 2.231 | 2.148 | 2.628 | 2.079 | 2.241 | 2.163 | 2.670 | ns |
| | GCLK PLL | $t_{su}$ | 1.014 | 1.033 | 1.728 | 1.824 | 2.017 | 1.916 | 1.792 | 1.843 | 2.045 | 1.936 | 1.848 | ns |
| | | $t_h$ | -0.746 | -0.745 | -1.270 | -1.348 | -1.489 | -1.419 | -1.280 | -1.357 | -1.504 | -1.430 | -1.331 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -1.121 | -1.187 | -1.818 | -1.833 | -1.982 | -1.912 | -2.387 | -1.841 | -1.981 | -1.918 | -2.425 | ns |
| | | $t_h$ | 1.250 | 1.333 | 2.038 | 2.062 | 2.231 | 2.148 | 2.628 | 2.079 | 2.241 | 2.163 | 2.670 | ns |
| | GCLK PLL | $t_{su}$ | 1.014 | 1.033 | 1.728 | 1.824 | 2.017 | 1.916 | 1.792 | 1.843 | 2.045 | 1.936 | 1.848 | ns |
| | | $t_h$ | -0.746 | -0.745 | -1.270 | -1.348 | -1.489 | -1.419 | -1.280 | -1.357 | -1.504 | -1.430 | -1.331 | ns |

Table 1–96 lists the EP3SL340 row pins input timing parameters for differential I/O standards.

**Table 1–96.** EP3SL340 Row Pins Input Timing Parameters (Part 1 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -1.246 | -1.308 | -1.577 | -1.488 | -1.656 | -1.595 | -2.046 | -1.456 | -1.615 | -1.558 | -2.087 | ns |
| | | $t_h$ | 1.380 | 1.458 | 1.832 | 1.758 | 1.950 | 1.878 | 2.332 | 1.738 | 1.920 | 1.853 | 2.374 | ns |
| | GCLK PLL | $t_{su}$ | 0.822 | 0.846 | 1.911 | 2.121 | 2.309 | 2.193 | 2.091 | 2.181 | 2.377 | 2.260 | 2.149 | ns |
| | | $t_h$ | -0.548 | -0.552 | -1.422 | -1.604 | -1.736 | -1.650 | -1.536 | -1.651 | -1.790 | -1.702 | -1.588 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -1.246 | -1.308 | -1.577 | -1.488 | -1.656 | -1.595 | -2.046 | -1.456 | -1.615 | -1.558 | -2.087 | ns |
| | | $t_h$ | 1.380 | 1.458 | 1.832 | 1.758 | 1.950 | 1.878 | 2.332 | 1.738 | 1.920 | 1.853 | 2.374 | ns |
| | GCLK PLL | $t_{su}$ | 0.822 | 0.846 | 1.911 | 2.121 | 2.309 | 2.193 | 2.091 | 2.181 | 2.377 | 2.260 | 2.149 | ns |
| | | $t_h$ | -0.548 | -0.552 | -1.422 | -1.604 | -1.736 | -1.650 | -1.536 | -1.651 | -1.790 | -1.702 | -1.588 | ns |
| RSDS | GCLK | $t_{su}$ | -1.246 | -1.308 | -1.577 | -1.488 | -1.656 | -1.595 | -2.046 | -1.456 | -1.615 | -1.558 | -2.087 | ns |
| | | $t_h$ | 1.380 | 1.458 | 1.832 | 1.758 | 1.950 | 1.878 | 2.332 | 1.738 | 1.920 | 1.853 | 2.374 | ns |
| | GCLK PLL | $t_{su}$ | 0.822 | 0.846 | 1.911 | 2.121 | 2.309 | 2.193 | 2.091 | 2.181 | 2.377 | 2.260 | 2.149 | ns |
| | | $t_h$ | -0.548 | -0.552 | -1.422 | -1.604 | -1.736 | -1.650 | -1.536 | -1.651 | -1.790 | -1.702 | -1.588 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -1.051 | -1.123 | -1.707 | -1.717 | -1.845 | -1.779 | -2.225 | -1.727 | -1.852 | -1.790 | -2.271 | ns |
| | | $t_h$ | 1.178 | 1.264 | 1.926 | 1.941 | 2.090 | 2.013 | 2.462 | 1.960 | 2.105 | 2.033 | 2.509 | ns |
| | GCLK PLL | $t_{su}$ | 1.007 | 1.021 | 1.776 | 1.887 | 2.110 | 1.999 | 1.902 | 1.904 | 2.130 | 2.018 | 1.955 | ns |
| | | $t_h$ | -0.740 | -0.736 | -1.321 | -1.415 | -1.586 | -1.505 | -1.396 | -1.423 | -1.595 | -1.512 | -1.443 | ns |
| | GCLK | $t_{su}$ | -1.051 | -1.123 | -1.707 | -1.717 | -1.845 | -1.779 | -2.225 | -1.727 | -1.852 | -1.790 | -2.271 | ns |
| | | $t_h$ | 1.178 | 1.264 | 1.926 | 1.941 | 2.090 | 2.013 | 2.462 | 1.960 | 2.105 | 2.033 | 2.509 | ns |
| | GCLK PLL | $t_{su}$ | 1.007 | 1.021 | 1.776 | 1.887 | 2.110 | 1.999 | 1.902 | 1.904 | 2.130 | 2.018 | 1.955 | ns |
| | | $t_h$ | -0.740 | -0.736 | -1.321 | -1.415 | -1.586 | -1.505 | -1.396 | -1.423 | -1.595 | -1.512 | -1.443 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -1.060 | -1.135 | -1.716 | -1.727 | -1.861 | -1.795 | -2.241 | -1.736 | -1.868 | -1.806 | -2.287 | ns |
| | | $t_h$ | 1.187 | 1.276 | 1.935 | 1.951 | 2.106 | 2.029 | 2.478 | 1.969 | 2.121 | 2.049 | 2.525 | ns |
| | GCLK PLL | $t_{su}$ | 0.998 | 1.009 | 1.767 | 1.877 | 2.094 | 1.983 | 1.886 | 1.895 | 2.114 | 2.002 | 1.939 | ns |
| | | $t_h$ | -0.731 | -0.724 | -1.312 | -1.405 | -1.570 | -1.489 | -1.380 | -1.414 | -1.579 | -1.496 | -1.427 | ns |
| | GCLK | $t_{su}$ | -1.060 | -1.135 | -1.716 | -1.727 | -1.861 | -1.795 | -2.241 | -1.736 | -1.868 | -1.806 | -2.287 | ns |
| | | $t_h$ | 1.187 | 1.276 | 1.935 | 1.951 | 2.106 | 2.029 | 2.478 | 1.969 | 2.121 | 2.049 | 2.525 | ns |
| | GCLK PLL | $t_{su}$ | 0.998 | 1.009 | 1.767 | 1.877 | 2.094 | 1.983 | 1.886 | 1.895 | 2.114 | 2.002 | 1.939 | ns |
| | | $t_h$ | -0.731 | -0.724 | -1.312 | -1.405 | -1.570 | -1.489 | -1.380 | -1.414 | -1.579 | -1.496 | -1.427 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -1.074 | -1.147 | -1.725 | -1.737 | -1.879 | -1.813 | -2.259 | -1.747 | -1.885 | -1.823 | -2.304 | ns |
| | | $t_h$ | 1.201 | 1.288 | 1.944 | 1.961 | 2.124 | 2.047 | 2.496 | 1.980 | 2.138 | 2.066 | 2.542 | ns |
| | GCLK PLL | $t_{su}$ | 0.984 | 0.997 | 1.754 | 1.867 | 2.076 | 1.965 | 1.868 | 1.884 | 2.097 | 1.985 | 1.922 | ns |
| | | $t_h$ | -0.717 | -0.712 | -1.300 | -1.395 | -1.552 | -1.471 | -1.362 | -1.403 | -1.562 | -1.479 | -1.410 | ns |

**Table 1–96.** EP3SL340 Row Pins Input Timing Parameters (Part 2 of 2)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -1.074 | -1.147 | -1.725 | -1.737 | -1.879 | -1.813 | -2.259 | -1.747 | -1.885 | -1.823 | -2.304 | ns |
| | | $t_h$ | 1.201 | 1.288 | 1.944 | 1.961 | 2.124 | 2.047 | 2.496 | 1.980 | 2.138 | 2.066 | 2.542 | ns |
| | GCLK PLL | $t_{su}$ | 0.984 | 0.997 | 1.754 | 1.867 | 2.076 | 1.965 | 1.868 | 1.884 | 2.097 | 1.985 | 1.922 | ns |
| | | $t_h$ | -0.717 | -0.712 | -1.300 | -1.395 | -1.552 | -1.471 | -1.362 | -1.403 | -1.562 | -1.479 | -1.410 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -1.060 | -1.135 | -1.716 | -1.727 | -1.861 | -1.795 | -2.241 | -1.736 | -1.868 | -1.806 | -2.287 | ns |
| | | $t_h$ | 1.187 | 1.276 | 1.935 | 1.951 | 2.106 | 2.029 | 2.478 | 1.969 | 2.121 | 2.049 | 2.525 | ns |
| | GCLK PLL | $t_{su}$ | 0.998 | 1.009 | 1.767 | 1.877 | 2.094 | 1.983 | 1.886 | 1.895 | 2.114 | 2.002 | 1.939 | ns |
| | | $t_h$ | -0.731 | -0.724 | -1.312 | -1.405 | -1.570 | -1.489 | -1.380 | -1.414 | -1.579 | -1.496 | -1.427 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -1.060 | -1.135 | -1.716 | -1.727 | -1.861 | -1.795 | -2.241 | -1.736 | -1.868 | -1.806 | -2.287 | ns |
| | | $t_h$ | 1.187 | 1.276 | 1.935 | 1.951 | 2.106 | 2.029 | 2.478 | 1.969 | 2.121 | 2.049 | 2.525 | ns |
| | GCLK PLL | $t_{su}$ | 0.998 | 1.009 | 1.767 | 1.877 | 2.094 | 1.983 | 1.886 | 1.895 | 2.114 | 2.002 | 1.939 | ns |
| | | $t_h$ | -0.731 | -0.724 | -1.312 | -1.405 | -1.570 | -1.489 | -1.380 | -1.414 | -1.579 | -1.496 | -1.427 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -1.074 | -1.147 | -1.725 | -1.737 | -1.879 | -1.813 | -2.259 | -1.747 | -1.885 | -1.823 | -2.304 | ns |
| | | $t_h$ | 1.201 | 1.288 | 1.944 | 1.961 | 2.124 | 2.047 | 2.496 | 1.980 | 2.138 | 2.066 | 2.542 | ns |
| | GCLK PLL | $t_{su}$ | 0.984 | 0.997 | 1.754 | 1.867 | 2.076 | 1.965 | 1.868 | 1.884 | 2.097 | 1.985 | 1.922 | ns |
| | | $t_h$ | -0.717 | -0.712 | -1.300 | -1.395 | -1.552 | -1.471 | -1.362 | -1.403 | -1.562 | -1.479 | -1.410 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -1.074 | -1.147 | -1.725 | -1.737 | -1.879 | -1.813 | -2.259 | -1.747 | -1.885 | -1.823 | -2.304 | ns |
| | | $t_h$ | 1.201 | 1.288 | 1.944 | 1.961 | 2.124 | 2.047 | 2.496 | 1.980 | 2.138 | 2.066 | 2.542 | ns |
| | GCLK PLL | $t_{su}$ | 0.984 | 0.997 | 1.754 | 1.867 | 2.076 | 1.965 | 1.868 | 1.884 | 2.097 | 1.985 | 1.922 | ns |
| | | $t_h$ | -0.717 | -0.712 | -1.300 | -1.395 | -1.552 | -1.471 | -1.362 | -1.403 | -1.562 | -1.479 | -1.410 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -1.083 | -1.156 | -1.739 | -1.748 | -1.886 | -1.821 | -2.265 | -1.754 | -1.886 | -1.826 | -2.306 | ns |
| | | $t_h$ | 1.210 | 1.297 | 1.959 | 1.975 | 2.134 | 2.057 | 2.507 | 1.990 | 2.144 | 2.071 | 2.549 | ns |
| | GCLK PLL | $t_{su}$ | 0.985 | 0.998 | 1.749 | 1.861 | 2.075 | 1.963 | 1.867 | 1.883 | 2.101 | 1.987 | 1.925 | ns |
| | | $t_h$ | -0.718 | -0.713 | -1.295 | -1.387 | -1.548 | -1.467 | -1.357 | -1.399 | -1.563 | -1.480 | -1.409 | ns |
| | GCLK | $t_{su}$ | -1.083 | -1.156 | -1.739 | -1.748 | -1.886 | -1.821 | -2.265 | -1.754 | -1.886 | -1.826 | -2.306 | ns |
| | | $t_h$ | 1.210 | 1.297 | 1.959 | 1.975 | 2.134 | 2.057 | 2.507 | 1.990 | 2.144 | 2.071 | 2.549 | ns |
| | GCLK PLL | $t_{su}$ | 0.985 | 0.998 | 1.749 | 1.861 | 2.075 | 1.963 | 1.867 | 1.883 | 2.101 | 1.987 | 1.925 | ns |
| | | $t_h$ | -0.718 | -0.713 | -1.295 | -1.387 | -1.548 | -1.467 | -1.357 | -1.399 | -1.563 | -1.480 | -1.409 | ns |


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Table 1–97 lists the EP3SL340 column pins output timing parameters for differential I/O standards.

**Table 1–97.** EP3SL340 Column Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.438 | 3.700 | 5.415 | 5.607 | 6.143 | 5.991 | 6.399 | 5.739 | 6.274 | 6.122 | 6.475 | ns |
| | | GCLK PLL | $t_{co}$ | 1.427 | 1.606 | 2.089 | 2.181 | 2.406 | 2.407 | 2.475 | 2.287 | 2.511 | 2.514 | 2.459 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.434 | 3.703 | 5.462 | 5.662 | 6.205 | 6.053 | 6.461 | 5.798 | 6.340 | 6.188 | 6.541 | ns |
| | | GCLK PLL | $t_{co}$ | 1.423 | 1.609 | 2.136 | 2.236 | 2.468 | 2.469 | 2.537 | 2.346 | 2.577 | 2.580 | 2.525 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.438 | 3.700 | 5.415 | 5.607 | 6.143 | 5.991 | 6.399 | 5.739 | 6.274 | 6.122 | 6.475 | ns |
| | | GCLK PLL | $t_{co}$ | 1.427 | 1.606 | 2.089 | 2.181 | 2.406 | 2.407 | 2.475 | 2.287 | 2.511 | 2.514 | 2.459 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.434 | 3.703 | 5.462 | 5.662 | 6.205 | 6.053 | 6.461 | 5.798 | 6.340 | 6.188 | 6.541 | ns |
| | | GCLK PLL | $t_{co}$ | 1.423 | 1.609 | 2.136 | 2.236 | 2.468 | 2.469 | 2.537 | 2.346 | 2.577 | 2.580 | 2.525 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.438 | 3.700 | 5.415 | 5.607 | 6.143 | 5.991 | 6.399 | 5.739 | 6.274 | 6.122 | 6.475 | ns |
| | | GCLK PLL | $t_{co}$ | 1.427 | 1.606 | 2.089 | 2.181 | 2.406 | 2.407 | 2.475 | 2.287 | 2.511 | 2.514 | 2.459 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.434 | 3.703 | 5.462 | 5.662 | 6.205 | 6.053 | 6.461 | 5.798 | 6.340 | 6.188 | 6.541 | ns |
| | | GCLK PLL | $t_{co}$ | 1.423 | 1.609 | 2.136 | 2.236 | 2.468 | 2.469 | 2.537 | 2.346 | 2.577 | 2.580 | 2.525 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.465 | 3.733 | 5.486 | 5.685 | 6.227 | 6.075 | 6.483 | 5.819 | 6.360 | 6.208 | 6.561 | ns |
| | | GCLK PLL | $t_{co}$ | 1.454 | 1.639 | 2.160 | 2.259 | 2.490 | 2.491 | 2.559 | 2.367 | 2.597 | 2.600 | 2.545 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.455 | 3.723 | 5.476 | 5.674 | 6.217 | 6.065 | 6.473 | 5.808 | 6.350 | 6.198 | 6.551 | ns |
| | | GCLK PLL | $t_{co}$ | 1.444 | 1.629 | 2.150 | 2.248 | 2.480 | 2.481 | 2.549 | 2.356 | 2.587 | 2.590 | 2.535 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.455 | 3.723 | 5.479 | 5.678 | 6.221 | 6.069 | 6.477 | 5.813 | 6.355 | 6.203 | 6.556 | ns |
| | | GCLK PLL | $t_{co}$ | 1.444 | 1.629 | 2.153 | 2.252 | 2.484 | 2.485 | 2.553 | 2.361 | 2.592 | 2.595 | 2.540 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.448 | 3.717 | 5.472 | 5.672 | 6.215 | 6.063 | 6.471 | 5.806 | 6.349 | 6.197 | 6.550 | ns |
| | | GCLK PLL | $t_{co}$ | 1.437 | 1.623 | 2.146 | 2.246 | 2.478 | 2.479 | 2.547 | 2.354 | 2.586 | 2.589 | 2.534 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.447 | 3.715 | 5.469 | 5.669 | 6.212 | 6.060 | 6.468 | 5.803 | 6.345 | 6.193 | 6.546 | ns |
| | | GCLK PLL | $t_{co}$ | 1.436 | 1.621 | 2.143 | 2.243 | 2.475 | 2.476 | 2.544 | 2.351 | 2.582 | 2.585 | 2.530 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.469 | 3.737 | 5.490 | 5.689 | 6.231 | 6.079 | 6.487 | 5.823 | 6.365 | 6.213 | 6.566 | ns |
| | | GCLK PLL | $t_{co}$ | 1.458 | 1.643 | 2.164 | 2.263 | 2.494 | 2.495 | 2.563 | 2.371 | 2.602 | 2.605 | 2.550 | ns |

**Table 1–97.** EP3SL340 Column Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.459 | 3.726 | 5.469 | 5.666 | 6.206 | 6.054 | 6.462 | 5.799 | 6.338 | 6.186 | 6.539 | ns |
| | | GCLK PLL | $t_{co}$ | 1.448 | 1.632 | 2.143 | 2.240 | 2.469 | 2.470 | 2.538 | 2.347 | 2.575 | 2.578 | 2.523 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.454 | 3.722 | 5.469 | 5.666 | 6.207 | 6.055 | 6.463 | 5.800 | 6.340 | 6.188 | 6.541 | ns |
| | | GCLK PLL | $t_{co}$ | 1.443 | 1.628 | 2.143 | 2.240 | 2.470 | 2.471 | 2.539 | 2.348 | 2.577 | 2.580 | 2.525 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.452 | 3.720 | 5.468 | 5.665 | 6.205 | 6.053 | 6.461 | 5.799 | 6.339 | 6.187 | 6.540 | ns |
| | | GCLK PLL | $t_{co}$ | 1.441 | 1.626 | 2.142 | 2.239 | 2.468 | 2.469 | 2.537 | 2.347 | 2.576 | 2.579 | 2.524 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.444 | 3.711 | 5.458 | 5.655 | 6.196 | 6.044 | 6.452 | 5.789 | 6.329 | 6.177 | 6.530 | ns |
| | | GCLK PLL | $t_{co}$ | 1.433 | 1.617 | 2.132 | 2.229 | 2.459 | 2.460 | 2.528 | 2.337 | 2.566 | 2.569 | 2.514 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.445 | 3.713 | 5.464 | 5.662 | 6.204 | 6.052 | 6.460 | 5.797 | 6.338 | 6.186 | 6.539 | ns |
| | | GCLK PLL | $t_{co}$ | 1.434 | 1.619 | 2.138 | 2.236 | 2.467 | 2.468 | 2.536 | 2.345 | 2.575 | 2.578 | 2.523 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.444 | 3.710 | 5.447 | 5.643 | 6.182 | 6.030 | 6.438 | 5.776 | 6.314 | 6.162 | 6.515 | ns |
| | | GCLK PLL | $t_{co}$ | 1.433 | 1.616 | 2.121 | 2.217 | 2.445 | 2.446 | 2.514 | 2.324 | 2.551 | 2.554 | 2.499 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.456 | 3.723 | 5.465 | 5.661 | 6.200 | 6.048 | 6.456 | 5.795 | 6.333 | 6.181 | 6.534 | ns |
| | | GCLK PLL | $t_{co}$ | 1.445 | 1.629 | 2.139 | 2.235 | 2.463 | 2.464 | 2.532 | 2.343 | 2.570 | 2.573 | 2.518 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.452 | 3.720 | 5.466 | 5.663 | 6.204 | 6.052 | 6.460 | 5.797 | 6.337 | 6.185 | 6.538 | ns |
| | | GCLK PLL | $t_{co}$ | 1.441 | 1.626 | 2.140 | 2.237 | 2.467 | 2.468 | 2.536 | 2.345 | 2.574 | 2.577 | 2.522 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.442 | 3.709 | 5.455 | 5.652 | 6.192 | 6.040 | 6.448 | 5.786 | 6.325 | 6.173 | 6.526 | ns |
| | | GCLK PLL | $t_{co}$ | 1.431 | 1.615 | 2.129 | 2.226 | 2.455 | 2.456 | 2.524 | 2.334 | 2.562 | 2.565 | 2.510 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.440 | 3.707 | 5.453 | 5.649 | 6.190 | 6.038 | 6.446 | 5.784 | 6.323 | 6.171 | 6.524 | ns |
| | | GCLK PLL | $t_{co}$ | 1.429 | 1.613 | 2.127 | 2.223 | 2.453 | 2.454 | 2.522 | 2.332 | 2.560 | 2.563 | 2.508 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.440 | 3.708 | 5.456 | 5.654 | 6.195 | 6.043 | 6.451 | 5.788 | 6.329 | 6.177 | 6.530 | ns |
| | | GCLK PLL | $t_{co}$ | 1.429 | 1.614 | 2.130 | 2.228 | 2.458 | 2.459 | 2.527 | 2.336 | 2.566 | 2.569 | 2.514 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.444 | 3.711 | 5.453 | 5.649 | 6.189 | 6.037 | 6.445 | 5.783 | 6.322 | 6.170 | 6.523 | ns |
| | | GCLK PLL | $t_{co}$ | 1.433 | 1.617 | 2.127 | 2.223 | 2.452 | 2.453 | 2.521 | 2.331 | 2.559 | 2.562 | 2.507 | ns |


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**Table 1–97.** EP3SL340 Column Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.470 | 3.740 | 5.498 | 5.697 | 6.239 | 6.087 | 6.495 | 5.831 | 6.372 | 6.220 | 6.573 | ns |
| | | GCLK PLL | $t_{co}$ | 1.459 | 1.646 | 2.172 | 2.271 | 2.502 | 2.503 | 2.571 | 2.379 | 2.609 | 2.612 | 2.557 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.456 | 3.726 | 5.486 | 5.686 | 6.229 | 6.077 | 6.485 | 5.821 | 6.363 | 6.211 | 6.564 | ns |
| | | GCLK PLL | $t_{co}$ | 1.445 | 1.632 | 2.160 | 2.260 | 2.492 | 2.493 | 2.561 | 2.369 | 2.600 | 2.603 | 2.548 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.444 | 3.713 | 5.469 | 5.668 | 6.211 | 6.059 | 6.467 | 5.803 | 6.345 | 6.193 | 6.546 | ns |
| | | GCLK PLL | $t_{co}$ | 1.433 | 1.619 | 2.143 | 2.242 | 2.474 | 2.475 | 2.543 | 2.351 | 2.582 | 2.585 | 2.530 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.444 | 3.713 | 5.472 | 5.672 | 6.215 | 6.063 | 6.471 | 5.807 | 6.350 | 6.198 | 6.551 | ns |
| | | GCLK PLL | $t_{co}$ | 1.433 | 1.619 | 2.146 | 2.246 | 2.478 | 2.479 | 2.547 | 2.355 | 2.587 | 2.590 | 2.535 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.440 | 3.709 | 5.465 | 5.664 | 6.208 | 6.056 | 6.464 | 5.800 | 6.342 | 6.190 | 6.543 | ns |
| | | GCLK PLL | $t_{co}$ | 1.429 | 1.615 | 2.139 | 2.238 | 2.471 | 2.472 | 2.540 | 2.348 | 2.579 | 2.582 | 2.527 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.444 | 3.711 | 5.458 | 5.655 | 6.196 | 6.044 | 6.452 | 5.789 | 6.329 | 6.177 | 6.530 | ns |
| | | GCLK PLL | $t_{co}$ | 1.433 | 1.617 | 2.132 | 2.229 | 2.459 | 2.460 | 2.528 | 2.337 | 2.566 | 2.569 | 2.514 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.445 | 3.713 | 5.466 | 5.665 | 6.207 | 6.055 | 6.463 | 5.799 | 6.341 | 6.189 | 6.542 | ns |
| | | GCLK PLL | $t_{co}$ | 1.434 | 1.619 | 2.140 | 2.239 | 2.470 | 2.471 | 2.539 | 2.347 | 2.578 | 2.581 | 2.526 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.473 | 3.743 | 5.497 | 5.695 | 6.237 | 6.085 | 6.493 | 5.830 | 6.370 | 6.218 | 6.571 | ns |
| | | GCLK PLL | $t_{co}$ | 1.462 | 1.649 | 2.171 | 2.269 | 2.500 | 2.501 | 2.569 | 2.378 | 2.607 | 2.610 | 2.555 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.462 | 3.731 | 5.485 | 5.683 | 6.225 | 6.073 | 6.481 | 5.818 | 6.358 | 6.206 | 6.559 | ns |
| | | GCLK PLL | $t_{co}$ | 1.451 | 1.637 | 2.159 | 2.257 | 2.488 | 2.489 | 2.557 | 2.366 | 2.595 | 2.598 | 2.543 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.457 | 3.727 | 5.485 | 5.684 | 6.226 | 6.074 | 6.482 | 5.819 | 6.360 | 6.208 | 6.561 | ns |
| | | GCLK PLL | $t_{co}$ | 1.446 | 1.633 | 2.159 | 2.258 | 2.489 | 2.490 | 2.558 | 2.367 | 2.597 | 2.600 | 2.545 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.443 | 3.712 | 5.467 | 5.665 | 6.207 | 6.055 | 6.463 | 5.800 | 6.342 | 6.190 | 6.543 | ns |
| | | GCLK PLL | $t_{co}$ | 1.432 | 1.618 | 2.141 | 2.239 | 2.470 | 2.471 | 2.539 | 2.348 | 2.579 | 2.582 | 2.527 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.441 | 3.710 | 5.465 | 5.663 | 6.205 | 6.053 | 6.461 | 5.798 | 6.339 | 6.187 | 6.540 | ns |
| | | GCLK PLL | $t_{co}$ | 1.430 | 1.616 | 2.139 | 2.237 | 2.468 | 2.469 | 2.537 | 2.346 | 2.576 | 2.579 | 2.524 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.445 | 3.712 | 5.457 | 5.653 | 6.193 | 6.041 | 6.449 | 5.787 | 6.326 | 6.174 | 6.527 | ns |
| | | GCLK PLL | $t_{co}$ | 1.434 | 1.618 | 2.131 | 2.227 | 2.456 | 2.457 | 2.525 | 2.335 | 2.563 | 2.566 | 2.511 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.445 | 3.713 | 5.465 | 5.663 | 6.205 | 6.053 | 6.461 | 5.798 | 6.339 | 6.187 | 6.540 | ns |
| | | GCLK PLL | $t_{co}$ | 1.434 | 1.619 | 2.139 | 2.237 | 2.468 | 2.469 | 2.537 | 2.346 | 2.576 | 2.579 | 2.524 | ns |

**Table 1–97.** EP3SL340 Column Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.461 | 3.730 | 5.481 | 5.678 | 6.219 | 6.067 | 6.475 | 5.813 | 6.352 | 6.200 | 6.553 | ns |
| | | GCLK PLL | $t_{co}$ | 1.450 | 1.636 | 2.155 | 2.252 | 2.482 | 2.483 | 2.551 | 2.361 | 2.589 | 2.592 | 2.537 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.461 | 3.730 | 5.481 | 5.678 | 6.219 | 6.067 | 6.475 | 5.813 | 6.352 | 6.200 | 6.553 | ns |
| | | GCLK PLL | $t_{co}$ | 1.450 | 1.636 | 2.155 | 2.252 | 2.482 | 2.483 | 2.551 | 2.361 | 2.589 | 2.592 | 2.537 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.451 | 3.720 | 5.471 | 5.668 | 6.209 | 6.057 | 6.465 | 5.803 | 6.343 | 6.191 | 6.544 | ns |
| | | GCLK PLL | $t_{co}$ | 1.440 | 1.626 | 2.145 | 2.242 | 2.472 | 2.473 | 2.541 | 2.351 | 2.580 | 2.583 | 2.528 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.444 | 3.712 | 5.457 | 5.653 | 6.193 | 6.041 | 6.449 | 5.787 | 6.326 | 6.174 | 6.527 | ns |
| | | GCLK PLL | $t_{co}$ | 1.433 | 1.618 | 2.131 | 2.227 | 2.456 | 2.457 | 2.525 | 2.335 | 2.563 | 2.566 | 2.511 | ns |

Table 1–98 lists the EP3SL340 row pins output timing parameters for differential I/O standards.

**Table 1–98.** EP3SL340 Row Pins Output Timing Parameters (Part 1 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | — | GCLK | $t_{co}$ | 3.022 | 3.234 | 4.714 | 4.872 | 5.362 | 5.217 | 5.602 | 4.981 | 5.467 | 5.326 | 5.662 | ns |
| | | GCLK PLL | $t_{co}$ | 1.063 | 1.193 | 1.445 | 1.501 | 1.678 | 1.690 | 1.735 | 1.583 | 1.761 | 1.772 | 1.704 | ns |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.414 | 3.678 | 5.396 | 5.588 | 6.125 | 5.972 | 6.349 | 5.722 | 6.255 | 6.105 | 6.425 | ns |
| | | GCLK PLL | $t_{co}$ | 1.455 | 1.637 | 2.127 | 2.217 | 2.441 | 2.445 | 2.482 | 2.324 | 2.549 | 2.551 | 2.467 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.396 | 3.668 | 5.434 | 5.634 | 6.179 | 6.026 | 6.403 | 5.773 | 6.316 | 6.166 | 6.486 | ns |
| | | GCLK PLL | $t_{co}$ | 1.437 | 1.627 | 2.165 | 2.263 | 2.495 | 2.499 | 2.536 | 2.375 | 2.610 | 2.612 | 2.528 | ns |
| MINI-LVDS | — | GCLK | $t_{co}$ | 3.022 | 3.234 | 4.714 | 4.872 | 5.362 | 5.217 | 5.602 | 4.981 | 5.467 | 5.326 | 5.662 | ns |
| | | GCLK PLL | $t_{co}$ | 1.063 | 1.193 | 1.445 | 1.501 | 1.678 | 1.690 | 1.735 | 1.583 | 1.761 | 1.772 | 1.704 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.414 | 3.678 | 5.396 | 5.588 | 6.125 | 5.972 | 6.349 | 5.722 | 6.255 | 6.105 | 6.425 | ns |
| | | GCLK PLL | $t_{co}$ | 1.455 | 1.637 | 2.127 | 2.217 | 2.441 | 2.445 | 2.482 | 2.324 | 2.549 | 2.551 | 2.467 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.396 | 3.668 | 5.434 | 5.634 | 6.179 | 6.026 | 6.403 | 5.773 | 6.316 | 6.166 | 6.486 | ns |
| | | GCLK PLL | $t_{co}$ | 1.437 | 1.627 | 2.165 | 2.263 | 2.495 | 2.499 | 2.536 | 2.375 | 2.610 | 2.612 | 2.528 | ns |
| RSDS | — | GCLK | $t_{co}$ | 3.022 | 3.234 | 4.714 | 4.872 | 5.362 | 5.217 | 5.602 | 4.981 | 5.467 | 5.326 | 5.662 | ns |
| | | GCLK PLL | $t_{co}$ | 1.063 | 1.193 | 1.445 | 1.501 | 1.678 | 1.690 | 1.735 | 1.583 | 1.761 | 1.772 | 1.704 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.414 | 3.678 | 5.396 | 5.588 | 6.125 | 5.972 | 6.349 | 5.722 | 6.255 | 6.105 | 6.425 | ns |
| | | GCLK PLL | $t_{co}$ | 1.455 | 1.637 | 2.127 | 2.217 | 2.441 | 2.445 | 2.482 | 2.324 | 2.549 | 2.551 | 2.467 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.396 | 3.668 | 5.434 | 5.634 | 6.179 | 6.026 | 6.403 | 5.773 | 6.316 | 6.166 | 6.486 | ns |
| | | GCLK PLL | $t_{co}$ | 1.437 | 1.627 | 2.165 | 2.263 | 2.495 | 2.499 | 2.536 | 2.375 | 2.610 | 2.612 | 2.528 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.440 | 3.711 | 5.470 | 5.668 | 6.212 | 6.059 | 6.436 | 5.806 | 6.345 | 6.195 | 6.515 | ns |
| | | GCLK PLL | $t_{co}$ | 1.491 | 1.680 | 2.211 | 2.307 | 2.538 | 2.542 | 2.579 | 2.418 | 2.649 | 2.651 | 2.567 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.426 | 3.697 | 5.457 | 5.655 | 6.199 | 6.046 | 6.423 | 5.792 | 6.332 | 6.182 | 6.502 | ns |
| | | GCLK PLL | $t_{co}$ | 1.477 | 1.666 | 2.198 | 2.294 | 2.525 | 2.529 | 2.566 | 2.404 | 2.636 | 2.638 | 2.554 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.422 | 3.693 | 5.455 | 5.655 | 6.200 | 6.047 | 6.424 | 5.792 | 6.334 | 6.184 | 6.504 | ns |
| | | GCLK PLL | $t_{co}$ | 1.473 | 1.662 | 2.196 | 2.294 | 2.526 | 2.530 | 2.567 | 2.404 | 2.638 | 2.640 | 2.556 | ns |

**Table 1–98.** EP3SL340 Row Pins Output Timing Parameters (Part 2 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.438 | 3.708 | 5.456 | 5.652 | 6.194 | 6.041 | 6.418 | 5.789 | 6.327 | 6.177 | 6.497 | ns |
| | | GCLK PLL | $t_{co}$ | 1.489 | 1.677 | 2.197 | 2.291 | 2.520 | 2.524 | 2.561 | 2.401 | 2.631 | 2.633 | 2.549 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.427 | 3.698 | 5.452 | 5.648 | 6.191 | 6.038 | 6.415 | 5.786 | 6.324 | 6.174 | 6.494 | ns |
| | | GCLK PLL | $t_{co}$ | 1.478 | 1.667 | 2.193 | 2.287 | 2.517 | 2.521 | 2.558 | 2.398 | 2.628 | 2.630 | 2.546 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.424 | 3.695 | 5.450 | 5.646 | 6.189 | 6.036 | 6.413 | 5.784 | 6.323 | 6.173 | 6.493 | ns |
| | | GCLK PLL | $t_{co}$ | 1.475 | 1.664 | 2.191 | 2.285 | 2.515 | 2.519 | 2.556 | 2.396 | 2.627 | 2.629 | 2.545 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.435 | 3.705 | 5.451 | 5.647 | 6.188 | 6.035 | 6.412 | 5.784 | 6.321 | 6.171 | 6.491 | ns |
| | | GCLK PLL | $t_{co}$ | 1.486 | 1.674 | 2.192 | 2.286 | 2.514 | 2.518 | 2.555 | 2.396 | 2.625 | 2.627 | 2.543 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.425 | 3.696 | 5.449 | 5.645 | 6.187 | 6.034 | 6.411 | 5.783 | 6.321 | 6.171 | 6.491 | ns |
| | | GCLK PLL | $t_{co}$ | 1.476 | 1.665 | 2.190 | 2.284 | 2.513 | 2.517 | 2.554 | 2.395 | 2.625 | 2.627 | 2.543 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.411 | 3.682 | 5.434 | 5.630 | 6.173 | 6.020 | 6.397 | 5.768 | 6.306 | 6.156 | 6.476 | ns |
| | | GCLK PLL | $t_{co}$ | 1.462 | 1.651 | 2.175 | 2.269 | 2.499 | 2.503 | 2.540 | 2.380 | 2.610 | 2.612 | 2.528 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.408 | 3.678 | 5.430 | 5.626 | 6.169 | 6.016 | 6.393 | 5.764 | 6.302 | 6.152 | 6.472 | ns |
| | | GCLK PLL | $t_{co}$ | 1.459 | 1.647 | 2.171 | 2.265 | 2.495 | 2.499 | 2.536 | 2.376 | 2.606 | 2.608 | 2.524 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.405 | 3.676 | 5.431 | 5.629 | 6.172 | 6.019 | 6.396 | 5.767 | 6.306 | 6.156 | 6.476 | ns |
| | | GCLK PLL | $t_{co}$ | 1.456 | 1.645 | 2.172 | 2.268 | 2.498 | 2.502 | 2.539 | 2.379 | 2.610 | 2.612 | 2.528 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.406 | 3.676 | 5.421 | 5.617 | 6.159 | 6.006 | 6.383 | 5.754 | 6.292 | 6.142 | 6.462 | ns |
| | | GCLK PLL | $t_{co}$ | 1.457 | 1.645 | 2.162 | 2.256 | 2.485 | 2.489 | 2.526 | 2.366 | 2.596 | 2.598 | 2.514 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.455 | 3.729 | 5.492 | 5.690 | 6.235 | 6.082 | 6.459 | 5.828 | 6.368 | 6.218 | 6.538 | ns |
| | | GCLK PLL | $t_{co}$ | 1.506 | 1.698 | 2.233 | 2.329 | 2.561 | 2.565 | 2.602 | 2.440 | 2.672 | 2.674 | 2.590 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.431 | 3.705 | 5.474 | 5.673 | 6.218 | 6.065 | 6.442 | 5.811 | 6.353 | 6.203 | 6.523 | ns |
| | | GCLK PLL | $t_{co}$ | 1.482 | 1.674 | 2.215 | 2.312 | 2.544 | 2.548 | 2.585 | 2.423 | 2.657 | 2.659 | 2.575 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.414 | 3.686 | 5.452 | 5.651 | 6.196 | 6.043 | 6.420 | 5.789 | 6.331 | 6.181 | 6.501 | ns |
| | | GCLK PLL | $t_{co}$ | 1.465 | 1.655 | 2.193 | 2.290 | 2.522 | 2.526 | 2.563 | 2.401 | 2.635 | 2.637 | 2.553 | ns |


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**Table 1–98.** EP3SL340 Row Pins Output Timing Parameters (Part 3 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.459 | 3.732 | 5.492 | 5.690 | 6.234 | 6.081 | 6.458 | 5.828 | 6.368 | 6.218 | 6.538 | ns |
| | | GCLK PLL | $t_{co}$ | 1.510 | 1.701 | 2.233 | 2.329 | 2.560 | 2.564 | 2.601 | 2.440 | 2.672 | 2.674 | 2.590 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.444 | 3.717 | 5.478 | 5.675 | 6.219 | 6.066 | 6.443 | 5.813 | 6.353 | 6.203 | 6.523 | ns |
| | | GCLK PLL | $t_{co}$ | 1.495 | 1.686 | 2.219 | 2.314 | 2.545 | 2.549 | 2.586 | 2.425 | 2.657 | 2.659 | 2.575 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.433 | 3.706 | 5.473 | 5.672 | 6.216 | 6.063 | 6.440 | 5.810 | 6.351 | 6.201 | 6.521 | ns |
| | | GCLK PLL | $t_{co}$ | 1.484 | 1.675 | 2.214 | 2.311 | 2.542 | 2.546 | 2.583 | 2.422 | 2.655 | 2.657 | 2.573 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.413 | 3.686 | 5.450 | 5.648 | 6.193 | 6.040 | 6.417 | 5.787 | 6.327 | 6.177 | 6.497 | ns |
| | | GCLK PLL | $t_{co}$ | 1.464 | 1.655 | 2.191 | 2.287 | 2.519 | 2.523 | 2.560 | 2.399 | 2.631 | 2.633 | 2.549 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.410 | 3.682 | 5.446 | 5.645 | 6.189 | 6.036 | 6.413 | 5.783 | 6.324 | 6.174 | 6.494 | ns |
| | | GCLK PLL | $t_{co}$ | 1.461 | 1.651 | 2.187 | 2.284 | 2.515 | 2.519 | 2.556 | 2.395 | 2.628 | 2.630 | 2.546 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.415 | 3.686 | 5.437 | 5.633 | 6.175 | 6.022 | 6.399 | 5.770 | 6.308 | 6.158 | 6.478 | ns |
| | | GCLK PLL | $t_{co}$ | 1.466 | 1.655 | 2.178 | 2.272 | 2.501 | 2.505 | 2.542 | 2.382 | 2.612 | 2.614 | 2.530 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.408 | 3.679 | 5.436 | 5.634 | 6.178 | 6.025 | 6.402 | 5.773 | 6.313 | 6.163 | 6.483 | ns |
| | | GCLK PLL | $t_{co}$ | 1.459 | 1.648 | 2.177 | 2.273 | 2.504 | 2.508 | 2.545 | 2.385 | 2.617 | 2.619 | 2.535 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.446 | 3.718 | 5.474 | 5.671 | 6.214 | 6.061 | 6.438 | 5.809 | 6.348 | 6.198 | 6.518 | ns |
| | | GCLK PLL | $t_{co}$ | 1.487 | 1.677 | 2.205 | 2.300 | 2.530 | 2.534 | 2.571 | 2.411 | 2.642 | 2.644 | 2.560 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.428 | 3.701 | 5.459 | 5.656 | 6.199 | 6.046 | 6.423 | 5.794 | 6.333 | 6.183 | 6.503 | ns |
| | | GCLK PLL | $t_{co}$ | 1.469 | 1.660 | 2.190 | 2.285 | 2.515 | 2.519 | 2.556 | 2.396 | 2.627 | 2.629 | 2.545 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.414 | 3.685 | 5.436 | 5.632 | 6.174 | 6.021 | 6.398 | 5.770 | 6.308 | 6.158 | 6.478 | ns |
| | | GCLK PLL | $t_{co}$ | 1.455 | 1.644 | 2.167 | 2.261 | 2.490 | 2.494 | 2.531 | 2.372 | 2.602 | 2.604 | 2.520 | ns |

Table 1–99 and Table 1–100 list the EP3SL340 regional (RCLK) clock adder values that must be added to the GCLK values. Use these adder values to determine I/O timing when the I/O pin is driven using the regional clock. This applies to all I/O standards supported by Stratix III devices.

Table 1–99 lists the EP3SL340 column pin delay adders when using the regional clock.

**Table 1–99.** EP3SL340 Column Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.318 | 0.171 | 0.255 | 0.247 | 0.257 | 0.244 | 0.369 | 0.37 | 0.253 | 0.232 | 0.336 | ns |
| RCLK PLL input adder | 2.716 | 2.739 | 4.379 | 4.508 | 4.926 | 4.717 | 5.376 | 4.508 | 4.94 | 4.89 | 5.434 | ns |
| RCLK output adder | -0.341 | -0.107 | -0.18 | -0.169 | -0.171 | -0.167 | -0.362 | -0.03 | -0.043 | -0.034 | -0.287 | ns |
| RCLK PLL output adder | -2.36 | -2.128 | -3.344 | -3.384 | -3.571 | -3.487 | -3.545 | -3.246 | -3.636 | -3.357 | -3.544 | ns |

Table 1–100 lists the EP3SL340 row pin delay adders when using the regional clock.

**Table 1–100.** EP3SL340 Row Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.075 | 0.079 | 0.133 | 0.124 | 0.125 | 0.124 | 0.307 | 0.117 | 0.116 | 0.117 | 0.31 | ns |
| RCLK PLL input adder | 0.157 | 0.151 | 0.262 | 0.274 | 0.306 | 0.288 | 0.464 | 0.268 | 0.291 | 0.278 | 0.46 | ns |
| RCLK output adder | -0.052 | -0.066 | -0.107 | -0.098 | -0.127 | -0.129 | -0.282 | -0.082 | -0.118 | -0.085 | -0.285 | ns |
| RCLK PLL output adder | -0.157 | -0.139 | -0.232 | -0.248 | -0.272 | -0.259 | -0.422 | -0.252 | -0.256 | -0.244 | -0.444 | ns |

## EP3SE50 I/O Timing Parameters

Table 1–101 through Table 1–104 list the maximum I/O timing parameters for EP3SE50 devices for single-ended I/O standards.

Table 1–101 lists the EP3SE50 column pins input timing parameters for single-ended I/O standards.

**Table 1–101.** EP3SE50 Column Pins Input Timing Parameters (Part 1 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -0.743 | -0.742 | -1.063 | -1.165 | -1.374 | -1.329 | -1.605 | -1.165 | -1.374 | -1.329 | -1.605 | ns |
| | | $t_h$ | 0.870 | 0.869 | 1.241 | 1.366 | 1.595 | 1.538 | 1.815 | 1.366 | 1.595 | 1.538 | 1.815 | ns |
| | GCLK PLL | $t_{su}$ | -1.037 | -1.037 | -1.466 | -1.593 | -1.830 | -1.772 | -2.038 | -1.593 | -1.830 | -1.772 | -2.038 | ns |
| | | $t_h$ | 1.290 | 1.290 | 1.836 | 2.009 | 2.292 | 2.207 | 2.484 | 2.009 | 2.292 | 2.207 | 2.484 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -0.743 | -0.742 | -1.063 | -1.165 | -1.374 | -1.329 | -1.605 | -1.165 | -1.374 | -1.329 | -1.605 | ns |
| | | $t_h$ | 0.870 | 0.869 | 1.241 | 1.366 | 1.595 | 1.538 | 1.815 | 1.366 | 1.595 | 1.538 | 1.815 | ns |
| | GCLK PLL | $t_{su}$ | -1.037 | -1.037 | -1.466 | -1.593 | -1.830 | -1.772 | -2.038 | -1.593 | -1.830 | -1.772 | -2.038 | ns |
| | | $t_h$ | 1.290 | 1.290 | 1.836 | 2.009 | 2.292 | 2.207 | 2.484 | 2.009 | 2.292 | 2.207 | 2.484 | ns |

**Table 1–101.** EP3SE50 Column Pins Input Timing Parameters (Part 2 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -0.754 | -0.753 | -1.062 | -1.167 | -1.373 | -1.328 | -1.604 | -1.167 | -1.373 | -1.328 | -1.604 | ns |
| | | $t_h$ | 0.881 | 0.880 | 1.240 | 1.368 | 1.594 | 1.537 | 1.814 | 1.368 | 1.594 | 1.537 | 1.814 | ns |
| | GCLK PLL | $t_{su}$ | -1.048 | -1.048 | -1.465 | -1.595 | -1.829 | -1.771 | -2.037 | -1.595 | -1.829 | -1.771 | -2.037 | ns |
| | | $t_h$ | 1.301 | 1.301 | 1.835 | 2.011 | 2.291 | 2.206 | 2.483 | 2.011 | 2.291 | 2.206 | 2.483 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -0.754 | -0.753 | -1.062 | -1.167 | -1.373 | -1.328 | -1.604 | -1.167 | -1.373 | -1.328 | -1.604 | ns |
| | | $t_h$ | 0.881 | 0.880 | 1.240 | 1.368 | 1.594 | 1.537 | 1.814 | 1.368 | 1.594 | 1.537 | 1.814 | ns |
| | GCLK PLL | $t_{su}$ | -1.048 | -1.048 | -1.465 | -1.595 | -1.829 | -1.771 | -2.037 | -1.595 | -1.829 | -1.771 | -2.037 | ns |
| | | $t_h$ | 1.301 | 1.301 | 1.835 | 2.011 | 2.291 | 2.206 | 2.483 | 2.011 | 2.291 | 2.206 | 2.483 | ns |
| 2.5 V | GCLK | $t_{su}$ | -0.749 | -0.748 | -1.071 | -1.179 | -1.392 | -1.347 | -1.623 | -1.179 | -1.392 | -1.347 | -1.623 | ns |
| | | $t_h$ | 0.876 | 0.875 | 1.249 | 1.380 | 1.613 | 1.556 | 1.833 | 1.380 | 1.613 | 1.556 | 1.833 | ns |
| | GCLK PLL | $t_{su}$ | -1.043 | -1.043 | -1.474 | -1.607 | -1.848 | -1.790 | -2.056 | -1.607 | -1.848 | -1.790 | -2.056 | ns |
| | | $t_h$ | 1.296 | 1.296 | 1.844 | 2.023 | 2.310 | 2.225 | 2.502 | 2.023 | 2.310 | 2.225 | 2.502 | ns |
| 1.8 V | GCLK | $t_{su}$ | -0.769 | -0.768 | -1.111 | -1.215 | -1.390 | -1.345 | -1.621 | -1.215 | -1.390 | -1.345 | -1.621 | ns |
| | | $t_h$ | 0.898 | 0.897 | 1.289 | 1.416 | 1.611 | 1.554 | 1.831 | 1.416 | 1.611 | 1.554 | 1.831 | ns |
| | GCLK PLL | $t_{su}$ | -1.065 | -1.065 | -1.514 | -1.643 | -1.846 | -1.788 | -2.054 | -1.643 | -1.846 | -1.788 | -2.054 | ns |
| | | $t_h$ | 1.320 | 1.320 | 1.884 | 2.059 | 2.308 | 2.223 | 2.500 | 2.059 | 2.308 | 2.223 | 2.500 | ns |
| 1.5 V | GCLK | $t_{su}$ | -0.759 | -0.758 | -1.088 | -1.183 | -1.320 | -1.275 | -1.551 | -1.183 | -1.320 | -1.275 | -1.551 | ns |
| | | $t_h$ | 0.888 | 0.887 | 1.266 | 1.384 | 1.541 | 1.484 | 1.761 | 1.384 | 1.541 | 1.484 | 1.761 | ns |
| | GCLK PLL | $t_{su}$ | -1.055 | -1.055 | -1.491 | -1.611 | -1.776 | -1.718 | -1.984 | -1.611 | -1.776 | -1.718 | -1.984 | ns |
| | | $t_h$ | 1.310 | 1.310 | 1.861 | 2.027 | 2.238 | 2.153 | 2.430 | 2.027 | 2.238 | 2.153 | 2.430 | ns |
| 1.2 V | GCLK | $t_{su}$ | -0.707 | -0.706 | -1.011 | -1.084 | -1.164 | -1.119 | -1.395 | -1.084 | -1.164 | -1.119 | -1.395 | ns |
| | | $t_h$ | 0.836 | 0.835 | 1.189 | 1.285 | 1.385 | 1.328 | 1.605 | 1.285 | 1.385 | 1.328 | 1.605 | ns |
| | GCLK PLL | $t_{su}$ | -1.003 | -1.003 | -1.414 | -1.512 | -1.620 | -1.562 | -1.828 | -1.512 | -1.620 | -1.562 | -1.828 | ns |
| | | $t_h$ | 1.258 | 1.258 | 1.784 | 1.928 | 2.082 | 1.997 | 2.274 | 1.928 | 2.082 | 1.997 | 2.274 | ns |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -0.678 | -0.677 | -0.983 | -1.068 | -1.166 | -1.121 | -1.397 | -1.068 | -1.166 | -1.121 | -1.397 | ns |
| | | $t_h$ | 0.807 | 0.806 | 1.161 | 1.269 | 1.387 | 1.330 | 1.607 | 1.269 | 1.387 | 1.330 | 1.607 | ns |
| | GCLK PLL | $t_{su}$ | -0.974 | -0.974 | -1.386 | -1.496 | -1.622 | -1.564 | -1.830 | -1.496 | -1.622 | -1.564 | -1.830 | ns |
| | | $t_h$ | 1.229 | 1.229 | 1.756 | 1.912 | 2.084 | 1.999 | 2.276 | 1.912 | 2.084 | 1.999 | 2.276 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -0.678 | -0.677 | -0.983 | -1.068 | -1.166 | -1.121 | -1.397 | -1.068 | -1.166 | -1.121 | -1.397 | ns |
| | | $t_h$ | 0.807 | 0.806 | 1.161 | 1.269 | 1.387 | 1.330 | 1.607 | 1.269 | 1.387 | 1.330 | 1.607 | ns |
| | GCLK PLL | $t_{su}$ | -0.974 | -0.974 | -1.386 | -1.496 | -1.622 | -1.564 | -1.830 | -1.496 | -1.622 | -1.564 | -1.830 | ns |
| | | $t_h$ | 1.229 | 1.229 | 1.756 | 1.912 | 2.084 | 1.999 | 2.276 | 1.912 | 2.084 | 1.999 | 2.276 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -0.672 | -0.671 | -0.971 | -1.063 | -1.166 | -1.119 | -1.398 | -1.063 | -1.166 | -1.119 | -1.398 | ns |
| | | $t_h$ | 0.801 | 0.800 | 1.148 | 1.261 | 1.384 | 1.327 | 1.603 | 1.261 | 1.384 | 1.327 | 1.603 | ns |
| | GCLK PLL | $t_{su}$ | -0.968 | -0.968 | -1.373 | -1.488 | -1.619 | -1.559 | -1.828 | -1.488 | -1.619 | -1.559 | -1.828 | ns |
| | | $t_h$ | 1.223 | 1.223 | 1.743 | 1.901 | 2.078 | 1.993 | 2.269 | 1.901 | 2.078 | 1.993 | 2.269 | ns |

**Table 1–101.** EP3SE50 Column Pins Input Timing Parameters (Part 3 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -0.672 | -0.671 | -0.971 | -1.063 | -1.166 | -1.119 | -1.398 | -1.063 | -1.166 | -1.119 | -1.398 | ns |
| | | $t_h$ | 0.801 | 0.800 | 1.148 | 1.261 | 1.384 | 1.327 | 1.603 | 1.261 | 1.384 | 1.327 | 1.603 | ns |
| | GCLK PLL | $t_{su}$ | -0.968 | -0.968 | -1.373 | -1.488 | -1.619 | -1.559 | -1.828 | -1.488 | -1.619 | -1.559 | -1.828 | ns |
| | | $t_h$ | 1.223 | 1.223 | 1.743 | 1.901 | 2.078 | 1.993 | 2.269 | 1.901 | 2.078 | 1.993 | 2.269 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -0.661 | -0.660 | -0.962 | -1.052 | -1.147 | -1.100 | -1.379 | -1.052 | -1.147 | -1.100 | -1.379 | ns |
| | | $t_h$ | 0.790 | 0.789 | 1.138 | 1.250 | 1.365 | 1.308 | 1.584 | 1.250 | 1.365 | 1.308 | 1.584 | ns |
| | GCLK PLL | $t_{su}$ | -0.957 | -0.957 | -1.362 | -1.477 | -1.600 | -1.540 | -1.809 | -1.477 | -1.600 | -1.540 | -1.809 | ns |
| | | $t_h$ | 1.212 | 1.212 | 1.731 | 1.890 | 2.059 | 1.974 | 2.250 | 1.890 | 2.059 | 1.974 | 2.250 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.661 | -0.660 | -0.962 | -1.052 | -1.147 | -1.100 | -1.379 | -1.052 | -1.147 | -1.100 | -1.379 | ns |
| | | $t_h$ | 0.790 | 0.789 | 1.138 | 1.250 | 1.365 | 1.308 | 1.584 | 1.250 | 1.365 | 1.308 | 1.584 | ns |
| | GCLK PLL | $t_{su}$ | -0.957 | -0.957 | -1.362 | -1.477 | -1.600 | -1.540 | -1.809 | -1.477 | -1.600 | -1.540 | -1.809 | ns |
| | | $t_h$ | 1.212 | 1.212 | 1.731 | 1.890 | 2.059 | 1.974 | 2.250 | 1.890 | 2.059 | 1.974 | 2.250 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.672 | -0.671 | -0.971 | -1.063 | -1.166 | -1.119 | -1.398 | -1.063 | -1.166 | -1.119 | -1.398 | ns |
| | | $t_h$ | 0.801 | 0.800 | 1.148 | 1.261 | 1.384 | 1.327 | 1.603 | 1.261 | 1.384 | 1.327 | 1.603 | ns |
| | GCLK PLL | $t_{su}$ | -0.968 | -0.968 | -1.373 | -1.488 | -1.619 | -1.559 | -1.828 | -1.488 | -1.619 | -1.559 | -1.828 | ns |
| | | $t_h$ | 1.223 | 1.223 | 1.743 | 1.901 | 2.078 | 1.993 | 2.269 | 1.901 | 2.078 | 1.993 | 2.269 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.672 | -0.671 | -0.971 | -1.063 | -1.166 | -1.119 | -1.398 | -1.063 | -1.166 | -1.119 | -1.398 | ns |
| | | $t_h$ | 0.801 | 0.800 | 1.148 | 1.261 | 1.384 | 1.327 | 1.603 | 1.261 | 1.384 | 1.327 | 1.603 | ns |
| | GCLK PLL | $t_{su}$ | -0.968 | -0.968 | -1.373 | -1.488 | -1.619 | -1.559 | -1.828 | -1.488 | -1.619 | -1.559 | -1.828 | ns |
| | | $t_h$ | 1.223 | 1.223 | 1.743 | 1.901 | 2.078 | 1.993 | 2.269 | 1.901 | 2.078 | 1.993 | 2.269 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.661 | -0.660 | -0.962 | -1.052 | -1.147 | -1.100 | -1.379 | -1.052 | -1.147 | -1.100 | -1.379 | ns |
| | | $t_h$ | 0.790 | 0.789 | 1.138 | 1.250 | 1.365 | 1.308 | 1.584 | 1.250 | 1.365 | 1.308 | 1.584 | ns |
| | GCLK PLL | $t_{su}$ | -0.957 | -0.957 | -1.362 | -1.477 | -1.600 | -1.540 | -1.809 | -1.477 | -1.600 | -1.540 | -1.809 | ns |
| | | $t_h$ | 1.212 | 1.212 | 1.731 | 1.890 | 2.059 | 1.974 | 2.250 | 1.890 | 2.059 | 1.974 | 2.250 | ns |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.661 | -0.660 | -0.962 | -1.052 | -1.147 | -1.100 | -1.379 | -1.052 | -1.147 | -1.100 | -1.379 | ns |
| | | $t_h$ | 0.790 | 0.789 | 1.138 | 1.250 | 1.365 | 1.308 | 1.584 | 1.250 | 1.365 | 1.308 | 1.584 | ns |
| | GCLK PLL | $t_{su}$ | -0.957 | -0.957 | -1.362 | -1.477 | -1.600 | -1.540 | -1.809 | -1.477 | -1.600 | -1.540 | -1.809 | ns |
| | | $t_h$ | 1.212 | 1.212 | 1.731 | 1.890 | 2.059 | 1.974 | 2.250 | 1.890 | 2.059 | 1.974 | 2.250 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.649 | -0.648 | -0.952 | -1.041 | -1.131 | -1.084 | -1.363 | -1.041 | -1.131 | -1.084 | -1.363 | ns |
| | | $t_h$ | 0.778 | 0.777 | 1.128 | 1.239 | 1.349 | 1.292 | 1.568 | 1.239 | 1.349 | 1.292 | 1.568 | ns |
| | GCLK PLL | $t_{su}$ | -0.945 | -0.945 | -1.352 | -1.466 | -1.584 | -1.524 | -1.793 | -1.466 | -1.584 | -1.524 | -1.793 | ns |
| | | $t_h$ | 1.200 | 1.200 | 1.721 | 1.879 | 2.043 | 1.958 | 2.234 | 1.879 | 2.043 | 1.958 | 2.234 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -0.649 | -0.648 | -0.952 | -1.041 | -1.131 | -1.084 | -1.363 | -1.041 | -1.131 | -1.084 | -1.363 | ns |
| | | $t_h$ | 0.778 | 0.777 | 1.128 | 1.239 | 1.349 | 1.292 | 1.568 | 1.239 | 1.349 | 1.292 | 1.568 | ns |
| | GCLK PLL | $t_{su}$ | -0.945 | -0.945 | -1.352 | -1.466 | -1.584 | -1.524 | -1.793 | -1.466 | -1.584 | -1.524 | -1.793 | ns |
| | | $t_h$ | 1.200 | 1.200 | 1.721 | 1.879 | 2.043 | 1.958 | 2.234 | 1.879 | 2.043 | 1.958 | 2.234 | ns |

**Table 1–101.** EP3SE50 Column Pins Input Timing Parameters (Part 4 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V \| PCI-X | GCLK | $t_{su}$ | -0.754 | -0.753 | -1.062 | -1.167 | -1.373 | -1.328 | -1.604 | -1.167 | -1.373 | -1.328 | -1.604 | ns |
| | | $t_h$ | 0.881 | 0.880 | 1.240 | 1.368 | 1.594 | 1.537 | 1.814 | 1.368 | 1.594 | 1.537 | 1.814 | ns |
| | GCLK PLL | $t_{su}$ | -1.048 | -1.048 | -1.465 | -1.595 | -1.829 | -1.771 | -2.037 | -1.595 | -1.829 | -1.771 | -2.037 | ns |
| | | $t_h$ | 1.301 | 1.301 | 1.835 | 2.011 | 2.291 | 2.206 | 2.483 | 2.011 | 2.291 | 2.206 | 2.483 | ns |

Table 1–102 lists the EP3SE50 row pins input timing parameters for single-ended I/O standards.

**Table 1–102.** EP3SE50 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -0.896 | -0.926 | -1.311 | -1.433 | -1.658 | -1.605 | -1.896 | -1.451 | -1.663 | -1.612 | -1.927 | ns |
| | | $t_h$ | 1.009 | 1.052 | 1.597 | 1.816 | 1.931 | 1.813 | 1.843 | 1.809 | 1.936 | 1.818 | 1.895 | ns |
| | GCLK PLL | $t_{su}$ | 0.952 | 0.960 | 1.494 | 1.640 | 1.888 | 1.819 | 2.111 | 1.667 | 1.903 | 1.836 | 2.144 | ns |
| | | $t_h$ | -0.703 | -0.700 | -1.311 | -1.433 | -1.658 | -1.605 | -1.896 | -1.451 | -1.663 | -1.612 | -1.927 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -0.896 | -0.926 | -1.311 | -1.433 | -1.658 | -1.605 | -1.896 | -1.451 | -1.663 | -1.612 | -1.927 | ns |
| | | $t_h$ | 1.009 | 1.052 | 1.597 | 1.816 | 1.931 | 1.813 | 1.843 | 1.809 | 1.936 | 1.818 | 1.895 | ns |
| | GCLK PLL | $t_{su}$ | 0.952 | 0.960 | 1.494 | 1.640 | 1.888 | 1.819 | 2.111 | 1.667 | 1.903 | 1.836 | 2.144 | ns |
| | | $t_h$ | -0.703 | -0.700 | -1.308 | -1.434 | -1.661 | -1.608 | -1.899 | -1.450 | -1.668 | -1.617 | -1.932 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -0.902 | -0.937 | 1.491 | 1.641 | 1.891 | 1.822 | 2.114 | 1.666 | 1.908 | 1.841 | 2.149 | ns |
| | | $t_h$ | 1.015 | 1.063 | -1.308 | -1.434 | -1.661 | -1.608 | -1.899 | -1.450 | -1.668 | -1.617 | -1.932 | ns |
| | GCLK PLL | $t_{su}$ | 0.946 | 0.949 | 1.600 | 1.815 | 1.928 | 1.810 | 1.840 | 1.810 | 1.931 | 1.813 | 1.890 | ns |
| | | $t_h$ | -0.697 | -0.689 | 1.491 | 1.641 | 1.891 | 1.822 | 2.114 | 1.666 | 1.908 | 1.841 | 2.149 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -0.902 | -0.937 | 1.500 | 1.654 | 1.906 | 1.837 | 2.129 | 1.675 | 1.918 | 1.851 | 2.159 | ns |
| | | $t_h$ | 1.015 | 1.063 | -1.317 | -1.447 | -1.676 | -1.623 | -1.914 | -1.459 | -1.678 | -1.627 | -1.942 | ns |
| | GCLK PLL | $t_{su}$ | 0.946 | 0.949 | 1.591 | 1.802 | 1.913 | 1.795 | 1.825 | 1.801 | 1.921 | 1.803 | 1.880 | ns |
| | | $t_h$ | -0.697 | -0.689 | 1.500 | 1.654 | 1.906 | 1.837 | 2.129 | 1.675 | 1.918 | 1.851 | 2.159 | ns |
| 2.5 V | GCLK | $t_{su}$ | -0.890 | -0.930 | 1.510 | 1.730 | 1.876 | 1.758 | 1.788 | 1.729 | 1.881 | 1.762 | 1.840 | ns |
| | | $t_h$ | 1.003 | 1.056 | 1.458 | 1.596 | 1.807 | 1.742 | 2.015 | 1.614 | 1.817 | 1.754 | 2.048 | ns |
| | GCLK PLL | $t_{su}$ | 0.958 | 0.956 | -1.272 | -1.388 | -1.573 | -1.523 | -1.797 | -1.395 | -1.573 | -1.526 | -1.829 | ns |
| | | $t_h$ | -0.709 | -0.696 | 1.510 | 1.730 | 1.876 | 1.758 | 1.788 | 1.729 | 1.881 | 1.762 | 1.840 | ns |
| 1.8 V | GCLK | $t_{su}$ | -0.869 | -0.907 | 1.534 | 1.762 | 1.944 | 1.826 | 1.856 | 1.760 | 1.946 | 1.827 | 1.905 | ns |
| | | $t_h$ | 0.890 | 0.886 | 1.434 | 1.564 | 1.739 | 1.674 | 1.947 | 1.583 | 1.752 | 1.689 | 1.983 | ns |
| | GCLK PLL | $t_{su}$ | 0.986 | 1.035 | -1.248 | -1.356 | -1.505 | -1.455 | -1.729 | -1.364 | -1.508 | -1.461 | -1.764 | ns |
| | | $t_h$ | -0.859 | -0.896 | 1.613 | 1.863 | 2.103 | 1.985 | 2.015 | 1.856 | 2.101 | 1.982 | 2.060 | ns |

**Table 1–102.** EP3SE50 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5 V | GCLK | $t_{su}$ | 0.900 | 0.897 | 1.355 | 1.463 | 1.580 | 1.515 | 1.788 | 1.487 | 1.597 | 1.534 | 1.828 | ns |
| | | $t_h$ | 0.976 | 1.024 | -1.169 | -1.255 | -1.346 | -1.296 | -1.570 | -1.268 | -1.353 | -1.306 | -1.609 | ns |
| | GCLK PLL | $t_{su}$ | -0.799 | -0.843 | 1.677 | 1.911 | 2.133 | 2.015 | 2.045 | 1.913 | 2.138 | 2.020 | 2.097 | ns |
| | | $t_h$ | 0.960 | 0.950 | 1.414 | 1.545 | 1.686 | 1.617 | 1.909 | 1.563 | 1.701 | 1.634 | 1.942 | ns |
| 1.2 V | GCLK | $t_{su}$ | 0.916 | 0.971 | -1.131 | -1.230 | -1.344 | -1.293 | -1.568 | -1.239 | -1.349 | -1.300 | -1.604 | ns |
| | | $t_h$ | -0.833 | -0.872 | 1.651 | -1.230 | -1.344 | -1.293 | -1.568 | -1.239 | -1.349 | -1.300 | -1.604 | ns |
| | GCLK PLL | $t_{su}$ | 1.015 | 1.014 | 1.317 | 1.436 | 1.575 | 1.510 | 1.782 | 1.455 | 1.590 | 1.527 | 1.819 | ns |
| | | $t_h$ | 0.947 | 0.999 | -1.131 | 1.890 | 2.108 | 1.991 | 2.019 | 1.888 | 2.108 | 1.990 | 2.067 | ns |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -0.833 | -0.872 | 1.651 | 1.890 | 2.108 | 1.991 | 2.019 | 1.888 | 2.108 | 1.990 | 2.067 | ns |
| | | $t_h$ | 1.015 | 1.014 | 1.317 | -1.442 | -1.607 | -1.521 | -1.544 | -1.432 | -1.599 | -1.511 | -1.589 | ns |
| | GCLK PLL | $t_{su}$ | 0.947 | 0.999 | -1.131 | -1.230 | -1.344 | -1.293 | -1.568 | -1.239 | -1.349 | -1.300 | -1.604 | ns |
| | | $t_h$ | -0.773 | -0.808 | 1.651 | 1.436 | 1.575 | 1.510 | 1.782 | 1.455 | 1.590 | 1.527 | 1.819 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | 0.986 | 0.985 | 1.317 | 1.890 | 2.108 | 1.991 | 2.019 | 1.888 | 2.108 | 1.990 | 2.067 | ns |
| | | $t_h$ | 0.890 | 0.936 | -1.131 | -1.442 | -1.607 | -1.521 | -1.544 | -1.432 | -1.599 | -1.511 | -1.589 | ns |
| | GCLK PLL | $t_{su}$ | -0.773 | -0.808 | -1.267 | -1.220 | -1.326 | -1.275 | -1.550 | -1.228 | -1.332 | -1.283 | -1.587 | ns |
| | | $t_h$ | 0.986 | 0.985 | -1.118 | 1.426 | 1.557 | 1.492 | 1.764 | 1.444 | 1.573 | 1.510 | 1.802 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | 0.890 | 0.936 | 1.305 | 1.900 | 2.126 | 2.009 | 2.037 | 1.899 | 2.125 | 2.007 | 2.084 | ns |
| | | $t_h$ | -0.759 | -0.796 | 1.651 | 1.900 | 2.126 | 2.009 | 2.037 | 1.899 | 2.125 | 2.007 | 2.084 | ns |
| | GCLK PLL | $t_{su}$ | 1.000 | 0.997 | 1.317 | -1.452 | -1.625 | -1.539 | -1.562 | -1.443 | -1.616 | -1.528 | -1.606 | ns |
| | | $t_h$ | 0.876 | 0.924 | -1.131 | -1.220 | -1.326 | -1.275 | -1.550 | -1.228 | -1.332 | -1.283 | -1.587 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -0.773 | -0.808 | 1.651 | -1.442 | -1.607 | -1.521 | -1.544 | -1.432 | -1.599 | -1.511 | -1.589 | ns |
| | | $t_h$ | 0.986 | 0.985 | 1.317 | -1.230 | -1.344 | -1.293 | -1.568 | -1.239 | -1.349 | -1.300 | -1.604 | ns |
| | GCLK PLL | $t_{su}$ | 0.890 | 0.936 | -1.131 | 1.436 | 1.575 | 1.510 | 1.782 | 1.455 | 1.590 | 1.527 | 1.819 | ns |
| | | $t_h$ | -0.773 | -0.808 | -1.267 | 1.890 | 2.108 | 1.991 | 2.019 | 1.888 | 2.108 | 1.990 | 2.067 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | 0.986 | 0.985 | -1.118 | -1.442 | -1.607 | -1.521 | -1.544 | -1.432 | -1.599 | -1.511 | -1.589 | ns |
| | | $t_h$ | 0.890 | 0.936 | 1.305 | -1.230 | -1.344 | -1.293 | -1.568 | -1.239 | -1.349 | -1.300 | -1.604 | ns |
| | GCLK PLL | $t_{su}$ | -0.759 | -0.796 | 1.666 | 1.436 | 1.575 | 1.510 | 1.782 | 1.455 | 1.590 | 1.527 | 1.819 | ns |
| | | $t_h$ | 1.000 | 0.997 | -1.267 | 1.890 | 2.108 | 1.991 | 2.019 | 1.888 | 2.108 | 1.990 | 2.067 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | 0.876 | 0.924 | -1.118 | -1.442 | -1.607 | -1.521 | -1.544 | -1.432 | -1.599 | -1.511 | -1.589 | ns |
| | | $t_h$ | -0.759 | -0.796 | -1.276 | 1.900 | 2.126 | 2.009 | 2.037 | 1.899 | 2.125 | 2.007 | 2.084 | ns |
| | GCLK PLL | $t_{su}$ | 1.000 | 0.997 | -1.109 | -1.452 | -1.625 | -1.539 | -1.562 | -1.443 | -1.616 | -1.528 | -1.606 | ns |
| | | $t_h$ | 0.876 | 0.924 | 1.296 | -1.220 | -1.326 | -1.275 | -1.550 | -1.228 | -1.332 | -1.283 | -1.587 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.750 | -0.784 | 1.675 | 1.426 | 1.557 | 1.492 | 1.764 | 1.444 | 1.573 | 1.510 | 1.802 | ns |
| | | $t_h$ | 1.009 | 1.009 | -1.276 | 1.900 | 2.126 | 2.009 | 2.037 | 1.899 | 2.125 | 2.007 | 2.084 | ns |
| | GCLK PLL | $t_{su}$ | 0.867 | 0.912 | -1.109 | -1.452 | -1.625 | -1.539 | -1.562 | -1.443 | -1.616 | -1.528 | -1.606 | ns |
| | | $t_h$ | -0.750 | -0.784 | -1.276 | 1.910 | 2.142 | 2.025 | 2.053 | 1.908 | 2.141 | 2.023 | 2.100 | ns |

**Table 1–102.** EP3SE50 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | 1.009 | 1.009 | -1.308 | -1.462 | -1.641 | -1.555 | -1.578 | -1.452 | -1.632 | -1.544 | -1.622 | ns |
| | | $t_h$ | 0.867 | 0.912 | 1.600 | -1.210 | -1.310 | -1.259 | -1.534 | -1.219 | -1.316 | -1.267 | -1.571 | ns |
| | GCLK PLL | $t_{su}$ | -0.902 | -0.937 | 1.491 | 1.416 | 1.541 | 1.476 | 1.748 | 1.435 | 1.557 | 1.494 | 1.786 | ns |
| | | $t_h$ | 1.015 | 1.063 | -1.308 | 1.910 | 2.142 | 2.025 | 2.053 | 1.908 | 2.141 | 2.023 | 2.100 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | 0.946 | 0.949 | 1.600 | -1.462 | -1.641 | -1.555 | -1.578 | -1.452 | -1.632 | -1.544 | -1.622 | ns |
| | | $t_h$ | -0.697 | -0.689 | 1.491 | -1.210 | -1.310 | -1.259 | -1.534 | -1.219 | -1.316 | -1.267 | -1.571 | ns |
| | GCLK PLL | $t_{su}$ | -0.902 | -0.937 | 1.491 | 1.416 | 1.541 | 1.476 | 1.748 | 1.435 | 1.557 | 1.494 | 1.786 | ns |
| | | $t_h$ | 1.015 | 1.063 | 1.491 | 1.910 | 2.142 | 2.025 | 2.053 | 1.908 | 2.141 | 2.023 | 2.100 | ns |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | 0.946 | 0.949 | 1.491 | -1.462 | -1.641 | -1.555 | -1.578 | -1.452 | -1.632 | -1.544 | -1.622 | ns |
| | | $t_h$ | -0.697 | -0.689 | 1.491 | -1.210 | -1.310 | -1.259 | -1.534 | -1.219 | -1.316 | -1.267 | -1.571 | ns |
| | GCLK PLL | $t_{su}$ | -0.896 | -0.926 | -1.311 | -1.433 | -1.658 | -1.605 | -1.896 | -1.451 | -1.663 | -1.612 | -1.927 | ns |
| | | $t_h$ | 1.009 | 1.052 | 1.597 | 1.816 | 1.931 | 1.813 | 1.843 | 1.809 | 1.936 | 1.818 | 1.895 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | 0.952 | 0.960 | 1.494 | 1.640 | 1.888 | 1.819 | 2.111 | 1.667 | 1.903 | 1.836 | 2.144 | ns |
| | | $t_h$ | -0.703 | -0.700 | -1.311 | -1.433 | -1.658 | -1.605 | -1.896 | -1.451 | -1.663 | -1.612 | -1.927 | ns |
| | GCLK PLL | $t_{su}$ | -0.896 | -0.926 | -1.311 | -1.433 | -1.658 | -1.605 | -1.896 | -1.451 | -1.663 | -1.612 | -1.927 | ns |
| | | $t_h$ | 1.009 | 1.052 | 1.597 | 1.816 | 1.931 | 1.813 | 1.843 | 1.809 | 1.936 | 1.818 | 1.895 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | 0.952 | 0.960 | 1.494 | 1.640 | 1.888 | 1.819 | 2.111 | 1.667 | 1.903 | 1.836 | 2.144 | ns |
| | | $t_h$ | -0.703 | -0.700 | -1.308 | -1.434 | -1.661 | -1.608 | -1.899 | -1.450 | -1.668 | -1.617 | -1.932 | ns |
| | GCLK PLL | $t_{su}$ | -0.902 | -0.937 | 1.491 | 1.641 | 1.891 | 1.822 | 2.114 | 1.666 | 1.908 | 1.841 | 2.149 | ns |
| | | $t_h$ | 1.015 | 1.063 | -1.308 | -1.434 | -1.661 | -1.608 | -1.899 | -1.450 | -1.668 | -1.617 | -1.932 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | 0.946 | 0.949 | 1.600 | 1.815 | 1.928 | 1.810 | 1.840 | 1.810 | 1.931 | 1.813 | 1.890 | ns |
| | | $t_h$ | -0.697 | -0.689 | 1.491 | 1.641 | 1.891 | 1.822 | 2.114 | 1.666 | 1.908 | 1.841 | 2.149 | ns |
| | GCLK PLL | $t_{su}$ | -0.902 | -0.937 | 1.500 | 1.654 | 1.906 | 1.837 | 2.129 | 1.675 | 1.918 | 1.851 | 2.159 | ns |
| | | $t_h$ | 1.015 | 1.063 | -1.317 | -1.447 | -1.676 | -1.623 | -1.914 | -1.459 | -1.678 | -1.627 | -1.942 | ns |

Table 1–103 lists the EP3SE50 column pins output timing parameters for single-ended I/O standards.

**Table 1–103.** EP3SE50 Column Pins Output Timing Parameters (Part 1 of 6)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.293 | 3.293 | 4.559 | 4.925 | 5.402 | 5.282 | 5.365 | 4.925 | 5.402 | 5.282 | 5.365 | ns |
| | | GCLK PLL | $t_{co}$ | 3.550 | 3.524 | 4.903 | 5.329 | 5.819 | 5.674 | 5.973 | 5.329 | 5.819 | 5.674 | 5.973 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.176 | 3.176 | 4.405 | 4.763 | 5.232 | 5.112 | 5.252 | 4.763 | 5.232 | 5.112 | 5.252 | ns |
| | | GCLK PLL | $t_{co}$ | 3.483 | 3.457 | 4.794 | 5.218 | 5.706 | 5.561 | 5.860 | 5.218 | 5.706 | 5.561 | 5.860 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.081 | 3.081 | 4.268 | 4.620 | 5.080 | 4.960 | 5.162 | 4.620 | 5.080 | 4.960 | 5.162 | ns |
| | | GCLK PLL | $t_{co}$ | 3.397 | 3.371 | 4.691 | 5.120 | 5.614 | 5.469 | 5.768 | 5.120 | 5.614 | 5.469 | 5.768 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.041 | 3.051 | 4.243 | 4.596 | 5.055 | 4.935 | 5.120 | 4.596 | 5.055 | 4.935 | 5.120 | ns |
| | | GCLK PLL | $t_{co}$ | 3.390 | 3.364 | 4.674 | 5.092 | 5.573 | 5.428 | 5.727 | 5.092 | 5.573 | 5.428 | 5.727 | ns |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.296 | 3.296 | 4.563 | 4.937 | 5.416 | 5.296 | 5.373 | 4.937 | 5.416 | 5.296 | 5.373 | ns |
| | | GCLK PLL | $t_{co}$ | 3.556 | 3.530 | 4.908 | 5.334 | 5.826 | 5.681 | 5.980 | 5.334 | 5.826 | 5.681 | 5.980 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.096 | 3.096 | 4.273 | 4.625 | 5.086 | 4.966 | 5.172 | 4.625 | 5.086 | 4.966 | 5.172 | ns |
| | | GCLK PLL | $t_{co}$ | 3.401 | 3.375 | 4.701 | 5.137 | 5.625 | 5.480 | 5.779 | 5.137 | 5.625 | 5.480 | 5.779 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.059 | 3.069 | 4.236 | 4.594 | 5.055 | 4.935 | 5.148 | 4.594 | 5.055 | 4.935 | 5.148 | ns |
| | | GCLK PLL | $t_{co}$ | 3.408 | 3.382 | 4.695 | 5.116 | 5.599 | 5.454 | 5.753 | 5.116 | 5.599 | 5.454 | 5.753 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.043 | 3.053 | 4.212 | 4.553 | 5.025 | 4.904 | 5.119 | 4.553 | 5.025 | 4.904 | 5.119 | ns |
| | | GCLK PLL | $t_{co}$ | 3.392 | 3.366 | 4.672 | 5.090 | 5.570 | 5.425 | 5.724 | 5.090 | 5.570 | 5.425 | 5.724 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.238 | 3.238 | 4.508 | 4.876 | 5.367 | 5.247 | 5.356 | 4.876 | 5.367 | 5.247 | 5.356 | ns |
| | | GCLK PLL | $t_{co}$ | 3.514 | 3.488 | 4.870 | 5.298 | 5.786 | 5.641 | 5.940 | 5.298 | 5.786 | 5.641 | 5.940 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.108 | 3.108 | 4.339 | 4.704 | 5.205 | 5.086 | 5.239 | 4.704 | 5.205 | 5.086 | 5.239 | ns |
| | | GCLK PLL | $t_{co}$ | 3.403 | 3.377 | 4.740 | 5.164 | 5.648 | 5.504 | 5.801 | 5.164 | 5.648 | 5.504 | 5.801 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.033 | 3.033 | 4.250 | 4.605 | 5.103 | 4.984 | 5.175 | 4.605 | 5.103 | 4.984 | 5.175 | ns |
| | | GCLK PLL | $t_{co}$ | 3.367 | 3.341 | 4.677 | 5.095 | 5.574 | 5.430 | 5.728 | 5.095 | 5.574 | 5.430 | 5.728 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.000 | 3.010 | 4.188 | 4.536 | 5.053 | 4.934 | 5.152 | 4.536 | 5.053 | 4.934 | 5.152 | ns |
| | | GCLK PLL | $t_{co}$ | 3.349 | 3.323 | 4.648 | 5.067 | 5.546 | 5.401 | 5.700 | 5.067 | 5.546 | 5.401 | 5.700 | ns |


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**Table 1–103.** EP3SE50 Column Pins Output Timing Parameters (Part 2 of 6)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.146 | 3.146 | 4.397 | 4.757 | 5.259 | 5.140 | 5.275 | 4.757 | 5.259 | 5.140 | 5.275 | ns |
| | | GCLK PLL | $t_{co}$ | 3.428 | 3.402 | 4.774 | 5.197 | 5.683 | 5.539 | 5.836 | 5.197 | 5.683 | 5.539 | 5.836 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.009 | 3.010 | 4.202 | 4.558 | 5.077 | 4.958 | 5.165 | 4.558 | 5.077 | 4.958 | 5.165 | ns |
| | | GCLK PLL | $t_{co}$ | 3.349 | 3.323 | 4.651 | 5.068 | 5.548 | 5.404 | 5.701 | 5.068 | 5.548 | 5.404 | 5.701 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.995 | 3.005 | 4.183 | 4.524 | 5.009 | 4.889 | 5.134 | 4.524 | 5.009 | 4.889 | 5.134 | ns |
| | | GCLK PLL | $t_{co}$ | 3.344 | 3.318 | 4.643 | 5.061 | 5.540 | 5.395 | 5.694 | 5.061 | 5.540 | 5.395 | 5.694 | ns |
| | 16mA | GCLK | $t_{co}$ | 2.986 | 2.996 | 4.169 | 4.509 | 5.007 | 4.888 | 5.139 | 4.509 | 5.007 | 4.888 | 5.139 | ns |
| | | GCLK PLL | $t_{co}$ | 3.335 | 3.309 | 4.629 | 5.046 | 5.525 | 5.380 | 5.679 | 5.046 | 5.525 | 5.380 | 5.679 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.293 | 3.293 | 4.651 | 5.036 | 5.541 | 5.422 | 5.483 | 5.036 | 5.541 | 5.422 | 5.483 | ns |
| | | GCLK PLL | $t_{co}$ | 3.550 | 3.524 | 4.981 | 5.424 | 5.930 | 5.786 | 6.084 | 5.424 | 5.930 | 5.786 | 6.084 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.168 | 3.168 | 4.478 | 4.852 | 5.344 | 5.225 | 5.359 | 4.852 | 5.344 | 5.225 | 5.359 | ns |
| | | GCLK PLL | $t_{co}$ | 3.450 | 3.424 | 4.862 | 5.298 | 5.798 | 5.654 | 5.951 | 5.298 | 5.798 | 5.654 | 5.951 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.068 | 3.068 | 4.349 | 4.716 | 5.204 | 5.085 | 5.281 | 4.716 | 5.204 | 5.085 | 5.281 | ns |
| | | GCLK PLL | $t_{co}$ | 3.406 | 3.380 | 4.775 | 5.208 | 5.703 | 5.558 | 5.857 | 5.208 | 5.703 | 5.558 | 5.857 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.041 | 3.041 | 4.280 | 4.649 | 5.154 | 5.035 | 5.224 | 4.649 | 5.154 | 5.035 | 5.224 | ns |
| | | GCLK PLL | $t_{co}$ | 3.368 | 3.342 | 4.736 | 5.165 | 5.660 | 5.515 | 5.814 | 5.165 | 5.660 | 5.515 | 5.814 | ns |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.556 | 3.556 | 5.088 | 5.519 | 6.078 | 5.958 | 5.880 | 5.519 | 6.078 | 5.958 | 5.880 | ns |
| | | GCLK PLL | $t_{co}$ | 3.741 | 3.715 | 5.303 | 5.784 | 6.335 | 6.190 | 6.489 | 5.784 | 6.335 | 6.190 | 6.489 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.315 | 3.315 | 4.728 | 5.113 | 5.617 | 5.498 | 5.549 | 5.113 | 5.617 | 5.498 | 5.549 | ns |
| | | GCLK PLL | $t_{co}$ | 3.560 | 3.534 | 5.024 | 5.475 | 5.987 | 5.843 | 6.140 | 5.475 | 5.987 | 5.843 | 6.140 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.197 | 3.197 | 4.538 | 4.923 | 5.443 | 5.323 | 5.437 | 4.923 | 5.443 | 5.323 | 5.437 | ns |
| | | GCLK PLL | $t_{co}$ | 3.478 | 3.452 | 4.917 | 5.360 | 5.877 | 5.732 | 6.031 | 5.360 | 5.877 | 5.732 | 6.031 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.143 | 3.143 | 4.438 | 4.825 | 5.331 | 5.211 | 5.360 | 4.825 | 5.331 | 5.211 | 5.360 | ns |
| | | GCLK PLL | $t_{co}$ | 3.458 | 3.432 | 4.858 | 5.307 | 5.811 | 5.666 | 5.965 | 5.307 | 5.811 | 5.666 | 5.965 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.075 | 3.075 | 4.342 | 4.727 | 5.217 | 5.097 | 5.291 | 4.727 | 5.217 | 5.097 | 5.291 | ns |
| | | GCLK PLL | $t_{co}$ | 3.395 | 3.369 | 4.797 | 5.232 | 5.730 | 5.585 | 5.884 | 5.232 | 5.730 | 5.585 | 5.884 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.051 | 3.051 | 4.317 | 4.680 | 5.179 | 5.059 | 5.258 | 4.680 | 5.179 | 5.059 | 5.258 | ns |
| | | GCLK PLL | $t_{co}$ | 3.377 | 3.351 | 4.777 | 5.210 | 5.707 | 5.562 | 5.861 | 5.210 | 5.707 | 5.562 | 5.861 | ns |

**Table 1–103.** EP3SE50 Column Pins Output Timing Parameters (Part 3 of 6)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.464 | 3.464 | 4.981 | 5.429 | 5.995 | 5.875 | 5.825 | 5.429 | 5.995 | 5.875 | 5.825 | ns |
| | | GCLK PLL | $t_{co}$ | 3.687 | 3.661 | 5.231 | 5.717 | 6.273 | 6.128 | 6.427 | 5.717 | 6.273 | 6.128 | 6.427 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.181 | 3.181 | 4.527 | 4.916 | 5.439 | 5.319 | 5.439 | 4.916 | 5.439 | 5.319 | 5.439 | ns |
| | | GCLK PLL | $t_{co}$ | 3.475 | 3.449 | 4.912 | 5.360 | 5.881 | 5.736 | 6.035 | 5.360 | 5.881 | 5.736 | 6.035 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.103 | 3.111 | 4.427 | 4.808 | 5.322 | 5.202 | 5.362 | 4.808 | 5.322 | 5.202 | 5.362 | ns |
| | | GCLK PLL | $t_{co}$ | 3.450 | 3.424 | 4.845 | 5.300 | 5.814 | 5.669 | 5.968 | 5.300 | 5.814 | 5.669 | 5.968 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.093 | 3.100 | 4.409 | 4.787 | 5.290 | 5.170 | 5.345 | 4.787 | 5.290 | 5.170 | 5.345 | ns |
| | | GCLK PLL | $t_{co}$ | 3.439 | 3.413 | 4.828 | 5.275 | 5.794 | 5.649 | 5.948 | 5.275 | 5.794 | 5.649 | 5.948 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.063 | 3.063 | 4.330 | 4.709 | 5.208 | 5.088 | 5.282 | 4.709 | 5.208 | 5.088 | 5.282 | ns |
| | | GCLK PLL | $t_{co}$ | 3.384 | 3.358 | 4.790 | 5.225 | 5.724 | 5.579 | 5.878 | 5.225 | 5.724 | 5.579 | 5.878 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.030 | 3.040 | 4.314 | 4.676 | 5.168 | 5.047 | 5.261 | 4.676 | 5.168 | 5.047 | 5.261 | ns |
| | | GCLK PLL | $t_{co}$ | 3.379 | 3.353 | 4.774 | 5.213 | 5.713 | 5.568 | 5.867 | 5.213 | 5.713 | 5.568 | 5.867 | ns |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.354 | 3.354 | 4.868 | 5.328 | 5.915 | 5.795 | 5.765 | 5.328 | 5.915 | 5.795 | 5.765 | ns |
| | | GCLK PLL | $t_{co}$ | 3.603 | 3.577 | 5.157 | 5.652 | 6.217 | 6.072 | 6.371 | 5.652 | 6.217 | 6.072 | 6.371 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.181 | 3.181 | 4.546 | 4.947 | 5.486 | 5.366 | 5.480 | 4.947 | 5.486 | 5.366 | 5.480 | ns |
| | | GCLK PLL | $t_{co}$ | 3.480 | 3.454 | 4.932 | 5.391 | 5.931 | 5.786 | 6.085 | 5.391 | 5.931 | 5.786 | 6.085 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.094 | 3.103 | 4.419 | 4.806 | 5.331 | 5.211 | 5.366 | 4.806 | 5.331 | 5.211 | 5.366 | ns |
| | | GCLK PLL | $t_{co}$ | 3.442 | 3.416 | 4.839 | 5.301 | 5.818 | 5.673 | 5.972 | 5.301 | 5.818 | 5.673 | 5.972 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.070 | 3.070 | 4.351 | 4.746 | 5.240 | 5.120 | 5.319 | 4.746 | 5.240 | 5.120 | 5.319 | ns |
| | | GCLK PLL | $t_{co}$ | 3.395 | 3.369 | 4.811 | 5.252 | 5.762 | 5.617 | 5.916 | 5.252 | 5.762 | 5.617 | 5.916 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.058 | 3.058 | 4.312 | 4.677 | 5.188 | 5.068 | 5.276 | 4.677 | 5.188 | 5.068 | 5.276 | ns |
| | | GCLK PLL | $t_{co}$ | 3.395 | 3.369 | 4.768 | 5.200 | 5.693 | 5.548 | 5.847 | 5.200 | 5.693 | 5.548 | 5.847 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.055 | 3.055 | 4.305 | 4.670 | 5.193 | 5.074 | 5.271 | 4.670 | 5.193 | 5.074 | 5.271 | ns |
| | | GCLK PLL | $t_{co}$ | 3.392 | 3.366 | 4.765 | 5.196 | 5.689 | 5.544 | 5.843 | 5.196 | 5.689 | 5.544 | 5.843 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.043 | 3.051 | 4.305 | 4.666 | 5.174 | 5.054 | 5.272 | 4.666 | 5.174 | 5.054 | 5.272 | ns |
| | | GCLK PLL | $t_{co}$ | 3.390 | 3.364 | 4.765 | 5.197 | 5.690 | 5.545 | 5.844 | 5.197 | 5.690 | 5.545 | 5.844 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.032 | 3.042 | 4.291 | 4.644 | 5.140 | 5.020 | 5.256 | 4.644 | 5.140 | 5.020 | 5.256 | ns |
| | | GCLK PLL | $t_{co}$ | 3.381 | 3.355 | 4.751 | 5.182 | 5.675 | 5.530 | 5.829 | 5.182 | 5.675 | 5.530 | 5.829 | ns |

**Table 1–103.** EP3SE50 Column Pins Output Timing Parameters (Part 4 of 6)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.074 | 3.074 | 4.324 | 4.692 | 5.215 | 5.096 | 5.295 | 4.692 | 5.215 | 5.096 | 5.295 | ns |
| | | GCLK PLL | $t_{co}$ | 3.402 | 3.376 | 4.780 | 5.214 | 5.709 | 5.564 | 5.863 | 5.214 | 5.709 | 5.564 | 5.863 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.057 | 3.059 | 4.321 | 4.689 | 5.205 | 5.085 | 5.293 | 4.689 | 5.205 | 5.085 | 5.293 | ns |
| | | GCLK PLL | $t_{co}$ | 3.398 | 3.372 | 4.778 | 5.212 | 5.707 | 5.562 | 5.861 | 5.212 | 5.707 | 5.562 | 5.861 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.045 | 3.048 | 4.308 | 4.669 | 5.197 | 5.078 | 5.291 | 4.669 | 5.197 | 5.078 | 5.291 | ns |
| | | GCLK PLL | $t_{co}$ | 3.387 | 3.361 | 4.768 | 5.202 | 5.698 | 5.553 | 5.852 | 5.202 | 5.698 | 5.553 | 5.852 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.027 | 3.037 | 4.296 | 4.652 | 5.159 | 5.039 | 5.266 | 4.652 | 5.159 | 5.039 | 5.266 | ns |
| | | GCLK PLL | $t_{co}$ | 3.376 | 3.350 | 4.756 | 5.189 | 5.685 | 5.540 | 5.839 | 5.189 | 5.685 | 5.540 | 5.839 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.027 | 3.037 | 4.295 | 4.652 | 5.159 | 5.039 | 5.265 | 4.652 | 5.159 | 5.039 | 5.265 | ns |
| | | GCLK PLL | $t_{co}$ | 3.376 | 3.350 | 4.755 | 5.189 | 5.685 | 5.540 | 5.839 | 5.189 | 5.685 | 5.540 | 5.839 | ns |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.033 | 3.043 | 4.294 | 4.649 | 5.159 | 5.039 | 5.268 | 4.649 | 5.159 | 5.039 | 5.268 | ns |
| | | GCLK PLL | $t_{co}$ | 3.382 | 3.356 | 4.754 | 5.186 | 5.680 | 5.535 | 5.834 | 5.186 | 5.680 | 5.535 | 5.834 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.036 | 3.046 | 4.302 | 4.658 | 5.164 | 5.044 | 5.291 | 4.658 | 5.164 | 5.044 | 5.291 | ns |
| | | GCLK PLL | $t_{co}$ | 3.385 | 3.359 | 4.762 | 5.196 | 5.692 | 5.547 | 5.846 | 5.196 | 5.692 | 5.547 | 5.846 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.068 | 3.068 | 4.338 | 4.709 | 5.230 | 5.110 | 5.310 | 4.709 | 5.230 | 5.110 | 5.310 | ns |
| | | GCLK PLL | $t_{co}$ | 3.406 | 3.380 | 4.790 | 5.225 | 5.722 | 5.577 | 5.876 | 5.225 | 5.722 | 5.577 | 5.876 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.043 | 3.053 | 4.319 | 4.688 | 5.204 | 5.084 | 5.296 | 4.688 | 5.204 | 5.084 | 5.296 | ns |
| | | GCLK PLL | $t_{co}$ | 3.392 | 3.366 | 4.779 | 5.215 | 5.713 | 5.568 | 5.867 | 5.215 | 5.713 | 5.568 | 5.867 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.032 | 3.042 | 4.306 | 4.667 | 5.180 | 5.060 | 5.281 | 4.667 | 5.180 | 5.060 | 5.281 | ns |
| | | GCLK PLL | $t_{co}$ | 3.381 | 3.355 | 4.766 | 5.201 | 5.699 | 5.554 | 5.853 | 5.201 | 5.699 | 5.554 | 5.853 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.031 | 3.041 | 4.309 | 4.667 | 5.169 | 5.049 | 5.278 | 4.667 | 5.169 | 5.049 | 5.278 | ns |
| | | GCLK PLL | $t_{co}$ | 3.380 | 3.354 | 4.769 | 5.205 | 5.703 | 5.558 | 5.857 | 5.205 | 5.703 | 5.558 | 5.857 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.028 | 3.038 | 4.303 | 4.662 | 5.159 | 5.039 | 5.272 | 4.662 | 5.159 | 5.039 | 5.272 | ns |
| | | GCLK PLL | $t_{co}$ | 3.377 | 3.351 | 4.763 | 5.199 | 5.697 | 5.552 | 5.851 | 5.199 | 5.697 | 5.552 | 5.851 | ns |
| SSTL-15 CLASS II | 8mA | GCLK | $t_{co}$ | 3.030 | 3.040 | 4.292 | 4.648 | 5.159 | 5.039 | 5.269 | 4.648 | 5.159 | 5.039 | 5.269 | ns |
| | | GCLK PLL | $t_{co}$ | 3.379 | 3.353 | 4.752 | 5.185 | 5.680 | 5.535 | 5.834 | 5.185 | 5.680 | 5.535 | 5.834 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.033 | 3.043 | 4.299 | 4.657 | 5.165 | 5.045 | 5.293 | 4.657 | 5.165 | 5.045 | 5.293 | ns |
| | | GCLK PLL | $t_{co}$ | 3.382 | 3.356 | 4.759 | 5.194 | 5.691 | 5.546 | 5.845 | 5.194 | 5.691 | 5.546 | 5.845 | ns |

**Table 1–103.** EP3SE50 Column Pins Output Timing Parameters (Part 5 of 6)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.042 | 3.050 | 4.294 | 4.654 | 5.173 | 5.053 | 5.270 | 4.654 | 5.173 | 5.053 | 5.270 | ns |
| | | GCLK PLL | $t_{co}$ | 3.389 | 3.363 | 4.754 | 5.185 | 5.678 | 5.533 | 5.832 | 5.185 | 5.678 | 5.533 | 5.832 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.033 | 3.043 | 4.292 | 4.646 | 5.169 | 5.050 | 5.275 | 4.646 | 5.169 | 5.050 | 5.275 | ns |
| | | GCLK PLL | $t_{co}$ | 3.382 | 3.356 | 4.752 | 5.184 | 5.677 | 5.532 | 5.831 | 5.184 | 5.677 | 5.532 | 5.831 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.025 | 3.035 | 4.285 | 4.639 | 5.142 | 5.023 | 5.257 | 4.639 | 5.142 | 5.023 | 5.257 | ns |
| | | GCLK PLL | $t_{co}$ | 3.374 | 3.348 | 4.745 | 5.176 | 5.670 | 5.525 | 5.824 | 5.176 | 5.670 | 5.525 | 5.824 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.028 | 3.038 | 4.288 | 4.642 | 5.145 | 5.025 | 5.260 | 4.642 | 5.145 | 5.025 | 5.260 | ns |
| | | GCLK PLL | $t_{co}$ | 3.377 | 3.351 | 4.748 | 5.180 | 5.674 | 5.529 | 5.828 | 5.180 | 5.674 | 5.529 | 5.828 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.025 | 3.035 | 4.290 | 4.646 | 5.144 | 5.025 | 5.267 | 4.646 | 5.144 | 5.025 | 5.267 | ns |
| | | GCLK PLL | $t_{co}$ | 3.374 | 3.348 | 4.750 | 5.183 | 5.678 | 5.533 | 5.832 | 5.183 | 5.678 | 5.533 | 5.832 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.033 | 3.043 | 4.289 | 4.643 | 5.141 | 5.021 | 5.271 | 4.643 | 5.141 | 5.021 | 5.271 | ns |
| | | GCLK PLL | $t_{co}$ | 3.382 | 3.356 | 4.749 | 5.181 | 5.674 | 5.529 | 5.828 | 5.181 | 5.674 | 5.529 | 5.828 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.048 | 3.055 | 4.303 | 4.667 | 5.189 | 5.069 | 5.283 | 4.667 | 5.189 | 5.069 | 5.283 | ns |
| | | GCLK PLL | $t_{co}$ | 3.394 | 3.368 | 4.763 | 5.195 | 5.689 | 5.544 | 5.843 | 5.195 | 5.689 | 5.544 | 5.843 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.041 | 3.051 | 4.304 | 4.662 | 5.178 | 5.058 | 5.280 | 4.662 | 5.178 | 5.058 | 5.280 | ns |
| | | GCLK PLL | $t_{co}$ | 3.390 | 3.364 | 4.764 | 5.197 | 5.692 | 5.547 | 5.846 | 5.197 | 5.692 | 5.547 | 5.846 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.037 | 3.047 | 4.299 | 4.655 | 5.172 | 5.052 | 5.275 | 4.655 | 5.172 | 5.052 | 5.275 | ns |
| | | GCLK PLL | $t_{co}$ | 3.386 | 3.360 | 4.759 | 5.192 | 5.687 | 5.542 | 5.841 | 5.192 | 5.687 | 5.542 | 5.841 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.030 | 3.040 | 4.292 | 4.648 | 5.159 | 5.039 | 5.269 | 4.648 | 5.159 | 5.039 | 5.269 | ns |
| | | GCLK PLL | $t_{co}$ | 3.379 | 3.353 | 4.752 | 5.185 | 5.680 | 5.535 | 5.834 | 5.185 | 5.680 | 5.535 | 5.834 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.031 | 3.041 | 4.299 | 4.656 | 5.155 | 5.035 | 5.272 | 4.656 | 5.155 | 5.035 | 5.272 | ns |
| | | GCLK PLL | $t_{co}$ | 3.380 | 3.354 | 4.759 | 5.193 | 5.690 | 5.545 | 5.844 | 5.193 | 5.690 | 5.545 | 5.844 | ns |
| 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.029 | 3.039 | 4.280 | 4.634 | 5.134 | 5.014 | 5.257 | 4.634 | 5.134 | 5.014 | 5.257 | ns |
| | | GCLK PLL | $t_{co}$ | 3.378 | 3.352 | 4.740 | 5.171 | 5.664 | 5.519 | 5.818 | 5.171 | 5.664 | 5.519 | 5.818 | ns |


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**Table 1–103.** EP3SE50 Column Pins Output Timing Parameters (Part 6 of 6)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.048 | 3.058 | 4.317 | 4.683 | 5.208 | 5.088 | 5.302 | 4.683 | 5.208 | 5.088 | 5.302 | ns |
| | | GCLK PLL | $t_{co}$ | 3.397 | 3.371 | 4.777 | 5.212 | 5.710 | 5.565 | 5.864 | 5.212 | 5.710 | 5.565 | 5.864 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.040 | 3.050 | 4.308 | 4.668 | 5.191 | 5.071 | 5.290 | 4.668 | 5.191 | 5.071 | 5.290 | ns |
| | | GCLK PLL | $t_{co}$ | 3.389 | 3.363 | 4.768 | 5.203 | 5.701 | 5.556 | 5.855 | 5.203 | 5.701 | 5.556 | 5.855 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.041 | 3.051 | 4.315 | 4.674 | 5.187 | 5.067 | 5.293 | 4.674 | 5.187 | 5.067 | 5.293 | ns |
| | | GCLK PLL | $t_{co}$ | 3.390 | 3.364 | 4.775 | 5.212 | 5.710 | 5.565 | 5.864 | 5.212 | 5.710 | 5.565 | 5.864 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.030 | 3.040 | 4.302 | 4.661 | 5.164 | 5.044 | 5.287 | 4.661 | 5.164 | 5.044 | 5.287 | ns |
| | | GCLK PLL | $t_{co}$ | 3.379 | 3.353 | 4.762 | 5.198 | 5.696 | 5.551 | 5.850 | 5.198 | 5.696 | 5.551 | 5.850 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.030 | 3.040 | 4.302 | 4.661 | 5.165 | 5.045 | 5.279 | 4.661 | 5.165 | 5.045 | 5.279 | ns |
| | | GCLK PLL | $t_{co}$ | 3.379 | 3.353 | 4.762 | 5.198 | 5.697 | 5.552 | 5.851 | 5.198 | 5.697 | 5.552 | 5.851 | ns |
| 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.061 | 3.061 | 4.318 | 4.685 | 5.243 | 5.123 | 5.316 | 4.685 | 5.243 | 5.123 | 5.316 | ns |
| | | GCLK PLL | $t_{co}$ | 3.400 | 3.374 | 4.778 | 5.213 | 5.710 | 5.565 | 5.864 | 5.213 | 5.710 | 5.565 | 5.864 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.154 | 3.164 | 4.363 | 4.710 | 5.218 | 5.098 | 5.347 | 4.710 | 5.218 | 5.098 | 5.347 | ns |
| | | GCLK PLL | $t_{co}$ | 3.503 | 3.477 | 4.823 | 5.247 | 5.735 | 5.590 | 5.889 | 5.247 | 5.735 | 5.590 | 5.889 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.154 | 3.164 | 4.363 | 4.710 | 5.218 | 5.098 | 5.347 | 4.710 | 5.218 | 5.098 | 5.347 | ns |
| | | GCLK PLL | $t_{co}$ | 3.503 | 3.477 | 4.823 | 5.247 | 5.735 | 5.590 | 5.889 | 5.247 | 5.735 | 5.590 | 5.889 | ns |

Table 1–104 lists the EP3SE50 row pins output timing parameters for single-ended I/O standards.

**Table 1–104.** EP3SE50 Row Pins Output Timing Parameters (Part 1 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.161 | 3.395 | 4.722 | 5.117 | 5.622 | 5.486 | 5.755 | 5.247 | 5.754 | 5.618 | 5.832 | ns |
| | | GCLK PLL | $t_{co}$ | 1.488 | 1.692 | 2.101 | 2.185 | 2.381 | 2.400 | 2.349 | 2.304 | 2.505 | 2.523 | 2.344 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.095 | 3.324 | 4.612 | 5.005 | 5.508 | 5.372 | 5.611 | 5.134 | 5.638 | 5.502 | 5.683 | ns |
| | | GCLK PLL | $t_{co}$ | 1.395 | 1.587 | 1.971 | 2.047 | 2.237 | 2.256 | 2.205 | 2.163 | 2.356 | 2.374 | 2.195 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.016 | 3.235 | 4.506 | 4.905 | 5.412 | 5.276 | 5.483 | 5.035 | 5.539 | 5.403 | 5.551 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.493 | 1.852 | 1.924 | 2.109 | 2.128 | 2.077 | 2.036 | 2.224 | 2.242 | 2.063 | ns |

**Table 1–104.** EP3SE50 Row Pins Output Timing Parameters (Part 2 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.163 | 3.402 | 4.726 | 5.122 | 5.631 | 5.495 | 5.760 | 5.255 | 5.766 | 5.630 | 5.837 | ns |
| | | GCLK PLL | $t_{co}$ | 1.498 | 1.696 | 2.109 | 2.190 | 2.386 | 2.405 | 2.354 | 2.310 | 2.510 | 2.528 | 2.349 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.020 | 3.239 | 4.517 | 4.920 | 5.422 | 5.286 | 5.489 | 5.047 | 5.548 | 5.412 | 5.558 | ns |
| | | GCLK PLL | $t_{co}$ | 1.318 | 1.497 | 1.858 | 1.930 | 2.115 | 2.134 | 2.083 | 2.042 | 2.231 | 2.249 | 2.070 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.122 | 3.356 | 4.689 | 5.085 | 5.588 | 5.452 | 5.712 | 5.215 | 5.720 | 5.584 | 5.790 | ns |
| | | GCLK PLL | $t_{co}$ | 1.442 | 1.638 | 2.053 | 2.138 | 2.338 | 2.357 | 2.306 | 2.261 | 2.463 | 2.481 | 2.302 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.021 | 3.244 | 4.552 | 4.943 | 5.443 | 5.307 | 5.548 | 5.073 | 5.575 | 5.438 | 5.625 | ns |
| | | GCLK PLL | $t_{co}$ | 1.319 | 1.511 | 1.900 | 1.979 | 2.174 | 2.193 | 2.142 | 2.099 | 2.299 | 2.316 | 2.137 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.984 | 3.206 | 4.492 | 4.878 | 5.373 | 5.237 | 5.460 | 5.005 | 5.501 | 5.365 | 5.532 | ns |
| | | GCLK PLL | $t_{co}$ | 1.282 | 1.464 | 1.818 | 1.896 | 2.086 | 2.105 | 2.054 | 2.013 | 2.206 | 2.223 | 2.044 | ns |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.043 | 3.268 | 4.587 | 4.978 | 5.479 | 5.343 | 5.601 | 5.107 | 5.611 | 5.474 | 5.678 | ns |
| | | GCLK PLL | $t_{co}$ | 1.356 | 1.557 | 1.947 | 2.031 | 2.227 | 2.246 | 2.195 | 2.153 | 2.352 | 2.369 | 2.190 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.971 | 3.190 | 4.464 | 4.849 | 5.345 | 5.209 | 5.421 | 4.975 | 5.473 | 5.336 | 5.492 | ns |
| | | GCLK PLL | $t_{co}$ | 1.269 | 1.448 | 1.783 | 1.857 | 2.047 | 2.066 | 2.015 | 1.973 | 2.166 | 2.183 | 2.004 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.148 | 3.393 | 4.797 | 5.211 | 5.733 | 5.597 | 5.884 | 5.347 | 5.872 | 5.736 | 5.968 | ns |
| | | GCLK PLL | $t_{co}$ | 1.468 | 1.674 | 2.185 | 2.292 | 2.510 | 2.529 | 2.478 | 2.421 | 2.642 | 2.659 | 2.480 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.063 | 3.290 | 4.673 | 5.076 | 5.591 | 5.455 | 5.714 | 5.210 | 5.728 | 5.591 | 5.794 | ns |
| | | GCLK PLL | $t_{co}$ | 1.361 | 1.575 | 2.030 | 2.129 | 2.340 | 2.359 | 2.308 | 2.254 | 2.468 | 2.485 | 2.306 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.006 | 3.246 | 4.589 | 4.990 | 5.500 | 5.364 | 5.588 | 5.121 | 5.633 | 5.497 | 5.664 | ns |
| | | GCLK PLL | $t_{co}$ | 1.312 | 1.504 | 1.919 | 2.010 | 2.214 | 2.233 | 2.182 | 2.131 | 2.338 | 2.355 | 2.176 | ns |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.405 | 3.663 | 5.253 | 5.717 | 6.292 | 6.156 | 6.368 | 5.867 | 6.444 | 6.308 | 6.461 | ns |
| | | GCLK PLL | $t_{co}$ | 1.650 | 1.863 | 2.459 | 2.597 | 2.849 | 2.868 | 2.787 | 2.729 | 2.984 | 3.002 | 2.793 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.180 | 3.461 | 4.926 | 5.349 | 5.887 | 5.751 | 5.963 | 5.502 | 6.038 | 5.901 | 6.054 | ns |
| | | GCLK PLL | $t_{co}$ | 1.477 | 1.677 | 2.168 | 2.271 | 2.489 | 2.508 | 2.427 | 2.403 | 2.623 | 2.640 | 2.431 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.115 | 3.359 | 4.773 | 5.199 | 5.728 | 5.592 | 5.804 | 5.334 | 5.865 | 5.729 | 5.882 | ns |
| | | GCLK PLL | $t_{co}$ | 1.402 | 1.595 | 2.069 | 2.166 | 2.388 | 2.407 | 2.326 | 2.289 | 2.517 | 2.535 | 2.326 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.055 | 3.285 | 4.696 | 5.106 | 5.632 | 5.496 | 5.708 | 5.239 | 5.771 | 5.635 | 5.788 | ns |
| | | GCLK PLL | $t_{co}$ | 1.384 | 1.575 | 2.012 | 2.113 | 2.323 | 2.342 | 2.261 | 2.233 | 2.445 | 2.463 | 2.254 | ns |


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**Table 1–104.** EP3SE50 Row Pins Output Timing Parameters (Part 3 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.316 | 3.581 | 5.163 | 5.631 | 6.220 | 6.084 | 6.296 | 5.774 | 6.368 | 6.232 | 6.385 | ns |
| | | GCLK PLL | $t_{co}$ | 1.592 | 1.806 | 2.387 | 2.524 | 2.786 | 2.805 | 2.724 | 2.650 | 2.919 | 2.937 | 2.728 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.074 | 3.324 | 4.758 | 5.194 | 5.729 | 5.593 | 5.805 | 5.328 | 5.864 | 5.728 | 5.881 | ns |
| | | GCLK PLL | $t_{co}$ | 1.400 | 1.592 | 2.065 | 2.166 | 2.392 | 2.411 | 2.330 | 2.286 | 2.518 | 2.536 | 2.327 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.047 | 3.276 | 4.685 | 5.098 | 5.623 | 5.487 | 5.699 | 5.230 | 5.759 | 5.623 | 5.776 | ns |
| | | GCLK PLL | $t_{co}$ | 1.373 | 1.566 | 1.996 | 2.105 | 2.323 | 2.342 | 2.261 | 2.226 | 2.445 | 2.463 | 2.254 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.038 | 3.267 | 4.663 | 5.080 | 5.604 | 5.468 | 5.680 | 5.212 | 5.737 | 5.601 | 5.754 | ns |
| | | GCLK PLL | $t_{co}$ | 1.354 | 1.555 | 1.980 | 2.081 | 2.304 | 2.323 | 2.242 | 2.202 | 2.426 | 2.444 | 2.235 | ns |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.259 | 3.506 | 5.073 | 5.545 | 6.145 | 6.009 | 6.221 | 5.686 | 6.284 | 6.148 | 6.301 | ns |
| | | GCLK PLL | $t_{co}$ | 1.522 | 1.719 | 2.308 | 2.456 | 2.725 | 2.744 | 2.663 | 2.582 | 2.850 | 2.868 | 2.659 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.079 | 3.317 | 4.780 | 5.222 | 5.770 | 5.634 | 5.846 | 5.353 | 5.906 | 5.770 | 5.923 | ns |
| | | GCLK PLL | $t_{co}$ | 1.405 | 1.596 | 2.082 | 2.194 | 2.440 | 2.459 | 2.378 | 2.315 | 2.562 | 2.580 | 2.371 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.010 | 3.234 | 4.582 | 4.981 | 5.490 | 5.354 | 5.556 | 5.108 | 5.619 | 5.483 | 5.627 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.492 | 1.899 | 1.984 | 2.183 | 2.202 | 2.150 | 2.100 | 2.301 | 2.318 | 2.139 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.005 | 3.230 | 4.579 | 4.979 | 5.488 | 5.352 | 5.548 | 5.107 | 5.618 | 5.482 | 5.620 | ns |
| | | GCLK PLL | $t_{co}$ | 1.303 | 1.488 | 1.896 | 1.982 | 2.181 | 2.200 | 2.142 | 2.099 | 2.300 | 2.317 | 2.132 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 2.996 | 3.219 | 4.564 | 4.963 | 5.471 | 5.335 | 5.521 | 5.090 | 5.600 | 5.464 | 5.593 | ns |
| | | GCLK PLL | $t_{co}$ | 1.294 | 1.477 | 1.881 | 1.966 | 2.164 | 2.183 | 2.115 | 2.082 | 2.282 | 2.299 | 2.105 | ns |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.016 | 3.241 | 4.591 | 4.993 | 5.505 | 5.369 | 5.581 | 5.120 | 5.634 | 5.498 | 5.651 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.519 | 1.931 | 2.017 | 2.218 | 2.237 | 2.156 | 2.132 | 2.336 | 2.354 | 2.145 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.001 | 3.227 | 4.588 | 4.991 | 5.503 | 5.367 | 5.579 | 5.118 | 5.632 | 5.496 | 5.649 | ns |
| | | GCLK PLL | $t_{co}$ | 1.328 | 1.514 | 1.929 | 2.016 | 2.217 | 2.236 | 2.155 | 2.130 | 2.334 | 2.352 | 2.143 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.990 | 3.215 | 4.571 | 4.974 | 5.486 | 5.350 | 5.562 | 5.101 | 5.616 | 5.480 | 5.633 | ns |
| | | GCLK PLL | $t_{co}$ | 1.317 | 1.503 | 1.919 | 2.006 | 2.207 | 2.226 | 2.145 | 2.121 | 2.325 | 2.343 | 2.134 | ns |
| | 10mA | GCLK | $t_{co}$ | 2.966 | 3.192 | 4.555 | 4.958 | 5.471 | 5.335 | 5.547 | 5.086 | 5.601 | 5.465 | 5.618 | ns |
| | | GCLK PLL | $t_{co}$ | 1.306 | 1.492 | 1.906 | 1.993 | 2.194 | 2.213 | 2.132 | 2.109 | 2.313 | 2.331 | 2.122 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.966 | 3.191 | 4.554 | 4.957 | 5.470 | 5.334 | 5.546 | 5.085 | 5.600 | 5.464 | 5.617 | ns |
| | | GCLK PLL | $t_{co}$ | 1.306 | 1.491 | 1.906 | 1.993 | 2.194 | 2.213 | 2.132 | 2.108 | 2.313 | 2.331 | 2.122 | ns |

**Table 1–104.** EP3SE50 Row Pins Output Timing Parameters (Part 4 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 2.976 | 3.200 | 4.552 | 4.953 | 5.464 | 5.328 | 5.540 | 5.080 | 5.593 | 5.457 | 5.610 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.498 | 1.905 | 1.990 | 2.189 | 2.208 | 2.127 | 2.104 | 2.307 | 2.325 | 2.116 | ns |
| | 16mA | GCLK | $t_{co}$ | 2.975 | 3.198 | 4.551 | 4.954 | 5.466 | 5.330 | 5.542 | 5.082 | 5.597 | 5.461 | 5.614 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.501 | 1.911 | 1.998 | 2.199 | 2.218 | 2.137 | 2.113 | 2.318 | 2.336 | 2.127 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.012 | 3.237 | 4.602 | 5.007 | 5.522 | 5.386 | 5.598 | 5.133 | 5.650 | 5.514 | 5.667 | ns |
| | | GCLK PLL | $t_{co}$ | 1.336 | 1.522 | 1.940 | 2.028 | 2.231 | 2.250 | 2.169 | 2.142 | 2.348 | 2.366 | 2.157 | ns |
| | 6mA | GCLK | $t_{co}$ | 2.989 | 3.215 | 4.584 | 4.990 | 5.505 | 5.369 | 5.581 | 5.117 | 5.634 | 5.498 | 5.651 | ns |
| | | GCLK PLL | $t_{co}$ | 1.322 | 1.508 | 1.929 | 2.018 | 2.221 | 2.240 | 2.159 | 2.133 | 2.339 | 2.357 | 2.148 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.972 | 3.198 | 4.567 | 4.972 | 5.487 | 5.351 | 5.563 | 5.099 | 5.617 | 5.481 | 5.634 | ns |
| | | GCLK PLL | $t_{co}$ | 1.311 | 1.496 | 1.916 | 2.005 | 2.208 | 2.227 | 2.146 | 2.120 | 2.326 | 2.344 | 2.135 | ns |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 2.991 | 3.213 | 4.558 | 4.958 | 5.467 | 5.331 | 5.543 | 5.084 | 5.596 | 5.460 | 5.613 | ns |
| | | GCLK PLL | $t_{co}$ | 1.321 | 1.504 | 1.904 | 1.988 | 2.187 | 2.206 | 2.125 | 2.103 | 2.304 | 2.322 | 2.113 | ns |
| | 6mA | GCLK | $t_{co}$ | 2.979 | 3.201 | 4.549 | 4.950 | 5.459 | 5.323 | 5.535 | 5.076 | 5.589 | 5.453 | 5.606 | ns |
| | | GCLK PLL | $t_{co}$ | 1.314 | 1.498 | 1.902 | 1.987 | 2.186 | 2.205 | 2.124 | 2.102 | 2.304 | 2.322 | 2.113 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.966 | 3.189 | 4.541 | 4.941 | 5.451 | 5.315 | 5.527 | 5.068 | 5.581 | 5.445 | 5.598 | ns |
| | | GCLK PLL | $t_{co}$ | 1.305 | 1.490 | 1.895 | 1.980 | 2.179 | 2.198 | 2.117 | 2.095 | 2.297 | 2.315 | 2.106 | ns |
| | 10mA | GCLK | $t_{co}$ | 2.968 | 3.191 | 4.543 | 4.944 | 5.454 | 5.318 | 5.530 | 5.071 | 5.584 | 5.448 | 5.601 | ns |
| | | GCLK PLL | $t_{co}$ | 1.308 | 1.492 | 1.898 | 1.983 | 2.183 | 2.202 | 2.121 | 2.098 | 2.300 | 2.318 | 2.109 | ns |
| | 12mA | GCLK | $t_{co}$ | 2.964 | 3.186 | 4.541 | 4.943 | 5.454 | 5.318 | 5.530 | 5.071 | 5.585 | 5.449 | 5.602 | ns |
| | | GCLK PLL | $t_{co}$ | 1.304 | 1.489 | 1.900 | 1.986 | 2.186 | 2.205 | 2.124 | 2.101 | 2.305 | 2.323 | 2.114 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 2.972 | 3.194 | 4.536 | 4.935 | 5.445 | 5.309 | 5.521 | 5.062 | 5.574 | 5.438 | 5.591 | ns |
| | | GCLK PLL | $t_{co}$ | 1.312 | 1.497 | 1.898 | 1.983 | 2.182 | 2.201 | 2.120 | 2.097 | 2.299 | 2.317 | 2.108 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 2.998 | 3.220 | 4.569 | 4.971 | 5.482 | 5.346 | 5.558 | 5.096 | 5.610 | 5.474 | 5.627 | ns |
| | | GCLK PLL | $t_{co}$ | 1.327 | 1.510 | 1.913 | 1.998 | 2.198 | 2.217 | 2.136 | 2.112 | 2.315 | 2.333 | 2.124 | ns |
| | 6mA | GCLK | $t_{co}$ | 2.986 | 3.210 | 4.565 | 4.967 | 5.478 | 5.342 | 5.554 | 5.093 | 5.607 | 5.471 | 5.624 | ns |
| | | GCLK PLL | $t_{co}$ | 1.321 | 1.505 | 1.914 | 2.000 | 2.200 | 2.219 | 2.138 | 2.114 | 2.318 | 2.336 | 2.127 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.982 | 3.205 | 4.559 | 4.961 | 5.472 | 5.336 | 5.548 | 5.087 | 5.601 | 5.465 | 5.618 | ns |
| | | GCLK PLL | $t_{co}$ | 1.317 | 1.501 | 1.909 | 1.995 | 2.195 | 2.214 | 2.133 | 2.109 | 2.312 | 2.330 | 2.121 | ns |

**Table 1–104.** EP3SE50 Row Pins Output Timing Parameters (Part 5 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 2.997 | 3.219 | 4.580 | 4.985 | 5.500 | 5.364 | 5.576 | 5.110 | 5.627 | 5.491 | 5.644 | ns |
| | | GCLK PLL | $t_{co}$ | 1.329 | 1.512 | 1.926 | 2.014 | 2.217 | 2.236 | 2.155 | 2.128 | 2.334 | 2.352 | 2.143 | ns |
| | 6mA | GCLK | $t_{co}$ | 2.985 | 3.207 | 4.569 | 4.973 | 5.488 | 5.352 | 5.564 | 5.099 | 5.616 | 5.480 | 5.633 | ns |
| | | GCLK PLL | $t_{co}$ | 1.320 | 1.504 | 1.917 | 2.005 | 2.208 | 2.227 | 2.146 | 2.119 | 2.325 | 2.343 | 2.134 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.982 | 3.205 | 4.573 | 4.978 | 5.494 | 5.358 | 5.570 | 5.105 | 5.623 | 5.487 | 5.640 | ns |
| | | GCLK PLL | $t_{co}$ | 1.319 | 1.504 | 1.924 | 2.013 | 2.217 | 2.236 | 2.155 | 2.128 | 2.335 | 2.353 | 2.144 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.116 | 3.340 | 4.634 | 5.027 | 5.530 | 5.394 | 5.578 | 5.156 | 5.661 | 5.525 | 5.651 | ns |
| | | GCLK PLL | $t_{co}$ | 1.414 | 1.598 | 1.951 | 2.030 | 2.223 | 2.242 | 2.160 | 2.148 | 2.343 | 2.360 | 2.151 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.116 | 3.340 | 4.634 | 5.027 | 5.530 | 5.394 | 5.578 | 5.156 | 5.661 | 5.525 | 5.651 | ns |
| | | GCLK PLL | $t_{co}$ | 1.414 | 1.598 | 1.951 | 2.030 | 2.223 | 2.242 | 2.160 | 2.148 | 2.343 | 2.360 | 2.151 | ns |

Table 1–115 through Table 1–108 list the maximum I/O timing parameters for EP3SE50 devices for differential I/O standards.

Table 1–105 lists the EP3SE50 column pins input timing parameters for differential I/O standards.

**Table 1–105.** EP3SE50 Column Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -0.730 | -0.751 | -1.114 | -1.228 | -1.341 | -1.284 | -1.581 | -1.230 | -1.344 | -1.290 | -1.617 | ns |
| | | $t_h$ | 0.848 | 0.884 | 1.299 | 1.436 | 1.571 | 1.501 | 1.798 | 1.446 | 1.583 | 1.516 | 1.835 | ns |
| | GCLK PLL | $t_{su}$ | 1.120 | 1.138 | 1.796 | 2.027 | 2.253 | 2.141 | 2.145 | 2.036 | 2.262 | 2.145 | 2.193 | ns |
| | | $t_h$ | -0.867 | -0.870 | -1.397 | -1.578 | -1.752 | -1.669 | -1.666 | -1.580 | -1.754 | -1.665 | -1.710 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -0.730 | -0.751 | -1.114 | -1.228 | -1.341 | -1.284 | -1.581 | -1.230 | -1.344 | -1.290 | -1.617 | ns |
| | | $t_h$ | 0.848 | 0.884 | 1.299 | 1.436 | 1.571 | 1.501 | 1.798 | 1.446 | 1.583 | 1.516 | 1.835 | ns |
| | GCLK PLL | $t_{su}$ | 1.120 | 1.138 | 1.796 | 2.027 | 2.253 | 2.141 | 2.145 | 2.036 | 2.262 | 2.145 | 2.193 | ns |
| | | $t_h$ | -0.867 | -0.870 | -1.397 | -1.578 | -1.752 | -1.669 | -1.666 | -1.580 | -1.754 | -1.665 | -1.710 | ns |
| RSDS | GCLK | $t_{su}$ | -0.738 | -0.763 | -1.124 | -1.239 | -1.357 | -1.300 | -1.597 | -1.241 | -1.359 | -1.305 | -1.632 | ns |
| | | $t_h$ | 0.856 | 0.896 | 1.309 | 1.447 | 1.587 | 1.517 | 1.814 | 1.457 | 1.598 | 1.531 | 1.850 | ns |
| | GCLK PLL | $t_{su}$ | 1.112 | 1.126 | 1.786 | 2.016 | 2.237 | 2.125 | 2.129 | 2.025 | 2.247 | 2.130 | 2.178 | ns |
| | | $t_h$ | -0.859 | -0.858 | -1.387 | -1.567 | -1.736 | -1.653 | -1.650 | -1.569 | -1.739 | -1.650 | -1.695 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.738 | -0.763 | -1.124 | -1.239 | -1.357 | -1.300 | -1.597 | -1.241 | -1.359 | -1.305 | -1.632 | ns |
| | | $t_h$ | 0.856 | 0.896 | 1.309 | 1.447 | 1.587 | 1.517 | 1.814 | 1.457 | 1.598 | 1.531 | 1.850 | ns |
| | GCLK PLL | $t_{su}$ | 1.112 | 1.126 | 1.786 | 2.016 | 2.237 | 2.125 | 2.129 | 2.025 | 2.247 | 2.130 | 2.178 | ns |
| | | $t_h$ | -0.859 | -0.858 | -1.387 | -1.567 | -1.736 | -1.653 | -1.650 | -1.569 | -1.739 | -1.650 | -1.695 | ns |

**Table 1–105.** EP3SE50 Column Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.750 | -0.774 | -1.133 | -1.250 | -1.376 | -1.319 | -1.616 | -1.252 | -1.377 | -1.323 | -1.650 | ns |
| | | $t_h$ | 0.868 | 0.907 | 1.319 | 1.458 | 1.606 | 1.536 | 1.833 | 1.468 | 1.616 | 1.549 | 1.868 | ns |
| | GCLK PLL | $t_{su}$ | 1.100 | 1.115 | 1.777 | 2.005 | 2.218 | 2.106 | 2.110 | 2.014 | 2.229 | 2.112 | 2.160 | ns |
| | | $t_h$ | -0.847 | -0.847 | -1.377 | -1.556 | -1.717 | -1.634 | -1.631 | -1.558 | -1.721 | -1.632 | -1.677 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.750 | -0.774 | -1.133 | -1.250 | -1.376 | -1.319 | -1.616 | -1.252 | -1.377 | -1.323 | -1.650 | ns |
| | | $t_h$ | 0.868 | 0.907 | 1.319 | 1.458 | 1.606 | 1.536 | 1.833 | 1.468 | 1.616 | 1.549 | 1.868 | ns |
| | GCLK PLL | $t_{su}$ | 1.100 | 1.115 | 1.777 | 2.005 | 2.218 | 2.106 | 2.110 | 2.014 | 2.229 | 2.112 | 2.160 | ns |
| | | $t_h$ | -0.847 | -0.847 | -1.377 | -1.556 | -1.717 | -1.634 | -1.631 | -1.558 | -1.721 | -1.632 | -1.677 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.738 | -0.763 | -1.124 | -1.239 | -1.357 | -1.300 | -1.597 | -1.241 | -1.359 | -1.305 | -1.632 | ns |
| | | $t_h$ | 0.856 | 0.896 | 1.309 | 1.447 | 1.587 | 1.517 | 1.814 | 1.457 | 1.598 | 1.531 | 1.850 | ns |
| | GCLK PLL | $t_{su}$ | 1.112 | 1.126 | 1.786 | 2.016 | 2.237 | 2.125 | 2.129 | 2.025 | 2.247 | 2.130 | 2.178 | ns |
| | | $t_h$ | -0.859 | -0.858 | -1.387 | -1.567 | -1.736 | -1.653 | -1.650 | -1.569 | -1.739 | -1.650 | -1.695 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.738 | -0.763 | -1.124 | -1.239 | -1.357 | -1.300 | -1.597 | -1.241 | -1.359 | -1.305 | -1.632 | ns |
| | | $t_h$ | 0.856 | 0.896 | 1.309 | 1.447 | 1.587 | 1.517 | 1.814 | 1.457 | 1.598 | 1.531 | 1.850 | ns |
| | GCLK PLL | $t_{su}$ | 1.112 | 1.126 | 1.786 | 2.016 | 2.237 | 2.125 | 2.129 | 2.025 | 2.247 | 2.130 | 2.178 | ns |
| | | $t_h$ | -0.859 | -0.858 | -1.387 | -1.567 | -1.736 | -1.653 | -1.650 | -1.569 | -1.739 | -1.650 | -1.695 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.750 | -0.774 | -1.133 | -1.250 | -1.376 | -1.319 | -1.616 | -1.252 | -1.377 | -1.323 | -1.650 | ns |
| | | $t_h$ | 0.868 | 0.907 | 1.319 | 1.458 | 1.606 | 1.536 | 1.833 | 1.468 | 1.616 | 1.549 | 1.868 | ns |
| | GCLK PLL | $t_{su}$ | 1.100 | 1.115 | 1.777 | 2.005 | 2.218 | 2.106 | 2.110 | 2.014 | 2.229 | 2.112 | 2.160 | ns |
| | | $t_h$ | -0.847 | -0.847 | -1.377 | -1.556 | -1.717 | -1.634 | -1.631 | -1.558 | -1.721 | -1.632 | -1.677 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.750 | -0.774 | -1.133 | -1.250 | -1.376 | -1.319 | -1.616 | -1.252 | -1.377 | -1.323 | -1.650 | ns |
| | | $t_h$ | 0.868 | 0.907 | 1.319 | 1.458 | 1.606 | 1.536 | 1.833 | 1.468 | 1.616 | 1.549 | 1.868 | ns |
| | GCLK PLL | $t_{su}$ | 1.100 | 1.115 | 1.777 | 2.005 | 2.218 | 2.106 | 2.110 | 2.014 | 2.229 | 2.112 | 2.160 | ns |
| | | $t_h$ | -0.847 | -0.847 | -1.377 | -1.556 | -1.717 | -1.634 | -1.631 | -1.558 | -1.721 | -1.632 | -1.677 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.757 | -0.780 | -1.145 | -1.255 | -1.376 | -1.321 | -1.615 | -1.256 | -1.372 | -1.321 | -1.646 | ns |
| | | $t_h$ | 0.875 | 0.913 | 1.332 | 1.466 | 1.609 | 1.539 | 1.837 | 1.475 | 1.616 | 1.548 | 1.869 | ns |
| | GCLK PLL | $t_{su}$ | 1.093 | 1.109 | 1.765 | 2.000 | 2.218 | 2.104 | 2.111 | 2.010 | 2.234 | 2.114 | 2.164 | ns |
| | | $t_h$ | -0.840 | -0.841 | -1.364 | -1.548 | -1.714 | -1.631 | -1.627 | -1.551 | -1.721 | -1.633 | -1.676 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -0.757 | -0.780 | -1.145 | -1.255 | -1.376 | -1.321 | -1.615 | -1.256 | -1.372 | -1.321 | -1.646 | ns |
| | | $t_h$ | 0.875 | 0.913 | 1.332 | 1.466 | 1.609 | 1.539 | 1.837 | 1.475 | 1.616 | 1.548 | 1.869 | ns |
| | GCLK PLL | $t_{su}$ | 1.093 | 1.109 | 1.765 | 2.000 | 2.218 | 2.104 | 2.111 | 2.010 | 2.234 | 2.114 | 2.164 | ns |
| | | $t_h$ | -0.840 | -0.841 | -1.364 | -1.548 | -1.714 | -1.631 | -1.627 | -1.551 | -1.721 | -1.633 | -1.676 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -0.730 | -0.751 | -1.114 | -1.228 | -1.341 | -1.284 | -1.581 | -1.230 | -1.344 | -1.290 | -1.617 | ns |
| | | $t_h$ | 0.848 | 0.884 | 1.299 | 1.436 | 1.571 | 1.501 | 1.798 | 1.446 | 1.583 | 1.516 | 1.835 | ns |
| | GCLK PLL | $t_{su}$ | 1.120 | 1.138 | 1.796 | 2.027 | 2.253 | 2.141 | 2.145 | 2.036 | 2.262 | 2.145 | 2.193 | ns |
| | | $t_h$ | -0.867 | -0.870 | -1.397 | -1.578 | -1.752 | -1.669 | -1.666 | -1.580 | -1.754 | -1.665 | -1.710 | ns |

**Table 1–105.** EP3SE50 Column Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.730 | -0.751 | -1.114 | -1.228 | -1.341 | -1.284 | -1.581 | -1.230 | -1.344 | -1.290 | -1.617 | ns |
| | | $t_h$ | 0.848 | 0.884 | 1.299 | 1.436 | 1.571 | 1.501 | 1.798 | 1.446 | 1.583 | 1.516 | 1.835 | ns |
| | GCLK PLL | $t_{su}$ | 1.120 | 1.138 | 1.796 | 2.027 | 2.253 | 2.141 | 2.145 | 2.036 | 2.262 | 2.145 | 2.193 | ns |
| | | $t_h$ | -0.867 | -0.870 | -1.397 | -1.578 | -1.752 | -1.669 | -1.666 | -1.580 | -1.754 | -1.665 | -1.710 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.738 | -0.763 | -1.124 | -1.239 | -1.357 | -1.300 | -1.597 | -1.241 | -1.359 | -1.305 | -1.632 | ns |
| | | $t_h$ | 0.856 | 0.896 | 1.309 | 1.447 | 1.587 | 1.517 | 1.814 | 1.457 | 1.598 | 1.531 | 1.850 | ns |
| | GCLK PLL | $t_{su}$ | 1.112 | 1.126 | 1.786 | 2.016 | 2.237 | 2.125 | 2.129 | 2.025 | 2.247 | 2.130 | 2.178 | ns |
| | | $t_h$ | -0.859 | -0.858 | -1.387 | -1.567 | -1.736 | -1.653 | -1.650 | -1.569 | -1.739 | -1.650 | -1.695 | ns |

Table 1–106 lists the EP3SE50 row pins input timing parameters for differential I/O standards.

**Table 1–106.** EP3SE50 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -0.925 | -0.948 | -1.004 | -0.967 | -1.102 | -1.057 | -1.337 | -0.933 | -1.060 | -1.017 | -1.369 | ns |
| | | $t_h$ | 1.048 | 1.086 | 1.223 | 1.219 | 1.381 | 1.322 | 1.601 | 1.199 | 1.353 | 1.296 | 1.634 | ns |
| | GCLK PLL | $t_{su}$ | 0.886 | 0.901 | 1.866 | 2.244 | 2.450 | 2.324 | 2.344 | 2.289 | 2.502 | 2.376 | 2.396 | ns |
| | | $t_h$ | -0.626 | -0.628 | -1.432 | -1.750 | -1.897 | -1.803 | -1.817 | -1.782 | -1.937 | -1.842 | -1.867 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -0.925 | -0.948 | -1.004 | -0.967 | -1.102 | -1.057 | -1.337 | -0.933 | -1.060 | -1.017 | -1.369 | ns |
| | | $t_h$ | 1.048 | 1.086 | 1.223 | 1.219 | 1.381 | 1.322 | 1.601 | 1.199 | 1.353 | 1.296 | 1.634 | ns |
| | GCLK PLL | $t_{su}$ | 0.886 | 0.901 | 1.866 | 2.244 | 2.450 | 2.324 | 2.344 | 2.289 | 2.502 | 2.376 | 2.396 | ns |
| | | $t_h$ | -0.626 | -0.628 | -1.432 | -1.750 | -1.897 | -1.803 | -1.817 | -1.782 | -1.937 | -1.842 | -1.867 | ns |
| RSDS | GCLK | $t_{su}$ | -0.925 | -0.948 | -1.004 | -0.967 | -1.102 | -1.057 | -1.337 | -0.933 | -1.060 | -1.017 | -1.369 | ns |
| | | $t_h$ | 1.048 | 1.086 | 1.223 | 1.219 | 1.381 | 1.322 | 1.601 | 1.199 | 1.353 | 1.296 | 1.634 | ns |
| | GCLK PLL | $t_{su}$ | 0.886 | 0.901 | 1.866 | 2.244 | 2.450 | 2.324 | 2.344 | 2.289 | 2.502 | 2.376 | 2.396 | ns |
| | | $t_h$ | -0.626 | -0.628 | -1.432 | -1.750 | -1.897 | -1.803 | -1.817 | -1.782 | -1.937 | -1.842 | -1.867 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.740 | -0.773 | -1.101 | -1.201 | -1.301 | -1.251 | -1.526 | -1.210 | -1.307 | -1.259 | -1.563 | ns |
| | | $t_h$ | 0.856 | 0.902 | 1.288 | 1.408 | 1.531 | 1.467 | 1.741 | 1.427 | 1.548 | 1.486 | 1.779 | ns |
| | GCLK PLL | $t_{su}$ | 1.081 | 1.086 | 1.779 | 2.020 | 2.261 | 2.140 | 2.165 | 2.022 | 2.265 | 2.144 | 2.212 | ns |
| | | $t_h$ | -0.828 | -0.822 | -1.377 | -1.571 | -1.757 | -1.668 | -1.687 | -1.564 | -1.752 | -1.662 | -1.732 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.740 | -0.773 | -1.101 | -1.201 | -1.301 | -1.251 | -1.526 | -1.210 | -1.307 | -1.259 | -1.563 | ns |
| | | $t_h$ | 0.856 | 0.902 | 1.288 | 1.408 | 1.531 | 1.467 | 1.741 | 1.427 | 1.548 | 1.486 | 1.779 | ns |
| | GCLK PLL | $t_{su}$ | 1.081 | 1.086 | 1.779 | 2.020 | 2.261 | 2.140 | 2.165 | 2.022 | 2.265 | 2.144 | 2.212 | ns |
| | | $t_h$ | -0.828 | -0.822 | -1.377 | -1.571 | -1.757 | -1.668 | -1.687 | -1.564 | -1.752 | -1.662 | -1.732 | ns |

**Table 1–106.** EP3SE50 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.749 | -0.785 | -1.110 | -1.211 | -1.317 | -1.267 | -1.542 | -1.219 | -1.323 | -1.275 | -1.579 | ns |
| | | $t_h$ | 0.865 | 0.914 | 1.297 | 1.418 | 1.547 | 1.483 | 1.757 | 1.436 | 1.564 | 1.502 | 1.795 | ns |
| | GCLK PLL | $t_{su}$ | 1.072 | 1.074 | 1.770 | 2.010 | 2.245 | 2.124 | 2.149 | 2.013 | 2.249 | 2.128 | 2.196 | ns |
| | | $t_h$ | -0.819 | -0.810 | -1.368 | -1.561 | -1.741 | -1.652 | -1.671 | -1.555 | -1.736 | -1.646 | -1.716 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.749 | -0.785 | -1.110 | -1.211 | -1.317 | -1.267 | -1.542 | -1.219 | -1.323 | -1.275 | -1.579 | ns |
| | | $t_h$ | 0.865 | 0.914 | 1.297 | 1.418 | 1.547 | 1.483 | 1.757 | 1.436 | 1.564 | 1.502 | 1.795 | ns |
| | GCLK PLL | $t_{su}$ | 1.072 | 1.074 | 1.770 | 2.010 | 2.245 | 2.124 | 2.149 | 2.013 | 2.249 | 2.128 | 2.196 | ns |
| | | $t_h$ | -0.819 | -0.810 | -1.368 | -1.561 | -1.741 | -1.652 | -1.671 | -1.555 | -1.736 | -1.646 | -1.716 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.763 | -0.797 | -1.123 | -1.221 | -1.335 | -1.285 | -1.560 | -1.230 | -1.340 | -1.292 | -1.596 | ns |
| | | $t_h$ | 0.879 | 0.926 | 1.309 | 1.428 | 1.565 | 1.501 | 1.775 | 1.447 | 1.581 | 1.519 | 1.812 | ns |
| | GCLK PLL | $t_{su}$ | 1.058 | 1.062 | 1.757 | 2.000 | 2.227 | 2.106 | 2.131 | 2.002 | 2.232 | 2.111 | 2.179 | ns |
| | | $t_h$ | -0.805 | -0.798 | -1.356 | -1.551 | -1.723 | -1.634 | -1.653 | -1.544 | -1.719 | -1.629 | -1.699 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.763 | -0.797 | -1.123 | -1.221 | -1.335 | -1.285 | -1.560 | -1.230 | -1.340 | -1.292 | -1.596 | ns |
| | | $t_h$ | 0.879 | 0.926 | 1.309 | 1.428 | 1.565 | 1.501 | 1.775 | 1.447 | 1.581 | 1.519 | 1.812 | ns |
| | GCLK PLL | $t_{su}$ | 1.058 | 1.062 | 1.757 | 2.000 | 2.227 | 2.106 | 2.131 | 2.002 | 2.232 | 2.111 | 2.179 | ns |
| | | $t_h$ | -0.805 | -0.798 | -1.356 | -1.551 | -1.723 | -1.634 | -1.653 | -1.544 | -1.719 | -1.629 | -1.699 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.749 | -0.785 | -1.110 | -1.211 | -1.317 | -1.267 | -1.542 | -1.219 | -1.323 | -1.275 | -1.579 | ns |
| | | $t_h$ | 0.865 | 0.914 | 1.297 | 1.418 | 1.547 | 1.483 | 1.757 | 1.436 | 1.564 | 1.502 | 1.795 | ns |
| | GCLK PLL | $t_{su}$ | 1.072 | 1.074 | 1.770 | 2.010 | 2.245 | 2.124 | 2.149 | 2.013 | 2.249 | 2.128 | 2.196 | ns |
| | | $t_h$ | -0.819 | -0.810 | -1.368 | -1.561 | -1.741 | -1.652 | -1.671 | -1.555 | -1.736 | -1.646 | -1.716 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.749 | -0.785 | -1.110 | -1.211 | -1.317 | -1.267 | -1.542 | -1.219 | -1.323 | -1.275 | -1.579 | ns |
| | | $t_h$ | 0.865 | 0.914 | 1.297 | 1.418 | 1.547 | 1.483 | 1.757 | 1.436 | 1.564 | 1.502 | 1.795 | ns |
| | GCLK PLL | $t_{su}$ | 1.072 | 1.074 | 1.770 | 2.010 | 2.245 | 2.124 | 2.149 | 2.013 | 2.249 | 2.128 | 2.196 | ns |
| | | $t_h$ | -0.819 | -0.810 | -1.368 | -1.561 | -1.741 | -1.652 | -1.671 | -1.555 | -1.736 | -1.646 | -1.716 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -0.763 | -0.797 | -1.123 | -1.221 | -1.335 | -1.285 | -1.560 | -1.230 | -1.340 | -1.292 | -1.596 | ns |
| | | $t_h$ | 0.879 | 0.926 | 1.309 | 1.428 | 1.565 | 1.501 | 1.775 | 1.447 | 1.581 | 1.519 | 1.812 | ns |
| | GCLK PLL | $t_{su}$ | 1.058 | 1.062 | 1.757 | 2.000 | 2.227 | 2.106 | 2.131 | 2.002 | 2.232 | 2.111 | 2.179 | ns |
| | | $t_h$ | -0.805 | -0.798 | -1.356 | -1.551 | -1.723 | -1.634 | -1.653 | -1.544 | -1.719 | -1.629 | -1.699 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -0.763 | -0.797 | -1.123 | -1.221 | -1.335 | -1.285 | -1.560 | -1.230 | -1.340 | -1.292 | -1.596 | ns |
| | | $t_h$ | 0.879 | 0.926 | 1.309 | 1.428 | 1.565 | 1.501 | 1.775 | 1.447 | 1.581 | 1.519 | 1.812 | ns |
| | GCLK PLL | $t_{su}$ | 1.058 | 1.062 | 1.757 | 2.000 | 2.227 | 2.106 | 2.131 | 2.002 | 2.232 | 2.111 | 2.179 | ns |
| | | $t_h$ | -0.805 | -0.798 | -1.356 | -1.551 | -1.723 | -1.634 | -1.653 | -1.544 | -1.719 | -1.629 | -1.699 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.762 | -0.796 | -1.128 | -1.227 | -1.336 | -1.287 | -1.561 | -1.231 | -1.336 | -1.290 | -1.593 | ns |
| | | $t_h$ | 0.878 | 0.925 | 1.314 | 1.436 | 1.569 | 1.505 | 1.780 | 1.451 | 1.580 | 1.518 | 1.813 | ns |
| | GCLK PLL | $t_{su}$ | 1.049 | 1.053 | 1.742 | 1.984 | 2.216 | 2.094 | 2.120 | 1.991 | 2.226 | 2.103 | 2.172 | ns |
| | | $t_h$ | -0.796 | -0.789 | -1.341 | -1.533 | -1.709 | -1.620 | -1.638 | -1.530 | -1.710 | -1.620 | -1.688 | ns |


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**Table 1–106.** EP3SE50 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.762 | -0.796 | -1.128 | -1.227 | -1.336 | -1.287 | -1.561 | -1.231 | -1.336 | -1.290 | -1.593 | ns |
| | | $t_h$ | 0.878 | 0.925 | 1.314 | 1.436 | 1.569 | 1.505 | 1.780 | 1.451 | 1.580 | 1.518 | 1.813 | ns |
| | GCLK PLL | $t_{su}$ | 1.049 | 1.053 | 1.742 | 1.984 | 2.216 | 2.094 | 2.120 | 1.991 | 2.226 | 2.103 | 2.172 | ns |
| | | $t_h$ | -0.796 | -0.789 | -1.341 | -1.533 | -1.709 | -1.620 | -1.638 | -1.530 | -1.710 | -1.620 | -1.688 | ns |

Table 1–107 lists the EP3SE50 column pins output timing parameters for differential I/O standards.

**Table 1–107.** EP3SE50 Column Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.058 | 3.277 | 4.610 | 5.014 | 5.527 | 5.385 | 5.614 | 5.140 | 5.654 | 5.514 | 5.680 | ns |
| | | GCLK PLL | $t_{co}$ | 3.054 | 3.280 | 4.657 | 5.069 | 5.589 | 5.447 | 5.676 | 5.199 | 5.720 | 5.580 | 5.746 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.058 | 3.277 | 4.610 | 5.014 | 5.527 | 5.385 | 5.614 | 5.140 | 5.654 | 5.514 | 5.680 | ns |
| | | GCLK PLL | $t_{co}$ | 3.054 | 3.280 | 4.657 | 5.069 | 5.589 | 5.447 | 5.676 | 5.199 | 5.720 | 5.580 | 5.746 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.058 | 3.277 | 4.610 | 5.014 | 5.527 | 5.385 | 5.614 | 5.140 | 5.654 | 5.514 | 5.680 | ns |
| | | GCLK PLL | $t_{co}$ | 3.054 | 3.280 | 4.657 | 5.069 | 5.589 | 5.447 | 5.676 | 5.199 | 5.720 | 5.580 | 5.746 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.085 | 3.310 | 4.681 | 5.092 | 5.611 | 5.469 | 5.698 | 5.220 | 5.740 | 5.600 | 5.766 | ns |
| | | GCLK PLL | $t_{co}$ | 3.075 | 3.300 | 4.671 | 5.081 | 5.601 | 5.459 | 5.688 | 5.209 | 5.730 | 5.590 | 5.756 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.075 | 3.300 | 4.674 | 5.085 | 5.605 | 5.463 | 5.692 | 5.214 | 5.735 | 5.595 | 5.761 | ns |
| | | GCLK PLL | $t_{co}$ | 3.068 | 3.294 | 4.667 | 5.079 | 5.599 | 5.457 | 5.686 | 5.207 | 5.729 | 5.589 | 5.755 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.067 | 3.292 | 4.664 | 5.076 | 5.596 | 5.454 | 5.683 | 5.204 | 5.725 | 5.585 | 5.751 | ns |
| | | GCLK PLL | $t_{co}$ | 3.089 | 3.314 | 4.685 | 5.096 | 5.615 | 5.473 | 5.702 | 5.224 | 5.745 | 5.605 | 5.771 | ns |

**Table 1–107.** EP3SE50 Column Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.079 | 3.303 | 4.664 | 5.073 | 5.590 | 5.448 | 5.677 | 5.200 | 5.718 | 5.578 | 5.744 | ns |
| | | GCLK PLL | $t_{co}$ | 3.074 | 3.299 | 4.664 | 5.073 | 5.591 | 5.449 | 5.678 | 5.201 | 5.720 | 5.580 | 5.746 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.072 | 3.297 | 4.663 | 5.072 | 5.589 | 5.447 | 5.676 | 5.200 | 5.719 | 5.579 | 5.745 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.288 | 4.653 | 5.062 | 5.580 | 5.438 | 5.667 | 5.190 | 5.709 | 5.569 | 5.735 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.065 | 3.290 | 4.659 | 5.069 | 5.588 | 5.446 | 5.675 | 5.198 | 5.718 | 5.578 | 5.744 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.287 | 4.642 | 5.050 | 5.566 | 5.424 | 5.653 | 5.177 | 5.694 | 5.554 | 5.720 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.076 | 3.300 | 4.660 | 5.068 | 5.584 | 5.442 | 5.671 | 5.196 | 5.713 | 5.573 | 5.739 | ns |
| | | GCLK PLL | $t_{co}$ | 3.072 | 3.297 | 4.661 | 5.070 | 5.588 | 5.446 | 5.675 | 5.198 | 5.717 | 5.577 | 5.743 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.062 | 3.286 | 4.650 | 5.059 | 5.576 | 5.434 | 5.663 | 5.187 | 5.705 | 5.565 | 5.731 | ns |
| | | GCLK PLL | $t_{co}$ | 3.060 | 3.284 | 4.648 | 5.056 | 5.574 | 5.432 | 5.661 | 5.185 | 5.703 | 5.563 | 5.729 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.060 | 3.285 | 4.651 | 5.061 | 5.579 | 5.437 | 5.666 | 5.189 | 5.709 | 5.569 | 5.735 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.288 | 4.648 | 5.056 | 5.573 | 5.431 | 5.660 | 5.184 | 5.702 | 5.562 | 5.728 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.090 | 3.317 | 4.693 | 5.104 | 5.623 | 5.481 | 5.710 | 5.232 | 5.752 | 5.612 | 5.778 | ns |
| | | GCLK PLL | $t_{co}$ | 3.076 | 3.303 | 4.681 | 5.093 | 5.613 | 5.471 | 5.700 | 5.222 | 5.743 | 5.603 | 5.769 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.064 | 3.290 | 4.664 | 5.075 | 5.595 | 5.453 | 5.682 | 5.204 | 5.725 | 5.585 | 5.751 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.290 | 4.667 | 5.079 | 5.599 | 5.457 | 5.686 | 5.208 | 5.730 | 5.590 | 5.756 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.060 | 3.286 | 4.660 | 5.071 | 5.592 | 5.450 | 5.679 | 5.201 | 5.722 | 5.582 | 5.748 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.288 | 4.653 | 5.062 | 5.580 | 5.438 | 5.667 | 5.190 | 5.709 | 5.569 | 5.735 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.065 | 3.290 | 4.661 | 5.072 | 5.591 | 5.449 | 5.678 | 5.200 | 5.721 | 5.581 | 5.747 | ns |
| | | GCLK PLL | $t_{co}$ | 3.093 | 3.320 | 4.692 | 5.102 | 5.621 | 5.479 | 5.708 | 5.231 | 5.750 | 5.610 | 5.776 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.082 | 3.308 | 4.680 | 5.090 | 5.609 | 5.467 | 5.696 | 5.219 | 5.738 | 5.598 | 5.764 | ns |
| | | GCLK PLL | $t_{co}$ | 3.077 | 3.304 | 4.680 | 5.091 | 5.610 | 5.468 | 5.697 | 5.220 | 5.740 | 5.600 | 5.766 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.063 | 3.289 | 4.662 | 5.072 | 5.591 | 5.449 | 5.678 | 5.201 | 5.722 | 5.582 | 5.748 | ns |
| | | GCLK PLL | $t_{co}$ | 3.061 | 3.287 | 4.660 | 5.070 | 5.589 | 5.447 | 5.676 | 5.199 | 5.719 | 5.579 | 5.745 | ns |

**Table 1–107.** EP3SE50 Column Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.065 | 3.289 | 4.652 | 5.060 | 5.577 | 5.435 | 5.664 | 5.188 | 5.706 | 5.566 | 5.732 | ns |
| | | GCLK PLL | $t_{co}$ | 3.065 | 3.290 | 4.660 | 5.070 | 5.589 | 5.447 | 5.676 | 5.199 | 5.719 | 5.579 | 5.745 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.081 | 3.307 | 4.676 | 5.085 | 5.603 | 5.461 | 5.690 | 5.214 | 5.732 | 5.592 | 5.758 | ns |
| | | GCLK PLL | $t_{co}$ | 3.081 | 3.307 | 4.676 | 5.085 | 5.603 | 5.461 | 5.690 | 5.214 | 5.732 | 5.592 | 5.758 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.071 | 3.297 | 4.666 | 5.075 | 5.593 | 5.451 | 5.680 | 5.204 | 5.723 | 5.583 | 5.749 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.289 | 4.652 | 5.060 | 5.577 | 5.435 | 5.664 | 5.188 | 5.706 | 5.566 | 5.732 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.058 | 3.277 | 4.610 | 5.014 | 5.527 | 5.385 | 5.614 | 5.140 | 5.654 | 5.514 | 5.680 | ns |
| | | GCLK PLL | $t_{co}$ | 3.054 | 3.280 | 4.657 | 5.069 | 5.589 | 5.447 | 5.676 | 5.199 | 5.720 | 5.580 | 5.746 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.058 | 3.277 | 4.610 | 5.014 | 5.527 | 5.385 | 5.614 | 5.140 | 5.654 | 5.514 | 5.680 | ns |
| | | GCLK PLL | $t_{co}$ | 3.054 | 3.280 | 4.657 | 5.069 | 5.589 | 5.447 | 5.676 | 5.199 | 5.720 | 5.580 | 5.746 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.058 | 3.277 | 4.610 | 5.014 | 5.527 | 5.385 | 5.614 | 5.140 | 5.654 | 5.514 | 5.680 | ns |
| | | GCLK PLL | $t_{co}$ | 3.054 | 3.280 | 4.657 | 5.069 | 5.589 | 5.447 | 5.676 | 5.199 | 5.720 | 5.580 | 5.746 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.085 | 3.310 | 4.681 | 5.092 | 5.611 | 5.469 | 5.698 | 5.220 | 5.740 | 5.600 | 5.766 | ns |
| | | GCLK PLL | $t_{co}$ | 3.075 | 3.300 | 4.671 | 5.081 | 5.601 | 5.459 | 5.688 | 5.209 | 5.730 | 5.590 | 5.756 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.075 | 3.300 | 4.674 | 5.085 | 5.605 | 5.463 | 5.692 | 5.214 | 5.735 | 5.595 | 5.761 | ns |
| | | GCLK PLL | $t_{co}$ | 3.068 | 3.294 | 4.667 | 5.079 | 5.599 | 5.457 | 5.686 | 5.207 | 5.729 | 5.589 | 5.755 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.067 | 3.292 | 4.664 | 5.076 | 5.596 | 5.454 | 5.683 | 5.204 | 5.725 | 5.585 | 5.751 | ns |
| | | GCLK PLL | $t_{co}$ | 3.089 | 3.314 | 4.685 | 5.096 | 5.615 | 5.473 | 5.702 | 5.224 | 5.745 | 5.605 | 5.771 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.079 | 3.303 | 4.664 | 5.073 | 5.590 | 5.448 | 5.677 | 5.200 | 5.718 | 5.578 | 5.744 | ns |
| | | GCLK PLL | $t_{co}$ | 3.074 | 3.299 | 4.664 | 5.073 | 5.591 | 5.449 | 5.678 | 5.201 | 5.720 | 5.580 | 5.746 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.072 | 3.297 | 4.663 | 5.072 | 5.589 | 5.447 | 5.676 | 5.200 | 5.719 | 5.579 | 5.745 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.288 | 4.653 | 5.062 | 5.580 | 5.438 | 5.667 | 5.190 | 5.709 | 5.569 | 5.735 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.065 | 3.290 | 4.659 | 5.069 | 5.588 | 5.446 | 5.675 | 5.198 | 5.718 | 5.578 | 5.744 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.287 | 4.642 | 5.050 | 5.566 | 5.424 | 5.653 | 5.177 | 5.694 | 5.554 | 5.720 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.076 | 3.300 | 4.660 | 5.068 | 5.584 | 5.442 | 5.671 | 5.196 | 5.713 | 5.573 | 5.739 | ns |
| | | GCLK PLL | $t_{co}$ | 3.072 | 3.297 | 4.661 | 5.070 | 5.588 | 5.446 | 5.675 | 5.198 | 5.717 | 5.577 | 5.743 | ns |

**Table 1–107.** EP3SE50 Column Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.062 | 3.286 | 4.650 | 5.059 | 5.576 | 5.434 | 5.663 | 5.187 | 5.705 | 5.565 | 5.731 | ns |
| | | GCLK PLL | $t_{co}$ | 3.060 | 3.284 | 4.648 | 5.056 | 5.574 | 5.432 | 5.661 | 5.185 | 5.703 | 5.563 | 5.729 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.060 | 3.285 | 4.651 | 5.061 | 5.579 | 5.437 | 5.666 | 5.189 | 5.709 | 5.569 | 5.735 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.288 | 4.648 | 5.056 | 5.573 | 5.431 | 5.660 | 5.184 | 5.702 | 5.562 | 5.728 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.090 | 3.317 | 4.693 | 5.104 | 5.623 | 5.481 | 5.710 | 5.232 | 5.752 | 5.612 | 5.778 | ns |
| | | GCLK PLL | $t_{co}$ | 3.076 | 3.303 | 4.681 | 5.093 | 5.613 | 5.471 | 5.700 | 5.222 | 5.743 | 5.603 | 5.769 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.064 | 3.290 | 4.664 | 5.075 | 5.595 | 5.453 | 5.682 | 5.204 | 5.725 | 5.585 | 5.751 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.290 | 4.667 | 5.079 | 5.599 | 5.457 | 5.686 | 5.208 | 5.730 | 5.590 | 5.756 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.060 | 3.286 | 4.660 | 5.071 | 5.592 | 5.450 | 5.679 | 5.201 | 5.722 | 5.582 | 5.748 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.288 | 4.653 | 5.062 | 5.580 | 5.438 | 5.667 | 5.190 | 5.709 | 5.569 | 5.735 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.065 | 3.290 | 4.661 | 5.072 | 5.591 | 5.449 | 5.678 | 5.200 | 5.721 | 5.581 | 5.747 | ns |
| | | GCLK PLL | $t_{co}$ | 3.093 | 3.320 | 4.692 | 5.102 | 5.621 | 5.479 | 5.708 | 5.231 | 5.750 | 5.610 | 5.776 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.082 | 3.308 | 4.680 | 5.090 | 5.609 | 5.467 | 5.696 | 5.219 | 5.738 | 5.598 | 5.764 | ns |
| | | GCLK PLL | $t_{co}$ | 3.077 | 3.304 | 4.680 | 5.091 | 5.610 | 5.468 | 5.697 | 5.220 | 5.740 | 5.600 | 5.766 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.063 | 3.289 | 4.662 | 5.072 | 5.591 | 5.449 | 5.678 | 5.201 | 5.722 | 5.582 | 5.748 | ns |
| | | GCLK PLL | $t_{co}$ | 3.061 | 3.287 | 4.660 | 5.070 | 5.589 | 5.447 | 5.676 | 5.199 | 5.719 | 5.579 | 5.745 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.065 | 3.289 | 4.652 | 5.060 | 5.577 | 5.435 | 5.664 | 5.188 | 5.706 | 5.566 | 5.732 | ns |
| | | GCLK PLL | $t_{co}$ | 3.065 | 3.290 | 4.660 | 5.070 | 5.589 | 5.447 | 5.676 | 5.199 | 5.719 | 5.579 | 5.745 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.081 | 3.307 | 4.676 | 5.085 | 5.603 | 5.461 | 5.690 | 5.214 | 5.732 | 5.592 | 5.758 | ns |
| | | GCLK PLL | $t_{co}$ | 3.081 | 3.307 | 4.676 | 5.085 | 5.603 | 5.461 | 5.690 | 5.214 | 5.732 | 5.592 | 5.758 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.071 | 3.297 | 4.666 | 5.075 | 5.593 | 5.451 | 5.680 | 5.204 | 5.723 | 5.583 | 5.749 | ns |
| | | GCLK PLL | $t_{co}$ | 3.064 | 3.289 | 4.652 | 5.060 | 5.577 | 5.435 | 5.664 | 5.188 | 5.706 | 5.566 | 5.732 | ns |

Table 1–108 lists the EP3SE50 row pins output timing parameters for differential I/O standards.

**Table 1–108.** EP3SE50 Row Pins Output Timing Parameters (Part 1 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | — | GCLK | $t_{co}$ | 2.674 | 2.849 | 3.990 | 4.359 | 4.834 | 4.699 | 4.910 | 4.467 | 4.945 | 4.809 | 4.961 | ns |
| | | GCLK PLL | $t_{co}$ | 3.068 | 3.295 | 4.657 | 5.068 | 5.588 | 5.445 | 5.648 | 5.200 | 5.724 | 5.579 | 5.715 | ns |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.050 | 3.285 | 4.695 | 5.114 | 5.642 | 5.499 | 5.702 | 5.251 | 5.785 | 5.640 | 5.776 | ns |
| | | GCLK PLL | $t_{co}$ | 2.674 | 2.849 | 3.990 | 4.359 | 4.834 | 4.699 | 4.910 | 4.467 | 4.945 | 4.809 | 4.961 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.068 | 3.295 | 4.657 | 5.068 | 5.588 | 5.445 | 5.648 | 5.200 | 5.724 | 5.579 | 5.715 | ns |
| | | GCLK PLL | $t_{co}$ | 3.050 | 3.285 | 4.695 | 5.114 | 5.642 | 5.499 | 5.702 | 5.251 | 5.785 | 5.640 | 5.776 | ns |
| MINI-LVDS | — | GCLK | $t_{co}$ | 2.674 | 2.849 | 3.990 | 4.359 | 4.834 | 4.699 | 4.910 | 4.467 | 4.945 | 4.809 | 4.961 | ns |
| | | GCLK PLL | $t_{co}$ | 3.068 | 3.295 | 4.657 | 5.068 | 5.588 | 5.445 | 5.648 | 5.200 | 5.724 | 5.579 | 5.715 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.050 | 3.285 | 4.695 | 5.114 | 5.642 | 5.499 | 5.702 | 5.251 | 5.785 | 5.640 | 5.776 | ns |
| | | GCLK PLL | $t_{co}$ | 3.104 | 3.338 | 4.741 | 5.158 | 5.685 | 5.542 | 5.745 | 5.294 | 5.824 | 5.679 | 5.815 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.090 | 3.324 | 4.728 | 5.145 | 5.672 | 5.529 | 5.732 | 5.280 | 5.811 | 5.666 | 5.802 | ns |
| | | GCLK PLL | $t_{co}$ | 3.086 | 3.320 | 4.726 | 5.145 | 5.673 | 5.530 | 5.733 | 5.280 | 5.813 | 5.668 | 5.804 | ns |
| RSDS | — | GCLK | $t_{co}$ | 3.102 | 3.335 | 4.727 | 5.142 | 5.667 | 5.524 | 5.727 | 5.277 | 5.806 | 5.661 | 5.797 | ns |
| | | GCLK PLL | $t_{co}$ | 3.091 | 3.325 | 4.723 | 5.138 | 5.664 | 5.521 | 5.724 | 5.274 | 5.803 | 5.658 | 5.794 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.088 | 3.322 | 4.721 | 5.136 | 5.662 | 5.519 | 5.722 | 5.272 | 5.802 | 5.657 | 5.793 | ns |
| | | GCLK PLL | $t_{co}$ | 3.099 | 3.332 | 4.722 | 5.137 | 5.661 | 5.518 | 5.721 | 5.271 | 5.800 | 5.655 | 5.791 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.089 | 3.323 | 4.720 | 5.135 | 5.660 | 5.517 | 5.720 | 5.271 | 5.800 | 5.655 | 5.791 | ns |
| | | GCLK PLL | $t_{co}$ | 3.075 | 3.309 | 4.705 | 5.120 | 5.646 | 5.503 | 5.706 | 5.256 | 5.785 | 5.640 | 5.776 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.072 | 3.305 | 4.701 | 5.116 | 5.642 | 5.499 | 5.702 | 5.252 | 5.781 | 5.636 | 5.772 | ns |
| | | GCLK PLL | $t_{co}$ | 3.069 | 3.303 | 4.702 | 5.119 | 5.645 | 5.502 | 5.705 | 5.255 | 5.785 | 5.640 | 5.776 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.070 | 3.303 | 4.692 | 5.107 | 5.632 | 5.489 | 5.692 | 5.242 | 5.771 | 5.626 | 5.762 | ns |
| | | GCLK PLL | $t_{co}$ | 3.119 | 3.356 | 4.763 | 5.180 | 5.708 | 5.565 | 5.768 | 5.316 | 5.847 | 5.702 | 5.838 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.095 | 3.332 | 4.745 | 5.163 | 5.691 | 5.548 | 5.751 | 5.299 | 5.832 | 5.687 | 5.823 | ns |
| | | GCLK PLL | $t_{co}$ | 3.077 | 3.313 | 4.723 | 5.141 | 5.669 | 5.526 | 5.729 | 5.277 | 5.810 | 5.665 | 5.801 | ns |

**Table 1–108.** EP3SE50 Row Pins Output Timing Parameters (Part 2 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.123 | 3.359 | 4.763 | 5.180 | 5.707 | 5.564 | 5.767 | 5.316 | 5.847 | 5.702 | 5.838 | ns |
| | | GCLK PLL | $t_{co}$ | 3.108 | 3.344 | 4.749 | 5.165 | 5.692 | 5.549 | 5.752 | 5.301 | 5.832 | 5.687 | 5.823 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.097 | 3.333 | 4.744 | 5.162 | 5.689 | 5.546 | 5.749 | 5.298 | 5.830 | 5.685 | 5.821 | ns |
| | | GCLK PLL | $t_{co}$ | 3.077 | 3.313 | 4.721 | 5.138 | 5.666 | 5.523 | 5.726 | 5.275 | 5.806 | 5.661 | 5.797 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.074 | 3.309 | 4.717 | 5.135 | 5.662 | 5.519 | 5.722 | 5.271 | 5.803 | 5.658 | 5.794 | ns |
| | | GCLK PLL | $t_{co}$ | 3.079 | 3.313 | 4.708 | 5.123 | 5.648 | 5.505 | 5.708 | 5.258 | 5.787 | 5.642 | 5.778 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.072 | 3.306 | 4.707 | 5.124 | 5.651 | 5.508 | 5.711 | 5.261 | 5.792 | 5.647 | 5.783 | ns |
| | | GCLK PLL | $t_{co}$ | 3.100 | 3.335 | 4.735 | 5.151 | 5.677 | 5.534 | 5.737 | 5.287 | 5.817 | 5.672 | 5.808 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.082 | 3.318 | 4.720 | 5.136 | 5.662 | 5.519 | 5.722 | 5.272 | 5.802 | 5.657 | 5.793 | ns |
| | | GCLK PLL | $t_{co}$ | 3.068 | 3.302 | 4.697 | 5.112 | 5.637 | 5.494 | 5.697 | 5.248 | 5.777 | 5.632 | 5.768 | ns |
| | 8mA | GCLK | $t_{co}$ | 2.674 | 2.849 | 3.990 | 4.359 | 4.834 | 4.699 | 4.910 | 4.467 | 4.945 | 4.809 | 4.961 | ns |
| | | GCLK PLL | $t_{co}$ | 3.068 | 3.295 | 4.657 | 5.068 | 5.588 | 5.445 | 5.648 | 5.200 | 5.724 | 5.579 | 5.715 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.050 | 3.285 | 4.695 | 5.114 | 5.642 | 5.499 | 5.702 | 5.251 | 5.785 | 5.640 | 5.776 | ns |
| | | GCLK PLL | $t_{co}$ | 2.674 | 2.849 | 3.990 | 4.359 | 4.834 | 4.699 | 4.910 | 4.467 | 4.945 | 4.809 | 4.961 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.068 | 3.295 | 4.657 | 5.068 | 5.588 | 5.445 | 5.648 | 5.200 | 5.724 | 5.579 | 5.715 | ns |
| | | GCLK PLL | $t_{co}$ | 3.050 | 3.285 | 4.695 | 5.114 | 5.642 | 5.499 | 5.702 | 5.251 | 5.785 | 5.640 | 5.776 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 2.674 | 2.849 | 3.990 | 4.359 | 4.834 | 4.699 | 4.910 | 4.467 | 4.945 | 4.809 | 4.961 | ns |
| | | GCLK PLL | $t_{co}$ | 3.068 | 3.295 | 4.657 | 5.068 | 5.588 | 5.445 | 5.648 | 5.200 | 5.724 | 5.579 | 5.715 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.050 | 3.285 | 4.695 | 5.114 | 5.642 | 5.499 | 5.702 | 5.251 | 5.785 | 5.640 | 5.776 | ns |
| | | GCLK PLL | $t_{co}$ | 3.104 | 3.338 | 4.741 | 5.158 | 5.685 | 5.542 | 5.745 | 5.294 | 5.824 | 5.679 | 5.815 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.090 | 3.324 | 4.728 | 5.145 | 5.672 | 5.529 | 5.732 | 5.280 | 5.811 | 5.666 | 5.802 | ns |
| | | GCLK PLL | $t_{co}$ | 3.086 | 3.320 | 4.726 | 5.145 | 5.673 | 5.530 | 5.733 | 5.280 | 5.813 | 5.668 | 5.804 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.102 | 3.335 | 4.727 | 5.142 | 5.667 | 5.524 | 5.727 | 5.277 | 5.806 | 5.661 | 5.797 | ns |
| | | GCLK PLL | $t_{co}$ | 3.091 | 3.325 | 4.723 | 5.138 | 5.664 | 5.521 | 5.724 | 5.274 | 5.803 | 5.658 | 5.794 | ns |


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**Table 1–108.** EP3SE50 Row Pins Output Timing Parameters (Part 3 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.088 | 3.322 | 4.721 | 5.136 | 5.662 | 5.519 | 5.722 | 5.272 | 5.802 | 5.657 | 5.793 | ns |
| | | GCLK PLL | $t_{co}$ | 3.099 | 3.332 | 4.722 | 5.137 | 5.661 | 5.518 | 5.721 | 5.271 | 5.800 | 5.655 | 5.791 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.089 | 3.323 | 4.720 | 5.135 | 5.660 | 5.517 | 5.720 | 5.271 | 5.800 | 5.655 | 5.791 | ns |
| | | GCLK PLL | $t_{co}$ | 3.075 | 3.309 | 4.705 | 5.120 | 5.646 | 5.503 | 5.706 | 5.256 | 5.785 | 5.640 | 5.776 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.072 | 3.305 | 4.701 | 5.116 | 5.642 | 5.499 | 5.702 | 5.252 | 5.781 | 5.636 | 5.772 | ns |
| | | GCLK PLL | $t_{co}$ | 3.069 | 3.303 | 4.702 | 5.119 | 5.645 | 5.502 | 5.705 | 5.255 | 5.785 | 5.640 | 5.776 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.070 | 3.303 | 4.692 | 5.107 | 5.632 | 5.489 | 5.692 | 5.242 | 5.771 | 5.626 | 5.762 | ns |
| | | GCLK PLL | $t_{co}$ | 3.119 | 3.356 | 4.763 | 5.180 | 5.708 | 5.565 | 5.768 | 5.316 | 5.847 | 5.702 | 5.838 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.095 | 3.332 | 4.745 | 5.163 | 5.691 | 5.548 | 5.751 | 5.299 | 5.832 | 5.687 | 5.823 | ns |
| | | GCLK PLL | $t_{co}$ | 3.077 | 3.313 | 4.723 | 5.141 | 5.669 | 5.526 | 5.729 | 5.277 | 5.810 | 5.665 | 5.801 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.123 | 3.359 | 4.763 | 5.180 | 5.707 | 5.564 | 5.767 | 5.316 | 5.847 | 5.702 | 5.838 | ns |
| | | GCLK PLL | $t_{co}$ | 3.108 | 3.344 | 4.749 | 5.165 | 5.692 | 5.549 | 5.752 | 5.301 | 5.832 | 5.687 | 5.823 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.097 | 3.333 | 4.744 | 5.162 | 5.689 | 5.546 | 5.749 | 5.298 | 5.830 | 5.685 | 5.821 | ns |
| | | GCLK PLL | $t_{co}$ | 3.077 | 3.313 | 4.721 | 5.138 | 5.666 | 5.523 | 5.726 | 5.275 | 5.806 | 5.661 | 5.797 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.074 | 3.309 | 4.717 | 5.135 | 5.662 | 5.519 | 5.722 | 5.271 | 5.803 | 5.658 | 5.794 | ns |
| | | GCLK PLL | $t_{co}$ | 3.079 | 3.313 | 4.708 | 5.123 | 5.648 | 5.505 | 5.708 | 5.258 | 5.787 | 5.642 | 5.778 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.072 | 3.306 | 4.707 | 5.124 | 5.651 | 5.508 | 5.711 | 5.261 | 5.792 | 5.647 | 5.783 | ns |
| | | GCLK PLL | $t_{co}$ | 3.100 | 3.335 | 4.735 | 5.151 | 5.677 | 5.534 | 5.737 | 5.287 | 5.817 | 5.672 | 5.808 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.082 | 3.318 | 4.720 | 5.136 | 5.662 | 5.519 | 5.722 | 5.272 | 5.802 | 5.657 | 5.793 | ns |
| | | GCLK PLL | $t_{co}$ | 3.068 | 3.302 | 4.697 | 5.112 | 5.637 | 5.494 | 5.697 | 5.248 | 5.777 | 5.632 | 5.768 | ns |

Table 1–109 and Table 1–110 list the EP3SE50 regional clock (RCLK) adder values that must be added to the GCLK values. Use these adder values to determine I/O timing when the I/O pin is driven using the regional clock. This applies to all I/O standards supported by Stratix III devices.

Table 1–109 lists the EP3SE50 column pin delay adders when using the regional clock in Stratix III devices.

**Table 1–109.** EP3SE50 Column Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.152 | 0.164 | 0.22 | 0.237 | 0.25 | 0.244 | 0.31 | 0.24 | 0.254 | 0.246 | 0.312 | ns |
| RCLK PLL input adder | -0.001 | -0.001 | -0.003 | -0.004 | -0.004 | -0.004 | -0.006 | -0.003 | -0.004 | -0.004 | -0.006 | ns |
| RCLK output adder | -0.116 | -0.119 | -0.134 | -0.136 | -0.17 | -0.171 | -0.249 | -0.131 | -0.13 | -0.13 | -0.216 | ns |
| RCLK PLL output adder | 1.647 | 1.684 | 2.61 | 2.926 | 3.238 | 3.084 | 3.298 | 2.943 | 3.254 | 3.098 | 3.374 | ns |

Table 1–110 lists the EP3SE50 row pin delay adders when using the regional clock in Stratix III devices.

**Table 1–110.** EP3SE50 Row Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.113 | 0.125 | 0.182 | 0.197 | 0.212 | 0.205 | 0.274 | 0.201 | 0.215 | 0.21 | 0.275 | ns |
| RCLK PLL input adder | 0.13 | 0.14 | 0.213 | 0.241 | 0.267 | 0.255 | 0.385 | 0.244 | 0.27 | 0.256 | 0.386 | ns |
| RCLK output adder | -0.116 | -0.129 | -0.186 | -0.202 | -0.218 | -0.209 | -0.28 | -0.206 | -0.221 | -0.214 | -0.283 | ns |
| RCLK PLL output adder | -0.137 | -0.143 | -0.193 | -0.214 | -0.236 | -0.225 | -0.295 | -0.215 | -0.237 | -0.226 | -0.297 | ns |

## EP3SE80 I/O Timing Parameters

Table 1–111 through Table 1–114 list the maximum I/O timing parameters for EP3SE80 devices for single-ended I/O standards.

Table 1–111 lists the EP3SE80 column pins input timing parameters for single-ended I/O standards.

**Table 1–111.** EP3SE80 Column Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -1.054 | -1.054 | -1.505 | -1.636 | -1.872 | -1.819 | -2.173 | -1.636 | -1.872 | -1.819 | -2.173 | ns |
| | | $t_h$ | 1.195 | 1.195 | 1.704 | 1.861 | 2.117 | 2.050 | 2.409 | 1.861 | 2.117 | 2.050 | 2.409 | ns |
| | GCLK PLL | $t_{su}$ | -1.307 | -1.307 | -1.870 | -2.028 | -2.321 | -2.214 | -2.661 | -2.028 | -2.321 | -2.214 | -2.661 | ns |
| | | $t_h$ | 1.605 | 1.605 | 2.302 | 2.513 | 2.858 | 2.721 | 3.186 | 2.513 | 2.858 | 2.721 | 3.186 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -1.054 | -1.054 | -1.505 | -1.636 | -1.872 | -1.819 | -2.173 | -1.636 | -1.872 | -1.819 | -2.173 | ns |
| | | $t_h$ | 1.195 | 1.195 | 1.704 | 1.861 | 2.117 | 2.050 | 2.409 | 1.861 | 2.117 | 2.050 | 2.409 | ns |
| | GCLK PLL | $t_{su}$ | -1.307 | -1.307 | -1.870 | -2.028 | -2.321 | -2.214 | -2.661 | -2.028 | -2.321 | -2.214 | -2.661 | ns |
| | | $t_h$ | 1.605 | 1.605 | 2.302 | 2.513 | 2.858 | 2.721 | 3.186 | 2.513 | 2.858 | 2.721 | 3.186 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -1.065 | -1.065 | -1.504 | -1.638 | -1.871 | -1.818 | -2.172 | -1.638 | -1.871 | -1.818 | -2.172 | ns |
| | | $t_h$ | 1.206 | 1.206 | 1.703 | 1.863 | 2.116 | 2.049 | 2.408 | 1.863 | 2.116 | 2.049 | 2.408 | ns |
| | GCLK PLL | $t_{su}$ | -1.318 | -1.318 | -1.869 | -2.030 | -2.320 | -2.213 | -2.660 | -2.030 | -2.320 | -2.213 | -2.660 | ns |
| | | $t_h$ | 1.616 | 1.616 | 2.301 | 2.515 | 2.857 | 2.720 | 3.185 | 2.515 | 2.857 | 2.720 | 3.185 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -1.065 | -1.065 | -1.504 | -1.638 | -1.871 | -1.818 | -2.172 | -1.638 | -1.871 | -1.818 | -2.172 | ns |
| | | $t_h$ | 1.206 | 1.206 | 1.703 | 1.863 | 2.116 | 2.049 | 2.408 | 1.863 | 2.116 | 2.049 | 2.408 | ns |
| | GCLK PLL | $t_{su}$ | -1.318 | -1.318 | -1.869 | -2.030 | -2.320 | -2.213 | -2.660 | -2.030 | -2.320 | -2.213 | -2.660 | ns |
| | | $t_h$ | 1.616 | 1.616 | 2.301 | 2.515 | 2.857 | 2.720 | 3.185 | 2.515 | 2.857 | 2.720 | 3.185 | ns |
| 2.5 V | GCLK | $t_{su}$ | -1.060 | -1.060 | -1.513 | -1.650 | -1.890 | -1.837 | -2.191 | -1.650 | -1.890 | -1.837 | -2.191 | ns |
| | | $t_h$ | 1.201 | 1.201 | 1.712 | 1.875 | 2.135 | 2.068 | 2.427 | 1.875 | 2.135 | 2.068 | 2.427 | ns |
| | GCLK PLL | $t_{su}$ | -1.313 | -1.313 | -1.878 | -2.042 | -2.339 | -2.232 | -2.679 | -2.042 | -2.339 | -2.232 | -2.679 | ns |
| | | $t_h$ | 1.611 | 1.611 | 2.310 | 2.527 | 2.876 | 2.739 | 3.204 | 2.527 | 2.876 | 2.739 | 3.204 | ns |
| 1.8 V | GCLK | $t_{su}$ | -1.082 | -1.082 | -1.553 | -1.686 | -1.888 | -1.835 | -2.189 | -1.686 | -1.888 | -1.835 | -2.189 | ns |
| | | $t_h$ | 1.225 | 1.225 | 1.752 | 1.911 | 2.133 | 2.066 | 2.425 | 1.911 | 2.133 | 2.066 | 2.425 | ns |
| | GCLK PLL | $t_{su}$ | -1.335 | -1.335 | -1.918 | -2.078 | -2.337 | -2.230 | -2.677 | -2.078 | -2.337 | -2.230 | -2.677 | ns |
| | | $t_h$ | 1.635 | 1.635 | 2.350 | 2.563 | 2.874 | 2.737 | 3.202 | 2.563 | 2.874 | 2.737 | 3.202 | ns |
| 1.5 V | GCLK | $t_{su}$ | -1.072 | -1.072 | -1.530 | -1.654 | -1.818 | -1.765 | -2.119 | -1.654 | -1.818 | -1.765 | -2.119 | ns |
| | | $t_h$ | 1.215 | 1.215 | 1.729 | 1.879 | 2.063 | 1.996 | 2.355 | 1.879 | 2.063 | 1.996 | 2.355 | ns |
| | GCLK PLL | $t_{su}$ | -1.325 | -1.325 | -1.895 | -2.046 | -2.267 | -2.160 | -2.607 | -2.046 | -2.267 | -2.160 | -2.607 | ns |
| | | $t_h$ | 1.625 | 1.625 | 2.327 | 2.531 | 2.804 | 2.667 | 3.132 | 2.531 | 2.804 | 2.667 | 3.132 | ns |
| 1.2 V | GCLK | $t_{su}$ | -1.020 | -1.020 | -1.453 | -1.555 | -1.662 | -1.609 | -1.963 | -1.555 | -1.662 | -1.609 | -1.963 | ns |
| | | $t_h$ | 1.163 | 1.163 | 1.652 | 1.780 | 1.907 | 1.840 | 2.199 | 1.780 | 1.907 | 1.840 | 2.199 | ns |
| | GCLK PLL | $t_{su}$ | -1.273 | -1.273 | -1.818 | -1.947 | -2.111 | -2.004 | -2.451 | -1.947 | -2.111 | -2.004 | -2.451 | ns |
| | | $t_h$ | 1.573 | 1.573 | 2.250 | 2.432 | 2.648 | 2.511 | 2.976 | 2.432 | 2.648 | 2.511 | 2.976 | ns |

**Table 1–111.** EP3SE80 Column Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -0.991 | -0.991 | -1.425 | -1.539 | -1.664 | -1.611 | -1.965 | -1.539 | -1.664 | -1.611 | -1.965 | ns |
| | | $t_h$ | 1.134 | 1.134 | 1.624 | 1.764 | 1.909 | 1.842 | 2.201 | 1.764 | 1.909 | 1.842 | 2.201 | ns |
| | GCLK PLL | $t_{su}$ | -1.244 | -1.244 | -1.790 | -1.931 | -2.113 | -2.006 | -2.453 | -1.931 | -2.113 | -2.006 | -2.453 | ns |
| | | $t_h$ | 1.544 | 1.544 | 2.222 | 2.416 | 2.650 | 2.513 | 2.978 | 2.416 | 2.650 | 2.513 | 2.978 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -0.991 | -0.991 | -1.425 | -1.539 | -1.664 | -1.611 | -1.965 | -1.539 | -1.664 | -1.611 | -1.965 | ns |
| | | $t_h$ | 1.134 | 1.134 | 1.624 | 1.764 | 1.909 | 1.842 | 2.201 | 1.764 | 1.909 | 1.842 | 2.201 | ns |
| | GCLK PLL | $t_{su}$ | -1.244 | -1.244 | -1.790 | -1.931 | -2.113 | -2.006 | -2.453 | -1.931 | -2.113 | -2.006 | -2.453 | ns |
| | | $t_h$ | 1.544 | 1.544 | 2.222 | 2.416 | 2.650 | 2.513 | 2.978 | 2.416 | 2.650 | 2.513 | 2.978 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -0.985 | -0.985 | -1.412 | -1.531 | -1.661 | -1.606 | -1.963 | -1.531 | -1.661 | -1.606 | -1.963 | ns |
| | | $t_h$ | 1.128 | 1.128 | 1.611 | 1.753 | 1.903 | 1.836 | 2.194 | 1.753 | 1.903 | 1.836 | 2.194 | ns |
| | GCLK PLL | $t_{su}$ | -1.238 | -1.238 | -1.777 | -1.923 | -2.110 | -2.001 | -2.451 | -1.923 | -2.110 | -2.001 | -2.451 | ns |
| | | $t_h$ | 1.538 | 1.538 | 2.209 | 2.405 | 2.644 | 2.507 | 2.971 | 2.405 | 2.644 | 2.507 | 2.971 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -0.985 | -0.985 | -1.412 | -1.531 | -1.661 | -1.606 | -1.963 | -1.531 | -1.661 | -1.606 | -1.963 | ns |
| | | $t_h$ | 1.128 | 1.128 | 1.611 | 1.753 | 1.903 | 1.836 | 2.194 | 1.753 | 1.903 | 1.836 | 2.194 | ns |
| | GCLK PLL | $t_{su}$ | -1.238 | -1.238 | -1.777 | -1.923 | -2.110 | -2.001 | -2.451 | -1.923 | -2.110 | -2.001 | -2.451 | ns |
| | | $t_h$ | 1.538 | 1.538 | 2.209 | 2.405 | 2.644 | 2.507 | 2.971 | 2.405 | 2.644 | 2.507 | 2.971 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -0.974 | -0.974 | -1.401 | -1.520 | -1.642 | -1.587 | -1.944 | -1.520 | -1.642 | -1.587 | -1.944 | ns |
| | | $t_h$ | 1.117 | 1.117 | 1.599 | 1.742 | 1.884 | 1.817 | 2.175 | 1.742 | 1.884 | 1.817 | 2.175 | ns |
| | GCLK PLL | $t_{su}$ | -1.227 | -1.227 | -1.766 | -1.912 | -2.091 | -1.982 | -2.432 | -1.912 | -2.091 | -1.982 | -2.432 | ns |
| | | $t_h$ | 1.527 | 1.527 | 2.197 | 2.394 | 2.625 | 2.488 | 2.952 | 2.394 | 2.625 | 2.488 | 2.952 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.974 | -0.974 | -1.401 | -1.520 | -1.642 | -1.587 | -1.944 | -1.520 | -1.642 | -1.587 | -1.944 | ns |
| | | $t_h$ | 1.117 | 1.117 | 1.599 | 1.742 | 1.884 | 1.817 | 2.175 | 1.742 | 1.884 | 1.817 | 2.175 | ns |
| | GCLK PLL | $t_{su}$ | -1.227 | -1.227 | -1.766 | -1.912 | -2.091 | -1.982 | -2.432 | -1.912 | -2.091 | -1.982 | -2.432 | ns |
| | | $t_h$ | 1.527 | 1.527 | 2.197 | 2.394 | 2.625 | 2.488 | 2.952 | 2.394 | 2.625 | 2.488 | 2.952 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.985 | -0.985 | -1.412 | -1.531 | -1.661 | -1.606 | -1.963 | -1.531 | -1.661 | -1.606 | -1.963 | ns |
| | | $t_h$ | 1.128 | 1.128 | 1.611 | 1.753 | 1.903 | 1.836 | 2.194 | 1.753 | 1.903 | 1.836 | 2.194 | ns |
| | GCLK PLL | $t_{su}$ | -1.238 | -1.238 | -1.777 | -1.923 | -2.110 | -2.001 | -2.451 | -1.923 | -2.110 | -2.001 | -2.451 | ns |
| | | $t_h$ | 1.538 | 1.538 | 2.209 | 2.405 | 2.644 | 2.507 | 2.971 | 2.405 | 2.644 | 2.507 | 2.971 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.985 | -0.985 | -1.412 | -1.531 | -1.661 | -1.606 | -1.963 | -1.531 | -1.661 | -1.606 | -1.963 | ns |
| | | $t_h$ | 1.128 | 1.128 | 1.611 | 1.753 | 1.903 | 1.836 | 2.194 | 1.753 | 1.903 | 1.836 | 2.194 | ns |
| | GCLK PLL | $t_{su}$ | -1.238 | -1.238 | -1.777 | -1.923 | -2.110 | -2.001 | -2.451 | -1.923 | -2.110 | -2.001 | -2.451 | ns |
| | | $t_h$ | 1.538 | 1.538 | 2.209 | 2.405 | 2.644 | 2.507 | 2.971 | 2.405 | 2.644 | 2.507 | 2.971 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.974 | -0.974 | -1.401 | -1.520 | -1.642 | -1.587 | -1.944 | -1.520 | -1.642 | -1.587 | -1.944 | ns |
| | | $t_h$ | 1.117 | 1.117 | 1.599 | 1.742 | 1.884 | 1.817 | 2.175 | 1.742 | 1.884 | 1.817 | 2.175 | ns |
| | GCLK PLL | $t_{su}$ | -1.227 | -1.227 | -1.766 | -1.912 | -2.091 | -1.982 | -2.432 | -1.912 | -2.091 | -1.982 | -2.432 | ns |
| | | $t_h$ | 1.527 | 1.527 | 2.197 | 2.394 | 2.625 | 2.488 | 2.952 | 2.394 | 2.625 | 2.488 | 2.952 | ns |


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**Table 1–111.** EP3SE80 Column Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.974 | -0.974 | -1.401 | -1.520 | -1.642 | -1.587 | -1.944 | -1.520 | -1.642 | -1.587 | -1.944 | ns |
| | | $t_h$ | 1.117 | 1.117 | 1.599 | 1.742 | 1.884 | 1.817 | 2.175 | 1.742 | 1.884 | 1.817 | 2.175 | ns |
| | GCLK PLL | $t_{su}$ | -1.227 | -1.227 | -1.766 | -1.912 | -2.091 | -1.982 | -2.432 | -1.912 | -2.091 | -1.982 | -2.432 | ns |
| | | $t_h$ | 1.527 | 1.527 | 2.197 | 2.394 | 2.625 | 2.488 | 2.952 | 2.394 | 2.625 | 2.488 | 2.952 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.962 | -0.962 | -1.391 | -1.509 | -1.626 | -1.571 | -1.928 | -1.509 | -1.626 | -1.571 | -1.928 | ns |
| | | $t_h$ | 1.105 | 1.105 | 1.589 | 1.731 | 1.868 | 1.801 | 2.159 | 1.731 | 1.868 | 1.801 | 2.159 | ns |
| | GCLK PLL | $t_{su}$ | -1.215 | -1.215 | -1.756 | -1.901 | -2.075 | -1.966 | -2.416 | -1.901 | -2.075 | -1.966 | -2.416 | ns |
| | | $t_h$ | 1.515 | 1.515 | 2.187 | 2.383 | 2.609 | 2.472 | 2.936 | 2.383 | 2.609 | 2.472 | 2.936 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -0.962 | -0.962 | -1.391 | -1.509 | -1.626 | -1.571 | -1.928 | -1.509 | -1.626 | -1.571 | -1.928 | ns |
| | | $t_h$ | 1.105 | 1.105 | 1.589 | 1.731 | 1.868 | 1.801 | 2.159 | 1.731 | 1.868 | 1.801 | 2.159 | ns |
| | GCLK PLL | $t_{su}$ | -1.215 | -1.215 | -1.756 | -1.901 | -2.075 | -1.966 | -2.416 | -1.901 | -2.075 | -1.966 | -2.416 | ns |
| | | $t_h$ | 1.515 | 1.515 | 2.187 | 2.383 | 2.609 | 2.472 | 2.936 | 2.383 | 2.609 | 2.472 | 2.936 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | -1.065 | -1.065 | -1.504 | -1.638 | -1.871 | -1.818 | -2.172 | -1.638 | -1.871 | -1.818 | -2.172 | ns |
| | | $t_h$ | 1.206 | 1.206 | 1.703 | 1.863 | 2.116 | 2.049 | 2.408 | 1.863 | 2.116 | 2.049 | 2.408 | ns |
| | GCLK PLL | $t_{su}$ | -1.318 | -1.318 | -1.869 | -2.030 | -2.320 | -2.213 | -2.660 | -2.030 | -2.320 | -2.213 | -2.660 | ns |
| | | $t_h$ | 1.616 | 1.616 | 2.301 | 2.515 | 2.857 | 2.720 | 3.185 | 2.515 | 2.857 | 2.720 | 3.185 | ns |

Table 1–112 lists the EP3SE80 row pins input timing parameters for single-ended I/O standards.

**Table 1–112.** EP3SE80 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -0.922 | -0.964 | -1.369 | -1.481 | -1.595 | -1.647 | -1.890 | -1.492 | -1.697 | -1.649 | -1.929 | ns |
| | | $t_h$ | 1.045 | 1.103 | 1.566 | 1.703 | 1.842 | 1.878 | 2.128 | 1.725 | 1.950 | 1.890 | 2.168 | ns |
| | GCLK PLL | $t_{su}$ | 1.087 | 1.110 | 1.770 | 2.000 | 1.985 | 2.004 | 1.799 | 2.012 | 2.003 | 2.024 | 1.850 | ns |
| | | $t_h$ | -0.825 | -0.830 | -1.353 | -1.532 | -1.470 | -1.513 | -1.300 | -1.533 | -1.477 | -1.523 | -1.349 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -0.922 | -0.964 | -1.369 | -1.481 | -1.595 | -1.647 | -1.890 | -1.492 | -1.697 | -1.649 | -1.929 | ns |
| | | $t_h$ | 1.045 | 1.103 | 1.566 | 1.703 | 1.842 | 1.878 | 2.128 | 1.725 | 1.950 | 1.890 | 2.168 | ns |
| | GCLK PLL | $t_{su}$ | 1.087 | 1.110 | 1.770 | 2.000 | 1.985 | 2.004 | 1.799 | 2.012 | 2.003 | 2.024 | 1.850 | ns |
| | | $t_h$ | -0.825 | -0.830 | -1.353 | -1.532 | -1.470 | -1.513 | -1.300 | -1.533 | -1.477 | -1.523 | -1.349 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -0.928 | -0.975 | -1.366 | -1.482 | -1.598 | -1.650 | -1.893 | -1.491 | -1.702 | -1.654 | -1.934 | ns |
| | | $t_h$ | 1.051 | 1.114 | 1.563 | 1.704 | 1.845 | 1.881 | 2.131 | 1.724 | 1.955 | 1.895 | 2.173 | ns |
| | GCLK PLL | $t_{su}$ | 1.081 | 1.099 | 1.773 | 1.999 | 1.982 | 2.001 | 1.796 | 2.013 | 1.998 | 2.019 | 1.845 | ns |
| | | $t_h$ | -0.819 | -0.819 | -1.356 | -1.531 | -1.467 | -1.510 | -1.297 | -1.534 | -1.472 | -1.518 | -1.344 | ns |

**Table 1–112.** EP3SE80 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -0.928 | -0.975 | -1.366 | -1.482 | -1.598 | -1.650 | -1.893 | -1.491 | -1.702 | -1.654 | -1.934 | ns |
| | | $t_h$ | 1.051 | 1.114 | 1.563 | 1.704 | 1.845 | 1.881 | 2.131 | 1.724 | 1.955 | 1.895 | 2.173 | ns |
| | GCLK PLL | $t_{su}$ | 1.081 | 1.099 | 1.773 | 1.999 | 1.982 | 2.001 | 1.796 | 2.013 | 1.998 | 2.019 | 1.845 | ns |
| | | $t_h$ | -0.819 | -0.819 | -1.356 | -1.531 | -1.467 | -1.510 | -1.297 | -1.534 | -1.472 | -1.518 | -1.344 | ns |
| 2.5 V | GCLK | $t_{su}$ | -0.916 | -0.968 | -1.375 | -1.495 | -1.613 | -1.665 | -1.908 | -1.500 | -1.712 | -1.664 | -1.944 | ns |
| | | $t_h$ | 1.039 | 1.107 | 1.572 | 1.717 | 1.860 | 1.896 | 2.146 | 1.733 | 1.965 | 1.905 | 2.183 | ns |
| | GCLK PLL | $t_{su}$ | 1.093 | 1.106 | 1.764 | 1.986 | 1.967 | 1.986 | 1.781 | 2.004 | 1.988 | 2.009 | 1.835 | ns |
| | | $t_h$ | -0.831 | -0.826 | -1.347 | -1.518 | -1.452 | -1.495 | -1.282 | -1.525 | -1.462 | -1.508 | -1.334 | ns |
| 1.8 V | GCLK | $t_{su}$ | -0.973 | -1.027 | -1.441 | -1.555 | -1.741 | -1.689 | -1.906 | -1.560 | -1.739 | -1.691 | -1.945 | ns |
| | | $t_h$ | 1.097 | 1.167 | 1.638 | 1.777 | 1.984 | 1.920 | 2.144 | 1.792 | 1.992 | 1.931 | 2.184 | ns |
| | GCLK PLL | $t_{su}$ | 0.974 | 0.984 | 1.606 | 1.824 | 1.969 | 1.854 | 1.783 | 1.837 | 1.987 | 1.870 | 1.834 | ns |
| | | $t_h$ | -0.714 | -0.705 | -1.192 | -1.359 | -1.454 | -1.366 | -1.284 | -1.362 | -1.461 | -1.373 | -1.333 | ns |
| 1.5 V | GCLK | $t_{su}$ | -0.963 | -1.016 | -1.417 | -1.523 | -1.673 | -1.621 | -1.838 | -1.529 | -1.674 | -1.626 | -1.880 | ns |
| | | $t_h$ | 1.087 | 1.156 | 1.614 | 1.745 | 1.916 | 1.852 | 2.076 | 1.761 | 1.927 | 1.866 | 2.119 | ns |
| | GCLK PLL | $t_{su}$ | 0.984 | 0.995 | 1.630 | 1.856 | 2.037 | 1.922 | 1.851 | 1.868 | 2.052 | 1.935 | 1.899 | ns |
| | | $t_h$ | -0.724 | -0.716 | -1.216 | -1.391 | -1.522 | -1.434 | -1.352 | -1.393 | -1.526 | -1.438 | -1.398 | ns |
| 1.2 V | GCLK | $t_{su}$ | -0.903 | -0.963 | -1.338 | -1.422 | -1.514 | -1.462 | -1.679 | -1.433 | -1.519 | -1.471 | -1.725 | ns |
| | | $t_h$ | 1.027 | 1.103 | 1.535 | 1.644 | 1.757 | 1.693 | 1.917 | 1.665 | 1.772 | 1.711 | 1.964 | ns |
| | GCLK PLL | $t_{su}$ | 1.044 | 1.048 | 1.709 | 1.957 | 2.196 | 2.081 | 2.010 | 1.964 | 2.207 | 2.090 | 2.054 | ns |
| | | $t_h$ | -0.784 | -0.769 | -1.295 | -1.492 | -1.681 | -1.593 | -1.511 | -1.489 | -1.681 | -1.593 | -1.553 | ns |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -0.859 | -0.910 | -1.289 | -1.386 | -1.393 | -1.445 | -1.688 | -1.388 | -1.495 | -1.447 | -1.727 | ns |
| | | $t_h$ | 0.983 | 1.050 | 1.486 | 1.608 | 1.640 | 1.676 | 1.926 | 1.621 | 1.748 | 1.688 | 1.966 | ns |
| | GCLK PLL | $t_{su}$ | 1.151 | 1.165 | 1.850 | 2.095 | 2.187 | 2.206 | 2.001 | 2.116 | 2.205 | 2.226 | 2.052 | ns |
| | | $t_h$ | -0.888 | -0.884 | -1.433 | -1.627 | -1.672 | -1.715 | -1.502 | -1.637 | -1.679 | -1.725 | -1.551 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -0.859 | -0.910 | -1.289 | -1.386 | -1.393 | -1.445 | -1.688 | -1.388 | -1.495 | -1.447 | -1.727 | ns |
| | | $t_h$ | 0.983 | 1.050 | 1.486 | 1.608 | 1.640 | 1.676 | 1.926 | 1.621 | 1.748 | 1.688 | 1.966 | ns |
| | GCLK PLL | $t_{su}$ | 1.151 | 1.165 | 1.850 | 2.095 | 2.187 | 2.206 | 2.001 | 2.116 | 2.205 | 2.226 | 2.052 | ns |
| | | $t_h$ | -0.888 | -0.884 | -1.433 | -1.627 | -1.672 | -1.715 | -1.502 | -1.637 | -1.679 | -1.725 | -1.551 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -0.877 | -0.928 | -1.300 | -1.395 | -1.509 | -1.456 | -1.677 | -1.401 | -1.512 | -1.463 | -1.720 | ns |
| | | $t_h$ | 1.001 | 1.068 | 1.497 | 1.615 | 1.750 | 1.686 | 1.911 | 1.631 | 1.762 | 1.702 | 1.955 | ns |
| | GCLK PLL | $t_{su}$ | 1.070 | 1.083 | 1.747 | 1.984 | 2.201 | 2.087 | 2.014 | 1.996 | 2.214 | 2.098 | 2.061 | ns |
| | | $t_h$ | -0.810 | -0.804 | -1.333 | -1.521 | -1.688 | -1.600 | -1.519 | -1.523 | -1.691 | -1.602 | -1.564 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -0.877 | -0.928 | -1.300 | -1.395 | -1.509 | -1.456 | -1.677 | -1.401 | -1.512 | -1.463 | -1.720 | ns |
| | | $t_h$ | 1.001 | 1.068 | 1.497 | 1.615 | 1.750 | 1.686 | 1.911 | 1.631 | 1.762 | 1.702 | 1.955 | ns |
| | GCLK PLL | $t_{su}$ | 1.070 | 1.083 | 1.747 | 1.984 | 2.201 | 2.087 | 2.014 | 1.996 | 2.214 | 2.098 | 2.061 | ns |
| | | $t_h$ | -0.810 | -0.804 | -1.333 | -1.521 | -1.688 | -1.600 | -1.519 | -1.523 | -1.691 | -1.602 | -1.564 | ns |

**Table 1–112.** EP3SE80 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -0.863 | -0.916 | -1.285 | -1.385 | -1.491 | -1.438 | -1.659 | -1.390 | -1.495 | -1.446 | -1.703 | ns |
| | | $t_h$ | 0.987 | 1.056 | 1.483 | 1.605 | 1.732 | 1.668 | 1.893 | 1.620 | 1.745 | 1.685 | 1.938 | ns |
| | GCLK PLL | $t_{su}$ | 1.084 | 1.095 | 1.762 | 1.994 | 2.219 | 2.105 | 2.032 | 2.007 | 2.231 | 2.115 | 2.078 | ns |
| | | $t_h$ | -0.824 | -0.816 | -1.347 | -1.531 | -1.706 | -1.618 | -1.537 | -1.534 | -1.708 | -1.619 | -1.581 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.877 | -0.928 | -1.300 | -1.395 | -1.509 | -1.456 | -1.677 | -1.401 | -1.512 | -1.463 | -1.720 | ns |
| | | $t_h$ | 1.001 | 1.068 | 1.497 | 1.615 | 1.750 | 1.686 | 1.911 | 1.631 | 1.762 | 1.702 | 1.955 | ns |
| | GCLK PLL | $t_{su}$ | 1.070 | 1.083 | 1.747 | 1.984 | 2.201 | 2.087 | 2.014 | 1.996 | 2.214 | 2.098 | 2.061 | ns |
| | | $t_h$ | -0.810 | -0.804 | -1.333 | -1.521 | -1.688 | -1.600 | -1.519 | -1.523 | -1.691 | -1.602 | -1.564 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.877 | -0.928 | -1.300 | -1.395 | -1.509 | -1.456 | -1.677 | -1.401 | -1.512 | -1.463 | -1.720 | ns |
| | | $t_h$ | 1.001 | 1.068 | 1.497 | 1.615 | 1.750 | 1.686 | 1.911 | 1.631 | 1.762 | 1.702 | 1.955 | ns |
| | GCLK PLL | $t_{su}$ | 1.070 | 1.083 | 1.747 | 1.984 | 2.201 | 2.087 | 2.014 | 1.996 | 2.214 | 2.098 | 2.061 | ns |
| | | $t_h$ | -0.810 | -0.804 | -1.333 | -1.521 | -1.688 | -1.600 | -1.519 | -1.523 | -1.691 | -1.602 | -1.564 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.863 | -0.916 | -1.285 | -1.385 | -1.491 | -1.438 | -1.659 | -1.390 | -1.495 | -1.446 | -1.703 | ns |
| | | $t_h$ | 0.987 | 1.056 | 1.483 | 1.605 | 1.732 | 1.668 | 1.893 | 1.620 | 1.745 | 1.685 | 1.938 | ns |
| | GCLK PLL | $t_{su}$ | 1.084 | 1.095 | 1.762 | 1.994 | 2.219 | 2.105 | 2.032 | 2.007 | 2.231 | 2.115 | 2.078 | ns |
| | | $t_h$ | -0.824 | -0.816 | -1.347 | -1.531 | -1.706 | -1.618 | -1.537 | -1.534 | -1.708 | -1.619 | -1.581 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.863 | -0.916 | -1.285 | -1.385 | -1.491 | -1.438 | -1.659 | -1.390 | -1.495 | -1.446 | -1.703 | ns |
| | | $t_h$ | 0.987 | 1.056 | 1.483 | 1.605 | 1.732 | 1.668 | 1.893 | 1.620 | 1.745 | 1.685 | 1.938 | ns |
| | GCLK PLL | $t_{su}$ | 1.084 | 1.095 | 1.762 | 1.994 | 2.219 | 2.105 | 2.032 | 2.007 | 2.231 | 2.115 | 2.078 | ns |
| | | $t_h$ | -0.824 | -0.816 | -1.347 | -1.531 | -1.706 | -1.618 | -1.537 | -1.534 | -1.708 | -1.619 | -1.581 | ns |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.854 | -0.904 | -1.276 | -1.375 | -1.475 | -1.422 | -1.643 | -1.381 | -1.479 | -1.430 | -1.687 | ns |
| | | $t_h$ | 0.978 | 1.044 | 1.474 | 1.595 | 1.716 | 1.652 | 1.877 | 1.611 | 1.729 | 1.669 | 1.922 | ns |
| | GCLK PLL | $t_{su}$ | 1.093 | 1.107 | 1.771 | 2.004 | 2.235 | 2.121 | 2.048 | 2.016 | 2.247 | 2.131 | 2.094 | ns |
| | | $t_h$ | -0.833 | -0.828 | -1.356 | -1.541 | -1.722 | -1.634 | -1.553 | -1.543 | -1.724 | -1.635 | -1.597 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.854 | -0.904 | -1.276 | -1.375 | -1.475 | -1.422 | -1.643 | -1.381 | -1.479 | -1.430 | -1.687 | ns |
| | | $t_h$ | 0.978 | 1.044 | 1.474 | 1.595 | 1.716 | 1.652 | 1.877 | 1.611 | 1.729 | 1.669 | 1.922 | ns |
| | GCLK PLL | $t_{su}$ | 1.093 | 1.107 | 1.771 | 2.004 | 2.235 | 2.121 | 2.048 | 2.016 | 2.247 | 2.131 | 2.094 | ns |
| | | $t_h$ | -0.833 | -0.828 | -1.356 | -1.541 | -1.722 | -1.634 | -1.553 | -1.543 | -1.724 | -1.635 | -1.597 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -0.928 | -0.975 | -1.366 | -1.482 | -1.598 | -1.650 | -1.893 | -1.491 | -1.702 | -1.654 | -1.934 | ns |
| | | $t_h$ | 1.051 | 1.114 | 1.563 | 1.704 | 1.845 | 1.881 | 2.131 | 1.724 | 1.955 | 1.895 | 2.173 | ns |
| | GCLK PLL | $t_{su}$ | 1.081 | 1.099 | 1.773 | 1.999 | 1.982 | 2.001 | 1.796 | 2.013 | 1.998 | 2.019 | 1.845 | ns |
| | | $t_h$ | -0.819 | -0.819 | -1.356 | -1.531 | -1.467 | -1.510 | -1.297 | -1.534 | -1.472 | -1.518 | -1.344 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | -0.928 | -0.975 | -1.366 | -1.482 | -1.598 | -1.650 | -1.893 | -1.491 | -1.702 | -1.654 | -1.934 | ns |
| | | $t_h$ | 1.051 | 1.114 | 1.563 | 1.704 | 1.845 | 1.881 | 2.131 | 1.724 | 1.955 | 1.895 | 2.173 | ns |
| | GCLK PLL | $t_{su}$ | 1.081 | 1.099 | 1.773 | 1.999 | 1.982 | 2.001 | 1.796 | 2.013 | 1.998 | 2.019 | 1.845 | ns |
| | | $t_h$ | -0.819 | -0.819 | -1.356 | -1.531 | -1.467 | -1.510 | -1.297 | -1.534 | -1.472 | -1.518 | -1.344 | ns |

Table 1–113 lists the EP3SE80 column pins output timing parameters for single-ended I/O standards.

**Table 1–113.** EP3SE80 Column Pins Output Timing Parameters (Part 1 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.559 | 3.559 | 4.935 | 5.323 | 5.638 | 5.693 | 5.865 | 5.323 | 5.638 | 5.693 | 5.865 | ns |
| | | GCLK PLL | $t_{co}$ | 3.859 | 3.865 | 5.394 | 5.826 | 6.396 | 6.210 | 6.631 | 5.826 | 6.396 | 6.210 | 6.631 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.442 | 3.442 | 4.781 | 5.161 | 5.525 | 5.523 | 5.752 | 5.161 | 5.525 | 5.523 | 5.752 | ns |
| | | GCLK PLL | $t_{co}$ | 3.792 | 3.798 | 5.285 | 5.715 | 6.283 | 6.097 | 6.518 | 5.715 | 6.283 | 6.097 | 6.518 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.347 | 3.347 | 4.644 | 5.018 | 5.433 | 5.371 | 5.660 | 5.018 | 5.433 | 5.371 | 5.660 | ns |
| | | GCLK PLL | $t_{co}$ | 3.706 | 3.712 | 5.181 | 5.616 | 6.191 | 6.005 | 6.426 | 5.616 | 6.191 | 6.005 | 6.426 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.302 | 3.302 | 4.619 | 4.994 | 5.392 | 5.346 | 5.619 | 4.994 | 5.392 | 5.346 | 5.619 | ns |
| | | GCLK PLL | $t_{co}$ | 3.699 | 3.705 | 5.164 | 5.588 | 6.150 | 5.964 | 6.385 | 5.588 | 6.150 | 5.964 | 6.385 | ns |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.562 | 3.562 | 4.939 | 5.335 | 5.645 | 5.707 | 5.872 | 5.335 | 5.645 | 5.707 | 5.872 | ns |
| | | GCLK PLL | $t_{co}$ | 3.865 | 3.871 | 5.398 | 5.831 | 6.403 | 6.217 | 6.638 | 5.831 | 6.403 | 6.217 | 6.638 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.362 | 3.362 | 4.649 | 5.023 | 5.444 | 5.377 | 5.671 | 5.023 | 5.444 | 5.377 | 5.671 | ns |
| | | GCLK PLL | $t_{co}$ | 3.710 | 3.716 | 5.191 | 5.633 | 6.202 | 6.016 | 6.437 | 5.633 | 6.202 | 6.016 | 6.437 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.305 | 3.305 | 4.612 | 4.992 | 5.418 | 5.346 | 5.645 | 4.992 | 5.418 | 5.346 | 5.645 | ns |
| | | GCLK PLL | $t_{co}$ | 3.717 | 3.723 | 5.185 | 5.612 | 6.176 | 5.990 | 6.411 | 5.612 | 6.176 | 5.990 | 6.411 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.285 | 3.285 | 4.558 | 4.934 | 5.389 | 5.289 | 5.616 | 4.934 | 5.389 | 5.289 | 5.616 | ns |
| | | GCLK PLL | $t_{co}$ | 3.701 | 3.707 | 5.163 | 5.587 | 6.147 | 5.961 | 6.382 | 5.587 | 6.147 | 5.961 | 6.382 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.504 | 3.504 | 4.884 | 5.274 | 5.605 | 5.658 | 5.832 | 5.274 | 5.605 | 5.658 | 5.832 | ns |
| | | GCLK PLL | $t_{co}$ | 3.823 | 3.829 | 5.361 | 5.794 | 6.363 | 6.177 | 6.598 | 5.794 | 6.363 | 6.177 | 6.598 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.374 | 3.374 | 4.715 | 5.102 | 5.468 | 5.497 | 5.693 | 5.102 | 5.468 | 5.497 | 5.693 | ns |
| | | GCLK PLL | $t_{co}$ | 3.712 | 3.718 | 5.231 | 5.660 | 6.225 | 6.041 | 6.459 | 5.660 | 6.225 | 6.041 | 6.459 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.299 | 3.299 | 4.626 | 5.003 | 5.394 | 5.395 | 5.620 | 5.003 | 5.394 | 5.395 | 5.620 | ns |
| | | GCLK PLL | $t_{co}$ | 3.676 | 3.682 | 5.168 | 5.591 | 6.151 | 5.967 | 6.386 | 5.591 | 6.151 | 5.967 | 6.386 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.262 | 3.262 | 4.561 | 4.934 | 5.365 | 5.345 | 5.592 | 4.934 | 5.365 | 5.345 | 5.592 | ns |
| | | GCLK PLL | $t_{co}$ | 3.658 | 3.664 | 5.139 | 5.563 | 6.123 | 5.937 | 6.358 | 5.563 | 6.123 | 5.937 | 6.358 | ns |

**Table 1–113.** EP3SE80 Column Pins Output Timing Parameters (Part 2 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.412 | 3.412 | 4.773 | 5.155 | 5.503 | 5.551 | 5.728 | 5.155 | 5.503 | 5.551 | 5.728 | ns |
| | | GCLK PLL | $t_{co}$ | 3.737 | 3.743 | 5.265 | 5.694 | 6.260 | 6.076 | 6.494 | 5.694 | 6.260 | 6.076 | 6.494 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.275 | 3.275 | 4.578 | 4.956 | 5.368 | 5.369 | 5.593 | 4.956 | 5.368 | 5.369 | 5.593 | ns |
| | | GCLK PLL | $t_{co}$ | 3.658 | 3.664 | 5.141 | 5.565 | 6.125 | 5.941 | 6.359 | 5.565 | 6.125 | 5.941 | 6.359 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.245 | 3.245 | 4.532 | 4.904 | 5.359 | 5.300 | 5.586 | 4.904 | 5.359 | 5.300 | 5.586 | ns |
| | | GCLK PLL | $t_{co}$ | 3.653 | 3.659 | 5.134 | 5.558 | 6.117 | 5.931 | 6.352 | 5.558 | 6.117 | 5.931 | 6.352 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.223 | 3.224 | 4.510 | 4.883 | 5.344 | 5.299 | 5.571 | 4.883 | 5.344 | 5.299 | 5.571 | ns |
| | | GCLK PLL | $t_{co}$ | 3.644 | 3.650 | 5.120 | 5.543 | 6.102 | 5.916 | 6.337 | 5.543 | 6.102 | 5.916 | 6.337 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.559 | 3.559 | 5.027 | 5.434 | 5.750 | 5.833 | 5.976 | 5.434 | 5.750 | 5.833 | 5.976 | ns |
| | | GCLK PLL | $t_{co}$ | 3.859 | 3.865 | 5.472 | 5.921 | 6.507 | 6.323 | 6.742 | 5.921 | 6.507 | 6.323 | 6.742 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.434 | 3.434 | 4.854 | 5.250 | 5.618 | 5.636 | 5.843 | 5.250 | 5.618 | 5.636 | 5.843 | ns |
| | | GCLK PLL | $t_{co}$ | 3.759 | 3.765 | 5.353 | 5.795 | 6.375 | 6.191 | 6.609 | 5.795 | 6.375 | 6.191 | 6.609 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.334 | 3.334 | 4.725 | 5.114 | 5.522 | 5.496 | 5.749 | 5.114 | 5.522 | 5.496 | 5.749 | ns |
| | | GCLK PLL | $t_{co}$ | 3.715 | 3.721 | 5.266 | 5.704 | 6.280 | 6.094 | 6.515 | 5.704 | 6.280 | 6.094 | 6.515 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.307 | 3.307 | 4.656 | 5.047 | 5.479 | 5.446 | 5.706 | 5.047 | 5.479 | 5.446 | 5.706 | ns |
| | | GCLK PLL | $t_{co}$ | 3.677 | 3.683 | 5.227 | 5.662 | 6.237 | 6.051 | 6.472 | 5.662 | 6.237 | 6.051 | 6.472 | ns |

**Table 1–113.** EP3SE80 Column Pins Output Timing Parameters (Part 3 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.822 | 3.822 | 5.464 | 5.917 | 6.154 | 6.369 | 6.381 | 5.917 | 6.154 | 6.369 | 6.381 | ns |
| | | GCLK PLL | $t_{co}$ | 4.050 | 4.056 | 5.793 | 6.281 | 6.912 | 6.726 | 7.147 | 6.281 | 6.912 | 6.726 | 7.147 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.581 | 3.581 | 5.104 | 5.511 | 5.807 | 5.909 | 6.032 | 5.511 | 5.807 | 5.909 | 6.032 | ns |
| | | GCLK PLL | $t_{co}$ | 3.869 | 3.875 | 5.514 | 5.972 | 6.564 | 6.380 | 6.798 | 5.972 | 6.564 | 6.380 | 6.798 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.463 | 3.463 | 4.914 | 5.321 | 5.696 | 5.734 | 5.923 | 5.321 | 5.696 | 5.734 | 5.923 | ns |
| | | GCLK PLL | $t_{co}$ | 3.787 | 3.793 | 5.407 | 5.857 | 6.454 | 6.268 | 6.689 | 5.857 | 6.454 | 6.268 | 6.689 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.409 | 3.409 | 4.814 | 5.223 | 5.630 | 5.622 | 5.857 | 5.223 | 5.630 | 5.622 | 5.857 | ns |
| | | GCLK PLL | $t_{co}$ | 3.767 | 3.773 | 5.349 | 5.803 | 6.388 | 6.202 | 6.623 | 5.803 | 6.388 | 6.202 | 6.623 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.341 | 3.341 | 4.718 | 5.125 | 5.549 | 5.508 | 5.776 | 5.125 | 5.549 | 5.508 | 5.776 | ns |
| | | GCLK PLL | $t_{co}$ | 3.704 | 3.710 | 5.288 | 5.728 | 6.307 | 6.121 | 6.542 | 5.728 | 6.307 | 6.121 | 6.542 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.317 | 3.317 | 4.685 | 5.078 | 5.526 | 5.470 | 5.753 | 5.078 | 5.526 | 5.470 | 5.753 | ns |
| | | GCLK PLL | $t_{co}$ | 3.686 | 3.692 | 5.267 | 5.707 | 6.284 | 6.098 | 6.519 | 5.707 | 6.284 | 6.098 | 6.519 | ns |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.730 | 3.730 | 5.357 | 5.827 | 6.092 | 6.286 | 6.319 | 5.827 | 6.092 | 6.286 | 6.319 | ns |
| | | GCLK PLL | $t_{co}$ | 3.996 | 4.002 | 5.722 | 6.213 | 6.850 | 6.664 | 7.085 | 6.213 | 6.850 | 6.664 | 7.085 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.447 | 3.447 | 4.903 | 5.314 | 5.700 | 5.730 | 5.927 | 5.314 | 5.700 | 5.730 | 5.927 | ns |
| | | GCLK PLL | $t_{co}$ | 3.784 | 3.790 | 5.403 | 5.857 | 6.458 | 6.272 | 6.693 | 5.857 | 6.458 | 6.272 | 6.693 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.369 | 3.369 | 4.803 | 5.206 | 5.633 | 5.613 | 5.860 | 5.206 | 5.633 | 5.613 | 5.860 | ns |
| | | GCLK PLL | $t_{co}$ | 3.759 | 3.765 | 5.336 | 5.797 | 6.391 | 6.205 | 6.626 | 5.797 | 6.391 | 6.205 | 6.626 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.359 | 3.359 | 4.785 | 5.185 | 5.613 | 5.581 | 5.840 | 5.185 | 5.613 | 5.581 | 5.840 | ns |
| | | GCLK PLL | $t_{co}$ | 3.748 | 3.754 | 5.319 | 5.772 | 6.371 | 6.185 | 6.606 | 5.772 | 6.371 | 6.185 | 6.606 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.329 | 3.329 | 4.701 | 5.107 | 5.543 | 5.499 | 5.770 | 5.107 | 5.543 | 5.499 | 5.770 | ns |
| | | GCLK PLL | $t_{co}$ | 3.693 | 3.699 | 5.281 | 5.721 | 6.301 | 6.115 | 6.536 | 5.721 | 6.301 | 6.115 | 6.536 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.280 | 3.280 | 4.679 | 5.072 | 5.532 | 5.457 | 5.759 | 5.072 | 5.532 | 5.457 | 5.759 | ns |
| | | GCLK PLL | $t_{co}$ | 3.688 | 3.694 | 5.264 | 5.710 | 6.290 | 6.104 | 6.525 | 5.710 | 6.290 | 6.104 | 6.525 | ns |

**Table 1–113.** EP3SE80 Column Pins Output Timing Parameters (Part 4 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.620 | 3.620 | 5.244 | 5.726 | 6.036 | 6.206 | 6.263 | 5.726 | 6.036 | 6.206 | 6.263 | ns |
| | | GCLK PLL | $t_{co}$ | 3.912 | 3.918 | 5.648 | 6.149 | 6.794 | 6.608 | 7.029 | 6.149 | 6.794 | 6.608 | 7.029 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.447 | 3.447 | 4.922 | 5.345 | 5.750 | 5.777 | 5.977 | 5.345 | 5.750 | 5.777 | 5.977 | ns |
| | | GCLK PLL | $t_{co}$ | 3.789 | 3.795 | 5.422 | 5.887 | 6.508 | 6.322 | 6.743 | 5.887 | 6.508 | 6.322 | 6.743 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.360 | 3.360 | 4.795 | 5.204 | 5.637 | 5.622 | 5.864 | 5.204 | 5.637 | 5.622 | 5.864 | ns |
| | | GCLK PLL | $t_{co}$ | 3.751 | 3.757 | 5.330 | 5.798 | 6.395 | 6.209 | 6.630 | 5.798 | 6.395 | 6.209 | 6.630 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.336 | 3.336 | 4.726 | 5.144 | 5.581 | 5.531 | 5.808 | 5.144 | 5.581 | 5.531 | 5.808 | ns |
| | | GCLK PLL | $t_{co}$ | 3.704 | 3.710 | 5.302 | 5.749 | 6.339 | 6.153 | 6.574 | 5.749 | 6.339 | 6.153 | 6.574 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.324 | 3.324 | 4.688 | 5.075 | 5.512 | 5.479 | 5.739 | 5.075 | 5.512 | 5.479 | 5.739 | ns |
| | | GCLK PLL | $t_{co}$ | 3.704 | 3.710 | 5.259 | 5.696 | 6.270 | 6.084 | 6.505 | 5.696 | 6.270 | 6.084 | 6.505 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.321 | 3.321 | 4.681 | 5.068 | 5.508 | 5.485 | 5.735 | 5.068 | 5.508 | 5.485 | 5.735 | ns |
| | | GCLK PLL | $t_{co}$ | 3.701 | 3.707 | 5.256 | 5.693 | 6.266 | 6.080 | 6.501 | 5.693 | 6.266 | 6.080 | 6.501 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.309 | 3.309 | 4.677 | 5.064 | 5.509 | 5.465 | 5.736 | 5.064 | 5.509 | 5.465 | 5.736 | ns |
| | | GCLK PLL | $t_{co}$ | 3.699 | 3.705 | 5.256 | 5.694 | 6.267 | 6.081 | 6.502 | 5.694 | 6.267 | 6.081 | 6.502 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.286 | 3.286 | 4.647 | 5.033 | 5.494 | 5.431 | 5.721 | 5.033 | 5.494 | 5.431 | 5.721 | ns |
| | | GCLK PLL | $t_{co}$ | 3.690 | 3.696 | 5.241 | 5.678 | 6.252 | 6.066 | 6.487 | 5.678 | 6.252 | 6.066 | 6.487 | ns |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.340 | 3.340 | 4.700 | 5.090 | 5.528 | 5.507 | 5.755 | 5.090 | 5.528 | 5.507 | 5.755 | ns |
| | | GCLK PLL | $t_{co}$ | 3.711 | 3.717 | 5.271 | 5.710 | 6.286 | 6.100 | 6.521 | 5.710 | 6.286 | 6.100 | 6.521 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.323 | 3.323 | 4.697 | 5.087 | 5.526 | 5.496 | 5.753 | 5.087 | 5.526 | 5.496 | 5.753 | ns |
| | | GCLK PLL | $t_{co}$ | 3.707 | 3.713 | 5.269 | 5.708 | 6.284 | 6.098 | 6.519 | 5.708 | 6.284 | 6.098 | 6.519 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.311 | 3.311 | 4.677 | 5.067 | 5.517 | 5.489 | 5.744 | 5.067 | 5.517 | 5.489 | 5.744 | ns |
| | | GCLK PLL | $t_{co}$ | 3.696 | 3.702 | 5.259 | 5.699 | 6.275 | 6.089 | 6.510 | 5.699 | 6.275 | 6.089 | 6.510 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.282 | 3.282 | 4.659 | 5.049 | 5.504 | 5.450 | 5.731 | 5.049 | 5.504 | 5.450 | 5.731 | ns |
| | | GCLK PLL | $t_{co}$ | 3.685 | 3.691 | 5.246 | 5.686 | 6.262 | 6.076 | 6.497 | 5.686 | 6.262 | 6.076 | 6.497 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.281 | 3.281 | 4.659 | 5.049 | 5.504 | 5.450 | 5.731 | 5.049 | 5.504 | 5.450 | 5.731 | ns |
| | | GCLK PLL | $t_{co}$ | 3.685 | 3.691 | 5.246 | 5.686 | 6.262 | 6.076 | 6.497 | 5.686 | 6.262 | 6.076 | 6.497 | ns |

**Table 1–113.** EP3SE80 Column Pins Output Timing Parameters (Part 5 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.290 | 3.290 | 4.656 | 5.044 | 5.499 | 5.450 | 5.726 | 5.044 | 5.499 | 5.450 | 5.726 | ns |
| | | GCLK PLL | $t_{co}$ | 3.691 | 3.697 | 5.245 | 5.683 | 6.257 | 6.071 | 6.492 | 5.683 | 6.257 | 6.071 | 6.492 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.279 | 3.279 | 4.649 | 5.039 | 5.511 | 5.455 | 5.738 | 5.039 | 5.511 | 5.455 | 5.738 | ns |
| | | GCLK PLL | $t_{co}$ | 3.694 | 3.700 | 5.253 | 5.692 | 6.269 | 6.083 | 6.504 | 5.692 | 6.269 | 6.083 | 6.504 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.334 | 3.334 | 4.714 | 5.107 | 5.541 | 5.521 | 5.768 | 5.107 | 5.541 | 5.521 | 5.768 | ns |
| | | GCLK PLL | $t_{co}$ | 3.715 | 3.721 | 5.280 | 5.722 | 6.299 | 6.113 | 6.534 | 5.722 | 6.299 | 6.113 | 6.534 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.309 | 3.309 | 4.693 | 5.086 | 5.532 | 5.495 | 5.759 | 5.086 | 5.532 | 5.495 | 5.759 | ns |
| | | GCLK PLL | $t_{co}$ | 3.701 | 3.707 | 5.270 | 5.712 | 6.290 | 6.104 | 6.525 | 5.712 | 6.290 | 6.104 | 6.525 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.289 | 3.289 | 4.672 | 5.065 | 5.518 | 5.471 | 5.745 | 5.065 | 5.518 | 5.471 | 5.745 | ns |
| | | GCLK PLL | $t_{co}$ | 3.690 | 3.696 | 5.256 | 5.698 | 6.276 | 6.090 | 6.511 | 5.698 | 6.276 | 6.090 | 6.511 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.280 | 3.280 | 4.666 | 5.059 | 5.522 | 5.460 | 5.749 | 5.059 | 5.522 | 5.460 | 5.749 | ns |
| | | GCLK PLL | $t_{co}$ | 3.689 | 3.695 | 5.259 | 5.701 | 6.280 | 6.094 | 6.515 | 5.701 | 6.280 | 6.094 | 6.515 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.275 | 3.275 | 4.659 | 5.051 | 5.516 | 5.450 | 5.743 | 5.051 | 5.516 | 5.450 | 5.743 | ns |
| | | GCLK PLL | $t_{co}$ | 3.686 | 3.692 | 5.254 | 5.696 | 6.274 | 6.088 | 6.509 | 5.696 | 6.274 | 6.088 | 6.509 | ns |
| SSTL-15 CLASS II | 8mA | GCLK | $t_{co}$ | 3.284 | 3.284 | 4.652 | 5.042 | 5.499 | 5.450 | 5.726 | 5.042 | 5.499 | 5.450 | 5.726 | ns |
| | | GCLK PLL | $t_{co}$ | 3.688 | 3.694 | 5.243 | 5.682 | 6.257 | 6.071 | 6.492 | 5.682 | 6.257 | 6.071 | 6.492 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.274 | 3.274 | 4.646 | 5.036 | 5.510 | 5.456 | 5.737 | 5.036 | 5.510 | 5.456 | 5.737 | ns |
| | | GCLK PLL | $t_{co}$ | 3.691 | 3.697 | 5.250 | 5.691 | 6.268 | 6.082 | 6.503 | 5.691 | 6.268 | 6.082 | 6.503 | ns |


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**Table 1–113.** EP3SE80 Column Pins Output Timing Parameters (Part 6 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.308 | 3.308 | 4.665 | 5.052 | 5.497 | 5.464 | 5.724 | 5.052 | 5.497 | 5.464 | 5.724 | ns |
| | | GCLK PLL | $t_{co}$ | 3.698 | 3.704 | 5.245 | 5.682 | 6.255 | 6.069 | 6.490 | 5.682 | 6.255 | 6.069 | 6.490 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.294 | 3.294 | 4.652 | 5.040 | 5.496 | 5.461 | 5.723 | 5.040 | 5.496 | 5.461 | 5.723 | ns |
| | | GCLK PLL | $t_{co}$ | 3.691 | 3.697 | 5.243 | 5.680 | 6.254 | 6.068 | 6.489 | 5.680 | 6.254 | 6.068 | 6.489 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.278 | 3.278 | 4.642 | 5.029 | 5.489 | 5.434 | 5.716 | 5.029 | 5.489 | 5.434 | 5.716 | ns |
| | | GCLK PLL | $t_{co}$ | 3.683 | 3.689 | 5.235 | 5.673 | 6.247 | 6.061 | 6.482 | 5.673 | 6.247 | 6.061 | 6.482 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.279 | 3.279 | 4.644 | 5.032 | 5.493 | 5.436 | 5.720 | 5.032 | 5.493 | 5.436 | 5.720 | ns |
| | | GCLK PLL | $t_{co}$ | 3.686 | 3.692 | 5.238 | 5.676 | 6.251 | 6.065 | 6.486 | 5.676 | 6.251 | 6.065 | 6.486 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.271 | 3.271 | 4.640 | 5.028 | 5.497 | 5.436 | 5.724 | 5.028 | 5.497 | 5.436 | 5.724 | ns |
| | | GCLK PLL | $t_{co}$ | 3.683 | 3.689 | 5.241 | 5.680 | 6.255 | 6.069 | 6.490 | 5.680 | 6.255 | 6.069 | 6.490 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.274 | 3.274 | 4.631 | 5.018 | 5.493 | 5.432 | 5.720 | 5.018 | 5.493 | 5.432 | 5.720 | ns |
| | | GCLK PLL | $t_{co}$ | 3.691 | 3.697 | 5.240 | 5.677 | 6.251 | 6.065 | 6.486 | 5.677 | 6.251 | 6.065 | 6.486 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.314 | 3.314 | 4.676 | 5.065 | 5.508 | 5.480 | 5.735 | 5.065 | 5.508 | 5.480 | 5.735 | ns |
| | | GCLK PLL | $t_{co}$ | 3.703 | 3.709 | 5.253 | 5.692 | 6.266 | 6.080 | 6.501 | 5.692 | 6.266 | 6.080 | 6.501 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.302 | 3.302 | 4.670 | 5.060 | 5.511 | 5.469 | 5.738 | 5.060 | 5.511 | 5.469 | 5.738 | ns |
| | | GCLK PLL | $t_{co}$ | 3.699 | 3.705 | 5.254 | 5.693 | 6.269 | 6.083 | 6.504 | 5.693 | 6.269 | 6.083 | 6.504 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.296 | 3.296 | 4.664 | 5.053 | 5.506 | 5.463 | 5.733 | 5.053 | 5.506 | 5.463 | 5.733 | ns |
| | | GCLK PLL | $t_{co}$ | 3.695 | 3.701 | 5.250 | 5.689 | 6.264 | 6.078 | 6.499 | 5.689 | 6.264 | 6.078 | 6.499 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.284 | 3.284 | 4.652 | 5.042 | 5.499 | 5.450 | 5.726 | 5.042 | 5.499 | 5.450 | 5.726 | ns |
| | | GCLK PLL | $t_{co}$ | 3.688 | 3.694 | 5.243 | 5.682 | 6.257 | 6.071 | 6.492 | 5.682 | 6.257 | 6.071 | 6.492 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.279 | 3.279 | 4.653 | 5.043 | 5.509 | 5.446 | 5.736 | 5.043 | 5.509 | 5.446 | 5.736 | ns |
| | | GCLK PLL | $t_{co}$ | 3.689 | 3.695 | 5.250 | 5.690 | 6.267 | 6.081 | 6.502 | 5.690 | 6.267 | 6.081 | 6.502 | ns |
| 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.275 | 3.275 | 4.629 | 5.015 | 5.483 | 5.425 | 5.710 | 5.015 | 5.483 | 5.425 | 5.710 | ns |
| | | GCLK PLL | $t_{co}$ | 3.687 | 3.693 | 5.231 | 5.668 | 6.241 | 6.055 | 6.476 | 5.668 | 6.241 | 6.055 | 6.476 | ns |

**Table 1–113.** EP3SE80 Column Pins Output Timing Parameters (Part 7 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.312 | 3.312 | 4.688 | 5.081 | 5.529 | 5.499 | 5.756 | 5.081 | 5.529 | 5.499 | 5.756 | ns |
| | | GCLK PLL | $t_{co}$ | 3.706 | 3.712 | 5.267 | 5.709 | 6.287 | 6.101 | 6.522 | 5.709 | 6.287 | 6.101 | 6.522 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.298 | 3.298 | 4.674 | 5.066 | 5.520 | 5.482 | 5.747 | 5.066 | 5.520 | 5.482 | 5.747 | ns |
| | | GCLK PLL | $t_{co}$ | 3.698 | 3.704 | 5.258 | 5.700 | 6.278 | 6.092 | 6.513 | 5.700 | 6.278 | 6.092 | 6.513 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.292 | 3.292 | 4.675 | 5.068 | 5.529 | 5.478 | 5.756 | 5.068 | 5.529 | 5.478 | 5.756 | ns |
| | | GCLK PLL | $t_{co}$ | 3.699 | 3.705 | 5.266 | 5.708 | 6.287 | 6.101 | 6.522 | 5.708 | 6.287 | 6.101 | 6.522 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.277 | 3.277 | 4.657 | 5.049 | 5.515 | 5.455 | 5.742 | 5.049 | 5.515 | 5.455 | 5.742 | ns |
| | | GCLK PLL | $t_{co}$ | 3.688 | 3.694 | 5.253 | 5.695 | 6.273 | 6.087 | 6.508 | 5.695 | 6.273 | 6.087 | 6.508 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.277 | 3.277 | 4.657 | 5.049 | 5.516 | 5.456 | 5.743 | 5.049 | 5.516 | 5.456 | 5.743 | ns |
| | | GCLK PLL | $t_{co}$ | 3.688 | 3.694 | 5.253 | 5.695 | 6.274 | 6.088 | 6.509 | 5.695 | 6.274 | 6.088 | 6.509 | ns |
| 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.327 | 3.327 | 4.692 | 5.083 | 5.529 | 5.534 | 5.756 | 5.083 | 5.529 | 5.534 | 5.756 | ns |
| | | GCLK PLL | $t_{co}$ | 3.709 | 3.715 | 5.269 | 5.710 | 6.287 | 6.101 | 6.522 | 5.710 | 6.287 | 6.101 | 6.522 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.395 | 3.395 | 4.701 | 5.080 | 5.554 | 5.509 | 5.781 | 5.080 | 5.554 | 5.509 | 5.781 | ns |
| | | GCLK PLL | $t_{co}$ | 3.812 | 3.818 | 5.314 | 5.744 | 6.312 | 6.126 | 6.547 | 5.744 | 6.312 | 6.126 | 6.547 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.395 | 3.395 | 4.701 | 5.080 | 5.554 | 5.509 | 5.781 | 5.080 | 5.554 | 5.509 | 5.781 | ns |
| | | GCLK PLL | $t_{co}$ | 3.812 | 3.818 | 5.314 | 5.744 | 6.312 | 6.126 | 6.547 | 5.744 | 6.312 | 6.126 | 6.547 | ns |

Table 1–114 lists the EP3SE80 row pins output timing parameters for single-ended I/O standards.

**Table 1–114.** EP3SE80 Row Pins Output Timing Parameters (Part 1 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.238 | 3.493 | 4.856 | 5.245 | 5.757 | 5.609 | 5.907 | 5.368 | 5.891 | 5.735 | 5.990 | ns |
| | | GCLK PLL | $t_{co}$ | 1.439 | 1.634 | 2.039 | 2.121 | 2.343 | 2.334 | 2.309 | 2.226 | 2.430 | 2.441 | 2.301 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.156 | 3.399 | 4.726 | 5.107 | 5.612 | 5.464 | 5.762 | 5.227 | 5.742 | 5.586 | 5.841 | ns |
| | | GCLK PLL | $t_{co}$ | 1.346 | 1.529 | 1.909 | 1.983 | 2.198 | 2.189 | 2.195 | 2.085 | 2.281 | 2.292 | 2.186 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.077 | 3.310 | 4.607 | 4.984 | 5.484 | 5.348 | 5.634 | 5.107 | 5.610 | 5.468 | 5.709 | ns |
| | | GCLK PLL | $t_{co}$ | 1.247 | 1.423 | 1.790 | 1.860 | 2.070 | 2.061 | 2.099 | 1.958 | 2.149 | 2.160 | 2.086 | ns |

**Table 1–114.** EP3SE80 Row Pins Output Timing Parameters (Part 2 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.248 | 3.497 | 4.864 | 5.250 | 5.761 | 5.613 | 5.911 | 5.374 | 5.895 | 5.739 | 5.994 | ns |
| | | GCLK PLL | $t_{co}$ | 1.449 | 1.638 | 2.047 | 2.126 | 2.347 | 2.338 | 2.318 | 2.232 | 2.434 | 2.445 | 2.313 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.081 | 3.314 | 4.613 | 4.999 | 5.490 | 5.358 | 5.640 | 5.119 | 5.617 | 5.477 | 5.716 | ns |
| | | GCLK PLL | $t_{co}$ | 1.251 | 1.429 | 1.796 | 1.866 | 2.076 | 2.067 | 2.109 | 1.964 | 2.156 | 2.167 | 2.095 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.192 | 3.439 | 4.808 | 5.198 | 5.713 | 5.565 | 5.863 | 5.325 | 5.849 | 5.693 | 5.948 | ns |
| | | GCLK PLL | $t_{co}$ | 1.393 | 1.580 | 1.991 | 2.074 | 2.299 | 2.290 | 2.275 | 2.183 | 2.388 | 2.399 | 2.267 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.082 | 3.319 | 4.655 | 5.039 | 5.549 | 5.401 | 5.699 | 5.163 | 5.685 | 5.528 | 5.783 | ns |
| | | GCLK PLL | $t_{co}$ | 1.268 | 1.453 | 1.838 | 1.915 | 2.135 | 2.126 | 2.130 | 2.021 | 2.224 | 2.234 | 2.121 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.045 | 3.281 | 4.582 | 4.957 | 5.461 | 5.313 | 5.611 | 5.077 | 5.592 | 5.435 | 5.690 | ns |
| | | GCLK PLL | $t_{co}$ | 1.229 | 1.402 | 1.756 | 1.832 | 2.047 | 2.038 | 2.060 | 1.935 | 2.131 | 2.141 | 2.048 | ns |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.106 | 3.358 | 4.702 | 5.091 | 5.603 | 5.455 | 5.753 | 5.217 | 5.738 | 5.581 | 5.836 | ns |
| | | GCLK PLL | $t_{co}$ | 1.307 | 1.499 | 1.885 | 1.967 | 2.189 | 2.180 | 2.166 | 2.075 | 2.277 | 2.287 | 2.157 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.032 | 3.265 | 4.554 | 4.928 | 5.422 | 5.281 | 5.572 | 5.047 | 5.552 | 5.401 | 5.650 | ns |
| | | GCLK PLL | $t_{co}$ | 1.207 | 1.380 | 1.721 | 1.793 | 2.008 | 1.999 | 2.032 | 1.895 | 2.091 | 2.101 | 2.019 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.218 | 3.475 | 4.940 | 5.352 | 5.885 | 5.737 | 6.035 | 5.485 | 6.028 | 5.871 | 6.126 | ns |
| | | GCLK PLL | $t_{co}$ | 1.419 | 1.616 | 2.123 | 2.228 | 2.471 | 2.462 | 2.420 | 2.343 | 2.567 | 2.577 | 2.419 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.124 | 3.377 | 4.785 | 5.189 | 5.715 | 5.567 | 5.865 | 5.318 | 5.854 | 5.697 | 5.952 | ns |
| | | GCLK PLL | $t_{co}$ | 1.309 | 1.518 | 1.968 | 2.065 | 2.301 | 2.292 | 2.278 | 2.176 | 2.393 | 2.403 | 2.274 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.067 | 3.321 | 4.679 | 5.070 | 5.589 | 5.441 | 5.739 | 5.195 | 5.724 | 5.567 | 5.822 | ns |
| | | GCLK PLL | $t_{co}$ | 1.263 | 1.441 | 1.857 | 1.946 | 2.175 | 2.166 | 2.187 | 2.053 | 2.263 | 2.273 | 2.180 | ns |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.451 | 3.722 | 5.326 | 5.781 | 6.360 | 6.212 | 6.510 | 5.922 | 6.504 | 6.356 | 6.611 | ns |
| | | GCLK PLL | $t_{co}$ | 1.652 | 1.862 | 2.507 | 2.657 | 2.761 | 2.937 | 2.944 | 2.780 | 2.883 | 3.062 | 2.957 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.229 | 3.520 | 4.999 | 5.412 | 5.955 | 5.807 | 6.105 | 5.557 | 6.098 | 5.949 | 6.204 | ns |
| | | GCLK PLL | $t_{co}$ | 1.427 | 1.660 | 2.180 | 2.288 | 2.401 | 2.532 | 2.539 | 2.415 | 2.522 | 2.655 | 2.550 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.161 | 3.418 | 4.846 | 5.262 | 5.796 | 5.648 | 5.946 | 5.389 | 5.925 | 5.777 | 6.032 | ns |
| | | GCLK PLL | $t_{co}$ | 1.362 | 1.558 | 2.027 | 2.138 | 2.301 | 2.373 | 2.380 | 2.247 | 2.416 | 2.483 | 2.378 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.136 | 3.379 | 4.770 | 5.176 | 5.699 | 5.552 | 5.849 | 5.300 | 5.831 | 5.683 | 5.938 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.497 | 1.950 | 2.044 | 2.235 | 2.276 | 2.297 | 2.152 | 2.344 | 2.389 | 2.290 | ns |

**Table 1–114.** EP3SE80 Row Pins Output Timing Parameters (Part 3 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.362 | 3.640 | 5.236 | 5.694 | 6.288 | 6.140 | 6.438 | 5.829 | 6.428 | 6.280 | 6.535 | ns |
| | | GCLK PLL | $t_{co}$ | 1.563 | 1.780 | 2.417 | 2.570 | 2.698 | 2.865 | 2.872 | 2.687 | 2.818 | 2.986 | 2.881 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.152 | 3.396 | 4.831 | 5.257 | 5.797 | 5.649 | 5.947 | 5.383 | 5.924 | 5.776 | 6.031 | ns |
| | | GCLK PLL | $t_{co}$ | 1.331 | 1.522 | 2.012 | 2.133 | 2.304 | 2.374 | 2.381 | 2.241 | 2.417 | 2.482 | 2.377 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.125 | 3.370 | 4.758 | 5.168 | 5.691 | 5.552 | 5.841 | 5.293 | 5.819 | 5.677 | 5.926 | ns |
| | | GCLK PLL | $t_{co}$ | 1.304 | 1.488 | 1.939 | 2.037 | 2.235 | 2.268 | 2.297 | 2.143 | 2.344 | 2.377 | 2.290 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.106 | 3.359 | 4.738 | 5.143 | 5.672 | 5.533 | 5.822 | 5.269 | 5.797 | 5.658 | 5.904 | ns |
| | | GCLK PLL | $t_{co}$ | 1.285 | 1.477 | 1.917 | 2.019 | 2.216 | 2.249 | 2.278 | 2.125 | 2.325 | 2.355 | 2.271 | ns |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.305 | 3.565 | 5.146 | 5.608 | 6.213 | 6.065 | 6.363 | 5.741 | 6.344 | 6.196 | 6.451 | ns |
| | | GCLK PLL | $t_{co}$ | 1.506 | 1.705 | 2.327 | 2.484 | 2.637 | 2.790 | 2.797 | 2.599 | 2.749 | 2.902 | 2.797 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.157 | 3.400 | 4.853 | 5.285 | 5.838 | 5.690 | 5.988 | 5.408 | 5.966 | 5.818 | 6.073 | ns |
| | | GCLK PLL | $t_{co}$ | 1.336 | 1.518 | 2.034 | 2.161 | 2.352 | 2.415 | 2.422 | 2.266 | 2.461 | 2.524 | 2.419 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.071 | 3.309 | 4.672 | 5.060 | 5.557 | 5.426 | 5.707 | 5.180 | 5.686 | 5.548 | 5.785 | ns |
| | | GCLK PLL | $t_{co}$ | 1.248 | 1.427 | 1.835 | 1.918 | 2.143 | 2.134 | 2.177 | 2.020 | 2.225 | 2.236 | 2.166 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.066 | 3.305 | 4.669 | 5.058 | 5.549 | 5.424 | 5.699 | 5.179 | 5.679 | 5.547 | 5.778 | ns |
| | | GCLK PLL | $t_{co}$ | 1.236 | 1.415 | 1.827 | 1.910 | 2.135 | 2.126 | 2.175 | 2.012 | 2.218 | 2.229 | 2.165 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.057 | 3.294 | 4.654 | 5.042 | 5.522 | 5.407 | 5.672 | 5.162 | 5.652 | 5.529 | 5.751 | ns |
| | | GCLK PLL | $t_{co}$ | 1.220 | 1.397 | 1.802 | 1.885 | 2.108 | 2.099 | 2.158 | 1.986 | 2.191 | 2.202 | 2.147 | ns |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.085 | 3.323 | 4.689 | 5.080 | 5.578 | 5.447 | 5.724 | 5.199 | 5.698 | 5.568 | 5.802 | ns |
| | | GCLK PLL | $t_{co}$ | 1.264 | 1.441 | 1.849 | 1.934 | 2.130 | 2.151 | 2.192 | 2.035 | 2.235 | 2.254 | 2.181 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.080 | 3.318 | 4.687 | 5.079 | 5.577 | 5.446 | 5.723 | 5.197 | 5.696 | 5.566 | 5.800 | ns |
| | | GCLK PLL | $t_{co}$ | 1.259 | 1.436 | 1.847 | 1.933 | 2.129 | 2.150 | 2.191 | 2.033 | 2.233 | 2.252 | 2.179 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.069 | 3.307 | 4.677 | 5.069 | 5.567 | 5.436 | 5.713 | 5.188 | 5.687 | 5.557 | 5.791 | ns |
| | | GCLK PLL | $t_{co}$ | 1.248 | 1.425 | 1.837 | 1.923 | 2.119 | 2.140 | 2.181 | 2.024 | 2.224 | 2.243 | 2.170 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.058 | 3.296 | 4.664 | 5.056 | 5.554 | 5.423 | 5.700 | 5.176 | 5.675 | 5.545 | 5.779 | ns |
| | | GCLK PLL | $t_{co}$ | 1.237 | 1.414 | 1.824 | 1.910 | 2.106 | 2.127 | 2.168 | 2.012 | 2.212 | 2.231 | 2.158 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.058 | 3.295 | 4.664 | 5.056 | 5.554 | 5.423 | 5.700 | 5.175 | 5.675 | 5.545 | 5.779 | ns |
| | | GCLK PLL | $t_{co}$ | 1.237 | 1.413 | 1.824 | 1.910 | 2.106 | 2.127 | 2.168 | 2.011 | 2.212 | 2.231 | 2.158 | ns |


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**Table 1–114.** EP3SE80 Row Pins Output Timing Parameters (Part 4 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.066 | 3.302 | 4.663 | 5.053 | 5.549 | 5.418 | 5.695 | 5.171 | 5.669 | 5.539 | 5.773 | ns |
| | | GCLK PLL | $t_{co}$ | 1.245 | 1.420 | 1.823 | 1.907 | 2.101 | 2.122 | 2.163 | 2.007 | 2.206 | 2.225 | 2.152 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.067 | 3.305 | 4.669 | 5.061 | 5.559 | 5.428 | 5.705 | 5.180 | 5.680 | 5.550 | 5.784 | ns |
| | | GCLK PLL | $t_{co}$ | 1.246 | 1.423 | 1.829 | 1.915 | 2.111 | 2.132 | 2.173 | 2.016 | 2.217 | 2.236 | 2.163 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.088 | 3.326 | 4.698 | 5.091 | 5.591 | 5.460 | 5.740 | 5.209 | 5.710 | 5.580 | 5.817 | ns |
| | | GCLK PLL | $t_{co}$ | 1.267 | 1.444 | 1.858 | 1.946 | 2.143 | 2.167 | 2.205 | 2.046 | 2.247 | 2.268 | 2.193 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.074 | 3.312 | 4.687 | 5.081 | 5.581 | 5.450 | 5.727 | 5.200 | 5.701 | 5.571 | 5.805 | ns |
| | | GCLK PLL | $t_{co}$ | 1.253 | 1.430 | 1.847 | 1.935 | 2.133 | 2.154 | 2.195 | 2.036 | 2.238 | 2.257 | 2.184 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.063 | 3.300 | 4.674 | 5.068 | 5.568 | 5.437 | 5.714 | 5.187 | 5.688 | 5.558 | 5.792 | ns |
| | | GCLK PLL | $t_{co}$ | 1.242 | 1.418 | 1.834 | 1.922 | 2.120 | 2.141 | 2.182 | 2.023 | 2.225 | 2.244 | 2.171 | ns |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.073 | 3.308 | 4.662 | 5.051 | 5.547 | 5.416 | 5.693 | 5.170 | 5.666 | 5.536 | 5.770 | ns |
| | | GCLK PLL | $t_{co}$ | 1.252 | 1.426 | 1.822 | 1.905 | 2.099 | 2.120 | 2.161 | 2.006 | 2.203 | 2.222 | 2.149 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.066 | 3.302 | 4.660 | 5.050 | 5.546 | 5.415 | 5.692 | 5.169 | 5.666 | 5.536 | 5.770 | ns |
| | | GCLK PLL | $t_{co}$ | 1.245 | 1.420 | 1.820 | 1.904 | 2.098 | 2.119 | 2.160 | 2.005 | 2.203 | 2.222 | 2.149 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.057 | 3.294 | 4.653 | 5.043 | 5.539 | 5.408 | 5.685 | 5.162 | 5.659 | 5.529 | 5.763 | ns |
| | | GCLK PLL | $t_{co}$ | 1.236 | 1.412 | 1.813 | 1.897 | 2.091 | 2.112 | 2.153 | 1.998 | 2.196 | 2.215 | 2.142 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.060 | 3.296 | 4.656 | 5.046 | 5.543 | 5.412 | 5.689 | 5.165 | 5.662 | 5.532 | 5.766 | ns |
| | | GCLK PLL | $t_{co}$ | 1.239 | 1.414 | 1.816 | 1.900 | 2.095 | 2.116 | 2.157 | 2.001 | 2.199 | 2.218 | 2.145 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.056 | 3.293 | 4.658 | 5.049 | 5.546 | 5.415 | 5.692 | 5.168 | 5.667 | 5.537 | 5.771 | ns |
| | | GCLK PLL | $t_{co}$ | 1.235 | 1.411 | 1.818 | 1.903 | 2.098 | 2.119 | 2.160 | 2.004 | 2.204 | 2.223 | 2.150 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.064 | 3.301 | 4.656 | 5.046 | 5.542 | 5.411 | 5.688 | 5.164 | 5.661 | 5.531 | 5.765 | ns |
| | | GCLK PLL | $t_{co}$ | 1.243 | 1.419 | 1.816 | 1.900 | 2.094 | 2.115 | 2.156 | 2.000 | 2.198 | 2.217 | 2.144 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.079 | 3.314 | 4.671 | 5.061 | 5.558 | 5.427 | 5.704 | 5.179 | 5.677 | 5.547 | 5.781 | ns |
| | | GCLK PLL | $t_{co}$ | 1.258 | 1.432 | 1.831 | 1.915 | 2.110 | 2.131 | 2.172 | 2.015 | 2.214 | 2.233 | 2.160 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.073 | 3.309 | 4.672 | 5.063 | 5.560 | 5.429 | 5.706 | 5.181 | 5.680 | 5.550 | 5.784 | ns |
| | | GCLK PLL | $t_{co}$ | 1.252 | 1.427 | 1.832 | 1.917 | 2.112 | 2.133 | 2.174 | 2.017 | 2.217 | 2.236 | 2.163 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.069 | 3.305 | 4.667 | 5.058 | 5.555 | 5.424 | 5.701 | 5.176 | 5.674 | 5.544 | 5.778 | ns |
| | | GCLK PLL | $t_{co}$ | 1.248 | 1.423 | 1.827 | 1.912 | 2.107 | 2.128 | 2.169 | 2.012 | 2.211 | 2.230 | 2.157 | ns |

**Table 1–114.** EP3SE80 Row Pins Output Timing Parameters (Part 5 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.081 | 3.316 | 4.684 | 5.077 | 5.577 | 5.446 | 5.723 | 5.195 | 5.696 | 5.566 | 5.800 | ns |
| | | GCLK PLL | $t_{co}$ | 1.260 | 1.434 | 1.844 | 1.931 | 2.129 | 2.150 | 2.191 | 2.031 | 2.233 | 2.252 | 2.179 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.072 | 3.308 | 4.675 | 5.068 | 5.568 | 5.437 | 5.714 | 5.186 | 5.687 | 5.557 | 5.791 | ns |
| | | GCLK PLL | $t_{co}$ | 1.251 | 1.426 | 1.835 | 1.922 | 2.120 | 2.141 | 2.182 | 2.022 | 2.224 | 2.243 | 2.170 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.071 | 3.308 | 4.682 | 5.076 | 5.577 | 5.446 | 5.723 | 5.195 | 5.697 | 5.567 | 5.801 | ns |
| | | GCLK PLL | $t_{co}$ | 1.250 | 1.426 | 1.842 | 1.930 | 2.129 | 2.150 | 2.191 | 2.031 | 2.234 | 2.253 | 2.180 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.177 | 3.415 | 4.724 | 5.106 | 5.581 | 5.466 | 5.731 | 5.228 | 5.698 | 5.590 | 5.810 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.510 | 1.860 | 1.936 | 2.152 | 2.143 | 2.217 | 2.038 | 2.252 | 2.248 | 2.208 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.177 | 3.415 | 4.724 | 5.106 | 5.581 | 5.466 | 5.731 | 5.228 | 5.698 | 5.590 | 5.810 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.510 | 1.860 | 1.936 | 2.152 | 2.143 | 2.217 | 2.038 | 2.252 | 2.248 | 2.208 | ns |

Table 1–115 through Table 1–118 list the maximum I/O timing parameters for EP3SE80 devices for differential I/O standards.

Table 1–115 lists the EP3SE80 column pins input timing parameters for differential I/O standards.

**Table 1–115.** EP3SE80 Column Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -0.997 | -1.029 | -1.181 | -1.169 | -1.324 | -1.269 | -1.645 | -1.133 | -1.542 | -1.230 | -1.683 | ns |
| | | $t_h$ | 1.133 | 1.184 | 1.415 | 1.436 | 1.618 | 1.551 | 1.927 | 1.411 | 1.858 | 1.524 | 1.966 | ns |
| | GCLK PLL | $t_{su}$ | 0.960 | 0.994 | 1.879 | 2.224 | 2.401 | 2.288 | 2.194 | 2.277 | 2.567 | 2.345 | 2.245 | ns |
| | | $t_h$ | -0.691 | -0.701 | -1.428 | -1.714 | -1.834 | -1.749 | -1.648 | -1.756 | -1.968 | -1.795 | -1.697 | ns |
| MINI-LVDS | | $t_{su}$ | -0.997 | -1.029 | -1.181 | -1.169 | -1.324 | -1.269 | -1.645 | -1.133 | -1.542 | -1.230 | -1.683 | ns |
| | GCLK | $t_h$ | 1.133 | 1.184 | 1.415 | 1.436 | 1.618 | 1.551 | 1.927 | 1.411 | 1.858 | 1.524 | 1.966 | ns |
| | | $t_{su}$ | 0.960 | 0.994 | 1.879 | 2.224 | 2.401 | 2.288 | 2.194 | 2.277 | 2.567 | 2.345 | 2.245 | ns |
| | GCLK PLL | $t_h$ | -0.691 | -0.701 | -1.428 | -1.714 | -1.834 | -1.749 | -1.648 | -1.756 | -1.968 | -1.795 | -1.697 | ns |
| RSDS | | $t_{su}$ | -0.997 | -1.029 | -1.181 | -1.169 | -1.324 | -1.269 | -1.645 | -1.133 | -1.542 | -1.230 | -1.683 | ns |
| | | $t_h$ | 1.133 | 1.184 | 1.415 | 1.436 | 1.618 | 1.551 | 1.927 | 1.411 | 1.858 | 1.524 | 1.966 | ns |
| | GCLK | $t_{su}$ | 0.960 | 0.994 | 1.879 | 2.224 | 2.401 | 2.288 | 2.194 | 2.277 | 2.567 | 2.345 | 2.245 | ns |
| | | $t_h$ | -0.691 | -0.701 | -1.428 | -1.714 | -1.834 | -1.749 | -1.648 | -1.756 | -1.968 | -1.795 | -1.697 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.813 | -0.852 | -1.258 | -1.368 | -1.483 | -1.423 | -1.794 | -1.368 | -1.482 | -1.428 | -1.837 | ns |
| | | $t_h$ | 0.942 | 0.999 | 1.460 | 1.595 | 1.731 | 1.659 | 2.031 | 1.604 | 1.739 | 1.674 | 2.075 | ns |
| | GCLK PLL | $t_{su}$ | 1.144 | 1.171 | 1.802 | 2.025 | 2.242 | 2.134 | 2.045 | 2.042 | 2.260 | 2.147 | 2.091 | ns |
| | | $t_h$ | -0.882 | -0.886 | -1.383 | -1.555 | -1.721 | -1.641 | -1.544 | -1.563 | -1.729 | -1.645 | -1.588 | ns |

**Table 1–115.** EP3SE80 Column Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.813 | -0.852 | -1.258 | -1.368 | -1.483 | -1.423 | -1.794 | -1.368 | -1.482 | -1.428 | -1.837 | ns |
| | | $t_h$ | 0.942 | 0.999 | 1.460 | 1.595 | 1.731 | 1.659 | 2.031 | 1.604 | 1.739 | 1.674 | 2.075 | ns |
| | GCLK PLL | $t_{su}$ | 1.144 | 1.171 | 1.802 | 2.025 | 2.242 | 2.134 | 2.045 | 2.042 | 2.260 | 2.147 | 2.091 | ns |
| | | $t_h$ | -0.882 | -0.886 | -1.383 | -1.555 | -1.721 | -1.641 | -1.544 | -1.563 | -1.729 | -1.645 | -1.588 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.821 | -0.864 | -1.268 | -1.379 | -1.499 | -1.439 | -1.810 | -1.379 | -1.497 | -1.443 | -1.852 | ns |
| | | $t_h$ | 0.950 | 1.011 | 1.470 | 1.606 | 1.747 | 1.675 | 2.047 | 1.615 | 1.754 | 1.689 | 2.090 | ns |
| | GCLK PLL | $t_{su}$ | 1.136 | 1.159 | 1.792 | 2.014 | 2.226 | 2.118 | 2.029 | 2.031 | 2.245 | 2.132 | 2.076 | ns |
| | | $t_h$ | -0.874 | -0.874 | -1.373 | -1.544 | -1.705 | -1.625 | -1.528 | -1.552 | -1.714 | -1.630 | -1.573 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.821 | -0.864 | -1.268 | -1.379 | -1.499 | -1.439 | -1.810 | -1.379 | -1.497 | -1.443 | -1.852 | ns |
| | | $t_h$ | 0.950 | 1.011 | 1.470 | 1.606 | 1.747 | 1.675 | 2.047 | 1.615 | 1.754 | 1.689 | 2.090 | ns |
| | GCLK PLL | $t_{su}$ | 1.136 | 1.159 | 1.792 | 2.014 | 2.226 | 2.118 | 2.029 | 2.031 | 2.245 | 2.132 | 2.076 | ns |
| | | $t_h$ | -0.874 | -0.874 | -1.373 | -1.544 | -1.705 | -1.625 | -1.528 | -1.552 | -1.714 | -1.630 | -1.573 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.833 | -0.875 | -1.277 | -1.390 | -1.518 | -1.458 | -1.829 | -1.390 | -1.515 | -1.461 | -1.870 | ns |
| | | $t_h$ | 0.962 | 1.022 | 1.480 | 1.617 | 1.766 | 1.694 | 2.066 | 1.626 | 1.772 | 1.707 | 2.108 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.148 | 1.783 | 2.003 | 2.207 | 2.099 | 2.010 | 2.020 | 2.227 | 2.114 | 2.058 | ns |
| | | $t_h$ | -0.862 | -0.863 | -1.363 | -1.533 | -1.686 | -1.606 | -1.509 | -1.541 | -1.696 | -1.612 | -1.555 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.833 | -0.875 | -1.277 | -1.390 | -1.518 | -1.458 | -1.829 | -1.390 | -1.515 | -1.461 | -1.870 | ns |
| | | $t_h$ | 0.962 | 1.022 | 1.480 | 1.617 | 1.766 | 1.694 | 2.066 | 1.626 | 1.772 | 1.707 | 2.108 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.148 | 1.783 | 2.003 | 2.207 | 2.099 | 2.010 | 2.020 | 2.227 | 2.114 | 2.058 | ns |
| | | $t_h$ | -0.862 | -0.863 | -1.363 | -1.533 | -1.686 | -1.606 | -1.509 | -1.541 | -1.696 | -1.612 | -1.555 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.821 | -0.864 | -1.268 | -1.379 | -1.499 | -1.439 | -1.810 | -1.379 | -1.497 | -1.443 | -1.852 | ns |
| | | $t_h$ | 0.950 | 1.011 | 1.470 | 1.606 | 1.747 | 1.675 | 2.047 | 1.615 | 1.754 | 1.689 | 2.090 | ns |
| | GCLK PLL | $t_{su}$ | 1.136 | 1.159 | 1.792 | 2.014 | 2.226 | 2.118 | 2.029 | 2.031 | 2.245 | 2.132 | 2.076 | ns |
| | | $t_h$ | -0.874 | -0.874 | -1.373 | -1.544 | -1.705 | -1.625 | -1.528 | -1.552 | -1.714 | -1.630 | -1.573 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.821 | -0.864 | -1.268 | -1.379 | -1.499 | -1.439 | -1.810 | -1.379 | -1.497 | -1.443 | -1.852 | ns |
| | | $t_h$ | 0.950 | 1.011 | 1.470 | 1.606 | 1.747 | 1.675 | 2.047 | 1.615 | 1.754 | 1.689 | 2.090 | ns |
| | GCLK PLL | $t_{su}$ | 1.136 | 1.159 | 1.792 | 2.014 | 2.226 | 2.118 | 2.029 | 2.031 | 2.245 | 2.132 | 2.076 | ns |
| | | $t_h$ | -0.874 | -0.874 | -1.373 | -1.544 | -1.705 | -1.625 | -1.528 | -1.552 | -1.714 | -1.630 | -1.573 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -0.833 | -0.875 | -1.277 | -1.390 | -1.518 | -1.458 | -1.829 | -1.390 | -1.515 | -1.461 | -1.870 | ns |
| | | $t_h$ | 0.962 | 1.022 | 1.480 | 1.617 | 1.766 | 1.694 | 2.066 | 1.626 | 1.772 | 1.707 | 2.108 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.148 | 1.783 | 2.003 | 2.207 | 2.099 | 2.010 | 2.020 | 2.227 | 2.114 | 2.058 | ns |
| | | $t_h$ | -0.862 | -0.863 | -1.363 | -1.533 | -1.686 | -1.606 | -1.509 | -1.541 | -1.696 | -1.612 | -1.555 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -0.833 | -0.875 | -1.277 | -1.390 | -1.518 | -1.458 | -1.829 | -1.390 | -1.515 | -1.461 | -1.870 | ns |
| | | $t_h$ | 0.962 | 1.022 | 1.480 | 1.617 | 1.766 | 1.694 | 2.066 | 1.626 | 1.772 | 1.707 | 2.108 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.148 | 1.783 | 2.003 | 2.207 | 2.099 | 2.010 | 2.020 | 2.227 | 2.114 | 2.058 | ns |
| | | $t_h$ | -0.862 | -0.863 | -1.363 | -1.533 | -1.686 | -1.606 | -1.509 | -1.541 | -1.696 | -1.612 | -1.555 | ns |

**Table 1–115.** EP3SE80 Column Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.840 | -0.881 | -1.289 | -1.395 | -1.518 | -1.460 | -1.828 | -1.394 | -1.510 | -1.459 | -1.866 | ns |
| | | $t_h$ | 0.969 | 1.028 | 1.493 | 1.625 | 1.769 | 1.697 | 2.070 | 1.633 | 1.772 | 1.706 | 2.109 | ns |
| | GCLK PLL | $t_{su}$ | 1.117 | 1.142 | 1.771 | 1.998 | 2.207 | 2.097 | 2.011 | 2.016 | 2.232 | 2.116 | 2.062 | ns |
| | | $t_h$ | -0.855 | -0.857 | -1.350 | -1.525 | -1.683 | -1.603 | -1.505 | -1.534 | -1.696 | -1.613 | -1.554 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.840 | -0.881 | -1.289 | -1.395 | -1.518 | -1.460 | -1.828 | -1.394 | -1.510 | -1.459 | -1.866 | ns |
| | | $t_h$ | 0.969 | 1.028 | 1.493 | 1.625 | 1.769 | 1.697 | 2.070 | 1.633 | 1.772 | 1.706 | 2.109 | ns |
| | GCLK PLL | $t_{su}$ | 1.117 | 1.142 | 1.771 | 1.998 | 2.207 | 2.097 | 2.011 | 2.016 | 2.232 | 2.116 | 2.062 | ns |
| | | $t_h$ | -0.855 | -0.857 | -1.350 | -1.525 | -1.683 | -1.603 | -1.505 | -1.534 | -1.696 | -1.613 | -1.554 | ns |

Table 1–116 lists the EP3SE80 row pins input timing parameters for differential I/O standards.

**Table 1–116.** EP3SE80 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -0.944 | -0.979 | -1.054 | -1.015 | -1.154 | -1.107 | -1.454 | -0.975 | -1.107 | -1.061 | -1.493 | ns |
| | | $t_h$ | 1.077 | 1.130 | 1.288 | 1.285 | 1.447 | 1.389 | 1.737 | 1.257 | 1.412 | 1.355 | 1.777 | ns |
| | GCLK PLL | $t_{su}$ | 0.961 | 0.989 | 1.951 | 2.328 | 2.533 | 2.408 | 2.342 | 2.387 | 2.599 | 2.472 | 2.394 | ns |
| | | $t_h$ | -0.691 | -0.700 | -1.502 | -1.818 | -1.968 | -1.871 | -1.796 | -1.862 | -2.019 | -1.921 | -1.844 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -0.944 | -0.979 | -1.054 | -1.015 | -1.154 | -1.107 | -1.454 | -0.975 | -1.107 | -1.061 | -1.493 | ns |
| | | $t_h$ | 1.077 | 1.130 | 1.288 | 1.285 | 1.447 | 1.389 | 1.737 | 1.257 | 1.412 | 1.355 | 1.777 | ns |
| | GCLK PLL | $t_{su}$ | 0.961 | 0.989 | 1.951 | 2.328 | 2.533 | 2.408 | 2.342 | 2.387 | 2.599 | 2.472 | 2.394 | ns |
| | | $t_h$ | -0.691 | -0.700 | -1.502 | -1.818 | -1.968 | -1.871 | -1.796 | -1.862 | -2.019 | -1.921 | -1.844 | ns |
| RSDS | GCLK | $t_{su}$ | -0.944 | -0.979 | -1.054 | -1.015 | -1.154 | -1.107 | -1.454 | -0.975 | -1.107 | -1.061 | -1.493 | ns |
| | | $t_h$ | 1.077 | 1.130 | 1.288 | 1.285 | 1.447 | 1.389 | 1.737 | 1.257 | 1.412 | 1.355 | 1.777 | ns |
| | GCLK PLL | $t_{su}$ | 0.961 | 0.989 | 1.951 | 2.328 | 2.533 | 2.408 | 2.342 | 2.387 | 2.599 | 2.472 | 2.394 | ns |
| | | $t_h$ | -0.691 | -0.700 | -1.502 | -1.818 | -1.968 | -1.871 | -1.796 | -1.862 | -2.019 | -1.921 | -1.844 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.749 | -0.794 | -1.145 | -1.244 | -1.343 | -1.291 | -1.633 | -1.246 | -1.344 | -1.293 | -1.677 | ns |
| | | $t_h$ | 0.875 | 0.936 | 1.345 | 1.468 | 1.587 | 1.524 | 1.867 | 1.479 | 1.597 | 1.535 | 1.912 | ns |
| | GCLK PLL | $t_{su}$ | 1.156 | 1.174 | 1.864 | 2.104 | 2.344 | 2.224 | 2.163 | 2.120 | 2.362 | 2.240 | 2.210 | ns |
| | | $t_h$ | -0.893 | -0.894 | -1.447 | -1.639 | -1.828 | -1.736 | -1.666 | -1.644 | -1.834 | -1.741 | -1.709 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.749 | -0.794 | -1.145 | -1.244 | -1.343 | -1.291 | -1.633 | -1.246 | -1.344 | -1.293 | -1.677 | ns |
| | | $t_h$ | 0.875 | 0.936 | 1.345 | 1.468 | 1.587 | 1.524 | 1.867 | 1.479 | 1.597 | 1.535 | 1.912 | ns |
| | GCLK PLL | $t_{su}$ | 1.156 | 1.174 | 1.864 | 2.104 | 2.344 | 2.224 | 2.163 | 2.120 | 2.362 | 2.240 | 2.210 | ns |
| | | $t_h$ | -0.893 | -0.894 | -1.447 | -1.639 | -1.828 | -1.736 | -1.666 | -1.644 | -1.834 | -1.741 | -1.709 | ns |

**Table 1–116.** EP3SE80 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.758 | -0.806 | -1.154 | -1.254 | -1.359 | -1.307 | -1.649 | -1.255 | -1.360 | -1.309 | -1.693 | ns |
| | | $t_h$ | 0.884 | 0.948 | 1.354 | 1.478 | 1.603 | 1.540 | 1.883 | 1.488 | 1.613 | 1.551 | 1.928 | ns |
| | GCLK PLL | $t_{su}$ | 1.147 | 1.162 | 1.855 | 2.094 | 2.328 | 2.208 | 2.147 | 2.111 | 2.346 | 2.224 | 2.194 | ns |
| | | $t_h$ | -0.884 | -0.882 | -1.438 | -1.629 | -1.812 | -1.720 | -1.650 | -1.635 | -1.818 | -1.725 | -1.693 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.758 | -0.806 | -1.154 | -1.254 | -1.359 | -1.307 | -1.649 | -1.255 | -1.360 | -1.309 | -1.693 | ns |
| | | $t_h$ | 0.884 | 0.948 | 1.354 | 1.478 | 1.603 | 1.540 | 1.883 | 1.488 | 1.613 | 1.551 | 1.928 | ns |
| | GCLK PLL | $t_{su}$ | 1.147 | 1.162 | 1.855 | 2.094 | 2.328 | 2.208 | 2.147 | 2.111 | 2.346 | 2.224 | 2.194 | ns |
| | | $t_h$ | -0.884 | -0.882 | -1.438 | -1.629 | -1.812 | -1.720 | -1.650 | -1.635 | -1.818 | -1.725 | -1.693 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.772 | -0.818 | -1.163 | -1.264 | -1.377 | -1.325 | -1.667 | -1.266 | -1.377 | -1.326 | -1.710 | ns |
| | | $t_h$ | 0.898 | 0.960 | 1.364 | 1.488 | 1.621 | 1.558 | 1.901 | 1.499 | 1.630 | 1.568 | 1.945 | ns |
| | GCLK PLL | $t_{su}$ | 1.133 | 1.150 | 1.842 | 2.084 | 2.310 | 2.190 | 2.129 | 2.100 | 2.329 | 2.207 | 2.177 | ns |
| | | $t_h$ | -0.870 | -0.870 | -1.426 | -1.619 | -1.794 | -1.702 | -1.632 | -1.624 | -1.801 | -1.708 | -1.676 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.772 | -0.818 | -1.163 | -1.264 | -1.377 | -1.325 | -1.667 | -1.266 | -1.377 | -1.326 | -1.710 | ns |
| | | $t_h$ | 0.898 | 0.960 | 1.364 | 1.488 | 1.621 | 1.558 | 1.901 | 1.499 | 1.630 | 1.568 | 1.945 | ns |
| | GCLK PLL | $t_{su}$ | 1.133 | 1.150 | 1.842 | 2.084 | 2.310 | 2.190 | 2.129 | 2.100 | 2.329 | 2.207 | 2.177 | ns |
| | | $t_h$ | -0.870 | -0.870 | -1.426 | -1.619 | -1.794 | -1.702 | -1.632 | -1.624 | -1.801 | -1.708 | -1.676 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.758 | -0.806 | -1.154 | -1.254 | -1.359 | -1.307 | -1.649 | -1.255 | -1.360 | -1.309 | -1.693 | ns |
| | | $t_h$ | 0.884 | 0.948 | 1.354 | 1.478 | 1.603 | 1.540 | 1.883 | 1.488 | 1.613 | 1.551 | 1.928 | ns |
| | GCLK PLL | $t_{su}$ | 1.147 | 1.162 | 1.855 | 2.094 | 2.328 | 2.208 | 2.147 | 2.111 | 2.346 | 2.224 | 2.194 | ns |
| | | $t_h$ | -0.884 | -0.882 | -1.438 | -1.629 | -1.812 | -1.720 | -1.650 | -1.635 | -1.818 | -1.725 | -1.693 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.758 | -0.806 | -1.154 | -1.254 | -1.359 | -1.307 | -1.649 | -1.255 | -1.360 | -1.309 | -1.693 | ns |
| | | $t_h$ | 0.884 | 0.948 | 1.354 | 1.478 | 1.603 | 1.540 | 1.883 | 1.488 | 1.613 | 1.551 | 1.928 | ns |
| | GCLK PLL | $t_{su}$ | 1.147 | 1.162 | 1.855 | 2.094 | 2.328 | 2.208 | 2.147 | 2.111 | 2.346 | 2.224 | 2.194 | ns |
| | | $t_h$ | -0.884 | -0.882 | -1.438 | -1.629 | -1.812 | -1.720 | -1.650 | -1.635 | -1.818 | -1.725 | -1.693 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -0.772 | -0.818 | -1.163 | -1.264 | -1.377 | -1.325 | -1.667 | -1.266 | -1.377 | -1.326 | -1.710 | ns |
| | | $t_h$ | 0.898 | 0.960 | 1.364 | 1.488 | 1.621 | 1.558 | 1.901 | 1.499 | 1.630 | 1.568 | 1.945 | ns |
| | GCLK PLL | $t_{su}$ | 1.133 | 1.150 | 1.842 | 2.084 | 2.310 | 2.190 | 2.129 | 2.100 | 2.329 | 2.207 | 2.177 | ns |
| | | $t_h$ | -0.870 | -0.870 | -1.426 | -1.619 | -1.794 | -1.702 | -1.632 | -1.624 | -1.801 | -1.708 | -1.676 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -0.772 | -0.818 | -1.163 | -1.264 | -1.377 | -1.325 | -1.667 | -1.266 | -1.377 | -1.326 | -1.710 | ns |
| | | $t_h$ | 0.898 | 0.960 | 1.364 | 1.488 | 1.621 | 1.558 | 1.901 | 1.499 | 1.630 | 1.568 | 1.945 | ns |
| | GCLK PLL | $t_{su}$ | 1.133 | 1.150 | 1.842 | 2.084 | 2.310 | 2.190 | 2.129 | 2.100 | 2.329 | 2.207 | 2.177 | ns |
| | | $t_h$ | -0.870 | -0.870 | -1.426 | -1.619 | -1.794 | -1.702 | -1.632 | -1.624 | -1.801 | -1.708 | -1.676 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.781 | -0.827 | -1.178 | -1.275 | -1.384 | -1.333 | -1.673 | -1.273 | -1.378 | -1.329 | -1.712 | ns |
| | | $t_h$ | 0.907 | 0.969 | 1.379 | 1.502 | 1.631 | 1.568 | 1.912 | 1.509 | 1.636 | 1.573 | 1.952 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.141 | 1.827 | 2.068 | 2.299 | 2.178 | 2.118 | 2.089 | 2.323 | 2.199 | 2.170 | ns |
| | | $t_h$ | -0.861 | -0.861 | -1.411 | -1.601 | -1.780 | -1.688 | -1.617 | -1.610 | -1.792 | -1.699 | -1.665 | ns |

**Table 1–116.** EP3SE80 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.781 | -0.827 | -1.178 | -1.275 | -1.384 | -1.333 | -1.673 | -1.273 | -1.378 | -1.329 | -1.712 | ns |
| | | $t_h$ | 0.907 | 0.969 | 1.379 | 1.502 | 1.631 | 1.568 | 1.912 | 1.509 | 1.636 | 1.573 | 1.952 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.141 | 1.827 | 2.068 | 2.299 | 2.178 | 2.118 | 2.089 | 2.323 | 2.199 | 2.170 | ns |
| | | $t_h$ | -0.861 | -0.861 | -1.411 | -1.601 | -1.780 | -1.688 | -1.617 | -1.610 | -1.792 | -1.699 | -1.665 | ns |

Table 1–117 lists the EP3SE80 column pins output timing parameters for differential I/O standards.

**Table 1–117.** EP3SE80 Column Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.152 | 3.387 | 4.757 | 5.155 | 5.666 | 5.526 | 5.826 | 5.278 | 5.789 | 5.650 | 5.899 | ns |
| | | GCLK PLL | $t_{co}$ | 1.328 | 1.502 | 1.913 | 2.006 | 2.214 | 2.225 | 2.251 | 2.110 | 2.321 | 2.331 | 2.237 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.148 | 3.390 | 4.804 | 5.210 | 5.728 | 5.588 | 5.888 | 5.337 | 5.855 | 5.716 | 5.965 | ns |
| | | GCLK PLL | $t_{co}$ | 1.324 | 1.505 | 1.960 | 2.061 | 2.276 | 2.287 | 2.313 | 2.169 | 2.387 | 2.397 | 2.303 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.152 | 3.387 | 4.757 | 5.155 | 5.666 | 5.526 | 5.826 | 5.278 | 5.789 | 5.650 | 5.899 | ns |
| | | GCLK PLL | $t_{co}$ | 1.328 | 1.502 | 1.913 | 2.006 | 2.214 | 2.225 | 2.251 | 2.110 | 2.321 | 2.331 | 2.237 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.148 | 3.390 | 4.804 | 5.210 | 5.728 | 5.588 | 5.888 | 5.337 | 5.855 | 5.716 | 5.965 | ns |
| | | GCLK PLL | $t_{co}$ | 1.324 | 1.505 | 1.960 | 2.061 | 2.276 | 2.287 | 2.313 | 2.169 | 2.387 | 2.397 | 2.303 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.152 | 3.387 | 4.757 | 5.155 | 5.666 | 5.526 | 5.826 | 5.278 | 5.789 | 5.650 | 5.899 | ns |
| | | GCLK PLL | $t_{co}$ | 1.328 | 1.502 | 1.913 | 2.006 | 2.214 | 2.225 | 2.251 | 2.110 | 2.321 | 2.331 | 2.237 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.148 | 3.390 | 4.804 | 5.210 | 5.728 | 5.588 | 5.888 | 5.337 | 5.855 | 5.716 | 5.965 | ns |
| | | GCLK PLL | $t_{co}$ | 1.324 | 1.505 | 1.960 | 2.061 | 2.276 | 2.287 | 2.313 | 2.169 | 2.387 | 2.397 | 2.303 | ns |


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**Table 1–117.** EP3SE80 Column Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.179 | 3.420 | 4.828 | 5.233 | 5.750 | 5.610 | 5.910 | 5.358 | 5.875 | 5.736 | 5.985 | ns |
| | | GCLK PLL | $t_{co}$ | 1.355 | 1.535 | 1.984 | 2.084 | 2.298 | 2.309 | 2.335 | 2.190 | 2.407 | 2.417 | 2.323 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.169 | 3.410 | 4.818 | 5.222 | 5.740 | 5.600 | 5.900 | 5.347 | 5.865 | 5.726 | 5.975 | ns |
| | | GCLK PLL | $t_{co}$ | 1.345 | 1.525 | 1.974 | 2.073 | 2.288 | 2.299 | 2.325 | 2.179 | 2.397 | 2.407 | 2.313 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.169 | 3.410 | 4.821 | 5.226 | 5.744 | 5.604 | 5.904 | 5.352 | 5.870 | 5.731 | 5.980 | ns |
| | | GCLK PLL | $t_{co}$ | 1.345 | 1.525 | 1.977 | 2.077 | 2.292 | 2.303 | 2.329 | 2.184 | 2.402 | 2.412 | 2.318 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.162 | 3.404 | 4.814 | 5.220 | 5.738 | 5.598 | 5.898 | 5.345 | 5.864 | 5.725 | 5.974 | ns |
| | | GCLK PLL | $t_{co}$ | 1.338 | 1.519 | 1.970 | 2.071 | 2.286 | 2.297 | 2.323 | 2.177 | 2.396 | 2.406 | 2.312 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.161 | 3.402 | 4.811 | 5.217 | 5.735 | 5.595 | 5.895 | 5.342 | 5.860 | 5.721 | 5.970 | ns |
| | | GCLK PLL | $t_{co}$ | 1.337 | 1.517 | 1.967 | 2.068 | 2.283 | 2.294 | 2.320 | 2.174 | 2.392 | 2.402 | 2.308 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.183 | 3.424 | 4.832 | 5.237 | 5.754 | 5.614 | 5.914 | 5.362 | 5.880 | 5.741 | 5.990 | ns |
| | | GCLK PLL | $t_{co}$ | 1.359 | 1.539 | 1.988 | 2.088 | 2.302 | 2.313 | 2.339 | 2.194 | 2.412 | 2.422 | 2.328 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.173 | 3.413 | 4.811 | 5.214 | 5.729 | 5.589 | 5.889 | 5.338 | 5.853 | 5.714 | 5.963 | ns |
| | | GCLK PLL | $t_{co}$ | 1.349 | 1.528 | 1.967 | 2.065 | 2.277 | 2.288 | 2.314 | 2.170 | 2.385 | 2.395 | 2.301 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.168 | 3.409 | 4.811 | 5.214 | 5.730 | 5.590 | 5.890 | 5.339 | 5.855 | 5.716 | 5.965 | ns |
| | | GCLK PLL | $t_{co}$ | 1.344 | 1.524 | 1.967 | 2.065 | 2.278 | 2.289 | 2.315 | 2.171 | 2.387 | 2.397 | 2.303 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.166 | 3.407 | 4.810 | 5.213 | 5.728 | 5.588 | 5.888 | 5.338 | 5.854 | 5.715 | 5.964 | ns |
| | | GCLK PLL | $t_{co}$ | 1.342 | 1.522 | 1.966 | 2.064 | 2.276 | 2.287 | 2.313 | 2.170 | 2.386 | 2.396 | 2.302 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.158 | 3.398 | 4.800 | 5.203 | 5.719 | 5.579 | 5.879 | 5.328 | 5.844 | 5.705 | 5.954 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.513 | 1.956 | 2.054 | 2.267 | 2.278 | 2.304 | 2.160 | 2.376 | 2.386 | 2.292 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.159 | 3.400 | 4.806 | 5.210 | 5.727 | 5.587 | 5.887 | 5.336 | 5.853 | 5.714 | 5.963 | ns |
| | | GCLK PLL | $t_{co}$ | 1.335 | 1.515 | 1.962 | 2.061 | 2.275 | 2.286 | 2.312 | 2.168 | 2.385 | 2.395 | 2.301 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.158 | 3.397 | 4.789 | 5.191 | 5.705 | 5.565 | 5.865 | 5.315 | 5.829 | 5.690 | 5.939 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.512 | 1.945 | 2.042 | 2.253 | 2.264 | 2.290 | 2.147 | 2.361 | 2.371 | 2.277 | ns |

**Table 1–117.** EP3SE80 Column Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.170 | 3.410 | 4.807 | 5.209 | 5.723 | 5.583 | 5.883 | 5.334 | 5.848 | 5.709 | 5.958 | ns |
| | | GCLK PLL | $t_{co}$ | 1.346 | 1.525 | 1.963 | 2.060 | 2.271 | 2.282 | 2.308 | 2.166 | 2.380 | 2.390 | 2.296 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.166 | 3.407 | 4.808 | 5.211 | 5.727 | 5.587 | 5.887 | 5.336 | 5.852 | 5.713 | 5.962 | ns |
| | | GCLK PLL | $t_{co}$ | 1.342 | 1.522 | 1.964 | 2.062 | 2.275 | 2.286 | 2.312 | 2.168 | 2.384 | 2.394 | 2.300 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.156 | 3.396 | 4.797 | 5.200 | 5.715 | 5.575 | 5.875 | 5.325 | 5.840 | 5.701 | 5.950 | ns |
| | | GCLK PLL | $t_{co}$ | 1.332 | 1.511 | 1.953 | 2.051 | 2.263 | 2.274 | 2.300 | 2.157 | 2.372 | 2.382 | 2.288 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.154 | 3.394 | 4.795 | 5.197 | 5.713 | 5.573 | 5.873 | 5.323 | 5.838 | 5.699 | 5.948 | ns |
| | | GCLK PLL | $t_{co}$ | 1.330 | 1.509 | 1.951 | 2.048 | 2.261 | 2.272 | 2.298 | 2.155 | 2.370 | 2.380 | 2.286 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.154 | 3.395 | 4.798 | 5.202 | 5.718 | 5.578 | 5.878 | 5.327 | 5.844 | 5.705 | 5.954 | ns |
| | | GCLK PLL | $t_{co}$ | 1.330 | 1.510 | 1.954 | 2.053 | 2.266 | 2.277 | 2.303 | 2.159 | 2.376 | 2.386 | 2.292 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.158 | 3.398 | 4.795 | 5.197 | 5.712 | 5.572 | 5.872 | 5.322 | 5.837 | 5.698 | 5.947 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.513 | 1.951 | 2.048 | 2.260 | 2.271 | 2.297 | 2.154 | 2.369 | 2.379 | 2.285 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.184 | 3.427 | 4.840 | 5.245 | 5.762 | 5.622 | 5.922 | 5.370 | 5.887 | 5.748 | 5.997 | ns |
| | | GCLK PLL | $t_{co}$ | 1.360 | 1.542 | 1.996 | 2.096 | 2.310 | 2.321 | 2.347 | 2.202 | 2.419 | 2.429 | 2.335 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.170 | 3.413 | 4.828 | 5.234 | 5.752 | 5.612 | 5.912 | 5.360 | 5.878 | 5.739 | 5.988 | ns |
| | | GCLK PLL | $t_{co}$ | 1.346 | 1.528 | 1.984 | 2.085 | 2.300 | 2.311 | 2.337 | 2.192 | 2.410 | 2.420 | 2.326 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.158 | 3.400 | 4.811 | 5.216 | 5.734 | 5.594 | 5.894 | 5.342 | 5.860 | 5.721 | 5.970 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.515 | 1.967 | 2.067 | 2.282 | 2.293 | 2.319 | 2.174 | 2.392 | 2.402 | 2.308 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.158 | 3.400 | 4.814 | 5.220 | 5.738 | 5.598 | 5.898 | 5.346 | 5.865 | 5.726 | 5.975 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.515 | 1.970 | 2.071 | 2.286 | 2.297 | 2.323 | 2.178 | 2.397 | 2.407 | 2.313 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.154 | 3.396 | 4.807 | 5.212 | 5.731 | 5.591 | 5.891 | 5.339 | 5.857 | 5.718 | 5.967 | ns |
| | | GCLK PLL | $t_{co}$ | 1.330 | 1.511 | 1.963 | 2.063 | 2.279 | 2.290 | 2.316 | 2.171 | 2.389 | 2.399 | 2.305 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.158 | 3.398 | 4.800 | 5.203 | 5.719 | 5.579 | 5.879 | 5.328 | 5.844 | 5.705 | 5.954 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.513 | 1.956 | 2.054 | 2.267 | 2.278 | 2.304 | 2.160 | 2.376 | 2.386 | 2.292 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.159 | 3.400 | 4.808 | 5.213 | 5.730 | 5.590 | 5.890 | 5.338 | 5.856 | 5.717 | 5.966 | ns |
| | | GCLK PLL | $t_{co}$ | 1.335 | 1.515 | 1.964 | 2.064 | 2.278 | 2.289 | 2.315 | 2.170 | 2.388 | 2.398 | 2.304 | ns |


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**Table 1–117.** EP3SE80 Column Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.187 | 3.430 | 4.839 | 5.243 | 5.760 | 5.620 | 5.920 | 5.369 | 5.885 | 5.746 | 5.995 | ns |
| | | GCLK PLL | $t_{co}$ | 1.363 | 1.545 | 1.995 | 2.094 | 2.308 | 2.319 | 2.345 | 2.201 | 2.417 | 2.427 | 2.333 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.176 | 3.418 | 4.827 | 5.231 | 5.748 | 5.608 | 5.908 | 5.357 | 5.873 | 5.734 | 5.983 | ns |
| | | GCLK PLL | $t_{co}$ | 1.352 | 1.533 | 1.983 | 2.082 | 2.296 | 2.307 | 2.333 | 2.189 | 2.405 | 2.415 | 2.321 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.171 | 3.414 | 4.827 | 5.232 | 5.749 | 5.609 | 5.909 | 5.358 | 5.875 | 5.736 | 5.985 | ns |
| | | GCLK PLL | $t_{co}$ | 1.347 | 1.529 | 1.983 | 2.083 | 2.297 | 2.308 | 2.334 | 2.190 | 2.407 | 2.417 | 2.323 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.157 | 3.399 | 4.809 | 5.213 | 5.730 | 5.590 | 5.890 | 5.339 | 5.857 | 5.718 | 5.967 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.514 | 1.965 | 2.064 | 2.278 | 2.289 | 2.315 | 2.171 | 2.389 | 2.399 | 2.305 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.155 | 3.397 | 4.807 | 5.211 | 5.728 | 5.588 | 5.888 | 5.337 | 5.854 | 5.715 | 5.964 | ns |
| | | GCLK PLL | $t_{co}$ | 1.331 | 1.512 | 1.963 | 2.062 | 2.276 | 2.287 | 2.313 | 2.169 | 2.386 | 2.396 | 2.302 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.159 | 3.399 | 4.799 | 5.201 | 5.716 | 5.576 | 5.876 | 5.326 | 5.841 | 5.702 | 5.951 | ns |
| | | GCLK PLL | $t_{co}$ | 1.335 | 1.514 | 1.955 | 2.052 | 2.264 | 2.275 | 2.301 | 2.158 | 2.373 | 2.383 | 2.289 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.159 | 3.400 | 4.807 | 5.211 | 5.728 | 5.588 | 5.888 | 5.337 | 5.854 | 5.715 | 5.964 | ns |
| | | GCLK PLL | $t_{co}$ | 1.335 | 1.515 | 1.963 | 2.062 | 2.276 | 2.287 | 2.313 | 2.169 | 2.386 | 2.396 | 2.302 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.175 | 3.417 | 4.823 | 5.226 | 5.742 | 5.602 | 5.902 | 5.352 | 5.867 | 5.728 | 5.977 | ns |
| | | GCLK PLL | $t_{co}$ | 1.351 | 1.532 | 1.979 | 2.077 | 2.290 | 2.301 | 2.327 | 2.184 | 2.399 | 2.409 | 2.315 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.175 | 3.417 | 4.823 | 5.226 | 5.742 | 5.602 | 5.902 | 5.352 | 5.867 | 5.728 | 5.977 | ns |
| | | GCLK PLL | $t_{co}$ | 1.351 | 1.532 | 1.979 | 2.077 | 2.290 | 2.301 | 2.327 | 2.184 | 2.399 | 2.409 | 2.315 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.165 | 3.407 | 4.813 | 5.216 | 5.732 | 5.592 | 5.892 | 5.342 | 5.858 | 5.719 | 5.968 | ns |
| | | GCLK PLL | $t_{co}$ | 1.341 | 1.522 | 1.969 | 2.067 | 2.280 | 2.291 | 2.317 | 2.174 | 2.390 | 2.400 | 2.306 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.158 | 3.399 | 4.799 | 5.201 | 5.716 | 5.576 | 5.876 | 5.326 | 5.841 | 5.702 | 5.951 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.514 | 1.955 | 2.052 | 2.264 | 2.275 | 2.301 | 2.158 | 2.373 | 2.383 | 2.289 | ns |

Table 1–118 lists the EP3SE80 row pins output timing parameters for differential I/O standards.

**Table 1–118.** EP3SE80 Row Pins Output Timing Parameters (Part 1 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | — | GCLK | $t_{co}$ | 2.744 | 2.932 | 4.083 | 4.440 | 4.901 | 4.771 | 5.049 | 4.540 | 5.002 | 4.873 | 5.107 | ns |
| | | GCLK PLL | $t_{co}$ | 0.931 | 1.057 | 1.249 | 1.300 | 1.458 | 1.480 | 1.486 | 1.382 | 1.545 | 1.563 | 1.456 | ns |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.136 | 3.376 | 4.754 | 5.156 | 5.664 | 5.526 | 5.797 | 5.281 | 5.790 | 5.652 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.511 | 1.930 | 2.026 | 2.231 | 2.245 | 2.243 | 2.133 | 2.343 | 2.352 | 2.229 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.118 | 3.366 | 4.792 | 5.202 | 5.718 | 5.580 | 5.851 | 5.332 | 5.851 | 5.713 | 5.932 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.501 | 1.968 | 2.072 | 2.285 | 2.299 | 2.297 | 2.184 | 2.404 | 2.413 | 2.290 | ns |
| MINI-LVDS | — | GCLK | $t_{co}$ | 2.744 | 2.932 | 4.083 | 4.440 | 4.901 | 4.771 | 5.049 | 4.540 | 5.002 | 4.873 | 5.107 | ns |
| | | GCLK PLL | $t_{co}$ | 0.931 | 1.057 | 1.249 | 1.300 | 1.458 | 1.480 | 1.486 | 1.382 | 1.545 | 1.563 | 1.456 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.136 | 3.376 | 4.754 | 5.156 | 5.664 | 5.526 | 5.797 | 5.281 | 5.790 | 5.652 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.511 | 1.930 | 2.026 | 2.231 | 2.245 | 2.243 | 2.133 | 2.343 | 2.352 | 2.229 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.118 | 3.366 | 4.792 | 5.202 | 5.718 | 5.580 | 5.851 | 5.332 | 5.851 | 5.713 | 5.932 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.501 | 1.968 | 2.072 | 2.285 | 2.299 | 2.297 | 2.184 | 2.404 | 2.413 | 2.290 | ns |
| RSDS | — | GCLK | $t_{co}$ | 2.744 | 2.932 | 4.083 | 4.440 | 4.901 | 4.771 | 5.049 | 4.540 | 5.002 | 4.873 | 5.107 | ns |
| | | GCLK PLL | $t_{co}$ | 0.931 | 1.057 | 1.249 | 1.300 | 1.458 | 1.480 | 1.486 | 1.382 | 1.545 | 1.563 | 1.456 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.136 | 3.376 | 4.754 | 5.156 | 5.664 | 5.526 | 5.797 | 5.281 | 5.790 | 5.652 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.511 | 1.930 | 2.026 | 2.231 | 2.245 | 2.243 | 2.133 | 2.343 | 2.352 | 2.229 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.118 | 3.366 | 4.792 | 5.202 | 5.718 | 5.580 | 5.851 | 5.332 | 5.851 | 5.713 | 5.932 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.501 | 1.968 | 2.072 | 2.285 | 2.299 | 2.297 | 2.184 | 2.404 | 2.413 | 2.290 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.162 | 3.409 | 4.828 | 5.236 | 5.751 | 5.613 | 5.884 | 5.365 | 5.880 | 5.742 | 5.961 | ns |
| | | GCLK PLL | $t_{co}$ | 1.359 | 1.544 | 2.004 | 2.106 | 2.318 | 2.332 | 2.330 | 2.217 | 2.433 | 2.442 | 2.319 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.148 | 3.395 | 4.815 | 5.223 | 5.738 | 5.600 | 5.871 | 5.351 | 5.867 | 5.729 | 5.948 | ns |
| | | GCLK PLL | $t_{co}$ | 1.345 | 1.530 | 1.991 | 2.093 | 2.305 | 2.319 | 2.317 | 2.203 | 2.420 | 2.429 | 2.306 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.144 | 3.391 | 4.813 | 5.223 | 5.739 | 5.601 | 5.872 | 5.351 | 5.869 | 5.731 | 5.950 | ns |
| | | GCLK PLL | $t_{co}$ | 1.341 | 1.526 | 1.989 | 2.093 | 2.306 | 2.320 | 2.318 | 2.203 | 2.422 | 2.431 | 2.308 | ns |


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**Table 1–118.** EP3SE80 Row Pins Output Timing Parameters (Part 2 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.160 | 3.406 | 4.814 | 5.220 | 5.733 | 5.595 | 5.866 | 5.348 | 5.862 | 5.724 | 5.943 | ns |
| | | GCLK PLL | $t_{co}$ | 1.357 | 1.541 | 1.990 | 2.090 | 2.300 | 2.314 | 2.312 | 2.200 | 2.415 | 2.424 | 2.301 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.149 | 3.396 | 4.810 | 5.216 | 5.730 | 5.592 | 5.863 | 5.345 | 5.859 | 5.721 | 5.940 | ns |
| | | GCLK PLL | $t_{co}$ | 1.346 | 1.531 | 1.986 | 2.086 | 2.297 | 2.311 | 2.309 | 2.197 | 2.412 | 2.421 | 2.298 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.146 | 3.393 | 4.808 | 5.214 | 5.728 | 5.590 | 5.861 | 5.343 | 5.858 | 5.720 | 5.939 | ns |
| | | GCLK PLL | $t_{co}$ | 1.343 | 1.528 | 1.984 | 2.084 | 2.295 | 2.309 | 2.307 | 2.195 | 2.411 | 2.420 | 2.297 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.157 | 3.403 | 4.809 | 5.215 | 5.727 | 5.589 | 5.860 | 5.343 | 5.856 | 5.718 | 5.937 | ns |
| | | GCLK PLL | $t_{co}$ | 1.354 | 1.538 | 1.985 | 2.085 | 2.294 | 2.308 | 2.306 | 2.195 | 2.409 | 2.418 | 2.295 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.147 | 3.394 | 4.807 | 5.213 | 5.726 | 5.588 | 5.859 | 5.342 | 5.856 | 5.718 | 5.937 | ns |
| | | GCLK PLL | $t_{co}$ | 1.344 | 1.529 | 1.983 | 2.083 | 2.293 | 2.307 | 2.305 | 2.194 | 2.409 | 2.418 | 2.295 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.133 | 3.380 | 4.792 | 5.198 | 5.712 | 5.574 | 5.845 | 5.327 | 5.841 | 5.703 | 5.922 | ns |
| | | GCLK PLL | $t_{co}$ | 1.330 | 1.515 | 1.968 | 2.068 | 2.279 | 2.293 | 2.291 | 2.179 | 2.394 | 2.403 | 2.280 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.130 | 3.376 | 4.788 | 5.194 | 5.708 | 5.570 | 5.841 | 5.323 | 5.837 | 5.699 | 5.918 | ns |
| | | GCLK PLL | $t_{co}$ | 1.327 | 1.511 | 1.964 | 2.064 | 2.275 | 2.289 | 2.287 | 2.175 | 2.390 | 2.399 | 2.276 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.127 | 3.374 | 4.789 | 5.197 | 5.711 | 5.573 | 5.844 | 5.326 | 5.841 | 5.703 | 5.922 | ns |
| | | GCLK PLL | $t_{co}$ | 1.324 | 1.509 | 1.965 | 2.067 | 2.278 | 2.292 | 2.290 | 2.178 | 2.394 | 2.403 | 2.280 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.128 | 3.374 | 4.779 | 5.185 | 5.698 | 5.560 | 5.831 | 5.313 | 5.827 | 5.689 | 5.908 | ns |
| | | GCLK PLL | $t_{co}$ | 1.325 | 1.509 | 1.955 | 2.055 | 2.265 | 2.279 | 2.277 | 2.165 | 2.380 | 2.389 | 2.266 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.177 | 3.427 | 4.850 | 5.258 | 5.774 | 5.636 | 5.907 | 5.387 | 5.903 | 5.765 | 5.984 | ns |
| | | GCLK PLL | $t_{co}$ | 1.374 | 1.562 | 2.026 | 2.128 | 2.341 | 2.355 | 2.353 | 2.239 | 2.456 | 2.465 | 2.342 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.153 | 3.403 | 4.832 | 5.241 | 5.757 | 5.619 | 5.890 | 5.370 | 5.888 | 5.750 | 5.969 | ns |
| | | GCLK PLL | $t_{co}$ | 1.350 | 1.538 | 2.008 | 2.111 | 2.324 | 2.338 | 2.336 | 2.222 | 2.441 | 2.450 | 2.327 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.136 | 3.384 | 4.810 | 5.219 | 5.735 | 5.597 | 5.868 | 5.348 | 5.866 | 5.728 | 5.947 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.519 | 1.986 | 2.089 | 2.302 | 2.316 | 2.314 | 2.200 | 2.419 | 2.428 | 2.305 | ns |

**Table 1–118.** EP3SE80 Row Pins Output Timing Parameters (Part 3 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.181 | 3.430 | 4.850 | 5.258 | 5.773 | 5.635 | 5.906 | 5.387 | 5.903 | 5.765 | 5.984 | ns |
| | | GCLK PLL | $t_{co}$ | 1.378 | 1.565 | 2.026 | 2.128 | 2.340 | 2.354 | 2.352 | 2.239 | 2.456 | 2.465 | 2.342 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.166 | 3.415 | 4.836 | 5.243 | 5.758 | 5.620 | 5.891 | 5.372 | 5.888 | 5.750 | 5.969 | ns |
| | | GCLK PLL | $t_{co}$ | 1.363 | 1.550 | 2.012 | 2.113 | 2.325 | 2.339 | 2.337 | 2.224 | 2.441 | 2.450 | 2.327 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.155 | 3.404 | 4.831 | 5.240 | 5.755 | 5.617 | 5.888 | 5.369 | 5.886 | 5.748 | 5.967 | ns |
| | | GCLK PLL | $t_{co}$ | 1.352 | 1.539 | 2.007 | 2.110 | 2.322 | 2.336 | 2.334 | 2.221 | 2.439 | 2.448 | 2.325 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.135 | 3.384 | 4.808 | 5.216 | 5.732 | 5.594 | 5.865 | 5.346 | 5.862 | 5.724 | 5.943 | ns |
| | | GCLK PLL | $t_{co}$ | 1.332 | 1.519 | 1.984 | 2.086 | 2.299 | 2.313 | 2.311 | 2.198 | 2.415 | 2.424 | 2.301 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.132 | 3.380 | 4.804 | 5.213 | 5.728 | 5.590 | 5.861 | 5.342 | 5.859 | 5.721 | 5.940 | ns |
| | | GCLK PLL | $t_{co}$ | 1.329 | 1.515 | 1.980 | 2.083 | 2.295 | 2.309 | 2.307 | 2.194 | 2.412 | 2.421 | 2.298 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.137 | 3.384 | 4.795 | 5.201 | 5.714 | 5.576 | 5.847 | 5.329 | 5.843 | 5.705 | 5.924 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.519 | 1.971 | 2.071 | 2.281 | 2.295 | 2.293 | 2.181 | 2.396 | 2.405 | 2.282 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.130 | 3.377 | 4.794 | 5.202 | 5.717 | 5.579 | 5.850 | 5.332 | 5.848 | 5.710 | 5.929 | ns |
| | | GCLK PLL | $t_{co}$ | 1.327 | 1.512 | 1.970 | 2.072 | 2.284 | 2.298 | 2.296 | 2.184 | 2.401 | 2.410 | 2.287 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.168 | 3.416 | 4.832 | 5.239 | 5.753 | 5.615 | 5.886 | 5.368 | 5.883 | 5.745 | 5.964 | ns |
| | | GCLK PLL | $t_{co}$ | 1.365 | 1.551 | 2.008 | 2.109 | 2.320 | 2.334 | 2.332 | 2.220 | 2.436 | 2.445 | 2.322 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.150 | 3.399 | 4.817 | 5.224 | 5.738 | 5.600 | 5.871 | 5.353 | 5.868 | 5.730 | 5.949 | ns |
| | | GCLK PLL | $t_{co}$ | 1.347 | 1.534 | 1.993 | 2.094 | 2.305 | 2.319 | 2.317 | 2.205 | 2.421 | 2.430 | 2.307 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.136 | 3.383 | 4.794 | 5.200 | 5.713 | 5.575 | 5.846 | 5.329 | 5.843 | 5.705 | 5.924 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.518 | 1.970 | 2.070 | 2.280 | 2.294 | 2.292 | 2.181 | 2.396 | 2.405 | 2.282 | ns |


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Table 1–119 and Table 1–120 list the EP3SE80 regional clock (RCLK) adder values that must be added to the GCLK values. Use these adder values to determine I/O timing when the I/O pin is driven using the regional clock. This applies to all I/O standards supported by Stratix III devices.

Table 1–119 lists the EP3SE80 column pin delay adders when using the regional clock.

**Table 1–119.** EP3SE80 Column Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.251 | 0.187 | 0.308 | 0.239 | 0.389 | 0.103 | 0.176 | 0.199 | 0.102 | 0.099 | 0.172 | ns |
| RCLK PLL input adder | 1.895 | 1.982 | 2.923 | 3.16 | 3.601 | 4.28 | 4.913 | 3.261 | 4.491 | 4.295 | 4.833 | ns |
| RCLK output adder | -0.069 | 0.253 | 0.551 | 0.865 | 0.693 | -0.059 | -0.119 | 1.06 | 0.135 | 0.066 | -0.046 | ns |
| RCLK PLL output adder | -1.545 | -1.367 | -1.715 | -1.587 | -1.976 | -3.145 | -3.116 | -1.541 | -3.343 | -3.027 | -3.123 | ns |

Table 1–120 lists the EP3SE80 row pin delay adders when using the regional clock.

**Table 1–120.** EP3SE80 Row Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.014 | 0.014 | 0.018 | 0.005 | -0.022 | 0.0 | 0.052 | -0.004 | -0.014 | -0.008 | 0.056 | ns |
| RCLK PLL input adder | 0.116 | 0.122 | 0.192 | 0.206 | 0.231 | 0.217 | 0.367 | 0.198 | 0.223 | 0.21 | 0.371 | ns |
| RCLK output adder | 0.004 | 0.003 | 0.029 | 0.042 | 0.056 | 0.039 | -0.021 | 0.047 | 0.061 | 0.049 | -0.025 | ns |
| RCLK PLL output adder | -0.089 | -0.089 | -0.145 | -0.161 | -0.197 | -0.169 | -0.332 | -0.151 | -0.186 | -0.157 | -0.333 | ns |

## EP3SE110 I/O Timing Parameters

Table 1–121 through Table 1–124 list the maximum I/O timing parameters for EP3SE110 for single-ended I/O standards.

Table 1–121 lists the EP3SE110 column pins input timing parameters for single-ended I/O standards.

**Table 1–121.** EP3SE110 Column Pins Input Timing Parameters (Part 1 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -1.030 | -1.006 | -1.454 | -1.613 | -1.847 | -1.786 | -2.148 | -1.613 | -1.847 | -1.786 | -2.148 | ns |
| | | $t_h$ | 1.172 | 1.144 | 1.648 | 1.838 | 2.093 | 2.017 | 2.385 | 1.838 | 2.093 | 2.017 | 2.385 | ns |
| | GCLK PLL | $t_{su}$ | -1.297 | -1.267 | -1.831 | -2.023 | -2.261 | -2.187 | -2.655 | -2.023 | -2.261 | -2.187 | -2.655 | ns |
| | | $t_h$ | 1.600 | 1.565 | 2.262 | 2.514 | 2.793 | 2.689 | 3.180 | 2.514 | 2.793 | 2.689 | 3.180 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -1.030 | -1.006 | -1.454 | -1.613 | -1.847 | -1.786 | -2.148 | -1.613 | -1.847 | -1.786 | -2.148 | ns |
| | | $t_h$ | 1.172 | 1.144 | 1.648 | 1.838 | 2.093 | 2.017 | 2.385 | 1.838 | 2.093 | 2.017 | 2.385 | ns |
| | GCLK PLL | $t_{su}$ | -1.297 | -1.267 | -1.831 | -2.023 | -2.261 | -2.187 | -2.655 | -2.023 | -2.261 | -2.187 | -2.655 | ns |
| | | $t_h$ | 1.600 | 1.565 | 2.262 | 2.514 | 2.793 | 2.689 | 3.180 | 2.514 | 2.793 | 2.689 | 3.180 | ns |

**Table 1–121.** EP3SE110 Column Pins Input Timing Parameters (Part 2 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -1.041 | -1.017 | -1.453 | -1.615 | -1.846 | -1.785 | -2.147 | -1.615 | -1.846 | -1.785 | -2.147 | ns |
| | | $t_h$ | 1.183 | 1.155 | 1.647 | 1.840 | 2.092 | 2.016 | 2.384 | 1.840 | 2.092 | 2.016 | 2.384 | ns |
| | GCLK PLL | $t_{su}$ | -1.308 | -1.278 | -1.830 | -2.025 | -2.260 | -2.186 | -2.654 | -2.025 | -2.260 | -2.186 | -2.654 | ns |
| | | $t_h$ | 1.611 | 1.576 | 2.261 | 2.516 | 2.792 | 2.688 | 3.179 | 2.516 | 2.792 | 2.688 | 3.179 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -1.041 | -1.017 | -1.453 | -1.615 | -1.846 | -1.785 | -2.147 | -1.615 | -1.846 | -1.785 | -2.147 | ns |
| | | $t_h$ | 1.183 | 1.155 | 1.647 | 1.840 | 2.092 | 2.016 | 2.384 | 1.840 | 2.092 | 2.016 | 2.384 | ns |
| | GCLK PLL | $t_{su}$ | -1.308 | -1.278 | -1.830 | -2.025 | -2.260 | -2.186 | -2.654 | -2.025 | -2.260 | -2.186 | -2.654 | ns |
| | | $t_h$ | 1.611 | 1.576 | 2.261 | 2.516 | 2.792 | 2.688 | 3.179 | 2.516 | 2.792 | 2.688 | 3.179 | ns |
| 2.5 V | GCLK | $t_{su}$ | -1.036 | -1.012 | -1.462 | -1.627 | -1.865 | -1.804 | -2.166 | -1.627 | -1.865 | -1.804 | -2.166 | ns |
| | | $t_h$ | 1.178 | 1.150 | 1.656 | 1.852 | 2.111 | 2.035 | 2.403 | 1.852 | 2.111 | 2.035 | 2.403 | ns |
| | GCLK PLL | $t_{su}$ | -1.303 | -1.273 | -1.839 | -2.037 | -2.279 | -2.205 | -2.673 | -2.037 | -2.279 | -2.205 | -2.673 | ns |
| | | $t_h$ | 1.606 | 1.571 | 2.270 | 2.528 | 2.811 | 2.707 | 3.198 | 2.528 | 2.811 | 2.707 | 3.198 | ns |
| 1.8 V | GCLK | $t_{su}$ | -1.058 | -1.034 | -1.502 | -1.663 | -1.863 | -1.802 | -2.164 | -1.663 | -1.863 | -1.802 | -2.164 | ns |
| | | $t_h$ | 1.202 | 1.174 | 1.696 | 1.888 | 2.109 | 2.033 | 2.401 | 1.888 | 2.109 | 2.033 | 2.401 | ns |
| | GCLK PLL | $t_{su}$ | -1.325 | -1.295 | -1.879 | -2.073 | -2.277 | -2.203 | -2.671 | -2.073 | -2.277 | -2.203 | -2.671 | ns |
| | | $t_h$ | 1.630 | 1.595 | 2.310 | 2.564 | 2.809 | 2.705 | 3.196 | 2.564 | 2.809 | 2.705 | 3.196 | ns |
| 1.5 V | GCLK | $t_{su}$ | -1.048 | -1.024 | -1.479 | -1.631 | -1.793 | -1.732 | -2.094 | -1.631 | -1.793 | -1.732 | -2.094 | ns |
| | | $t_h$ | 1.192 | 1.164 | 1.673 | 1.856 | 2.039 | 1.963 | 2.331 | 1.856 | 2.039 | 1.963 | 2.331 | ns |
| | GCLK PLL | $t_{su}$ | -1.315 | -1.285 | -1.856 | -2.041 | -2.207 | -2.133 | -2.601 | -2.041 | -2.207 | -2.133 | -2.601 | ns |
| | | $t_h$ | 1.620 | 1.585 | 2.287 | 2.532 | 2.739 | 2.635 | 3.126 | 2.532 | 2.739 | 2.635 | 3.126 | ns |
| 1.2 V | GCLK | $t_{su}$ | -0.996 | -0.972 | -1.402 | -1.532 | -1.637 | -1.576 | -1.938 | -1.532 | -1.637 | -1.576 | -1.938 | ns |
| | | $t_h$ | 1.140 | 1.112 | 1.596 | 1.757 | 1.883 | 1.807 | 2.175 | 1.757 | 1.883 | 1.807 | 2.175 | ns |
| | GCLK PLL | $t_{su}$ | -1.263 | -1.233 | -1.779 | -1.942 | -2.051 | -1.977 | -2.445 | -1.942 | -2.051 | -1.977 | -2.445 | ns |
| | | $t_h$ | 1.568 | 1.533 | 2.210 | 2.433 | 2.583 | 2.479 | 2.970 | 2.433 | 2.583 | 2.479 | 2.970 | ns |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -0.967 | -0.943 | -1.374 | -1.516 | -1.639 | -1.578 | -1.940 | -1.516 | -1.639 | -1.578 | -1.940 | ns |
| | | $t_h$ | 1.111 | 1.083 | 1.568 | 1.741 | 1.885 | 1.809 | 2.177 | 1.741 | 1.885 | 1.809 | 2.177 | ns |
| | GCLK PLL | $t_{su}$ | -1.234 | -1.204 | -1.751 | -1.926 | -2.053 | -1.979 | -2.447 | -1.926 | -2.053 | -1.979 | -2.447 | ns |
| | | $t_h$ | 1.539 | 1.504 | 2.182 | 2.417 | 2.585 | 2.481 | 2.972 | 2.417 | 2.585 | 2.481 | 2.972 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -0.967 | -0.943 | -1.374 | -1.516 | -1.639 | -1.578 | -1.940 | -1.516 | -1.639 | -1.578 | -1.940 | ns |
| | | $t_h$ | 1.111 | 1.083 | 1.568 | 1.741 | 1.885 | 1.809 | 2.177 | 1.741 | 1.885 | 1.809 | 2.177 | ns |
| | GCLK PLL | $t_{su}$ | -1.234 | -1.204 | -1.751 | -1.926 | -2.053 | -1.979 | -2.447 | -1.926 | -2.053 | -1.979 | -2.447 | ns |
| | | $t_h$ | 1.539 | 1.504 | 2.182 | 2.417 | 2.585 | 2.481 | 2.972 | 2.417 | 2.585 | 2.481 | 2.972 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -0.961 | -0.937 | -1.361 | -1.508 | -1.636 | -1.573 | -1.938 | -1.508 | -1.636 | -1.573 | -1.938 | ns |
| | | $t_h$ | 1.105 | 1.077 | 1.555 | 1.730 | 1.879 | 1.803 | 2.170 | 1.730 | 1.879 | 1.803 | 2.170 | ns |
| | GCLK PLL | $t_{su}$ | -1.228 | -1.198 | -1.738 | -1.918 | -2.050 | -1.974 | -2.445 | -1.918 | -2.050 | -1.974 | -2.445 | ns |
| | | $t_h$ | 1.533 | 1.498 | 2.169 | 2.406 | 2.579 | 2.475 | 2.965 | 2.406 | 2.579 | 2.475 | 2.965 | ns |

**Table 1–121.** EP3SE110 Column Pins Input Timing Parameters (Part 3 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -0.961 | -0.937 | -1.361 | -1.508 | -1.636 | -1.573 | -1.938 | -1.508 | -1.636 | -1.573 | -1.938 | ns |
| | | $t_h$ | 1.105 | 1.077 | 1.555 | 1.730 | 1.879 | 1.803 | 2.170 | 1.730 | 1.879 | 1.803 | 2.170 | ns |
| | GCLK PLL | $t_{su}$ | -1.228 | -1.198 | -1.738 | -1.918 | -2.050 | -1.974 | -2.445 | -1.918 | -2.050 | -1.974 | -2.445 | ns |
| | | $t_h$ | 1.533 | 1.498 | 2.169 | 2.406 | 2.579 | 2.475 | 2.965 | 2.406 | 2.579 | 2.475 | 2.965 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -0.950 | -0.926 | -1.350 | -1.497 | -1.617 | -1.554 | -1.919 | -1.497 | -1.617 | -1.554 | -1.919 | ns |
| | | $t_h$ | 1.094 | 1.066 | 1.543 | 1.719 | 1.860 | 1.784 | 2.151 | 1.719 | 1.860 | 1.784 | 2.151 | ns |
| | GCLK PLL | $t_{su}$ | -1.217 | -1.187 | -1.727 | -1.907 | -2.031 | -1.955 | -2.426 | -1.907 | -2.031 | -1.955 | -2.426 | ns |
| | | $t_h$ | 1.522 | 1.487 | 2.157 | 2.395 | 2.560 | 2.456 | 2.946 | 2.395 | 2.560 | 2.456 | 2.946 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.950 | -0.926 | -1.350 | -1.497 | -1.617 | -1.554 | -1.919 | -1.497 | -1.617 | -1.554 | -1.919 | ns |
| | | $t_h$ | 1.094 | 1.066 | 1.543 | 1.719 | 1.860 | 1.784 | 2.151 | 1.719 | 1.860 | 1.784 | 2.151 | ns |
| | GCLK PLL | $t_{su}$ | -1.217 | -1.187 | -1.727 | -1.907 | -2.031 | -1.955 | -2.426 | -1.907 | -2.031 | -1.955 | -2.426 | ns |
| | | $t_h$ | 1.522 | 1.487 | 2.157 | 2.395 | 2.560 | 2.456 | 2.946 | 2.395 | 2.560 | 2.456 | 2.946 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.961 | -0.937 | -1.361 | -1.508 | -1.636 | -1.573 | -1.938 | -1.508 | -1.636 | -1.573 | -1.938 | ns |
| | | $t_h$ | 1.105 | 1.077 | 1.555 | 1.730 | 1.879 | 1.803 | 2.170 | 1.730 | 1.879 | 1.803 | 2.170 | ns |
| | GCLK PLL | $t_{su}$ | -1.228 | -1.198 | -1.738 | -1.918 | -2.050 | -1.974 | -2.445 | -1.918 | -2.050 | -1.974 | -2.445 | ns |
| | | $t_h$ | 1.533 | 1.498 | 2.169 | 2.406 | 2.579 | 2.475 | 2.965 | 2.406 | 2.579 | 2.475 | 2.965 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.961 | -0.937 | -1.361 | -1.508 | -1.636 | -1.573 | -1.938 | -1.508 | -1.636 | -1.573 | -1.938 | ns |
| | | $t_h$ | 1.105 | 1.077 | 1.555 | 1.730 | 1.879 | 1.803 | 2.170 | 1.730 | 1.879 | 1.803 | 2.170 | ns |
| | GCLK PLL | $t_{su}$ | -1.228 | -1.198 | -1.738 | -1.918 | -2.050 | -1.974 | -2.445 | -1.918 | -2.050 | -1.974 | -2.445 | ns |
| | | $t_h$ | 1.533 | 1.498 | 2.169 | 2.406 | 2.579 | 2.475 | 2.965 | 2.406 | 2.579 | 2.475 | 2.965 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.950 | -0.926 | -1.350 | -1.497 | -1.617 | -1.554 | -1.919 | -1.497 | -1.617 | -1.554 | -1.919 | ns |
| | | $t_h$ | 1.094 | 1.066 | 1.543 | 1.719 | 1.860 | 1.784 | 2.151 | 1.719 | 1.860 | 1.784 | 2.151 | ns |
| | GCLK PLL | $t_{su}$ | -1.217 | -1.187 | -1.727 | -1.907 | -2.031 | -1.955 | -2.426 | -1.907 | -2.031 | -1.955 | -2.426 | ns |
| | | $t_h$ | 1.522 | 1.487 | 2.157 | 2.395 | 2.560 | 2.456 | 2.946 | 2.395 | 2.560 | 2.456 | 2.946 | ns |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.950 | -0.926 | -1.350 | -1.497 | -1.617 | -1.554 | -1.919 | -1.497 | -1.617 | -1.554 | -1.919 | ns |
| | | $t_h$ | 1.094 | 1.066 | 1.543 | 1.719 | 1.860 | 1.784 | 2.151 | 1.719 | 1.860 | 1.784 | 2.151 | ns |
| | GCLK PLL | $t_{su}$ | -1.217 | -1.187 | -1.727 | -1.907 | -2.031 | -1.955 | -2.426 | -1.907 | -2.031 | -1.955 | -2.426 | ns |
| | | $t_h$ | 1.522 | 1.487 | 2.157 | 2.395 | 2.560 | 2.456 | 2.946 | 2.395 | 2.560 | 2.456 | 2.946 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.938 | -0.914 | -1.340 | -1.486 | -1.601 | -1.538 | -1.903 | -1.486 | -1.601 | -1.538 | -1.903 | ns |
| | | $t_h$ | 1.082 | 1.054 | 1.533 | 1.708 | 1.844 | 1.768 | 2.135 | 1.708 | 1.844 | 1.768 | 2.135 | ns |
| | GCLK PLL | $t_{su}$ | -1.205 | -1.175 | -1.717 | -1.896 | -2.015 | -1.939 | -2.410 | -1.896 | -2.015 | -1.939 | -2.410 | ns |
| | | $t_h$ | 1.510 | 1.475 | 2.147 | 2.384 | 2.544 | 2.440 | 2.930 | 2.384 | 2.544 | 2.440 | 2.930 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -0.938 | -0.914 | -1.340 | -1.486 | -1.601 | -1.538 | -1.903 | -1.486 | -1.601 | -1.538 | -1.903 | ns |
| | | $t_h$ | 1.082 | 1.054 | 1.533 | 1.708 | 1.844 | 1.768 | 2.135 | 1.708 | 1.844 | 1.768 | 2.135 | ns |
| | GCLK PLL | $t_{su}$ | -1.205 | -1.175 | -1.717 | -1.896 | -2.015 | -1.939 | -2.410 | -1.896 | -2.015 | -1.939 | -2.410 | ns |
| | | $t_h$ | 1.510 | 1.475 | 2.147 | 2.384 | 2.544 | 2.440 | 2.930 | 2.384 | 2.544 | 2.440 | 2.930 | ns |

**Table 1–121.** EP3SE110 Column Pins Input Timing Parameters (Part 4 of 4)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V PCI-X | GCLK | $t_{su}$ | -1.041 | -1.017 | -1.453 | -1.615 | -1.846 | -1.785 | -2.147 | -1.615 | -1.846 | -1.785 | -2.147 | ns |
| | | $t_h$ | 1.183 | 1.155 | 1.647 | 1.840 | 2.092 | 2.016 | 2.384 | 1.840 | 2.092 | 2.016 | 2.384 | ns |
| | GCLK PLL | $t_{su}$ | -1.308 | -1.278 | -1.830 | -2.025 | -2.260 | -2.186 | -2.654 | -2.025 | -2.260 | -2.186 | -2.654 | ns |
| | | $t_h$ | 1.611 | 1.576 | 2.261 | 2.516 | 2.792 | 2.688 | 3.179 | 2.516 | 2.792 | 2.688 | 3.179 | ns |

Table 1–122 lists the EP3SE110 row pins input timing parameters for single-ended I/O standards.

**Table 1–122.** EP3SE110 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -0.917 | -0.960 | -1.364 | -1.476 | -1.736 | -1.642 | -2.026 | -1.488 | -1.737 | -1.683 | -2.064 | ns |
| | | $t_h$ | 1.041 | 1.099 | 1.561 | 1.698 | 1.978 | 1.873 | 2.261 | 1.720 | 1.989 | 1.922 | 2.300 | ns |
| | GCLK PLL | $t_{su}$ | 1.022 | 1.000 | 1.632 | 1.851 | 1.964 | 1.893 | 1.808 | 1.901 | 1.982 | 1.864 | 1.859 | ns |
| | | $t_h$ | -0.762 | -0.722 | -1.218 | -1.386 | -1.449 | -1.406 | -1.309 | -1.426 | -1.456 | -1.368 | -1.357 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -0.917 | -0.960 | -1.364 | -1.476 | -1.736 | -1.642 | -2.026 | -1.488 | -1.737 | -1.683 | -2.064 | ns |
| | | $t_h$ | 1.041 | 1.099 | 1.561 | 1.698 | 1.978 | 1.873 | 2.261 | 1.720 | 1.989 | 1.922 | 2.300 | ns |
| | GCLK PLL | $t_{su}$ | 1.022 | 1.000 | 1.632 | 1.851 | 1.964 | 1.893 | 1.808 | 1.901 | 1.982 | 1.864 | 1.859 | ns |
| | | $t_h$ | -0.762 | -0.722 | -1.218 | -1.386 | -1.449 | -1.406 | -1.309 | -1.426 | -1.456 | -1.368 | -1.357 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -0.923 | -0.971 | -1.361 | -1.477 | -1.739 | -1.645 | -2.029 | -1.487 | -1.742 | -1.688 | -2.069 | ns |
| | | $t_h$ | 1.047 | 1.110 | 1.558 | 1.699 | 1.981 | 1.876 | 2.264 | 1.719 | 1.994 | 1.927 | 2.305 | ns |
| | GCLK PLL | $t_{su}$ | 1.016 | 0.989 | 1.635 | 1.850 | 1.961 | 1.890 | 1.805 | 1.902 | 1.977 | 1.859 | 1.854 | ns |
| | | $t_h$ | -0.756 | -0.711 | -1.221 | -1.385 | -1.446 | -1.403 | -1.306 | -1.427 | -1.451 | -1.363 | -1.352 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -0.923 | -0.971 | -1.361 | -1.477 | -1.739 | -1.645 | -2.029 | -1.487 | -1.742 | -1.688 | -2.069 | ns |
| | | $t_h$ | 1.047 | 1.110 | 1.558 | 1.699 | 1.981 | 1.876 | 2.264 | 1.719 | 1.994 | 1.927 | 2.305 | ns |
| | GCLK PLL | $t_{su}$ | 1.016 | 0.989 | 1.635 | 1.850 | 1.961 | 1.890 | 1.805 | 1.902 | 1.977 | 1.859 | 1.854 | ns |
| | | $t_h$ | -0.756 | -0.711 | -1.221 | -1.385 | -1.446 | -1.403 | -1.306 | -1.427 | -1.451 | -1.363 | -1.352 | ns |
| 2.5 V | GCLK | $t_{su}$ | -0.911 | -0.964 | -1.370 | -1.490 | -1.754 | -1.660 | -2.044 | -1.496 | -1.752 | -1.698 | -2.079 | ns |
| | | $t_h$ | 1.035 | 1.103 | 1.567 | 1.712 | 1.996 | 1.891 | 2.279 | 1.728 | 2.004 | 1.937 | 2.315 | ns |
| | GCLK PLL | $t_{su}$ | 1.028 | 0.996 | 1.626 | 1.837 | 1.946 | 1.875 | 1.790 | 1.893 | 1.967 | 1.849 | 1.844 | ns |
| | | $t_h$ | -0.768 | -0.718 | -1.212 | -1.372 | -1.431 | -1.388 | -1.291 | -1.418 | -1.441 | -1.353 | -1.342 | ns |
| 1.8 V | GCLK | $t_{su}$ | -0.987 | -1.042 | -1.456 | -1.570 | -1.756 | -1.705 | -2.042 | -1.576 | -1.754 | -1.707 | -2.080 | ns |
| | | $t_h$ | 1.112 | 1.182 | 1.653 | 1.793 | 1.999 | 1.936 | 2.277 | 1.808 | 2.007 | 1.948 | 2.316 | ns |
| | GCLK PLL | $t_{su}$ | 1.040 | 1.054 | 1.703 | 1.929 | 1.948 | 1.963 | 1.900 | 1.946 | 1.966 | 1.848 | 1.952 | ns |
| | | $t_h$ | -0.777 | -0.773 | -1.286 | -1.461 | -1.433 | -1.472 | -1.399 | -1.468 | -1.440 | -1.352 | -1.447 | ns |


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**Table 1–122.** EP3SE110 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5 V | GCLK | $t_{su}$ | -0.977 | -1.031 | -1.432 | -1.538 | -1.688 | -1.637 | -1.974 | -1.545 | -1.689 | -1.642 | -2.015 | ns |
| | | $t_h$ | 1.102 | 1.171 | 1.629 | 1.761 | 1.931 | 1.868 | 2.209 | 1.777 | 1.942 | 1.883 | 2.251 | ns |
| | GCLK PLL | $t_{su}$ | 1.050 | 1.065 | 1.727 | 1.961 | 2.016 | 2.031 | 1.968 | 1.977 | 2.031 | 1.913 | 2.017 | ns |
| | | $t_h$ | -0.787 | -0.784 | -1.310 | -1.493 | -1.501 | -1.540 | -1.467 | -1.499 | -1.505 | -1.417 | -1.512 | ns |
| 1.2 V | GCLK | $t_{su}$ | -0.917 | -0.978 | -1.353 | -1.437 | -1.529 | -1.478 | -1.815 | -1.449 | -1.534 | -1.487 | -1.860 | ns |
| | | $t_h$ | 1.042 | 1.118 | 1.550 | 1.660 | 1.772 | 1.709 | 2.050 | 1.681 | 1.787 | 1.728 | 2.096 | ns |
| | GCLK PLL | $t_{su}$ | 1.110 | 1.118 | 1.806 | 2.062 | 2.175 | 2.190 | 2.127 | 2.073 | 2.186 | 2.068 | 2.172 | ns |
| | | $t_h$ | -0.847 | -0.837 | -1.389 | -1.594 | -1.660 | -1.699 | -1.626 | -1.595 | -1.660 | -1.572 | -1.667 | ns |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -0.854 | -0.906 | -1.284 | -1.381 | -1.534 | -1.440 | -1.824 | -1.384 | -1.535 | -1.481 | -1.862 | ns |
| | | $t_h$ | 0.979 | 1.046 | 1.481 | 1.603 | 1.776 | 1.671 | 2.059 | 1.616 | 1.787 | 1.720 | 2.098 | ns |
| | GCLK PLL | $t_{su}$ | 1.085 | 1.054 | 1.712 | 1.946 | 2.166 | 2.095 | 2.010 | 2.005 | 2.184 | 2.066 | 2.061 | ns |
| | | $t_h$ | -0.824 | -0.775 | -1.298 | -1.481 | -1.651 | -1.608 | -1.511 | -1.530 | -1.658 | -1.570 | -1.559 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -0.854 | -0.906 | -1.284 | -1.381 | -1.534 | -1.440 | -1.824 | -1.384 | -1.535 | -1.481 | -1.862 | ns |
| | | $t_h$ | 0.979 | 1.046 | 1.481 | 1.603 | 1.776 | 1.671 | 2.059 | 1.616 | 1.787 | 1.720 | 2.098 | ns |
| | GCLK PLL | $t_{su}$ | 1.085 | 1.054 | 1.712 | 1.946 | 2.166 | 2.095 | 2.010 | 2.005 | 2.184 | 2.066 | 2.061 | ns |
| | | $t_h$ | -0.824 | -0.775 | -1.298 | -1.481 | -1.651 | -1.608 | -1.511 | -1.530 | -1.658 | -1.570 | -1.559 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -0.891 | -0.943 | -1.315 | -1.410 | -1.524 | -1.472 | -1.811 | -1.417 | -1.530 | -1.479 | -1.853 | ns |
| | | $t_h$ | 1.016 | 1.083 | 1.512 | 1.631 | 1.765 | 1.702 | 2.042 | 1.647 | 1.778 | 1.719 | 2.085 | ns |
| | GCLK PLL | $t_{su}$ | 1.136 | 1.153 | 1.844 | 2.087 | 2.180 | 2.193 | 2.129 | 2.102 | 2.193 | 2.076 | 2.177 | ns |
| | | $t_h$ | -0.873 | -0.872 | -1.427 | -1.621 | -1.667 | -1.704 | -1.632 | -1.627 | -1.670 | -1.581 | -1.676 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -0.891 | -0.943 | -1.315 | -1.410 | -1.524 | -1.472 | -1.811 | -1.417 | -1.530 | -1.479 | -1.853 | ns |
| | | $t_h$ | 1.016 | 1.083 | 1.512 | 1.631 | 1.765 | 1.702 | 2.042 | 1.647 | 1.778 | 1.719 | 2.085 | ns |
| | GCLK PLL | $t_{su}$ | 1.136 | 1.153 | 1.844 | 2.087 | 2.180 | 2.193 | 2.129 | 2.102 | 2.193 | 2.076 | 2.177 | ns |
| | | $t_h$ | -0.873 | -0.872 | -1.427 | -1.621 | -1.667 | -1.704 | -1.632 | -1.627 | -1.670 | -1.581 | -1.676 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -0.877 | -0.931 | -1.300 | -1.400 | -1.506 | -1.454 | -1.793 | -1.406 | -1.513 | -1.462 | -1.836 | ns |
| | | $t_h$ | 1.002 | 1.071 | 1.498 | 1.621 | 1.747 | 1.684 | 2.024 | 1.636 | 1.761 | 1.702 | 2.068 | ns |
| | GCLK PLL | $t_{su}$ | 1.150 | 1.165 | 1.857 | 2.097 | 2.198 | 2.211 | 2.147 | 2.113 | 2.210 | 2.093 | 2.194 | ns |
| | | $t_h$ | -0.887 | -0.884 | -1.439 | -1.631 | -1.685 | -1.722 | -1.650 | -1.638 | -1.687 | -1.598 | -1.693 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.891 | -0.943 | -1.315 | -1.410 | -1.524 | -1.472 | -1.811 | -1.417 | -1.530 | -1.479 | -1.853 | ns |
| | | $t_h$ | 1.016 | 1.083 | 1.512 | 1.631 | 1.765 | 1.702 | 2.042 | 1.647 | 1.778 | 1.719 | 2.085 | ns |
| | GCLK PLL | $t_{su}$ | 1.136 | 1.153 | 1.844 | 2.087 | 2.180 | 2.193 | 2.129 | 2.102 | 2.193 | 2.076 | 2.177 | ns |
| | | $t_h$ | -0.873 | -0.872 | -1.427 | -1.621 | -1.667 | -1.704 | -1.632 | -1.627 | -1.670 | -1.581 | -1.676 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.891 | -0.943 | -1.315 | -1.410 | -1.524 | -1.472 | -1.811 | -1.417 | -1.530 | -1.479 | -1.853 | ns |
| | | $t_h$ | 1.016 | 1.083 | 1.512 | 1.631 | 1.765 | 1.702 | 2.042 | 1.647 | 1.778 | 1.719 | 2.085 | ns |
| | GCLK PLL | $t_{su}$ | 1.136 | 1.153 | 1.844 | 2.087 | 2.180 | 2.193 | 2.129 | 2.102 | 2.193 | 2.076 | 2.177 | ns |
| | | $t_h$ | -0.873 | -0.872 | -1.427 | -1.621 | -1.667 | -1.704 | -1.632 | -1.627 | -1.670 | -1.581 | -1.676 | ns |

**Table 1–122.** EP3SE110 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.877 | -0.931 | -1.300 | -1.400 | -1.506 | -1.454 | -1.793 | -1.406 | -1.513 | -1.462 | -1.836 | ns |
| | | $t_h$ | 1.002 | 1.071 | 1.498 | 1.621 | 1.747 | 1.684 | 2.024 | 1.636 | 1.761 | 1.702 | 2.068 | ns |
| | GCLK PLL | $t_{su}$ | 1.150 | 1.165 | 1.857 | 2.097 | 2.198 | 2.211 | 2.147 | 2.113 | 2.210 | 2.093 | 2.194 | ns |
| | | $t_h$ | -0.887 | -0.884 | -1.439 | -1.631 | -1.685 | -1.722 | -1.650 | -1.638 | -1.687 | -1.598 | -1.693 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.877 | -0.931 | -1.300 | -1.400 | -1.506 | -1.454 | -1.793 | -1.406 | -1.513 | -1.462 | -1.836 | ns |
| | | $t_h$ | 1.002 | 1.071 | 1.498 | 1.621 | 1.747 | 1.684 | 2.024 | 1.636 | 1.761 | 1.702 | 2.068 | ns |
| | GCLK PLL | $t_{su}$ | 1.150 | 1.165 | 1.857 | 2.097 | 2.198 | 2.211 | 2.147 | 2.113 | 2.210 | 2.093 | 2.194 | ns |
| | | $t_h$ | -0.887 | -0.884 | -1.439 | -1.631 | -1.685 | -1.722 | -1.650 | -1.638 | -1.687 | -1.598 | -1.693 | ns |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.868 | -0.919 | -1.291 | -1.390 | -1.490 | -1.438 | -1.777 | -1.397 | -1.497 | -1.446 | -1.820 | ns |
| | | $t_h$ | 0.993 | 1.059 | 1.489 | 1.611 | 1.731 | 1.668 | 2.008 | 1.627 | 1.745 | 1.686 | 2.052 | ns |
| | GCLK PLL | $t_{su}$ | 1.159 | 1.177 | 1.866 | 2.107 | 2.214 | 2.227 | 2.163 | 2.122 | 2.226 | 2.109 | 2.210 | ns |
| | | $t_h$ | -0.896 | -0.896 | -1.448 | -1.641 | -1.701 | -1.738 | -1.666 | -1.647 | -1.703 | -1.614 | -1.709 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.868 | -0.919 | -1.291 | -1.390 | -1.490 | -1.438 | -1.777 | -1.397 | -1.497 | -1.446 | -1.820 | ns |
| | | $t_h$ | 0.993 | 1.059 | 1.489 | 1.611 | 1.731 | 1.668 | 2.008 | 1.627 | 1.745 | 1.686 | 2.052 | ns |
| | GCLK PLL | $t_{su}$ | 1.159 | 1.177 | 1.866 | 2.107 | 2.214 | 2.227 | 2.163 | 2.122 | 2.226 | 2.109 | 2.210 | ns |
| | | $t_h$ | -0.896 | -0.896 | -1.448 | -1.641 | -1.701 | -1.738 | -1.666 | -1.647 | -1.703 | -1.614 | -1.709 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -0.923 | -0.971 | -1.361 | -1.477 | -1.739 | -1.645 | -2.029 | -1.487 | -1.742 | -1.688 | -2.069 | ns |
| | | $t_h$ | 1.047 | 1.110 | 1.558 | 1.699 | 1.981 | 1.876 | 2.264 | 1.719 | 1.994 | 1.927 | 2.305 | ns |
| | GCLK PLL | $t_{su}$ | 1.016 | 0.989 | 1.635 | 1.850 | 1.961 | 1.890 | 1.805 | 1.902 | 1.977 | 1.859 | 1.854 | ns |
| | | $t_h$ | -0.756 | -0.711 | -1.221 | -1.385 | -1.446 | -1.403 | -1.306 | -1.427 | -1.451 | -1.363 | -1.352 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | -0.923 | -0.971 | -1.361 | -1.477 | -1.739 | -1.645 | -2.029 | -1.487 | -1.742 | -1.688 | -2.069 | ns |
| | | $t_h$ | 1.047 | 1.110 | 1.558 | 1.699 | 1.981 | 1.876 | 2.264 | 1.719 | 1.994 | 1.927 | 2.305 | ns |
| | GCLK PLL | $t_{su}$ | 1.016 | 0.989 | 1.635 | 1.850 | 1.961 | 1.890 | 1.805 | 1.902 | 1.977 | 1.859 | 1.854 | ns |
| | | $t_h$ | -0.756 | -0.711 | -1.221 | -1.385 | -1.446 | -1.403 | -1.306 | -1.427 | -1.451 | -1.363 | -1.352 | ns |

Table 1–123 lists the EP3SE110 column pins output timing parameters for single-ended I/O standards.

**Table 1–123.** EP3SE110 Column Pins Output Timing Parameters (Part 1 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | UnitS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.489 | 3.489 | 4.830 | 5.213 | 5.686 | 5.551 | 5.863 | 5.213 | 5.686 | 5.551 | 5.863 | ns |
| | | GCLK PLL | $t_{co}$ | 3.868 | 3.881 | 5.415 | 5.837 | 6.442 | 6.278 | 6.680 | 5.837 | 6.442 | 6.278 | 6.680 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.422 | 3.422 | 4.721 | 5.102 | 5.573 | 5.438 | 5.750 | 5.102 | 5.573 | 5.438 | 5.750 | ns |
| | | GCLK PLL | $t_{co}$ | 3.801 | 3.814 | 5.306 | 5.726 | 6.329 | 6.165 | 6.567 | 5.726 | 6.329 | 6.165 | 6.567 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.336 | 3.336 | 4.617 | 5.003 | 5.481 | 5.346 | 5.658 | 5.003 | 5.481 | 5.346 | 5.658 | ns |
| | | GCLK PLL | $t_{co}$ | 3.715 | 3.728 | 5.203 | 5.628 | 6.237 | 6.073 | 6.475 | 5.628 | 6.237 | 6.073 | 6.475 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.329 | 3.329 | 4.600 | 4.975 | 5.440 | 5.305 | 5.617 | 4.975 | 5.440 | 5.305 | 5.617 | ns |
| | | GCLK PLL | $t_{co}$ | 3.709 | 3.721 | 5.186 | 5.600 | 6.196 | 6.032 | 6.434 | 5.600 | 6.196 | 6.032 | 6.434 | ns |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.495 | 3.495 | 4.834 | 5.218 | 5.693 | 5.558 | 5.870 | 5.218 | 5.693 | 5.558 | 5.870 | ns |
| | | GCLK PLL | $t_{co}$ | 3.874 | 3.887 | 5.420 | 5.842 | 6.449 | 6.285 | 6.687 | 5.842 | 6.449 | 6.285 | 6.687 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.340 | 3.340 | 4.627 | 5.020 | 5.492 | 5.357 | 5.669 | 5.020 | 5.492 | 5.357 | 5.669 | ns |
| | | GCLK PLL | $t_{co}$ | 3.719 | 3.732 | 5.213 | 5.645 | 6.248 | 6.084 | 6.486 | 5.645 | 6.248 | 6.084 | 6.486 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.347 | 3.347 | 4.621 | 4.999 | 5.466 | 5.331 | 5.643 | 4.999 | 5.466 | 5.331 | 5.643 | ns |
| | | GCLK PLL | $t_{co}$ | 3.726 | 3.739 | 5.207 | 5.624 | 6.222 | 6.058 | 6.460 | 5.624 | 6.222 | 6.058 | 6.460 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.331 | 3.331 | 4.599 | 4.974 | 5.437 | 5.302 | 5.614 | 4.974 | 5.437 | 5.302 | 5.614 | ns |
| | | GCLK PLL | $t_{co}$ | 3.710 | 3.723 | 5.184 | 5.599 | 6.193 | 6.029 | 6.431 | 5.599 | 6.193 | 6.029 | 6.431 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.453 | 3.453 | 4.797 | 5.181 | 5.653 | 5.518 | 5.830 | 5.181 | 5.653 | 5.518 | 5.830 | ns |
| | | GCLK PLL | $t_{co}$ | 3.831 | 3.845 | 5.382 | 5.805 | 6.409 | 6.245 | 6.647 | 5.805 | 6.409 | 6.245 | 6.647 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.342 | 3.342 | 4.667 | 5.047 | 5.515 | 5.381 | 5.691 | 5.047 | 5.515 | 5.381 | 5.691 | ns |
| | | GCLK PLL | $t_{co}$ | 3.724 | 3.734 | 5.252 | 5.674 | 6.272 | 6.109 | 6.509 | 5.674 | 6.272 | 6.109 | 6.509 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.306 | 3.306 | 4.604 | 4.978 | 5.441 | 5.307 | 5.618 | 4.978 | 5.441 | 5.307 | 5.618 | ns |
| | | GCLK PLL | $t_{co}$ | 3.686 | 3.698 | 5.189 | 5.602 | 6.198 | 6.035 | 6.435 | 5.602 | 6.198 | 6.035 | 6.435 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.288 | 3.288 | 4.575 | 4.950 | 5.413 | 5.278 | 5.590 | 4.950 | 5.413 | 5.278 | 5.590 | ns |
| | | GCLK PLL | $t_{co}$ | 3.667 | 3.680 | 5.160 | 5.575 | 6.169 | 6.005 | 6.407 | 5.575 | 6.169 | 6.005 | 6.407 | ns |

**Table 1–123.** EP3SE110 Column Pins Output Timing Parameters (Part 2 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | UnitS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.367 | 3.367 | 4.701 | 5.081 | 5.550 | 5.416 | 5.726 | 5.081 | 5.550 | 5.416 | 5.726 | ns |
| | | GCLK PLL | $t_{co}$ | 3.748 | 3.759 | 5.286 | 5.707 | 6.307 | 6.144 | 6.544 | 5.707 | 6.307 | 6.144 | 6.544 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.288 | 3.288 | 4.577 | 4.952 | 5.415 | 5.281 | 5.591 | 4.952 | 5.415 | 5.281 | 5.591 | ns |
| | | GCLK PLL | $t_{co}$ | 3.669 | 3.680 | 5.163 | 5.577 | 6.172 | 6.009 | 6.413 | 5.577 | 6.172 | 6.009 | 6.413 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.283 | 3.283 | 4.570 | 4.945 | 5.407 | 5.272 | 5.584 | 4.945 | 5.407 | 5.272 | 5.584 | ns |
| | | GCLK PLL | $t_{co}$ | 3.662 | 3.675 | 5.155 | 5.570 | 6.163 | 5.999 | 6.401 | 5.570 | 6.163 | 5.999 | 6.401 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.274 | 3.274 | 4.556 | 4.930 | 5.392 | 5.257 | 5.569 | 4.930 | 5.392 | 5.257 | 5.569 | ns |
| | | GCLK PLL | $t_{co}$ | 3.653 | 3.666 | 5.141 | 5.554 | 6.148 | 5.984 | 6.387 | 5.554 | 6.148 | 5.984 | 6.387 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.489 | 3.489 | 4.908 | 5.308 | 5.797 | 5.663 | 5.974 | 5.308 | 5.797 | 5.663 | 5.974 | ns |
| | | GCLK PLL | $t_{co}$ | 3.868 | 3.881 | 5.493 | 5.932 | 6.554 | 6.391 | 6.791 | 5.932 | 6.554 | 6.391 | 6.791 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.389 | 3.389 | 4.789 | 5.182 | 5.665 | 5.531 | 5.841 | 5.182 | 5.665 | 5.531 | 5.841 | ns |
| | | GCLK PLL | $t_{co}$ | 3.771 | 3.781 | 5.374 | 5.807 | 6.422 | 6.259 | 6.659 | 5.807 | 6.422 | 6.259 | 6.659 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.345 | 3.345 | 4.702 | 5.091 | 5.570 | 5.435 | 5.747 | 5.091 | 5.570 | 5.435 | 5.747 | ns |
| | | GCLK PLL | $t_{co}$ | 3.726 | 3.737 | 5.287 | 5.716 | 6.326 | 6.162 | 6.564 | 5.716 | 6.326 | 6.162 | 6.564 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.307 | 3.307 | 4.663 | 5.049 | 5.527 | 5.392 | 5.704 | 5.049 | 5.527 | 5.392 | 5.704 | ns |
| | | GCLK PLL | $t_{co}$ | 3.687 | 3.699 | 5.248 | 5.674 | 6.283 | 6.119 | 6.521 | 5.674 | 6.283 | 6.119 | 6.521 | ns |

**Table 1–123.** EP3SE110 Column Pins Output Timing Parameters (Part 3 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | UnitS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.680 | 3.680 | 5.229 | 5.668 | 6.202 | 6.067 | 6.379 | 5.668 | 6.202 | 6.067 | 6.379 | ns |
| | | GCLK PLL | $t_{co}$ | 4.059 | 4.072 | 5.815 | 6.291 | 6.958 | 6.794 | 7.196 | 6.291 | 6.958 | 6.794 | 7.196 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.499 | 3.499 | 4.950 | 5.359 | 5.854 | 5.720 | 6.030 | 5.359 | 5.854 | 5.720 | 6.030 | ns |
| | | GCLK PLL | $t_{co}$ | 3.881 | 3.891 | 5.536 | 5.984 | 6.611 | 6.448 | 6.848 | 5.984 | 6.611 | 6.448 | 6.848 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.417 | 3.417 | 4.843 | 5.244 | 5.744 | 5.609 | 5.921 | 5.244 | 5.744 | 5.609 | 5.921 | ns |
| | | GCLK PLL | $t_{co}$ | 3.796 | 3.809 | 5.429 | 5.868 | 6.500 | 6.336 | 6.738 | 5.868 | 6.500 | 6.336 | 6.738 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.397 | 3.397 | 4.785 | 5.190 | 5.678 | 5.543 | 5.855 | 5.190 | 5.678 | 5.543 | 5.855 | ns |
| | | GCLK PLL | $t_{co}$ | 3.776 | 3.789 | 5.370 | 5.814 | 6.434 | 6.270 | 6.672 | 5.814 | 6.434 | 6.270 | 6.672 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.334 | 3.334 | 4.724 | 5.115 | 5.597 | 5.462 | 5.774 | 5.115 | 5.597 | 5.462 | 5.774 | ns |
| | | GCLK PLL | $t_{co}$ | 3.713 | 3.726 | 5.309 | 5.740 | 6.353 | 6.189 | 6.591 | 5.740 | 6.353 | 6.189 | 6.591 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.316 | 3.316 | 4.703 | 5.094 | 5.574 | 5.439 | 5.751 | 5.094 | 5.574 | 5.439 | 5.751 | ns |
| | | GCLK PLL | $t_{co}$ | 3.696 | 3.708 | 5.289 | 5.719 | 6.330 | 6.166 | 6.568 | 5.719 | 6.330 | 6.166 | 6.568 | ns |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.626 | 3.626 | 5.158 | 5.600 | 6.140 | 6.005 | 6.317 | 5.600 | 6.140 | 6.005 | 6.317 | ns |
| | | GCLK PLL | $t_{co}$ | 4.005 | 4.018 | 5.743 | 6.224 | 6.896 | 6.732 | 7.134 | 6.224 | 6.896 | 6.732 | 7.134 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.414 | 3.414 | 4.839 | 5.244 | 5.748 | 5.613 | 5.925 | 5.244 | 5.748 | 5.613 | 5.925 | ns |
| | | GCLK PLL | $t_{co}$ | 3.793 | 3.806 | 5.424 | 5.867 | 6.504 | 6.340 | 6.742 | 5.867 | 6.504 | 6.340 | 6.742 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.389 | 3.389 | 4.772 | 5.184 | 5.681 | 5.546 | 5.858 | 5.184 | 5.681 | 5.546 | 5.858 | ns |
| | | GCLK PLL | $t_{co}$ | 3.769 | 3.781 | 5.357 | 5.809 | 6.437 | 6.273 | 6.675 | 5.809 | 6.437 | 6.273 | 6.675 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.378 | 3.378 | 4.755 | 5.159 | 5.661 | 5.526 | 5.838 | 5.159 | 5.661 | 5.526 | 5.838 | ns |
| | | GCLK PLL | $t_{co}$ | 3.757 | 3.770 | 5.340 | 5.784 | 6.417 | 6.253 | 6.655 | 5.784 | 6.417 | 6.253 | 6.655 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.323 | 3.323 | 4.717 | 5.108 | 5.591 | 5.456 | 5.768 | 5.108 | 5.591 | 5.456 | 5.768 | ns |
| | | GCLK PLL | $t_{co}$ | 3.702 | 3.715 | 5.302 | 5.733 | 6.347 | 6.183 | 6.585 | 5.733 | 6.347 | 6.183 | 6.585 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.318 | 3.318 | 4.700 | 5.097 | 5.580 | 5.445 | 5.757 | 5.097 | 5.580 | 5.445 | 5.757 | ns |
| | | GCLK PLL | $t_{co}$ | 3.696 | 3.710 | 5.286 | 5.720 | 6.336 | 6.172 | 6.574 | 5.720 | 6.336 | 6.172 | 6.574 | ns |

**Table 1–123.** EP3SE110 Column Pins Output Timing Parameters (Part 4 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | UnitS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.542 | 3.542 | 5.084 | 5.536 | 6.084 | 5.949 | 6.261 | 5.536 | 6.084 | 5.949 | 6.261 | ns |
| | | GCLK PLL | $t_{co}$ | 3.921 | 3.934 | 5.669 | 6.159 | 6.840 | 6.676 | 7.078 | 6.159 | 6.840 | 6.676 | 7.078 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.419 | 3.419 | 4.858 | 5.274 | 5.798 | 5.663 | 5.975 | 5.274 | 5.798 | 5.663 | 5.975 | ns |
| | | GCLK PLL | $t_{co}$ | 3.799 | 3.811 | 5.444 | 5.899 | 6.554 | 6.390 | 6.792 | 5.899 | 6.554 | 6.390 | 6.792 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.381 | 3.381 | 4.766 | 5.185 | 5.685 | 5.550 | 5.862 | 5.185 | 5.685 | 5.550 | 5.862 | ns |
| | | GCLK PLL | $t_{co}$ | 3.761 | 3.773 | 5.351 | 5.809 | 6.441 | 6.277 | 6.679 | 5.809 | 6.441 | 6.277 | 6.679 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.334 | 3.334 | 4.738 | 5.136 | 5.629 | 5.494 | 5.806 | 5.136 | 5.629 | 5.494 | 5.806 | ns |
| | | GCLK PLL | $t_{co}$ | 3.712 | 3.726 | 5.323 | 5.759 | 6.385 | 6.221 | 6.623 | 5.759 | 6.385 | 6.221 | 6.623 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.334 | 3.334 | 4.695 | 5.083 | 5.560 | 5.425 | 5.737 | 5.083 | 5.560 | 5.425 | 5.737 | ns |
| | | GCLK PLL | $t_{co}$ | 3.713 | 3.726 | 5.280 | 5.706 | 6.316 | 6.152 | 6.554 | 5.706 | 6.316 | 6.152 | 6.554 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.331 | 3.331 | 4.692 | 5.080 | 5.556 | 5.421 | 5.733 | 5.080 | 5.556 | 5.421 | 5.733 | ns |
| | | GCLK PLL | $t_{co}$ | 3.710 | 3.723 | 5.277 | 5.702 | 6.312 | 6.148 | 6.550 | 5.702 | 6.312 | 6.148 | 6.550 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.329 | 3.329 | 4.692 | 5.081 | 5.557 | 5.422 | 5.734 | 5.081 | 5.557 | 5.422 | 5.734 | ns |
| | | GCLK PLL | $t_{co}$ | 3.709 | 3.721 | 5.277 | 5.703 | 6.313 | 6.149 | 6.551 | 5.703 | 6.313 | 6.149 | 6.551 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.320 | 3.320 | 4.677 | 5.065 | 5.542 | 5.407 | 5.719 | 5.065 | 5.542 | 5.407 | 5.719 | ns |
| | | GCLK PLL | $t_{co}$ | 3.700 | 3.712 | 5.263 | 5.689 | 6.298 | 6.134 | 6.536 | 5.689 | 6.298 | 6.134 | 6.536 | ns |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.341 | 3.341 | 4.707 | 5.097 | 5.576 | 5.441 | 5.753 | 5.097 | 5.576 | 5.441 | 5.753 | ns |
| | | GCLK PLL | $t_{co}$ | 3.720 | 3.733 | 5.292 | 5.720 | 6.332 | 6.168 | 6.570 | 5.720 | 6.332 | 6.168 | 6.570 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.337 | 3.337 | 4.705 | 5.095 | 5.574 | 5.439 | 5.751 | 5.095 | 5.574 | 5.439 | 5.751 | ns |
| | | GCLK PLL | $t_{co}$ | 3.716 | 3.729 | 5.290 | 5.718 | 6.330 | 6.166 | 6.568 | 5.718 | 6.330 | 6.166 | 6.568 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.326 | 3.326 | 4.695 | 5.086 | 5.565 | 5.430 | 5.742 | 5.086 | 5.565 | 5.430 | 5.742 | ns |
| | | GCLK PLL | $t_{co}$ | 3.706 | 3.718 | 5.280 | 5.709 | 6.321 | 6.157 | 6.559 | 5.709 | 6.321 | 6.157 | 6.559 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.315 | 3.315 | 4.682 | 5.073 | 5.552 | 5.417 | 5.729 | 5.073 | 5.552 | 5.417 | 5.729 | ns |
| | | GCLK PLL | $t_{co}$ | 3.694 | 3.707 | 5.268 | 5.696 | 6.308 | 6.144 | 6.546 | 5.696 | 6.308 | 6.144 | 6.546 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.315 | 3.315 | 4.682 | 5.073 | 5.552 | 5.417 | 5.729 | 5.073 | 5.552 | 5.417 | 5.729 | ns |
| | | GCLK PLL | $t_{co}$ | 3.694 | 3.707 | 5.267 | 5.696 | 6.308 | 6.144 | 6.546 | 5.696 | 6.308 | 6.144 | 6.546 | ns |

**Table 1–123.** EP3SE110 Column Pins Output Timing Parameters (Part 5 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | UnitS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.321 | 3.321 | 4.681 | 5.070 | 5.547 | 5.412 | 5.724 | 5.070 | 5.547 | 5.412 | 5.724 | ns |
| | | GCLK PLL | $t_{co}$ | 3.701 | 3.713 | 5.266 | 5.693 | 6.303 | 6.139 | 6.541 | 5.693 | 6.303 | 6.139 | 6.541 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.324 | 3.324 | 4.689 | 5.079 | 5.559 | 5.424 | 5.736 | 5.079 | 5.559 | 5.424 | 5.736 | ns |
| | | GCLK PLL | $t_{co}$ | 3.703 | 3.716 | 5.274 | 5.702 | 6.315 | 6.151 | 6.553 | 5.702 | 6.315 | 6.151 | 6.553 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.345 | 3.345 | 4.716 | 5.109 | 5.589 | 5.454 | 5.766 | 5.109 | 5.589 | 5.454 | 5.766 | ns |
| | | GCLK PLL | $t_{co}$ | 3.723 | 3.737 | 5.302 | 5.731 | 6.345 | 6.181 | 6.583 | 5.731 | 6.345 | 6.181 | 6.583 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.331 | 3.331 | 4.706 | 5.099 | 5.580 | 5.445 | 5.757 | 5.099 | 5.580 | 5.445 | 5.757 | ns |
| | | GCLK PLL | $t_{co}$ | 3.711 | 3.723 | 5.291 | 5.722 | 6.336 | 6.172 | 6.574 | 5.722 | 6.336 | 6.172 | 6.574 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.320 | 3.320 | 4.692 | 5.085 | 5.566 | 5.431 | 5.743 | 5.085 | 5.566 | 5.431 | 5.743 | ns |
| | | GCLK PLL | $t_{co}$ | 3.699 | 3.712 | 5.278 | 5.708 | 6.322 | 6.158 | 6.560 | 5.708 | 6.322 | 6.158 | 6.560 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.319 | 3.319 | 4.695 | 5.088 | 5.570 | 5.435 | 5.747 | 5.088 | 5.570 | 5.435 | 5.747 | ns |
| | | GCLK PLL | $t_{co}$ | 3.698 | 3.711 | 5.281 | 5.711 | 6.326 | 6.162 | 6.564 | 5.711 | 6.326 | 6.162 | 6.564 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.316 | 3.316 | 4.690 | 5.083 | 5.564 | 5.429 | 5.741 | 5.083 | 5.564 | 5.429 | 5.741 | ns |
| | | GCLK PLL | $t_{co}$ | 3.695 | 3.708 | 5.275 | 5.705 | 6.320 | 6.156 | 6.558 | 5.705 | 6.320 | 6.156 | 6.558 | ns |
| SSTL-15 CLASS II | 8mA | GCLK | $t_{co}$ | 3.318 | 3.318 | 4.679 | 5.069 | 5.547 | 5.412 | 5.724 | 5.069 | 5.547 | 5.412 | 5.724 | ns |
| | | GCLK PLL | $t_{co}$ | 3.697 | 3.710 | 5.264 | 5.692 | 6.303 | 6.139 | 6.541 | 5.692 | 6.303 | 6.139 | 6.541 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.321 | 3.321 | 4.686 | 5.078 | 5.558 | 5.423 | 5.735 | 5.078 | 5.558 | 5.423 | 5.735 | ns |
| | | GCLK PLL | $t_{co}$ | 3.700 | 3.713 | 5.271 | 5.700 | 6.314 | 6.150 | 6.552 | 5.700 | 6.314 | 6.150 | 6.552 | ns |

**Table 1–123.** EP3SE110 Column Pins Output Timing Parameters (Part 6 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | UnitS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.328 | 3.328 | 4.681 | 5.069 | 5.545 | 5.410 | 5.722 | 5.069 | 5.545 | 5.410 | 5.722 | ns |
| | | GCLK PLL | $t_{co}$ | 3.707 | 3.720 | 5.266 | 5.691 | 6.301 | 6.137 | 6.539 | 5.691 | 6.301 | 6.137 | 6.539 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.321 | 3.321 | 4.679 | 5.067 | 5.544 | 5.409 | 5.721 | 5.067 | 5.544 | 5.409 | 5.721 | ns |
| | | GCLK PLL | $t_{co}$ | 3.701 | 3.713 | 5.264 | 5.691 | 6.300 | 6.136 | 6.538 | 5.691 | 6.300 | 6.136 | 6.538 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.313 | 3.313 | 4.671 | 5.060 | 5.537 | 5.402 | 5.714 | 5.060 | 5.537 | 5.402 | 5.714 | ns |
| | | GCLK PLL | $t_{co}$ | 3.693 | 3.705 | 5.257 | 5.683 | 6.293 | 6.129 | 6.531 | 5.683 | 6.293 | 6.129 | 6.531 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.316 | 3.316 | 4.674 | 5.063 | 5.541 | 5.406 | 5.718 | 5.063 | 5.541 | 5.406 | 5.718 | ns |
| | | GCLK PLL | $t_{co}$ | 3.695 | 3.708 | 5.260 | 5.686 | 6.297 | 6.133 | 6.535 | 5.686 | 6.297 | 6.133 | 6.535 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.313 | 3.313 | 4.677 | 5.067 | 5.545 | 5.410 | 5.722 | 5.067 | 5.545 | 5.410 | 5.722 | ns |
| | | GCLK PLL | $t_{co}$ | 3.692 | 3.705 | 5.262 | 5.689 | 6.301 | 6.137 | 6.539 | 5.689 | 6.301 | 6.137 | 6.539 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.321 | 3.321 | 4.676 | 5.064 | 5.541 | 5.406 | 5.718 | 5.064 | 5.541 | 5.406 | 5.718 | ns |
| | | GCLK PLL | $t_{co}$ | 3.700 | 3.713 | 5.261 | 5.687 | 6.297 | 6.133 | 6.535 | 5.687 | 6.297 | 6.133 | 6.535 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.333 | 3.333 | 4.689 | 5.079 | 5.556 | 5.421 | 5.733 | 5.079 | 5.556 | 5.421 | 5.733 | ns |
| | | GCLK PLL | $t_{co}$ | 3.712 | 3.725 | 5.275 | 5.701 | 6.312 | 6.148 | 6.550 | 5.701 | 6.312 | 6.148 | 6.550 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.329 | 3.329 | 4.690 | 5.080 | 5.559 | 5.424 | 5.736 | 5.080 | 5.559 | 5.424 | 5.736 | ns |
| | | GCLK PLL | $t_{co}$ | 3.708 | 3.721 | 5.276 | 5.704 | 6.315 | 6.151 | 6.553 | 5.704 | 6.315 | 6.151 | 6.553 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.325 | 3.325 | 4.686 | 5.076 | 5.554 | 5.419 | 5.731 | 5.076 | 5.554 | 5.419 | 5.731 | ns |
| | | GCLK PLL | $t_{co}$ | 3.704 | 3.717 | 5.271 | 5.699 | 6.310 | 6.146 | 6.548 | 5.699 | 6.310 | 6.146 | 6.548 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.318 | 3.318 | 4.679 | 5.069 | 5.547 | 5.412 | 5.724 | 5.069 | 5.547 | 5.412 | 5.724 | ns |
| | | GCLK PLL | $t_{co}$ | 3.697 | 3.710 | 5.264 | 5.692 | 6.303 | 6.139 | 6.541 | 5.692 | 6.303 | 6.139 | 6.541 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.319 | 3.319 | 4.686 | 5.077 | 5.557 | 5.422 | 5.734 | 5.077 | 5.557 | 5.422 | 5.734 | ns |
| | | GCLK PLL | $t_{co}$ | 3.697 | 3.711 | 5.271 | 5.699 | 6.313 | 6.149 | 6.551 | 5.699 | 6.313 | 6.149 | 6.551 | ns |
| 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.317 | 3.317 | 4.667 | 5.055 | 5.531 | 5.396 | 5.708 | 5.055 | 5.531 | 5.396 | 5.708 | ns |
| | | GCLK PLL | $t_{co}$ | 3.695 | 3.709 | 5.252 | 5.677 | 6.287 | 6.123 | 6.525 | 5.677 | 6.287 | 6.123 | 6.525 | ns |

**Table 1–123.** EP3SE110 Column Pins Output Timing Parameters (Part 7 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | UnitS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.336 | 3.336 | 4.703 | 5.096 | 5.577 | 5.442 | 5.754 | 5.096 | 5.577 | 5.442 | 5.754 | ns |
| | | GCLK PLL | $t_{co}$ | 3.716 | 3.728 | 5.289 | 5.719 | 6.333 | 6.169 | 6.571 | 5.719 | 6.333 | 6.169 | 6.571 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.328 | 3.328 | 4.694 | 5.087 | 5.568 | 5.433 | 5.745 | 5.087 | 5.568 | 5.433 | 5.745 | ns |
| | | GCLK PLL | $t_{co}$ | 3.707 | 3.720 | 5.280 | 5.710 | 6.324 | 6.160 | 6.562 | 5.710 | 6.324 | 6.160 | 6.562 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.329 | 3.329 | 4.702 | 5.095 | 5.577 | 5.442 | 5.754 | 5.095 | 5.577 | 5.442 | 5.754 | ns |
| | | GCLK PLL | $t_{co}$ | 3.707 | 3.721 | 5.287 | 5.718 | 6.333 | 6.169 | 6.571 | 5.718 | 6.333 | 6.169 | 6.571 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.318 | 3.318 | 4.689 | 5.082 | 5.563 | 5.428 | 5.740 | 5.082 | 5.563 | 5.428 | 5.740 | ns |
| | | GCLK PLL | $t_{co}$ | 3.697 | 3.710 | 5.274 | 5.704 | 6.319 | 6.155 | 6.557 | 5.704 | 6.319 | 6.155 | 6.557 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.318 | 3.318 | 4.689 | 5.082 | 5.564 | 5.429 | 5.741 | 5.082 | 5.564 | 5.429 | 5.741 | ns |
| | | GCLK PLL | $t_{co}$ | 3.697 | 3.710 | 5.274 | 5.705 | 6.320 | 6.156 | 6.558 | 5.705 | 6.320 | 6.156 | 6.558 | ns |
| 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.339 | 3.339 | 4.705 | 5.097 | 5.577 | 5.442 | 5.754 | 5.097 | 5.577 | 5.442 | 5.754 | ns |
| | | GCLK PLL | $t_{co}$ | 3.718 | 3.731 | 5.290 | 5.720 | 6.333 | 6.169 | 6.571 | 5.720 | 6.333 | 6.169 | 6.571 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.442 | 3.442 | 4.750 | 5.131 | 5.602 | 5.467 | 5.779 | 5.131 | 5.602 | 5.467 | 5.779 | ns |
| | | GCLK PLL | $t_{co}$ | 3.821 | 3.834 | 5.335 | 5.756 | 6.358 | 6.194 | 6.596 | 5.756 | 6.358 | 6.194 | 6.596 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.442 | 3.442 | 4.750 | 5.131 | 5.602 | 5.467 | 5.779 | 5.131 | 5.602 | 5.467 | 5.779 | ns |
| | | GCLK PLL | $t_{co}$ | 3.821 | 3.834 | 5.335 | 5.756 | 6.358 | 6.194 | 6.596 | 5.756 | 6.358 | 6.194 | 6.596 | ns |

Table 1–124 lists the EP3SE110 row pins output timing parameters for single-ended I/O standards.

**Table 1–124.** EP3SE110 Row Pins Output Timing Parameters (Part 1 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.208 | 3.456 | 4.797 | 5.180 | 5.703 | 5.543 | 5.850 | 5.304 | 5.827 | 5.696 | 5.930 | ns |
| | | GCLK PLL | $t_{co}$ | 1.452 | 1.625 | 2.008 | 2.086 | 2.326 | 2.346 | 2.347 | 2.239 | 2.435 | 2.455 | 2.342 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.142 | 3.385 | 4.687 | 5.069 | 5.589 | 5.429 | 5.736 | 5.191 | 5.712 | 5.581 | 5.815 | ns |
| | | GCLK PLL | $t_{co}$ | 1.359 | 1.554 | 1.898 | 1.975 | 2.181 | 2.201 | 2.202 | 2.098 | 2.286 | 2.306 | 2.193 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.063 | 3.296 | 4.581 | 4.969 | 5.493 | 5.333 | 5.640 | 5.092 | 5.612 | 5.481 | 5.715 | ns |
| | | GCLK PLL | $t_{co}$ | 1.260 | 1.465 | 1.792 | 1.875 | 2.053 | 2.073 | 2.074 | 1.971 | 2.154 | 2.174 | 2.061 | ns |

**Table 1–124.** EP3SE110 Row Pins Output Timing Parameters (Part 2 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.210 | 3.463 | 4.801 | 5.186 | 5.712 | 5.552 | 5.859 | 5.312 | 5.839 | 5.708 | 5.942 | ns |
| | | GCLK PLL | $t_{co}$ | 1.462 | 1.632 | 2.012 | 2.092 | 2.330 | 2.350 | 2.351 | 2.245 | 2.439 | 2.459 | 2.346 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.067 | 3.300 | 4.592 | 4.984 | 5.503 | 5.343 | 5.650 | 5.104 | 5.621 | 5.490 | 5.724 | ns |
| | | GCLK PLL | $t_{co}$ | 1.264 | 1.469 | 1.803 | 1.890 | 2.059 | 2.079 | 2.080 | 1.977 | 2.161 | 2.181 | 2.068 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.169 | 3.417 | 4.764 | 5.149 | 5.669 | 5.509 | 5.816 | 5.272 | 5.793 | 5.662 | 5.896 | ns |
| | | GCLK PLL | $t_{co}$ | 1.406 | 1.586 | 1.975 | 2.055 | 2.282 | 2.302 | 2.303 | 2.196 | 2.393 | 2.413 | 2.300 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.068 | 3.305 | 4.627 | 5.007 | 5.524 | 5.364 | 5.671 | 5.130 | 5.648 | 5.516 | 5.750 | ns |
| | | GCLK PLL | $t_{co}$ | 1.281 | 1.474 | 1.838 | 1.913 | 2.118 | 2.138 | 2.139 | 2.034 | 2.229 | 2.248 | 2.135 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.031 | 3.267 | 4.567 | 4.942 | 5.454 | 5.294 | 5.601 | 5.062 | 5.574 | 5.443 | 5.677 | ns |
| | | GCLK PLL | $t_{co}$ | 1.242 | 1.436 | 1.778 | 1.848 | 2.030 | 2.050 | 2.051 | 1.948 | 2.136 | 2.155 | 2.042 | ns |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.090 | 3.329 | 4.662 | 5.042 | 5.560 | 5.400 | 5.707 | 5.163 | 5.684 | 5.552 | 5.786 | ns |
| | | GCLK PLL | $t_{co}$ | 1.320 | 1.498 | 1.873 | 1.948 | 2.172 | 2.192 | 2.193 | 2.088 | 2.282 | 2.301 | 2.188 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.018 | 3.251 | 4.539 | 4.913 | 5.426 | 5.266 | 5.573 | 5.032 | 5.546 | 5.414 | 5.648 | ns |
| | | GCLK PLL | $t_{co}$ | 1.220 | 1.420 | 1.750 | 1.819 | 1.991 | 2.011 | 2.012 | 1.908 | 2.096 | 2.115 | 2.002 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.195 | 3.454 | 4.872 | 5.275 | 5.814 | 5.654 | 5.961 | 5.404 | 5.945 | 5.814 | 6.048 | ns |
| | | GCLK PLL | $t_{co}$ | 1.432 | 1.623 | 2.083 | 2.181 | 2.454 | 2.474 | 2.475 | 2.356 | 2.572 | 2.591 | 2.478 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.110 | 3.351 | 4.748 | 5.140 | 5.672 | 5.512 | 5.819 | 5.267 | 5.801 | 5.669 | 5.903 | ns |
| | | GCLK PLL | $t_{co}$ | 1.322 | 1.520 | 1.959 | 2.046 | 2.284 | 2.304 | 2.305 | 2.189 | 2.398 | 2.417 | 2.304 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.053 | 3.307 | 4.664 | 5.054 | 5.581 | 5.421 | 5.728 | 5.178 | 5.706 | 5.575 | 5.809 | ns |
| | | GCLK PLL | $t_{co}$ | 1.276 | 1.476 | 1.875 | 1.960 | 2.158 | 2.178 | 2.179 | 2.066 | 2.268 | 2.287 | 2.174 | ns |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.458 | 3.730 | 5.334 | 5.790 | 6.350 | 6.220 | 6.500 | 5.931 | 6.493 | 6.365 | 6.600 | ns |
| | | GCLK PLL | $t_{co}$ | 1.663 | 1.874 | 2.520 | 2.669 | 2.929 | 2.949 | 2.954 | 2.792 | 3.056 | 3.075 | 2.967 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.233 | 3.528 | 5.007 | 5.421 | 5.945 | 5.815 | 6.095 | 5.566 | 6.087 | 5.958 | 6.193 | ns |
| | | GCLK PLL | $t_{co}$ | 1.438 | 1.672 | 2.193 | 2.300 | 2.524 | 2.544 | 2.549 | 2.427 | 2.650 | 2.668 | 2.560 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.168 | 3.426 | 4.854 | 5.271 | 5.786 | 5.656 | 5.936 | 5.398 | 5.914 | 5.786 | 6.021 | ns |
| | | GCLK PLL | $t_{co}$ | 1.373 | 1.570 | 2.040 | 2.150 | 2.365 | 2.385 | 2.390 | 2.259 | 2.477 | 2.496 | 2.388 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.108 | 3.352 | 4.777 | 5.177 | 5.691 | 5.559 | 5.839 | 5.303 | 5.820 | 5.692 | 5.927 | ns |
| | | GCLK PLL | $t_{co}$ | 1.313 | 1.496 | 1.963 | 2.056 | 2.268 | 2.288 | 2.293 | 2.164 | 2.383 | 2.402 | 2.294 | ns |


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**Table 1–124.** EP3SE110 Row Pins Output Timing Parameters (Part 3 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.369 | 3.648 | 5.244 | 5.703 | 6.278 | 6.148 | 6.428 | 5.838 | 6.417 | 6.289 | 6.524 | ns |
| | | GCLK PLL | $t_{co}$ | 1.574 | 1.792 | 2.430 | 2.582 | 2.857 | 2.877 | 2.882 | 2.699 | 2.980 | 2.999 | 2.891 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.127 | 3.390 | 4.839 | 5.266 | 5.787 | 5.657 | 5.937 | 5.392 | 5.913 | 5.785 | 6.020 | ns |
| | | GCLK PLL | $t_{co}$ | 1.332 | 1.534 | 2.025 | 2.145 | 2.366 | 2.386 | 2.391 | 2.253 | 2.476 | 2.495 | 2.387 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.100 | 3.343 | 4.766 | 5.170 | 5.691 | 5.551 | 5.834 | 5.294 | 5.816 | 5.685 | 5.916 | ns |
| | | GCLK PLL | $t_{co}$ | 1.305 | 1.487 | 1.952 | 2.049 | 2.260 | 2.280 | 2.285 | 2.155 | 2.371 | 2.390 | 2.282 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.091 | 3.334 | 4.744 | 5.152 | 5.672 | 5.532 | 5.815 | 5.276 | 5.797 | 5.666 | 5.897 | ns |
| | | GCLK PLL | $t_{co}$ | 1.296 | 1.478 | 1.930 | 2.031 | 2.241 | 2.261 | 2.266 | 2.137 | 2.349 | 2.368 | 2.260 | ns |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.312 | 3.573 | 5.154 | 5.617 | 6.203 | 6.073 | 6.353 | 5.750 | 6.333 | 6.205 | 6.440 | ns |
| | | GCLK PLL | $t_{co}$ | 1.517 | 1.717 | 2.340 | 2.496 | 2.782 | 2.802 | 2.807 | 2.611 | 2.896 | 2.915 | 2.807 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.132 | 3.384 | 4.861 | 5.294 | 5.828 | 5.698 | 5.978 | 5.417 | 5.955 | 5.827 | 6.062 | ns |
| | | GCLK PLL | $t_{co}$ | 1.337 | 1.528 | 2.047 | 2.173 | 2.407 | 2.427 | 2.432 | 2.278 | 2.518 | 2.537 | 2.429 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.057 | 3.295 | 4.657 | 5.045 | 5.571 | 5.411 | 5.718 | 5.165 | 5.692 | 5.561 | 5.795 | ns |
| | | GCLK PLL | $t_{co}$ | 1.261 | 1.464 | 1.868 | 1.951 | 2.126 | 2.146 | 2.147 | 2.033 | 2.230 | 2.250 | 2.137 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.052 | 3.291 | 4.654 | 5.043 | 5.569 | 5.409 | 5.716 | 5.164 | 5.691 | 5.560 | 5.794 | ns |
| | | GCLK PLL | $t_{co}$ | 1.249 | 1.460 | 1.865 | 1.949 | 2.118 | 2.138 | 2.139 | 2.025 | 2.223 | 2.243 | 2.130 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.043 | 3.280 | 4.639 | 5.027 | 5.552 | 5.392 | 5.699 | 5.147 | 5.673 | 5.542 | 5.776 | ns |
| | | GCLK PLL | $t_{co}$ | 1.234 | 1.449 | 1.850 | 1.933 | 2.097 | 2.111 | 2.112 | 1.999 | 2.202 | 2.221 | 2.103 | ns |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.069 | 3.308 | 4.672 | 5.065 | 5.586 | 5.433 | 5.729 | 5.184 | 5.707 | 5.576 | 5.807 | ns |
| | | GCLK PLL | $t_{co}$ | 1.274 | 1.452 | 1.858 | 1.944 | 2.142 | 2.162 | 2.167 | 2.045 | 2.246 | 2.265 | 2.157 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.054 | 3.294 | 4.669 | 5.063 | 5.585 | 5.431 | 5.728 | 5.182 | 5.705 | 5.574 | 5.805 | ns |
| | | GCLK PLL | $t_{co}$ | 1.259 | 1.438 | 1.855 | 1.942 | 2.140 | 2.160 | 2.165 | 2.043 | 2.244 | 2.263 | 2.155 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.043 | 3.282 | 4.652 | 5.046 | 5.575 | 5.414 | 5.718 | 5.165 | 5.696 | 5.565 | 5.796 | ns |
| | | GCLK PLL | $t_{co}$ | 1.248 | 1.426 | 1.838 | 1.925 | 2.123 | 2.143 | 2.148 | 2.026 | 2.228 | 2.247 | 2.139 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.030 | 3.267 | 4.636 | 5.030 | 5.562 | 5.399 | 5.705 | 5.150 | 5.684 | 5.553 | 5.784 | ns |
| | | GCLK PLL | $t_{co}$ | 1.228 | 1.404 | 1.822 | 1.909 | 2.108 | 2.128 | 2.133 | 2.011 | 2.213 | 2.232 | 2.124 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.030 | 3.266 | 4.635 | 5.029 | 5.562 | 5.398 | 5.705 | 5.149 | 5.684 | 5.553 | 5.784 | ns |
| | | GCLK PLL | $t_{co}$ | 1.228 | 1.403 | 1.821 | 1.908 | 2.107 | 2.127 | 2.132 | 2.010 | 2.213 | 2.232 | 2.123 | ns |

**Table 1–124.** EP3SE110 Row Pins Output Timing Parameters (Part 4 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.038 | 3.273 | 4.633 | 5.025 | 5.557 | 5.392 | 5.700 | 5.144 | 5.678 | 5.547 | 5.778 | ns |
| | | GCLK PLL | $t_{co}$ | 1.236 | 1.411 | 1.819 | 1.904 | 2.102 | 2.121 | 2.126 | 2.005 | 2.207 | 2.226 | 2.116 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.039 | 3.276 | 4.639 | 5.031 | 5.567 | 5.400 | 5.710 | 5.150 | 5.689 | 5.558 | 5.789 | ns |
| | | GCLK PLL | $t_{co}$ | 1.237 | 1.413 | 1.818 | 1.905 | 2.112 | 2.123 | 2.128 | 2.007 | 2.218 | 2.237 | 2.120 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.065 | 3.304 | 4.683 | 5.079 | 5.599 | 5.450 | 5.742 | 5.197 | 5.719 | 5.588 | 5.819 | ns |
| | | GCLK PLL | $t_{co}$ | 1.270 | 1.448 | 1.869 | 1.958 | 2.159 | 2.179 | 2.184 | 2.058 | 2.262 | 2.281 | 2.173 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.046 | 3.283 | 4.665 | 5.062 | 5.589 | 5.433 | 5.732 | 5.181 | 5.710 | 5.579 | 5.810 | ns |
| | | GCLK PLL | $t_{co}$ | 1.247 | 1.426 | 1.851 | 1.941 | 2.142 | 2.162 | 2.167 | 2.042 | 2.246 | 2.265 | 2.157 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.035 | 3.271 | 4.648 | 5.044 | 5.576 | 5.415 | 5.719 | 5.163 | 5.697 | 5.566 | 5.797 | ns |
| | | GCLK PLL | $t_{co}$ | 1.233 | 1.409 | 1.834 | 1.923 | 2.124 | 2.144 | 2.149 | 2.024 | 2.229 | 2.248 | 2.140 | ns |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.045 | 3.280 | 4.639 | 5.030 | 5.555 | 5.395 | 5.698 | 5.148 | 5.675 | 5.544 | 5.775 | ns |
| | | GCLK PLL | $t_{co}$ | 1.249 | 1.424 | 1.825 | 1.909 | 2.104 | 2.124 | 2.129 | 2.009 | 2.208 | 2.227 | 2.119 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.038 | 3.273 | 4.630 | 5.022 | 5.554 | 5.387 | 5.697 | 5.140 | 5.675 | 5.544 | 5.775 | ns |
| | | GCLK PLL | $t_{co}$ | 1.237 | 1.412 | 1.816 | 1.901 | 2.099 | 2.116 | 2.121 | 2.001 | 2.204 | 2.223 | 2.112 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.029 | 3.265 | 4.623 | 5.013 | 5.547 | 5.380 | 5.690 | 5.132 | 5.668 | 5.537 | 5.768 | ns |
| | | GCLK PLL | $t_{co}$ | 1.227 | 1.402 | 1.807 | 1.892 | 2.092 | 2.108 | 2.113 | 1.993 | 2.197 | 2.216 | 2.104 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.032 | 3.267 | 4.626 | 5.016 | 5.551 | 5.384 | 5.694 | 5.135 | 5.671 | 5.540 | 5.771 | ns |
| | | GCLK PLL | $t_{co}$ | 1.230 | 1.404 | 1.810 | 1.895 | 2.096 | 2.111 | 2.116 | 1.996 | 2.200 | 2.219 | 2.107 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.028 | 3.264 | 4.628 | 5.019 | 5.554 | 5.387 | 5.697 | 5.138 | 5.676 | 5.545 | 5.776 | ns |
| | | GCLK PLL | $t_{co}$ | 1.226 | 1.401 | 1.808 | 1.894 | 2.099 | 2.111 | 2.116 | 1.996 | 2.205 | 2.224 | 2.108 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.036 | 3.272 | 4.626 | 5.016 | 5.550 | 5.383 | 5.693 | 5.134 | 5.670 | 5.539 | 5.770 | ns |
| | | GCLK PLL | $t_{co}$ | 1.234 | 1.409 | 1.805 | 1.890 | 2.095 | 2.106 | 2.107 | 1.991 | 2.199 | 2.218 | 2.097 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.051 | 3.287 | 4.650 | 5.043 | 5.566 | 5.410 | 5.709 | 5.160 | 5.686 | 5.555 | 5.786 | ns |
| | | GCLK PLL | $t_{co}$ | 1.256 | 1.431 | 1.836 | 1.922 | 2.119 | 2.139 | 2.144 | 2.021 | 2.222 | 2.241 | 2.133 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.045 | 3.280 | 4.646 | 5.039 | 5.568 | 5.406 | 5.711 | 5.157 | 5.689 | 5.558 | 5.789 | ns |
| | | GCLK PLL | $t_{co}$ | 1.244 | 1.421 | 1.832 | 1.918 | 2.115 | 2.135 | 2.140 | 2.018 | 2.219 | 2.238 | 2.130 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.041 | 3.276 | 4.640 | 5.033 | 5.563 | 5.400 | 5.706 | 5.151 | 5.683 | 5.552 | 5.783 | ns |
| | | GCLK PLL | $t_{co}$ | 1.240 | 1.416 | 1.826 | 1.912 | 2.109 | 2.129 | 2.134 | 2.012 | 2.213 | 2.232 | 2.124 | ns |


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**Table 1–124.** EP3SE110 Row Pins Output Timing Parameters (Part 5 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.053 | 3.287 | 4.661 | 5.057 | 5.585 | 5.428 | 5.728 | 5.174 | 5.705 | 5.574 | 5.805 | ns |
| | | GCLK PLL | $t_{co}$ | 1.255 | 1.430 | 1.847 | 1.936 | 2.137 | 2.157 | 2.162 | 2.035 | 2.239 | 2.258 | 2.150 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.044 | 3.279 | 4.650 | 5.045 | 5.576 | 5.416 | 5.719 | 5.163 | 5.696 | 5.565 | 5.796 | ns |
| | | GCLK PLL | $t_{co}$ | 1.243 | 1.418 | 1.836 | 1.924 | 2.125 | 2.145 | 2.150 | 2.024 | 2.228 | 2.247 | 2.139 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.043 | 3.279 | 4.654 | 5.050 | 5.585 | 5.422 | 5.728 | 5.169 | 5.706 | 5.575 | 5.806 | ns |
| | | GCLK PLL | $t_{co}$ | 1.241 | 1.416 | 1.840 | 1.929 | 2.131 | 2.151 | 2.156 | 2.030 | 2.235 | 2.254 | 2.146 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.163 | 3.401 | 4.709 | 5.091 | 5.611 | 5.451 | 5.758 | 5.213 | 5.734 | 5.603 | 5.837 | ns |
| | | GCLK PLL | $t_{co}$ | 1.354 | 1.570 | 1.920 | 1.997 | 2.156 | 2.167 | 2.156 | 2.061 | 2.263 | 2.282 | 2.149 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.163 | 3.401 | 4.709 | 5.091 | 5.611 | 5.451 | 5.758 | 5.213 | 5.734 | 5.603 | 5.837 | ns |
| | | GCLK PLL | $t_{co}$ | 1.354 | 1.570 | 1.920 | 1.997 | 2.156 | 2.167 | 2.156 | 2.061 | 2.263 | 2.282 | 2.149 | ns |

Table 1–125 through Table 1–128 list the maximum I/O timing parameters for EP3SE110 devices for differential I/O standards.

Table 1–125 lists the EP3SE110 column pins input timing parameters for differential I/O standards.

**Table 1–125.** EP3SE110 Column Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -0.997 | -1.029 | -1.181 | -1.169 | -1.324 | -1.269 | -1.645 | -1.133 | -1.542 | -1.230 | -1.683 | ns |
| | | $t_h$ | 1.133 | 1.184 | 1.415 | 1.436 | 1.618 | 1.551 | 1.927 | 1.411 | 1.858 | 1.524 | 1.966 | ns |
| | GCLK PLL | $t_{su}$ | 0.960 | 0.994 | 1.879 | 2.224 | 2.401 | 2.288 | 2.194 | 2.277 | 2.567 | 2.345 | 2.245 | ns |
| | | $t_h$ | -0.691 | -0.701 | -1.428 | -1.714 | -1.834 | -1.749 | -1.648 | -1.756 | -1.968 | -1.795 | -1.697 | ns |
| MINI-LVDS | | $t_{su}$ | -0.997 | -1.029 | -1.181 | -1.169 | -1.324 | -1.269 | -1.645 | -1.133 | -1.542 | -1.230 | -1.683 | ns |
| | GCLK | $t_h$ | 1.133 | 1.184 | 1.415 | 1.436 | 1.618 | 1.551 | 1.927 | 1.411 | 1.858 | 1.524 | 1.966 | ns |
| | | $t_{su}$ | 0.960 | 0.994 | 1.879 | 2.224 | 2.401 | 2.288 | 2.194 | 2.277 | 2.567 | 2.345 | 2.245 | ns |
| | GCLK PLL | $t_h$ | -0.691 | -0.701 | -1.428 | -1.714 | -1.834 | -1.749 | -1.648 | -1.756 | -1.968 | -1.795 | -1.697 | ns |
| RSDS | | $t_{su}$ | -0.997 | -1.029 | -1.181 | -1.169 | -1.324 | -1.269 | -1.645 | -1.133 | -1.542 | -1.230 | -1.683 | ns |
| | | $t_h$ | 1.133 | 1.184 | 1.415 | 1.436 | 1.618 | 1.551 | 1.927 | 1.411 | 1.858 | 1.524 | 1.966 | ns |
| | GCLK | $t_{su}$ | 0.960 | 0.994 | 1.879 | 2.224 | 2.401 | 2.288 | 2.194 | 2.277 | 2.567 | 2.345 | 2.245 | ns |
| | | $t_h$ | -0.691 | -0.701 | -1.428 | -1.714 | -1.834 | -1.749 | -1.648 | -1.756 | -1.968 | -1.795 | -1.697 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.813 | -0.852 | -1.258 | -1.368 | -1.483 | -1.423 | -1.794 | -1.368 | -1.482 | -1.428 | -1.837 | ns |
| | | $t_h$ | 0.942 | 0.999 | 1.460 | 1.595 | 1.731 | 1.659 | 2.031 | 1.604 | 1.739 | 1.674 | 2.075 | ns |
| | GCLK PLL | $t_{su}$ | 1.144 | 1.171 | 1.802 | 2.025 | 2.242 | 2.134 | 2.045 | 2.042 | 2.260 | 2.147 | 2.091 | ns |
| | | $t_h$ | -0.882 | -0.886 | -1.383 | -1.555 | -1.721 | -1.641 | -1.544 | -1.563 | -1.729 | -1.645 | -1.588 | ns |

**Table 1–125.** EP3SE110 Column Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.813 | -0.852 | -1.258 | -1.368 | -1.483 | -1.423 | -1.794 | -1.368 | -1.482 | -1.428 | -1.837 | ns |
| | | $t_h$ | 0.942 | 0.999 | 1.460 | 1.595 | 1.731 | 1.659 | 2.031 | 1.604 | 1.739 | 1.674 | 2.075 | ns |
| | GCLK PLL | $t_{su}$ | 1.144 | 1.171 | 1.802 | 2.025 | 2.242 | 2.134 | 2.045 | 2.042 | 2.260 | 2.147 | 2.091 | ns |
| | | $t_h$ | -0.882 | -0.886 | -1.383 | -1.555 | -1.721 | -1.641 | -1.544 | -1.563 | -1.729 | -1.645 | -1.588 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.821 | -0.864 | -1.268 | -1.379 | -1.499 | -1.439 | -1.810 | -1.379 | -1.497 | -1.443 | -1.852 | ns |
| | | $t_h$ | 0.950 | 1.011 | 1.470 | 1.606 | 1.747 | 1.675 | 2.047 | 1.615 | 1.754 | 1.689 | 2.090 | ns |
| | GCLK PLL | $t_{su}$ | 1.136 | 1.159 | 1.792 | 2.014 | 2.226 | 2.118 | 2.029 | 2.031 | 2.245 | 2.132 | 2.076 | ns |
| | | $t_h$ | -0.874 | -0.874 | -1.373 | -1.544 | -1.705 | -1.625 | -1.528 | -1.552 | -1.714 | -1.630 | -1.573 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.821 | -0.864 | -1.268 | -1.379 | -1.499 | -1.439 | -1.810 | -1.379 | -1.497 | -1.443 | -1.852 | ns |
| | | $t_h$ | 0.950 | 1.011 | 1.470 | 1.606 | 1.747 | 1.675 | 2.047 | 1.615 | 1.754 | 1.689 | 2.090 | ns |
| | GCLK PLL | $t_{su}$ | 1.136 | 1.159 | 1.792 | 2.014 | 2.226 | 2.118 | 2.029 | 2.031 | 2.245 | 2.132 | 2.076 | ns |
| | | $t_h$ | -0.874 | -0.874 | -1.373 | -1.544 | -1.705 | -1.625 | -1.528 | -1.552 | -1.714 | -1.630 | -1.573 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.833 | -0.875 | -1.277 | -1.390 | -1.518 | -1.458 | -1.829 | -1.390 | -1.515 | -1.461 | -1.870 | ns |
| | | $t_h$ | 0.962 | 1.022 | 1.480 | 1.617 | 1.766 | 1.694 | 2.066 | 1.626 | 1.772 | 1.707 | 2.108 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.148 | 1.783 | 2.003 | 2.207 | 2.099 | 2.010 | 2.020 | 2.227 | 2.114 | 2.058 | ns |
| | | $t_h$ | -0.862 | -0.863 | -1.363 | -1.533 | -1.686 | -1.606 | -1.509 | -1.541 | -1.696 | -1.612 | -1.555 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.833 | -0.875 | -1.277 | -1.390 | -1.518 | -1.458 | -1.829 | -1.390 | -1.515 | -1.461 | -1.870 | ns |
| | | $t_h$ | 0.962 | 1.022 | 1.480 | 1.617 | 1.766 | 1.694 | 2.066 | 1.626 | 1.772 | 1.707 | 2.108 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.148 | 1.783 | 2.003 | 2.207 | 2.099 | 2.010 | 2.020 | 2.227 | 2.114 | 2.058 | ns |
| | | $t_h$ | -0.862 | -0.863 | -1.363 | -1.533 | -1.686 | -1.606 | -1.509 | -1.541 | -1.696 | -1.612 | -1.555 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.821 | -0.864 | -1.268 | -1.379 | -1.499 | -1.439 | -1.810 | -1.379 | -1.497 | -1.443 | -1.852 | ns |
| | | $t_h$ | 0.950 | 1.011 | 1.470 | 1.606 | 1.747 | 1.675 | 2.047 | 1.615 | 1.754 | 1.689 | 2.090 | ns |
| | GCLK PLL | $t_{su}$ | 1.136 | 1.159 | 1.792 | 2.014 | 2.226 | 2.118 | 2.029 | 2.031 | 2.245 | 2.132 | 2.076 | ns |
| | | $t_h$ | -0.874 | -0.874 | -1.373 | -1.544 | -1.705 | -1.625 | -1.528 | -1.552 | -1.714 | -1.630 | -1.573 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.821 | -0.864 | -1.268 | -1.379 | -1.499 | -1.439 | -1.810 | -1.379 | -1.497 | -1.443 | -1.852 | ns |
| | | $t_h$ | 0.950 | 1.011 | 1.470 | 1.606 | 1.747 | 1.675 | 2.047 | 1.615 | 1.754 | 1.689 | 2.090 | ns |
| | GCLK PLL | $t_{su}$ | 1.136 | 1.159 | 1.792 | 2.014 | 2.226 | 2.118 | 2.029 | 2.031 | 2.245 | 2.132 | 2.076 | ns |
| | | $t_h$ | -0.874 | -0.874 | -1.373 | -1.544 | -1.705 | -1.625 | -1.528 | -1.552 | -1.714 | -1.630 | -1.573 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -0.833 | -0.875 | -1.277 | -1.390 | -1.518 | -1.458 | -1.829 | -1.390 | -1.515 | -1.461 | -1.870 | ns |
| | | $t_h$ | 0.962 | 1.022 | 1.480 | 1.617 | 1.766 | 1.694 | 2.066 | 1.626 | 1.772 | 1.707 | 2.108 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.148 | 1.783 | 2.003 | 2.207 | 2.099 | 2.010 | 2.020 | 2.227 | 2.114 | 2.058 | ns |
| | | $t_h$ | -0.862 | -0.863 | -1.363 | -1.533 | -1.686 | -1.606 | -1.509 | -1.541 | -1.696 | -1.612 | -1.555 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -0.833 | -0.875 | -1.277 | -1.390 | -1.518 | -1.458 | -1.829 | -1.390 | -1.515 | -1.461 | -1.870 | ns |
| | | $t_h$ | 0.962 | 1.022 | 1.480 | 1.617 | 1.766 | 1.694 | 2.066 | 1.626 | 1.772 | 1.707 | 2.108 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.148 | 1.783 | 2.003 | 2.207 | 2.099 | 2.010 | 2.020 | 2.227 | 2.114 | 2.058 | ns |
| | | $t_h$ | -0.862 | -0.863 | -1.363 | -1.533 | -1.686 | -1.606 | -1.509 | -1.541 | -1.696 | -1.612 | -1.555 | ns |

**Table 1–125.** EP3SE110 Column Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.840 | -0.881 | -1.289 | -1.395 | -1.518 | -1.460 | -1.828 | -1.394 | -1.510 | -1.459 | -1.866 | ns |
| | | $t_h$ | 0.969 | 1.028 | 1.493 | 1.625 | 1.769 | 1.697 | 2.070 | 1.633 | 1.772 | 1.706 | 2.109 | ns |
| | GCLK PLL | $t_{su}$ | 1.117 | 1.142 | 1.771 | 1.998 | 2.207 | 2.097 | 2.011 | 2.016 | 2.232 | 2.116 | 2.062 | ns |
| | | $t_h$ | -0.855 | -0.857 | -1.350 | -1.525 | -1.683 | -1.603 | -1.505 | -1.534 | -1.696 | -1.613 | -1.554 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.840 | -0.881 | -1.289 | -1.395 | -1.518 | -1.460 | -1.828 | -1.394 | -1.510 | -1.459 | -1.866 | ns |
| | | $t_h$ | 0.969 | 1.028 | 1.493 | 1.625 | 1.769 | 1.697 | 2.070 | 1.633 | 1.772 | 1.706 | 2.109 | ns |
| | GCLK PLL | $t_{su}$ | 1.117 | 1.142 | 1.771 | 1.998 | 2.207 | 2.097 | 2.011 | 2.016 | 2.232 | 2.116 | 2.062 | ns |
| | | $t_h$ | -0.855 | -0.857 | -1.350 | -1.525 | -1.683 | -1.603 | -1.505 | -1.534 | -1.696 | -1.613 | -1.554 | ns |

Table 1–126 lists the EP3SE110 row pins input timing parameters for differential I/O standards

**Table 1–126.** EP3SE110 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -0.944 | -0.979 | -1.054 | -1.015 | -1.154 | -1.107 | -1.454 | -0.975 | -1.107 | -1.061 | -1.493 | ns |
| | | $t_h$ | 1.077 | 1.130 | 1.288 | 1.285 | 1.447 | 1.389 | 1.737 | 1.257 | 1.412 | 1.355 | 1.777 | ns |
| | GCLK PLL | $t_{su}$ | 0.961 | 0.989 | 1.951 | 2.328 | 2.533 | 2.408 | 2.342 | 2.387 | 2.599 | 2.472 | 2.394 | ns |
| | | $t_h$ | -0.691 | -0.700 | -1.502 | -1.818 | -1.968 | -1.871 | -1.796 | -1.862 | -2.019 | -1.921 | -1.844 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -0.944 | -0.979 | -1.054 | -1.015 | -1.154 | -1.107 | -1.454 | -0.975 | -1.107 | -1.061 | -1.493 | ns |
| | | $t_h$ | 1.077 | 1.130 | 1.288 | 1.285 | 1.447 | 1.389 | 1.737 | 1.257 | 1.412 | 1.355 | 1.777 | ns |
| | GCLK PLL | $t_{su}$ | 0.961 | 0.989 | 1.951 | 2.328 | 2.533 | 2.408 | 2.342 | 2.387 | 2.599 | 2.472 | 2.394 | ns |
| | | $t_h$ | -0.691 | -0.700 | -1.502 | -1.818 | -1.968 | -1.871 | -1.796 | -1.862 | -2.019 | -1.921 | -1.844 | ns |
| RSDS | GCLK | $t_{su}$ | -0.944 | -0.979 | -1.054 | -1.015 | -1.154 | -1.107 | -1.454 | -0.975 | -1.107 | -1.061 | -1.493 | ns |
| | | $t_h$ | 1.077 | 1.130 | 1.288 | 1.285 | 1.447 | 1.389 | 1.737 | 1.257 | 1.412 | 1.355 | 1.777 | ns |
| | GCLK PLL | $t_{su}$ | 0.961 | 0.989 | 1.951 | 2.328 | 2.533 | 2.408 | 2.342 | 2.387 | 2.599 | 2.472 | 2.394 | ns |
| | | $t_h$ | -0.691 | -0.700 | -1.502 | -1.818 | -1.968 | -1.871 | -1.796 | -1.862 | -2.019 | -1.921 | -1.844 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -0.749 | -0.794 | -1.145 | -1.244 | -1.343 | -1.291 | -1.633 | -1.246 | -1.344 | -1.293 | -1.677 | ns |
| | | $t_h$ | 0.875 | 0.936 | 1.345 | 1.468 | 1.587 | 1.524 | 1.867 | 1.479 | 1.597 | 1.535 | 1.912 | ns |
| | GCLK PLL | $t_{su}$ | 1.156 | 1.174 | 1.864 | 2.104 | 2.344 | 2.224 | 2.163 | 2.120 | 2.362 | 2.240 | 2.210 | ns |
| | | $t_h$ | -0.893 | -0.894 | -1.447 | -1.639 | -1.828 | -1.736 | -1.666 | -1.644 | -1.834 | -1.741 | -1.709 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -0.749 | -0.794 | -1.145 | -1.244 | -1.343 | -1.291 | -1.633 | -1.246 | -1.344 | -1.293 | -1.677 | ns |
| | | $t_h$ | 0.875 | 0.936 | 1.345 | 1.468 | 1.587 | 1.524 | 1.867 | 1.479 | 1.597 | 1.535 | 1.912 | ns |
| | GCLK PLL | $t_{su}$ | 1.156 | 1.174 | 1.864 | 2.104 | 2.344 | 2.224 | 2.163 | 2.120 | 2.362 | 2.240 | 2.210 | ns |
| | | $t_h$ | -0.893 | -0.894 | -1.447 | -1.639 | -1.828 | -1.736 | -1.666 | -1.644 | -1.834 | -1.741 | -1.709 | ns |

**Table 1–126.** EP3SE110 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -0.758 | -0.806 | -1.154 | -1.254 | -1.359 | -1.307 | -1.649 | -1.255 | -1.360 | -1.309 | -1.693 | ns |
| | | $t_h$ | 0.884 | 0.948 | 1.354 | 1.478 | 1.603 | 1.540 | 1.883 | 1.488 | 1.613 | 1.551 | 1.928 | ns |
| | GCLK PLL | $t_{su}$ | 1.147 | 1.162 | 1.855 | 2.094 | 2.328 | 2.208 | 2.147 | 2.111 | 2.346 | 2.224 | 2.194 | ns |
| | | $t_h$ | -0.884 | -0.882 | -1.438 | -1.629 | -1.812 | -1.720 | -1.650 | -1.635 | -1.818 | -1.725 | -1.693 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -0.758 | -0.806 | -1.154 | -1.254 | -1.359 | -1.307 | -1.649 | -1.255 | -1.360 | -1.309 | -1.693 | ns |
| | | $t_h$ | 0.884 | 0.948 | 1.354 | 1.478 | 1.603 | 1.540 | 1.883 | 1.488 | 1.613 | 1.551 | 1.928 | ns |
| | GCLK PLL | $t_{su}$ | 1.147 | 1.162 | 1.855 | 2.094 | 2.328 | 2.208 | 2.147 | 2.111 | 2.346 | 2.224 | 2.194 | ns |
| | | $t_h$ | -0.884 | -0.882 | -1.438 | -1.629 | -1.812 | -1.720 | -1.650 | -1.635 | -1.818 | -1.725 | -1.693 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -0.772 | -0.818 | -1.163 | -1.264 | -1.377 | -1.325 | -1.667 | -1.266 | -1.377 | -1.326 | -1.710 | ns |
| | | $t_h$ | 0.898 | 0.960 | 1.364 | 1.488 | 1.621 | 1.558 | 1.901 | 1.499 | 1.630 | 1.568 | 1.945 | ns |
| | GCLK PLL | $t_{su}$ | 1.133 | 1.150 | 1.842 | 2.084 | 2.310 | 2.190 | 2.129 | 2.100 | 2.329 | 2.207 | 2.177 | ns |
| | | $t_h$ | -0.870 | -0.870 | -1.426 | -1.619 | -1.794 | -1.702 | -1.632 | -1.624 | -1.801 | -1.708 | -1.676 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -0.772 | -0.818 | -1.163 | -1.264 | -1.377 | -1.325 | -1.667 | -1.266 | -1.377 | -1.326 | -1.710 | ns |
| | | $t_h$ | 0.898 | 0.960 | 1.364 | 1.488 | 1.621 | 1.558 | 1.901 | 1.499 | 1.630 | 1.568 | 1.945 | ns |
| | GCLK PLL | $t_{su}$ | 1.133 | 1.150 | 1.842 | 2.084 | 2.310 | 2.190 | 2.129 | 2.100 | 2.329 | 2.207 | 2.177 | ns |
| | | $t_h$ | -0.870 | -0.870 | -1.426 | -1.619 | -1.794 | -1.702 | -1.632 | -1.624 | -1.801 | -1.708 | -1.676 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.758 | -0.806 | -1.154 | -1.254 | -1.359 | -1.307 | -1.649 | -1.255 | -1.360 | -1.309 | -1.693 | ns |
| | | $t_h$ | 0.884 | 0.948 | 1.354 | 1.478 | 1.603 | 1.540 | 1.883 | 1.488 | 1.613 | 1.551 | 1.928 | ns |
| | GCLK PLL | $t_{su}$ | 1.147 | 1.162 | 1.855 | 2.094 | 2.328 | 2.208 | 2.147 | 2.111 | 2.346 | 2.224 | 2.194 | ns |
| | | $t_h$ | -0.884 | -0.882 | -1.438 | -1.629 | -1.812 | -1.720 | -1.650 | -1.635 | -1.818 | -1.725 | -1.693 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.758 | -0.806 | -1.154 | -1.254 | -1.359 | -1.307 | -1.649 | -1.255 | -1.360 | -1.309 | -1.693 | ns |
| | | $t_h$ | 0.884 | 0.948 | 1.354 | 1.478 | 1.603 | 1.540 | 1.883 | 1.488 | 1.613 | 1.551 | 1.928 | ns |
| | GCLK PLL | $t_{su}$ | 1.147 | 1.162 | 1.855 | 2.094 | 2.328 | 2.208 | 2.147 | 2.111 | 2.346 | 2.224 | 2.194 | ns |
| | | $t_h$ | -0.884 | -0.882 | -1.438 | -1.629 | -1.812 | -1.720 | -1.650 | -1.635 | -1.818 | -1.725 | -1.693 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -0.772 | -0.818 | -1.163 | -1.264 | -1.377 | -1.325 | -1.667 | -1.266 | -1.377 | -1.326 | -1.710 | ns |
| | | $t_h$ | 0.898 | 0.960 | 1.364 | 1.488 | 1.621 | 1.558 | 1.901 | 1.499 | 1.630 | 1.568 | 1.945 | ns |
| | GCLK PLL | $t_{su}$ | 1.133 | 1.150 | 1.842 | 2.084 | 2.310 | 2.190 | 2.129 | 2.100 | 2.329 | 2.207 | 2.177 | ns |
| | | $t_h$ | -0.870 | -0.870 | -1.426 | -1.619 | -1.794 | -1.702 | -1.632 | -1.624 | -1.801 | -1.708 | -1.676 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -0.772 | -0.818 | -1.163 | -1.264 | -1.377 | -1.325 | -1.667 | -1.266 | -1.377 | -1.326 | -1.710 | ns |
| | | $t_h$ | 0.898 | 0.960 | 1.364 | 1.488 | 1.621 | 1.558 | 1.901 | 1.499 | 1.630 | 1.568 | 1.945 | ns |
| | GCLK PLL | $t_{su}$ | 1.133 | 1.150 | 1.842 | 2.084 | 2.310 | 2.190 | 2.129 | 2.100 | 2.329 | 2.207 | 2.177 | ns |
| | | $t_h$ | -0.870 | -0.870 | -1.426 | -1.619 | -1.794 | -1.702 | -1.632 | -1.624 | -1.801 | -1.708 | -1.676 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -0.781 | -0.827 | -1.178 | -1.275 | -1.384 | -1.333 | -1.673 | -1.273 | -1.378 | -1.329 | -1.712 | ns |
| | | $t_h$ | 0.907 | 0.969 | 1.379 | 1.502 | 1.631 | 1.568 | 1.912 | 1.509 | 1.636 | 1.573 | 1.952 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.141 | 1.827 | 2.068 | 2.299 | 2.178 | 2.118 | 2.089 | 2.323 | 2.199 | 2.170 | ns |
| | | $t_h$ | -0.861 | -0.861 | -1.411 | -1.601 | -1.780 | -1.688 | -1.617 | -1.610 | -1.792 | -1.699 | -1.665 | ns |


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**Table 1–126.** EP3SE110 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -0.781 | -0.827 | -1.178 | -1.275 | -1.384 | -1.333 | -1.673 | -1.273 | -1.378 | -1.329 | -1.712 | ns |
| | | $t_h$ | 0.907 | 0.969 | 1.379 | 1.502 | 1.631 | 1.568 | 1.912 | 1.509 | 1.636 | 1.573 | 1.952 | ns |
| | GCLK PLL | $t_{su}$ | 1.124 | 1.141 | 1.827 | 2.068 | 2.299 | 2.178 | 2.118 | 2.089 | 2.323 | 2.199 | 2.170 | ns |
| | | $t_h$ | -0.861 | -0.861 | -1.411 | -1.601 | -1.780 | -1.688 | -1.617 | -1.610 | -1.792 | -1.699 | -1.665 | ns |

Table 1–127 lists the EP3SE110 column pins output timing parameters for differential I/O standards.

**Table 1–127.** EP3SE110 Column Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 0.9V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 0.9V | |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.152 | 3.387 | 4.757 | 5.155 | 5.666 | 5.526 | 5.826 | 5.278 | 5.789 | 5.650 | 5.899 | ns |
| | | GCLK PLL | $t_{co}$ | 1.328 | 1.502 | 1.913 | 2.006 | 2.214 | 2.225 | 2.251 | 2.110 | 2.321 | 2.331 | 2.237 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.148 | 3.390 | 4.804 | 5.210 | 5.728 | 5.588 | 5.888 | 5.337 | 5.855 | 5.716 | 5.965 | ns |
| | | GCLK PLL | $t_{co}$ | 1.324 | 1.505 | 1.960 | 2.061 | 2.276 | 2.287 | 2.313 | 2.169 | 2.387 | 2.397 | 2.303 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.152 | 3.387 | 4.757 | 5.155 | 5.666 | 5.526 | 5.826 | 5.278 | 5.789 | 5.650 | 5.899 | ns |
| | | GCLK PLL | $t_{co}$ | 1.328 | 1.502 | 1.913 | 2.006 | 2.214 | 2.225 | 2.251 | 2.110 | 2.321 | 2.331 | 2.237 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.148 | 3.390 | 4.804 | 5.210 | 5.728 | 5.588 | 5.888 | 5.337 | 5.855 | 5.716 | 5.965 | ns |
| | | GCLK PLL | $t_{co}$ | 1.324 | 1.505 | 1.960 | 2.061 | 2.276 | 2.287 | 2.313 | 2.169 | 2.387 | 2.397 | 2.303 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.152 | 3.387 | 4.757 | 5.155 | 5.666 | 5.526 | 5.826 | 5.278 | 5.789 | 5.650 | 5.899 | ns |
| | | GCLK PLL | $t_{co}$ | 1.328 | 1.502 | 1.913 | 2.006 | 2.214 | 2.225 | 2.251 | 2.110 | 2.321 | 2.331 | 2.237 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.148 | 3.390 | 4.804 | 5.210 | 5.728 | 5.588 | 5.888 | 5.337 | 5.855 | 5.716 | 5.965 | ns |
| | | GCLK PLL | $t_{co}$ | 1.324 | 1.505 | 1.960 | 2.061 | 2.276 | 2.287 | 2.313 | 2.169 | 2.387 | 2.397 | 2.303 | ns |

**Table 1–127.** EP3SE110 Column Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 0.9V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 0.9V | |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.179 | 3.420 | 4.828 | 5.233 | 5.750 | 5.610 | 5.910 | 5.358 | 5.875 | 5.736 | 5.985 | ns |
| | | GCLK PLL | $t_{co}$ | 1.355 | 1.535 | 1.984 | 2.084 | 2.298 | 2.309 | 2.335 | 2.190 | 2.407 | 2.417 | 2.323 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.169 | 3.410 | 4.818 | 5.222 | 5.740 | 5.600 | 5.900 | 5.347 | 5.865 | 5.726 | 5.975 | ns |
| | | GCLK PLL | $t_{co}$ | 1.345 | 1.525 | 1.974 | 2.073 | 2.288 | 2.299 | 2.325 | 2.179 | 2.397 | 2.407 | 2.313 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.169 | 3.410 | 4.821 | 5.226 | 5.744 | 5.604 | 5.904 | 5.352 | 5.870 | 5.731 | 5.980 | ns |
| | | GCLK PLL | $t_{co}$ | 1.345 | 1.525 | 1.977 | 2.077 | 2.292 | 2.303 | 2.329 | 2.184 | 2.402 | 2.412 | 2.318 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.162 | 3.404 | 4.814 | 5.220 | 5.738 | 5.598 | 5.898 | 5.345 | 5.864 | 5.725 | 5.974 | ns |
| | | GCLK PLL | $t_{co}$ | 1.338 | 1.519 | 1.970 | 2.071 | 2.286 | 2.297 | 2.323 | 2.177 | 2.396 | 2.406 | 2.312 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.161 | 3.402 | 4.811 | 5.217 | 5.735 | 5.595 | 5.895 | 5.342 | 5.860 | 5.721 | 5.970 | ns |
| | | GCLK PLL | $t_{co}$ | 1.337 | 1.517 | 1.967 | 2.068 | 2.283 | 2.294 | 2.320 | 2.174 | 2.392 | 2.402 | 2.308 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.183 | 3.424 | 4.832 | 5.237 | 5.754 | 5.614 | 5.914 | 5.362 | 5.880 | 5.741 | 5.990 | ns |
| | | GCLK PLL | $t_{co}$ | 1.359 | 1.539 | 1.988 | 2.088 | 2.302 | 2.313 | 2.339 | 2.194 | 2.412 | 2.422 | 2.328 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.173 | 3.413 | 4.811 | 5.214 | 5.729 | 5.589 | 5.889 | 5.338 | 5.853 | 5.714 | 5.963 | ns |
| | | GCLK PLL | $t_{co}$ | 1.349 | 1.528 | 1.967 | 2.065 | 2.277 | 2.288 | 2.314 | 2.170 | 2.385 | 2.395 | 2.301 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.168 | 3.409 | 4.811 | 5.214 | 5.730 | 5.590 | 5.890 | 5.339 | 5.855 | 5.716 | 5.965 | ns |
| | | GCLK PLL | $t_{co}$ | 1.344 | 1.524 | 1.967 | 2.065 | 2.278 | 2.289 | 2.315 | 2.171 | 2.387 | 2.397 | 2.303 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.166 | 3.407 | 4.810 | 5.213 | 5.728 | 5.588 | 5.888 | 5.338 | 5.854 | 5.715 | 5.964 | ns |
| | | GCLK PLL | $t_{co}$ | 1.342 | 1.522 | 1.966 | 2.064 | 2.276 | 2.287 | 2.313 | 2.170 | 2.386 | 2.396 | 2.302 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.158 | 3.398 | 4.800 | 5.203 | 5.719 | 5.579 | 5.879 | 5.328 | 5.844 | 5.705 | 5.954 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.513 | 1.956 | 2.054 | 2.267 | 2.278 | 2.304 | 2.160 | 2.376 | 2.386 | 2.292 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.159 | 3.400 | 4.806 | 5.210 | 5.727 | 5.587 | 5.887 | 5.336 | 5.853 | 5.714 | 5.963 | ns |
| | | GCLK PLL | $t_{co}$ | 1.335 | 1.515 | 1.962 | 2.061 | 2.275 | 2.286 | 2.312 | 2.168 | 2.385 | 2.395 | 2.301 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.158 | 3.397 | 4.789 | 5.191 | 5.705 | 5.565 | 5.865 | 5.315 | 5.829 | 5.690 | 5.939 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.512 | 1.945 | 2.042 | 2.253 | 2.264 | 2.290 | 2.147 | 2.361 | 2.371 | 2.277 | ns |


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**Table 1–127.** EP3SE110 Column Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 0.9V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 0.9V | |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.170 | 3.410 | 4.807 | 5.209 | 5.723 | 5.583 | 5.883 | 5.334 | 5.848 | 5.709 | 5.958 | ns |
| | | GCLK PLL | $t_{co}$ | 1.346 | 1.525 | 1.963 | 2.060 | 2.271 | 2.282 | 2.308 | 2.166 | 2.380 | 2.390 | 2.296 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.166 | 3.407 | 4.808 | 5.211 | 5.727 | 5.587 | 5.887 | 5.336 | 5.852 | 5.713 | 5.962 | ns |
| | | GCLK PLL | $t_{co}$ | 1.342 | 1.522 | 1.964 | 2.062 | 2.275 | 2.286 | 2.312 | 2.168 | 2.384 | 2.394 | 2.300 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.156 | 3.396 | 4.797 | 5.200 | 5.715 | 5.575 | 5.875 | 5.325 | 5.840 | 5.701 | 5.950 | ns |
| | | GCLK PLL | $t_{co}$ | 1.332 | 1.511 | 1.953 | 2.051 | 2.263 | 2.274 | 2.300 | 2.157 | 2.372 | 2.382 | 2.288 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.154 | 3.394 | 4.795 | 5.197 | 5.713 | 5.573 | 5.873 | 5.323 | 5.838 | 5.699 | 5.948 | ns |
| | | GCLK PLL | $t_{co}$ | 1.330 | 1.509 | 1.951 | 2.048 | 2.261 | 2.272 | 2.298 | 2.155 | 2.370 | 2.380 | 2.286 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.154 | 3.395 | 4.798 | 5.202 | 5.718 | 5.578 | 5.878 | 5.327 | 5.844 | 5.705 | 5.954 | ns |
| | | GCLK PLL | $t_{co}$ | 1.330 | 1.510 | 1.954 | 2.053 | 2.266 | 2.277 | 2.303 | 2.159 | 2.376 | 2.386 | 2.292 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.158 | 3.398 | 4.795 | 5.197 | 5.712 | 5.572 | 5.872 | 5.322 | 5.837 | 5.698 | 5.947 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.513 | 1.951 | 2.048 | 2.260 | 2.271 | 2.297 | 2.154 | 2.369 | 2.379 | 2.285 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.184 | 3.427 | 4.840 | 5.245 | 5.762 | 5.622 | 5.922 | 5.370 | 5.887 | 5.748 | 5.997 | ns |
| | | GCLK PLL | $t_{co}$ | 1.360 | 1.542 | 1.996 | 2.096 | 2.310 | 2.321 | 2.347 | 2.202 | 2.419 | 2.429 | 2.335 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.170 | 3.413 | 4.828 | 5.234 | 5.752 | 5.612 | 5.912 | 5.360 | 5.878 | 5.739 | 5.988 | ns |
| | | GCLK PLL | $t_{co}$ | 1.346 | 1.528 | 1.984 | 2.085 | 2.300 | 2.311 | 2.337 | 2.192 | 2.410 | 2.420 | 2.326 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.158 | 3.400 | 4.811 | 5.216 | 5.734 | 5.594 | 5.894 | 5.342 | 5.860 | 5.721 | 5.970 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.515 | 1.967 | 2.067 | 2.282 | 2.293 | 2.319 | 2.174 | 2.392 | 2.402 | 2.308 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.158 | 3.400 | 4.814 | 5.220 | 5.738 | 5.598 | 5.898 | 5.346 | 5.865 | 5.726 | 5.975 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.515 | 1.970 | 2.071 | 2.286 | 2.297 | 2.323 | 2.178 | 2.397 | 2.407 | 2.313 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.154 | 3.396 | 4.807 | 5.212 | 5.731 | 5.591 | 5.891 | 5.339 | 5.857 | 5.718 | 5.967 | ns |
| | | GCLK PLL | $t_{co}$ | 1.330 | 1.511 | 1.963 | 2.063 | 2.279 | 2.290 | 2.316 | 2.171 | 2.389 | 2.399 | 2.305 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.158 | 3.398 | 4.800 | 5.203 | 5.719 | 5.579 | 5.879 | 5.328 | 5.844 | 5.705 | 5.954 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.513 | 1.956 | 2.054 | 2.267 | 2.278 | 2.304 | 2.160 | 2.376 | 2.386 | 2.292 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.159 | 3.400 | 4.808 | 5.213 | 5.730 | 5.590 | 5.890 | 5.338 | 5.856 | 5.717 | 5.966 | ns |
| | | GCLK PLL | $t_{co}$ | 1.335 | 1.515 | 1.964 | 2.064 | 2.278 | 2.289 | 2.315 | 2.170 | 2.388 | 2.398 | 2.304 | ns |

**Table 1–127.** EP3SE110 Column Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 0.9V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1V | $V_{CCL}$= 0.9V | |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.187 | 3.430 | 4.839 | 5.243 | 5.760 | 5.620 | 5.920 | 5.369 | 5.885 | 5.746 | 5.995 | ns |
| | | GCLK PLL | $t_{co}$ | 1.363 | 1.545 | 1.995 | 2.094 | 2.308 | 2.319 | 2.345 | 2.201 | 2.417 | 2.427 | 2.333 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.176 | 3.418 | 4.827 | 5.231 | 5.748 | 5.608 | 5.908 | 5.357 | 5.873 | 5.734 | 5.983 | ns |
| | | GCLK PLL | $t_{co}$ | 1.352 | 1.533 | 1.983 | 2.082 | 2.296 | 2.307 | 2.333 | 2.189 | 2.405 | 2.415 | 2.321 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.171 | 3.414 | 4.827 | 5.232 | 5.749 | 5.609 | 5.909 | 5.358 | 5.875 | 5.736 | 5.985 | ns |
| | | GCLK PLL | $t_{co}$ | 1.347 | 1.529 | 1.983 | 2.083 | 2.297 | 2.308 | 2.334 | 2.190 | 2.407 | 2.417 | 2.323 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.157 | 3.399 | 4.809 | 5.213 | 5.730 | 5.590 | 5.890 | 5.339 | 5.857 | 5.718 | 5.967 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.514 | 1.965 | 2.064 | 2.278 | 2.289 | 2.315 | 2.171 | 2.389 | 2.399 | 2.305 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.155 | 3.397 | 4.807 | 5.211 | 5.728 | 5.588 | 5.888 | 5.337 | 5.854 | 5.715 | 5.964 | ns |
| | | GCLK PLL | $t_{co}$ | 1.331 | 1.512 | 1.963 | 2.062 | 2.276 | 2.287 | 2.313 | 2.169 | 2.386 | 2.396 | 2.302 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.159 | 3.399 | 4.799 | 5.201 | 5.716 | 5.576 | 5.876 | 5.326 | 5.841 | 5.702 | 5.951 | ns |
| | | GCLK PLL | $t_{co}$ | 1.335 | 1.514 | 1.955 | 2.052 | 2.264 | 2.275 | 2.301 | 2.158 | 2.373 | 2.383 | 2.289 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.159 | 3.400 | 4.807 | 5.211 | 5.728 | 5.588 | 5.888 | 5.337 | 5.854 | 5.715 | 5.964 | ns |
| | | GCLK PLL | $t_{co}$ | 1.335 | 1.515 | 1.963 | 2.062 | 2.276 | 2.287 | 2.313 | 2.169 | 2.386 | 2.396 | 2.302 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.175 | 3.417 | 4.823 | 5.226 | 5.742 | 5.602 | 5.902 | 5.352 | 5.867 | 5.728 | 5.977 | ns |
| | | GCLK PLL | $t_{co}$ | 1.351 | 1.532 | 1.979 | 2.077 | 2.290 | 2.301 | 2.327 | 2.184 | 2.399 | 2.409 | 2.315 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.175 | 3.417 | 4.823 | 5.226 | 5.742 | 5.602 | 5.902 | 5.352 | 5.867 | 5.728 | 5.977 | ns |
| | | GCLK PLL | $t_{co}$ | 1.351 | 1.532 | 1.979 | 2.077 | 2.290 | 2.301 | 2.327 | 2.184 | 2.399 | 2.409 | 2.315 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.165 | 3.407 | 4.813 | 5.216 | 5.732 | 5.592 | 5.892 | 5.342 | 5.858 | 5.719 | 5.968 | ns |
| | | GCLK PLL | $t_{co}$ | 1.341 | 1.522 | 1.969 | 2.067 | 2.280 | 2.291 | 2.317 | 2.174 | 2.390 | 2.400 | 2.306 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.158 | 3.399 | 4.799 | 5.201 | 5.716 | 5.576 | 5.876 | 5.326 | 5.841 | 5.702 | 5.951 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.514 | 1.955 | 2.052 | 2.264 | 2.275 | 2.301 | 2.158 | 2.373 | 2.383 | 2.289 | ns |


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Table 1–128 lists the EP3SE110 row pins output timing parameters for differential I/O standards.

**Table 1–128.** EP3SE110 Row Pins Output Timing Parameters (Part 1 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | — | GCLK | $t_{co}$ | 2.744 | 2.932 | 4.083 | 4.440 | 4.901 | 4.771 | 5.049 | 4.540 | 5.002 | 4.873 | 5.107 | ns |
| | | GCLK PLL | $t_{co}$ | 0.931 | 1.057 | 1.249 | 1.300 | 1.458 | 1.480 | 1.486 | 1.382 | 1.545 | 1.563 | 1.456 | ns |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.136 | 3.376 | 4.754 | 5.156 | 5.664 | 5.526 | 5.797 | 5.281 | 5.790 | 5.652 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.511 | 1.930 | 2.026 | 2.231 | 2.245 | 2.243 | 2.133 | 2.343 | 2.352 | 2.229 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.118 | 3.366 | 4.792 | 5.202 | 5.718 | 5.580 | 5.851 | 5.332 | 5.851 | 5.713 | 5.932 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.501 | 1.968 | 2.072 | 2.285 | 2.299 | 2.297 | 2.184 | 2.404 | 2.413 | 2.290 | ns |
| MINI-LVDS | — | GCLK | $t_{co}$ | 2.744 | 2.932 | 4.083 | 4.440 | 4.901 | 4.771 | 5.049 | 4.540 | 5.002 | 4.873 | 5.107 | ns |
| | | GCLK PLL | $t_{co}$ | 0.931 | 1.057 | 1.249 | 1.300 | 1.458 | 1.480 | 1.486 | 1.382 | 1.545 | 1.563 | 1.456 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.136 | 3.376 | 4.754 | 5.156 | 5.664 | 5.526 | 5.797 | 5.281 | 5.790 | 5.652 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.511 | 1.930 | 2.026 | 2.231 | 2.245 | 2.243 | 2.133 | 2.343 | 2.352 | 2.229 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.118 | 3.366 | 4.792 | 5.202 | 5.718 | 5.580 | 5.851 | 5.332 | 5.851 | 5.713 | 5.932 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.501 | 1.968 | 2.072 | 2.285 | 2.299 | 2.297 | 2.184 | 2.404 | 2.413 | 2.290 | ns |
| RSDS | — | GCLK | $t_{co}$ | 2.744 | 2.932 | 4.083 | 4.440 | 4.901 | 4.771 | 5.049 | 4.540 | 5.002 | 4.873 | 5.107 | ns |
| | | GCLK PLL | $t_{co}$ | 0.931 | 1.057 | 1.249 | 1.300 | 1.458 | 1.480 | 1.486 | 1.382 | 1.545 | 1.563 | 1.456 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.136 | 3.376 | 4.754 | 5.156 | 5.664 | 5.526 | 5.797 | 5.281 | 5.790 | 5.652 | 5.871 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.511 | 1.930 | 2.026 | 2.231 | 2.245 | 2.243 | 2.133 | 2.343 | 2.352 | 2.229 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.118 | 3.366 | 4.792 | 5.202 | 5.718 | 5.580 | 5.851 | 5.332 | 5.851 | 5.713 | 5.932 | ns |
| | | GCLK PLL | $t_{co}$ | 1.315 | 1.501 | 1.968 | 2.072 | 2.285 | 2.299 | 2.297 | 2.184 | 2.404 | 2.413 | 2.290 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.162 | 3.409 | 4.828 | 5.236 | 5.751 | 5.613 | 5.884 | 5.365 | 5.880 | 5.742 | 5.961 | ns |
| | | GCLK PLL | $t_{co}$ | 1.359 | 1.544 | 2.004 | 2.106 | 2.318 | 2.332 | 2.330 | 2.217 | 2.433 | 2.442 | 2.319 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.148 | 3.395 | 4.815 | 5.223 | 5.738 | 5.600 | 5.871 | 5.351 | 5.867 | 5.729 | 5.948 | ns |
| | | GCLK PLL | $t_{co}$ | 1.345 | 1.530 | 1.991 | 2.093 | 2.305 | 2.319 | 2.317 | 2.203 | 2.420 | 2.429 | 2.306 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.144 | 3.391 | 4.813 | 5.223 | 5.739 | 5.601 | 5.872 | 5.351 | 5.869 | 5.731 | 5.950 | ns |
| | | GCLK PLL | $t_{co}$ | 1.341 | 1.526 | 1.989 | 2.093 | 2.306 | 2.320 | 2.318 | 2.203 | 2.422 | 2.431 | 2.308 | ns |

**Table 1–128.** EP3SE110 Row Pins Output Timing Parameters (Part 2 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.160 | 3.406 | 4.814 | 5.220 | 5.733 | 5.595 | 5.866 | 5.348 | 5.862 | 5.724 | 5.943 | ns |
| | | GCLK PLL | $t_{co}$ | 1.357 | 1.541 | 1.990 | 2.090 | 2.300 | 2.314 | 2.312 | 2.200 | 2.415 | 2.424 | 2.301 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.149 | 3.396 | 4.810 | 5.216 | 5.730 | 5.592 | 5.863 | 5.345 | 5.859 | 5.721 | 5.940 | ns |
| | | GCLK PLL | $t_{co}$ | 1.346 | 1.531 | 1.986 | 2.086 | 2.297 | 2.311 | 2.309 | 2.197 | 2.412 | 2.421 | 2.298 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.146 | 3.393 | 4.808 | 5.214 | 5.728 | 5.590 | 5.861 | 5.343 | 5.858 | 5.720 | 5.939 | ns |
| | | GCLK PLL | $t_{co}$ | 1.343 | 1.528 | 1.984 | 2.084 | 2.295 | 2.309 | 2.307 | 2.195 | 2.411 | 2.420 | 2.297 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.157 | 3.403 | 4.809 | 5.215 | 5.727 | 5.589 | 5.860 | 5.343 | 5.856 | 5.718 | 5.937 | ns |
| | | GCLK PLL | $t_{co}$ | 1.354 | 1.538 | 1.985 | 2.085 | 2.294 | 2.308 | 2.306 | 2.195 | 2.409 | 2.418 | 2.295 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.147 | 3.394 | 4.807 | 5.213 | 5.726 | 5.588 | 5.859 | 5.342 | 5.856 | 5.718 | 5.937 | ns |
| | | GCLK PLL | $t_{co}$ | 1.344 | 1.529 | 1.983 | 2.083 | 2.293 | 2.307 | 2.305 | 2.194 | 2.409 | 2.418 | 2.295 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.133 | 3.380 | 4.792 | 5.198 | 5.712 | 5.574 | 5.845 | 5.327 | 5.841 | 5.703 | 5.922 | ns |
| | | GCLK PLL | $t_{co}$ | 1.330 | 1.515 | 1.968 | 2.068 | 2.279 | 2.293 | 2.291 | 2.179 | 2.394 | 2.403 | 2.280 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.130 | 3.376 | 4.788 | 5.194 | 5.708 | 5.570 | 5.841 | 5.323 | 5.837 | 5.699 | 5.918 | ns |
| | | GCLK PLL | $t_{co}$ | 1.327 | 1.511 | 1.964 | 2.064 | 2.275 | 2.289 | 2.287 | 2.175 | 2.390 | 2.399 | 2.276 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.127 | 3.374 | 4.789 | 5.197 | 5.711 | 5.573 | 5.844 | 5.326 | 5.841 | 5.703 | 5.922 | ns |
| | | GCLK PLL | $t_{co}$ | 1.324 | 1.509 | 1.965 | 2.067 | 2.278 | 2.292 | 2.290 | 2.178 | 2.394 | 2.403 | 2.280 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.128 | 3.374 | 4.779 | 5.185 | 5.698 | 5.560 | 5.831 | 5.313 | 5.827 | 5.689 | 5.908 | ns |
| | | GCLK PLL | $t_{co}$ | 1.325 | 1.509 | 1.955 | 2.055 | 2.265 | 2.279 | 2.277 | 2.165 | 2.380 | 2.389 | 2.266 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.177 | 3.427 | 4.850 | 5.258 | 5.774 | 5.636 | 5.907 | 5.387 | 5.903 | 5.765 | 5.984 | ns |
| | | GCLK PLL | $t_{co}$ | 1.374 | 1.562 | 2.026 | 2.128 | 2.341 | 2.355 | 2.353 | 2.239 | 2.456 | 2.465 | 2.342 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.153 | 3.403 | 4.832 | 5.241 | 5.757 | 5.619 | 5.890 | 5.370 | 5.888 | 5.750 | 5.969 | ns |
| | | GCLK PLL | $t_{co}$ | 1.350 | 1.538 | 2.008 | 2.111 | 2.324 | 2.338 | 2.336 | 2.222 | 2.441 | 2.450 | 2.327 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.136 | 3.384 | 4.810 | 5.219 | 5.735 | 5.597 | 5.868 | 5.348 | 5.866 | 5.728 | 5.947 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.519 | 1.986 | 2.089 | 2.302 | 2.316 | 2.314 | 2.200 | 2.419 | 2.428 | 2.305 | ns |


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**Table 1–128.** EP3SE110 Row Pins Output Timing Parameters (Part 3 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.181 | 3.430 | 4.850 | 5.258 | 5.773 | 5.635 | 5.906 | 5.387 | 5.903 | 5.765 | 5.984 | ns |
| | | GCLK PLL | $t_{co}$ | 1.378 | 1.565 | 2.026 | 2.128 | 2.340 | 2.354 | 2.352 | 2.239 | 2.456 | 2.465 | 2.342 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.166 | 3.415 | 4.836 | 5.243 | 5.758 | 5.620 | 5.891 | 5.372 | 5.888 | 5.750 | 5.969 | ns |
| | | GCLK PLL | $t_{co}$ | 1.363 | 1.550 | 2.012 | 2.113 | 2.325 | 2.339 | 2.337 | 2.224 | 2.441 | 2.450 | 2.327 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.155 | 3.404 | 4.831 | 5.240 | 5.755 | 5.617 | 5.888 | 5.369 | 5.886 | 5.748 | 5.967 | ns |
| | | GCLK PLL | $t_{co}$ | 1.352 | 1.539 | 2.007 | 2.110 | 2.322 | 2.336 | 2.334 | 2.221 | 2.439 | 2.448 | 2.325 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.135 | 3.384 | 4.808 | 5.216 | 5.732 | 5.594 | 5.865 | 5.346 | 5.862 | 5.724 | 5.943 | ns |
| | | GCLK PLL | $t_{co}$ | 1.332 | 1.519 | 1.984 | 2.086 | 2.299 | 2.313 | 2.311 | 2.198 | 2.415 | 2.424 | 2.301 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.132 | 3.380 | 4.804 | 5.213 | 5.728 | 5.590 | 5.861 | 5.342 | 5.859 | 5.721 | 5.940 | ns |
| | | GCLK PLL | $t_{co}$ | 1.329 | 1.515 | 1.980 | 2.083 | 2.295 | 2.309 | 2.307 | 2.194 | 2.412 | 2.421 | 2.298 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.137 | 3.384 | 4.795 | 5.201 | 5.714 | 5.576 | 5.847 | 5.329 | 5.843 | 5.705 | 5.924 | ns |
| | | GCLK PLL | $t_{co}$ | 1.334 | 1.519 | 1.971 | 2.071 | 2.281 | 2.295 | 2.293 | 2.181 | 2.396 | 2.405 | 2.282 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.130 | 3.377 | 4.794 | 5.202 | 5.717 | 5.579 | 5.850 | 5.332 | 5.848 | 5.710 | 5.929 | ns |
| | | GCLK PLL | $t_{co}$ | 1.327 | 1.512 | 1.970 | 2.072 | 2.284 | 2.298 | 2.296 | 2.184 | 2.401 | 2.410 | 2.287 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.168 | 3.416 | 4.832 | 5.239 | 5.753 | 5.615 | 5.886 | 5.368 | 5.883 | 5.745 | 5.964 | ns |
| | | GCLK PLL | $t_{co}$ | 1.365 | 1.551 | 2.008 | 2.109 | 2.320 | 2.334 | 2.332 | 2.220 | 2.436 | 2.445 | 2.322 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.150 | 3.399 | 4.817 | 5.224 | 5.738 | 5.600 | 5.871 | 5.353 | 5.868 | 5.730 | 5.949 | ns |
| | | GCLK PLL | $t_{co}$ | 1.347 | 1.534 | 1.993 | 2.094 | 2.305 | 2.319 | 2.317 | 2.205 | 2.421 | 2.430 | 2.307 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.136 | 3.383 | 4.794 | 5.200 | 5.713 | 5.575 | 5.846 | 5.329 | 5.843 | 5.705 | 5.924 | ns |
| | | GCLK PLL | $t_{co}$ | 1.333 | 1.518 | 1.970 | 2.070 | 2.280 | 2.294 | 2.292 | 2.181 | 2.396 | 2.405 | 2.282 | ns |

Table 1–129 and Table 1–130 list the EP3SE110 regional clock (RCLK) adder values that must be added to the GCLK values. Use these adder values to determine I/O timing when the I/O pin is driven using the regional clock. This applies to all I/O standards supported by Stratix III devices.

Table 1–129 lists the EP3SE110 column pin delay adders when using the regional clock.

**Table 1–129.** EP3SE110 Column Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.111 | 0.14 | 0.19 | 0.103 | 0.105 | 0.103 | 0.177 | 0.085 | 0.101 | 0.098 | 0.146 | ns |
| RCLK PLL input adder | 2.506 | 2.513 | 3.782 | 4.081 | 4.579 | 4.381 | 4.923 | 4.222 | 4.603 | 4.401 | 4.984 | ns |
| RCLK output adder | -0.281 | -0.062 | -0.079 | -0.074 | -0.074 | -0.072 | -0.128 | 0.056 | 0.051 | 0.054 | -0.055 | ns |
| RCLK PLL output adder | -2.121 | -1.833 | -2.75 | -2.908 | -3.127 | -3.057 | -3.165 | -2.959 | -3.157 | -2.903 | -3.172 | ns |

Table 1–130 lists the EP3SE110 row pin delay adders when using the regional clock.

**Table 1–130.** EP3SE110 Row Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | -0.003 | -0.002 | 0.001 | -0.012 | -0.01 | -0.017 | 0.078 | -0.02 | -0.02 | -0.016 | 0.08 | ns |
| RCLK PLL input adder | 0.116 | 0.122 | 0.192 | 0.212 | 0.227 | 0.217 | 0.375 | 0.198 | 0.219 | 0.209 | 0.379 | ns |
| RCLK output adder | 0.02 | 0.019 | 0.027 | 0.041 | 0.044 | 0.048 | -0.038 | 0.051 | 0.057 | 0.051 | -0.04 | ns |
| RCLK PLL output adder | -0.103 | -0.105 | -0.162 | -0.179 | -0.194 | -0.185 | -0.322 | -0.167 | -0.183 | -0.175 | -0.324 | ns |

## EP3SE260 I/O Timing Parameters

Table 1–131 through Table 1–135 list the maximum I/O timing parameters for EP3SE260 devices for single-ended I/O standards.

Table 1–131 lists the EP3SE260 column pins input timing parameters for single-ended I/O standards.

**Table 1–131.** EP3SE260 Column Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -1.242 | -1.186 | -1.822 | -1.915 | -2.184 | -2.050 | -2.482 | -1.915 | -2.184 | -2.050 | -2.482 | ns |
| | | $t_h$ | 1.388 | 1.332 | 2.045 | 2.146 | 2.437 | 2.285 | 2.724 | 2.146 | 2.437 | 2.285 | 2.724 | ns |
| | GCLK PLL | $t_{su}$ | -1.417 | -1.465 | -2.238 | -2.189 | -2.558 | -2.477 | -3.038 | -2.189 | -2.558 | -2.477 | -3.038 | ns |
| | | $t_h$ | 1.732 | 1.778 | 2.727 | 2.697 | 3.113 | 3.000 | 3.584 | 2.697 | 3.113 | 3.000 | 3.584 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -1.242 | -1.186 | -1.822 | -1.915 | -2.184 | -2.050 | -2.482 | -1.915 | -2.184 | -2.050 | -2.482 | ns |
| | | $t_h$ | 1.388 | 1.332 | 2.045 | 2.146 | 2.437 | 2.285 | 2.724 | 2.146 | 2.437 | 2.285 | 2.724 | ns |
| | GCLK PLL | $t_{su}$ | -1.417 | -1.465 | -2.238 | -2.189 | -2.558 | -2.477 | -3.038 | -2.189 | -2.558 | -2.477 | -3.038 | ns |
| | | $t_h$ | 1.732 | 1.778 | 2.727 | 2.697 | 3.113 | 3.000 | 3.584 | 2.697 | 3.113 | 3.000 | 3.584 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -1.253 | -1.197 | -1.821 | -1.917 | -2.183 | -2.049 | -2.481 | -1.917 | -2.183 | -2.049 | -2.481 | ns |
| | | $t_h$ | 1.399 | 1.343 | 2.044 | 2.148 | 2.436 | 2.284 | 2.723 | 2.148 | 2.436 | 2.284 | 2.723 | ns |
| | GCLK PLL | $t_{su}$ | -1.428 | -1.476 | -2.237 | -2.191 | -2.557 | -2.476 | -3.037 | -2.191 | -2.557 | -2.476 | -3.037 | ns |
| | | $t_h$ | 1.743 | 1.789 | 2.726 | 2.699 | 3.112 | 2.999 | 3.583 | 2.699 | 3.112 | 2.999 | 3.583 | ns |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -1.253 | -1.197 | -1.821 | -1.917 | -2.183 | -2.049 | -2.481 | -1.917 | -2.183 | -2.049 | -2.481 | ns |
| | | $t_h$ | 1.399 | 1.343 | 2.044 | 2.148 | 2.436 | 2.284 | 2.723 | 2.148 | 2.436 | 2.284 | 2.723 | ns |
| | GCLK PLL | $t_{su}$ | -1.428 | -1.476 | -2.237 | -2.191 | -2.557 | -2.476 | -3.037 | -2.191 | -2.557 | -2.476 | -3.037 | ns |
| | | $t_h$ | 1.743 | 1.789 | 2.726 | 2.699 | 3.112 | 2.999 | 3.583 | 2.699 | 3.112 | 2.999 | 3.583 | ns |
| 2.5 V | GCLK | $t_{su}$ | -1.248 | -1.192 | -1.830 | -1.929 | -2.202 | -2.068 | -2.500 | -1.929 | -2.202 | -2.068 | -2.500 | ns |
| | | $t_h$ | 1.394 | 1.338 | 2.053 | 2.160 | 2.455 | 2.303 | 2.742 | 2.160 | 2.455 | 2.303 | 2.742 | ns |
| | GCLK PLL | $t_{su}$ | -1.423 | -1.471 | -2.246 | -2.203 | -2.576 | -2.495 | -3.056 | -2.203 | -2.576 | -2.495 | -3.056 | ns |
| | | $t_h$ | 1.738 | 1.784 | 2.735 | 2.711 | 3.131 | 3.018 | 3.602 | 2.711 | 3.131 | 3.018 | 3.602 | ns |
| 1.8 V | GCLK | $t_{su}$ | -1.270 | -1.214 | -1.870 | -1.965 | -2.200 | -2.066 | -2.498 | -1.965 | -2.200 | -2.066 | -2.498 | ns |
| | | $t_h$ | 1.418 | 1.362 | 2.093 | 2.196 | 2.453 | 2.301 | 2.740 | 2.196 | 2.453 | 2.301 | 2.740 | ns |
| | GCLK PLL | $t_{su}$ | -1.443 | -1.493 | -2.286 | -2.239 | -2.574 | -2.493 | -3.054 | -2.239 | -2.574 | -2.493 | -3.054 | ns |
| | | $t_h$ | 1.760 | 1.808 | 2.775 | 2.747 | 3.129 | 3.016 | 3.600 | 2.747 | 3.129 | 3.016 | 3.600 | ns |
| 1.5 V | GCLK | $t_{su}$ | -1.260 | -1.204 | -1.847 | -1.933 | -2.130 | -1.996 | -2.428 | -1.933 | -2.130 | -1.996 | -2.428 | ns |
| | | $t_h$ | 1.408 | 1.352 | 2.070 | 2.164 | 2.383 | 2.231 | 2.670 | 2.164 | 2.383 | 2.231 | 2.670 | ns |
| | GCLK PLL | $t_{su}$ | -1.433 | -1.483 | -2.263 | -2.207 | -2.504 | -2.423 | -2.984 | -2.207 | -2.504 | -2.423 | -2.984 | ns |
| | | $t_h$ | 1.750 | 1.798 | 2.752 | 2.715 | 3.059 | 2.946 | 3.530 | 2.715 | 3.059 | 2.946 | 3.530 | ns |
| 1.2 V | GCLK | $t_{su}$ | -1.208 | -1.152 | -1.770 | -1.834 | -1.974 | -1.840 | -2.272 | -1.834 | -1.974 | -1.840 | -2.272 | ns |
| | | $t_h$ | 1.356 | 1.300 | 1.993 | 2.065 | 2.227 | 2.075 | 2.514 | 2.065 | 2.227 | 2.075 | 2.514 | ns |
| | GCLK PLL | $t_{su}$ | -1.381 | -1.431 | -2.186 | -2.108 | -2.348 | -2.267 | -2.828 | -2.108 | -2.348 | -2.267 | -2.828 | ns |
| | | $t_h$ | 1.698 | 1.746 | 2.675 | 2.616 | 2.903 | 2.790 | 3.374 | 2.616 | 2.903 | 2.790 | 3.374 | ns |

**Table 1–131.** EP3SE260 Column Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -1.179 | -1.123 | -1.742 | -1.818 | -1.976 | -1.842 | -2.274 | -1.818 | -1.976 | -1.842 | -2.274 | ns |
| | | $t_h$ | 1.327 | 1.271 | 1.965 | 2.049 | 2.229 | 2.077 | 2.516 | 2.049 | 2.229 | 2.077 | 2.516 | ns |
| | GCLK PLL | $t_{su}$ | -1.352 | -1.402 | -2.158 | -2.092 | -2.350 | -2.269 | -2.830 | -2.092 | -2.350 | -2.269 | -2.830 | ns |
| | | $t_h$ | 1.669 | 1.717 | 2.647 | 2.600 | 2.905 | 2.792 | 3.376 | 2.600 | 2.905 | 2.792 | 3.376 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | -1.179 | -1.123 | -1.742 | -1.818 | -1.976 | -1.842 | -2.274 | -1.818 | -1.976 | -1.842 | -2.274 | ns |
| | | $t_h$ | 1.327 | 1.271 | 1.965 | 2.049 | 2.229 | 2.077 | 2.516 | 2.049 | 2.229 | 2.077 | 2.516 | ns |
| | GCLK PLL | $t_{su}$ | -1.352 | -1.402 | -2.158 | -2.092 | -2.350 | -2.269 | -2.830 | -2.092 | -2.350 | -2.269 | -2.830 | ns |
| | | $t_h$ | 1.669 | 1.717 | 2.647 | 2.600 | 2.905 | 2.792 | 3.376 | 2.600 | 2.905 | 2.792 | 3.376 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | -1.173 | -1.117 | -1.729 | -1.810 | -1.973 | -1.837 | -2.272 | -1.810 | -1.973 | -1.837 | -2.272 | ns |
| | | $t_h$ | 1.321 | 1.265 | 1.952 | 2.038 | 2.223 | 2.071 | 2.509 | 2.038 | 2.223 | 2.071 | 2.509 | ns |
| | GCLK PLL | $t_{su}$ | -1.346 | -1.396 | -2.145 | -2.087 | -2.347 | -2.264 | -2.828 | -2.087 | -2.347 | -2.264 | -2.828 | ns |
| | | $t_h$ | 1.663 | 1.711 | 2.634 | 2.592 | 2.899 | 2.786 | 3.369 | 2.592 | 2.899 | 2.786 | 3.369 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -1.173 | -1.117 | -1.729 | -1.810 | -1.973 | -1.837 | -2.272 | -1.810 | -1.973 | -1.837 | -2.272 | ns |
| | | $t_h$ | 1.321 | 1.265 | 1.952 | 2.038 | 2.223 | 2.071 | 2.509 | 2.038 | 2.223 | 2.071 | 2.509 | ns |
| | GCLK PLL | $t_{su}$ | -1.346 | -1.396 | -2.145 | -2.087 | -2.347 | -2.264 | -2.828 | -2.087 | -2.347 | -2.264 | -2.828 | ns |
| | | $t_h$ | 1.663 | 1.711 | 2.634 | 2.592 | 2.899 | 2.786 | 3.369 | 2.592 | 2.899 | 2.786 | 3.369 | ns |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | -1.162 | -1.106 | -1.718 | -1.799 | -1.954 | -1.818 | -2.253 | -1.799 | -1.954 | -1.818 | -2.253 | ns |
| | | $t_h$ | 1.310 | 1.254 | 1.940 | 2.027 | 2.204 | 2.052 | 2.490 | 2.027 | 2.204 | 2.052 | 2.490 | ns |
| | GCLK PLL | $t_{su}$ | -1.335 | -1.385 | -2.134 | -2.076 | -2.328 | -2.245 | -2.809 | -2.076 | -2.328 | -2.245 | -2.809 | ns |
| | | $t_h$ | 1.652 | 1.700 | 2.622 | 2.581 | 2.880 | 2.767 | 3.350 | 2.581 | 2.880 | 2.767 | 3.350 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -1.162 | -1.106 | -1.718 | -1.799 | -1.954 | -1.818 | -2.253 | -1.799 | -1.954 | -1.818 | -2.253 | ns |
| | | $t_h$ | 1.310 | 1.254 | 1.940 | 2.027 | 2.204 | 2.052 | 2.490 | 2.027 | 2.204 | 2.052 | 2.490 | ns |
| | GCLK PLL | $t_{su}$ | -1.335 | -1.385 | -2.134 | -2.076 | -2.328 | -2.245 | -2.809 | -2.076 | -2.328 | -2.245 | -2.809 | ns |
| | | $t_h$ | 1.652 | 1.700 | 2.622 | 2.581 | 2.880 | 2.767 | 3.350 | 2.581 | 2.880 | 2.767 | 3.350 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -1.173 | -1.117 | -1.729 | -1.810 | -1.973 | -1.837 | -2.272 | -1.810 | -1.973 | -1.837 | -2.272 | ns |
| | | $t_h$ | 1.321 | 1.265 | 1.952 | 2.038 | 2.223 | 2.071 | 2.509 | 2.038 | 2.223 | 2.071 | 2.509 | ns |
| | GCLK PLL | $t_{su}$ | -1.346 | -1.396 | -2.145 | -2.087 | -2.347 | -2.264 | -2.828 | -2.087 | -2.347 | -2.264 | -2.828 | ns |
| | | $t_h$ | 1.663 | 1.711 | 2.634 | 2.592 | 2.899 | 2.786 | 3.369 | 2.592 | 2.899 | 2.786 | 3.369 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -1.173 | -1.117 | -1.729 | -1.810 | -1.973 | -1.837 | -2.272 | -1.810 | -1.973 | -1.837 | -2.272 | ns |
| | | $t_h$ | 1.321 | 1.265 | 1.952 | 2.038 | 2.223 | 2.071 | 2.509 | 2.038 | 2.223 | 2.071 | 2.509 | ns |
| | GCLK PLL | $t_{su}$ | -1.346 | -1.396 | -2.145 | -2.087 | -2.347 | -2.264 | -2.828 | -2.087 | -2.347 | -2.264 | -2.828 | ns |
| | | $t_h$ | 1.663 | 1.711 | 2.634 | 2.592 | 2.899 | 2.786 | 3.369 | 2.592 | 2.899 | 2.786 | 3.369 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -1.162 | -1.106 | -1.718 | -1.799 | -1.954 | -1.818 | -2.253 | -1.799 | -1.954 | -1.818 | -2.253 | ns |
| | | $t_h$ | 1.310 | 1.254 | 1.940 | 2.027 | 2.204 | 2.052 | 2.490 | 2.027 | 2.204 | 2.052 | 2.490 | ns |
| | GCLK PLL | $t_{su}$ | -1.335 | -1.385 | -2.134 | -2.076 | -2.328 | -2.245 | -2.809 | -2.076 | -2.328 | -2.245 | -2.809 | ns |
| | | $t_h$ | 1.652 | 1.700 | 2.622 | 2.581 | 2.880 | 2.767 | 3.350 | 2.581 | 2.880 | 2.767 | 3.350 | ns |

**Table 1–131.** EP3SE260 Column Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -1.162 | -1.106 | -1.718 | -1.799 | -1.954 | -1.818 | -2.253 | -1.799 | -1.954 | -1.818 | -2.253 | ns |
| | | $t_h$ | 1.310 | 1.254 | 1.940 | 2.027 | 2.204 | 2.052 | 2.490 | 2.027 | 2.204 | 2.052 | 2.490 | ns |
| | GCLK PLL | $t_{su}$ | -1.335 | -1.385 | -2.134 | -2.076 | -2.328 | -2.245 | -2.809 | -2.076 | -2.328 | -2.245 | -2.809 | ns |
| | | $t_h$ | 1.652 | 1.700 | 2.622 | 2.581 | 2.880 | 2.767 | 3.350 | 2.581 | 2.880 | 2.767 | 3.350 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -1.150 | -1.094 | -1.708 | -1.788 | -1.938 | -1.802 | -2.237 | -1.788 | -1.938 | -1.802 | -2.237 | ns |
| | | $t_h$ | 1.298 | 1.242 | 1.930 | 2.016 | 2.188 | 2.036 | 2.474 | 2.016 | 2.188 | 2.036 | 2.474 | ns |
| | GCLK PLL | $t_{su}$ | -1.323 | -1.373 | -2.124 | -2.065 | -2.312 | -2.229 | -2.793 | -2.065 | -2.312 | -2.229 | -2.793 | ns |
| | | $t_h$ | 1.640 | 1.688 | 2.612 | 2.570 | 2.864 | 2.751 | 3.334 | 2.570 | 2.864 | 2.751 | 3.334 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | -1.150 | -1.094 | -1.708 | -1.788 | -1.938 | -1.802 | -2.237 | -1.788 | -1.938 | -1.802 | -2.237 | ns |
| | | $t_h$ | 1.298 | 1.242 | 1.930 | 2.016 | 2.188 | 2.036 | 2.474 | 2.016 | 2.188 | 2.036 | 2.474 | ns |
| | GCLK PLL | $t_{su}$ | -1.323 | -1.373 | -2.124 | -2.065 | -2.312 | -2.229 | -2.793 | -2.065 | -2.312 | -2.229 | -2.793 | ns |
| | | $t_h$ | 1.640 | 1.688 | 2.612 | 2.570 | 2.864 | 2.751 | 3.334 | 2.570 | 2.864 | 2.751 | 3.334 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | -1.253 | -1.197 | -1.821 | -1.917 | -2.183 | -2.049 | -2.481 | -1.917 | -2.183 | -2.049 | -2.481 | ns |
| | | $t_h$ | 1.399 | 1.343 | 2.044 | 2.148 | 2.436 | 2.284 | 2.723 | 2.148 | 2.436 | 2.284 | 2.723 | ns |
| | GCLK PLL | $t_{su}$ | -1.428 | -1.476 | -2.237 | -2.191 | -2.557 | -2.476 | -3.037 | -2.191 | -2.557 | -2.476 | -3.037 | ns |
| | | $t_h$ | 1.743 | 1.789 | 2.726 | 2.699 | 3.112 | 2.999 | 3.583 | 2.699 | 3.112 | 2.999 | 3.583 | ns |

Table 1–132 lists the EP3SE260 row pins input timing parameters for single-ended I/O standards.

**Table 1–132.** EP3SE260 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | GCLK | $t_{su}$ | -1.219 | -1.374 | -2.059 | -1.988 | -2.283 | -2.177 | -2.643 | -2.003 | -2.382 | -2.177 | -2.643 | ns |
| | | $t_h$ | 1.355 | 1.524 | 1.749 | 1.864 | 1.862 | 1.767 | 1.884 | 1.864 | 1.883 | 1.767 | 1.884 | ns |
| | GCLK PLL | $t_{su}$ | 0.983 | 0.983 | 2.293 | 2.233 | 2.553 | 2.431 | 2.902 | 2.260 | 2.659 | 2.431 | 2.902 | ns |
| | | $t_h$ | -0.704 | -0.685 | -2.059 | -1.988 | -2.283 | -2.177 | -2.643 | -2.003 | -2.382 | -2.177 | -2.643 | ns |
| 3.3-V LVCMOS | GCLK | $t_{su}$ | -1.219 | -1.374 | -2.059 | -1.988 | -2.283 | -2.177 | -2.643 | -2.003 | -2.382 | -2.177 | -2.643 | ns |
| | | $t_h$ | 1.355 | 1.524 | 1.749 | 1.864 | 1.862 | 1.767 | 1.884 | 1.864 | 1.883 | 1.767 | 1.884 | ns |
| | GCLK PLL | $t_{su}$ | 0.983 | 0.983 | 2.293 | 2.233 | 2.553 | 2.431 | 2.902 | 2.260 | 2.659 | 2.431 | 2.902 | ns |
| | | $t_h$ | -0.704 | -0.685 | -2.056 | -1.989 | -2.286 | -2.180 | -2.646 | -2.002 | -2.387 | -2.180 | -2.646 | ns |
| 3.0-V LVTTL | GCLK | $t_{su}$ | -1.225 | -1.385 | 2.290 | 2.234 | 2.556 | 2.434 | 2.905 | 2.259 | 2.664 | 2.434 | 2.905 | ns |
| | | $t_h$ | 1.361 | 1.535 | -2.056 | -1.989 | -2.286 | -2.180 | -2.646 | -2.002 | -2.387 | -2.180 | -2.646 | ns |
| | GCLK PLL | $t_{su}$ | 0.977 | 0.972 | 1.752 | 1.863 | 1.859 | 1.764 | 1.881 | 1.865 | 1.878 | 1.764 | 1.881 | ns |
| | | $t_h$ | -0.698 | -0.674 | 2.290 | 2.234 | 2.556 | 2.434 | 2.905 | 2.259 | 2.664 | 2.434 | 2.905 | ns |

**Table 1–132.** EP3SE260 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVCMOS | GCLK | $t_{su}$ | -1.225 | -1.385 | 2.299 | 2.247 | 2.571 | 2.449 | 2.920 | 2.268 | 2.674 | 2.449 | 2.920 | ns |
| | | $t_h$ | 1.361 | 1.535 | -2.065 | -2.002 | -2.301 | -2.195 | -2.661 | -2.011 | -2.397 | -2.195 | -2.661 | ns |
| | GCLK PLL | $t_{su}$ | 0.977 | 0.972 | 1.743 | 1.850 | 1.844 | 1.749 | 1.866 | 1.856 | 1.868 | 1.749 | 1.866 | ns |
| | | $t_h$ | -0.698 | -0.674 | 2.299 | 2.247 | 2.571 | 2.449 | 2.920 | 2.268 | 2.674 | 2.449 | 2.920 | ns |
| 2.5 V | GCLK | $t_{su}$ | -1.213 | -1.378 | 1.617 | 1.714 | 1.860 | 1.741 | 1.759 | 1.830 | 1.861 | 1.741 | 1.759 | ns |
| | | $t_h$ | 1.349 | 1.528 | 2.364 | 2.410 | 2.627 | 2.565 | 3.018 | 2.344 | 2.687 | 2.565 | 3.018 | ns |
| | GCLK PLL | $t_{su}$ | 0.989 | 0.979 | -2.130 | -2.167 | -2.360 | -2.314 | -2.765 | -2.088 | -2.409 | -2.314 | -2.765 | ns |
| | | $t_h$ | -0.710 | -0.681 | 1.617 | 1.714 | 1.860 | 1.741 | 1.759 | 1.830 | 1.861 | 1.741 | 1.759 | ns |
| 1.8 V | GCLK | $t_{su}$ | -1.283 | -1.435 | 1.641 | 1.746 | 1.928 | 1.809 | 1.827 | 1.861 | 1.926 | 1.809 | 1.827 | ns |
| | | $t_h$ | 0.968 | 0.896 | 2.340 | 2.378 | 2.559 | 2.497 | 2.950 | 2.313 | 2.622 | 2.497 | 2.950 | ns |
| | GCLK PLL | $t_{su}$ | 1.421 | 1.586 | -2.106 | -2.135 | -2.292 | -2.246 | -2.697 | -2.057 | -2.344 | -2.246 | -2.697 | ns |
| | | $t_h$ | -1.273 | -1.424 | 1.720 | 1.847 | 2.087 | 1.968 | 1.986 | 1.957 | 2.081 | 1.968 | 1.986 | ns |
| 1.5 V | GCLK | $t_{su}$ | 0.978 | 0.907 | 2.261 | 2.277 | 2.400 | 2.338 | 2.791 | 2.217 | 2.467 | 2.338 | 2.791 | ns |
| | | $t_h$ | 1.411 | 1.575 | -2.027 | -2.034 | -2.133 | -2.087 | -2.538 | -1.961 | -2.189 | -2.087 | -2.538 | ns |
| | GCLK PLL | $t_{su}$ | -1.213 | -1.371 | 1.829 | 1.959 | 2.064 | 1.969 | 2.086 | 1.968 | 2.085 | 1.969 | 2.086 | ns |
| | | $t_h$ | 1.038 | 0.960 | 2.213 | 2.138 | 2.351 | 2.229 | 2.700 | 2.156 | 2.457 | 2.229 | 2.700 | ns |
| 1.2 V | GCLK | $t_{su}$ | 1.351 | 1.522 | -1.989 | -2.007 | -2.128 | -2.081 | -2.534 | -1.932 | -2.182 | -2.081 | -2.534 | ns |
| | | $t_h$ | -1.155 | -1.320 | 1.758 | -2.007 | -2.128 | -2.081 | -2.534 | -1.932 | -2.182 | -2.081 | -2.534 | ns |
| | GCLK PLL | $t_{su}$ | 1.047 | 1.038 | 2.223 | 2.248 | 2.393 | 2.331 | 2.783 | 2.185 | 2.457 | 2.331 | 2.783 | ns |
| | | $t_h$ | 1.292 | 1.471 | -1.989 | 1.874 | 2.092 | 1.974 | 1.990 | 1.986 | 2.088 | 1.974 | 1.990 | ns |
| SSTL-2 CLASS I | GCLK | $t_{su}$ | -1.155 | -1.320 | 1.758 | 1.874 | 2.092 | 1.974 | 1.990 | 1.986 | 2.088 | 1.974 | 1.990 | ns |
| | | $t_h$ | 1.047 | 1.038 | 2.223 | -1.378 | -1.541 | -1.455 | -1.458 | -1.477 | -1.526 | -1.455 | -1.458 | ns |
| | GCLK PLL | $t_{su}$ | 1.292 | 1.471 | -1.989 | -2.007 | -2.128 | -2.081 | -2.534 | -1.932 | -2.182 | -2.081 | -2.534 | ns |
| | | $t_h$ | -1.187 | -1.336 | 1.758 | 2.248 | 2.393 | 2.331 | 2.783 | 2.185 | 2.457 | 2.331 | 2.783 | ns |
| SSTL-2 CLASS II | GCLK | $t_{su}$ | 1.064 | 0.995 | 2.223 | 1.874 | 2.092 | 1.974 | 1.990 | 1.986 | 2.088 | 1.974 | 1.990 | ns |
| | | $t_h$ | 1.325 | 1.487 | -1.989 | -1.378 | -1.541 | -1.455 | -1.458 | -1.477 | -1.526 | -1.455 | -1.458 | ns |
| | GCLK PLL | $t_{su}$ | -1.187 | -1.336 | -1.294 | -1.997 | -2.110 | -2.063 | -2.516 | -1.921 | -2.165 | -2.063 | -2.516 | ns |
| | | $t_h$ | 1.064 | 0.995 | -1.974 | 2.238 | 2.375 | 2.313 | 2.765 | 2.174 | 2.440 | 2.313 | 2.765 | ns |
| SSTL-18 CLASS I | GCLK | $t_{su}$ | 1.325 | 1.487 | 2.209 | 1.884 | 2.110 | 1.992 | 2.008 | 1.997 | 2.105 | 1.992 | 2.008 | ns |
| | | $t_h$ | -1.173 | -1.324 | 1.758 | 1.884 | 2.110 | 1.992 | 2.008 | 1.997 | 2.105 | 1.992 | 2.008 | ns |
| | GCLK PLL | $t_{su}$ | 1.078 | 1.007 | 2.223 | -1.388 | -1.559 | -1.473 | -1.476 | -1.488 | -1.543 | -1.473 | -1.476 | ns |
| | | $t_h$ | 1.311 | 1.475 | -1.989 | -1.997 | -2.110 | -2.063 | -2.516 | -1.921 | -2.165 | -2.063 | -2.516 | ns |
| SSTL-18 CLASS II | GCLK | $t_{su}$ | -1.187 | -1.336 | 1.758 | -1.378 | -1.541 | -1.455 | -1.458 | -1.477 | -1.526 | -1.455 | -1.458 | ns |
| | | $t_h$ | 1.064 | 0.995 | 2.223 | -2.007 | -2.128 | -2.081 | -2.534 | -1.932 | -2.182 | -2.081 | -2.534 | ns |
| | GCLK PLL | $t_{su}$ | 1.325 | 1.487 | -1.989 | 2.248 | 2.393 | 2.331 | 2.783 | 2.185 | 2.457 | 2.331 | 2.783 | ns |
| | | $t_h$ | -1.187 | -1.336 | -1.294 | 1.874 | 2.092 | 1.974 | 1.990 | 1.986 | 2.088 | 1.974 | 1.990 | ns |

**Table 1–132.** EP3SE260 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-15 CLASS I | GCLK | $t_{su}$ | 1.064 | 0.995 | -1.974 | -1.378 | -1.541 | -1.455 | -1.458 | -1.477 | -1.526 | -1.455 | -1.458 | ns |
| | | $t_h$ | 1.325 | 1.487 | 2.209 | -2.007 | -2.128 | -2.081 | -2.534 | -1.932 | -2.182 | -2.081 | -2.534 | ns |
| | GCLK PLL | $t_{su}$ | -1.173 | -1.324 | 1.773 | 2.248 | 2.393 | 2.331 | 2.783 | 2.185 | 2.457 | 2.331 | 2.783 | ns |
| | | $t_h$ | 1.078 | 1.007 | -1.294 | 1.874 | 2.092 | 1.974 | 1.990 | 1.986 | 2.088 | 1.974 | 1.990 | ns |
| 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | 1.311 | 1.475 | -1.974 | -1.378 | -1.541 | -1.455 | -1.458 | -1.477 | -1.526 | -1.455 | -1.458 | ns |
| | | $t_h$ | -1.173 | -1.324 | -1.303 | 1.884 | 2.110 | 1.992 | 2.008 | 1.997 | 2.105 | 1.992 | 2.008 | ns |
| | GCLK PLL | $t_{su}$ | 1.078 | 1.007 | -1.965 | -1.388 | -1.559 | -1.473 | -1.476 | -1.488 | -1.543 | -1.473 | -1.476 | ns |
| | | $t_h$ | 1.311 | 1.475 | 2.200 | -1.997 | -2.110 | -2.063 | -2.516 | -1.921 | -2.165 | -2.063 | -2.516 | ns |
| 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -1.164 | -1.312 | 1.782 | 2.238 | 2.375 | 2.313 | 2.765 | 2.174 | 2.440 | 2.313 | 2.765 | ns |
| | | $t_h$ | 1.087 | 1.019 | -1.303 | 1.884 | 2.110 | 1.992 | 2.008 | 1.997 | 2.105 | 1.992 | 2.008 | ns |
| | GCLK PLL | $t_{su}$ | 1.302 | 1.463 | -1.965 | -1.388 | -1.559 | -1.473 | -1.476 | -1.488 | -1.543 | -1.473 | -1.476 | ns |
| | | $t_h$ | -1.164 | -1.312 | -1.303 | 1.894 | 2.126 | 2.008 | 2.024 | 2.006 | 2.121 | 2.008 | 2.024 | ns |
| 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | 1.087 | 1.019 | -2.056 | -1.398 | -1.575 | -1.489 | -1.492 | -1.497 | -1.559 | -1.489 | -1.492 | ns |
| | | $t_h$ | 1.302 | 1.463 | 1.752 | -1.987 | -2.094 | -2.047 | -2.500 | -1.912 | -2.149 | -2.047 | -2.500 | ns |
| | GCLK PLL | $t_{su}$ | -1.225 | -1.385 | 2.290 | 2.228 | 2.359 | 2.297 | 2.749 | 2.165 | 2.424 | 2.297 | 2.749 | ns |
| | | $t_h$ | 1.361 | 1.535 | -2.056 | 1.894 | 2.126 | 2.008 | 2.024 | 2.006 | 2.121 | 2.008 | 2.024 | ns |
| 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | 0.977 | 0.972 | 1.752 | -1.398 | -1.575 | -1.489 | -1.492 | -1.497 | -1.559 | -1.489 | -1.492 | ns |
| | | $t_h$ | -0.698 | -0.674 | 2.290 | -1.987 | -2.094 | -2.047 | -2.500 | -1.912 | -2.149 | -2.047 | -2.500 | ns |
| | GCLK PLL | $t_{su}$ | -1.225 | -1.385 | 2.290 | 2.228 | 2.359 | 2.297 | 2.749 | 2.165 | 2.424 | 2.297 | 2.749 | ns |
| | | $t_h$ | 1.361 | 1.535 | 2.290 | 1.894 | 2.126 | 2.008 | 2.024 | 2.006 | 2.121 | 2.008 | 2.024 | ns |
| 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | 0.977 | 0.972 | 2.290 | -1.398 | -1.575 | -1.489 | -1.492 | -1.497 | -1.559 | -1.489 | -1.492 | ns |
| | | $t_h$ | -0.698 | -0.674 | 2.290 | -1.987 | -2.094 | -2.047 | -2.500 | -1.912 | -2.149 | -2.047 | -2.500 | ns |
| | GCLK PLL | $t_{su}$ | -1.219 | -1.374 | -2.059 | -1.988 | -2.283 | -2.177 | -2.643 | -2.003 | -2.382 | -2.177 | -2.643 | ns |
| | | $t_h$ | 1.355 | 1.524 | 1.749 | 1.864 | 1.862 | 1.767 | 1.884 | 1.864 | 1.883 | 1.767 | 1.884 | ns |
| 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | 0.983 | 0.983 | 2.293 | 2.233 | 2.553 | 2.431 | 2.902 | 2.260 | 2.659 | 2.431 | 2.902 | ns |
| | | $t_h$ | -0.704 | -0.685 | -2.059 | -1.988 | -2.283 | -2.177 | -2.643 | -2.003 | -2.382 | -2.177 | -2.643 | ns |
| | GCLK PLL | $t_{su}$ | -1.219 | -1.374 | -2.059 | -1.988 | -2.283 | -2.177 | -2.643 | -2.003 | -2.382 | -2.177 | -2.643 | ns |
| | | $t_h$ | 1.355 | 1.524 | 1.749 | 1.864 | 1.862 | 1.767 | 1.884 | 1.864 | 1.883 | 1.767 | 1.884 | ns |
| 3.0-V PCI | GCLK | $t_{su}$ | 0.983 | 0.983 | 2.293 | 2.233 | 2.553 | 2.431 | 2.902 | 2.260 | 2.659 | 2.431 | 2.902 | ns |
| | | $t_h$ | -0.704 | -0.685 | -2.056 | -1.989 | -2.286 | -2.180 | -2.646 | -2.002 | -2.387 | -2.180 | -2.646 | ns |
| | GCLK PLL | $t_{su}$ | -1.225 | -1.385 | 2.290 | 2.234 | 2.556 | 2.434 | 2.905 | 2.259 | 2.664 | 2.434 | 2.905 | ns |
| | | $t_h$ | 1.361 | 1.535 | -2.056 | -1.989 | -2.286 | -2.180 | -2.646 | -2.002 | -2.387 | -2.180 | -2.646 | ns |
| 3.0-V PCI-X | GCLK | $t_{su}$ | 0.977 | 0.972 | 1.752 | 1.863 | 1.859 | 1.764 | 1.881 | 1.865 | 1.878 | 1.764 | 1.881 | ns |
| | | $t_h$ | -0.698 | -0.674 | 2.290 | 2.234 | 2.556 | 2.434 | 2.905 | 2.259 | 2.664 | 2.434 | 2.905 | ns |
| | GCLK PLL | $t_{su}$ | -1.225 | -1.385 | 2.299 | 2.247 | 2.571 | 2.449 | 2.920 | 2.268 | 2.674 | 2.449 | 2.920 | ns |
| | | $t_h$ | 1.361 | 1.535 | -2.065 | -2.002 | -2.301 | -2.195 | -2.661 | -2.011 | -2.397 | -2.195 | -2.661 | ns |

Table 1–133 lists the EP3SE260 column pins output timing parameters for single-ended I/O standards.

**Table 1–133.** EP3SE260 Column Pins Output Timing Parameters (Part 1 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.644 | 3.677 | 5.302 | 5.460 | 6.139 | 5.837 | 6.259 | 5.460 | 6.139 | 5.837 | 6.259 | ns |
| | | GCLK PLL | $t_{co}$ | 4.087 | 4.076 | 5.937 | 6.144 | 6.701 | 6.529 | 7.188 | 6.144 | 6.701 | 6.529 | 7.188 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.577 | 3.610 | 5.193 | 5.349 | 5.969 | 5.724 | 6.146 | 5.349 | 5.969 | 5.724 | 6.146 | ns |
| | | GCLK PLL | $t_{co}$ | 4.020 | 4.009 | 5.828 | 6.033 | 6.588 | 6.416 | 7.018 | 6.033 | 6.588 | 6.416 | 7.018 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.491 | 3.524 | 5.089 | 5.250 | 5.817 | 5.632 | 6.054 | 5.250 | 5.817 | 5.632 | 6.054 | ns |
| | | GCLK PLL | $t_{co}$ | 3.934 | 3.923 | 5.724 | 5.934 | 6.496 | 6.324 | 6.866 | 5.934 | 6.496 | 6.324 | 6.866 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.484 | 3.517 | 5.072 | 5.222 | 5.792 | 5.591 | 6.013 | 5.222 | 5.792 | 5.591 | 6.013 | ns |
| | | GCLK PLL | $t_{co}$ | 3.927 | 3.916 | 5.707 | 5.906 | 6.455 | 6.283 | 6.841 | 5.906 | 6.455 | 6.283 | 6.841 | ns |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.650 | 3.683 | 5.306 | 5.465 | 6.153 | 5.844 | 6.266 | 5.465 | 6.153 | 5.844 | 6.266 | ns |
| | | GCLK PLL | $t_{co}$ | 4.093 | 4.082 | 5.941 | 6.149 | 6.708 | 6.536 | 7.202 | 6.149 | 6.708 | 6.536 | 7.202 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.495 | 3.528 | 5.099 | 5.267 | 5.823 | 5.643 | 6.065 | 5.267 | 5.823 | 5.643 | 6.065 | ns |
| | | GCLK PLL | $t_{co}$ | 3.938 | 3.927 | 5.734 | 5.951 | 6.507 | 6.335 | 6.872 | 5.951 | 6.507 | 6.335 | 6.872 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.502 | 3.535 | 5.093 | 5.246 | 5.792 | 5.617 | 6.039 | 5.246 | 5.792 | 5.617 | 6.039 | ns |
| | | GCLK PLL | $t_{co}$ | 3.945 | 3.934 | 5.728 | 5.930 | 6.481 | 6.309 | 6.841 | 5.930 | 6.481 | 6.309 | 6.841 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.486 | 3.519 | 5.071 | 5.221 | 5.735 | 5.588 | 6.010 | 5.221 | 5.735 | 5.588 | 6.010 | ns |
| | | GCLK PLL | $t_{co}$ | 3.929 | 3.918 | 5.706 | 5.905 | 6.452 | 6.280 | 6.784 | 5.905 | 6.452 | 6.280 | 6.784 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.608 | 3.641 | 5.269 | 5.428 | 6.104 | 5.804 | 6.226 | 5.428 | 6.104 | 5.804 | 6.226 | ns |
| | | GCLK PLL | $t_{co}$ | 4.051 | 4.040 | 5.904 | 6.112 | 6.668 | 6.496 | 7.153 | 6.112 | 6.668 | 6.496 | 7.153 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.497 | 3.530 | 5.139 | 5.294 | 5.942 | 5.668 | 6.088 | 5.294 | 5.942 | 5.668 | 6.088 | ns |
| | | GCLK PLL | $t_{co}$ | 3.940 | 3.929 | 5.774 | 5.978 | 6.531 | 6.360 | 6.990 | 5.978 | 6.531 | 6.360 | 6.990 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.461 | 3.494 | 5.076 | 5.225 | 5.840 | 5.594 | 6.014 | 5.225 | 5.840 | 5.594 | 6.014 | ns |
| | | GCLK PLL | $t_{co}$ | 3.904 | 3.893 | 5.711 | 5.909 | 6.457 | 6.286 | 6.888 | 5.909 | 6.457 | 6.286 | 6.888 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.443 | 3.476 | 5.047 | 5.197 | 5.790 | 5.564 | 5.986 | 5.197 | 5.790 | 5.564 | 5.986 | ns |
| | | GCLK PLL | $t_{co}$ | 3.886 | 3.875 | 5.682 | 5.881 | 6.428 | 6.256 | 6.838 | 5.881 | 6.428 | 6.256 | 6.838 | ns |

**Table 1–133.** EP3SE260 Column Pins Output Timing Parameters (Part 2 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.522 | 3.555 | 5.173 | 5.328 | 5.996 | 5.703 | 6.123 | 5.328 | 5.996 | 5.703 | 6.123 | ns |
| | | GCLK PLL | $t_{co}$ | 3.965 | 3.954 | 5.808 | 6.012 | 6.566 | 6.395 | 7.044 | 6.012 | 6.566 | 6.395 | 7.044 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.443 | 3.476 | 5.049 | 5.199 | 5.814 | 5.568 | 5.988 | 5.199 | 5.814 | 5.568 | 5.988 | ns |
| | | GCLK PLL | $t_{co}$ | 3.886 | 3.875 | 5.684 | 5.883 | 6.431 | 6.260 | 6.862 | 5.883 | 6.431 | 6.260 | 6.862 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.438 | 3.471 | 5.042 | 5.192 | 5.746 | 5.558 | 5.980 | 5.192 | 5.746 | 5.558 | 5.980 | ns |
| | | GCLK PLL | $t_{co}$ | 3.881 | 3.870 | 5.677 | 5.876 | 6.422 | 6.250 | 6.795 | 5.876 | 6.422 | 6.250 | 6.795 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.429 | 3.462 | 5.028 | 5.177 | 5.744 | 5.543 | 5.965 | 5.177 | 5.744 | 5.543 | 5.965 | ns |
| | | GCLK PLL | $t_{co}$ | 3.872 | 3.861 | 5.663 | 5.861 | 6.407 | 6.235 | 6.792 | 5.861 | 6.407 | 6.235 | 6.792 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.644 | 3.677 | 5.380 | 5.555 | 6.278 | 5.950 | 6.370 | 5.555 | 6.278 | 5.950 | 6.370 | ns |
| | | GCLK PLL | $t_{co}$ | 4.087 | 4.076 | 6.015 | 6.239 | 6.813 | 6.642 | 7.326 | 6.239 | 6.813 | 6.642 | 7.326 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.544 | 3.577 | 5.261 | 5.429 | 6.081 | 5.818 | 6.238 | 5.429 | 6.081 | 5.818 | 6.238 | ns |
| | | GCLK PLL | $t_{co}$ | 3.987 | 3.976 | 5.896 | 6.113 | 6.681 | 6.510 | 7.129 | 6.113 | 6.681 | 6.510 | 7.129 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.500 | 3.533 | 5.174 | 5.338 | 5.941 | 5.721 | 6.143 | 5.338 | 5.941 | 5.721 | 6.143 | ns |
| | | GCLK PLL | $t_{co}$ | 3.943 | 3.932 | 5.809 | 6.022 | 6.585 | 6.413 | 6.989 | 6.022 | 6.585 | 6.413 | 6.989 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.462 | 3.495 | 5.135 | 5.296 | 5.891 | 5.678 | 6.100 | 5.296 | 5.891 | 5.678 | 6.100 | ns |
| | | GCLK PLL | $t_{co}$ | 3.905 | 3.894 | 5.770 | 5.980 | 6.542 | 6.370 | 6.939 | 5.980 | 6.542 | 6.370 | 6.939 | ns |

**Table 1–133.** EP3SE260 Column Pins Output Timing Parameters (Part 3 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.835 | 3.868 | 5.701 | 5.915 | 6.815 | 6.353 | 6.775 | 5.915 | 6.815 | 6.353 | 6.775 | ns |
| | | GCLK PLL | $t_{co}$ | 4.278 | 4.267 | 6.336 | 6.599 | 7.217 | 7.045 | 7.864 | 6.599 | 7.217 | 7.045 | 7.864 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.654 | 3.687 | 5.422 | 5.606 | 6.354 | 6.007 | 6.427 | 5.606 | 6.354 | 6.007 | 6.427 | ns |
| | | GCLK PLL | $t_{co}$ | 4.097 | 4.086 | 6.057 | 6.290 | 6.870 | 6.699 | 7.402 | 6.290 | 6.870 | 6.699 | 7.402 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.572 | 3.605 | 5.315 | 5.491 | 6.180 | 5.895 | 6.317 | 5.491 | 6.180 | 5.895 | 6.317 | ns |
| | | GCLK PLL | $t_{co}$ | 4.015 | 4.004 | 5.950 | 6.175 | 6.759 | 6.587 | 7.229 | 6.175 | 6.759 | 6.587 | 7.229 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.552 | 3.585 | 5.257 | 5.437 | 6.068 | 5.829 | 6.251 | 5.437 | 6.068 | 5.829 | 6.251 | ns |
| | | GCLK PLL | $t_{co}$ | 3.995 | 3.984 | 5.892 | 6.121 | 6.693 | 6.521 | 7.117 | 6.121 | 6.693 | 6.521 | 7.117 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.489 | 3.522 | 5.196 | 5.362 | 5.954 | 5.748 | 6.170 | 5.362 | 5.954 | 5.748 | 6.170 | ns |
| | | GCLK PLL | $t_{co}$ | 3.932 | 3.921 | 5.831 | 6.046 | 6.612 | 6.440 | 7.003 | 6.046 | 6.612 | 6.440 | 7.003 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.471 | 3.504 | 5.175 | 5.341 | 5.916 | 5.725 | 6.147 | 5.341 | 5.916 | 5.725 | 6.147 | ns |
| | | GCLK PLL | $t_{co}$ | 3.914 | 3.903 | 5.810 | 6.025 | 6.589 | 6.417 | 6.965 | 6.025 | 6.589 | 6.417 | 6.965 | ns |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.781 | 3.814 | 5.630 | 5.847 | 6.732 | 6.291 | 6.713 | 5.847 | 6.732 | 6.291 | 6.713 | ns |
| | | GCLK PLL | $t_{co}$ | 4.224 | 4.213 | 6.265 | 6.531 | 7.155 | 6.983 | 7.781 | 6.531 | 7.155 | 6.983 | 7.781 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.569 | 3.602 | 5.311 | 5.491 | 6.176 | 5.899 | 6.321 | 5.491 | 6.176 | 5.899 | 6.321 | ns |
| | | GCLK PLL | $t_{co}$ | 4.012 | 4.001 | 5.946 | 6.175 | 6.763 | 6.591 | 7.225 | 6.175 | 6.763 | 6.591 | 7.225 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.544 | 3.577 | 5.244 | 5.431 | 6.059 | 5.832 | 6.254 | 5.431 | 6.059 | 5.832 | 6.254 | ns |
| | | GCLK PLL | $t_{co}$ | 3.987 | 3.976 | 5.879 | 6.115 | 6.696 | 6.524 | 7.108 | 6.115 | 6.696 | 6.524 | 7.108 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.533 | 3.566 | 5.227 | 5.406 | 6.027 | 5.812 | 6.234 | 5.406 | 6.027 | 5.812 | 6.234 | ns |
| | | GCLK PLL | $t_{co}$ | 3.976 | 3.965 | 5.862 | 6.090 | 6.676 | 6.504 | 7.076 | 6.090 | 6.676 | 6.504 | 7.076 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.478 | 3.511 | 5.189 | 5.355 | 5.945 | 5.742 | 6.164 | 5.355 | 5.945 | 5.742 | 6.164 | ns |
| | | GCLK PLL | $t_{co}$ | 3.921 | 3.910 | 5.824 | 6.039 | 6.606 | 6.434 | 6.994 | 6.039 | 6.606 | 6.434 | 6.994 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.473 | 3.506 | 5.172 | 5.344 | 5.903 | 5.731 | 6.153 | 5.344 | 5.903 | 5.731 | 6.153 | ns |
| | | GCLK PLL | $t_{co}$ | 3.916 | 3.905 | 5.807 | 6.028 | 6.595 | 6.423 | 6.952 | 6.028 | 6.595 | 6.423 | 6.952 | ns |

**Table 1–133.** EP3SE260 Column Pins Output Timing Parameters (Part 4 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.697 | 3.730 | 5.556 | 5.783 | 6.652 | 6.235 | 6.657 | 5.783 | 6.652 | 6.235 | 6.657 | ns |
| | | GCLK PLL | $t_{co}$ | 4.140 | 4.129 | 6.191 | 6.467 | 7.099 | 6.927 | 7.701 | 6.467 | 7.099 | 6.927 | 7.701 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.574 | 3.607 | 5.330 | 5.521 | 6.223 | 5.949 | 6.371 | 5.521 | 6.223 | 5.949 | 6.371 | ns |
| | | GCLK PLL | $t_{co}$ | 4.017 | 4.006 | 5.965 | 6.205 | 6.813 | 6.641 | 7.272 | 6.205 | 6.813 | 6.641 | 7.272 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.536 | 3.569 | 5.238 | 5.432 | 6.068 | 5.836 | 6.258 | 5.432 | 6.068 | 5.836 | 6.258 | ns |
| | | GCLK PLL | $t_{co}$ | 3.979 | 3.968 | 5.873 | 6.116 | 6.700 | 6.528 | 7.117 | 6.116 | 6.700 | 6.528 | 7.117 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.489 | 3.522 | 5.210 | 5.383 | 5.977 | 5.780 | 6.202 | 5.383 | 5.977 | 5.780 | 6.202 | ns |
| | | GCLK PLL | $t_{co}$ | 3.932 | 3.921 | 5.845 | 6.067 | 6.644 | 6.472 | 7.026 | 6.067 | 6.644 | 6.472 | 7.026 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.489 | 3.522 | 5.167 | 5.330 | 5.925 | 5.711 | 6.133 | 5.330 | 5.925 | 5.711 | 6.133 | ns |
| | | GCLK PLL | $t_{co}$ | 3.932 | 3.921 | 5.802 | 6.014 | 6.575 | 6.403 | 6.974 | 6.014 | 6.575 | 6.403 | 6.974 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.486 | 3.519 | 5.164 | 5.327 | 5.930 | 5.707 | 6.129 | 5.327 | 5.930 | 5.707 | 6.129 | ns |
| | | GCLK PLL | $t_{co}$ | 3.929 | 3.918 | 5.799 | 6.011 | 6.571 | 6.399 | 6.978 | 6.011 | 6.571 | 6.399 | 6.978 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.484 | 3.517 | 5.164 | 5.328 | 5.911 | 5.708 | 6.130 | 5.328 | 5.911 | 5.708 | 6.130 | ns |
| | | GCLK PLL | $t_{co}$ | 3.927 | 3.916 | 5.799 | 6.012 | 6.572 | 6.400 | 6.960 | 6.012 | 6.572 | 6.400 | 6.960 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.475 | 3.508 | 5.149 | 5.312 | 5.877 | 5.693 | 6.115 | 5.312 | 5.877 | 5.693 | 6.115 | ns |
| | | GCLK PLL | $t_{co}$ | 3.918 | 3.907 | 5.784 | 5.996 | 6.557 | 6.385 | 6.926 | 5.996 | 6.557 | 6.385 | 6.926 | ns |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.496 | 3.529 | 5.179 | 5.344 | 5.952 | 5.727 | 6.149 | 5.344 | 5.952 | 5.727 | 6.149 | ns |
| | | GCLK PLL | $t_{co}$ | 3.939 | 3.928 | 5.814 | 6.028 | 6.591 | 6.419 | 7.000 | 6.028 | 6.591 | 6.419 | 7.000 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.492 | 3.525 | 5.177 | 5.342 | 5.942 | 5.725 | 6.147 | 5.342 | 5.942 | 5.725 | 6.147 | ns |
| | | GCLK PLL | $t_{co}$ | 3.935 | 3.924 | 5.812 | 6.026 | 6.589 | 6.417 | 6.991 | 6.026 | 6.589 | 6.417 | 6.991 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.481 | 3.514 | 5.167 | 5.333 | 5.934 | 5.716 | 6.138 | 5.333 | 5.934 | 5.716 | 6.138 | ns |
| | | GCLK PLL | $t_{co}$ | 3.924 | 3.913 | 5.802 | 6.017 | 6.580 | 6.408 | 6.982 | 6.017 | 6.580 | 6.408 | 6.982 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.470 | 3.503 | 5.154 | 5.320 | 5.896 | 5.703 | 6.125 | 5.320 | 5.896 | 5.703 | 6.125 | ns |
| | | GCLK PLL | $t_{co}$ | 3.913 | 3.902 | 5.789 | 6.004 | 6.567 | 6.395 | 6.945 | 6.004 | 6.567 | 6.395 | 6.945 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.470 | 3.503 | 5.154 | 5.320 | 5.896 | 5.703 | 6.125 | 5.320 | 5.896 | 5.703 | 6.125 | ns |
| | | GCLK PLL | $t_{co}$ | 3.913 | 3.902 | 5.789 | 6.004 | 6.567 | 6.395 | 6.945 | 6.004 | 6.567 | 6.395 | 6.945 | ns |

**Table 1–133.** EP3SE260 Column Pins Output Timing Parameters (Part 5 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.476 | 3.509 | 5.153 | 5.317 | 5.896 | 5.698 | 6.120 | 5.317 | 5.896 | 5.698 | 6.120 | ns |
| | | GCLK PLL | $t_{co}$ | 3.919 | 3.908 | 5.788 | 6.001 | 6.562 | 6.390 | 6.945 | 6.001 | 6.562 | 6.390 | 6.945 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.479 | 3.512 | 5.161 | 5.326 | 5.901 | 5.710 | 6.132 | 5.326 | 5.901 | 5.710 | 6.132 | ns |
| | | GCLK PLL | $t_{co}$ | 3.922 | 3.911 | 5.796 | 6.010 | 6.574 | 6.402 | 6.950 | 6.010 | 6.574 | 6.402 | 6.950 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.500 | 3.533 | 5.188 | 5.356 | 5.967 | 5.740 | 6.162 | 5.356 | 5.967 | 5.740 | 6.162 | ns |
| | | GCLK PLL | $t_{co}$ | 3.943 | 3.932 | 5.823 | 6.040 | 6.604 | 6.432 | 7.016 | 6.040 | 6.604 | 6.432 | 7.016 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.486 | 3.519 | 5.178 | 5.346 | 5.941 | 5.731 | 6.153 | 5.346 | 5.941 | 5.731 | 6.153 | ns |
| | | GCLK PLL | $t_{co}$ | 3.929 | 3.918 | 5.813 | 6.030 | 6.595 | 6.423 | 6.990 | 6.030 | 6.595 | 6.423 | 6.990 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.475 | 3.508 | 5.164 | 5.332 | 5.917 | 5.717 | 6.139 | 5.332 | 5.917 | 5.717 | 6.139 | ns |
| | | GCLK PLL | $t_{co}$ | 3.918 | 3.907 | 5.799 | 6.016 | 6.581 | 6.409 | 6.966 | 6.016 | 6.581 | 6.409 | 6.966 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.474 | 3.507 | 5.167 | 5.335 | 5.906 | 5.721 | 6.143 | 5.335 | 5.906 | 5.721 | 6.143 | ns |
| | | GCLK PLL | $t_{co}$ | 3.917 | 3.906 | 5.802 | 6.019 | 6.585 | 6.413 | 6.955 | 6.019 | 6.585 | 6.413 | 6.955 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.471 | 3.504 | 5.162 | 5.330 | 5.896 | 5.715 | 6.137 | 5.330 | 5.896 | 5.715 | 6.137 | ns |
| | | GCLK PLL | $t_{co}$ | 3.914 | 3.903 | 5.797 | 6.014 | 6.579 | 6.407 | 6.945 | 6.014 | 6.579 | 6.407 | 6.945 | ns |
| SSTL-15 CLASS II | 8mA | GCLK | $t_{co}$ | 3.473 | 3.506 | 5.151 | 5.316 | 5.896 | 5.698 | 6.120 | 5.316 | 5.896 | 5.698 | 6.120 | ns |
| | | GCLK PLL | $t_{co}$ | 3.916 | 3.905 | 5.786 | 6.000 | 6.562 | 6.390 | 6.945 | 6.000 | 6.562 | 6.390 | 6.945 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.476 | 3.509 | 5.158 | 5.325 | 5.902 | 5.709 | 6.131 | 5.325 | 5.902 | 5.709 | 6.131 | ns |
| | | GCLK PLL | $t_{co}$ | 3.919 | 3.908 | 5.793 | 6.009 | 6.573 | 6.401 | 6.951 | 6.009 | 6.573 | 6.401 | 6.951 | ns |


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**Table 1–133.** EP3SE260 Column Pins Output Timing Parameters (Part 6 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.483 | 3.516 | 5.153 | 5.316 | 5.910 | 5.696 | 6.118 | 5.316 | 5.910 | 5.696 | 6.118 | ns |
| | | GCLK PLL | $t_{co}$ | 3.926 | 3.915 | 5.788 | 6.000 | 6.560 | 6.388 | 6.959 | 6.000 | 6.560 | 6.388 | 6.959 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.476 | 3.509 | 5.151 | 5.314 | 5.906 | 5.695 | 6.117 | 5.314 | 5.906 | 5.695 | 6.117 | ns |
| | | GCLK PLL | $t_{co}$ | 3.919 | 3.908 | 5.786 | 5.998 | 6.559 | 6.387 | 6.954 | 5.998 | 6.559 | 6.387 | 6.954 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.468 | 3.501 | 5.143 | 5.307 | 5.879 | 5.688 | 6.110 | 5.307 | 5.879 | 5.688 | 6.110 | ns |
| | | GCLK PLL | $t_{co}$ | 3.911 | 3.900 | 5.778 | 5.991 | 6.552 | 6.380 | 6.928 | 5.991 | 6.552 | 6.380 | 6.928 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.471 | 3.504 | 5.146 | 5.310 | 5.882 | 5.692 | 6.114 | 5.310 | 5.882 | 5.692 | 6.114 | ns |
| | | GCLK PLL | $t_{co}$ | 3.914 | 3.903 | 5.781 | 5.994 | 6.556 | 6.384 | 6.931 | 5.994 | 6.556 | 6.384 | 6.931 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.468 | 3.501 | 5.149 | 5.314 | 5.881 | 5.696 | 6.118 | 5.314 | 5.881 | 5.696 | 6.118 | ns |
| | | GCLK PLL | $t_{co}$ | 3.911 | 3.900 | 5.784 | 5.998 | 6.560 | 6.388 | 6.929 | 5.998 | 6.560 | 6.388 | 6.929 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.476 | 3.509 | 5.148 | 5.311 | 5.878 | 5.692 | 6.114 | 5.311 | 5.878 | 5.692 | 6.114 | ns |
| | | GCLK PLL | $t_{co}$ | 3.919 | 3.908 | 5.783 | 5.995 | 6.556 | 6.384 | 6.927 | 5.995 | 6.556 | 6.384 | 6.927 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.488 | 3.521 | 5.161 | 5.326 | 5.926 | 5.707 | 6.129 | 5.326 | 5.926 | 5.707 | 6.129 | ns |
| | | GCLK PLL | $t_{co}$ | 3.931 | 3.920 | 5.796 | 6.010 | 6.571 | 6.399 | 6.975 | 6.010 | 6.571 | 6.399 | 6.975 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.484 | 3.517 | 5.162 | 5.327 | 5.915 | 5.710 | 6.132 | 5.327 | 5.915 | 5.710 | 6.132 | ns |
| | | GCLK PLL | $t_{co}$ | 3.927 | 3.916 | 5.797 | 6.011 | 6.574 | 6.402 | 6.964 | 6.011 | 6.574 | 6.402 | 6.964 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.480 | 3.513 | 5.158 | 5.323 | 5.909 | 5.705 | 6.127 | 5.323 | 5.909 | 5.705 | 6.127 | ns |
| | | GCLK PLL | $t_{co}$ | 3.923 | 3.912 | 5.793 | 6.007 | 6.569 | 6.397 | 6.958 | 6.007 | 6.569 | 6.397 | 6.958 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.473 | 3.506 | 5.151 | 5.316 | 5.896 | 5.698 | 6.120 | 5.316 | 5.896 | 5.698 | 6.120 | ns |
| | | GCLK PLL | $t_{co}$ | 3.916 | 3.905 | 5.786 | 6.000 | 6.562 | 6.390 | 6.945 | 6.000 | 6.562 | 6.390 | 6.945 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.474 | 3.507 | 5.158 | 5.324 | 5.892 | 5.708 | 6.130 | 5.324 | 5.892 | 5.708 | 6.130 | ns |
| | | GCLK PLL | $t_{co}$ | 3.917 | 3.906 | 5.793 | 6.008 | 6.572 | 6.400 | 6.941 | 6.008 | 6.572 | 6.400 | 6.941 | ns |
| 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.472 | 3.505 | 5.139 | 5.302 | 5.871 | 5.682 | 6.104 | 5.302 | 5.871 | 5.682 | 6.104 | ns |
| | | GCLK PLL | $t_{co}$ | 3.915 | 3.904 | 5.774 | 5.986 | 6.546 | 6.374 | 6.920 | 5.986 | 6.546 | 6.374 | 6.920 | ns |

**Table 1–133.** EP3SE260 Column Pins Output Timing Parameters (Part 7 of 7)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.491 | 3.524 | 5.175 | 5.343 | 5.945 | 5.728 | 6.150 | 5.343 | 5.945 | 5.728 | 6.150 | ns |
| | | GCLK PLL | $t_{co}$ | 3.934 | 3.923 | 5.810 | 6.027 | 6.592 | 6.420 | 6.994 | 6.027 | 6.592 | 6.420 | 6.994 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.483 | 3.516 | 5.166 | 5.334 | 5.928 | 5.719 | 6.141 | 5.334 | 5.928 | 5.719 | 6.141 | ns |
| | | GCLK PLL | $t_{co}$ | 3.926 | 3.915 | 5.801 | 6.018 | 6.583 | 6.411 | 6.977 | 6.018 | 6.583 | 6.411 | 6.977 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.484 | 3.517 | 5.174 | 5.342 | 5.924 | 5.728 | 6.150 | 5.342 | 5.924 | 5.728 | 6.150 | ns |
| | | GCLK PLL | $t_{co}$ | 3.927 | 3.916 | 5.809 | 6.026 | 6.592 | 6.420 | 6.973 | 6.026 | 6.592 | 6.420 | 6.973 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.473 | 3.506 | 5.161 | 5.329 | 5.901 | 5.714 | 6.136 | 5.329 | 5.901 | 5.714 | 6.136 | ns |
| | | GCLK PLL | $t_{co}$ | 3.916 | 3.905 | 5.796 | 6.013 | 6.578 | 6.406 | 6.950 | 6.013 | 6.578 | 6.406 | 6.950 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.473 | 3.506 | 5.161 | 5.329 | 5.902 | 5.715 | 6.137 | 5.329 | 5.902 | 5.715 | 6.137 | ns |
| | | GCLK PLL | $t_{co}$ | 3.916 | 3.905 | 5.796 | 6.013 | 6.579 | 6.407 | 6.951 | 6.013 | 6.579 | 6.407 | 6.951 | ns |
| 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.494 | 3.527 | 5.177 | 5.344 | 5.980 | 5.728 | 6.150 | 5.344 | 5.980 | 5.728 | 6.150 | ns |
| | | GCLK PLL | $t_{co}$ | 3.937 | 3.926 | 5.812 | 6.028 | 6.592 | 6.420 | 7.029 | 6.028 | 6.592 | 6.420 | 7.029 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.597 | 3.630 | 5.222 | 5.378 | 5.955 | 5.753 | 6.175 | 5.378 | 5.955 | 5.753 | 6.175 | ns |
| | | GCLK PLL | $t_{co}$ | 4.040 | 4.029 | 5.857 | 6.062 | 6.617 | 6.445 | 7.004 | 6.062 | 6.617 | 6.445 | 7.004 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.597 | 3.630 | 5.222 | 5.378 | 5.955 | 5.753 | 6.175 | 5.378 | 5.955 | 5.753 | 6.175 | ns |
| | | GCLK PLL | $t_{co}$ | 4.040 | 4.029 | 5.857 | 6.062 | 6.617 | 6.445 | 7.004 | 6.062 | 6.617 | 6.445 | 7.004 | ns |

Table 1–134 lists the EP3SE260 row pins output timing parameters for single-ended I/O standards.

**Table 1–134.** EP3SE260 Row Pins Output Timing Parameters (Part 1 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.648 | 3.902 | 5.663 | 5.865 | 6.484 | 6.256 | 6.709 | 6.063 | 6.530 | 6.256 | 6.709 | ns |
| | | GCLK PLL | $t_{co}$ | 1.582 | 1.785 | 2.228 | 2.322 | 2.505 | 2.489 | 2.454 | 2.441 | 2.632 | 2.489 | 2.454 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.555 | 3.797 | 5.533 | 5.727 | 6.340 | 6.112 | 6.565 | 5.922 | 6.414 | 6.112 | 6.565 | ns |
| | | GCLK PLL | $t_{co}$ | 1.489 | 1.680 | 2.098 | 2.184 | 2.361 | 2.346 | 2.310 | 2.300 | 2.483 | 2.346 | 2.310 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.456 | 3.707 | 5.414 | 5.604 | 6.212 | 5.995 | 6.446 | 5.795 | 6.315 | 5.995 | 6.446 | ns |
| | | GCLK PLL | $t_{co}$ | 1.390 | 1.574 | 1.979 | 2.061 | 2.233 | 2.250 | 2.182 | 2.173 | 2.354 | 2.250 | 2.182 | ns |

**Table 1–134.** EP3SE260 Row Pins Output Timing Parameters (Part 2 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 3.3-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.658 | 3.906 | 5.671 | 5.870 | 6.489 | 6.261 | 6.714 | 6.069 | 6.542 | 6.261 | 6.714 | ns |
| | | GCLK PLL | $t_{co}$ | 1.592 | 1.789 | 2.236 | 2.327 | 2.510 | 2.494 | 2.459 | 2.447 | 2.637 | 2.494 | 2.459 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.460 | 3.711 | 5.420 | 5.616 | 6.218 | 6.005 | 6.456 | 5.801 | 6.324 | 6.005 | 6.456 | ns |
| | | GCLK PLL | $t_{co}$ | 1.394 | 1.580 | 1.985 | 2.067 | 2.239 | 2.260 | 2.188 | 2.179 | 2.363 | 2.260 | 2.188 | ns |
| 3.0-V LVTTL | 4mA | GCLK | $t_{co}$ | 3.602 | 3.848 | 5.615 | 5.818 | 6.441 | 6.213 | 6.666 | 6.020 | 6.496 | 6.213 | 6.666 | ns |
| | | GCLK PLL | $t_{co}$ | 1.536 | 1.731 | 2.180 | 2.275 | 2.462 | 2.446 | 2.411 | 2.398 | 2.590 | 2.446 | 2.411 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.477 | 3.721 | 5.463 | 5.659 | 6.277 | 6.049 | 6.502 | 5.858 | 6.351 | 6.049 | 6.502 | ns |
| | | GCLK PLL | $t_{co}$ | 1.411 | 1.604 | 2.028 | 2.116 | 2.298 | 2.282 | 2.247 | 2.236 | 2.426 | 2.282 | 2.247 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.438 | 3.678 | 5.381 | 5.576 | 6.189 | 5.961 | 6.414 | 5.772 | 6.277 | 5.961 | 6.414 | ns |
| | | GCLK PLL | $t_{co}$ | 1.372 | 1.553 | 1.946 | 2.033 | 2.210 | 2.211 | 2.159 | 2.150 | 2.333 | 2.211 | 2.159 | ns |
| 3.0-V LVCMOS | 4mA | GCLK | $t_{co}$ | 3.516 | 3.767 | 5.510 | 5.711 | 6.330 | 6.102 | 6.555 | 5.912 | 6.387 | 6.102 | 6.555 | ns |
| | | GCLK PLL | $t_{co}$ | 1.450 | 1.650 | 2.075 | 2.168 | 2.351 | 2.335 | 2.300 | 2.290 | 2.479 | 2.335 | 2.300 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.416 | 3.662 | 5.351 | 5.545 | 6.150 | 5.928 | 6.379 | 5.732 | 6.249 | 5.928 | 6.379 | ns |
| | | GCLK PLL | $t_{co}$ | 1.350 | 1.531 | 1.911 | 1.994 | 2.171 | 2.183 | 2.120 | 2.110 | 2.293 | 2.183 | 2.120 | ns |
| 2.5 V | 4mA | GCLK | $t_{co}$ | 3.628 | 3.884 | 5.748 | 5.972 | 6.613 | 6.385 | 6.838 | 6.180 | 6.648 | 6.385 | 6.838 | ns |
| | | GCLK PLL | $t_{co}$ | 1.562 | 1.767 | 2.313 | 2.429 | 2.634 | 2.618 | 2.583 | 2.558 | 2.769 | 2.618 | 2.583 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.518 | 3.785 | 5.593 | 5.809 | 6.443 | 6.215 | 6.668 | 6.013 | 6.504 | 6.215 | 6.668 | ns |
| | | GCLK PLL | $t_{co}$ | 1.452 | 1.668 | 2.158 | 2.266 | 2.464 | 2.448 | 2.413 | 2.391 | 2.595 | 2.448 | 2.413 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.472 | 3.718 | 5.482 | 5.690 | 6.317 | 6.089 | 6.542 | 5.890 | 6.409 | 6.089 | 6.542 | ns |
| | | GCLK PLL | $t_{co}$ | 1.406 | 1.592 | 2.047 | 2.147 | 2.338 | 2.338 | 2.287 | 2.268 | 2.465 | 2.338 | 2.287 | ns |
| 1.8 V | 2mA | GCLK | $t_{co}$ | 3.886 | 4.170 | 6.174 | 6.450 | 7.088 | 6.750 | 7.260 | 6.640 | 7.070 | 6.750 | 7.260 | ns |
| | | GCLK PLL | $t_{co}$ | 1.787 | 2.014 | 2.698 | 2.822 | 3.109 | 3.100 | 3.058 | 2.988 | 3.253 | 3.100 | 3.058 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.661 | 3.968 | 5.848 | 6.082 | 6.683 | 6.390 | 6.855 | 6.275 | 6.709 | 6.390 | 6.855 | ns |
| | | GCLK PLL | $t_{co}$ | 1.562 | 1.812 | 2.372 | 2.454 | 2.704 | 2.695 | 2.653 | 2.623 | 2.847 | 2.695 | 2.653 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.596 | 3.866 | 5.694 | 5.932 | 6.524 | 6.289 | 6.709 | 6.107 | 6.603 | 6.289 | 6.709 | ns |
| | | GCLK PLL | $t_{co}$ | 1.497 | 1.710 | 2.218 | 2.304 | 2.545 | 2.536 | 2.494 | 2.455 | 2.674 | 2.536 | 2.494 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.536 | 3.792 | 5.617 | 5.839 | 6.428 | 6.224 | 6.644 | 6.012 | 6.531 | 6.224 | 6.644 | ns |
| | | GCLK PLL | $t_{co}$ | 1.437 | 1.649 | 2.141 | 2.227 | 2.449 | 2.440 | 2.398 | 2.360 | 2.580 | 2.440 | 2.398 | ns |

**Table 1–134.** EP3SE260 Row Pins Output Timing Parameters (Part 3 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.5 V | 2mA | GCLK | $t_{co}$ | 3.797 | 4.088 | 6.084 | 6.364 | 7.016 | 6.687 | 7.188 | 6.547 | 7.005 | 6.687 | 7.188 | ns |
| | | GCLK PLL | $t_{co}$ | 1.698 | 1.932 | 2.608 | 2.736 | 3.037 | 3.028 | 2.986 | 2.895 | 3.177 | 3.028 | 2.986 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.555 | 3.831 | 5.679 | 5.927 | 6.525 | 6.293 | 6.713 | 6.101 | 6.604 | 6.293 | 6.713 | ns |
| | | GCLK PLL | $t_{co}$ | 1.456 | 1.675 | 2.203 | 2.299 | 2.546 | 2.537 | 2.495 | 2.449 | 2.673 | 2.537 | 2.495 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.528 | 3.783 | 5.606 | 5.831 | 6.419 | 6.224 | 6.644 | 6.003 | 6.531 | 6.224 | 6.644 | ns |
| | | GCLK PLL | $t_{co}$ | 1.429 | 1.640 | 2.130 | 2.219 | 2.440 | 2.431 | 2.389 | 2.351 | 2.568 | 2.431 | 2.389 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.519 | 3.774 | 5.584 | 5.813 | 6.400 | 6.205 | 6.625 | 5.985 | 6.512 | 6.205 | 6.625 | ns |
| | | GCLK PLL | $t_{co}$ | 1.420 | 1.629 | 2.108 | 2.195 | 2.421 | 2.412 | 2.370 | 2.333 | 2.549 | 2.412 | 2.370 | ns |
| 1.2 V | 2mA | GCLK | $t_{co}$ | 3.740 | 4.013 | 5.994 | 6.278 | 6.941 | 6.626 | 7.113 | 6.459 | 6.936 | 6.626 | 7.113 | ns |
| | | GCLK PLL | $t_{co}$ | 1.641 | 1.857 | 2.518 | 2.650 | 2.962 | 2.953 | 2.911 | 2.807 | 3.093 | 2.953 | 2.911 | ns |
| | 4mA | GCLK | $t_{co}$ | 3.560 | 3.824 | 5.701 | 5.955 | 6.566 | 6.341 | 6.761 | 6.126 | 6.648 | 6.341 | 6.761 | ns |
| | | GCLK PLL | $t_{co}$ | 1.461 | 1.670 | 2.225 | 2.327 | 2.587 | 2.578 | 2.536 | 2.474 | 2.715 | 2.578 | 2.536 | ns |
| SSTL-2 CLASS I | 8mA | GCLK | $t_{co}$ | 3.457 | 3.706 | 5.468 | 5.677 | 6.285 | 6.073 | 6.524 | 5.857 | 6.395 | 6.073 | 6.524 | ns |
| | | GCLK PLL | $t_{co}$ | 1.391 | 1.578 | 2.024 | 2.119 | 2.306 | 2.328 | 2.255 | 2.235 | 2.434 | 2.328 | 2.255 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.445 | 3.702 | 5.465 | 5.675 | 6.277 | 6.071 | 6.522 | 5.849 | 6.394 | 6.071 | 6.522 | ns |
| | | GCLK PLL | $t_{co}$ | 1.379 | 1.566 | 2.016 | 2.111 | 2.301 | 2.326 | 2.247 | 2.227 | 2.433 | 2.326 | 2.247 | ns |
| SSTL-2 CLASS II | 16mA | GCLK | $t_{co}$ | 3.429 | 3.691 | 5.450 | 5.659 | 6.250 | 6.054 | 6.505 | 5.823 | 6.376 | 6.054 | 6.505 | ns |
| | | GCLK PLL | $t_{co}$ | 1.363 | 1.548 | 1.991 | 2.086 | 2.284 | 2.309 | 2.220 | 2.201 | 2.415 | 2.309 | 2.220 | ns |
| SSTL-18 CLASS I | 4mA | GCLK | $t_{co}$ | 3.497 | 3.748 | 5.512 | 5.726 | 6.301 | 6.119 | 6.539 | 5.893 | 6.422 | 6.119 | 6.539 | ns |
| | | GCLK PLL | $t_{co}$ | 1.398 | 1.593 | 2.041 | 2.131 | 2.324 | 2.313 | 2.271 | 2.241 | 2.459 | 2.313 | 2.271 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.482 | 3.734 | 5.509 | 5.724 | 6.299 | 6.118 | 6.538 | 5.891 | 6.420 | 6.118 | 6.538 | ns |
| | | GCLK PLL | $t_{co}$ | 1.383 | 1.588 | 2.039 | 2.130 | 2.323 | 2.311 | 2.269 | 2.239 | 2.457 | 2.311 | 2.269 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.471 | 3.722 | 5.492 | 5.707 | 6.282 | 6.108 | 6.528 | 5.874 | 6.411 | 6.108 | 6.528 | ns |
| | | GCLK PLL | $t_{co}$ | 1.372 | 1.577 | 2.029 | 2.120 | 2.313 | 2.294 | 2.252 | 2.222 | 2.448 | 2.294 | 2.252 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.447 | 3.699 | 5.476 | 5.691 | 6.267 | 6.095 | 6.515 | 5.859 | 6.399 | 6.095 | 6.515 | ns |
| | | GCLK PLL | $t_{co}$ | 1.348 | 1.566 | 2.016 | 2.107 | 2.300 | 2.279 | 2.237 | 2.207 | 2.436 | 2.279 | 2.237 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.447 | 3.698 | 5.475 | 5.690 | 6.266 | 6.095 | 6.515 | 5.858 | 6.399 | 6.095 | 6.515 | ns |
| | | GCLK PLL | $t_{co}$ | 1.348 | 1.565 | 2.016 | 2.107 | 2.300 | 2.278 | 2.236 | 2.206 | 2.436 | 2.278 | 2.236 | ns |


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**Table 1–134.** EP3SE260 Row Pins Output Timing Parameters (Part 4 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| SSTL-18 CLASS II | 8mA | GCLK | $t_{co}$ | 3.457 | 3.707 | 5.473 | 5.686 | 6.260 | 6.090 | 6.510 | 5.853 | 6.393 | 6.090 | 6.510 | ns |
| | | GCLK PLL | $t_{co}$ | 1.358 | 1.572 | 2.015 | 2.104 | 2.295 | 2.272 | 2.230 | 2.201 | 2.430 | 2.272 | 2.230 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.451 | 3.702 | 5.472 | 5.687 | 6.262 | 6.100 | 6.520 | 5.855 | 6.404 | 6.100 | 6.520 | ns |
| | | GCLK PLL | $t_{co}$ | 1.352 | 1.575 | 2.021 | 2.112 | 2.305 | 2.274 | 2.233 | 2.203 | 2.441 | 2.274 | 2.233 | ns |
| SSTL-15 CLASS I | 4mA | GCLK | $t_{co}$ | 3.493 | 3.744 | 5.523 | 5.740 | 6.318 | 6.132 | 6.552 | 5.906 | 6.434 | 6.132 | 6.552 | ns |
| | | GCLK PLL | $t_{co}$ | 1.394 | 1.596 | 2.050 | 2.142 | 2.339 | 2.330 | 2.288 | 2.254 | 2.471 | 2.330 | 2.288 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.470 | 3.722 | 5.505 | 5.723 | 6.301 | 6.122 | 6.542 | 5.890 | 6.425 | 6.122 | 6.542 | ns |
| | | GCLK PLL | $t_{co}$ | 1.371 | 1.582 | 2.039 | 2.132 | 2.327 | 2.313 | 2.271 | 2.238 | 2.462 | 2.313 | 2.271 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.453 | 3.705 | 5.488 | 5.705 | 6.283 | 6.109 | 6.529 | 5.872 | 6.412 | 6.109 | 6.529 | ns |
| | | GCLK PLL | $t_{co}$ | 1.354 | 1.570 | 2.026 | 2.119 | 2.314 | 2.295 | 2.253 | 2.220 | 2.449 | 2.295 | 2.253 | ns |
| 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.472 | 3.720 | 5.479 | 5.691 | 6.263 | 6.088 | 6.508 | 5.857 | 6.390 | 6.088 | 6.508 | ns |
| | | GCLK PLL | $t_{co}$ | 1.373 | 1.578 | 2.014 | 2.102 | 2.293 | 2.275 | 2.233 | 2.205 | 2.427 | 2.275 | 2.233 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.460 | 3.708 | 5.470 | 5.683 | 6.255 | 6.087 | 6.507 | 5.849 | 6.390 | 6.087 | 6.507 | ns |
| | | GCLK PLL | $t_{co}$ | 1.361 | 1.572 | 2.012 | 2.101 | 2.292 | 2.267 | 2.225 | 2.197 | 2.427 | 2.267 | 2.225 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.447 | 3.696 | 5.462 | 5.674 | 6.247 | 6.080 | 6.500 | 5.841 | 6.383 | 6.080 | 6.500 | ns |
| | | GCLK PLL | $t_{co}$ | 1.348 | 1.564 | 2.005 | 2.094 | 2.285 | 2.259 | 2.217 | 2.189 | 2.420 | 2.259 | 2.217 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.449 | 3.698 | 5.464 | 5.677 | 6.250 | 6.084 | 6.504 | 5.844 | 6.386 | 6.084 | 6.504 | ns |
| | | GCLK PLL | $t_{co}$ | 1.350 | 1.566 | 2.008 | 2.097 | 2.289 | 2.262 | 2.220 | 2.192 | 2.423 | 2.262 | 2.220 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.442 | 3.693 | 5.462 | 5.676 | 6.250 | 6.087 | 6.507 | 5.844 | 6.391 | 6.087 | 6.507 | ns |
| | | GCLK PLL | $t_{co}$ | 1.343 | 1.563 | 2.010 | 2.100 | 2.292 | 2.262 | 2.220 | 2.192 | 2.428 | 2.262 | 2.220 | ns |
| 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.448 | 3.697 | 5.457 | 5.668 | 6.241 | 6.083 | 6.503 | 5.835 | 6.385 | 6.083 | 6.503 | ns |
| | | GCLK PLL | $t_{co}$ | 1.349 | 1.571 | 2.008 | 2.097 | 2.288 | 2.253 | 2.216 | 2.183 | 2.422 | 2.253 | 2.216 | ns |
| 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.479 | 3.727 | 5.490 | 5.704 | 6.278 | 6.099 | 6.519 | 5.869 | 6.401 | 6.099 | 6.519 | ns |
| | | GCLK PLL | $t_{co}$ | 1.380 | 1.584 | 2.023 | 2.112 | 2.304 | 2.290 | 2.248 | 2.217 | 2.438 | 2.290 | 2.248 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.467 | 3.717 | 5.486 | 5.700 | 6.274 | 6.101 | 6.521 | 5.866 | 6.404 | 6.101 | 6.521 | ns |
| | | GCLK PLL | $t_{co}$ | 1.368 | 1.579 | 2.024 | 2.114 | 2.306 | 2.286 | 2.244 | 2.214 | 2.441 | 2.286 | 2.244 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.463 | 3.712 | 5.480 | 5.694 | 6.268 | 6.096 | 6.516 | 5.860 | 6.398 | 6.096 | 6.516 | ns |
| | | GCLK PLL | $t_{co}$ | 1.364 | 1.575 | 2.019 | 2.109 | 2.301 | 2.280 | 2.238 | 2.208 | 2.435 | 2.280 | 2.238 | ns |

**Table 1–134.** EP3SE260 Row Pins Output Timing Parameters (Part 5 of 5)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.478 | 3.726 | 5.501 | 5.718 | 6.296 | 6.118 | 6.538 | 5.883 | 6.420 | 6.118 | 6.538 | ns |
| | | GCLK PLL | $t_{co}$ | 1.379 | 1.586 | 2.036 | 2.128 | 2.323 | 2.308 | 2.266 | 2.231 | 2.457 | 2.308 | 2.266 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.466 | 3.714 | 5.490 | 5.706 | 6.284 | 6.109 | 6.529 | 5.872 | 6.411 | 6.109 | 6.529 | ns |
| | | GCLK PLL | $t_{co}$ | 1.367 | 1.578 | 2.027 | 2.119 | 2.314 | 2.296 | 2.254 | 2.220 | 2.448 | 2.296 | 2.254 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.463 | 3.712 | 5.494 | 5.711 | 6.290 | 6.118 | 6.538 | 5.878 | 6.421 | 6.118 | 6.538 | ns |
| | | GCLK PLL | $t_{co}$ | 1.364 | 1.578 | 2.034 | 2.127 | 2.323 | 2.302 | 2.260 | 2.226 | 2.458 | 2.302 | 2.260 | ns |
| 3.0-V PCI | — | GCLK | $t_{co}$ | 3.542 | 3.812 | 5.520 | 5.723 | 6.294 | 6.113 | 6.564 | 5.875 | 6.437 | 6.113 | 6.564 | ns |
| | | GCLK PLL | $t_{co}$ | 1.476 | 1.661 | 2.049 | 2.137 | 2.343 | 2.368 | 2.264 | 2.253 | 2.476 | 2.368 | 2.264 | ns |
| 3.0-V PCI-X | — | GCLK | $t_{co}$ | 3.542 | 3.812 | 5.520 | 5.723 | 6.294 | 6.113 | 6.564 | 5.875 | 6.437 | 6.113 | 6.564 | ns |
| | | GCLK PLL | $t_{co}$ | 1.476 | 1.661 | 2.049 | 2.137 | 2.343 | 2.368 | 2.264 | 2.253 | 2.476 | 2.368 | 2.264 | ns |

Table 1–135 through Table 1–138 list the maximum I/O timing parameters for EP3SE260 devices for differential I/O standards.

Table 1–135 lists the EP3SE260 column pins input timing parameters for differential I/O standards.

**Table 1–135.** EP3SE260 Column Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -1.153 | -1.221 | -1.879 | -1.911 | -2.067 | -1.987 | -2.459 | -1.928 | -2.084 | -1.987 | -2.459 | ns |
| | | $t_h$ | 1.289 | 1.376 | 2.114 | 2.150 | 2.330 | 2.237 | 2.711 | 2.177 | 2.355 | 2.237 | 2.711 | ns |
| | GCLK PLL | $t_{su}$ | 1.103 | 1.122 | 1.882 | 1.986 | 2.207 | 2.099 | 2.096 | 1.998 | 2.217 | 2.099 | 2.096 | ns |
| | | $t_h$ | -0.824 | -0.821 | -1.403 | -1.493 | -1.659 | -1.580 | -1.562 | -1.493 | -1.659 | -1.580 | -1.562 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -1.153 | -1.221 | -1.879 | -1.911 | -2.067 | -1.987 | -2.459 | -1.928 | -2.084 | -1.987 | -2.459 | ns |
| | | $t_h$ | 1.289 | 1.376 | 2.114 | 2.150 | 2.330 | 2.237 | 2.711 | 2.177 | 2.355 | 2.237 | 2.711 | ns |
| | GCLK PLL | $t_{su}$ | 1.103 | 1.122 | 1.882 | 1.986 | 2.207 | 2.099 | 2.096 | 1.998 | 2.217 | 2.099 | 2.096 | ns |
| | | $t_h$ | -0.824 | -0.821 | -1.403 | -1.493 | -1.659 | -1.580 | -1.562 | -1.493 | -1.659 | -1.580 | -1.562 | ns |
| RSDS | GCLK | $t_{su}$ | -1.161 | -1.233 | -1.889 | -1.922 | -2.083 | -2.003 | -2.475 | -1.939 | -2.099 | -2.003 | -2.475 | ns |
| | | $t_h$ | 1.297 | 1.388 | 2.124 | 2.161 | 2.346 | 2.253 | 2.727 | 2.188 | 2.370 | 2.253 | 2.727 | ns |
| | GCLK PLL | $t_{su}$ | 1.095 | 1.110 | 1.872 | 1.975 | 2.191 | 2.083 | 2.080 | 1.987 | 2.202 | 2.083 | 2.080 | ns |
| | | $t_h$ | -0.816 | -0.809 | -1.393 | -1.482 | -1.643 | -1.564 | -1.546 | -1.482 | -1.644 | -1.564 | -1.546 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -1.161 | -1.233 | -1.889 | -1.922 | -2.083 | -2.003 | -2.475 | -1.939 | -2.099 | -2.003 | -2.475 | ns |
| | | $t_h$ | 1.297 | 1.388 | 2.124 | 2.161 | 2.346 | 2.253 | 2.727 | 2.188 | 2.370 | 2.253 | 2.727 | ns |
| | GCLK PLL | $t_{su}$ | 1.095 | 1.110 | 1.872 | 1.975 | 2.191 | 2.083 | 2.080 | 1.987 | 2.202 | 2.083 | 2.080 | ns |
| | | $t_h$ | -0.816 | -0.809 | -1.393 | -1.482 | -1.643 | -1.564 | -1.546 | -1.482 | -1.644 | -1.564 | -1.546 | ns |

**Table 1–135.** EP3SE260 Column Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -1.173 | -1.244 | -1.898 | -1.933 | -2.102 | -2.022 | -2.494 | -1.950 | -2.117 | -2.022 | -2.494 | ns |
| | | $t_h$ | 1.309 | 1.399 | 2.133 | 2.172 | 2.365 | 2.272 | 2.746 | 2.199 | 2.388 | 2.272 | 2.746 | ns |
| | GCLK PLL | $t_{su}$ | 1.083 | 1.099 | 1.863 | 1.964 | 2.172 | 2.064 | 2.061 | 1.976 | 2.184 | 2.064 | 2.061 | ns |
| | | $t_h$ | -0.804 | -0.798 | -1.384 | -1.471 | -1.624 | -1.545 | -1.527 | -1.471 | -1.626 | -1.545 | -1.527 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -1.173 | -1.244 | -1.898 | -1.933 | -2.102 | -2.022 | -2.494 | -1.950 | -2.117 | -2.022 | -2.494 | ns |
| | | $t_h$ | 1.309 | 1.399 | 2.133 | 2.172 | 2.365 | 2.272 | 2.746 | 2.199 | 2.388 | 2.272 | 2.746 | ns |
| | GCLK PLL | $t_{su}$ | 1.083 | 1.099 | 1.863 | 1.964 | 2.172 | 2.064 | 2.061 | 1.976 | 2.184 | 2.064 | 2.061 | ns |
| | | $t_h$ | -0.804 | -0.798 | -1.384 | -1.471 | -1.624 | -1.545 | -1.527 | -1.471 | -1.626 | -1.545 | -1.527 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -1.161 | -1.233 | -1.889 | -1.922 | -2.083 | -2.003 | -2.475 | -1.939 | -2.099 | -2.003 | -2.475 | ns |
| | | $t_h$ | 1.297 | 1.388 | 2.124 | 2.161 | 2.346 | 2.253 | 2.727 | 2.188 | 2.370 | 2.253 | 2.727 | ns |
| | GCLK PLL | $t_{su}$ | 1.095 | 1.110 | 1.872 | 1.975 | 2.191 | 2.083 | 2.080 | 1.987 | 2.202 | 2.083 | 2.080 | ns |
| | | $t_h$ | -0.816 | -0.809 | -1.393 | -1.482 | -1.643 | -1.564 | -1.546 | -1.482 | -1.644 | -1.564 | -1.546 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -1.161 | -1.233 | -1.889 | -1.922 | -2.083 | -2.003 | -2.475 | -1.939 | -2.099 | -2.003 | -2.475 | ns |
| | | $t_h$ | 1.297 | 1.388 | 2.124 | 2.161 | 2.346 | 2.253 | 2.727 | 2.188 | 2.370 | 2.253 | 2.727 | ns |
| | GCLK PLL | $t_{su}$ | 1.095 | 1.110 | 1.872 | 1.975 | 2.191 | 2.083 | 2.080 | 1.987 | 2.202 | 2.083 | 2.080 | ns |
| | | $t_h$ | -0.816 | -0.809 | -1.393 | -1.482 | -1.643 | -1.564 | -1.546 | -1.482 | -1.644 | -1.564 | -1.546 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -1.173 | -1.244 | -1.898 | -1.933 | -2.102 | -2.022 | -2.494 | -1.950 | -2.117 | -2.022 | -2.494 | ns |
| | | $t_h$ | 1.309 | 1.399 | 2.133 | 2.172 | 2.365 | 2.272 | 2.746 | 2.199 | 2.388 | 2.272 | 2.746 | ns |
| | GCLK PLL | $t_{su}$ | 1.083 | 1.099 | 1.863 | 1.964 | 2.172 | 2.064 | 2.061 | 1.976 | 2.184 | 2.064 | 2.061 | ns |
| | | $t_h$ | -0.804 | -0.798 | -1.384 | -1.471 | -1.624 | -1.545 | -1.527 | -1.471 | -1.626 | -1.545 | -1.527 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -1.173 | -1.244 | -1.898 | -1.933 | -2.102 | -2.022 | -2.494 | -1.950 | -2.117 | -2.022 | -2.494 | ns |
| | | $t_h$ | 1.309 | 1.399 | 2.133 | 2.172 | 2.365 | 2.272 | 2.746 | 2.199 | 2.388 | 2.272 | 2.746 | ns |
| | GCLK PLL | $t_{su}$ | 1.083 | 1.099 | 1.863 | 1.964 | 2.172 | 2.064 | 2.061 | 1.976 | 2.184 | 2.064 | 2.061 | ns |
| | | $t_h$ | -0.804 | -0.798 | -1.384 | -1.471 | -1.624 | -1.545 | -1.527 | -1.471 | -1.626 | -1.545 | -1.527 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -1.180 | -1.250 | -1.910 | -1.938 | -2.102 | -2.024 | -2.493 | -1.954 | -2.112 | -2.024 | -2.493 | ns |
| | | $t_h$ | 1.316 | 1.405 | 2.146 | 2.180 | 2.368 | 2.275 | 2.750 | 2.206 | 2.388 | 2.275 | 2.750 | ns |
| | GCLK PLL | $t_{su}$ | 1.076 | 1.093 | 1.851 | 1.959 | 2.172 | 2.062 | 2.062 | 1.972 | 2.189 | 2.062 | 2.062 | ns |
| | | $t_h$ | -0.797 | -0.792 | -1.371 | -1.463 | -1.621 | -1.542 | -1.523 | -1.464 | -1.626 | -1.542 | -1.523 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -1.180 | -1.250 | -1.910 | -1.938 | -2.102 | -2.024 | -2.493 | -1.954 | -2.112 | -2.024 | -2.493 | ns |
| | | $t_h$ | 1.316 | 1.405 | 2.146 | 2.180 | 2.368 | 2.275 | 2.750 | 2.206 | 2.388 | 2.275 | 2.750 | ns |
| | GCLK PLL | $t_{su}$ | 1.076 | 1.093 | 1.851 | 1.959 | 2.172 | 2.062 | 2.062 | 1.972 | 2.189 | 2.062 | 2.062 | ns |
| | | $t_h$ | -0.797 | -0.792 | -1.371 | -1.463 | -1.621 | -1.542 | -1.523 | -1.464 | -1.626 | -1.542 | -1.523 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -1.153 | -1.221 | -1.879 | -1.911 | -2.067 | -1.987 | -2.459 | -1.928 | -2.084 | -1.987 | -2.459 | ns |
| | | $t_h$ | 1.289 | 1.376 | 2.114 | 2.150 | 2.330 | 2.237 | 2.711 | 2.177 | 2.355 | 2.237 | 2.711 | ns |
| | GCLK PLL | $t_{su}$ | 1.103 | 1.122 | 1.882 | 1.986 | 2.207 | 2.099 | 2.096 | 1.998 | 2.217 | 2.099 | 2.096 | ns |
| | | $t_h$ | -0.824 | -0.821 | -1.403 | -1.493 | -1.659 | -1.580 | -1.562 | -1.493 | -1.659 | -1.580 | -1.562 | ns |

**Table 1–135.** EP3SE260 Column Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -1.153 | -1.221 | -1.879 | -1.911 | -2.067 | -1.987 | -2.459 | -1.928 | -2.084 | -1.987 | -2.459 | ns |
| | | $t_h$ | 1.289 | 1.376 | 2.114 | 2.150 | 2.330 | 2.237 | 2.711 | 2.177 | 2.355 | 2.237 | 2.711 | ns |
| | GCLK PLL | $t_{su}$ | 1.103 | 1.122 | 1.882 | 1.986 | 2.207 | 2.099 | 2.096 | 1.998 | 2.217 | 2.099 | 2.096 | ns |
| | | $t_h$ | -0.824 | -0.821 | -1.403 | -1.493 | -1.659 | -1.580 | -1.562 | -1.493 | -1.659 | -1.580 | -1.562 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -1.161 | -1.233 | -1.889 | -1.922 | -2.083 | -2.003 | -2.475 | -1.939 | -2.099 | -2.003 | -2.475 | ns |
| | | $t_h$ | 1.297 | 1.388 | 2.124 | 2.161 | 2.346 | 2.253 | 2.727 | 2.188 | 2.370 | 2.253 | 2.727 | ns |
| | GCLK PLL | $t_{su}$ | 1.095 | 1.110 | 1.872 | 1.975 | 2.191 | 2.083 | 2.080 | 1.987 | 2.202 | 2.083 | 2.080 | ns |
| | | $t_h$ | -0.816 | -0.809 | -1.393 | -1.482 | -1.643 | -1.564 | -1.546 | -1.482 | -1.644 | -1.564 | -1.546 | ns |

Table 1–136 lists the EP3SE260 row pins input timing parameters for differential I/O standards.

**Table 1–136.** EP3SE260 Row Pins Input Timing Parameters (Part 1 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | GCLK | $t_{su}$ | -1.332 | -1.401 | -1.719 | -1.648 | -1.841 | -1.769 | -2.221 | -1.630 | -1.815 | -1.769 | -2.221 | ns |
| | | $t_h$ | 1.476 | 1.563 | 1.994 | 1.939 | 2.157 | 2.071 | 2.526 | 1.934 | 2.145 | 2.071 | 2.526 | ns |
| | GCLK PLL | $t_{su}$ | 0.869 | 0.886 | 1.991 | 2.205 | 2.405 | 2.282 | 2.297 | 2.252 | 2.458 | 2.282 | 2.297 | ns |
| | | $t_h$ | -0.581 | -0.578 | -1.475 | -1.662 | -1.803 | -1.711 | -1.711 | -1.692 | -1.839 | -1.711 | -1.711 | ns |
| MINI-LVDS | GCLK | $t_{su}$ | -1.332 | -1.401 | -1.719 | -1.648 | -1.841 | -1.769 | -2.221 | -1.630 | -1.815 | -1.769 | -2.221 | ns |
| | | $t_h$ | 1.476 | 1.563 | 1.994 | 1.939 | 2.157 | 2.071 | 2.526 | 1.934 | 2.145 | 2.071 | 2.526 | ns |
| | GCLK PLL | $t_{su}$ | 0.869 | 0.886 | 1.991 | 2.205 | 2.405 | 2.282 | 2.297 | 2.252 | 2.458 | 2.282 | 2.297 | ns |
| | | $t_h$ | -0.581 | -0.578 | -1.475 | -1.662 | -1.803 | -1.711 | -1.711 | -1.692 | -1.839 | -1.711 | -1.711 | ns |
| RSDS | GCLK | $t_{su}$ | -1.332 | -1.401 | -1.719 | -1.648 | -1.841 | -1.769 | -2.221 | -1.630 | -1.815 | -1.769 | -2.221 | ns |
| | | $t_h$ | 1.476 | 1.563 | 1.994 | 1.939 | 2.157 | 2.071 | 2.526 | 1.934 | 2.145 | 2.071 | 2.526 | ns |
| | GCLK PLL | $t_{su}$ | 0.869 | 0.886 | 1.991 | 2.205 | 2.405 | 2.282 | 2.297 | 2.252 | 2.458 | 2.282 | 2.297 | ns |
| | | $t_h$ | -0.581 | -0.578 | -1.475 | -1.662 | -1.803 | -1.711 | -1.711 | -1.692 | -1.839 | -1.711 | -1.711 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | GCLK | $t_{su}$ | -1.137 | -1.216 | -1.849 | -1.877 | -2.030 | -1.953 | -2.400 | -1.901 | -2.052 | -1.953 | -2.400 | ns |
| | | $t_h$ | 1.274 | 1.369 | 2.088 | 2.122 | 2.297 | 2.206 | 2.656 | 2.156 | 2.330 | 2.206 | 2.656 | ns |
| | GCLK PLL | $t_{su}$ | 1.064 | 1.071 | 1.866 | 1.981 | 2.216 | 2.098 | 2.118 | 1.985 | 2.221 | 2.098 | 2.118 | ns |
| | | $t_h$ | -0.783 | -0.772 | -1.384 | -1.483 | -1.663 | -1.576 | -1.581 | -1.474 | -1.654 | -1.576 | -1.581 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | GCLK | $t_{su}$ | -1.137 | -1.216 | -1.849 | -1.877 | -2.030 | -1.953 | -2.400 | -1.901 | -2.052 | -1.953 | -2.400 | ns |
| | | $t_h$ | 1.274 | 1.369 | 2.088 | 2.122 | 2.297 | 2.206 | 2.656 | 2.156 | 2.330 | 2.206 | 2.656 | ns |
| | GCLK PLL | $t_{su}$ | 1.064 | 1.071 | 1.866 | 1.981 | 2.216 | 2.098 | 2.118 | 1.985 | 2.221 | 2.098 | 2.118 | ns |
| | | $t_h$ | -0.783 | -0.772 | -1.384 | -1.483 | -1.663 | -1.576 | -1.581 | -1.474 | -1.654 | -1.576 | -1.581 | ns |

**Table 1–136.** EP3SE260 Row Pins Input Timing Parameters (Part 2 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | GCLK | $t_{su}$ | -1.146 | -1.228 | -1.858 | -1.887 | -2.046 | -1.969 | -2.416 | -1.910 | -2.068 | -1.969 | -2.416 | ns |
| | | $t_h$ | 1.283 | 1.381 | 2.097 | 2.132 | 2.313 | 2.222 | 2.672 | 2.165 | 2.346 | 2.222 | 2.672 | ns |
| | GCLK PLL | $t_{su}$ | 1.055 | 1.059 | 1.857 | 1.971 | 2.200 | 2.082 | 2.102 | 1.976 | 2.205 | 2.082 | 2.102 | ns |
| | | $t_h$ | -0.774 | -0.760 | -1.375 | -1.473 | -1.647 | -1.560 | -1.565 | -1.465 | -1.638 | -1.560 | -1.565 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | GCLK | $t_{su}$ | -1.146 | -1.228 | -1.858 | -1.887 | -2.046 | -1.969 | -2.416 | -1.910 | -2.068 | -1.969 | -2.416 | ns |
| | | $t_h$ | 1.283 | 1.381 | 2.097 | 2.132 | 2.313 | 2.222 | 2.672 | 2.165 | 2.346 | 2.222 | 2.672 | ns |
| | GCLK PLL | $t_{su}$ | 1.055 | 1.059 | 1.857 | 1.971 | 2.200 | 2.082 | 2.102 | 1.976 | 2.205 | 2.082 | 2.102 | ns |
| | | $t_h$ | -0.774 | -0.760 | -1.375 | -1.473 | -1.647 | -1.560 | -1.565 | -1.465 | -1.638 | -1.560 | -1.565 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | GCLK | $t_{su}$ | -1.160 | -1.240 | -1.867 | -1.897 | -2.064 | -1.987 | -2.434 | -1.921 | -2.085 | -1.987 | -2.434 | ns |
| | | $t_h$ | 1.297 | 1.393 | 2.106 | 2.142 | 2.331 | 2.240 | 2.690 | 2.176 | 2.363 | 2.240 | 2.690 | ns |
| | GCLK PLL | $t_{su}$ | 1.041 | 1.047 | 1.844 | 1.961 | 2.182 | 2.064 | 2.084 | 1.965 | 2.188 | 2.064 | 2.084 | ns |
| | | $t_h$ | -0.760 | -0.748 | -1.363 | -1.463 | -1.629 | -1.542 | -1.547 | -1.454 | -1.621 | -1.542 | -1.547 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | GCLK | $t_{su}$ | -1.160 | -1.240 | -1.867 | -1.897 | -2.064 | -1.987 | -2.434 | -1.921 | -2.085 | -1.987 | -2.434 | ns |
| | | $t_h$ | 1.297 | 1.393 | 2.106 | 2.142 | 2.331 | 2.240 | 2.690 | 2.176 | 2.363 | 2.240 | 2.690 | ns |
| | GCLK PLL | $t_{su}$ | 1.041 | 1.047 | 1.844 | 1.961 | 2.182 | 2.064 | 2.084 | 1.965 | 2.188 | 2.064 | 2.084 | ns |
| | | $t_h$ | -0.760 | -0.748 | -1.363 | -1.463 | -1.629 | -1.542 | -1.547 | -1.454 | -1.621 | -1.542 | -1.547 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | GCLK | $t_{su}$ | -1.146 | -1.228 | -1.858 | -1.887 | -2.046 | -1.969 | -2.416 | -1.910 | -2.068 | -1.969 | -2.416 | ns |
| | | $t_h$ | 1.283 | 1.381 | 2.097 | 2.132 | 2.313 | 2.222 | 2.672 | 2.165 | 2.346 | 2.222 | 2.672 | ns |
| | GCLK PLL | $t_{su}$ | 1.055 | 1.059 | 1.857 | 1.971 | 2.200 | 2.082 | 2.102 | 1.976 | 2.205 | 2.082 | 2.102 | ns |
| | | $t_h$ | -0.774 | -0.760 | -1.375 | -1.473 | -1.647 | -1.560 | -1.565 | -1.465 | -1.638 | -1.560 | -1.565 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | GCLK | $t_{su}$ | -1.146 | -1.228 | -1.858 | -1.887 | -2.046 | -1.969 | -2.416 | -1.910 | -2.068 | -1.969 | -2.416 | ns |
| | | $t_h$ | 1.283 | 1.381 | 2.097 | 2.132 | 2.313 | 2.222 | 2.672 | 2.165 | 2.346 | 2.222 | 2.672 | ns |
| | GCLK PLL | $t_{su}$ | 1.055 | 1.059 | 1.857 | 1.971 | 2.200 | 2.082 | 2.102 | 1.976 | 2.205 | 2.082 | 2.102 | ns |
| | | $t_h$ | -0.774 | -0.760 | -1.375 | -1.473 | -1.647 | -1.560 | -1.565 | -1.465 | -1.638 | -1.560 | -1.565 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS I | GCLK | $t_{su}$ | -1.160 | -1.240 | -1.867 | -1.897 | -2.064 | -1.987 | -2.434 | -1.921 | -2.085 | -1.987 | -2.434 | ns |
| | | $t_h$ | 1.297 | 1.393 | 2.106 | 2.142 | 2.331 | 2.240 | 2.690 | 2.176 | 2.363 | 2.240 | 2.690 | ns |
| | GCLK PLL | $t_{su}$ | 1.041 | 1.047 | 1.844 | 1.961 | 2.182 | 2.064 | 2.084 | 1.965 | 2.188 | 2.064 | 2.084 | ns |
| | | $t_h$ | -0.760 | -0.748 | -1.363 | -1.463 | -1.629 | -1.542 | -1.547 | -1.454 | -1.621 | -1.542 | -1.547 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | GCLK | $t_{su}$ | -1.160 | -1.240 | -1.867 | -1.897 | -2.064 | -1.987 | -2.434 | -1.921 | -2.085 | -1.987 | -2.434 | ns |
| | | $t_h$ | 1.297 | 1.393 | 2.106 | 2.142 | 2.331 | 2.240 | 2.690 | 2.176 | 2.363 | 2.240 | 2.690 | ns |
| | GCLK PLL | $t_{su}$ | 1.041 | 1.047 | 1.844 | 1.961 | 2.182 | 2.064 | 2.084 | 1.965 | 2.188 | 2.064 | 2.084 | ns |
| | | $t_h$ | -0.760 | -0.748 | -1.363 | -1.463 | -1.629 | -1.542 | -1.547 | -1.454 | -1.621 | -1.542 | -1.547 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | GCLK | $t_{su}$ | -1.169 | -1.249 | -1.881 | -1.908 | -2.071 | -1.995 | -2.440 | -1.928 | -2.086 | -1.995 | -2.440 | ns |
| | | $t_h$ | 1.306 | 1.402 | 2.121 | 2.156 | 2.341 | 2.250 | 2.701 | 2.186 | 2.369 | 2.250 | 2.701 | ns |
| | GCLK PLL | $t_{su}$ | 1.032 | 1.038 | 1.829 | 1.945 | 2.171 | 2.052 | 2.073 | 1.954 | 2.182 | 2.052 | 2.073 | ns |
| | | $t_h$ | -0.751 | -0.739 | -1.348 | -1.445 | -1.615 | -1.528 | -1.532 | -1.440 | -1.612 | -1.528 | -1.532 | ns |

**Table 1–136.** EP3SE260 Row Pins Input Timing Parameters (Part 3 of 3)

| I/O Standard | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 2.5-V SSTL CLASS II | GCLK | $t_{su}$ | -1.169 | -1.249 | -1.881 | -1.908 | -2.071 | -1.995 | -2.440 | -1.928 | -2.086 | -1.995 | -2.440 | ns |
| | | $t_h$ | 1.306 | 1.402 | 2.121 | 2.156 | 2.341 | 2.250 | 2.701 | 2.186 | 2.369 | 2.250 | 2.701 | ns |
| | GCLK PLL | $t_{su}$ | 1.032 | 1.038 | 1.829 | 1.945 | 2.171 | 2.052 | 2.073 | 1.954 | 2.182 | 2.052 | 2.073 | ns |
| | | $t_h$ | -0.751 | -0.739 | -1.348 | -1.445 | -1.615 | -1.528 | -1.532 | -1.440 | -1.612 | -1.528 | -1.532 | ns |

Table 1–137 lists the EP3SE260 column pins output timing parameters for differential I/O standards.

**Table 1–137.** EP3SE260 Column Pins Output Timing Parameters (Part 1 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.479 | 3.750 | 5.506 | 5.712 | 6.270 | 6.106 | 6.513 | 5.854 | 6.411 | 6.106 | 6.513 | ns |
| | | GCLK PLL | $t_{co}$ | 3.475 | 3.753 | 5.553 | 5.767 | 6.332 | 6.168 | 6.575 | 5.913 | 6.477 | 6.168 | 6.575 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.479 | 3.750 | 5.506 | 5.712 | 6.270 | 6.106 | 6.513 | 5.854 | 6.411 | 6.106 | 6.513 | ns |
| | | GCLK PLL | $t_{co}$ | 3.475 | 3.753 | 5.553 | 5.767 | 6.332 | 6.168 | 6.575 | 5.913 | 6.477 | 6.168 | 6.575 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.479 | 3.750 | 5.506 | 5.712 | 6.270 | 6.106 | 6.513 | 5.854 | 6.411 | 6.106 | 6.513 | ns |
| | | GCLK PLL | $t_{co}$ | 3.475 | 3.753 | 5.553 | 5.767 | 6.332 | 6.168 | 6.575 | 5.913 | 6.477 | 6.168 | 6.575 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.506 | 3.783 | 5.577 | 5.790 | 6.354 | 6.190 | 6.597 | 5.934 | 6.497 | 6.190 | 6.597 | ns |
| | | GCLK PLL | $t_{co}$ | 3.496 | 3.773 | 5.567 | 5.779 | 6.344 | 6.180 | 6.587 | 5.923 | 6.487 | 6.180 | 6.587 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.496 | 3.773 | 5.570 | 5.783 | 6.348 | 6.184 | 6.591 | 5.928 | 6.492 | 6.184 | 6.591 | ns |
| | | GCLK PLL | $t_{co}$ | 3.489 | 3.767 | 5.563 | 5.777 | 6.342 | 6.178 | 6.585 | 5.921 | 6.486 | 6.178 | 6.585 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.488 | 3.765 | 5.560 | 5.774 | 6.339 | 6.175 | 6.582 | 5.918 | 6.482 | 6.175 | 6.582 | ns |
| | | GCLK PLL | $t_{co}$ | 3.510 | 3.787 | 5.581 | 5.794 | 6.358 | 6.194 | 6.601 | 5.938 | 6.502 | 6.194 | 6.601 | ns |


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**Table 1–137.** EP3SE260 Column Pins Output Timing Parameters (Part 2 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.500 | 3.776 | 5.560 | 5.771 | 6.333 | 6.169 | 6.576 | 5.914 | 6.475 | 6.169 | 6.576 | ns |
| | | GCLK PLL | $t_{co}$ | 3.495 | 3.772 | 5.560 | 5.771 | 6.334 | 6.170 | 6.577 | 5.915 | 6.477 | 6.170 | 6.577 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.493 | 3.770 | 5.559 | 5.770 | 6.332 | 6.168 | 6.575 | 5.914 | 6.476 | 6.168 | 6.575 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.761 | 5.549 | 5.760 | 6.323 | 6.159 | 6.566 | 5.904 | 6.466 | 6.159 | 6.566 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.486 | 3.763 | 5.555 | 5.767 | 6.331 | 6.167 | 6.574 | 5.912 | 6.475 | 6.167 | 6.574 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.760 | 5.538 | 5.748 | 6.309 | 6.145 | 6.552 | 5.891 | 6.451 | 6.145 | 6.552 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.497 | 3.773 | 5.556 | 5.766 | 6.327 | 6.163 | 6.570 | 5.910 | 6.470 | 6.163 | 6.570 | ns |
| | | GCLK PLL | $t_{co}$ | 3.493 | 3.770 | 5.557 | 5.768 | 6.331 | 6.167 | 6.574 | 5.912 | 6.474 | 6.167 | 6.574 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.483 | 3.759 | 5.546 | 5.757 | 6.319 | 6.155 | 6.562 | 5.901 | 6.462 | 6.155 | 6.562 | ns |
| | | GCLK PLL | $t_{co}$ | 3.481 | 3.757 | 5.544 | 5.754 | 6.317 | 6.153 | 6.560 | 5.899 | 6.460 | 6.153 | 6.560 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.481 | 3.758 | 5.547 | 5.759 | 6.322 | 6.158 | 6.565 | 5.903 | 6.466 | 6.158 | 6.565 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.761 | 5.544 | 5.754 | 6.316 | 6.152 | 6.559 | 5.898 | 6.459 | 6.152 | 6.559 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.511 | 3.790 | 5.589 | 5.802 | 6.366 | 6.202 | 6.609 | 5.946 | 6.509 | 6.202 | 6.609 | ns |
| | | GCLK PLL | $t_{co}$ | 3.497 | 3.776 | 5.577 | 5.791 | 6.356 | 6.192 | 6.599 | 5.936 | 6.500 | 6.192 | 6.599 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.485 | 3.763 | 5.560 | 5.773 | 6.338 | 6.174 | 6.581 | 5.918 | 6.482 | 6.174 | 6.581 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.763 | 5.563 | 5.777 | 6.342 | 6.178 | 6.585 | 5.922 | 6.487 | 6.178 | 6.585 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.481 | 3.759 | 5.556 | 5.769 | 6.335 | 6.171 | 6.578 | 5.915 | 6.479 | 6.171 | 6.578 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.761 | 5.549 | 5.760 | 6.323 | 6.159 | 6.566 | 5.904 | 6.466 | 6.159 | 6.566 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.486 | 3.763 | 5.557 | 5.770 | 6.334 | 6.170 | 6.577 | 5.914 | 6.478 | 6.170 | 6.577 | ns |
| | | GCLK PLL | $t_{co}$ | 3.514 | 3.793 | 5.588 | 5.800 | 6.364 | 6.200 | 6.607 | 5.945 | 6.507 | 6.200 | 6.607 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.503 | 3.781 | 5.576 | 5.788 | 6.352 | 6.188 | 6.595 | 5.933 | 6.495 | 6.188 | 6.595 | ns |
| | | GCLK PLL | $t_{co}$ | 3.498 | 3.777 | 5.576 | 5.789 | 6.353 | 6.189 | 6.596 | 5.934 | 6.497 | 6.189 | 6.596 | ns |
| DIFFERENTIAL 1.5-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.484 | 3.762 | 5.558 | 5.770 | 6.334 | 6.170 | 6.577 | 5.915 | 6.479 | 6.170 | 6.577 | ns |
| | | GCLK PLL | $t_{co}$ | 3.482 | 3.760 | 5.556 | 5.768 | 6.332 | 6.168 | 6.575 | 5.913 | 6.476 | 6.168 | 6.575 | ns |

**Table 1–137.** EP3SE260 Column Pins Output Timing Parameters (Part 3 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.486 | 3.762 | 5.548 | 5.758 | 6.320 | 6.156 | 6.563 | 5.902 | 6.463 | 6.156 | 6.563 | ns |
| | | GCLK PLL | $t_{co}$ | 3.486 | 3.763 | 5.556 | 5.768 | 6.332 | 6.168 | 6.575 | 5.913 | 6.476 | 6.168 | 6.575 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.502 | 3.780 | 5.572 | 5.783 | 6.346 | 6.182 | 6.589 | 5.928 | 6.489 | 6.182 | 6.589 | ns |
| | | GCLK PLL | $t_{co}$ | 3.502 | 3.780 | 5.572 | 5.783 | 6.346 | 6.182 | 6.589 | 5.928 | 6.489 | 6.182 | 6.589 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.492 | 3.770 | 5.562 | 5.773 | 6.336 | 6.172 | 6.579 | 5.918 | 6.480 | 6.172 | 6.579 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.762 | 5.548 | 5.758 | 6.320 | 6.156 | 6.563 | 5.902 | 6.463 | 6.156 | 6.563 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.479 | 3.750 | 5.506 | 5.712 | 6.270 | 6.106 | 6.513 | 5.854 | 6.411 | 6.106 | 6.513 | ns |
| | | GCLK PLL | $t_{co}$ | 3.475 | 3.753 | 5.553 | 5.767 | 6.332 | 6.168 | 6.575 | 5.913 | 6.477 | 6.168 | 6.575 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.479 | 3.750 | 5.506 | 5.712 | 6.270 | 6.106 | 6.513 | 5.854 | 6.411 | 6.106 | 6.513 | ns |
| | | GCLK PLL | $t_{co}$ | 3.475 | 3.753 | 5.553 | 5.767 | 6.332 | 6.168 | 6.575 | 5.913 | 6.477 | 6.168 | 6.575 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.479 | 3.750 | 5.506 | 5.712 | 6.270 | 6.106 | 6.513 | 5.854 | 6.411 | 6.106 | 6.513 | ns |
| | | GCLK PLL | $t_{co}$ | 3.475 | 3.753 | 5.553 | 5.767 | 6.332 | 6.168 | 6.575 | 5.913 | 6.477 | 6.168 | 6.575 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.506 | 3.783 | 5.577 | 5.790 | 6.354 | 6.190 | 6.597 | 5.934 | 6.497 | 6.190 | 6.597 | ns |
| | | GCLK PLL | $t_{co}$ | 3.496 | 3.773 | 5.567 | 5.779 | 6.344 | 6.180 | 6.587 | 5.923 | 6.487 | 6.180 | 6.587 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.496 | 3.773 | 5.570 | 5.783 | 6.348 | 6.184 | 6.591 | 5.928 | 6.492 | 6.184 | 6.591 | ns |
| | | GCLK PLL | $t_{co}$ | 3.489 | 3.767 | 5.563 | 5.777 | 6.342 | 6.178 | 6.585 | 5.921 | 6.486 | 6.178 | 6.585 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.488 | 3.765 | 5.560 | 5.774 | 6.339 | 6.175 | 6.582 | 5.918 | 6.482 | 6.175 | 6.582 | ns |
| | | GCLK PLL | $t_{co}$ | 3.510 | 3.787 | 5.581 | 5.794 | 6.358 | 6.194 | 6.601 | 5.938 | 6.502 | 6.194 | 6.601 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.500 | 3.776 | 5.560 | 5.771 | 6.333 | 6.169 | 6.576 | 5.914 | 6.475 | 6.169 | 6.576 | ns |
| | | GCLK PLL | $t_{co}$ | 3.495 | 3.772 | 5.560 | 5.771 | 6.334 | 6.170 | 6.577 | 5.915 | 6.477 | 6.170 | 6.577 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.493 | 3.770 | 5.559 | 5.770 | 6.332 | 6.168 | 6.575 | 5.914 | 6.476 | 6.168 | 6.575 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.761 | 5.549 | 5.760 | 6.323 | 6.159 | 6.566 | 5.904 | 6.466 | 6.159 | 6.566 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.486 | 3.763 | 5.555 | 5.767 | 6.331 | 6.167 | 6.574 | 5.912 | 6.475 | 6.167 | 6.574 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.760 | 5.538 | 5.748 | 6.309 | 6.145 | 6.552 | 5.891 | 6.451 | 6.145 | 6.552 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.497 | 3.773 | 5.556 | 5.766 | 6.327 | 6.163 | 6.570 | 5.910 | 6.470 | 6.163 | 6.570 | ns |
| | | GCLK PLL | $t_{co}$ | 3.493 | 3.770 | 5.557 | 5.768 | 6.331 | 6.167 | 6.574 | 5.912 | 6.474 | 6.167 | 6.574 | ns |


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**Table 1–137.** EP3SE260 Column Pins Output Timing Parameters (Part 4 of 4)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.483 | 3.759 | 5.546 | 5.757 | 6.319 | 6.155 | 6.562 | 5.901 | 6.462 | 6.155 | 6.562 | ns |
| | | GCLK PLL | $t_{co}$ | 3.481 | 3.757 | 5.544 | 5.754 | 6.317 | 6.153 | 6.560 | 5.899 | 6.460 | 6.153 | 6.560 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.481 | 3.758 | 5.547 | 5.759 | 6.322 | 6.158 | 6.565 | 5.903 | 6.466 | 6.158 | 6.565 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.761 | 5.544 | 5.754 | 6.316 | 6.152 | 6.559 | 5.898 | 6.459 | 6.152 | 6.559 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.511 | 3.790 | 5.589 | 5.802 | 6.366 | 6.202 | 6.609 | 5.946 | 6.509 | 6.202 | 6.609 | ns |
| | | GCLK PLL | $t_{co}$ | 3.497 | 3.776 | 5.577 | 5.791 | 6.356 | 6.192 | 6.599 | 5.936 | 6.500 | 6.192 | 6.599 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.485 | 3.763 | 5.560 | 5.773 | 6.338 | 6.174 | 6.581 | 5.918 | 6.482 | 6.174 | 6.581 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.763 | 5.563 | 5.777 | 6.342 | 6.178 | 6.585 | 5.922 | 6.487 | 6.178 | 6.585 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.481 | 3.759 | 5.556 | 5.769 | 6.335 | 6.171 | 6.578 | 5.915 | 6.479 | 6.171 | 6.578 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.761 | 5.549 | 5.760 | 6.323 | 6.159 | 6.566 | 5.904 | 6.466 | 6.159 | 6.566 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.486 | 3.763 | 5.557 | 5.770 | 6.334 | 6.170 | 6.577 | 5.914 | 6.478 | 6.170 | 6.577 | ns |
| | | GCLK PLL | $t_{co}$ | 3.514 | 3.793 | 5.588 | 5.800 | 6.364 | 6.200 | 6.607 | 5.945 | 6.507 | 6.200 | 6.607 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.503 | 3.781 | 5.576 | 5.788 | 6.352 | 6.188 | 6.595 | 5.933 | 6.495 | 6.188 | 6.595 | ns |
| | | GCLK PLL | $t_{co}$ | 3.498 | 3.777 | 5.576 | 5.789 | 6.353 | 6.189 | 6.596 | 5.934 | 6.497 | 6.189 | 6.596 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.484 | 3.762 | 5.558 | 5.770 | 6.334 | 6.170 | 6.577 | 5.915 | 6.479 | 6.170 | 6.577 | ns |
| | | GCLK PLL | $t_{co}$ | 3.482 | 3.760 | 5.556 | 5.768 | 6.332 | 6.168 | 6.575 | 5.913 | 6.476 | 6.168 | 6.575 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.486 | 3.762 | 5.548 | 5.758 | 6.320 | 6.156 | 6.563 | 5.902 | 6.463 | 6.156 | 6.563 | ns |
| | | GCLK PLL | $t_{co}$ | 3.486 | 3.763 | 5.556 | 5.768 | 6.332 | 6.168 | 6.575 | 5.913 | 6.476 | 6.168 | 6.575 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.502 | 3.780 | 5.572 | 5.783 | 6.346 | 6.182 | 6.589 | 5.928 | 6.489 | 6.182 | 6.589 | ns |
| | | GCLK PLL | $t_{co}$ | 3.502 | 3.780 | 5.572 | 5.783 | 6.346 | 6.182 | 6.589 | 5.928 | 6.489 | 6.182 | 6.589 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.492 | 3.770 | 5.562 | 5.773 | 6.336 | 6.172 | 6.579 | 5.918 | 6.480 | 6.172 | 6.579 | ns |
| | | GCLK PLL | $t_{co}$ | 3.485 | 3.762 | 5.548 | 5.758 | 6.320 | 6.156 | 6.563 | 5.902 | 6.463 | 6.156 | 6.563 | ns |

Table 1–138 lists the EP3SE260 row pins output timing parameters for differential I/O standards.

**Table 1–138.** EP3SE260 Row Pins Output Timing Parameters (Part 1 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| LVDS | — | GCLK | $t_{co}$ | 3.152 | 3.376 | 4.936 | 5.115 | 5.637 | 5.478 | 5.865 | 5.239 | 5.762 | 5.478 | 5.865 | ns |
| | | GCLK PLL | $t_{co}$ | 3.536 | 3.812 | 5.604 | 5.814 | 6.381 | 6.214 | 6.593 | 5.962 | 6.531 | 6.214 | 6.593 | ns |
| LVDS_E_1R | — | GCLK | $t_{co}$ | 3.518 | 3.802 | 5.642 | 5.860 | 6.435 | 6.268 | 6.647 | 6.013 | 6.592 | 6.268 | 6.647 | ns |
| | | GCLK PLL | $t_{co}$ | 3.152 | 3.376 | 4.936 | 5.115 | 5.637 | 5.478 | 5.865 | 5.239 | 5.762 | 5.478 | 5.865 | ns |
| LVDS_E_3R | — | GCLK | $t_{co}$ | 3.536 | 3.812 | 5.604 | 5.814 | 6.381 | 6.214 | 6.593 | 5.962 | 6.531 | 6.214 | 6.593 | ns |
| | | GCLK PLL | $t_{co}$ | 3.518 | 3.802 | 5.642 | 5.860 | 6.435 | 6.268 | 6.647 | 6.013 | 6.592 | 6.268 | 6.647 | ns |
| MINI-LVDS | — | GCLK | $t_{co}$ | 3.152 | 3.376 | 4.936 | 5.115 | 5.637 | 5.478 | 5.865 | 5.239 | 5.762 | 5.478 | 5.865 | ns |
| | | GCLK PLL | $t_{co}$ | 3.536 | 3.812 | 5.604 | 5.814 | 6.381 | 6.214 | 6.593 | 5.962 | 6.531 | 6.214 | 6.593 | ns |
| MINI-LVDS_E_1R | — | GCLK | $t_{co}$ | 3.518 | 3.802 | 5.642 | 5.860 | 6.435 | 6.268 | 6.647 | 6.013 | 6.592 | 6.268 | 6.647 | ns |
| | | GCLK PLL | $t_{co}$ | 3.562 | 3.845 | 5.678 | 5.894 | 6.468 | 6.301 | 6.680 | 6.046 | 6.621 | 6.301 | 6.680 | ns |
| MINI-LVDS_E_3R | — | GCLK | $t_{co}$ | 3.548 | 3.831 | 5.665 | 5.881 | 6.455 | 6.288 | 6.667 | 6.032 | 6.608 | 6.288 | 6.667 | ns |
| | | GCLK PLL | $t_{co}$ | 3.544 | 3.827 | 5.663 | 5.881 | 6.456 | 6.289 | 6.668 | 6.032 | 6.610 | 6.289 | 6.668 | ns |
| RSDS | — | GCLK | $t_{co}$ | 3.560 | 3.842 | 5.664 | 5.878 | 6.450 | 6.283 | 6.662 | 6.029 | 6.603 | 6.283 | 6.662 | ns |
| | | GCLK PLL | $t_{co}$ | 3.549 | 3.832 | 5.660 | 5.874 | 6.447 | 6.280 | 6.659 | 6.026 | 6.600 | 6.280 | 6.659 | ns |
| RSDS_E_1R | — | GCLK | $t_{co}$ | 3.546 | 3.829 | 5.658 | 5.872 | 6.445 | 6.278 | 6.657 | 6.024 | 6.599 | 6.278 | 6.657 | ns |
| | | GCLK PLL | $t_{co}$ | 3.557 | 3.839 | 5.659 | 5.873 | 6.444 | 6.277 | 6.656 | 6.023 | 6.597 | 6.277 | 6.656 | ns |
| RSDS_E_3R | — | GCLK | $t_{co}$ | 3.547 | 3.830 | 5.657 | 5.871 | 6.443 | 6.276 | 6.655 | 6.023 | 6.597 | 6.276 | 6.655 | ns |
| | | GCLK PLL | $t_{co}$ | 3.533 | 3.816 | 5.642 | 5.856 | 6.429 | 6.262 | 6.641 | 6.008 | 6.582 | 6.262 | 6.641 | ns |
| DIFFERENTIAL 1.2-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.530 | 3.812 | 5.638 | 5.852 | 6.425 | 6.258 | 6.637 | 6.004 | 6.578 | 6.258 | 6.637 | ns |
| | | GCLK PLL | $t_{co}$ | 3.527 | 3.810 | 5.639 | 5.855 | 6.428 | 6.261 | 6.640 | 6.007 | 6.582 | 6.261 | 6.640 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.528 | 3.810 | 5.629 | 5.843 | 6.415 | 6.248 | 6.627 | 5.994 | 6.568 | 6.248 | 6.627 | ns |
| | | GCLK PLL | $t_{co}$ | 3.577 | 3.863 | 5.700 | 5.916 | 6.491 | 6.324 | 6.703 | 6.068 | 6.644 | 6.324 | 6.703 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.553 | 3.839 | 5.682 | 5.899 | 6.474 | 6.307 | 6.686 | 6.051 | 6.629 | 6.307 | 6.686 | ns |
| | | GCLK PLL | $t_{co}$ | 3.535 | 3.820 | 5.660 | 5.877 | 6.452 | 6.285 | 6.664 | 6.029 | 6.607 | 6.285 | 6.664 | ns |

**Table 1–138.** EP3SE260 Row Pins Output Timing Parameters (Part 2 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.5-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.581 | 3.866 | 5.700 | 5.916 | 6.490 | 6.323 | 6.702 | 6.068 | 6.644 | 6.323 | 6.702 | ns |
| | | GCLK PLL | $t_{co}$ | 3.566 | 3.851 | 5.686 | 5.901 | 6.475 | 6.308 | 6.687 | 6.053 | 6.629 | 6.308 | 6.687 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.555 | 3.840 | 5.681 | 5.898 | 6.472 | 6.305 | 6.684 | 6.050 | 6.627 | 6.305 | 6.684 | ns |
| | | GCLK PLL | $t_{co}$ | 3.535 | 3.820 | 5.658 | 5.874 | 6.449 | 6.282 | 6.661 | 6.027 | 6.603 | 6.282 | 6.661 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.532 | 3.816 | 5.654 | 5.871 | 6.445 | 6.278 | 6.657 | 6.023 | 6.600 | 6.278 | 6.657 | ns |
| | | GCLK PLL | $t_{co}$ | 3.537 | 3.820 | 5.645 | 5.859 | 6.431 | 6.264 | 6.643 | 6.010 | 6.584 | 6.264 | 6.643 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.530 | 3.813 | 5.644 | 5.860 | 6.434 | 6.267 | 6.646 | 6.013 | 6.589 | 6.267 | 6.646 | ns |
| | | GCLK PLL | $t_{co}$ | 3.568 | 3.852 | 5.682 | 5.897 | 6.470 | 6.303 | 6.682 | 6.049 | 6.624 | 6.303 | 6.682 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.550 | 3.835 | 5.667 | 5.882 | 6.455 | 6.288 | 6.667 | 6.034 | 6.609 | 6.288 | 6.667 | ns |
| | | GCLK PLL | $t_{co}$ | 3.536 | 3.819 | 5.644 | 5.858 | 6.430 | 6.263 | 6.642 | 6.010 | 6.584 | 6.263 | 6.642 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.152 | 3.376 | 4.936 | 5.115 | 5.637 | 5.478 | 5.865 | 5.239 | 5.762 | 5.478 | 5.865 | ns |
| | | GCLK PLL | $t_{co}$ | 3.536 | 3.812 | 5.604 | 5.814 | 6.381 | 6.214 | 6.593 | 5.962 | 6.531 | 6.214 | 6.593 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.518 | 3.802 | 5.642 | 5.860 | 6.435 | 6.268 | 6.647 | 6.013 | 6.592 | 6.268 | 6.647 | ns |
| | | GCLK PLL | $t_{co}$ | 3.152 | 3.376 | 4.936 | 5.115 | 5.637 | 5.478 | 5.865 | 5.239 | 5.762 | 5.478 | 5.865 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.536 | 3.812 | 5.604 | 5.814 | 6.381 | 6.214 | 6.593 | 5.962 | 6.531 | 6.214 | 6.593 | ns |
| | | GCLK PLL | $t_{co}$ | 3.518 | 3.802 | 5.642 | 5.860 | 6.435 | 6.268 | 6.647 | 6.013 | 6.592 | 6.268 | 6.647 | ns |
| DIFFERENTIAL 1.8-V HSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.152 | 3.376 | 4.936 | 5.115 | 5.637 | 5.478 | 5.865 | 5.239 | 5.762 | 5.478 | 5.865 | ns |
| | | GCLK PLL | $t_{co}$ | 3.536 | 3.812 | 5.604 | 5.814 | 6.381 | 6.214 | 6.593 | 5.962 | 6.531 | 6.214 | 6.593 | ns |
| DIFFERENTIAL 1.5-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.518 | 3.802 | 5.642 | 5.860 | 6.435 | 6.268 | 6.647 | 6.013 | 6.592 | 6.268 | 6.647 | ns |
| | | GCLK PLL | $t_{co}$ | 3.562 | 3.845 | 5.678 | 5.894 | 6.468 | 6.301 | 6.680 | 6.046 | 6.621 | 6.301 | 6.680 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.548 | 3.831 | 5.665 | 5.881 | 6.455 | 6.288 | 6.667 | 6.032 | 6.608 | 6.288 | 6.667 | ns |
| | | GCLK PLL | $t_{co}$ | 3.544 | 3.827 | 5.663 | 5.881 | 6.456 | 6.289 | 6.668 | 6.032 | 6.610 | 6.289 | 6.668 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.560 | 3.842 | 5.664 | 5.878 | 6.450 | 6.283 | 6.662 | 6.029 | 6.603 | 6.283 | 6.662 | ns |
| | | GCLK PLL | $t_{co}$ | 3.549 | 3.832 | 5.660 | 5.874 | 6.447 | 6.280 | 6.659 | 6.026 | 6.600 | 6.280 | 6.659 | ns |

**Table 1–138.** EP3SE260 Row Pins Output Timing Parameters (Part 3 of 3)

| I/O Standard | Current Strength | Clock | Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| DIFFERENTIAL 1.8-V SSTL CLASS I | 4mA | GCLK | $t_{co}$ | 3.546 | 3.829 | 5.658 | 5.872 | 6.445 | 6.278 | 6.657 | 6.024 | 6.599 | 6.278 | 6.657 | ns |
| | | GCLK PLL | $t_{co}$ | 3.557 | 3.839 | 5.659 | 5.873 | 6.444 | 6.277 | 6.656 | 6.023 | 6.597 | 6.277 | 6.656 | ns |
| | 6mA | GCLK | $t_{co}$ | 3.547 | 3.830 | 5.657 | 5.871 | 6.443 | 6.276 | 6.655 | 6.023 | 6.597 | 6.276 | 6.655 | ns |
| | | GCLK PLL | $t_{co}$ | 3.533 | 3.816 | 5.642 | 5.856 | 6.429 | 6.262 | 6.641 | 6.008 | 6.582 | 6.262 | 6.641 | ns |
| | 8mA | GCLK | $t_{co}$ | 3.530 | 3.812 | 5.638 | 5.852 | 6.425 | 6.258 | 6.637 | 6.004 | 6.578 | 6.258 | 6.637 | ns |
| | | GCLK PLL | $t_{co}$ | 3.527 | 3.810 | 5.639 | 5.855 | 6.428 | 6.261 | 6.640 | 6.007 | 6.582 | 6.261 | 6.640 | ns |
| | 10mA | GCLK | $t_{co}$ | 3.528 | 3.810 | 5.629 | 5.843 | 6.415 | 6.248 | 6.627 | 5.994 | 6.568 | 6.248 | 6.627 | ns |
| | | GCLK PLL | $t_{co}$ | 3.577 | 3.863 | 5.700 | 5.916 | 6.491 | 6.324 | 6.703 | 6.068 | 6.644 | 6.324 | 6.703 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.553 | 3.839 | 5.682 | 5.899 | 6.474 | 6.307 | 6.686 | 6.051 | 6.629 | 6.307 | 6.686 | ns |
| | | GCLK PLL | $t_{co}$ | 3.535 | 3.820 | 5.660 | 5.877 | 6.452 | 6.285 | 6.664 | 6.029 | 6.607 | 6.285 | 6.664 | ns |
| DIFFERENTIAL 1.8-V SSTL CLASS II | 8mA | GCLK | $t_{co}$ | 3.581 | 3.866 | 5.700 | 5.916 | 6.490 | 6.323 | 6.702 | 6.068 | 6.644 | 6.323 | 6.702 | ns |
| | | GCLK PLL | $t_{co}$ | 3.566 | 3.851 | 5.686 | 5.901 | 6.475 | 6.308 | 6.687 | 6.053 | 6.629 | 6.308 | 6.687 | ns |
| | 16mA | GCLK | $t_{co}$ | 3.555 | 3.840 | 5.681 | 5.898 | 6.472 | 6.305 | 6.684 | 6.050 | 6.627 | 6.305 | 6.684 | ns |
| | | GCLK PLL | $t_{co}$ | 3.535 | 3.820 | 5.658 | 5.874 | 6.449 | 6.282 | 6.661 | 6.027 | 6.603 | 6.282 | 6.661 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS I | 8mA | GCLK | $t_{co}$ | 3.532 | 3.816 | 5.654 | 5.871 | 6.445 | 6.278 | 6.657 | 6.023 | 6.600 | 6.278 | 6.657 | ns |
| | | GCLK PLL | $t_{co}$ | 3.537 | 3.820 | 5.645 | 5.859 | 6.431 | 6.264 | 6.643 | 6.010 | 6.584 | 6.264 | 6.643 | ns |
| | 12mA | GCLK | $t_{co}$ | 3.530 | 3.813 | 5.644 | 5.860 | 6.434 | 6.267 | 6.646 | 6.013 | 6.589 | 6.267 | 6.646 | ns |
| | | GCLK PLL | $t_{co}$ | 3.568 | 3.852 | 5.682 | 5.897 | 6.470 | 6.303 | 6.682 | 6.049 | 6.624 | 6.303 | 6.682 | ns |
| DIFFERENTIAL 2.5-V SSTL CLASS II | 16mA | GCLK | $t_{co}$ | 3.550 | 3.835 | 5.667 | 5.882 | 6.455 | 6.288 | 6.667 | 6.034 | 6.609 | 6.288 | 6.667 | ns |
| | | GCLK PLL | $t_{co}$ | 3.536 | 3.819 | 5.644 | 5.858 | 6.430 | 6.263 | 6.642 | 6.010 | 6.584 | 6.263 | 6.642 | ns |


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Table 1–139 and Table 1–140 list the EP3SE260 regional clock (RCLK) adder values that must be added to the GCLK values. Use these adder values to determine I/O timing when the I/O pin is driven using the regional clock. This applies to all I/O standards supported by Stratix III devices.

Table 1–139 lists the EP3SE260 column pin delay adders when using the regional clock.

**Table 1–139.** EP3SE260 Column Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.233 | 0.311 | 0.488 | 0.489 | 0.45 | 0.439 | 0.515 | 0.416 | 0.458 | 0.439 | 0.515 | ns |
| RCLK PLL input adder | -0.036 | 0.028 | 0.059 | 0.06 | 0.113 | 0.11 | -0.005 | -0.038 | 0.121 | 0.11 | -0.005 | ns |
| RCLK output adder | -0.204 | -0.237 | -0.334 | -0.331 | -0.413 | -0.405 | -0.44 | -0.32 | -0.371 | -0.405 | -0.44 | ns |
| RCLK PLL output adder | 1.899 | 1.965 | 3.193 | 3.323 | 3.677 | 3.512 | 3.802 | 3.346 | 3.705 | 3.512 | 3.802 | ns |

Table 1–140 lists the EP3SE260 row pin delay adders when using the regional clock in Stratix III devices.

**Table 1–140.** EP3SE260 Row Pin Delay Adders for Regional Clock

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| RCLK input adder | 0.244 | 0.293 | 0.438 | 0.412 | 0.471 | 0.427 | 0.577 | 0.421 | 0.452 | 0.427 | 0.577 | ns |
| RCLK PLL input adder | 0.124 | 0.134 | 0.21 | 0.215 | 0.234 | 0.228 | 0.297 | 0.217 | 0.239 | 0.228 | 0.297 | ns |
| RCLK output adder | -0.256 | -0.289 | -0.418 | -0.424 | -0.484 | -0.438 | -0.591 | -0.443 | -0.464 | -0.438 | -0.591 | ns |
| RCLK PLL output adder | -0.134 | -0.147 | -0.228 | -0.233 | -0.254 | -0.261 | -0.322 | -0.236 | -0.262 | -0.261 | -0.322 | ns |

## Dedicated Clock Pin Timing

Table 1–141 to Table 1–201 list clock pin timing for Stratix III devices when the clock is driven by the global clock, regional clock, periphery clock, and a PLL.

Table 1–141 lists the Stratix III clock timing parameters.

**Table 1–141.** Clock Timing Parameters for Stratix III Devices

| Symbol | Parameter |
|---|---|
| $t_{CIN}$ | Delay from the clock pad to the I/O input register |
| $t_{COUT}$ | Delay from the clock pad to the I/O output register |
| $t_{PLLCIN}$ | Delay from the PLL `inclk` pad to the I/O input register |
| $t_{PLLCOUT}$ | Delay from the PLL `inclk` pad to the I/O output register |

### EP3SL50 Clock Timing Parameters

Table 1–142 and Table 1–143 list the global clock timing parameters for EP3SL50 devices.

**Table 1–142.** EP3SL50 Column Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.736 | 1.737 | 2.436 | 2.691 | 3.056 | 2.925 | 3.433 | 2.691 | 3.056 | 2.925 | 3.433 | ns |
| $t_{COUT}$ | 1.736 | 1.737 | 2.436 | 2.691 | 3.056 | 2.925 | 3.433 | 2.691 | 3.056 | 2.925 | 3.433 | ns |
| $t_{PLLCIN}$ | -0.018 | -0.026 | -0.261 | -0.312 | -0.251 | -0.230 | -0.011 | -0.312 | 0.161 | -0.230 | -0.011 | ns |
| $t_{PLLCOUT}$ | -0.018 | -0.026 | -0.261 | -0.312 | -0.251 | -0.230 | -0.011 | -0.312 | 0.161 | -0.230 | -0.011 | ns |

**Table 1–143.** EP3SL50 Row Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.732 | 1.843 | 2.527 | 2.758 | 3.099 | 2.997 | 3.227 | 2.811 | 3.146 | 3.055 | 3.260 | ns |
| $t_{COUT}$ | 1.650 | 1.752 | 2.385 | 2.595 | 2.918 | 2.826 | 3.068 | 2.641 | 2.957 | 2.876 | 3.101 | ns |
| $t_{PLLCIN}$ | 0.048 | 0.116 | -0.142 | -0.216 | -0.181 | -0.136 | -0.188 | -0.173 | 0.265 | -0.087 | -0.230 | ns |
| $t_{PLLCOUT}$ | -0.034 | 0.025 | -0.284 | -0.379 | -0.362 | -0.307 | -0.347 | -0.343 | 0.076 | -0.266 | -0.389 | ns |

Table 1–144 and Table 1–145 list the regional clock timing parameters for EP3SL50 devices.

**Table 1–144.** EP3SL50 Column Pin Regional Clock Timing Specifications (Part 1 of 2)

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.689 | 1.669 | 2.371 | 2.645 | 3.004 | 2.719 | 3.136 | 2.645 | 3.009 | 2.719 | 3.136 | ns |
| $t_{COUT}$ | 1.689 | 1.669 | 2.371 | 2.645 | 3.004 | 2.719 | 3.136 | 2.645 | 3.009 | 2.719 | 3.136 | ns |

**Table 1–144.** EP3SL50 Column Pin Regional Clock Timing Specifications (Part 2 of 2)

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{PLLCIN}$ | -0.019 | -0.025 | -0.264 | -0.315 | -0.256 | -0.236 | -0.017 | -0.315 | 0.224 | -0.236 | -0.017 | ns |
| $t_{PLLCOUT}$ | -0.019 | -0.025 | -0.264 | -0.315 | -0.256 | -0.236 | -0.017 | -0.315 | 0.224 | -0.236 | -0.017 | ns |

**Table 1–145.** EP3SL50 Row Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.636 | 1.729 | 2.356 | 2.567 | 2.894 | 2.800 | 2.964 | 2.622 | 2.941 | 2.853 | 2.997 | ns |
| $t_{COUT}$ | 1.554 | 1.638 | 2.214 | 2.404 | 2.713 | 2.629 | 2.805 | 2.452 | 2.752 | 2.674 | 2.838 | ns |
| $t_{PLLCIN}$ | 0.018 | 0.084 | -0.178 | -0.255 | -0.222 | -0.169 | -0.226 | -0.203 | 0.298 | -0.123 | -0.272 | ns |
| $t_{PLLCOUT}$ | -0.064 | -0.007 | -0.320 | -0.418 | -0.403 | -0.340 | -0.385 | -0.373 | 0.109 | -0.302 | -0.431 | ns |

Table 1–146 and Table 1–147 list the periphery clock timing parameters for EP3SL50 devices.

**Table 1–146.** EP3SL50 Column Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.468 | 1.469 | 2.143 | 2.418 | 2.797 | 2.668 | 3.219 | 2.418 | 2.801 | 2.668 | 3.219 | ns |
| $t_{COUT}$ | 1.468 | 1.469 | 2.143 | 2.418 | 2.797 | 2.668 | 3.219 | 2.418 | 2.801 | 2.668 | 3.219 | ns |
| $t_{PLLCIN}$ | -0.081 | -0.081 | -0.327 | -0.383 | -0.334 | -0.310 | -0.105 | -0.383 | 0.273 | -0.310 | -0.105 | ns |
| $t_{PLLCOUT}$ | -0.081 | -0.081 | -0.327 | -0.383 | -0.334 | -0.310 | -0.105 | -0.383 | 0.273 | -0.310 | -0.105 | ns |

**Table 1–147.** EP3SL50 Row Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.482 | 1.556 | 2.223 | 2.488 | 2.859 | 2.740 | 3.034 | 2.539 | 2.897 | 2.785 | 3.056 | ns |
| $t_{COUT}$ | 1.400 | 1.465 | 2.078 | 2.325 | 2.678 | 2.569 | 2.875 | 2.369 | 2.708 | 2.606 | 2.897 | ns |
| $t_{PLLCIN}$ | -0.014 | 0.042 | -0.222 | -0.299 | -0.278 | -0.224 | -0.295 | -0.256 | 0.368 | -0.177 | -0.257 | ns |
| $t_{PLLCOUT}$ | -0.096 | -0.049 | -0.364 | -0.462 | -0.459 | -0.395 | -0.454 | -0.426 | 0.179 | -0.356 | -0.416 | ns |

## EP3SL70 Clock Timing Parameters

Table 1–148 and Table 1–149 list the global clock timing specifications for EP3SL70 devices.

**Table 1–148.** EP3SL70 Column Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.749 | 1.735 | 2.434 | 2.702 | 3.056 | 2.950 | 3.403 | 2.702 | 3.056 | 2.950 | 3.403 | ns |
| $t_{COUT}$ | 1.749 | 1.735 | 2.434 | 2.702 | 3.056 | 2.950 | 3.403 | 2.702 | 3.056 | 2.950 | 3.403 | ns |
| $t_{PLLCIN}$ | -0.012 | -0.021 | -0.255 | -0.306 | -0.251 | -0.203 | -0.044 | -0.306 | 0.161 | -0.203 | -0.044 | ns |
| $t_{PLLCOUT}$ | -0.012 | -0.021 | -0.255 | -0.306 | -0.251 | -0.203 | -0.044 | -0.306 | 0.161 | -0.203 | -0.044 | ns |

**Table 1–149.** EP3SL70 Row Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.732 | 1.840 | 2.524 | 2.758 | 3.083 | 2.986 | 3.227 | 2.811 | 3.157 | 3.042 | 3.260 | ns |
| $t_{COUT}$ | 1.650 | 1.749 | 2.382 | 2.595 | 2.902 | 2.815 | 3.068 | 2.641 | 2.968 | 2.863 | 3.101 | ns |
| $t_{PLLCIN}$ | 0.051 | 0.115 | -0.144 | -0.219 | -0.193 | -0.144 | -0.188 | -0.170 | 0.275 | -0.097 | -0.234 | ns |
| $t_{PLLCOUT}$ | -0.031 | 0.024 | -0.286 | -0.382 | -0.374 | -0.315 | -0.347 | -0.340 | 0.086 | -0.276 | -0.393 | ns |

Table 1–150 and Table 1–151 list the regional clock timing parameters for EP3SL70 devices.

**Table 1–150.** EP3SL70 Column Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.689 | 1.689 | 2.388 | 2.649 | 3.004 | 2.723 | 3.132 | 2.649 | 3.014 | 2.723 | 3.132 | ns |
| $t_{COUT}$ | 1.689 | 1.689 | 2.388 | 2.649 | 3.004 | 2.723 | 3.132 | 2.649 | 3.014 | 2.723 | 3.132 | ns |
| $t_{PLLCIN}$ | -0.011 | -0.022 | -0.261 | -0.308 | -0.256 | -0.207 | -0.054 | -0.308 | 0.224 | -0.207 | -0.054 | ns |
| $t_{PLLCOUT}$ | -0.011 | -0.022 | -0.261 | -0.308 | -0.256 | -0.207 | -0.054 | -0.308 | 0.224 | -0.207 | -0.054 | ns |

**Table 1–151.** EP3SL70 Row Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.637 | 1.726 | 2.353 | 2.566 | 2.885 | 2.786 | 2.964 | 2.625 | 2.948 | 2.839 | 3.001 | ns |
| $t_{COUT}$ | 1.555 | 1.635 | 2.211 | 2.403 | 2.704 | 2.615 | 2.805 | 2.455 | 2.759 | 2.660 | 2.842 | ns |
| $t_{PLLCIN}$ | 0.018 | 0.085 | -0.176 | -0.252 | -0.230 | -0.180 | -0.226 | -0.203 | 0.307 | -0.139 | -0.272 | ns |
| $t_{PLLCOUT}$ | -0.064 | -0.006 | -0.318 | -0.415 | -0.411 | -0.351 | -0.385 | -0.373 | 0.118 | -0.318 | -0.431 | ns |

Table 1–152 and Table 1–153 list the periphery clock timing parameters for EP3SL70 devices.

**Table 1–152.** EP3SL70 Column Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.465 | 1.468 | 2.142 | 2.410 | 2.792 | 2.673 | 3.220 | 2.410 | 2.802 | 2.673 | 3.220 | ns |
| $t_{COUT}$ | 1.465 | 1.468 | 2.142 | 2.410 | 2.792 | 2.673 | 3.220 | 2.410 | 2.802 | 2.673 | 3.220 | ns |
| $t_{PLLCIN}$ | -0.068 | -0.083 | -0.330 | -0.370 | -0.334 | -0.288 | -0.133 | -0.370 | 0.273 | -0.288 | -0.133 | ns |
| $t_{PLLCOUT}$ | -0.068 | -0.083 | -0.330 | -0.370 | -0.334 | -0.288 | -0.133 | -0.370 | 0.273 | -0.288 | -0.133 | ns |

**Table 1–153.** EP3SL70 Row Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.482 | 1.558 | 2.227 | 2.488 | 2.851 | 2.727 | 3.031 | 2.539 | 2.905 | 2.777 | 3.056 | ns |
| $t_{COUT}$ | 1.400 | 1.467 | 2.082 | 2.325 | 2.670 | 2.556 | 2.872 | 2.369 | 2.716 | 2.598 | 2.897 | ns |
| $t_{PLLCIN}$ | -0.019 | 0.039 | -0.225 | -0.302 | -0.291 | -0.235 | -0.295 | -0.261 | 0.376 | -0.188 | -0.257 | ns |
| $t_{PLLCOUT}$ | -0.101 | -0.052 | -0.367 | -0.465 | -0.472 | -0.406 | -0.454 | -0.431 | 0.187 | -0.367 | -0.416 | ns |

## EP3SL110 Clock Timing Parameters

Table 1–154 and Table 1–155 list the global clock timing parameters for EP3SL110 devices.

**Table 1–154.** EP3SL110 Column Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.909 | 1.907 | 2.674 | 2.936 | 3.285 | 3.182 | 3.700 | 2.936 | 3.285 | 3.182 | 3.700 | ns |
| $t_{COUT}$ | 1.909 | 1.907 | 2.674 | 2.936 | 3.285 | 3.182 | 3.700 | 2.936 | 3.285 | 3.182 | 3.700 | ns |
| $t_{PLLCIN}$ | -0.048 | -0.050 | -0.274 | -0.330 | -0.290 | -0.251 | -0.032 | -0.330 | -0.290 | -0.251 | -0.032 | ns |
| $t_{PLLCOUT}$ | -0.048 | -0.050 | -0.274 | -0.330 | -0.290 | -0.251 | -0.032 | -0.330 | -0.290 | -0.251 | -0.032 | ns |

**Table 1–155.** EP3SL110 Row Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.882 | 2.014 | 2.754 | 2.975 | 3.344 | 3.221 | 3.511 | 3.062 | 3.413 | 3.287 | 3.551 | ns |
| $t_{COUT}$ | 1.800 | 1.923 | 2.612 | 2.812 | 3.163 | 3.050 | 3.352 | 2.892 | 3.224 | 3.108 | 3.392 | ns |
| $t_{PLLCIN}$ | -0.002 | 0.059 | -0.202 | -0.271 | -0.231 | -0.184 | -0.212 | -0.219 | -0.184 | -0.138 | -0.260 | ns |
| $t_{PLLCOUT}$ | -0.084 | -0.032 | -0.347 | -0.434 | -0.412 | -0.355 | -0.371 | -0.389 | -0.373 | -0.317 | -0.419 | ns |

Table 1–156 and Table 1–157 list the regional clock timing parameters for EP3SL110 devices.

**Table 1–156.** EP3SL110 Column Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.689 | 1.687 | 2.360 | 2.600 | 2.924 | 2.836 | 3.241 | 2.600 | 2.924 | 2.836 | 3.241 | ns |
| $t_{COUT}$ | 1.689 | 1.687 | 2.360 | 2.600 | 2.924 | 2.836 | 3.241 | 2.600 | 2.924 | 2.836 | 3.241 | ns |
| $t_{PLLCIN}$ | -0.036 | -0.038 | -0.262 | -0.317 | -0.278 | -0.239 | -0.020 | -0.317 | -0.278 | -0.239 | -0.020 | ns |
| $t_{PLLCOUT}$ | -0.036 | -0.038 | -0.262 | -0.317 | -0.278 | -0.239 | -0.020 | -0.317 | -0.278 | -0.239 | -0.020 | ns |

**Table 1–157.** EP3SL110 Row Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.684 | 1.792 | 2.440 | 2.644 | 2.985 | 2.879 | 3.044 | 2.720 | 3.044 | 2.938 | 3.083 | ns |
| $t_{COUT}$ | 1.602 | 1.701 | 2.298 | 2.481 | 2.804 | 2.708 | 2.885 | 2.550 | 2.855 | 2.759 | 2.924 | ns |
| $t_{PLLCIN}$ | 0.008 | 0.071 | -0.189 | -0.276 | -0.218 | -0.188 | -0.214 | -0.209 | -0.174 | -0.141 | -0.263 | ns |
| $t_{PLLCOUT}$ | -0.074 | -0.020 | -0.334 | -0.439 | -0.399 | -0.359 | -0.373 | -0.379 | -0.363 | -0.320 | -0.422 | ns |

Table 1–158 and Table 1–159 list the periphery clock timing parameters for EP3SL110 devices.

**Table 1–158.** EP3SL110 Column Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.541 | 1.538 | 2.257 | 2.539 | 2.931 | 2.810 | 3.345 | 2.539 | 2.931 | 2.810 | 3.345 | ns |
| $t_{COUT}$ | 1.541 | 1.538 | 2.257 | 2.539 | 2.931 | 2.810 | 3.345 | 2.539 | 2.931 | 2.810 | 3.345 | ns |
| $t_{PLLCIN}$ | -0.029 | -0.031 | -0.253 | -0.310 | -0.276 | -0.222 | -0.020 | -0.310 | -0.276 | -0.222 | -0.020 | ns |
| $t_{PLLCOUT}$ | -0.029 | -0.031 | -0.253 | -0.310 | -0.276 | -0.222 | -0.020 | -0.310 | -0.276 | -0.222 | -0.020 | ns |

**Table 1–159.** EP3SL110 Row Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.430 | 1.503 | 2.156 | 2.416 | 2.783 | 2.665 | 2.926 | 2.465 | 2.828 | 2.711 | 2.951 | ns |
| $t_{COUT}$ | 1.348 | 1.412 | 2.011 | 2.253 | 2.602 | 2.494 | 2.767 | 2.295 | 2.639 | 2.532 | 2.792 | ns |
| $t_{PLLCIN}$ | 0.015 | 0.072 | -0.188 | -0.267 | -0.219 | -0.180 | -0.214 | -0.206 | -0.170 | -0.133 | -0.263 | ns |
| $t_{PLLCOUT}$ | -0.067 | -0.019 | -0.333 | -0.430 | -0.400 | -0.351 | -0.373 | -0.376 | -0.359 | -0.312 | -0.422 | ns |

## EP3SL150 Clock Timing Parameters

Table 1–160 and Table 1–161 list the global clock timing parameters for EP3SL150 devices.

**Table 1–160.** EP3SL150 Column Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.898 | 1.926 | 2.692 | 2.920 | 3.294 | 3.170 | 3.719 | 2.920 | 3.294 | 3.170 | 3.719 | ns |
| $t_{COUT}$ | 1.898 | 1.926 | 2.692 | 2.920 | 3.294 | 3.170 | 3.719 | 2.920 | 3.294 | 3.170 | 3.719 | ns |
| $t_{PLLCIN}$ | -0.054 | -0.028 | -0.252 | -0.342 | -0.296 | -0.239 | -0.018 | -0.342 | -0.296 | -0.239 | -0.018 | ns |
| $t_{PLLCOUT}$ | -0.054 | -0.028 | -0.252 | -0.342 | -0.296 | -0.239 | -0.018 | -0.342 | -0.296 | -0.239 | -0.018 | ns |

**Table 1–161.** EP3SL150 Row Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.868 | 2.010 | 2.750 | 2.982 | 3.347 | 3.224 | 3.506 | 3.048 | 3.400 | 3.293 | 3.549 | ns |
| $t_{COUT}$ | 1.786 | 1.919 | 2.608 | 2.819 | 3.166 | 3.053 | 3.347 | 2.878 | 3.211 | 3.114 | 3.390 | ns |
| $t_{PLLCIN}$ | 0.007 | 0.059 | -0.202 | -0.255 | -0.231 | -0.184 | -0.214 | -0.210 | -0.173 | -0.122 | -0.249 | ns |
| $t_{PLLCOUT}$ | -0.075 | -0.032 | -0.347 | -0.418 | -0.412 | -0.355 | -0.373 | -0.380 | -0.362 | -0.301 | -0.408 | ns |

Table 1–162 and Table 1–163 list the regional clock timing parameters for EP3SL150 devices.

**Table 1–162.** EP3SL150 Column Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.683 | 1.701 | 2.375 | 2.595 | 2.936 | 2.833 | 3.255 | 2.595 | 2.936 | 2.833 | 3.255 | ns |
| $t_{COUT}$ | 1.683 | 1.701 | 2.375 | 2.595 | 2.936 | 2.833 | 3.255 | 2.595 | 2.936 | 2.833 | 3.255 | ns |
| $t_{PLLCIN}$ | -0.043 | -0.016 | -0.240 | -0.329 | -0.284 | -0.227 | -0.005 | -0.329 | -0.284 | -0.227 | -0.005 | ns |
| $t_{PLLCOUT}$ | -0.043 | -0.016 | -0.240 | -0.329 | -0.284 | -0.227 | -0.005 | -0.329 | -0.284 | -0.227 | -0.005 | ns |

**Table 1–163.** EP3SL150 Row Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.683 | 1.793 | 2.441 | 2.659 | 2.987 | 2.875 | 3.042 | 2.719 | 3.047 | 2.951 | 3.096 | ns |
| $t_{COUT}$ | 1.601 | 1.702 | 2.299 | 2.496 | 2.806 | 2.704 | 2.883 | 2.549 | 2.858 | 2.772 | 2.937 | ns |
| $t_{PLLCIN}$ | -0.007 | 0.068 | -0.192 | -0.269 | -0.221 | -0.188 | -0.211 | -0.226 | -0.186 | -0.135 | -0.260 | ns |
| $t_{PLLCOUT}$ | -0.089 | -0.023 | -0.337 | -0.432 | -0.402 | -0.359 | -0.370 | -0.396 | -0.375 | -0.314 | -0.419 | ns |

Table 1–164 and Table 1–165 list the periphery clock timing parameters for EP3SL150 devices.

**Table 1–164.** EP3SL150 Column Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.537 | 1.550 | 2.268 | 2.535 | 2.929 | 2.812 | 3.354 | 2.535 | 2.929 | 2.812 | 3.354 | ns |
| $t_{COUT}$ | 1.537 | 1.550 | 2.268 | 2.535 | 2.929 | 2.812 | 3.354 | 2.535 | 2.929 | 2.812 | 3.354 | ns |
| $t_{PLLCIN}$ | -0.040 | -0.012 | -0.235 | -0.326 | -0.267 | -0.234 | 0.002 | -0.326 | -0.267 | -0.234 | 0.002 | ns |
| $t_{PLLCOUT}$ | -0.040 | -0.012 | -0.235 | -0.326 | -0.267 | -0.234 | 0.002 | -0.326 | -0.267 | -0.234 | 0.002 | ns |

**Table 1–165.** EP3SL150 Row Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.438 | 1.505 | 2.159 | 2.429 | 2.783 | 2.657 | 2.934 | 2.475 | 2.838 | 2.725 | 2.972 | ns |
| $t_{COUT}$ | 1.356 | 1.414 | 2.014 | 2.266 | 2.602 | 2.486 | 2.775 | 2.305 | 2.649 | 2.546 | 2.813 | ns |
| $t_{PLLCIN}$ | 0.002 | 0.076 | -0.183 | -0.266 | -0.217 | -0.185 | -0.206 | -0.220 | -0.182 | -0.132 | -0.260 | ns |
| $t_{PLLCOUT}$ | -0.080 | -0.015 | -0.328 | -0.429 | -0.398 | -0.356 | -0.365 | -0.390 | -0.371 | -0.311 | -0.419 | ns |

### EP3SL200 Clock Timing Parameters

Table 1–166 and Table 1–167 list the global clock timing parameters for EP3SL200 devices.

**Table 1–166.** EP3SL200 Column Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 2.237 | 2.264 | 3.331 | 3.416 | 3.842 | 3.686 | 4.345 | 3.416 | 3.834 | 3.686 | 4.345 | ns |
| $t_{COUT}$ | 2.237 | 2.264 | 3.331 | 3.416 | 3.842 | 3.686 | 4.345 | 3.416 | 3.834 | 3.686 | 4.345 | ns |
| $t_{PLLCIN}$ | 0.032 | 0.060 | -0.177 | -0.219 | -0.137 | -0.122 | 0.088 | -0.219 | 0.287 | -0.122 | 0.088 | ns |
| $t_{PLLCOUT}$ | 0.032 | 0.060 | -0.177 | -0.219 | -0.137 | -0.122 | 0.088 | -0.219 | 0.287 | -0.122 | 0.088 | ns |

**Table 1–167.** EP3SL200 Row Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 2.208 | 2.371 | 3.453 | 3.526 | 3.900 | 3.747 | 4.190 | 3.601 | 3.977 | 3.747 | 4.190 | ns |
| $t_{COUT}$ | 2.126 | 2.280 | 3.301 | 3.366 | 3.719 | 3.576 | 4.031 | 3.433 | 3.788 | 3.576 | 4.031 | ns |
| $t_{PLLCIN}$ | 0.102 | 0.174 | -0.085 | -0.115 | -0.076 | -0.043 | -0.063 | -0.067 | 0.409 | -0.043 | -0.063 | ns |
| $t_{PLLCOUT}$ | 0.020 | 0.083 | -0.237 | -0.278 | -0.257 | -0.214 | -0.222 | -0.237 | 0.220 | -0.214 | -0.222 | ns |

Table 1–168 and Table 1–169 list the regional clock timing parameters for EP3SL200.

**Table 1–168.** EP3SL200 Column Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 2.006 | 2.035 | 3.020 | 3.113 | 3.494 | 3.213 | 3.743 | 3.113 | 3.531 | 3.213 | 3.743 | ns |
| $t_{COUT}$ | 2.006 | 2.035 | 3.020 | 3.113 | 3.494 | 3.213 | 3.743 | 3.113 | 3.531 | 3.213 | 3.743 | ns |
| $t_{PLLCIN}$ | 0.059 | 0.086 | -0.150 | -0.191 | -0.109 | -0.094 | 0.116 | -0.191 | 0.291 | -0.094 | 0.116 | ns |
| $t_{PLLCOUT}$ | 0.059 | 0.086 | -0.150 | -0.191 | -0.109 | -0.094 | 0.116 | -0.191 | 0.291 | -0.094 | 0.116 | ns |

**Table 1–169.** EP3SL200 Row Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.937 | 2.065 | 3.000 | 3.070 | 3.414 | 3.275 | 3.597 | 3.139 | 3.479 | 3.275 | 3.597 | ns |
| $t_{COUT}$ | 1.855 | 1.974 | 2.848 | 2.910 | 3.233 | 3.104 | 3.438 | 2.971 | 3.290 | 3.104 | 3.438 | ns |
| $t_{PLLCIN}$ | 0.126 | 0.197 | -0.059 | -0.091 | -0.051 | -0.036 | -0.041 | -0.043 | 0.410 | -0.036 | -0.041 | ns |
| $t_{PLLCOUT}$ | 0.044 | 0.106 | -0.211 | -0.254 | -0.232 | -0.207 | -0.200 | -0.213 | 0.221 | -0.207 | -0.200 | ns |

Table 1–170 and Table 1–171 list the periphery clock timing parameters for EP3SL200 devices.

**Table 1–170.** EP3SL200 Column Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.720 | 1.712 | 2.615 | 2.776 | 3.177 | 3.044 | 3.660 | 2.776 | 3.177 | 3.044 | 3.660 | ns |
| $t_{COUT}$ | 1.720 | 1.712 | 2.615 | 2.776 | 3.177 | 3.044 | 3.660 | 2.776 | 3.177 | 3.044 | 3.660 | ns |
| $t_{PLLCIN}$ | 0.037 | 0.064 | -0.173 | -0.213 | -0.135 | -0.118 | 0.090 | -0.213 | 0.292 | -0.118 | 0.090 | ns |
| $t_{PLLCOUT}$ | 0.037 | 0.064 | -0.173 | -0.213 | -0.135 | -0.118 | 0.090 | -0.213 | 0.292 | -0.118 | 0.090 | ns |

**Table 1–171.** EP3SL200 Row Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.501 | 1.575 | 2.380 | 2.518 | 2.892 | 2.761 | 3.077 | 2.567 | 2.938 | 2.761 | 3.077 | ns |
| $t_{COUT}$ | 1.419 | 1.484 | 2.225 | 2.355 | 2.711 | 2.590 | 2.918 | 2.397 | 2.749 | 2.590 | 2.918 | ns |
| $t_{PLLCIN}$ | 0.105 | 0.174 | -0.081 | -0.118 | -0.077 | -0.061 | -0.063 | -0.067 | 0.411 | -0.061 | -0.063 | ns |
| $t_{PLLCOUT}$ | 0.023 | 0.083 | -0.233 | -0.281 | -0.258 | -0.232 | -0.222 | -0.237 | 0.222 | -0.232 | -0.222 | ns |

## EP3SL340 Clock Timing Parameters

Table 1–172 and Table 1–173 list the global clock timing parameters for EP3S340 devices.

**Table 1–172.** EP3SL340 Column Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 2.357 | 2.331 | 3.440 | 3.566 | 3.938 | 3.807 | 4.482 | 3.566 | 3.938 | 3.807 | 4.482 | ns |
| $t_{COUT}$ | 2.357 | 2.331 | 3.440 | 3.566 | 3.938 | 3.807 | 4.482 | 3.566 | 3.938 | 3.807 | 4.482 | ns |
| $t_{PLLCIN}$ | 0.091 | 0.058 | -0.165 | -0.152 | -0.140 | -0.096 | 0.111 | -0.152 | -0.140 | -0.096 | 0.111 | ns |
| $t_{PLLCOUT}$ | 0.091 | 0.058 | -0.165 | -0.152 | -0.140 | -0.096 | 0.111 | -0.152 | -0.140 | -0.096 | 0.111 | ns |

**Table 1–173.** EP3SL340 Row Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 2.293 | 2.479 | 3.608 | 3.630 | 4.020 | 3.880 | 4.324 | 3.746 | 4.099 | 3.977 | 4.369 | ns |
| $t_{COUT}$ | 2.211 | 2.388 | 3.456 | 3.470 | 3.839 | 3.709 | 4.165 | 3.578 | 3.910 | 3.798 | 4.210 | ns |
| $t_{PLLCIN}$ | 0.121 | 0.210 | -0.034 | -0.098 | -0.045 | -0.001 | -0.042 | -0.031 | 0.005 | 0.051 | -0.083 | ns |
| $t_{PLLCOUT}$ | 0.039 | 0.119 | -0.186 | -0.261 | -0.226 | -0.172 | -0.201 | -0.201 | -0.184 | -0.128 | -0.242 | ns |

Table 1–174 and Table 1–175 list the regional clock timing parameters for EP3SL340 devices.

**Table 1–174.** EP3SL340 Column Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 2.031 | 2.013 | 2.958 | 3.073 | 3.435 | 3.308 | 3.803 | 3.073 | 3.435 | 3.308 | 3.803 | ns |
| $t_{COUT}$ | 2.031 | 2.013 | 2.958 | 3.073 | 3.435 | 3.308 | 3.803 | 3.073 | 3.435 | 3.308 | 3.803 | ns |
| $t_{PLLCIN}$ | 0.127 | 0.094 | -0.128 | -0.116 | -0.104 | -0.061 | 0.148 | -0.116 | -0.104 | -0.061 | 0.148 | ns |
| $t_{PLLCOUT}$ | 0.127 | 0.094 | -0.128 | -0.116 | -0.104 | -0.061 | 0.148 | -0.116 | -0.104 | -0.061 | 0.148 | ns |

**Table 1–175.** EP3SL340 Row Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.998 | 2.161 | 3.129 | 3.149 | 3.501 | 3.376 | 3.648 | 3.242 | 3.570 | 3.463 | 3.707 | ns |
| $t_{COUT}$ | 1.916 | 2.070 | 2.977 | 2.989 | 3.320 | 3.205 | 3.492 | 3.074 | 3.381 | 3.284 | 3.551 | ns |
| $t_{PLLCIN}$ | 0.157 | 0.248 | 0.006 | -0.069 | -0.009 | 0.017 | -0.011 | 0.003 | 0.039 | 0.093 | -0.057 | ns |
| $t_{PLLCOUT}$ | 0.075 | 0.157 | -0.146 | -0.232 | -0.190 | -0.154 | -0.170 | -0.167 | -0.150 | -0.086 | -0.216 | ns |

Table 1–176 and Table 1–177 list the periphery clock timing parameters for EP3SL340 devices.

**Table 1–176.** EP3SL340 Column Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.778 | 1.760 | 2.687 | 2.847 | 3.240 | 3.099 | 3.718 | 2.847 | 3.240 | 3.099 | 3.718 | ns |
| $t_{COUT}$ | 1.778 | 1.760 | 2.687 | 2.847 | 3.240 | 3.099 | 3.718 | 2.847 | 3.240 | 3.099 | 3.718 | ns |
| $t_{PLLCIN}$ | 0.086 | 0.061 | -0.164 | -0.161 | -0.140 | -0.097 | 0.101 | -0.161 | -0.140 | -0.097 | 0.101 | ns |
| $t_{PLLCOUT}$ | 0.086 | 0.061 | -0.164 | -0.161 | -0.140 | -0.097 | 0.101 | -0.161 | -0.140 | -0.097 | 0.101 | ns |

**Table 1–177.** EP3SL340 Row Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.524 | 1.616 | 2.435 | 2.567 | 2.958 | 2.823 | 3.141 | 2.605 | 3.002 | 2.861 | 3.165 | ns |
| $t_{COUT}$ | 1.442 | 1.525 | 2.280 | 2.404 | 2.777 | 2.652 | 2.982 | 2.435 | 2.813 | 2.682 | 3.006 | ns |
| $t_{PLLCIN}$ | 0.116 | 0.211 | -0.039 | -0.116 | -0.055 | -0.030 | -0.051 | -0.040 | -0.006 | 0.050 | -0.098 | ns |
| $t_{PLLCOUT}$ | 0.034 | 0.120 | -0.191 | -0.279 | -0.236 | -0.201 | -0.210 | -0.210 | -0.195 | -0.129 | -0.257 | ns |

### EP3SE50 Clock Timing Parameters

Table 1–178 and Table 1–179 list the global clock timing parameters for EP3SE50 devices.

**Table 1–178.** EP3SE50 Column Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.786 | 1.789 | 2.495 | 2.748 | 3.111 | 2.993 | 3.489 | 2.748 | 3.105 | 2.993 | 3.489 | ns |
| $t_{COUT}$ | 1.786 | 1.789 | 2.495 | 2.748 | 3.111 | 2.993 | 3.489 | 2.748 | 3.105 | 2.993 | 3.489 | ns |
| $t_{PLLCIN}$ | 0.023 | 0.027 | -0.204 | -0.268 | -0.226 | -0.180 | 0.025 | -0.268 | 0.249 | -0.180 | 0.025 | ns |
| $t_{PLLCOUT}$ | 0.083 | 0.103 | -0.068 | -0.131 | -0.226 | -0.010 | 0.025 | -0.131 | 0.249 | -0.010 | 0.025 | ns |

**Table 1–179.** EP3SE50 Row Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.739 | 1.849 | 2.536 | 2.769 | 3.112 | 3.010 | 3.250 | 2.830 | 3.171 | 3.069 | 3.276 | ns |
| $t_{COUT}$ | 1.657 | 1.758 | 2.394 | 2.606 | 2.931 | 2.839 | 3.091 | 2.660 | 2.982 | 2.890 | 3.117 | ns |
| $t_{PLLCIN}$ | 0.044 | 0.117 | -0.143 | -0.220 | -0.183 | -0.135 | -0.189 | -0.171 | 0.345 | -0.088 | -0.242 | ns |
| $t_{PLLCOUT}$ | -0.038 | 0.026 | -0.285 | -0.383 | -0.364 | -0.306 | -0.348 | -0.341 | 0.156 | -0.267 | -0.401 | ns |

Table 1–180 and Table 1–181 list the regional clock timing parameters for EP3SE50 devices.

**Table 1–180.** EP3SE50 Column Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.711 | 1.721 | 2.429 | 2.679 | 3.053 | 2.767 | 3.191 | 2.679 | 3.053 | 2.767 | 3.191 | ns |
| $t_{COUT}$ | 1.711 | 1.721 | 2.429 | 2.679 | 3.053 | 2.767 | 3.191 | 2.679 | 3.053 | 2.767 | 3.191 | ns |
| $t_{PLLCIN}$ | 0.034 | 0.038 | -0.193 | -0.255 | -0.212 | -0.168 | 0.040 | -0.255 | 0.263 | -0.168 | 0.040 | ns |
| $t_{PLLCOUT}$ | 0.106 | 0.102 | -0.074 | -0.101 | -0.212 | -0.168 | 0.040 | -0.101 | 0.263 | -0.168 | 0.040 | ns |

**Table 1–181.** EP3SE50 Row Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.640 | 1.732 | 2.361 | 2.580 | 2.905 | 2.810 | 2.977 | 2.636 | 2.960 | 2.868 | 3.003 | ns |
| $t_{COUT}$ | 1.558 | 1.641 | 2.219 | 2.417 | 2.724 | 2.639 | 2.818 | 2.466 | 2.771 | 2.689 | 2.844 | ns |
| $t_{PLLCIN}$ | 0.020 | 0.091 | -0.168 | -0.241 | -0.208 | -0.155 | -0.210 | -0.191 | 0.321 | -0.108 | -0.264 | ns |
| $t_{PLLCOUT}$ | -0.062 | 0.000 | -0.310 | -0.404 | -0.389 | -0.326 | -0.369 | -0.361 | 0.132 | -0.287 | -0.423 | ns |

Table 1–182 and Table 1–183 list the periphery clock timing parameters for EP3SE50 devices.

**Table 1–182.** EP3SE50 Column Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.472 | 1.481 | 2.155 | 2.417 | 2.825 | 2.681 | 3.247 | 2.417 | 2.819 | 2.681 | 3.247 | ns |
| $t_{COUT}$ | 1.472 | 1.481 | 2.155 | 2.417 | 2.825 | 2.681 | 3.247 | 2.417 | 2.819 | 2.681 | 3.247 | ns |
| $t_{PLLCIN}$ | -0.047 | -0.044 | -0.288 | -0.347 | -0.302 | -0.266 | -0.079 | -0.347 | 0.300 | -0.266 | -0.079 | ns |
| $t_{PLLCOUT}$ | -0.047 | -0.044 | -0.288 | -0.347 | -0.302 | -0.266 | -0.079 | -0.347 | 0.300 | -0.266 | -0.079 | ns |

**Table 1–183.** EP3SE50 Row Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.467 | 1.543 | 2.208 | 2.472 | 2.843 | 2.729 | 3.012 | 2.521 | 2.891 | 2.771 | 3.028 | ns |
| $t_{COUT}$ | 1.385 | 1.452 | 2.063 | 2.309 | 2.662 | 2.558 | 2.853 | 2.351 | 2.702 | 2.592 | 2.869 | ns |
| $t_{PLLCIN}$ | -0.021 | 0.036 | -0.231 | -0.307 | -0.282 | -0.230 | -0.301 | -0.262 | 0.372 | -0.184 | -0.361 | ns |
| $t_{PLLCOUT}$ | -0.103 | -0.055 | -0.373 | -0.470 | -0.463 | -0.401 | -0.460 | -0.432 | 0.183 | -0.363 | -0.520 | ns |

## EP3SE80 Clock Timing Parameters

Table 1–184 and Table 1–185 list the global clock timing parameters for EP3SE80 devices.

**Table 1–184.** EP3SE80 Column Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 2.037 | 2.059 | 2.879 | 3.127 | 3.524 | 3.430 | 3.989 | 3.127 | 3.524 | 3.430 | 3.989 | ns |
| $t_{COUT}$ | 2.037 | 2.059 | 2.879 | 3.127 | 3.524 | 3.430 | 3.989 | 3.127 | 3.524 | 3.430 | 3.989 | ns |
| $t_{PLLCIN}$ | -0.024 | -0.007 | -0.235 | -0.315 | -0.292 | -0.199 | -0.042 | -0.315 | -0.292 | -0.199 | -0.042 | ns |
| $t_{PLLCOUT}$ | -0.024 | -0.007 | -0.235 | -0.315 | -0.292 | -0.199 | -0.042 | -0.315 | -0.292 | -0.199 | -0.042 | ns |

**Table 1–185.** EP3SE80 Row Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.994 | 2.143 | 2.942 | 3.188 | 3.552 | 3.446 | 3.769 | 3.258 | 3.633 | 3.515 | 3.813 | ns |
| $t_{COUT}$ | 1.912 | 2.052 | 2.800 | 3.025 | 3.371 | 3.275 | 3.610 | 3.089 | 3.444 | 3.336 | 3.654 | ns |
| $t_{PLLCIN}$ | 0.020 | 0.086 | -0.177 | -0.249 | -0.221 | -0.171 | -0.221 | -0.199 | -0.173 | -0.121 | -0.266 | ns |
| $t_{PLLCOUT}$ | -0.062 | -0.005 | -0.319 | -0.412 | -0.402 | -0.342 | -0.380 | -0.369 | -0.362 | -0.300 | -0.425 | ns |

Table 1–186 and Table 1–187 list the regional clock timing parameters for EP3SE80 devices.

**Table 1–186.** EP3SE80 Column Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.828 | 1.849 | 2.578 | 2.811 | 3.171 | 3.087 | 3.547 | 2.811 | 3.171 | 3.087 | 3.547 | ns |
| $t_{COUT}$ | 1.828 | 1.849 | 2.578 | 2.811 | 3.171 | 3.087 | 3.547 | 2.811 | 3.171 | 3.087 | 3.547 | ns |
| $t_{PLLCIN}$ | -0.013 | 0.004 | -0.224 | -0.303 | -0.280 | -0.187 | -0.030 | -0.303 | -0.280 | -0.187 | -0.030 | ns |
| $t_{PLLCOUT}$ | -0.013 | 0.004 | -0.224 | -0.303 | -0.280 | -0.187 | -0.030 | -0.303 | -0.280 | -0.187 | -0.030 | ns |

**Table 1–187.** EP3SE80 Row Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.812 | 1.928 | 2.638 | 2.874 | 3.205 | 3.107 | 3.332 | 2.938 | 3.277 | 3.169 | 3.373 | ns |
| $t_{COUT}$ | 1.730 | 1.837 | 2.496 | 2.711 | 3.024 | 2.936 | 3.173 | 2.768 | 3.088 | 2.990 | 3.214 | ns |
| $t_{PLLCIN}$ | 0.010 | 0.087 | -0.176 | -0.259 | -0.231 | -0.167 | -0.229 | -0.210 | -0.169 | -0.118 | -0.275 | ns |
| $t_{PLLCOUT}$ | -0.072 | -0.004 | -0.318 | -0.422 | -0.412 | -0.338 | -0.388 | -0.380 | -0.358 | -0.297 | -0.434 | ns |

Table 1–188 and Table 1–189 list the periphery clock timing parameters for EP3SE80 devices.

**Table 1–188.** EP3SE80 Column Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.564 | 1.585 | 2.309 | 2.566 | 2.962 | 2.838 | 3.377 | 2.566 | 2.962 | 2.838 | 3.377 | ns |
| $t_{COUT}$ | 1.564 | 1.584 | 2.308 | 2.566 | 2.962 | 2.844 | 3.377 | 2.566 | 2.962 | 2.844 | 3.377 | ns |
| $t_{PLLCIN}$ | -0.028 | -0.006 | -0.234 | -0.327 | -0.270 | -0.193 | -0.018 | -0.327 | -0.270 | -0.193 | -0.018 | ns |
| $t_{PLLCOUT}$ | -0.028 | -0.006 | -0.234 | -0.327 | -0.270 | -0.193 | -0.018 | -0.327 | -0.270 | -0.193 | -0.018 | ns |

**Table 1–189.** EP3SE80 Row Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.441 | 1.503 | 2.156 | 2.429 | 2.776 | 2.665 | 2.934 | 2.477 | 2.828 | 2.711 | 2.959 | ns |
| $t_{COUT}$ | 1.359 | 1.412 | 2.011 | 2.266 | 2.595 | 2.494 | 2.775 | 2.307 | 2.639 | 2.532 | 2.800 | ns |
| $t_{PLLCIN}$ | 0.004 | 0.077 | -0.186 | -0.268 | -0.243 | -0.177 | -0.238 | -0.219 | -0.177 | -0.128 | -0.287 | ns |
| $t_{PLLCOUT}$ | -0.078 | -0.014 | -0.328 | -0.431 | -0.424 | -0.348 | -0.397 | -0.389 | -0.366 | -0.307 | -0.446 | ns |

### EP3SE110 Clock Timing Parameters

Table 1–190 and Table 1–191 list the global clock timing parameters for EP3SE110 devices.

**Table 1–190.** EP3SE110 Column Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 2.046 | 2.046 | 2.868 | 3.144 | 3.524 | 3.429 | 3.989 | 3.144 | 3.524 | 3.429 | 3.989 | ns |
| $t_{COUT}$ | 2.046 | 2.046 | 2.868 | 3.144 | 3.524 | 3.429 | 3.989 | 3.144 | 3.524 | 3.429 | 3.989 | ns |
| $t_{PLLCIN}$ | -0.020 | -0.034 | -0.265 | -0.311 | -0.267 | -0.198 | -0.034 | -0.311 | -0.267 | -0.198 | -0.034 | ns |
| $t_{PLLCOUT}$ | -0.020 | -0.034 | -0.265 | -0.311 | -0.267 | -0.198 | -0.034 | -0.311 | -0.267 | -0.198 | -0.034 | ns |

**Table 1–191.** EP3SE110 Row Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.985 | 2.130 | 2.928 | 3.183 | 3.546 | 3.437 | 3.772 | 3.250 | 3.615 | 3.507 | 3.815 | ns |
| $t_{COUT}$ | 1.903 | 2.039 | 2.786 | 3.020 | 3.365 | 3.266 | 3.613 | 3.082 | 3.426 | 3.328 | 3.656 | ns |
| $t_{PLLCIN}$ | 0.012 | 0.084 | -0.180 | -0.253 | -0.223 | -0.173 | -0.223 | -0.207 | -0.173 | -0.123 | -0.267 | ns |
| $t_{PLLCOUT}$ | -0.070 | -0.007 | -0.322 | -0.416 | -0.404 | -0.344 | -0.382 | -0.377 | -0.362 | -0.302 | -0.426 | ns |

Table 1–192 and Table 1–193 list the regional clock timing parameters for EP3SE110 devices.

**Table 1–192.** EP3SE110 Column Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.828 | 1.849 | 2.578 | 2.811 | 3.155 | 3.082 | 3.560 | 2.811 | 3.155 | 3.082 | 3.560 | ns |
| $t_{COUT}$ | 1.828 | 1.849 | 2.578 | 2.811 | 3.155 | 3.082 | 3.560 | 2.811 | 3.155 | 3.082 | 3.560 | ns |
| $t_{PLLCIN}$ | -0.008 | -0.022 | -0.254 | -0.299 | -0.255 | -0.186 | -0.021 | -0.299 | -0.255 | -0.186 | -0.021 | ns |
| $t_{PLLCOUT}$ | -0.008 | -0.022 | -0.254 | -0.299 | -0.255 | -0.186 | -0.021 | -0.299 | -0.255 | -0.186 | -0.021 | ns |

**Table 1–193.** EP3SE110 Row Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.798 | 1.924 | 2.631 | 2.860 | 3.204 | 3.101 | 3.332 | 2.920 | 3.268 | 3.163 | 3.373 | ns |
| $t_{COUT}$ | 1.716 | 1.833 | 2.489 | 2.697 | 3.023 | 2.930 | 3.173 | 2.750 | 3.079 | 2.984 | 3.214 | ns |
| $t_{PLLCIN}$ | 0.001 | 0.076 | -0.188 | -0.262 | -0.231 | -0.184 | -0.229 | -0.218 | -0.180 | -0.134 | -0.277 | ns |
| $t_{PLLCOUT}$ | -0.081 | -0.015 | -0.330 | -0.425 | -0.412 | -0.355 | -0.388 | -0.388 | -0.369 | -0.313 | -0.436 | ns |

Table 1–194 and Table 1–195 list the periphery clock timing parameters for EP3SE110 devices.

**Table 1–194.** EP3SE110 Column Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.564 | 1.585 | 2.309 | 2.566 | 2.951 | 2.843 | 3.398 | 2.566 | 2.951 | 2.843 | 3.398 | ns |
| $t_{COUT}$ | 1.564 | 1.584 | 2.308 | 2.566 | 2.951 | 2.843 | 3.398 | 2.566 | 2.951 | 2.843 | 3.398 | ns |
| $t_{PLLCIN}$ | -0.019 | -0.019 | -0.245 | -0.310 | -0.267 | -0.194 | -0.018 | -0.310 | -0.267 | -0.194 | -0.018 | ns |
| $t_{PLLCOUT}$ | -0.019 | -0.019 | -0.245 | -0.310 | -0.267 | -0.194 | -0.018 | -0.310 | -0.267 | -0.194 | -0.018 | ns |

**Table 1–195.** EP3SE110 Row Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.423 | 1.502 | 2.156 | 2.411 | 2.781 | 2.659 | 2.934 | 2.455 | 2.826 | 2.704 | 2.949 | ns |
| $t_{COUT}$ | 1.341 | 1.411 | 2.011 | 2.248 | 2.600 | 2.488 | 2.775 | 2.285 | 2.637 | 2.525 | 2.790 | ns |
| $t_{PLLCIN}$ | 0.001 | 0.069 | -0.195 | -0.271 | -0.241 | -0.188 | -0.238 | -0.222 | -0.190 | -0.139 | -0.288 | ns |
| $t_{PLLCOUT}$ | -0.081 | -0.022 | -0.337 | -0.434 | -0.422 | -0.359 | -0.397 | -0.392 | -0.379 | -0.318 | -0.447 | ns |

## EP3SE260 Clock Timing Parameters

Table 1–196 and Table 1–197 list the global clock timing parameters for EP3SE260 devices.

**Table 1–196.** EP3SE260 Column Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 2.237 | 2.237 | 3.302 | 3.416 | 3.837 | 3.683 | 4.331 | 3.416 | 3.837 | 3.683 | 4.331 | ns |
| $t_{COUT}$ | 2.237 | 2.237 | 3.302 | 3.416 | 3.837 | 3.683 | 4.331 | 3.416 | 3.837 | 3.683 | 4.331 | ns |
| $t_{PLLCIN}$ | 0.040 | 0.040 | -0.199 | -0.211 | -0.135 | -0.127 | 0.074 | -0.211 | 0.296 | -0.127 | 0.074 | ns |
| $t_{PLLCOUT}$ | 0.040 | 0.040 | -0.199 | -0.211 | -0.135 | -0.127 | 0.074 | -0.211 | 0.296 | -0.127 | 0.074 | ns |

**Table 1–197.** EP3SE260 Row Pin Global Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 2.171 | 2.374 | 3.458 | 3.526 | 3.868 | 3.768 | 4.184 | 3.564 | 3.943 | 3.768 | 4.184 | ns |
| $t_{COUT}$ | 2.089 | 2.283 | 3.306 | 3.366 | 3.687 | 3.597 | 4.025 | 3.396 | 3.754 | 3.597 | 4.025 | ns |
| $t_{PLLCIN}$ | 0.091 | 0.172 | -0.087 | -0.116 | -0.085 | -0.031 | -0.071 | -0.077 | 0.399 | -0.031 | -0.071 | ns |
| $t_{PLLCOUT}$ | 0.009 | 0.081 | -0.239 | -0.279 | -0.266 | -0.202 | -0.230 | -0.247 | 0.210 | -0.202 | -0.230 | ns |

Table 1–198 and Table 1–199 list the regional clock timing parameters for EP3SE260 devices.

**Table 1–198.** EP3SE260 Column Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.930 | 2.003 | 2.983 | 2.955 | 3.531 | 3.209 | 3.736 | 2.955 | 3.531 | 3.209 | 3.736 | ns |
| $t_{COUT}$ | 1.930 | 2.003 | 2.983 | 2.955 | 3.531 | 3.209 | 3.736 | 2.955 | 3.531 | 3.209 | 3.736 | ns |
| $t_{PLLCIN}$ | 0.061 | 0.066 | -0.172 | -0.191 | -0.109 | -0.091 | 0.102 | -0.191 | 0.302 | -0.091 | 0.102 | ns |
| $t_{PLLCOUT}$ | 0.061 | 0.066 | -0.172 | -0.191 | -0.109 | -0.091 | 0.102 | -0.191 | 0.302 | -0.091 | 0.102 | ns |

**Table 1–199.** EP3SE260 Row Pin Regional Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.903 | 2.065 | 3.000 | 3.070 | 3.388 | 3.294 | 3.593 | 3.103 | 3.457 | 3.294 | 3.593 | ns |
| $t_{COUT}$ | 1.821 | 1.974 | 2.848 | 2.910 | 3.207 | 3.123 | 3.434 | 2.935 | 3.268 | 3.123 | 3.434 | ns |
| $t_{PLLCIN}$ | 0.088 | 0.199 | -0.056 | -0.091 | -0.081 | -0.009 | -0.049 | -0.078 | 0.379 | -0.009 | -0.049 | ns |
| $t_{PLLCOUT}$ | 0.006 | 0.108 | -0.208 | -0.254 | -0.262 | -0.180 | -0.208 | -0.248 | 0.190 | -0.180 | -0.208 | ns |

Table 1–200 and Table 1–201 list the periphery clock timing parameters for EP3SE260 devices.

**Table 1–200.** EP3SE260 Column Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.709 | 1.716 | 2.620 | 2.765 | 3.177 | 3.039 | 3.668 | 2.765 | 3.177 | 3.039 | 3.668 | ns |
| $t_{COUT}$ | 1.709 | 1.716 | 2.620 | 2.765 | 3.177 | 3.039 | 3.668 | 2.765 | 3.177 | 3.039 | 3.668 | ns |
| $t_{PLLCIN}$ | 0.037 | 0.037 | -0.202 | -0.213 | -0.140 | -0.119 | 0.075 | -0.213 | 0.293 | -0.119 | 0.075 | ns |
| $t_{PLLCOUT}$ | 0.037 | 0.037 | -0.202 | -0.213 | -0.140 | -0.119 | 0.075 | -0.213 | 0.293 | -0.119 | 0.075 | ns |

**Table 1–201.** EP3SE260 Row Pin Periphery Clock Timing Specifications

| Parameter | Fast Model | | C2 | C3 | C4 | C4L | | I3 | I4 | I4L | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial | Commercial | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 1.1 V | $V_{CCL}$= 0.9 V | |
| $t_{CIN}$ | 1.495 | 1.574 | 2.378 | 2.518 | 2.878 | 2.776 | 3.072 | 2.555 | 2.926 | 2.776 | 3.072 | ns |
| $t_{COUT}$ | 1.413 | 1.483 | 2.223 | 2.355 | 2.697 | 2.605 | 2.913 | 2.385 | 2.737 | 2.605 | 2.913 | ns |
| $t_{PLLCIN}$ | 0.065 | 0.172 | -0.084 | -0.118 | -0.103 | -0.033 | -0.071 | -0.103 | 0.384 | -0.033 | -0.071 | ns |
| $t_{PLLCOUT}$ | -0.017 | 0.081 | -0.236 | -0.281 | -0.284 | -0.204 | -0.230 | -0.273 | 0.195 | -0.204 | -0.230 | ns |

# Glossary

The following table lists the glossary for this chapter.

*Table 1.*

*Glossary Table (Part 1 of 4)*

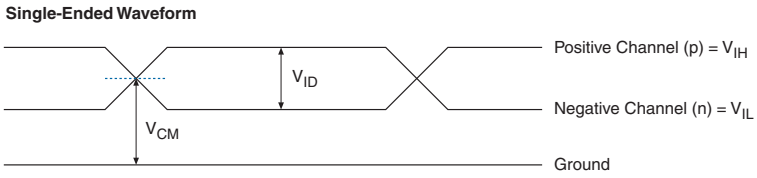
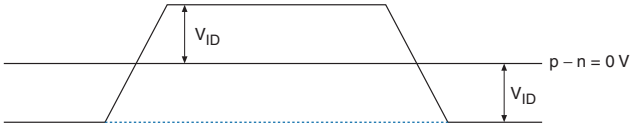
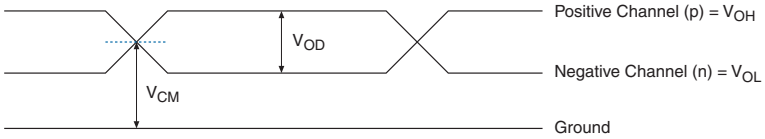
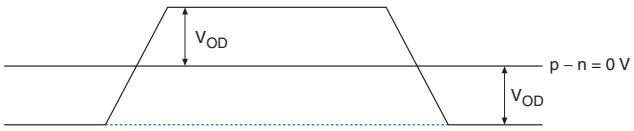
| Letter | Subject | Definitions |
|---|---|---|
| A | — | — |
| B | — | — |
| C | — | — |
| D | Differential I/O Standards | Receiver Input Waveforms<br>**Single-Ended Waveform**<br>  <br><br>**Differential Waveform**<br>  <br><br>Transmitter Output Waveforms<br>**Single-Ended Waveform**<br>  <br><br>**Differential Waveform**<br>  <br> |
| E | — | — |
| F | $f_{HSCLK}$ | High-Speed I/O Block: High-speed receiver/transmitter input and output clock frequency. |
| | $f_{HSDR}$ | High-Speed I/O Block: Maximum/minimum LVDS data transfer rate ($f_{HSDR}$ = 1/TUI), non-DPA. |
| | $f_{HSDRDPA}$ | High-Speed I/O Block: Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA. |
| G | — | — |
| H | — | — |
| I | — | — |

***Table 1.***

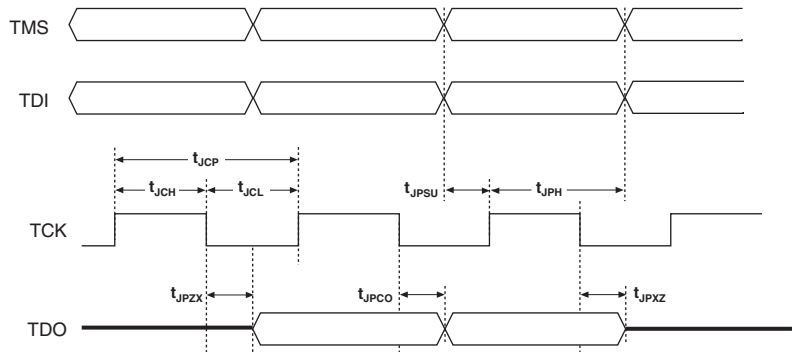
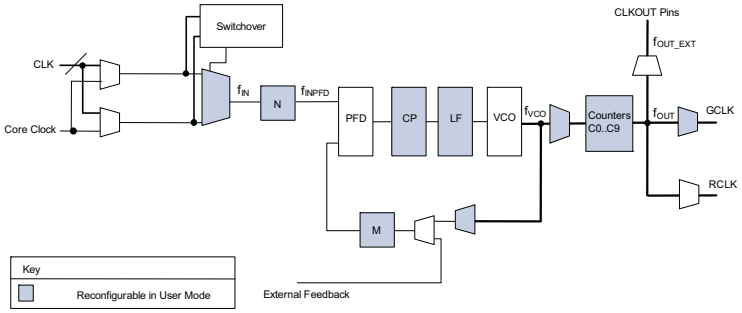
| *Glossary Table (Part 2 of 4)* | | |
|---|---|---|
| **Letter** | **Subject** | **Definitions** |
| **J** | J | High-Speed I/O Block: Deserialization factor (width of parallel data bus). |
| | JTAG Timing Specifications | JTAG Timing Specifications are in the following figure:<br>  |
| **K** | — | — |
| **L** | — | — |
| **M** | — | — |
| **N** | — | — |
| **O** | — | — |
| **P** | PLL Specifications | The block diagram shown in the following figure highlights the PLL Specification parameters:<br>Diagram of PLL Specifications (1)<br>  <br>**Note:**<br>(1) CoreClock can only be fed by dedicated clock input pins or PLL outputs. |
| **Q** | — | — |
| **R** | $R_L$ | Receiver differential input discrete resistor (external to Stratix III device). |

*Table 1.*

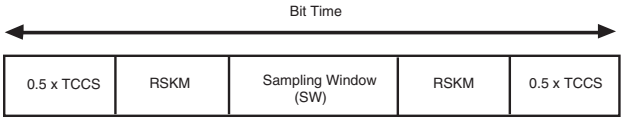
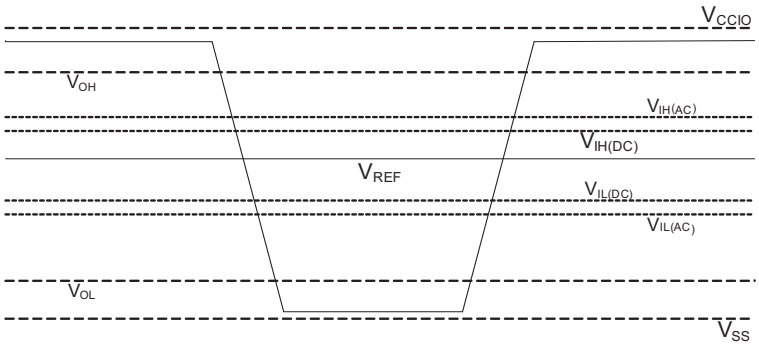
| *Glossary Table (Part 3 of 4)* | | |
|---|---|---|
| **Letter** | **Subject** | **Definitions** |
| **S** | SW (sampling window) | The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window (the following figure):<br>Timing Diagram<br>  |
| | Single-ended Voltage Referenced I/O Standard | The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.<br>The new logic state is maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing (The following figure):<br>Single-Ended Voltage Referenced I/O Standard<br>  |
| **T** | $t_C$ | High-Speed receiver/transmitter input and output clock period. |
| | TCCS (channel-to-channel-skew) | The timing difference between the fastest and slowest output edges, including $t_{co}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **S** in this table) |
| | $t_{DUTY}$ | High-Speed I/O Block: Duty cycle on high-speed transmitter output clock.<br>Timing Unit Interval (TUI)<br>The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = $t_C/w$) |
| | $t_{FALL}$ | Signal high-to-low transition time (80-20%) |
| | $t_{INCCJ}$ | Cycle-to-cycle jitter tolerance on PLL clock input |
| | $t_{OUTPJ_IO}$ | Period jitter on general purpose I/O driven by a PLL |
| | $t_{OUTPJ_DC}$ | Period jitter on dedicated clock output driven by a PLL |
| | $t_{RISE}$ | Signal low-to-high transition time (20-80%) |
| **U** | — | — |

***Table 1.***

| *Glossary Table (Part 4 of 4)* | | |
|---|---|---|
| **Letter** | **Subject** | **Definitions** |
| **V** | $V_{CM(DC)}$ | DC Common Mode Input Voltage. |
| | $V_{ICM}$ | Input Common Mode Voltage: The common mode of the differential signal at the receiver. |
| | $V_{ID}$ | Input Differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | $V_{DIF(AC)}$ | AC Differential Input Voltage: Minimum AC input differential voltage required for switching. |
| | $V_{DIF(DC)}$ | DC Differential Input Voltage: Minimum DC input differential voltage required for switching. |
| | $V_{IH}$ | Voltage Input High: The minimum positive voltage applied to the input that is accepted by the device as a logic high. |
| | $V_{IH(AC)}$ | High-level AC input voltage |
| | $V_{IH(DC)}$ | High-level DC input voltage |
| | $V_{IL}$ | Voltage Input Low: The maximum positive voltage applied to the input that is accepted by the device as a logic low. |
| | $V_{IL(AC)}$ | Low-level AC input voltage |
| | $V_{IL(DC)}$ | Low-level DC input voltage |
| | $V_{OCM}$ | Output Common Mode Voltage: The common mode of the differential signal at the transmitter. |
| | $V_{OD}$ | Output differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. |
| **W** | W | High-Speed I/O Block: Clock Boost Factor |
| **X** | — | — |
| **Y** | — | — |
| **Z** | — | — |

# Chapter Revision History

Table 1–202 lists the revision history for this chapter.

**Table 1–202.** Chapter Revision History (Part 1 of 2)

| Date | Version | Changes Made |
|---|---|---|
| July 2010 | 2.3 | Updated Table 1–11, Table 1–20, Table 1–25, and Table 1–33. |
| March 2010 | 2.2 | Updated for the Quartus II software version 9.1 SP2 release:<br>■ Updated Table 1–7, Table 1–8, Table 1–11, Table 1–19, Table 1–23, Table 1–25, Table 1–28, Table 1–29, and Table 1–33.<br>■ Updated the "Sinusoidal Maximum Allowed Overshoot/Undershoot Voltage" and "External Memory Interface Specifications" sections.<br>■ Minor text edits. |
| July 2009 | 2.1 | Minor text edits. |
| May 2009 | 2.0 | ■ Updated Table 1–1, Table 1–7, Table 1–9, Table 1–18, Table 1–21, Table 1–22, Table 1–23, Table 1–25, Table 1–26, Table 1–28, Table 1–29, Table 1–30, Table 1–33, Table 1–35, Table 1–41, Table 1–43, Table 1–51, Table 1–53, Table 1–61, Table 1–63, Table 1–71, Table 1–73, Table 1–81, Table 1–83, Table 1–91, Table 1–93, Table 1–101, Table 1–103, Table 1–111, Table 1–113, Table 1–121, Table 1–123, Table 1–131, and Table 1–133.<br>■ Updated Equation 1–1. |
| February 2009 | 1.9 | ■ Updated "Programmable IOE Delay", "PLL Specifications", "DSP Block Specifications", "TriMatrix Memory Block Specifications", "External Memory Interface Specifications", and "High-Speed I/O Specifications" sections.<br>■ Updated all Timing Information Tables in "User I/O Pin Timing" and "Dedicated Clock Pin Timing" sections.<br>■ Removed "Referenced Documents" and "Maximum Input and Output Toggle Rate" sections. |
| October 2008 | 1.8 | ■ Updated "Operating Conditions".<br>■ Added "Bus Hold Specifications".<br>■ Updated Table 1–3, Table 1–6, Table 1–7, Table 1–11, and Table 1–14.<br>■ Updated Table 1–17 to Table 1–25.<br>■ Updated Table 1–39 to Table 1–47.<br>■ Updated Table 1–50 to Table 1–210.<br>■ Added (Note 3) to Table 1–11.<br>■ Added (Note 1) to Table 1–14.<br>■ Added (Note 6) to Table 1–17.<br>■ Added (Note 1) to Table 1–47.<br>■ Added Table 1–26.<br>■ Added Figure 1–2. |

**Table 1–202.** Chapter Revision History (Part 2 of 2)

| Date | Version | Changes Made |
|---|---|---|
| July 2008 | 1.7 | ■ Updated "Operating Conditions" introduction section.<br>■ Updated Table 1–3, Table 1–7, Table 1–8, Table 1–19, Table 1–21, Table 1–22, Table 1–25, Table 1–26,Table 1–28, Table 1–29, Table 1–30, Table 1–31, Table 1–32, Table 1–33, Table 1–35, and Table 1–48.<br>■ Updated "PLL Specifications" introduction section.<br>■ Updated "I/O Timing Measurement Methodology" section.<br>■ Updated Figure 1–5, Figure 1–6, and Figure 1–7. |
| May 2008 | 1.6 | ■ Updated all tables for timing section.<br>■ Added "Internal Weak Pull-Up Resistor" section.<br>■ Removed "Stratix III Temperature Sensing Diode Specifications" section.<br>■ Added Figure 1–6 and Figure 1–7.<br>■ Added derating factors Table 1–45 and Table 1–46. |
| November 2007 | 1.5 | ■ Updated Table 1–90 to Table 1–109.<br>■ Updated Table 1–140 to Table 1–149.<br>■ Updated Table 1–175 to Table 1–180.<br>■ Updated Table 1–181 to Table 1–186.<br>■ Updated Table 1–205 to Table 1–210. |
| October 2007 | 1.4 | ■ Updated I/O Timing<br>■ Added new device packages for EP3SL50, EP3SL110, EP3SE80. |
| May 2007 | 1.3 | Added new contact information table to the About this Handbook section. |
| May 2007 | 1.2 | Updated Table 1–44 through Table 1–205. |
| March 2007 | 1.1 | Added I/O Timing section. |
| November 2006 | 1.0 | Initial Release. |