



CD4081B

Preliminary

CMOS IC

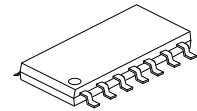
QUAD 2-INPUT AND BUFFERED B SERIES GATE

■ DESCRIPTION

The **UTC CD4081B** contains four independent 2-input AND gates, they perform the function $Y=A \bullet B$ in positive logic.

■ FEATURES

- * 5V-10V-15V Parametric Ratings
- * Quad 2-Input AND Gate
- * Symmetrical Output Characteristics
- * Maximum Input Current of 1uA at 15V Over Full Package Temperature Range
- * Low Power TTL:
Fan Out of 2 Driving 74L or 1 Driving 74LS Compatibility



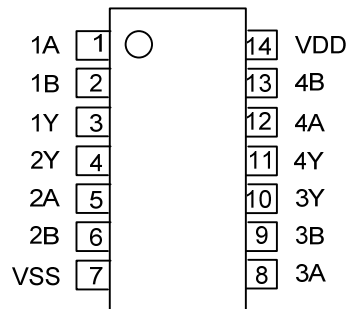
SOP-14

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
CD4081BL-S14-R	CD4081BG-S14-R	SOP-14	Tape Reel

CD4081BL-S14-R	(1) Packing Type (2) Package Type (3) Lead Free	(1) R: Tape Reel (2) S14: SOP-14 (3) G: Halogen Free, L: Lead Free
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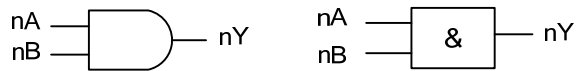
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT(A)	INPUT(B)	OUTPUT(Y)
H	H	H
H	L	L
L	H	L
L	L	L

■ LOGIC DIAGRAM (positive logic)



■ **ABSOLUTE MAXIMUM RATING**($T_a=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.5 ~ 18	V
Input Voltage	$V(nA,nB)$	-0.5 ~ $V_{DD} + 0.5$	V
Storage Temperature	T_{STG}	-65 ~ + 150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	3 ~ 15	V
Operating Temperature	T_{OPR}	-40 ~ +125	$^{\circ}\text{C}$

■ **ELECTRICAL CHARACTERISTICS**($T_a=25^{\circ}\text{C}$)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	High	V _{IH}	V _{DD} = 5.0V, V _O =0.5V	3.5	3		V
			V _{DD} = 10V, V _O =1.0V	7.0	6		
			V _{DD} = 15V, V _O =1.5V	11.0	9		
	Low	V _{IL}	V _{DD} = 5.0V, V _O =4.5V		2	1.5	V
			V _{DD} = 10V, V _O =9.0V		4	3.0	
			V _{DD} = 15V, V _O =13.5V		6	4.0	
Output Voltage	High	V _{OH}	V _{DD} = 5.0V, I _{OH} =1μA	4.95	5		V
			V _{DD} = 10V, I _{OH} =1μA	9.95	10		
			V _{DD} = 15V, I _{OH} =1μA	14.95	15		
	Low	V _{OL}	V _{DD} = 5.0V, I _{OL} =1μA		0	0.05	V
			V _{DD} = 10V, I _{OL} =1μA		0	0.05	
			V _{DD} = 15V, I _{OL} =1μA		0	0.05	
Output Current (Note 1)	High	I _{OH}	V _{DD} = 5.0V, V _O =4.6V	0.51	0.88		mA
			V _{DD} = 10V, V _O =9.5V	1.3	2.25		
			V _{DD} = 15V, V _O =13.5V	3.4	8.8		
	Low	I _{OL}	V _{DD} = 5.0V, V _O =0.4V	0.51	0.88		
			V _{DD} = 10V, V _O =0.5V	1.3	2.25		
			V _{DD} = 15V, V _O =1.5V	3.4	8.8		
Input Leakage Current		I _{I(LEAK)}	V _{DD} = 15V, V _{IN} = V _{DD} or GND			0.1	μA
Quiescent Supply Current		I _Q	V _{DD} = 5.0V, V _{IN} = V _{DD} or V _{SS} , I _{OUT} = 0		0.004	0.25	μA
			V _{DD} = 10V, V _{IN} = V _{DD} or V _{SS} , I _{OUT} = 0		0.005	0.5	
			V _{DD} = 15V, V _{IN} = V _{DD} or V _{SS} , I _{OUT} = 0		0.006	1.0	

Note: 1. I_{OL} and I_{OH} are tested one output at a time

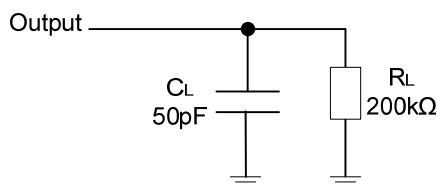
■ **SWITCHING CHARACTERISTICS**($T_A=25^{\circ}\text{C}$, Input: $t_R=t_F=20\text{ns}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from Input(A or B) to Output(Y)	t_{PLH}	$V_{DD}=5.0\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		120	250	ns
		$V_{DD}=10\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		50	100	
		$V_{DD}=15\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		35	70	
	t_{PHL}	$V_{DD}=5.0\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		100	250	
		$V_{DD}=10\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		40	100	
		$V_{DD}=15\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		30	70	
Transition Time	t_{TLH}	$V_{DD}=5.0\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		90	200	ns
	t_{THL}	$V_{DD}=10\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		50	100	
		$V_{DD}=15\text{V}$, $C_L=50\text{pF}$, $R_L=200\text{k}\Omega$		40	80	

■ **OPERATING CHARACTERISTICS**($T_a=25^{\circ}\text{C}$)

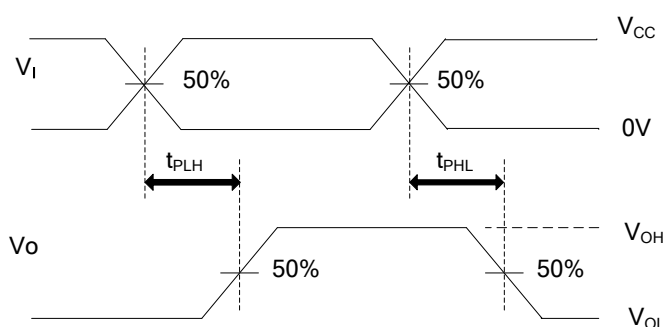
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average Input Capacitance	C_{IN}	Any Input		5	7.5	pF
Power Dissipation Capacitance	C_{PD}	Any Gate		18		

■ TEST CIRCUIT AND WAVEFORMS



Definitions for test circuit

Note: C_L includes probe and jig capacitance.



Propagation Delay Times

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