SLLS095D – SEPTEMBER 1973 – REVISED OCTOBER 1998

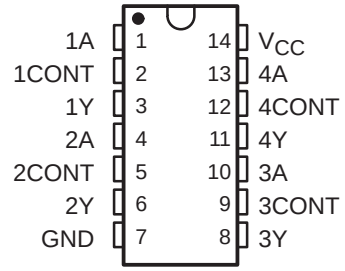
- **Input Resistance . . . 3 kΩ to 7 kΩ**
- **Input Signal Range . . . ±30 V**
- **Operate From Single 5-V Supply**
- **Built-In Input Hysteresis (Double Thresholds)**
- **Response Control that Provides:**
  - **Input Threshold Shifting**
  - **Input Noise Filtering**
- **Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V.28**
- **Fully Interchangeable With Motorola™ MC1489 and MC1489A**

description

These devices are monolithic low-power Schottky quadruple line receivers designed to satisfy the requirements of the standard interface between data-terminal equipment and data-communication equipment as defined by TIA/EIA-232-F. A separate response-control (CONT) terminal is provided for each receiver. A resistor or a resistor and bias-voltage source can be connected between this terminal and ground to shift the input threshold levels. An external capacitor can be connected between this terminal and ground to provide input noise filtering.

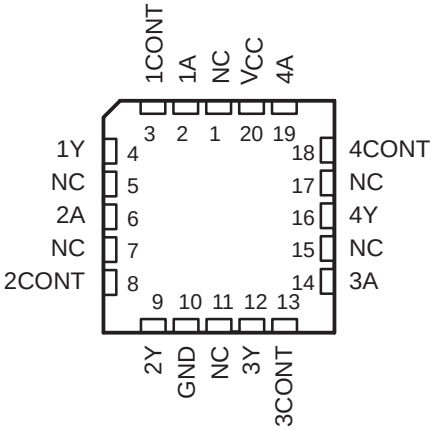
The SN55189 and SN55189A are characterized for operation over the full military temperature range of −55°C to 125°C. The MC1489, MC1489A, SN75189, and SN75189A are characterized for operation from 0°C to 70°C.

SN55189, SN55189A . . . J OR W PACKAGE
MC1489, MC1489A, SN75189, SN75189A
D, N, OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available left-end taped and reeled. For SN75189, order SN75189NSR.

SN55189, SN55189A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

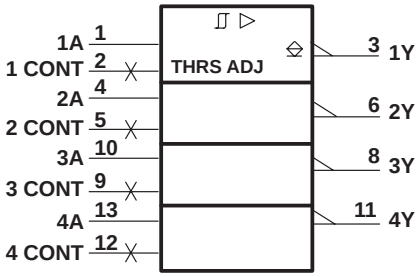
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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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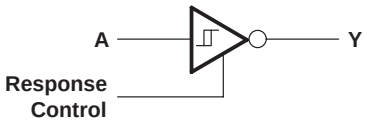
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

logic symbol†

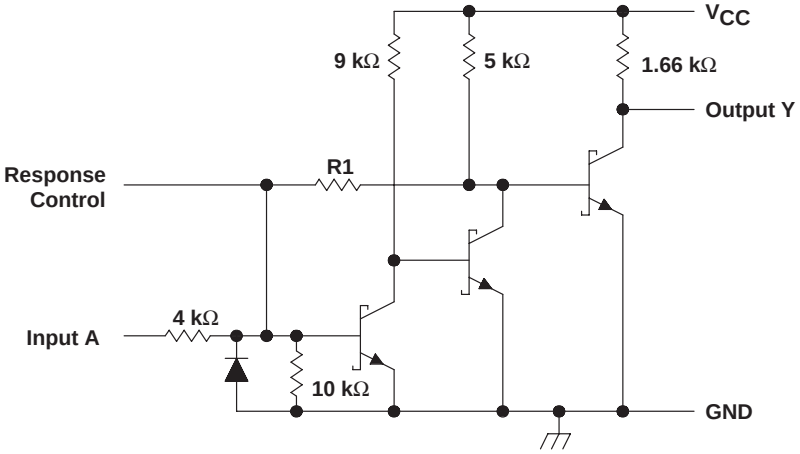


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, NS, and W packages.

logic diagram (positive logic)



schematic (each receiver)



	MC1489 SN55189 SN75189	MC1489A SN55189A SN75189A
R1	8.4 kΩ	1.84 kΩ

Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 10 V
Input voltage, V_I . . . . . ±30 V
Output voltage, I_O . . . . . 20 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55189, SN55189A . . . . . –55°C to 125°C
MC1489, MC1489A, SN75189, SN75189A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 60 seconds, FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or NS package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	N/A
NS	625 mW	4.0 mW/°C	445 mW	N/A
W	1000 mW	8.0 mW/°C	640 mW	200 mW

‡ In the J package, SN55189 and SN55189A chips are either silver glass or alloy mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Input voltage, V_I	–25		25	V
High-level output current, I_{OH}			–0.5	mA
Low-level output current, I_{OL}			10	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range, V_{CC} = 5 V ± 1% (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN55189 SN55189A			MC1489, MC1489A SN75189 SN75189A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IT+}	Positive-going input threshold voltage	1	'89	T_A = 25°C	1	1.3	1.5	1	1.3	1.5	V
				T_A = 0°C to 70°C				0.9		1.6	
				T_A = –55°C to 125°C	0.6		1.9				
			'89A	T_A = 25°C	1.75	1.9	2.25	1.75	1.9	2.25	
				T_A = 0°C to 70°C				1.55		2.25	
				T_A = –55°C to 125°C	1.30		2.65				
$V_{IT–}$	Negative-going input threshold voltage	1	'89, '89A	T_A = 25°C	0.75	1.0	1.25	0.75	1.0	1.25	V
				T_A = 0°C to 70°C				0.65		1.25	
				T_A = –55°C to 125°C	0.35		1.6				
V_{OH}	High-level output voltage	1	V_I = 0.75 V,	I_{OH} = –0.5 mA	2.6	4	5	2.6	4	5	V
			Input open,	I_{OH} = –0.5 mA	2.6	4	5	2.6	4	5	
V_{OL}	Low-level output voltage	1	V_I = 3 V,	I_{OL} = 10 mA		0.2	0.45		0.2	0.45	V
I_{IH}	High-level input current	2	V_I = 25 V		3.6		8.3	3.6		8.3	mA
			V_I = 3 V		0.43			0.43			
I_{IL}	Low-level input current	2	V_I = –25 V		–3.6		–8.3	–3.6		–8.3	mA
			V_I = –3 V		–0.43			–0.43			
I_{OS}	Short-circuit output current	3				–3			–3		mA
I_{CC}	Supply current	2	V_I = 5 V,	Outputs open		20	26		20	26	mA

† All characteristics are measured with the response-control terminal open.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	4	R_L = 3.9 kΩ		25	85	ns
t_{PHL}	Propagation delay time, high- to low-level output		R_L = 390 Ω		25	50	
t_{TLH}	Transition time, low- to high-level output		R_L = 3.9 kΩ		120	175	ns
t_{THL}	Transition time, high- to low-level output		R_L = 390 Ω		10	20	

PARAMETER MEASUREMENT INFORMATION†

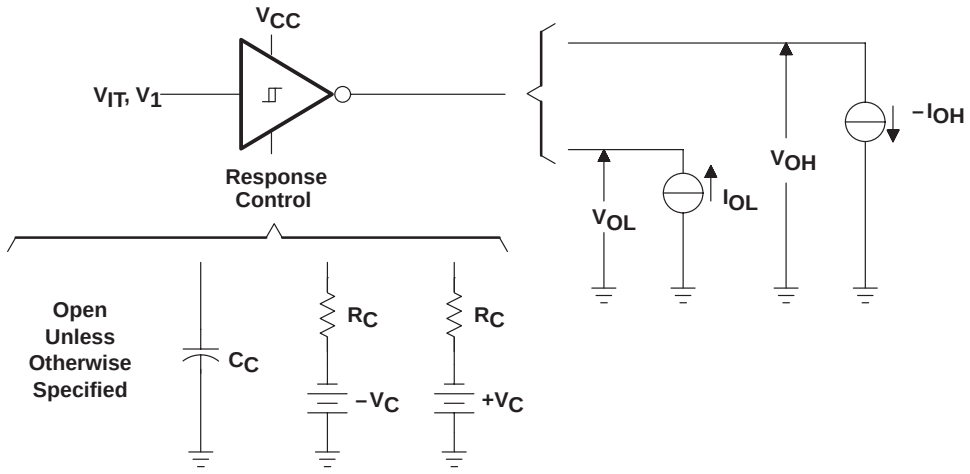
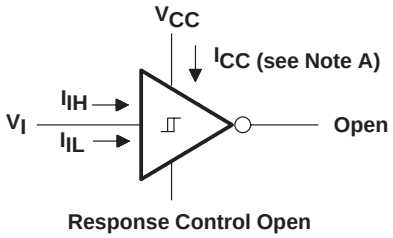


Figure 1. V_{IT+} , V_{IT-} , V_{OH} , V_{OL}



NOTE A: I_{CC} is tested for all four receivers simultaneously.

Figure 2. I_{IH} , I_{IL} , I_{CC}

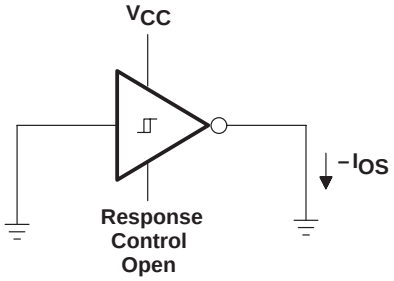
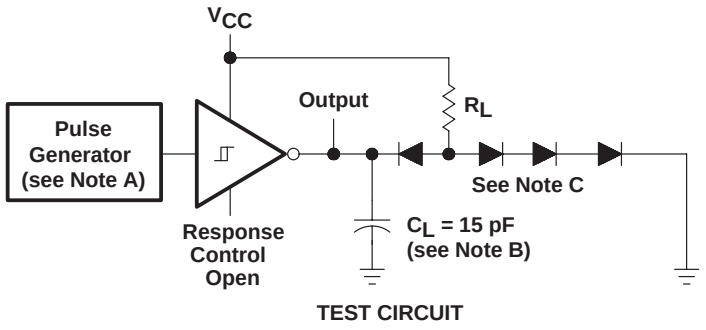


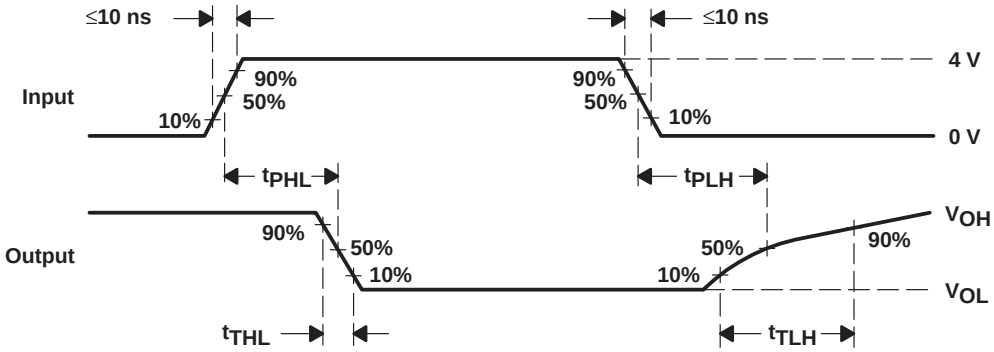
Figure 3. I_{OS}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_W = 500 ns.
B. C_L includes probe and jig capacitances.
C. All diodes are 1N3064 or equivalent.

Figure 4. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

**SN65189, SN75189
OUTPUT VOLTAGE
vs
INPUT VOLTAGE**

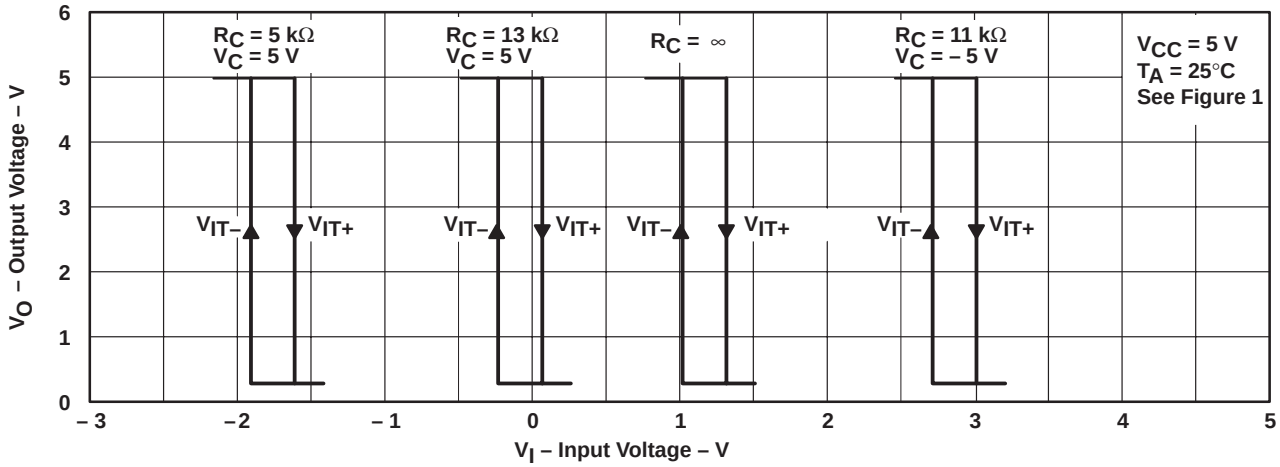


Figure 5

**SN65189A, SN75189A
OUTPUT VOLTAGE
vs
INPUT VOLTAGE**

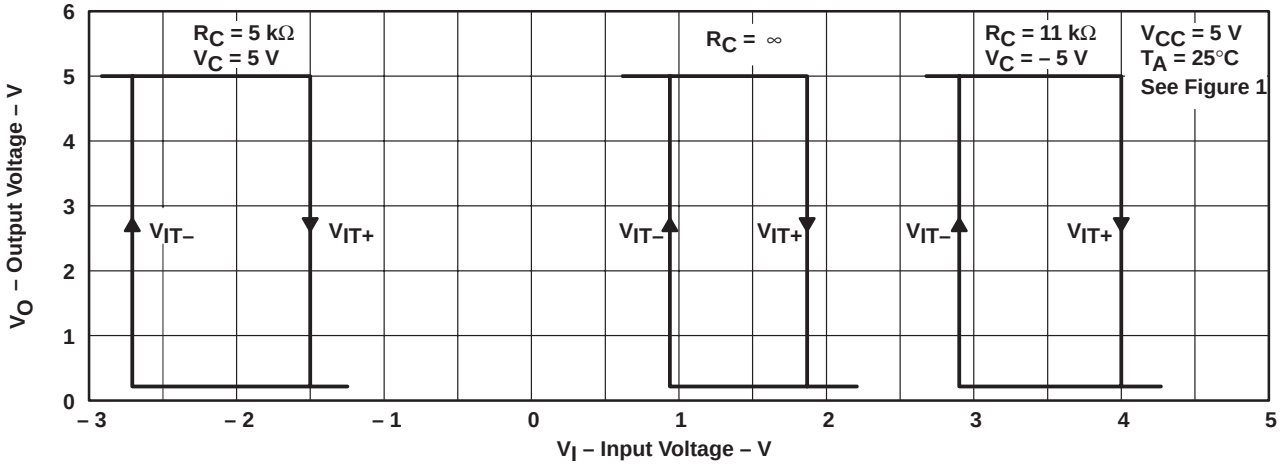


Figure 6

TYPICAL CHARACTERISTICS†

INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

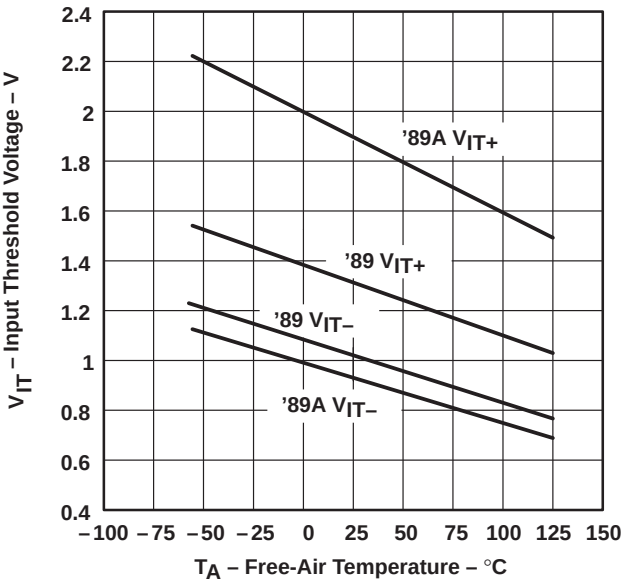


Figure 7

INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

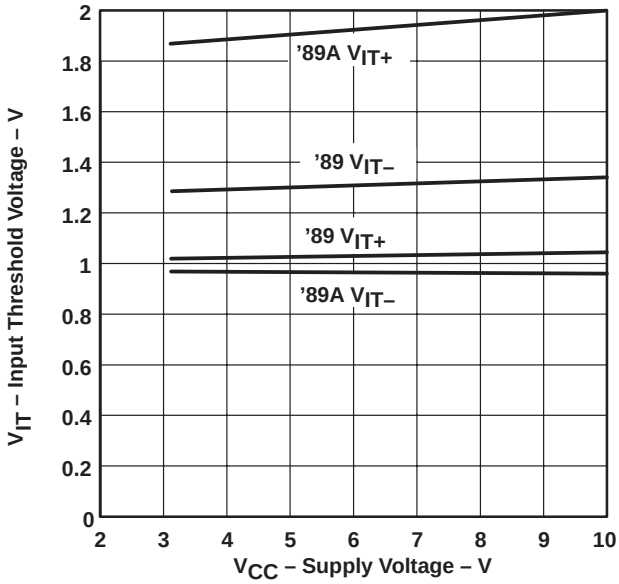
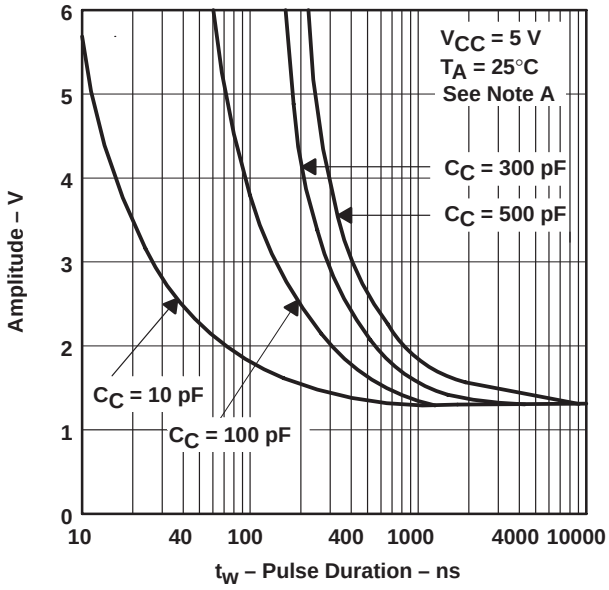


Figure 8

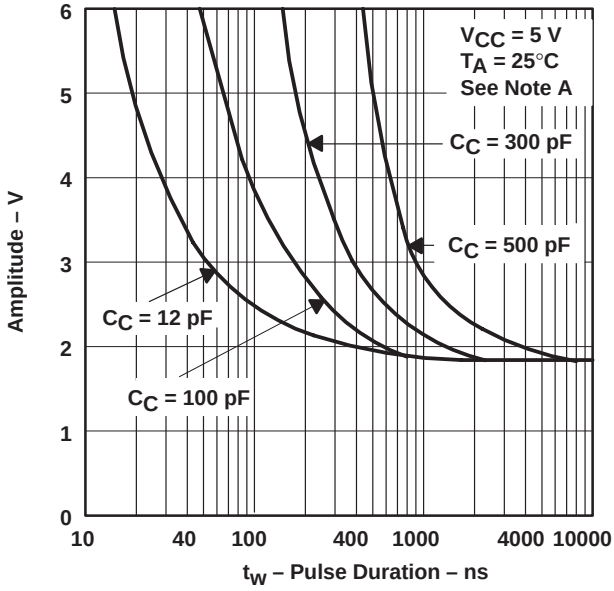
SN75189 NOISE REJECTION



NOTE A: Maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

Figure 9

SN75189A NOISE REJECTION



NOTE A: Maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

Figure 10

† Data for free-air temperatures below 0°C and above 70°C are applicable to SN55189 and SN55189A circuits only.

TYPICAL CHARACTERISTICS

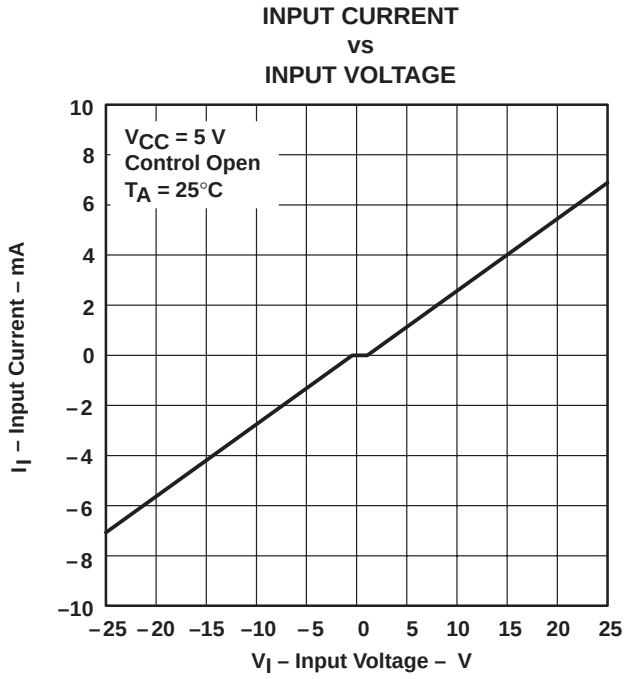


Figure 11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-86888022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-8688802CA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
5962-8688802DA	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	Level-NC-NC-NC
MC1489AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
MC1489ANE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
MC1489N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN55189AJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
SN55189J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN75189AD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75189ADE4	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75189ADR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75189ADRE4	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75189AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75189ANSLE	OBSOLETE	SO	NS	14		TBD	Call TI	Call TI
SN75189ANSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75189ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75189D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75189DE4	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75189DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75189DRE4	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75189N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75189NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75189NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75189NSRE4	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ55189AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
SNJ55189AJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
SNJ55189AW	ACTIVE	CFP	W	14	1	TBD	A42 SNPB	Level-NC-NC-NC
SNJ55189FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ55189J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

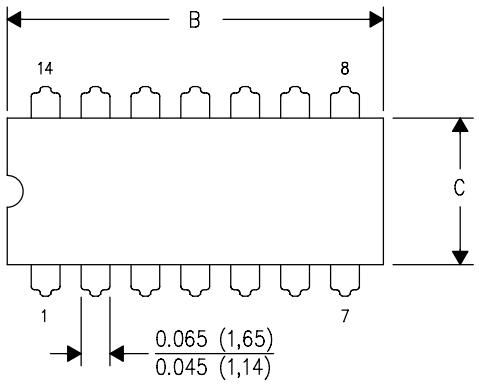
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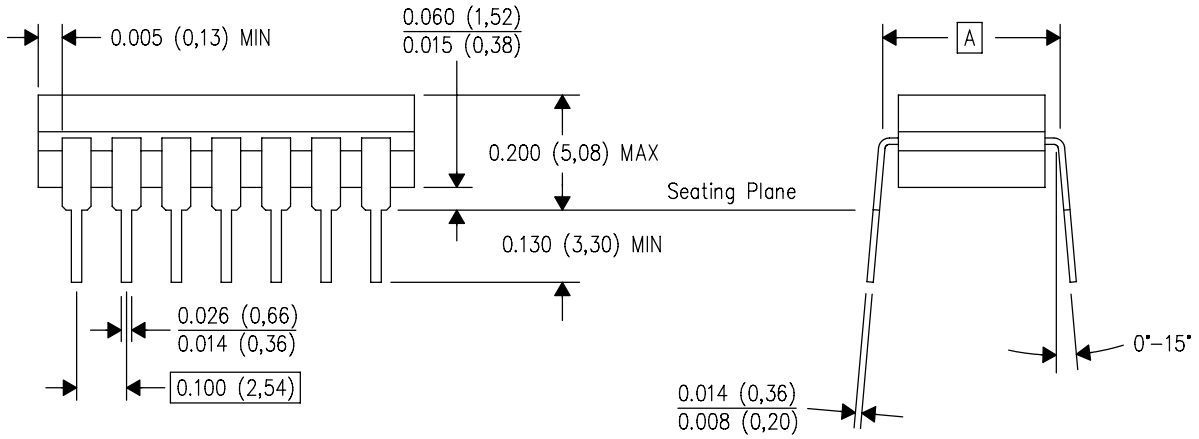
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



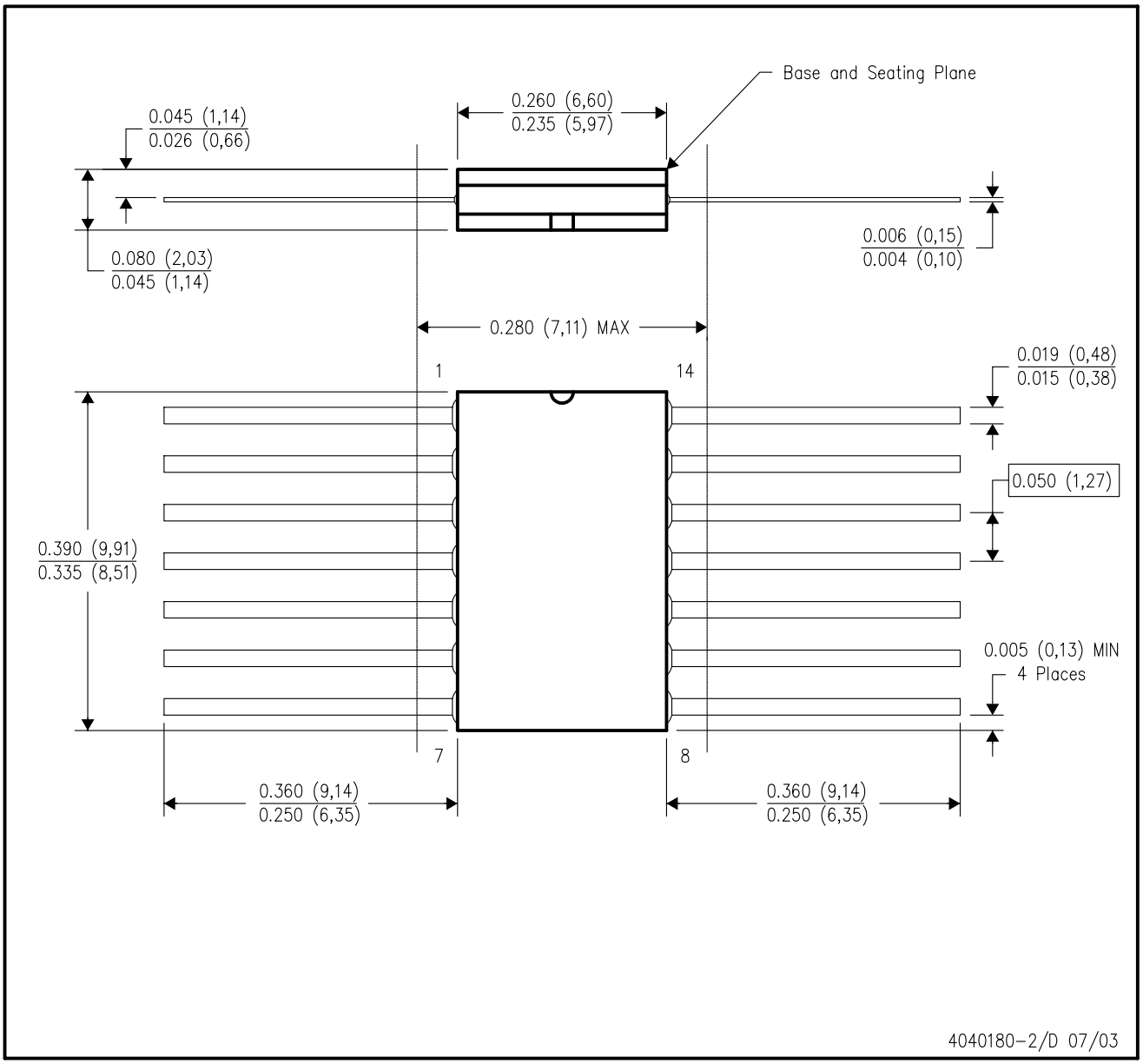
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

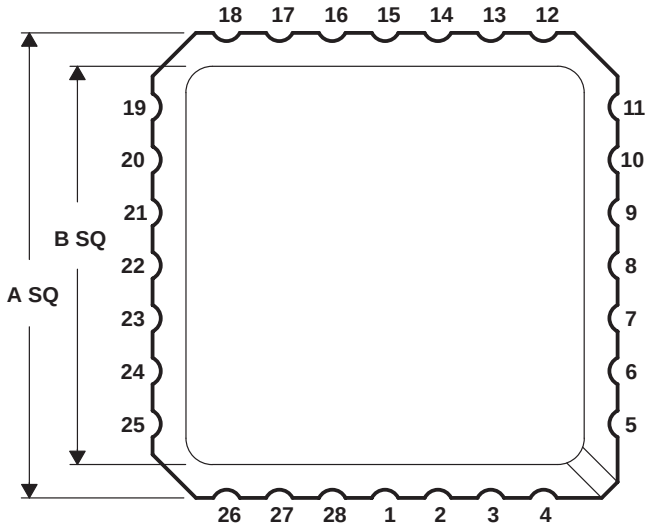
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



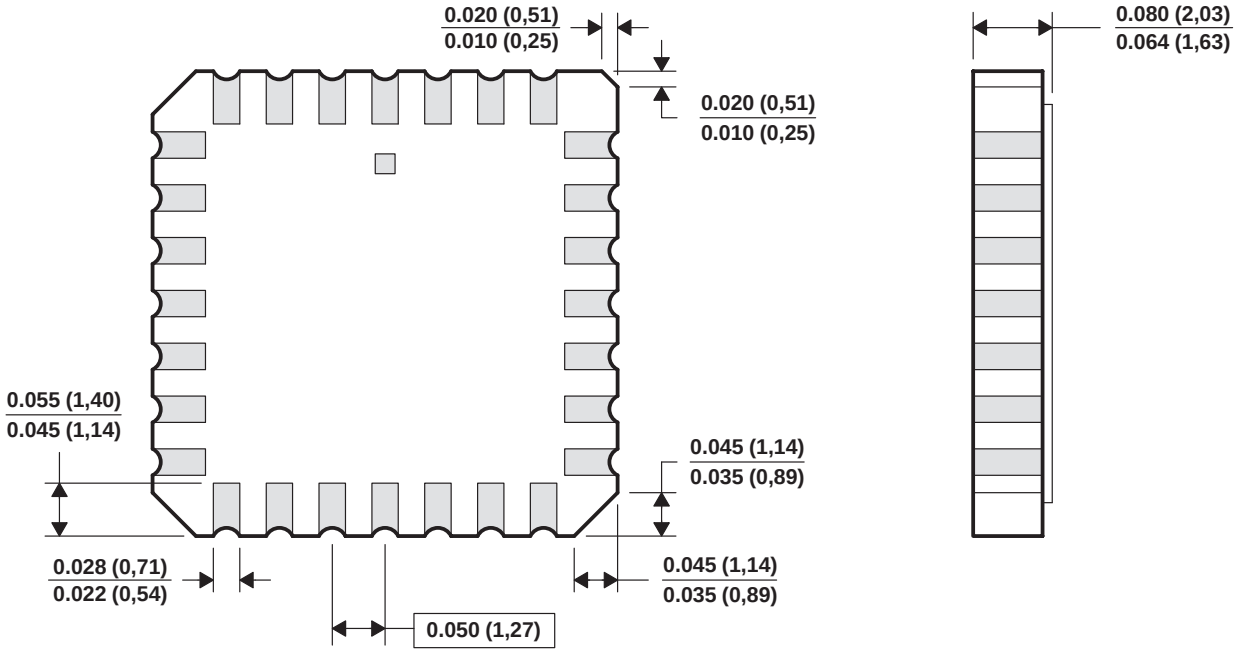
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



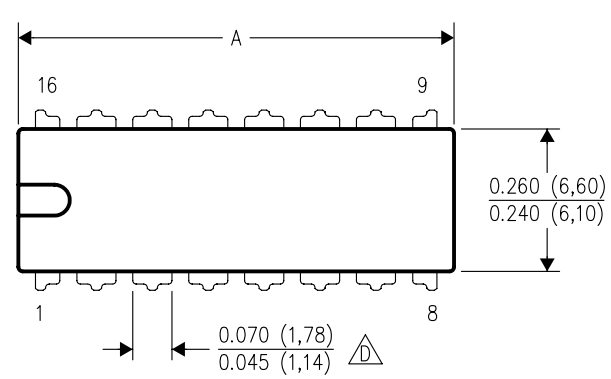
4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

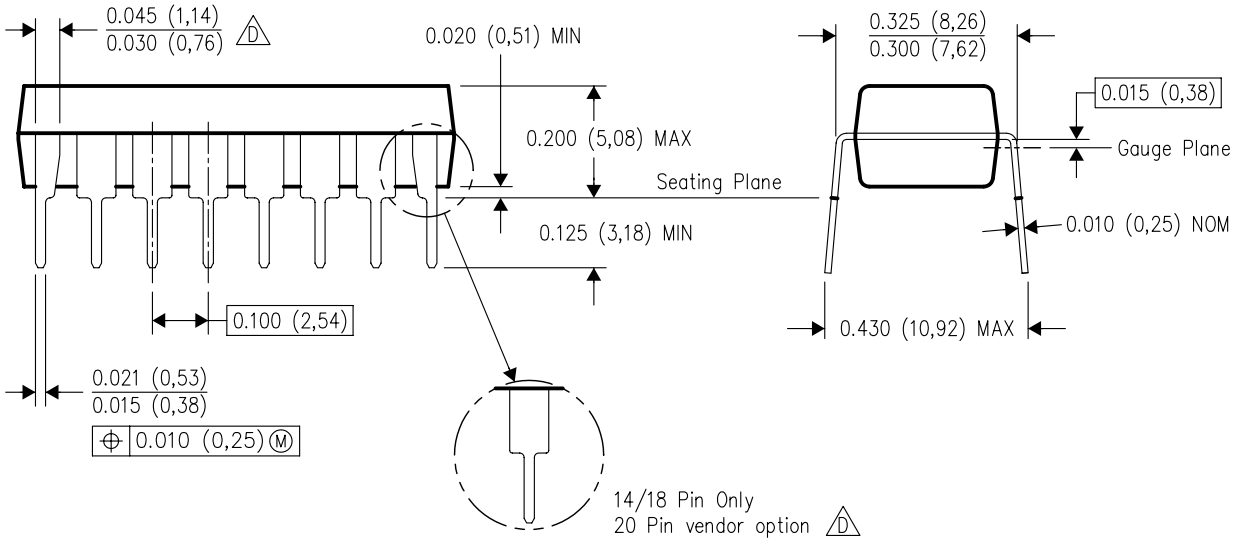
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



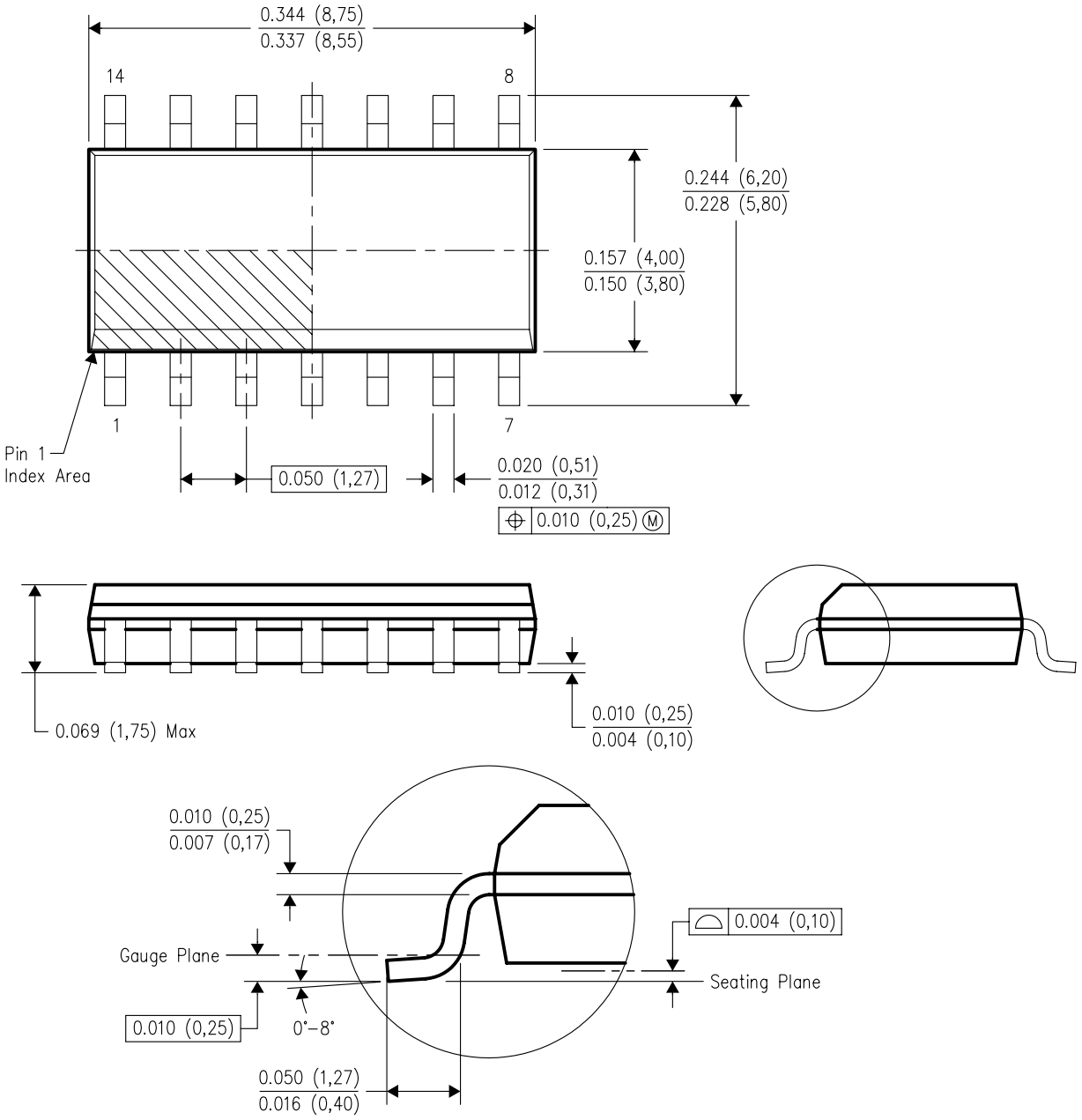
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE

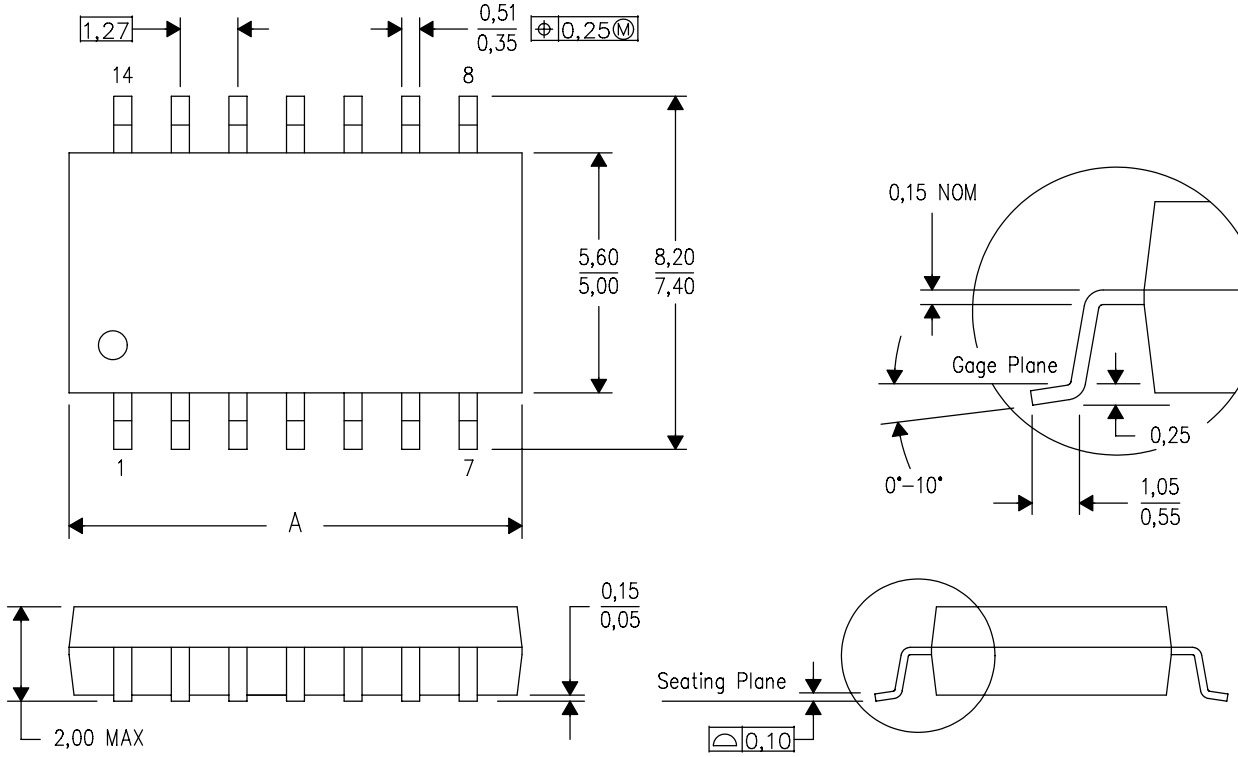


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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