19-2263; Rev 0; 12/01

MAXIM

Dual 10-Bit, 40Msps, 3V, Low-Power ADC with Internal Reference and Multiplexed Parallel Outputs

General Description

The MAX1186 is a 3V, dual 10-bit analog-to-digital converter (ADC) featuring fully-differential wideband track-and-hold (T/H) inputs, driving two pipelined, nine-stage ADCs. The MAX1186 is optimized for low-power, high dynamic performance applications in imaging, instrumentation, and digital communication applications. This ADC operates from a single 2.7V to 3.6V supply, consuming only 105mW while delivering a typical signal-to-noise ratio (SNR) of 59.4dB at an input frequency of 20MHz and a sampling rate of 40Msps. Digital outputs A and B are updated alternating on the rising (CHA) and the falling (CHB) edge of the clock. The T/H driven input stages incorporate 400MHz (-3dB) input amplifiers. The converters may also be operated with single-ended inputs. In addition to low operating power, the MAX1186 features a 2.8mA sleep mode as well as a 1µA power-down mode to conserve power during idle periods.

An internal 2.048V precision bandgap reference sets the full-scale range of the ADCs. A flexible reference structure allows the use of this internal or an externally derived reference, if desired for applications requiring increased accuracy or a different input voltage range.

The MAX1186 features parallel, multiplexed, CMOS-compatible three-state outputs. The digital output format can be set to two's complement or straight offset binary through a single control pin. The device provides for a separate output power supply of 1.7V to 3.6V for flexible interfacing. The MAX1186 is available in a 7mm x 7mm, 48-pin TQFP-EP package, and is specified for the extended industrial (-40°C to +85°C) temperature range.

Pin-compatible, nonmultiplexed, high-speed versions of the MAX1186 are also available. Please refer to the MAX1180 data sheet for 105Msps, the MAX1181 data sheet for 80Msps, the MAX1182 data sheet for 65Msps, the MAX1183 data sheet for 40Msps, and the MAX1184 data sheet for 20Msps. For a pin-compatible lower speed version (20Msps) of the MAX1186, please refer to the MAX1185 data sheet.

Applications

High-Resolution Imaging

I/Q Channel Digitization

Multichannel IF Sampling

Instrumentation

Video Application

Ultrasound

Features

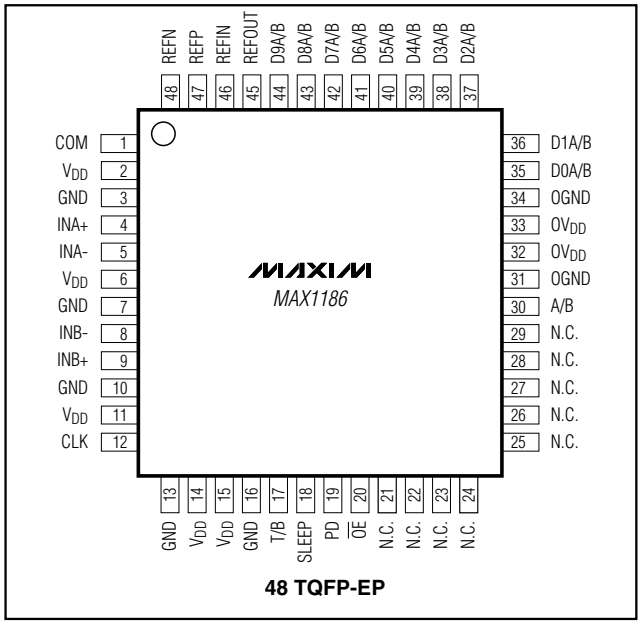
- **Single 3V Operation**
- **Excellent Dynamic Performance:**
  59.4dB SNR at f_{IN} = 20MHz
  72dBc SFDR at f_{IN} = 20MHz
- **Low Power:**
  35mA (Normal Operation)
  2.8mA (Sleep Mode)
  1µA (Shutdown Mode)
- **0.02dB Gain and 0.25° Phase Matching**
- **Wide ±1V_{P-P} Differential Analog Input Voltage Range**
- **400MHz, -3dB Input Bandwidth**
- **On-Chip 2.048V Precision Bandgap Reference**
- **Single 10-Bit Bus for Multiplexed, Digital Outputs**
- **User-Selectable Output Format–Two's Complement or Offset Binary**
- **48-Pin TQFP Package with Exposed Paddle For Improved Thermal Dissipation**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1186ECM	-40°C to +85°C	48 TQFP-EP

Functional Diagram appears at end of data sheet.

Pin Configuration



48 TQFP-EP

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Dual 10-Bit, 40Msps, 3V, Low-Power ADC with Internal Reference and Multiplexed Parallel Outputs

ABSOLUTE MAXIMUM RATINGS

V_{DD}, OV_{DD} to GND .....-0.3V to +3.6V
OGND to GND.....-0.3V to +0.3V
INA+, INA-, INB+, INB- to GND .....-0.3V to V_{DD}
REFIN, REFOUT, REFP, REFN, COM, CLK to GND.....-0.3V to (V_{DD} + 0.3V)
$\overline{OE}$, PD, SLEEP, T/B, D9A/B–D0A/B, A/B to OGND .....-0.3V to (OV_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP (derate 12.5mW/°C above +70°C).....1000mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3V, OV_{DD} = 2.5V, 0.1µF and 1µF capacitors from REFP, REFN, and COM to GND; REFOUT connected to REFIN through a 10kΩ resistor, V_{IN} = $2V_{P-P}$ (differential w.r.t. COM), C_L = 10pF at digital outputs (Note 5), f_{CLK} = 40MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			10			Bits
Integral Nonlinearity	INL	f_{IN} = 7.5MHz		±0.5	±1.7	LSB
Differential Nonlinearity	DNL	f_{IN} = 7.5MHz, no missing codes guaranteed		±0.25	±1.0	LSB
Offset Error				< ±1	±1.7	% FS
Gain Error				0	±2	% FS
ANALOG INPUT						
Differential Input Voltage Range	V_{DIFF}	Differential or single-ended inputs		±1		V
Common-Mode Input Voltage Range	V_{CM}			V_{DD}/2 ± 0.5		V
Input Resistance	R_{IN}	Switched capacitor load		100		kΩ
Input Capacitance	C_{IN}			5		pF
CONVERSION RATE						
Maximum Clock Frequency	f_{CLK}		40			MHz
Data Latency		CHA		5		Clock Cycles
		CHB		5.5		
DYNAMIC CHARACTERISTICS (f_{CLK} = 40MHz, 4096-point FFT)						
Signal-to-Noise Ratio	SNR	$f_{INA\ or\ B}$ = 7.5MHz, T_A = +25°C	57.3	59.5		dB
		$f_{INA\ or\ B}$ = 20MHz, T_A = +25°C	56.8	59.4		
Signal-to-Noise and Distortion	SINAD	$f_{INA\ or\ B}$ = 7.5MHz, T_A = +25°C	57	59.4		dB
		$f_{INA\ or\ B}$ = 20MHz, T_A = +25°C	56.5	59.2		
Spurious-Free Dynamic Range	SFDR	$f_{INA\ or\ B}$ = 7.5MHz, T_A = +25°C	64	74		dBc
		$f_{INA\ or\ B}$ = 20MHz, T_A = +25°C	64	72		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 2.5V, 0.1µF and 1µF capacitors from REFP, REFN, and COM to GND; REFOUT connected to REFIN through a 10kΩ resistor, V_{IN} = $2V_{P-P}$ (differential w.r.t. COM), C_L = 10pF at digital outputs (Note 5), f_{CLK} = 40MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Third-Harmonic Distortion	HD3	$f_{INA\ or\ B}$ = 7.5MHz		-74		dBc
		$f_{INA\ or\ B}$ = 20MHz		-72		
Intermodulation Distortion	IMD	$f_{INA\ or\ B}$ = 11.6066MHz at -6.5dB FS $f_{INA\ or\ B}$ = 13.3839MHz at -6.5dB FS (Note 2)		-76		dBc
Total Harmonic Distortion (first four harmonics)	THD	$f_{INA\ or\ B}$ = 7.5MHz, T_A = +25°C		-72	-64	dBc
		$f_{INA\ or\ B}$ = 20MHz		-71	-63	
Small-Signal Bandwidth		Input at -20dB FS, differential inputs		500		MHz
Full-Power Bandwidth	FPBW	Input at -0.5dB FS, differential inputs		400		MHz
Aperture Delay	t_{AD}			1		ns
Aperture Jitter	t_{AJ}			2		ps_{rms}
Overdrive Recovery Time		For 1.5 × full-scale input		2		ns
Differential Gain				±1		%
Differential Phase				±0.25		degrees
Output Noise		INA+ = INA- = INB+ = INB- = COM		0.2		LSB_{RMS}
INTERNAL REFERENCE						
Reference Output Voltage	REFOUT			2.048 ±3%		V
Reference Temperature Coefficient	TC_{REF}			60		ppm/°C
Load Regulation				1.25		mV/mA
BUFFERED EXTERNAL REFERENCE (V_{REFIN} = 2.048V)						
REFIN Input Voltage	V_{REFIN}			2.048		V
Positive Reference Output Voltage	V_{REFP}			2.012		V
Negative Reference Output Voltage	V_{REFN}			0.988		V
Differential Reference Output Voltage Range	ΔV_{REF}	ΔV_{REF} = V_{REFP} - V_{REFN}	0.98	1.024	1.07	V
REFIN Resistance	R_{REFIN}			>50		MΩ

Dual 10-Bit, 40Msps, 3V, Low-Power ADC with Internal Reference and Multiplexed Parallel Outputs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 2.5V, 0.1µF and 1µF capacitors from REFP, REFN, and COM to GND; REFOUT connected to REFIN through a 10kΩ resistor, V_{IN} = $2V_{P-P}$ (differential w.r.t. COM), C_L = 10pF at digital outputs (Note 5), f_{CLK} = 40MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum REFP, COM Source Current	I_{SOURCE}			5		mA
Maximum REFP, COM Sink Current	I_{SINK}			-250		µA
Maximum REFN Source Current	I_{SOURCE}			250		µA
Maximum REFN Sink Current	I_{SINK}			-5		mA
UNBUFFERED EXTERNAL REFERENCE (V_{REFIN} = GND, reference voltage applied to REFP, REFN, and COM)						
REFP, REFN Input Resistance	R_{REFP}, R_{REFN}	Measured between REFP and COM, and REFN and COM		4		kΩ
Differential Reference Input Voltage	ΔV_{REF}	$\Delta V_{REF} = V_{REFP} - V_{REFN}$		1.024 ±10%		V
COM Input Voltage	V_{COM}			$V_{DD}/2$ ±10%		V
REFP Input Voltage	V_{REFP}			$V_{COM} + \Delta V_{REF}/2$		V
REFN Input Voltage	V_{REFN}			$V_{COM} - \Delta V_{REF}/2$		V
DIGITAL INPUTS (CLK, PD, $\overline{OE}$, SLEEP, T/B)						
Input High Threshold	V_{IH}	CLK	$0.8 \times V_{DD}$			V
		PD, $\overline{OE}$, SLEEP, T/B	$0.8 \times OV_{DD}$			
Input Low Threshold	V_{IL}	CLK			$0.2 \times V_{DD}$	V
		PD, $\overline{OE}$, SLEEP, T/B			$0.2 \times OV_{DD}$	
Input Hysteresis	V_{HYST}			0.1		V
Input Leakage	I_{IH}	$V_{IH} = OV_{DD}$ or V_{DD} (CLK)			±5	µA
	I_{IL}	V_{IL} = 0			±5	
Input Capacitance	C_{IN}			5		pF
DIGITAL OUTPUTS (D0A/B–D9A/B, A/B)						
Output Voltage Low	V_{OL}	I_{SINK} = -200µA			0.2	V
Output Voltage High	V_{OH}	I_{SOURCE} = 200µA	OV_{DD} - 0.2			V
Three-State Leakage Current	I_{LEAK}	$\overline{OE} = OV_{DD}$			±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{OE} = OV_{DD}$		5		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 2.5V, 0.1µF and 1µF capacitors from REFP, REFN, and COM to GND; REFOUT connected to REFIN through a 10kΩ resistor, V_{IN} = $2V_{P-P}$ (differential w.r.t. COM), C_L = 10pF at digital outputs (Note 5), f_{CLK} = 40MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Analog Supply Voltage Range	V_{DD}		2.7	3.0	3.6	V
Output Supply Voltage Range	OV_{DD}		1.7	2.5	3.6	V
Analog Supply Current	I_{VDD}	Operating, $f_{INA\ or\ B}$ = 20MHz at -0.5dB FS		35	50	mA
		Sleep mode		2.8		
		Shutdown, clock idle, PD = $\overline{OE}$ = OV_{DD}		1	15	µA
Output Supply Current	I_{OVDD}	Operating, C_L = 15pF, $f_{INA\ or\ B}$ = 20MHz at -0.5dB FS		4		mA
		Sleep mode		100		µA
		Shutdown, clock idle, PD = $\overline{OE}$ = OV_{DD}		2	10	
Power Dissipation	PDISS	Operating, $f_{INA\ or\ B}$ = 20MHz at -0.5dB FS		105	150	mW
		Sleep mode		8.4		
		Shutdown, clock idle, PD = $\overline{OE}$ = OV_{DD}		3	45	µW
Power-Supply Rejection Ratio	PSRR	Offset		±0.2		mV/V
		Gain		±0.1		%/V
TIMING CHARACTERISTICS						
CLK Rise to CHA Output Data Valid	t_{DOA}	Figure 3 (Note 3)		5	8	ns
CLK Fall to CHB Output Data Valid	t_{DOB}	Figure 3 (Note 3)		5	8	ns
Clock Rise/Fall to A/B Rise/Fall Time	$t_{DA/B}$			6		ns
Output Enable Time	t_{ENABLE}	Figure 4		10		ns
Output Disable Time	$t_{DISABLE}$	Figure 4		1.5		ns
CLK Pulse Width High	t_{CH}	Figure 3, clock period: 25ns		12.5 ±3.8		ns
CLK Pulse Width Low	t_{CL}	Figure 3, clock period: 25ns		12.5 ±3.8		ns
Wake-Up Time	t_{WAKE}	Wake-up from sleep mode (Note 4)		0.41		µs
		Wake-up from shutdown (Note 4)		1.5		
CHANNEL-TO-CHANNEL MATCHING						
Crosstalk		$f_{INA\ or\ B}$ = 20MHz at -0.5dB FS		-70		dB
Gain Matching		$f_{INA\ or\ B}$ = 20MHz at -0.5dB FS		0.02	±0.2	dB
Phase Matching		$f_{INA\ or\ B}$ = 20MHz at -0.5dB FS		0.25		degrees

Note 1: SNR, SINAD, THD, SFDR, and HD3 are based on an analog input voltage of -0.5dB FS referenced to a 1.024V full-scale input voltage range.

Note 2: Intermodulation distortion is the total power of the intermodulation products relative to the individual carrier. This number is 6dB or better, if referenced to the two-tone envelope.

Note 3: Digital outputs settle to V_{IH} and V_{IL}. Parameter guaranteed by design.

Note 4: With REFIN driven externally, REFP, COM, and REFN are left floating while powered down.

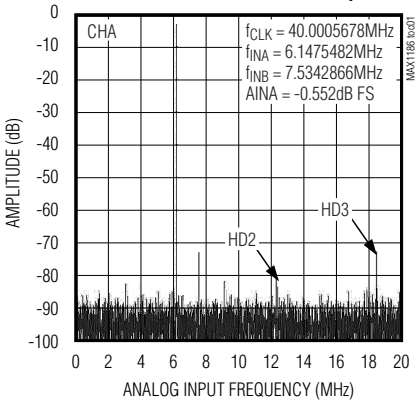
Note 5: Equivalent dynamic performance is obtainable over full OV_{DD} range with reduced C_L.

Dual 10-Bit, 40Msps, 3V, Low-Power ADC with Internal Reference and Multiplexed Parallel Outputs

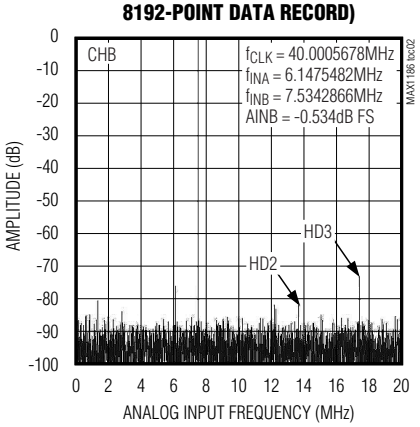
Typical Operating Characteristics

(V_{DD} = 3V, OV_{DD} = 2.5V, V_{REFIN} = 2.048V, differential input at -0.5dB FS, f_{CLK} = 40.00057MHz, C_L ≈ 10pF, T_A = +25°C, unless otherwise noted.)

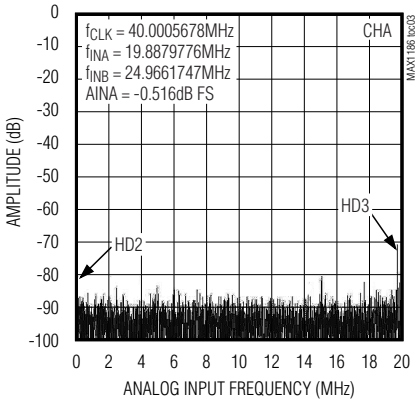
FFT PLOT CHA (DIFFERENTIAL INPUT, 8192-POINT DATA RECORD)



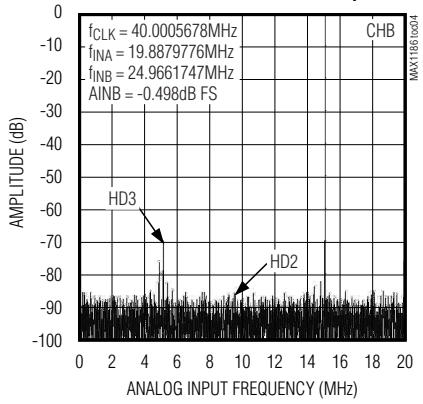
FFT PLOT CHB (DIFFERENTIAL INPUT, 8192-POINT DATA RECORD)



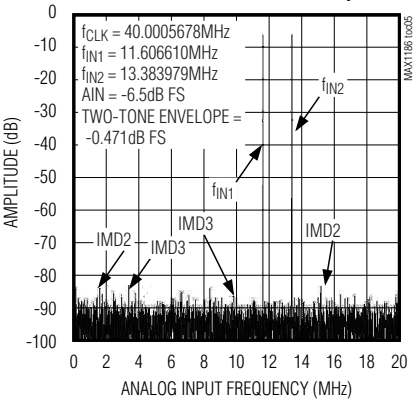
FFT PLOT CHA (DIFFERENTIAL INPUT, 8192-POINT DATA RECORD)



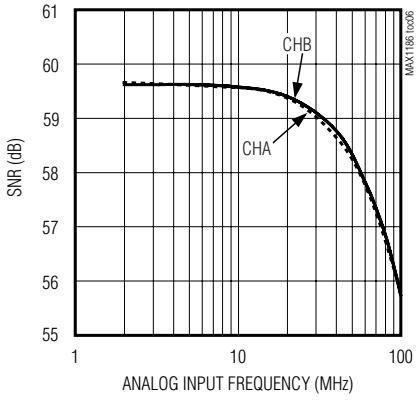
FFT PLOT CHB (DIFFERENTIAL INPUT, 8192-POINT DATA RECORD)



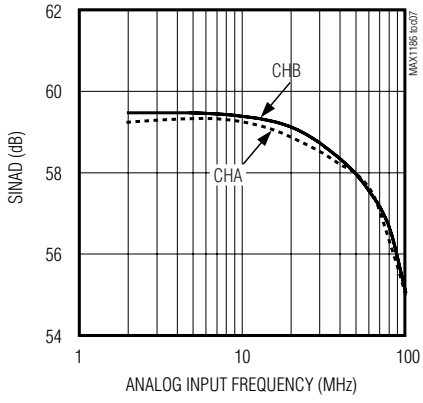
TWO-TONE IMD PLOT (DIFFERENTIAL INPUT, 8192-POINT DATA RECORD)



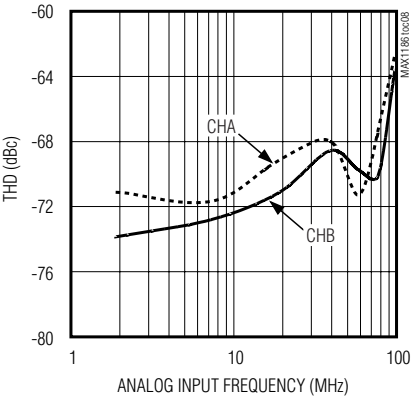
SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT FREQUENCY



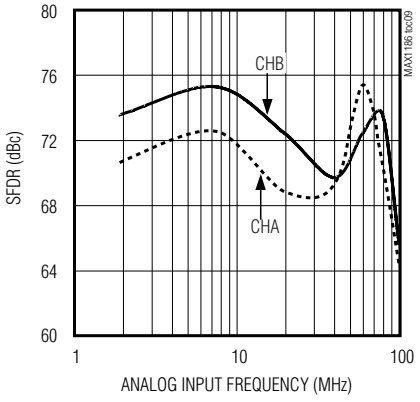
SIGNAL-TO-NOISE PLUS DISTORTION vs. ANALOG INPUT FREQUECNY



TOTAL HARMONIC DISTORTION vs. ANALOG INPUT FREQUENCY



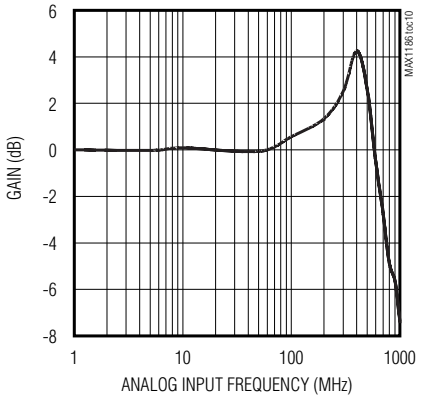
SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY



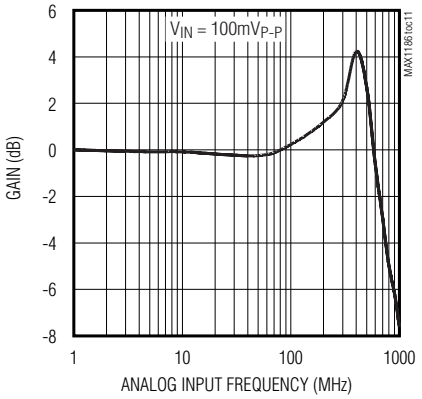
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 2.5V, V_{REFIN} = 2.048V, differential input at -0.5dB FS, f_{CLK} = 40.00057MHz, C_L ≈ 10pF, T_A = +25°C, unless otherwise noted.)

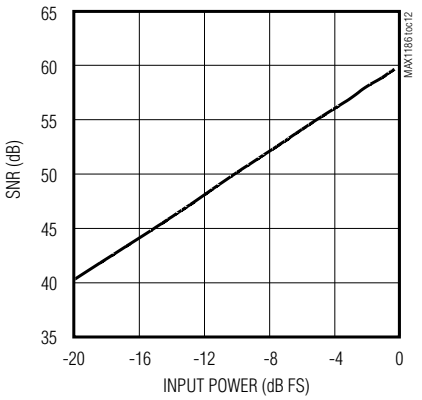
FULL-POWER INPUT BANDWIDTH vs. ANALOG INPUT FREQUENCY, SINGLE-ENDED



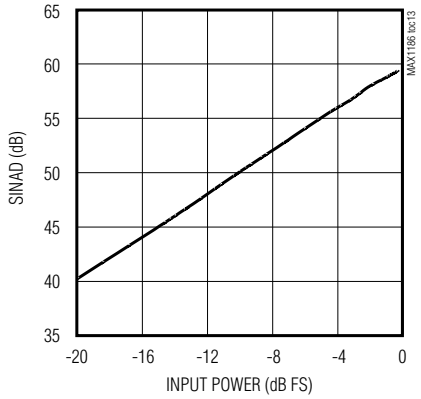
SMALL-SIGNAL INPUT BANDWIDTH vs. ANALOG INPUT FREQUENCY, SINGLE-ENDED



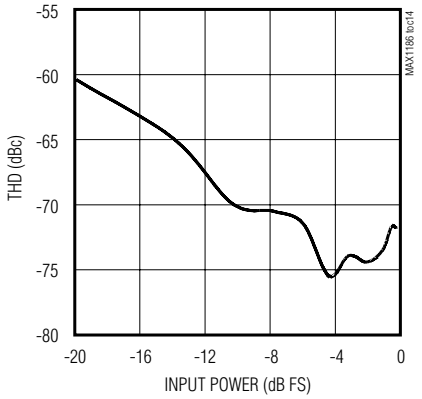
SIGNAL-TO-NOISE RATIO vs. INPUT POWER (f_{IN} = 19.8879776MHz)



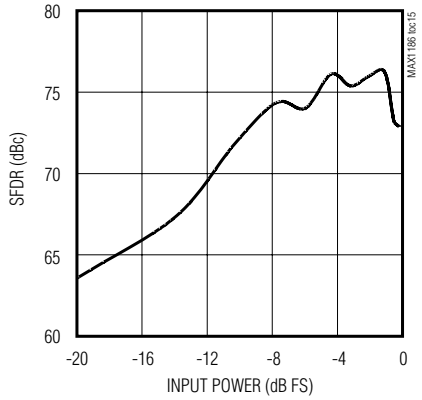
SIGNAL-TO-NOISE PLUS DISTORTION vs. INPUT POWER (f_{IN} = 19.8879776MHz)



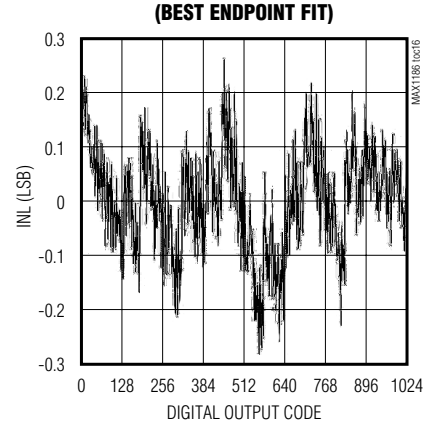
TOTAL HARMONIC DISTORTION vs. INPUT POWER (f_{IN} = 19.8879776MHz)



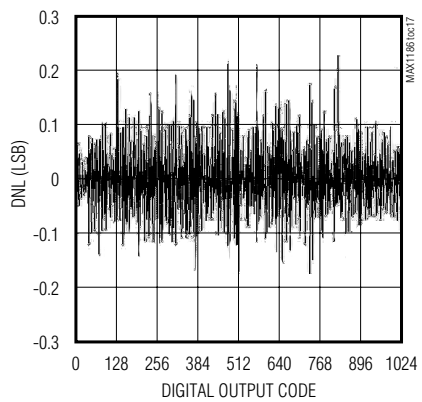
SPURIOUS-FREE DYNAMIC RANGE vs. INPUT POWER (f_{IN} = 19.8879776MHz)



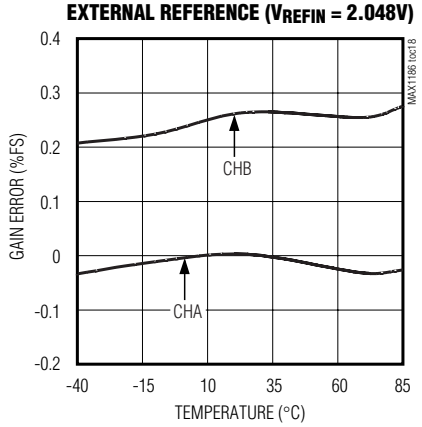
INTEGRAL NONLINEARITY (BEST ENDPOINT FIT)



DIFFERENTIAL NONLINEARITY



GAIN ERROR vs. TEMPERATURE EXTERNAL REFERENCE (V_{REFIN} = 2.048V)

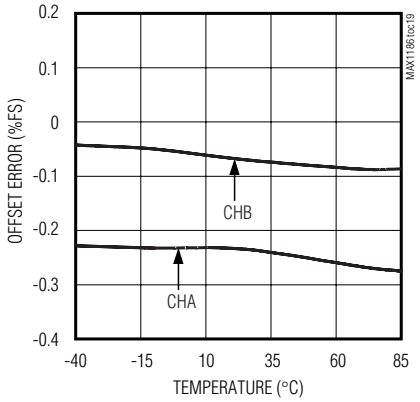


Dual 10-Bit, 40Msps, 3V, Low-Power ADC with Internal Reference and Multiplexed Parallel Outputs

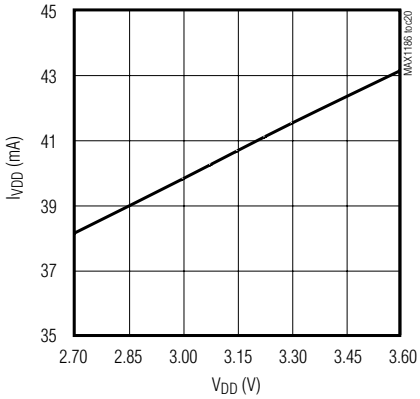
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 2.5V, V_{REFIN} = 2.048V, differential input at -0.5dB FS, f_{CLK} = 40.00057MHz, C_L ≈ 10pF, T_A = +25°C, unless otherwise noted.)

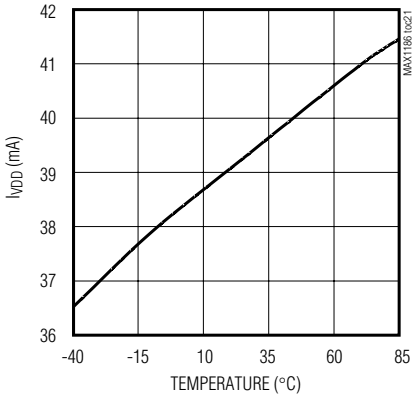
OFFSET ERROR vs. TEMPERATURE EXTERNAL REFERENCE (V_{REFIN} = 2.048V)



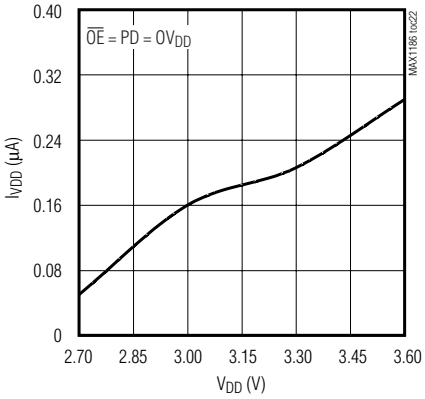
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



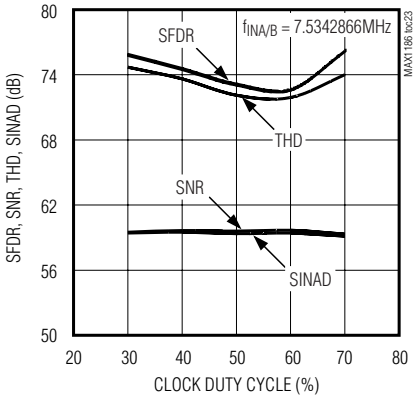
ANALOG SUPPLY CURRENT vs. TEMPERATURE



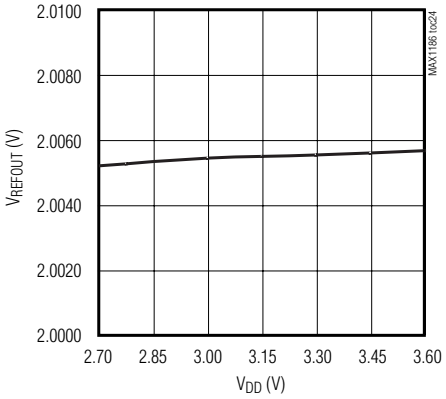
ANALOG POWER-DOWN CURRENT vs. ANALOG POWER SUPPLY



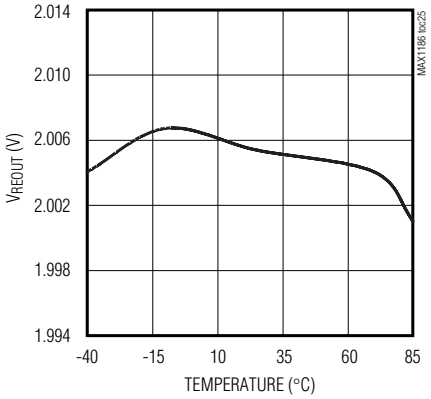
SFDR, SNR, THD, SINAD vs. CLOCK DUTY CTCLE



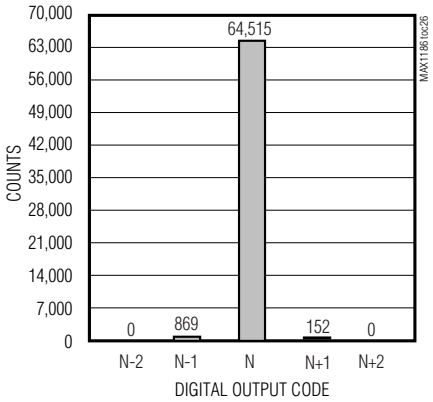
INTERNAL REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



OUTPUT NOISE HISTOGRAM (DC INPUT)



Pin Description

PIN	NAME	FUNCTION
1	COM	Common-Mode Voltage Input/Output. Bypass to GND with a ≥0.1µF capacitor.
2, 6, 11, 14, 15	V_{DD}	Analog Supply Voltage. Bypass to GND with a capacitor combination of 2.2µF in parallel with 0.1µF.
3, 7, 10, 13, 16	GND	Analog Ground
4	INA+	Channel A Positive Analog Input. For single-ended operation, connect signal source to INA+.
5	INA-	Channel A Negative Analog Input. For single-ended operation, connect INA- to COM.
8	INB-	Channel B Negative Analog Input. For single-ended operation, connect INB- to COM.
9	INB+	Channel B Positive Analog Input. For single-ended operation, connect signal source to INB+.
12	CLK	Converter Clock Input
17	T/B	T/B selects the ADC digital output format. High: Two's complement. Low: Straight offset binary.
18	SLEEP	Sleep Mode Input. High: Deactivates the two ADCs, but leaves the reference bias circuit active. Low: Normal operation.
19	PD	Power-Down Input. High: Power-down mode. Low: Normal operation.
20	$\overline{OE}$	Output Enable Input. High: Digital outputs disabled. Low: Digital outputs enabled.
21–29	N.C.	No Connection
30	A/B	A/B Data Indicator. This digital output indicates CHA data (A/B = 1) or CHB data (A/B = 0) to be present on the output. A/B follows the external clock signal with typically 6ns delay.
31, 34	OGND	Output Driver Ground
32, 33	OV_{DD}	Output Driver Supply Voltage. Bypass to OGND with a capacitor combination of 2.2µF in parallel with 0.1µF.
35	D0A/B	Three-State Digital Output, Bit 0 (LSB). Depending on status of A/B, output data reflects channel A or channel B data.
36	D1A/B	Three-State Digital Output, Bit 1. Depending on status of A/B, output data reflects channel A or channel B data.
37	D2A/B	Three-State Digital Output, Bit 2. Depending on status of A/B, output data reflects channel A or channel B data.
38	D3A/B	Three-State Digital Output, Bit 3. Depending on status of A/B, output data reflects channel A or channel B data.
39	D4A/B	Three-State Digital Output, Bit 4. Depending on status of A/B, output data reflects channel A or channel B data.
40	D5A/B	Three-State Digital Output, Bit 5. Depending on status of A/B, output data reflects channel A or channel B data.

Pin Description (continued)

PIN	NAME	FUNCTION
41	D6A/B	Three-State Digital Output, Bit 6. Depending on status of A/B, output data reflects channel A or channel B data.
42	D7A/B	Three-State Digital Output, Bit 7. Depending on status of A/B, output data reflects channel A or channel B data.
43	D8A/B	Three-State Digital Output, Bit 8. Depending on status of A/B, output data reflects channel A or channel B data.
44	D9A/B	Three-State Digital Output, Bit 9 (MSB). Depending on status of A/B, output data reflects channel A or channel B data.
45	REFOUT	Internal Reference Voltage Output. Maybe connected to REFIN through a resistor or a resistor-divider.
46	REFIN	Reference Input. $V_{REFIN} = 2 \times (V_{REFP} - V_{REFN})$. Bypass to GND with a >1nF capacitor.
47	REFP	Positive Reference Input/Output. Conversion range is $\pm(V_{REFP} - V_{REFN})$. Bypass to GND with a >0.1µF capacitor.
48	REFN	Negative Reference Input/Output. Conversion range is $\pm(V_{REFP} - V_{REFN})$. Bypass to GND with a >0.1µF capacitor.

Detailed Description

The MAX1186 uses a nine-stage, fully-differential, pipelined architecture (Figure 1) that allows for high-speed conversion while minimizing power consumption. Samples taken at the inputs move progressively through the pipeline stages every one-half clock cycle. Including the delay through the output latch, the total clock-cycle latency is five clock cycles.

1.5-bit (2-comparator) flash ADCs convert the held input voltages into a digital code. The digital-to-analog converters (DACs) convert the digitized results back into analog voltages, which are then subtracted from the original held input signals. The resulting error signals are then multiplied by two and the residues are passed along to the next pipeline stages, where the process is repeated until the signals have been processed by all nine stages. Digital error correction compensates for ADC comparator offsets in each of these pipeline stages and ensures no missing codes.

Both input channels are sampled on the rising edge of the clock and the resulting data is multiplexed at the output. CHA data is updated on the rising edge (5 clock cycles later) and CHB data is updated on the falling edge (5.5 clock cycles later) of the clock signal. The A/B indicator follows the clock signal with a typical delay time of 6ns and remains high when CHA data is updated and low when CHB data is updated.

Input Track-and-Hold (T/H) Circuits

Figure 2 displays a simplified functional diagram of the input track-and-hold (T/H) circuits in both track- and hold-mode. In track mode, switches S1, S2a, S2b, S4a, S4b, S5a, and S5b are closed. The fully-differential circuits sample the input signals onto the two capacitors (C2a and C2b) through switches S4a and S4b. S2a and S2b set the common mode for the amplifier input, and open simultaneously with S1, sampling the input waveform. Switches S4a and S4b are then opened before switches S3a and S3b connect capacitors C1a and C1b to the output of the amplifier and switch S4c is closed. The resulting differential voltages are held on capacitors C2a and C2b. The amplifiers are used to charge capacitors C1a and C1b to the same values originally held on C2a and C2b. These values are then presented to the first stage quantizers and isolate the pipelines from the fast-changing inputs. The wide input bandwidth T/H amplifiers allow the MAX1186 to track and sample/hold analog inputs of high frequencies (> Nyquist). Both ADC inputs (INA+, INB+, INA-, and INB-) can be driven either differentially or single-ended. Match the impedance of INA+ and INA-, as well as INB+ and INB-, and set the common-mode voltage to midsupply ($V_{DD}/2$) for optimum performance.

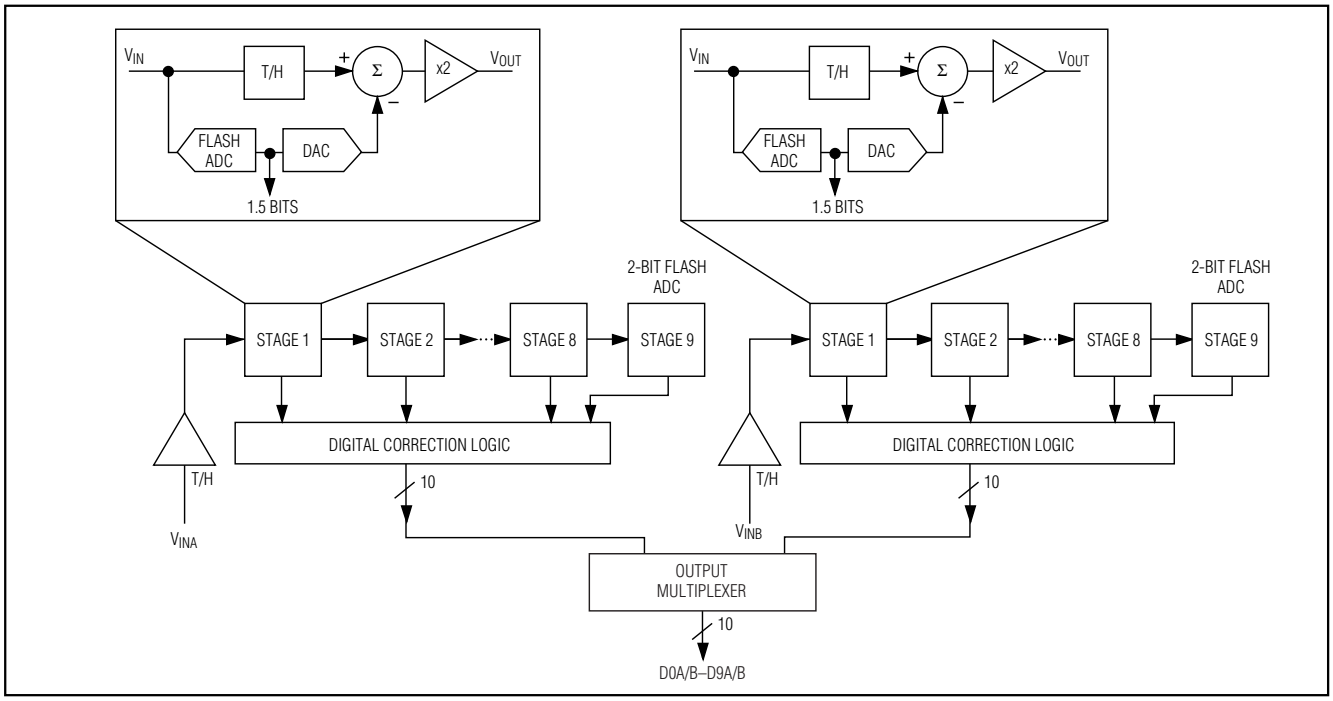


Figure 1. Pipelined Architecture—Stage Blocks

Dual 10-Bit, 40Msps, 3V, Low-Power ADC with Internal Reference and Multiplexed Parallel Outputs

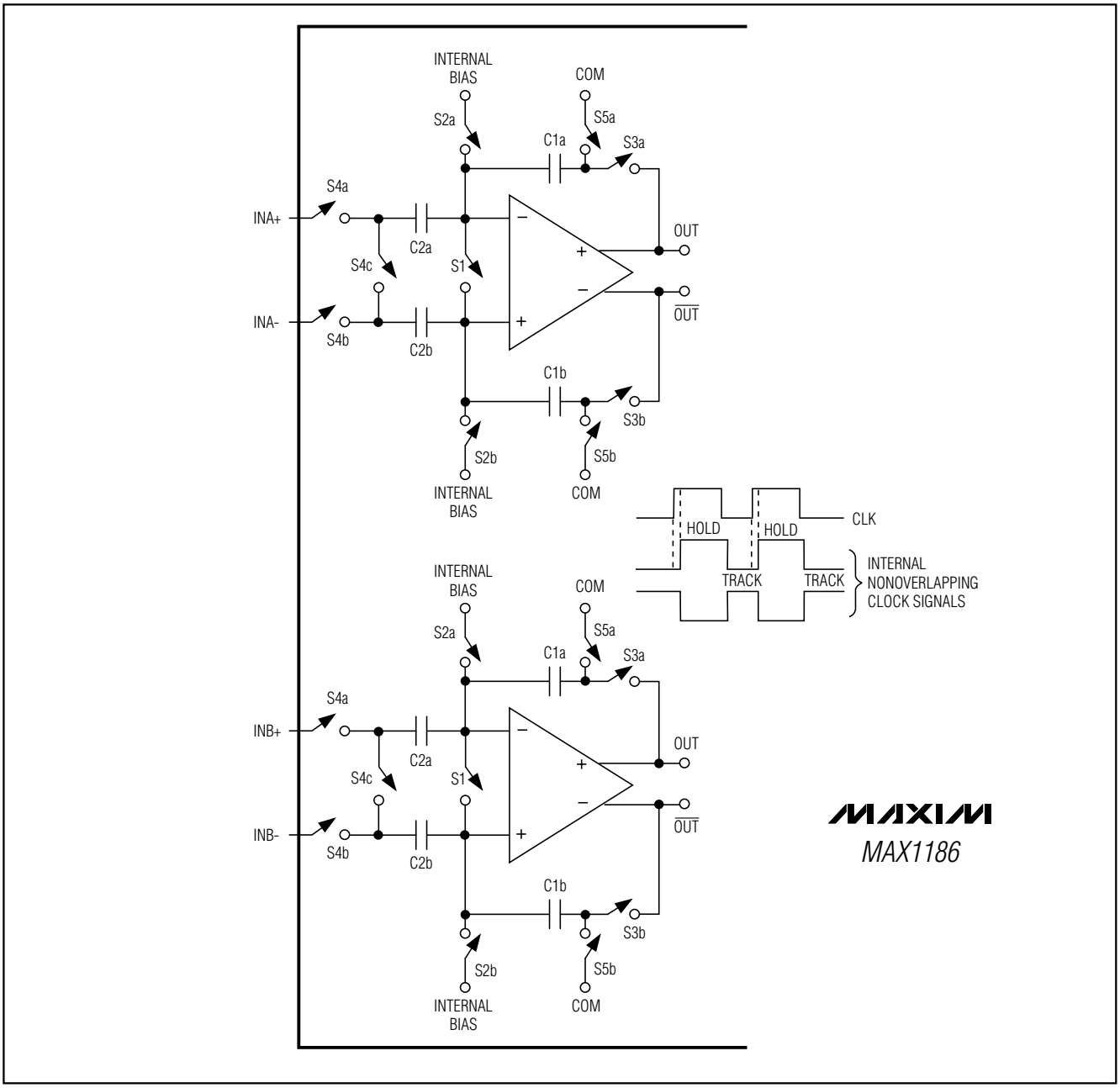


Figure 2. MAX1186 T/H Amplifiers

Analog Inputs and Reference Configurations

The full-scale range of the MAX1186 is determined by the internally generated voltage difference between REFP ($V_{DD}/2 + V_{REFIN}/4$) and REFN ($V_{DD}/2 - V_{REFIN}/4$). The full-scale range for both on-chip ADCs is adjustable through the REFIN pin, which is provided for this purpose.

REFOUT, REFP, COM ($V_{DD}/2$), and REFN are internally buffered low-impedance outputs.

The MAX1186 provides three modes of reference operation:

- Internal reference mode
- Buffered external reference mode
- Unbuffered external reference mode

In internal reference mode, connect the internal reference output REFOUT to REFIN through a resistor (e.g., 10kΩ) or resistor-divider, if an application requires a reduced full-scale range. For stability and noise filtering purposes, bypass REFIN with a >10nF capacitor to GND. In internal reference mode, REFOUT, COM, REFP, and REFN become low-impedance outputs.

In buffered external reference mode, adjust the reference voltage levels externally by applying a stable and accurate voltage at REFIN. In this mode, COM, REFP, and REFN become outputs. REFOUT may be left open or connected to REFIN through a >10kΩ resistor.

In unbuffered external reference mode, connect REFIN to GND. This deactivates the on-chip reference buffers for REFP, COM, and REFN. With their buffers shut down, these nodes become high impedance and may be driven through separate, external reference sources.

Clock Input (CLK)

The MAX1186's CLK input accepts CMOS-compatible clock signals. Since the interstage conversion of the device depends on the repeatability of the rising and falling edges of the external clock, use a clock with low jitter and fast rise and fall times (< 2ns). In particular, sampling occurs on the rising edge of the clock signal, requiring this edge to provide lowest possible jitter. Any significant aperture jitter would limit the SNR performance of the on-chip ADCs as follows:

$$SNR_{dB} = 20 \times \log_{10} (1 / [2\pi \times f_{IN} \times t_{AJ}])$$

where f_{IN} represents the analog input frequency and t_{AJ} is the time of the aperture jitter.

Clock jitter is especially critical for undersampling applications. The clock input should always be considered as an analog input and routed away from any analog input or other digital signal lines.

The MAX1186 clock input operates with a voltage threshold set to $V_{DD}/2$. Clock inputs with a duty cycle other than 50%, must meet the specifications for high and low periods as stated in the *Electrical Characteristics*.

System Timing Requirements

Figure 3 shows the relationship between clock and analog input, A/B indicator, and the resulting CHA/CHB data output. CHA and CHB data are sampled on the rising edge of the clock signal. Following the rising edge of the 5th clock cycles, the digitized value of the original CHA sample is presented at the output. This followed one-half clock cycle later by the digitized value of the original CHB sample.

A channel selection signal (A/B indicator) allows the user to determine which output data represents which input channel. With A/B = 1, digitized data from CHA is present at the output and with A/B = 0 digitized data from CHB is present.

Digital Output Data, Output Data Format Selection (T/B), Output Enable ($\overline{OE}$), Channel Selection (A/B)

All digital outputs, D0A/B–D9A/B (CHA or CHB data) and A/B are TTL/CMOS logic-compatible. The output coding can be chosen to be either offset binary or two's complement (Table 1) controlled by a single pin (T/B). Pull T/B low to select offset binary and high to activate two's complement output coding. The capacitive load on the digital outputs D0A/B–D9A/B should be kept as low as possible (<15pF), to avoid large digital currents that could feed back into the analog portion of the MAX1186, thereby degrading its dynamic performance. Using buffers on the digital outputs of the ADCs can further isolate the digital outputs from heavy capacitive loads. To further improve the dynamic performance of the MAX1186, small-series resistors (e.g., 100Ω) may be added to the digital output paths, close to the MAX1186.

Figure 4 displays the timing relationship between output enable and data output valid as well as power-down/wake-up and data output valid.

Power-Down (PD) and Sleep (SLEEP) Modes

The MAX1186 offers two power-save modes—sleep and full power-down mode. In sleep mode (SLEEP = 1), only the reference bias circuit is active (both ADCs are disabled), and current consumption is reduced to 2.8mA.

To enter full power-down mode, pull PD high. With $\overline{OE}$ simultaneously low, all outputs are latched at the last value prior to the power-down. Pulling $\overline{OE}$ high, forces the digital outputs into a high-impedance state.

Dual 10-Bit, 40Msps, 3V, Low-Power ADC with Internal Reference and Multiplexed Parallel Outputs

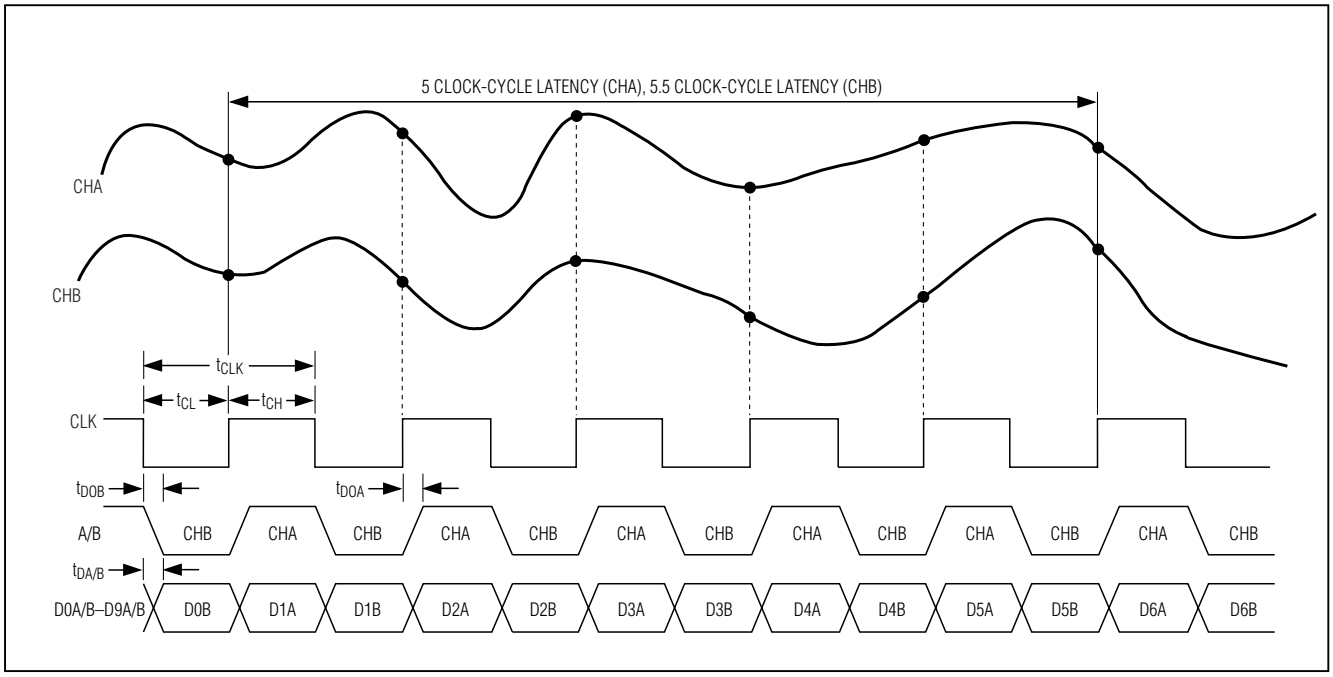


Figure 3. Timing Diagram for Multiplexed Outputs

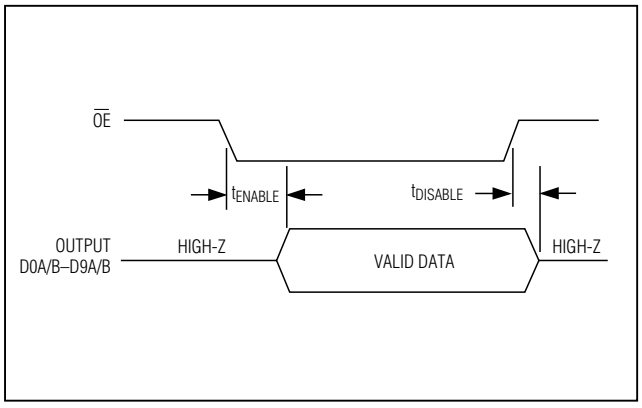


Figure 4. Output Timing Diagram

Applications Information

Figure 5 depicts a typical application circuit containing two single-ended to differential converters. The internal reference provides a $V_{DD}/2$ output voltage for level shifting purposes. The input is buffered and then split to a voltage follower and inverter. One lowpass filter per ADC suppresses some of the wideband noise associated with high-speed operational amplifiers that follows the amplifiers. The user may select the R_{ISO} and C_{IN} values to optimize the filter performance, to suit a particular application. For the application in Figure 5, a R_{ISO} of 50Ω is placed before the capacitive load to prevent ringing and oscillation. The 22pF C_{IN} capacitor acts as a small bypassing capacitor.

Using Transformer Coupling

An RF transformer (Figure 6) provides an excellent solution to convert a single-ended source signal to a fully differential signal, required by the MAX1186 for optimum performance. Connecting the center tap of the transformer to COM provides a $V_{DD}/2$ DC level shift to the input. Although a 1:1 transformer is shown, a step-up transformer may be selected to reduce the drive requirements. A reduced signal swing from the input driver, such as an op amp, may also improve the overall distortion.

In general, the MAX1186 provides better SFDR and THD with fully differential input signals than single-ended drive, especially for very high input frequencies. In differential input mode, even-order harmonics are lower as both inputs (INA+, INA- and/or INB+, INB-) are balanced, and each of the ADC inputs only requires half the signal swing compared to single-ended mode.

Table 1. MAX1186 Output Codes For Differential Inputs

DIFFERENTIAL INPUT VOLTAGE*	DIFFERENTIAL INPUT	STRAIGHT OFFSET BINARY T/B = 0	TWO'S COMPLEMENT T/B = 1
V_{REF} x 511/512	+FULL SCALE - 1LSB	11 1111 1111	01 1111 1111
V_{REF} x 1/512	+1LSB	10 0000 0001	00 0000 0001
0	Bipolar Zero	10 0000 0000	00 0000 0000
- V_{REF} x 1/512	-1LSB	01 1111 1111	11 1111 1111
-V_{REF} x 511/512	- FULL SCALE + 1LSB	00 0000 0001	10 0000 0001
-V_{REF} x 512/512	- FULL SCALE	00 0000 0000	10 0000 0000

*$V_{REF} = V_{REFP} - V_{REFN}$

Single-Ended AC-Coupled Input Signal

Figure 7 shows an AC-coupled, single-ended application. Amplifiers like the MAX4108 provide high speed, high bandwidth, low noise, and low distortion to maintain the integrity of the input signal.

Typical QAM Demodulation Application

The most frequently used modulation technique for digital communications applications is probably the Quadrature Amplitude Modulation (QAM). Typically found in spread-spectrum based systems, a QAM signal represents a carrier frequency modulated in both amplitude and phase. At the transmitter, modulating the baseband signal with quadrature outputs, a local oscillator followed by subsequent up-conversion can generate the QAM signal. The result is an in-phase (I) and a quadrature (Q) carrier component, where the Q component is 90 degree phase-shifted with respect to the in-phase component. At the receiver, the QAM signal is divided down into it's I and Q components, essentially representing the modulation process reversed. Figure 8 displays the demodulation process performed in the analog domain, using the dual matched 3V, 10-bit ADC MAX1186, and the MAX2451 quadrature demodulator to recover and digitize the I and Q baseband signals. Before being digitized by the MAX1186, the mixed-down signal components may be filtered by matched analog filters, such as Nyquist or pulse-shaping filters. These remove any unwanted images from the mixing process, thereby enhancing the overall signal-to-noise (SNR) performance and minimizing intersymbol interference.

Grounding, Bypassing, and Board Layout

The MAX1186 requires high-speed board layout design techniques. Locate all bypass capacitors as close to the device as possible, preferably on the same side as the ADC, using surface-mount devices for minimum inductance. Bypass V_{DD}, REFP, REFN, and COM with two parallel 0.1µF ceramic capacitors and a 2.2µF bipolar capacitor to GND. Follow the same rules to bypass the digital supply (OV_{DD}) to OGND. Multilayer boards with separated ground and power planes produce the highest level of signal integrity. Consider the use of a split ground plane arranged to match the physical location of the analog ground (GND) and the digital output driver ground (OGND) on the ADC's package. The two ground planes should be joined at a single point such that the noisy digital ground currents do not interfere with the analog ground plane. The ideal location of this connection can be determined experimentally at a point along the gap between the two ground planes, which produces optimum results. Make this connection with a low-value, surface-mount resistor (1Ω to 5Ω), a ferrite bead, or a direct short. Alternatively, all ground pins could share the same ground plane, if the ground plane is sufficiently isolated from any noisy, digital systems ground plane (e.g., downstream output buffer or DSP ground plane). Route high-speed digital signal traces away from the sensitive analog traces of either channel. Make sure to isolate the analog input lines to each respective converter to minimize channel-to-channel crosstalk. Keep all signal lines short and free of 90 degree turns.

Dual 10-Bit, 40Msps, 3V, Low-Power ADC with Internal Reference and Multiplexed Parallel Outputs

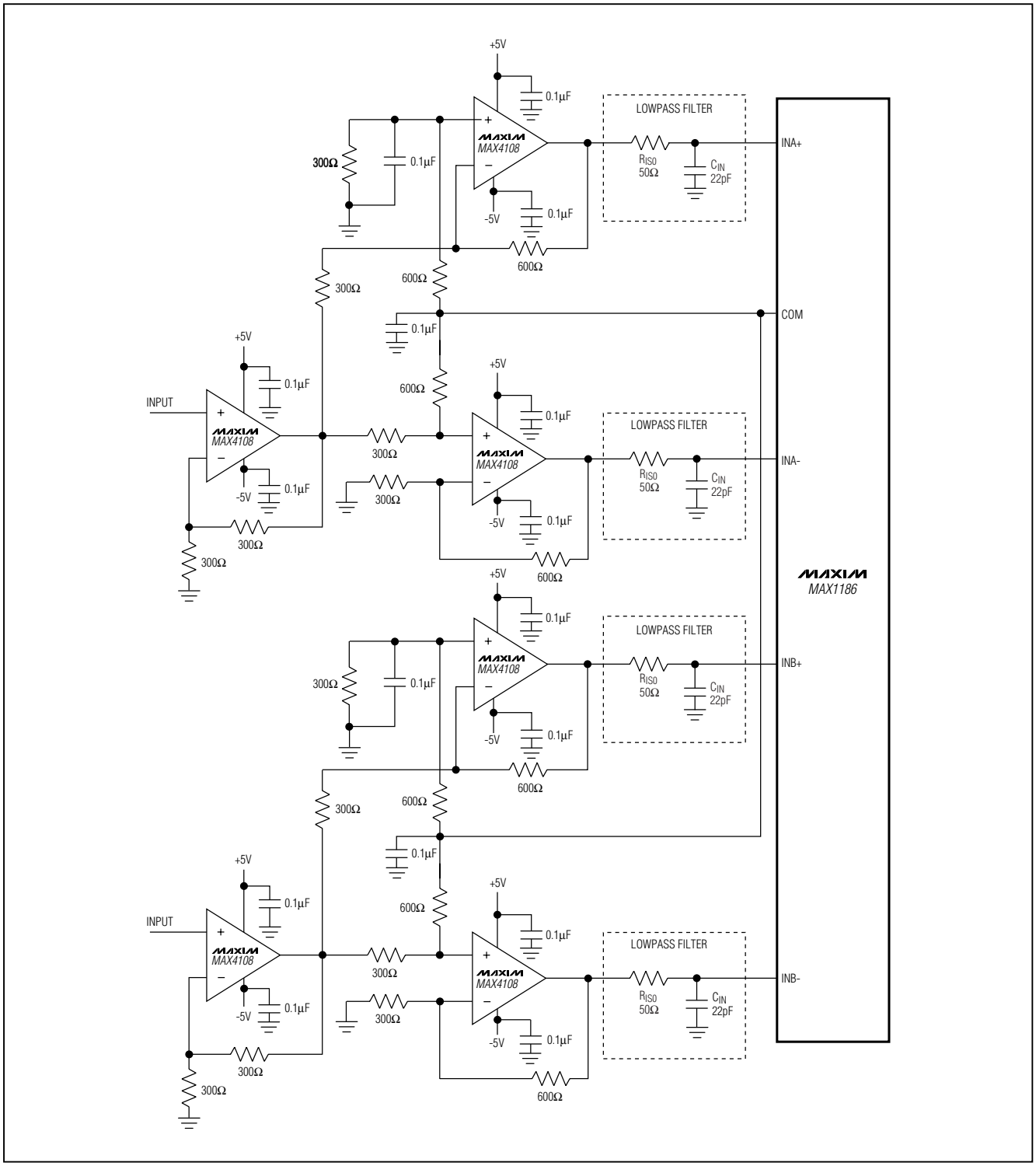


Figure 5. Typical Application for Single-Ended to Differential Conversion

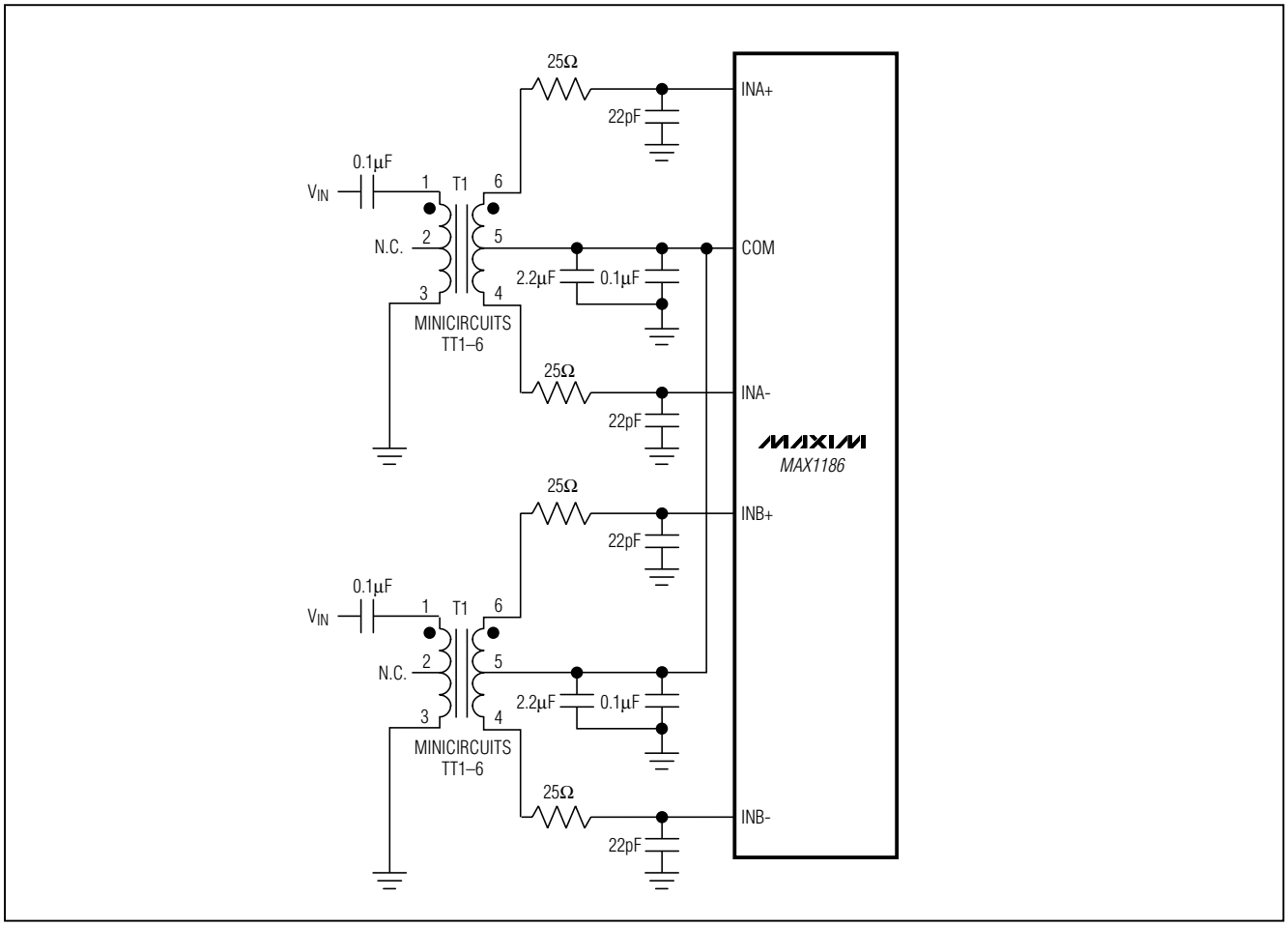


Figure 6. Transformer-Coupled Input Drive

Static Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1186 are measured using the best straight-line fit method.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Dynamic Parameter Definitions

Aperture Jitter

Figure 9 depicts the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the falling edge of the sampling clock and the instant when an actual sample is taken (Figure 9).

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantiza-

Dual 10-Bit, 40Msps, 3V, Low-Power ADC with Internal Reference and Multiplexed Parallel Outputs

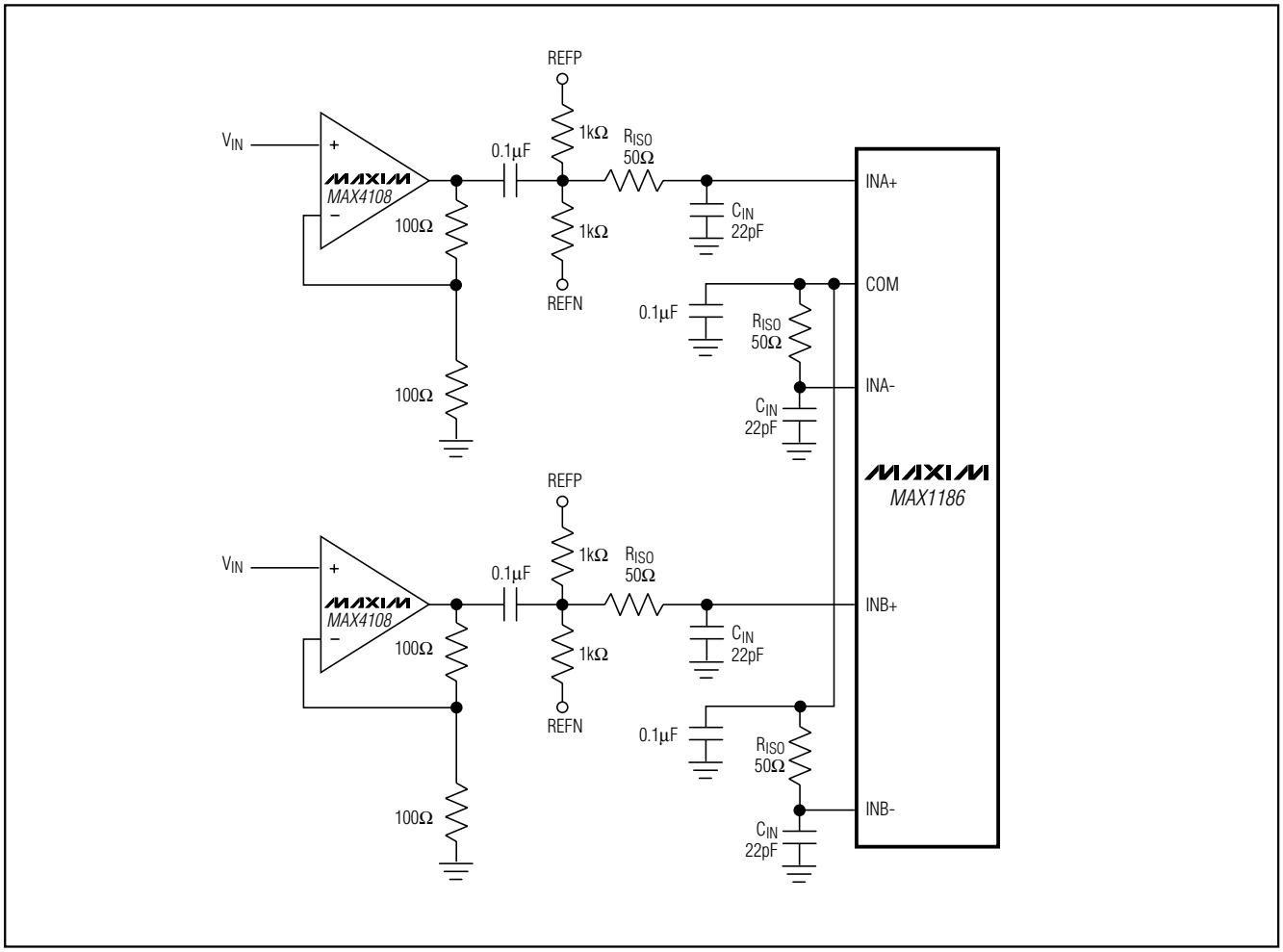


Figure 7: Using an Op Amp for Single-Ended, AC-Coupled Input Drive

tion error only and results directly from the ADC's resolution (N-Bits):

$$SNR_{dB[max]} = 6.02_{dB} \times N + 1.76_{dB}$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to all spectral components minus the fundamental and the DC offset.

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC error consists of quantization noise only. ENOB is computed from:

$$ENOB = \frac{SINAD_{dB} - 1.76_{dB}}{6.02_{dB}}$$

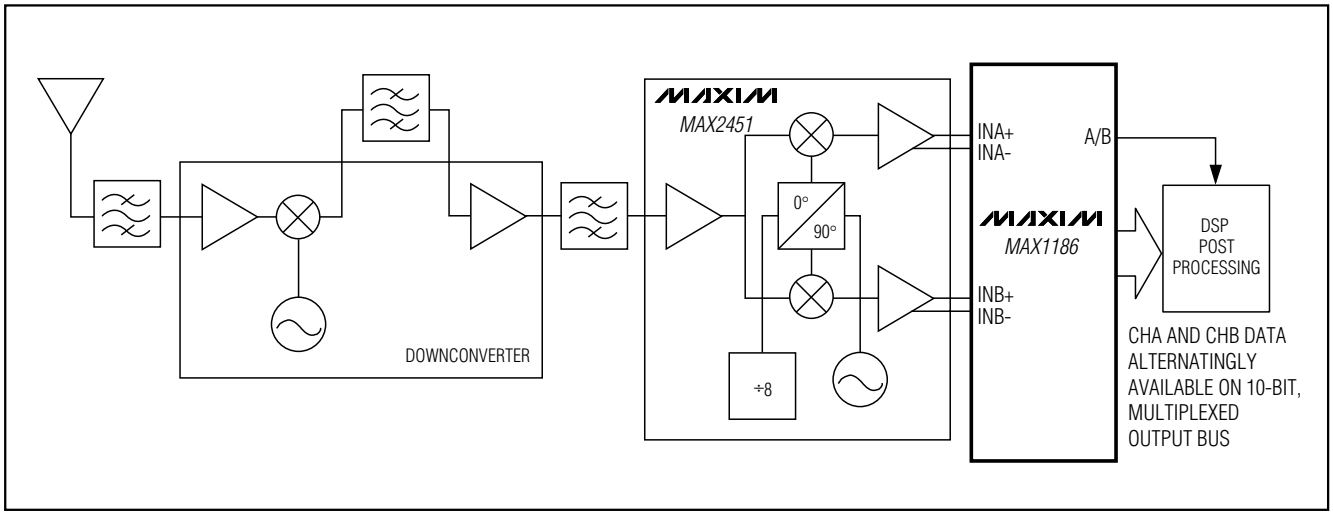


Figure 8. Typical QAM Application, Using the MAX1186

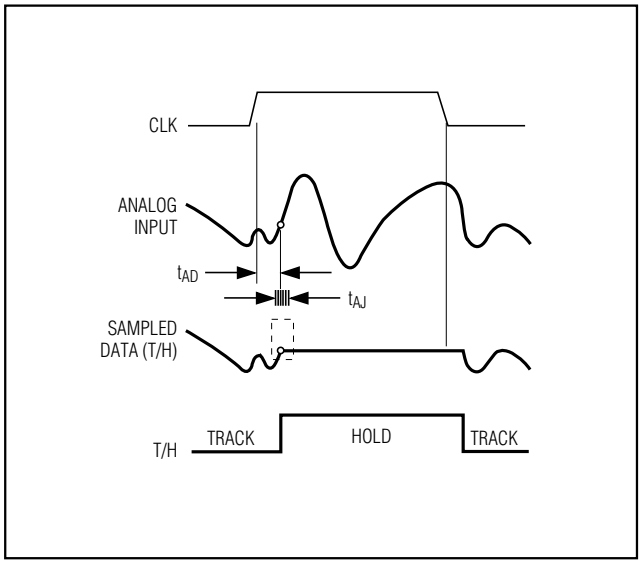


Figure 9. T/H Aperture Timing

Total Harmonic Distortion (THD)

THD is typically the ratio of the RMS sum of the first four harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log_{10}\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}\right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.

Intermodulation Distortion (IMD)

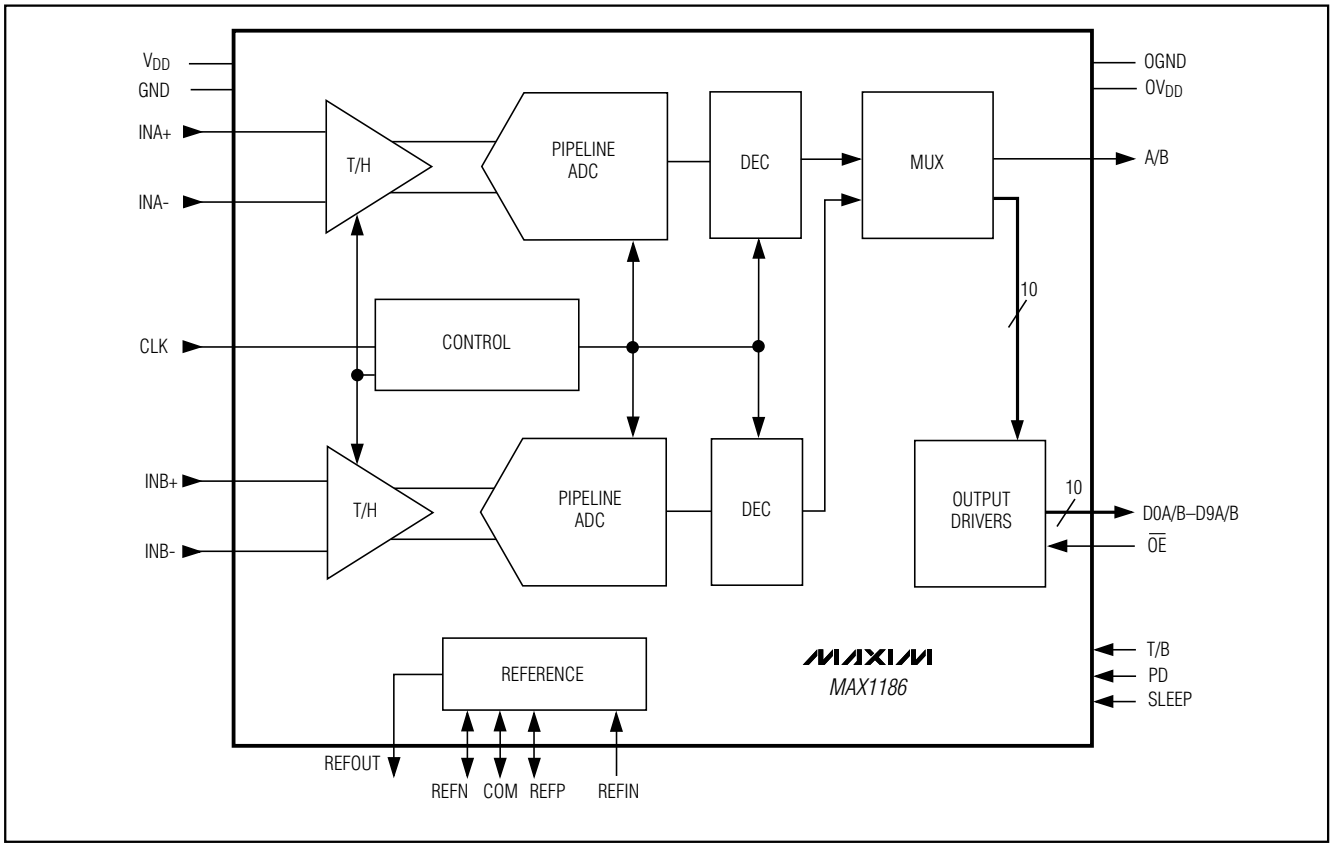
The two-tone IMD is the ratio expressed in decibels of either input tone to the worst 3rd-order (or higher) intermodulation products. The individual input tone levels are at -6.5dB full scale and their envelope is at -0.5dB full scale.

Chip Information

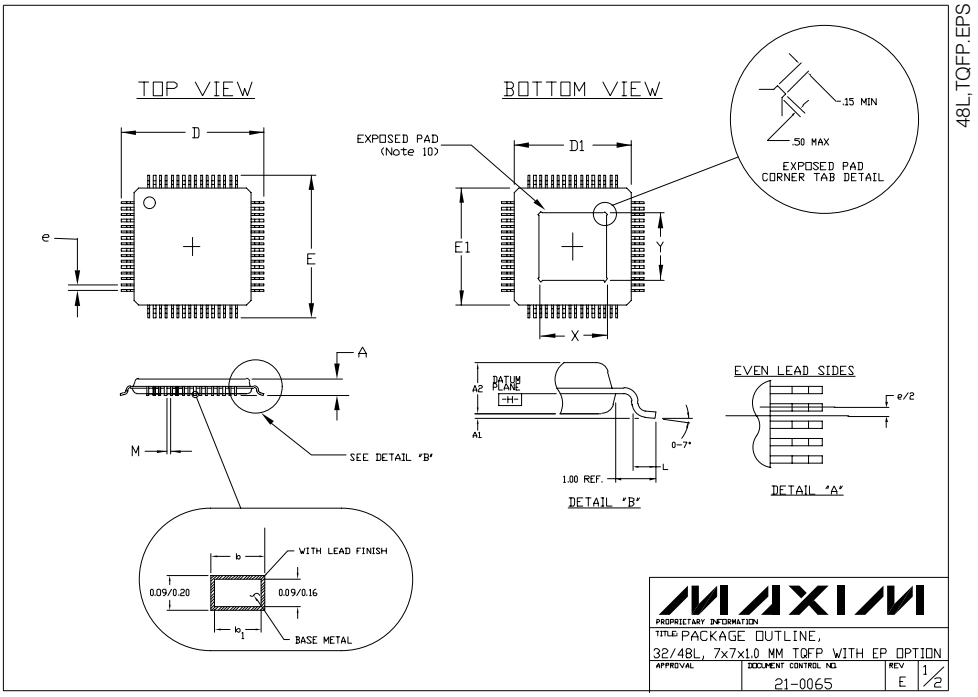
TRANSISTOR COUNT: 10,811
PROCESS: CMOS

Dual 10-Bit, 40Msps, 3V, Low-Power ADC with Internal Reference and Multiplexed Parallel Outputs

Functional Diagram



Package Information



NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS AC AND AE.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS					
	AC			AE		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.20	---	---	1.20
A_1	0.05	0.10	0.15	0.05	0.10	0.15
A_2	0.95	1.00	1.05	0.95	1.00	1.05
D	9.00 BSC.			9.00 BSC.		
D_1	7.00 BSC.			7.00 BSC.		
E	9.00 BSC.			9.00 BSC.		
E_1	7.00 BSC.			7.00 BSC.		
L	0.45	0.60	0.75	0.45	0.60	0.75
M	0.15	---	---	0.14	---	---
N	32			48		
e	0.80 BSC.			0.50 BSC.		
b	0.30	0.37	0.45	0.17	0.22	0.27
b1	0.30	0.35	0.40	0.17	0.20	0.23
*X	3.20	3.50	3.80	3.70	4.00	4.30
*Y	3.20	3.50	3.80	3.70	4.00	4.30

* EXPOSED PAD (Note 10)

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE,
32/48L, 7x7x1.0 MM TQFP WITH EP OPTION
APPROVAL
DOCUMENT CONTROL NO.
21-0065
REV
E
2/2

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