

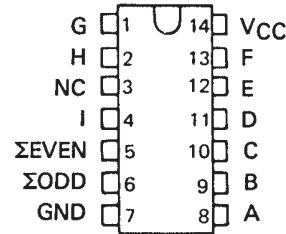
# SN54LS280, SN54S280, SN74LS280, SN74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

SDLS152 – DECEMBER 1972 – REVISED MARCH 1988

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits
- Can Be Used to Upgrade Existing Systems using MSI Parity Circuits
- Typical Data-to-Output Delay of Only 14 ns for 'S280 and 33 ns for 'LS280
- Typical Power Dissipation:  
'LS280 . . . 80 mW  
'S280 . . . 335 mW

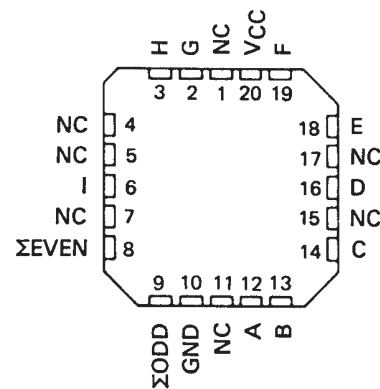
SN54LS280, SN54S280 . . . J OR W PACKAGE  
SN74LS280, SN74S280 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS280, SN54S280 . . . FK PACKAGE

(TOP VIEW)



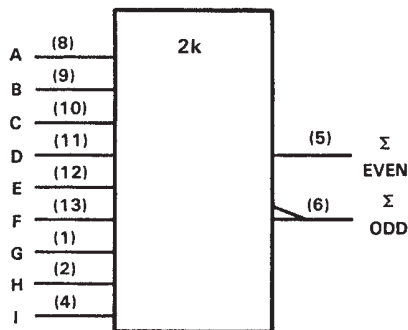
NC - No internal connection

FUNCTION TABLE

| NUMBER OF INPUTS A<br>THRU I THAT ARE HIGH | OUTPUTS |       |
|--------------------------------------------|---------|-------|
|                                            | Σ EVEN  | Σ ODD |
| 0, 2, 4, 6, 8                              | H       | L     |
| 1, 3, 5, 7, 9                              | L       | H     |

H = high level, L = low level

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

## description

These universal, monolithic, nine-bit parity generators/checkers utilize Schottky-clamped TTL high-performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading as shown under typical application data.

Series 54LS/74LS and Series 54S/74S parity generators/checkers offer the designer a trade-off between reduced power consumption and high performance. These devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the 'LS280 and 'S280 are implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the 'LS280 and 'S280 to be substituted for the '180 in existing designs to produce an identical function even if 'LS280's and 'S280's are mixed with existing '180's.

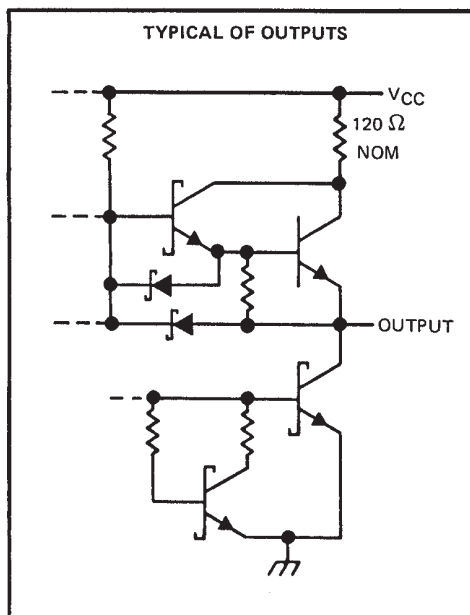
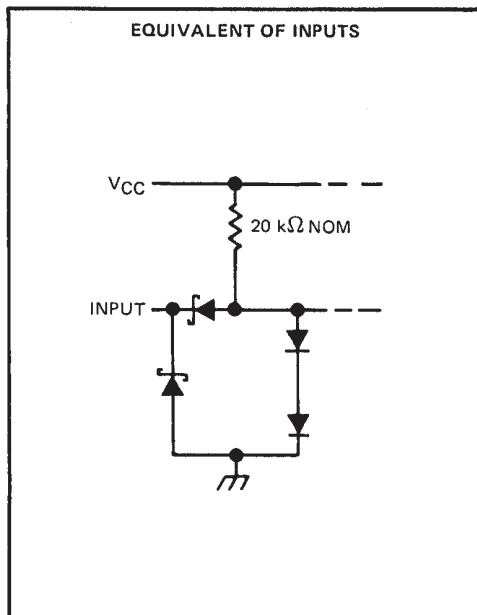
These devices are fully compatible with most other TTL circuits. All 'LS280 and 'S280 inputs are buffered to lower the drive requirements to one Series 54LS/74LS or Series 54S/74S standard load, respectively.

# SN54LS280, SN54S280, SN74LS280, SN74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

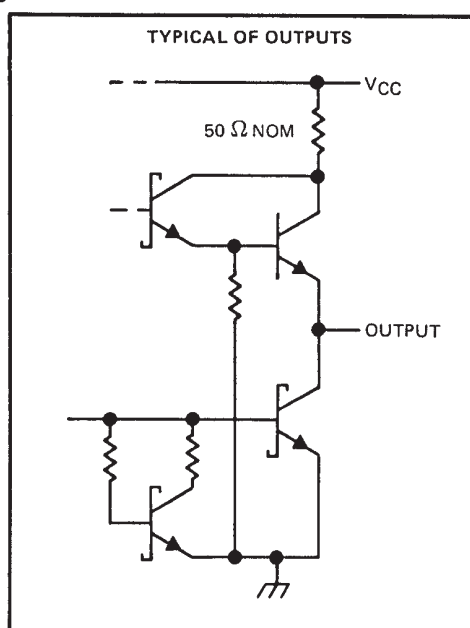
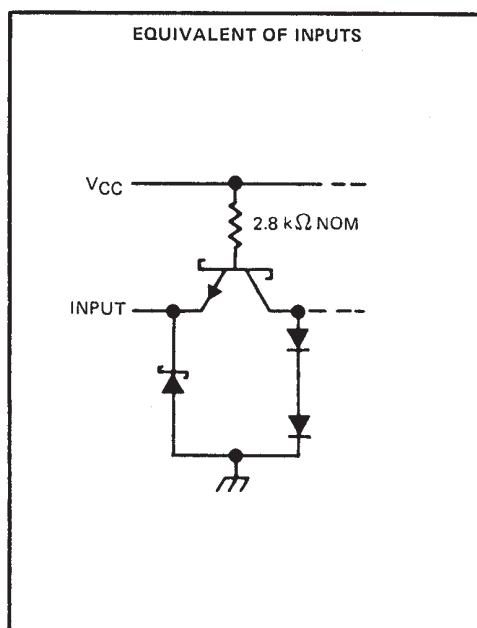
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## schematics of inputs and outputs

'LS280



'S280



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|                                                   |                 |
|---------------------------------------------------|-----------------|
| Supply voltage (see Note 1) .....                 | 7 V             |
| Input voltage: 'LS280 .....                       | 7 V             |
| 'S280 .....                                       | 5.5 V           |
| Operating free-air temperature range: SN54' ..... | – 55°C to 125°C |
| SN74' .....                                       | 0°C to 70°C     |
| Storage temperature range .....                   | – 65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

# SN54LS280, SN54S280, SN74LS280, SN74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

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## recommended operating conditions

|                                      | SN54LS280 |     |       | SN74LS280 |     |       | UNIT |
|--------------------------------------|-----------|-----|-------|-----------|-----|-------|------|
|                                      | MIN       | NOM | MAX   | MIN       | NOM | MAX   |      |
| $V_{CC}$ Supply voltage              | 4.5       | 5   | 5.5   | 4.75      | 5   | 5.25  | V    |
| $V_{IH}$ High-level input voltage    | 2         |     |       | 2         |     |       | V    |
| $V_{IL}$ Low-level input voltage     |           |     | 0.7   |           |     | 0.8   | V    |
| $I_{OH}$ High-level output current   |           |     | – 0.4 |           |     | – 0.4 | mA   |
| $I_{OL}$ Low-level output current    |           |     | 4     |           |     | 8     | mA   |
| $T_A$ Operating free-air temperature | – 55      |     | 125   | 0         |     | 70    | °C   |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS                                                                                 | SN54LS280 |      |       | SN74LS280 |      |          | UNIT |
|-----------|-------------------------------------------------------------------------------------------------|-----------|------|-------|-----------|------|----------|------|
|           |                                                                                                 | MIN       | TYP† | MAX   | MIN       | TYP† | MAX      |      |
| $V_{IK}$  | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$                                                     |           |      | – 1.5 |           |      | – 1.5    | V    |
| $V_{OH}$  | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$<br>$V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$ | 2.5       | 3.4  |       | 2.7       | 3.4  |          | V    |
| $V_{OL}$  | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$<br>$V_{IL} = \text{MAX}$                           | 0.25      | 0.4  |       | 0.25      | 0.4  |          | V    |
|           | $I_{OL} = 4 \text{ mA}$<br>$I_{OL} = 8 \text{ mA}$                                              |           |      |       |           |      | 0.35 0.5 |      |
| $I_I$     | $V_{CC} = \text{MAX}, V_I = 7 \text{ V}$                                                        |           |      | 0.1   |           |      | 0.1      | mA   |
| $I_{IH}$  | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$                                                      |           |      | 20    |           |      | 20       | μA   |
| $I_{IL}$  | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$                                                      |           |      | – 0.4 |           |      | – 0.4    | mA   |
| $I_{OS}§$ | $V_{CC} = \text{MAX}$                                                                           | – 20      |      | – 100 | – 20      |      | – 100    | mA   |
| $I_{CC}$  | $V_{CC} = \text{MAX},$ See Note 2                                                               |           | 16   | 27    |           | 16   | 27       | mA   |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with all inputs grounded and all outputs open.

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

| PARAMETER¶ | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS                                                       | MIN | TYP | MAX | UNIT |
|------------|-----------------|----------------|-----------------------------------------------------------------------|-----|-----|-----|------|
| tPLH       | Data            | Σ Even         | CL = 15 pF, RL = 2 kΩ,<br>Inputs not under test at 0 V,<br>See Note 3 |     | 33  | 50  | ns   |
| tPHL       |                 |                |                                                                       |     | 29  | 45  |      |
| tPLH       | Data            | Σ Odd          |                                                                       |     | 23  | 35  | ns   |
| tPHL       |                 |                |                                                                       |     | 31  | 50  |      |

¶  $t_{PLH}$  = propagation delay time, low-to-high-level output;  $t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



# SN54LS280, SN54S280, SN74LS280, SN74S280

## 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

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### recommended operating conditions

|                                       | SN54S280 |     |     | SN74S280 |     |      | UNIT |
|---------------------------------------|----------|-----|-----|----------|-----|------|------|
|                                       | MIN      | NOM | MAX | MIN      | NOM | MAX  |      |
| Supply voltage, $V_{CC}$              | 4.5      | 5   | 5.5 | 4.75     | 5   | 5.25 | V    |
| High-level output current, $I_{OH}$   |          |     | -1  |          |     | -1   | mA   |
| Low-level output current, $I_{OL}$    |          |     | 20  |          |     | 20   | mA   |
| Operating free-air temperature, $T_A$ | -55      |     | 125 | 0        |     | 70   | °C   |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                    | TEST CONDITIONS†                                                                                 | MIN       | TYP‡ | MAX  | UNIT |
|----------------------------------------------|--------------------------------------------------------------------------------------------------|-----------|------|------|------|
| $V_{IH}$ High-level input voltage            |                                                                                                  | 2         |      |      | V    |
| $V_{IL}$ Low-level input voltage             |                                                                                                  |           |      | 0.8  | V    |
| $V_{IK}$ Input clamp voltage                 | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$                                                      |           |      | -1.2 | V    |
| $V_{OH}$ High-level output voltage           | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$                                                     | 2.5       | 3.4  |      | V    |
|                                              | $V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$                                                 |           |      |      |      |
|                                              |                                                                                                  |           |      |      |      |
| $V_{OL}$ Low-level output voltage            | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$<br>$V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$ |           |      | 0.5  | V    |
| $I_I$ Input current at maximum input voltage | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$                                                       |           |      | 1    | mA   |
| $I_{IH}$ High-level input current            | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$                                                       |           |      | 50   | µA   |
| $I_{IL}$ Low-level input current             | $V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$                                                       |           |      | -2   | mA   |
| $I_{OS}$ Short-circuit output current§       | $V_{CC} = \text{MAX}$                                                                            | -40       |      | -100 | mA   |
| $I_{CC}$ Supply current                      | $V_{CC} = \text{MAX},$ See Note 2                                                                | SN54S280  | 67   | 99   | mA   |
|                                              |                                                                                                  | SN74S280  | 67   | 105  |      |
|                                              | $V_{CC} = \text{MAX}, T_A = 125^\circ\text{C},$<br>See Note 2                                    | SN54S280N |      | 94   | mA   |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with all inputs grounded and all outputs open.

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

| PARAMETER¶ | FROM<br>(INPUT) | TO<br>(OUTPUT) | TEST CONDITIONS                       | MIN | TYP  | MAX | UNIT |
|------------|-----------------|----------------|---------------------------------------|-----|------|-----|------|
| tPLH       | Data            | Σ Even         | CL = 15 pF, RL = 280 Ω,<br>See Note 3 |     | 14   | 21  | ns   |
| tPHL       |                 |                |                                       |     | 11.5 | 18  |      |
| tPLH       | Data            | Σ Odd          |                                       |     | 14   | 21  | ns   |
| tPHL       |                 |                |                                       |     | 11.5 | 18  |      |

¶  $t_{PLH}$  = propagation delay time, low-to-high-level output;  $t_{PHL}$  = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

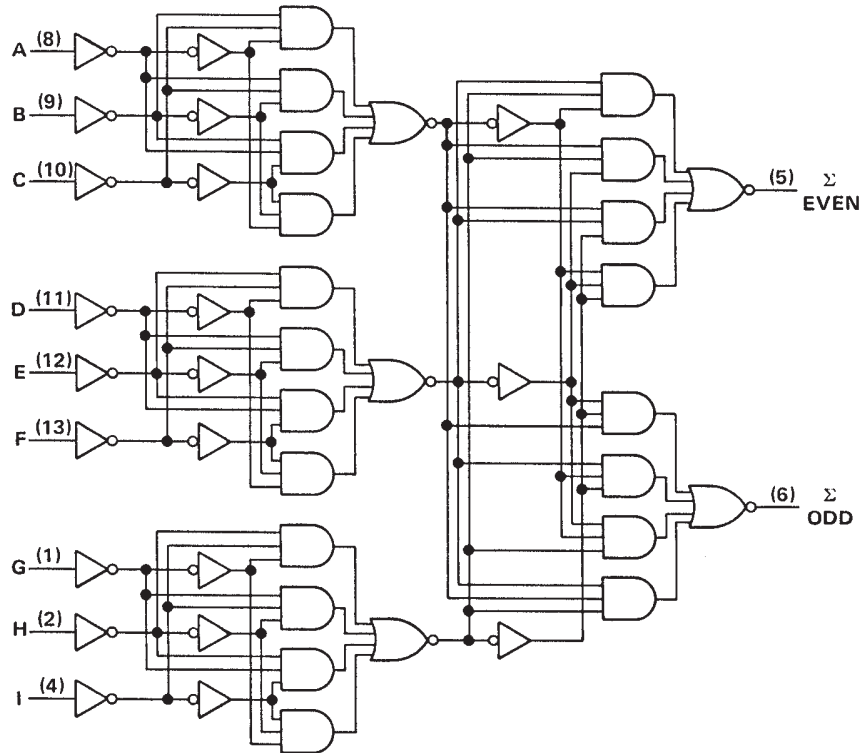


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# SN54LS280, SN54S280, SN74LS280, SN74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

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logic diagram (positive logic)

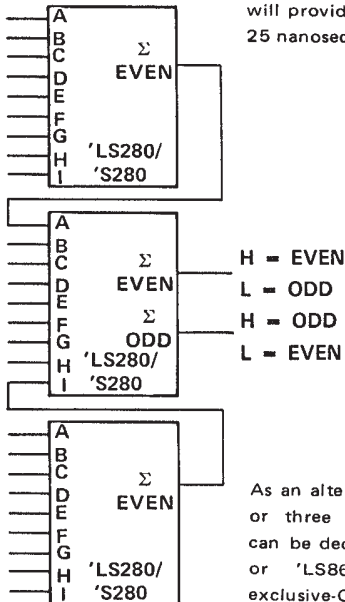


Pin numbers shown are for D, J, N, and W packages.

## TYPICAL APPLICATION DATA

### 25-LINE PARITY/GENERATOR CHECKER

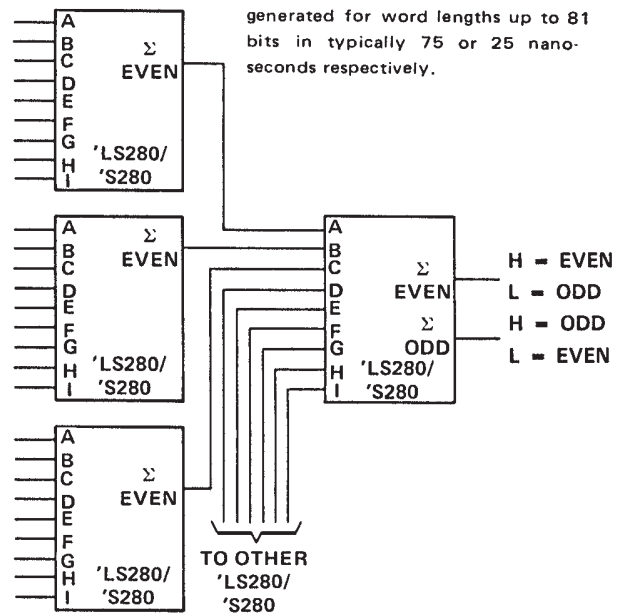
Three 'LS280's or 'S280's can be used to implement a 25-line parity generator/checker. This arrangement will provide parity in typically 75 or 25 nanoseconds respectively.



As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input ('S86 or 'LS86) or 3-input ('S135 or 'LS135) exclusive-OR gate for 18- or 27-line parity applications.

### 81-LINE PARITY/GENERATOR CHECKER

Longer word lengths can be implemented by cascading 'LS280's or 'S280's. As shown here, parity can be generated for word lengths up to 81 bits in typically 75 or 25 nanoseconds respectively.



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## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| JM38510/32901BCA | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>32901BCA    | <a href="#">Samples</a> |
| M38510/32901BCA  | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>32901BCA    | <a href="#">Samples</a> |
| M38510/32901BCA  | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | JM38510/<br>32901BCA    | <a href="#">Samples</a> |
| SN54LS280J       | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS280J              | <a href="#">Samples</a> |
| SN54LS280J       | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54LS280J              | <a href="#">Samples</a> |
| SN54S280J        | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54S280J               | <a href="#">Samples</a> |
| SN54S280J        | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SN54S280J               | <a href="#">Samples</a> |
| SN74LS280D       | ACTIVE        | SOIC         | D                  | 14   | 50             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS280                   | <a href="#">Samples</a> |
| SN74LS280D       | ACTIVE        | SOIC         | D                  | 14   | 50             | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | LS280                   | <a href="#">Samples</a> |
| SN74LS280N       | ACTIVE        | PDIP         | N                  | 14   | 25             | RoHS & Green        | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS280N              | <a href="#">Samples</a> |
| SN74LS280N       | ACTIVE        | PDIP         | N                  | 14   | 25             | RoHS & Green        | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN74LS280N              | <a href="#">Samples</a> |
| SN74LS280NSR     | ACTIVE        | SO           | NS                 | 14   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74LS280                 | <a href="#">Samples</a> |
| SN74LS280NSR     | ACTIVE        | SO           | NS                 | 14   | 2000           | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 74LS280                 | <a href="#">Samples</a> |
| SNJ54LS280J      | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS280J             | <a href="#">Samples</a> |
| SNJ54LS280J      | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS280J             | <a href="#">Samples</a> |
| SNJ54LS280W      | ACTIVE        | CFP          | W                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS280W             | <a href="#">Samples</a> |
| SNJ54LS280W      | ACTIVE        | CFP          | W                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54LS280W             | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SNJ54S280J       | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54S280J              | <a href="#">Samples</a> |
| SNJ54S280J       | ACTIVE        | CDIP         | J                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54S280J              | <a href="#">Samples</a> |
| SNJ54S280W       | ACTIVE        | CFP          | W                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54S280W              | <a href="#">Samples</a> |
| SNJ54S280W       | ACTIVE        | CFP          | W                  | 14   | 1              | Non-RoHS<br>& Green | SNPB                                 | N / A for Pkg Type   | -55 to 125   | SNJ54S280W              | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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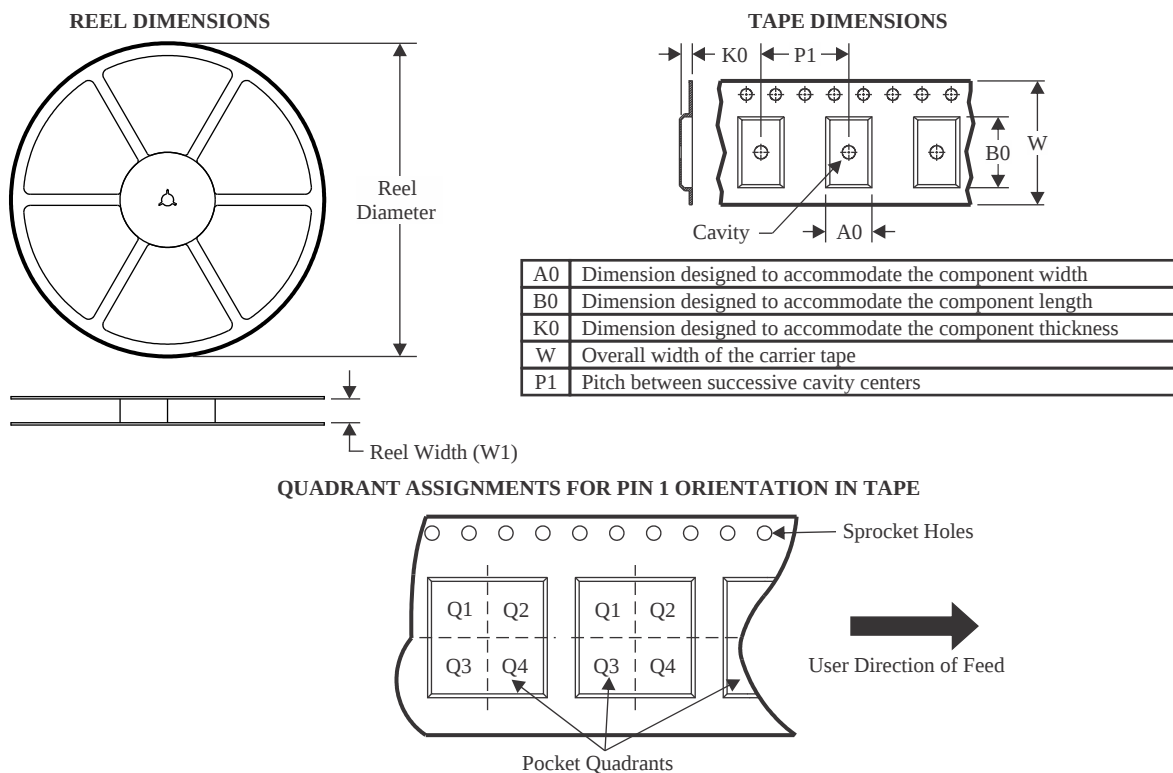
**OTHER QUALIFIED VERSIONS OF SN54LS280, SN74LS280 :**

- Catalog : [SN74LS280](#)
- Military : [SN54LS280](#)

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

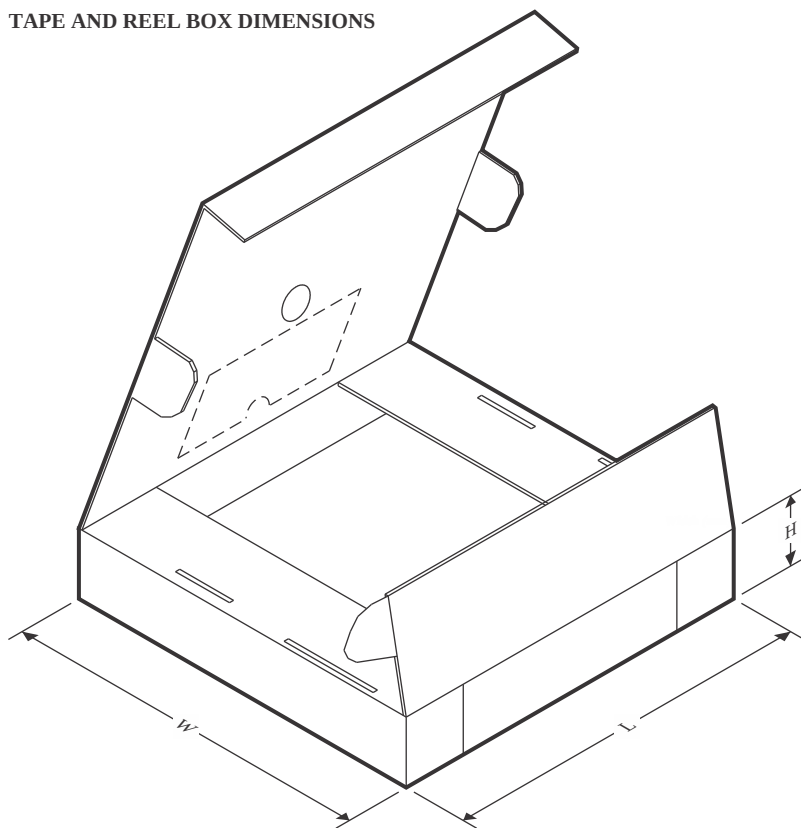
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS280NSR | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |

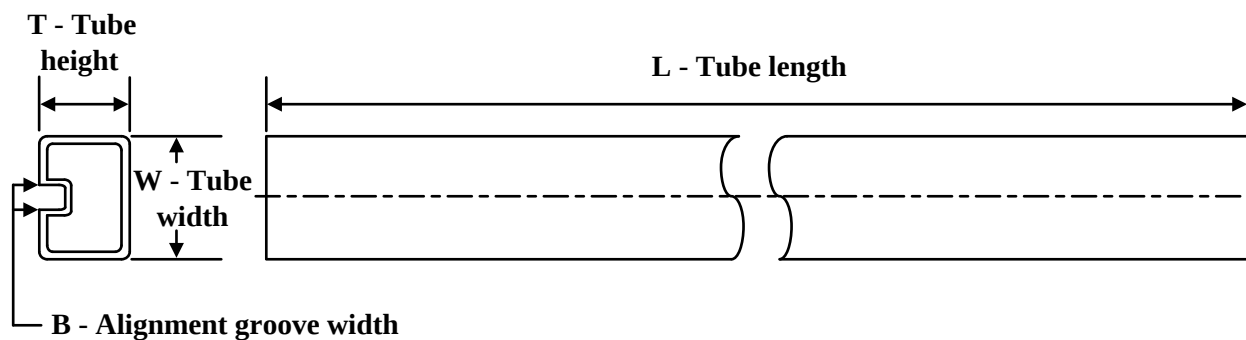
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS280NSR | SO           | NS              | 14   | 2000 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LS280D  | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74LS280N  | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74LS280N  | N            | PDIP         | 14   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54LS280W | W            | CFP          | 14   | 1   | 506.98 | 26.16  | 6220   | NA     |
| SNJ54S280W  | W            | CFP          | 14   | 1   | 506.98 | 26.16  | 6220   | NA     |

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

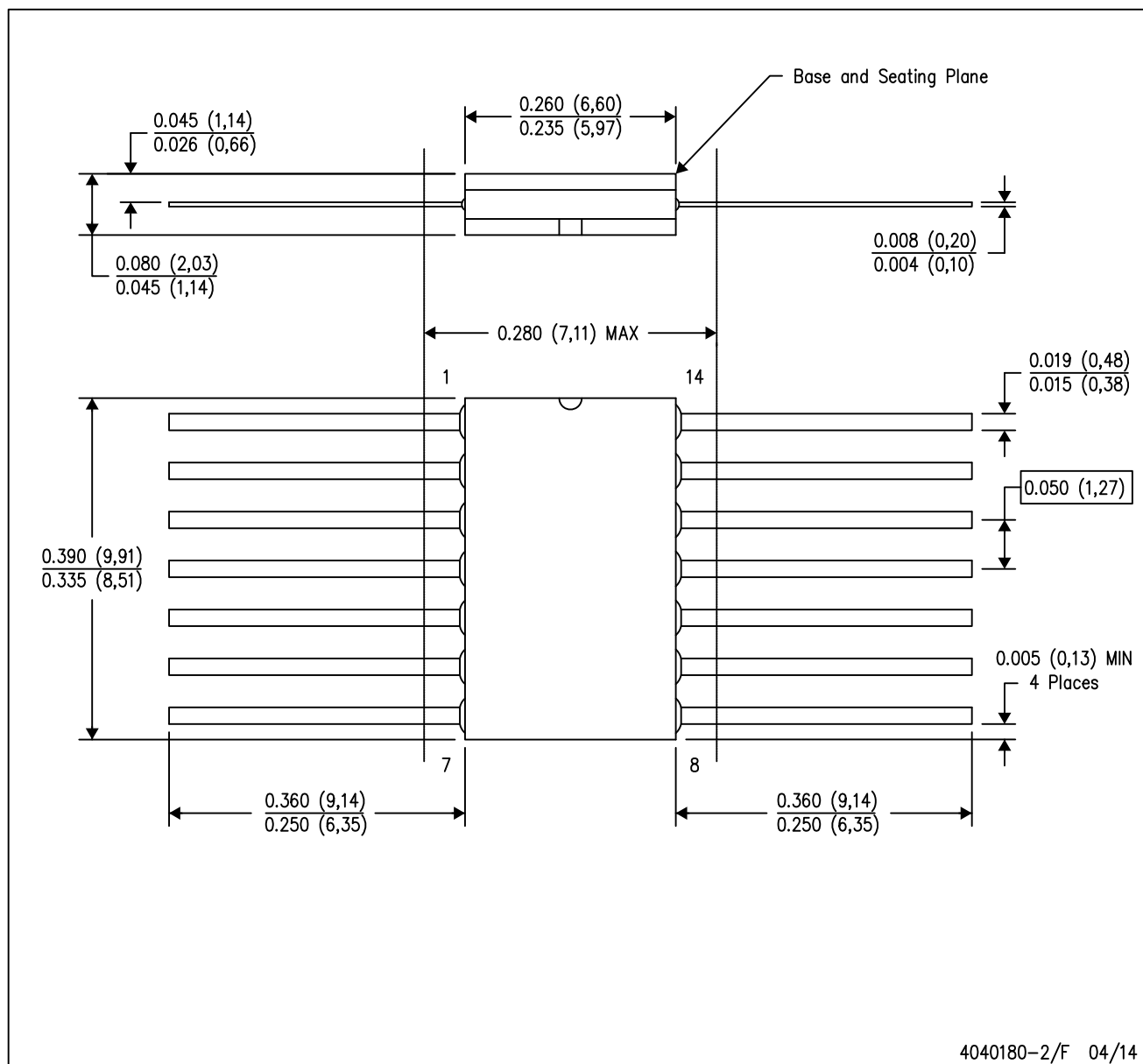
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

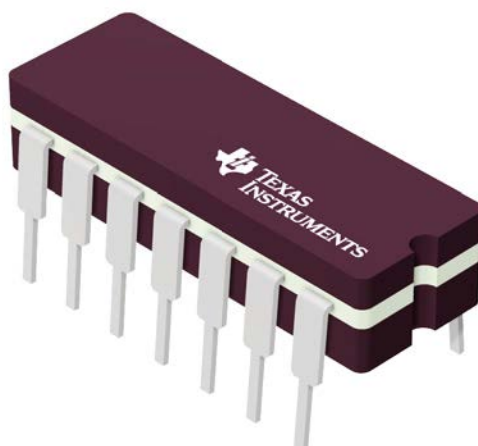


**J 14**

## GENERIC PACKAGE VIEW

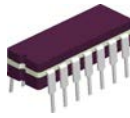
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE

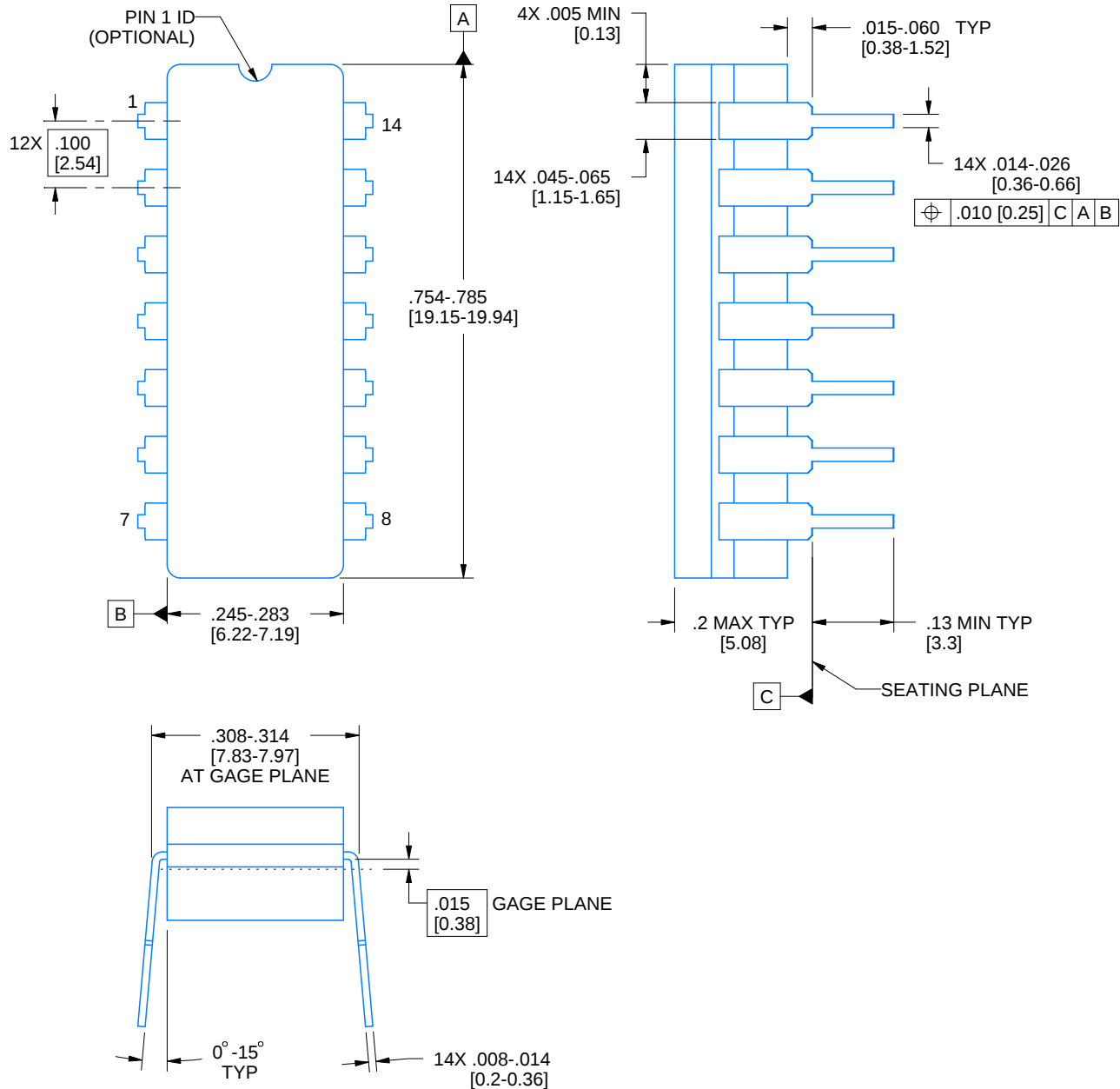


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

**J0014A****PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

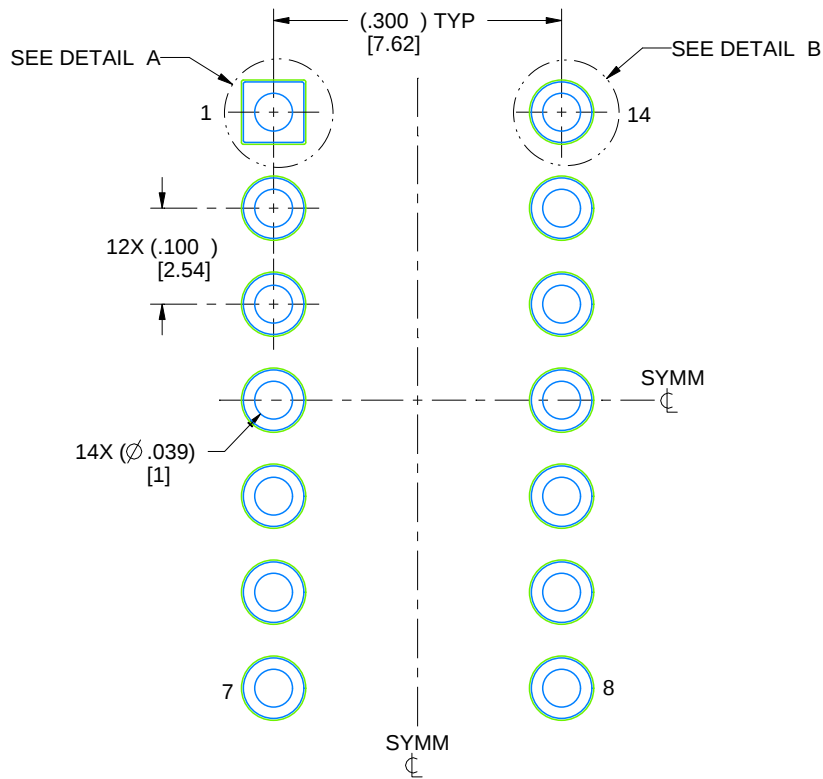
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

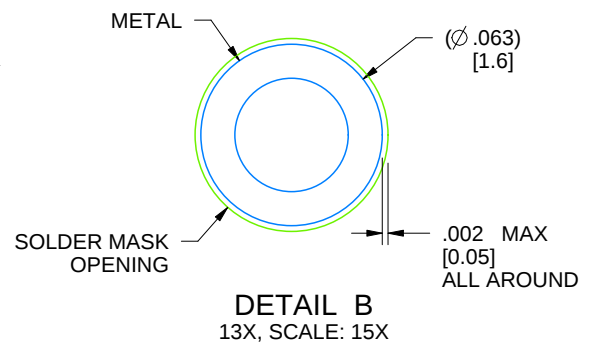
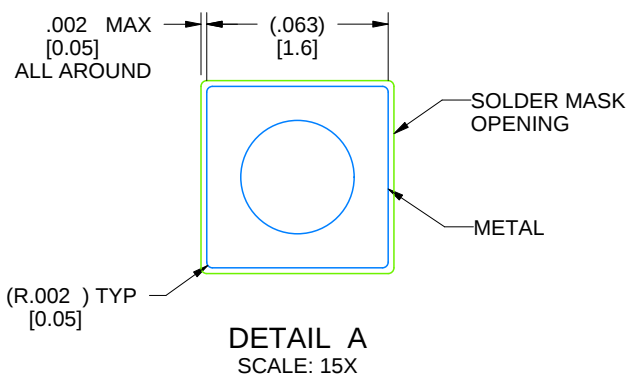
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



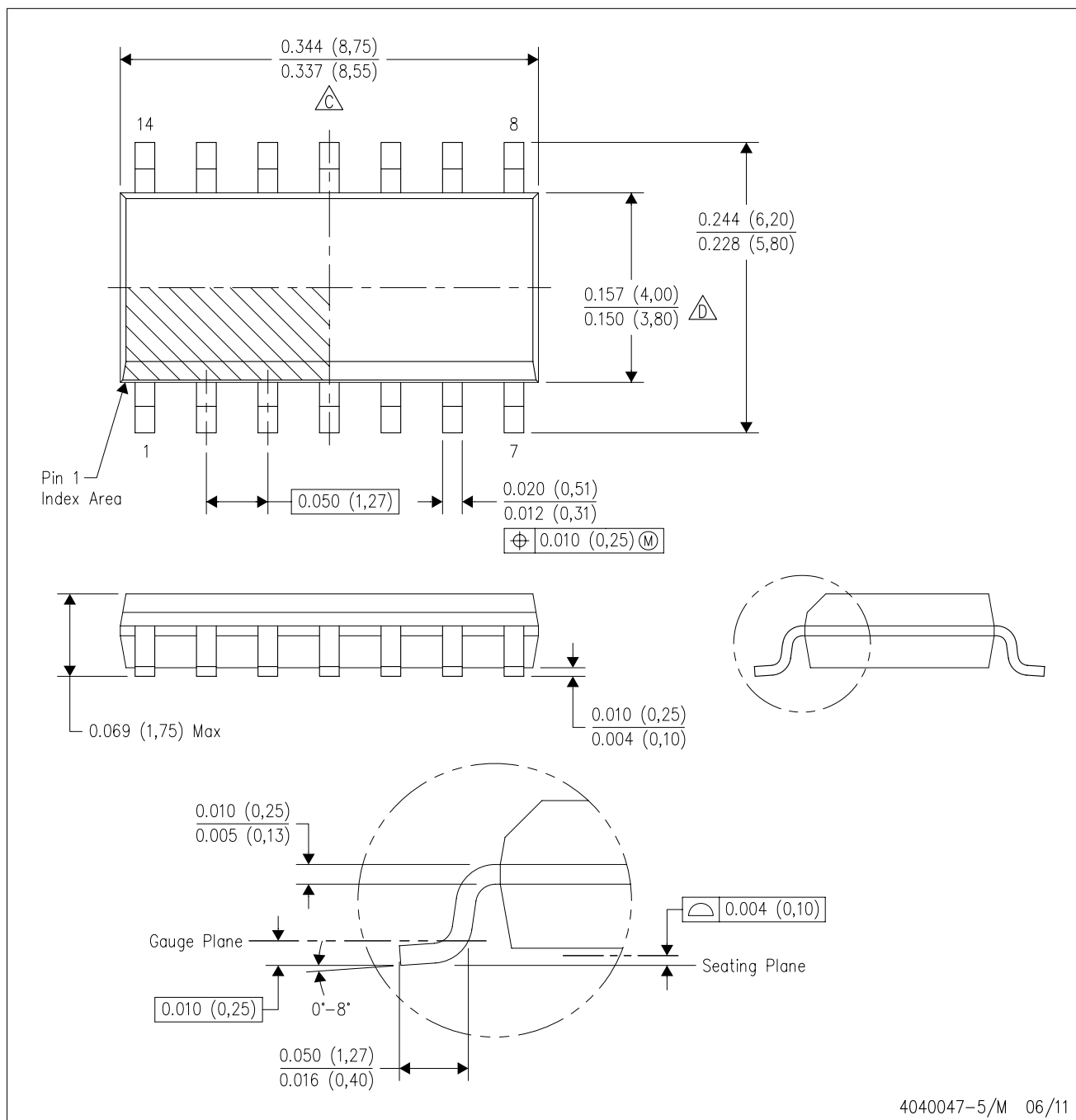
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

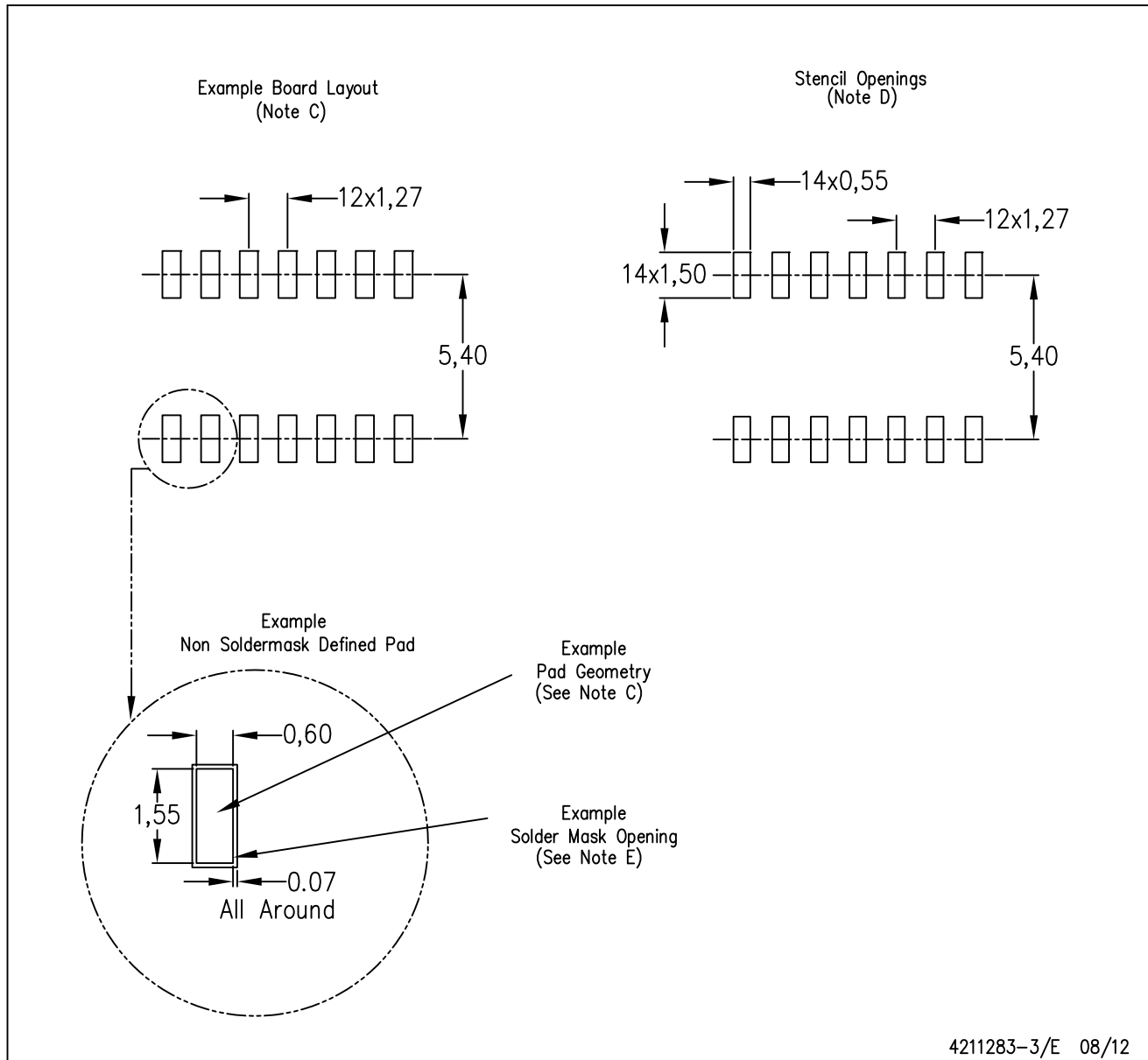


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

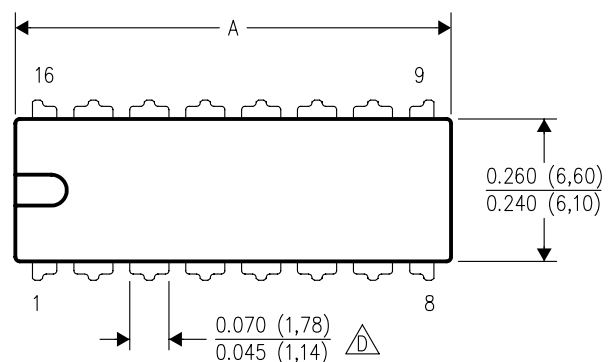


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

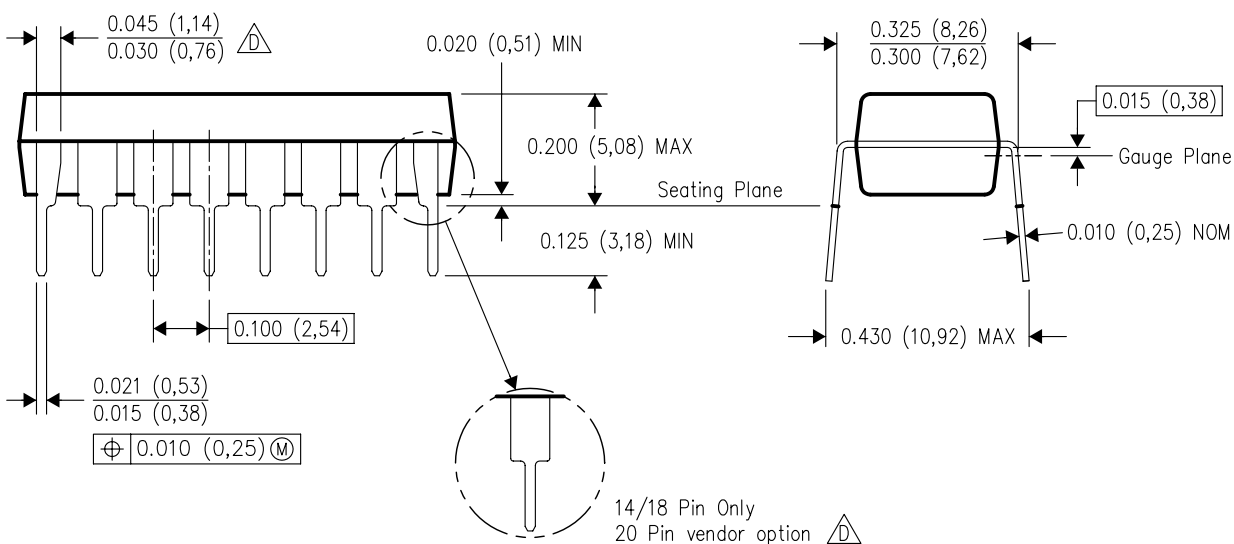
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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