

AN10580

GreenChip TEA1761 synchronous rectification and feedback controller

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Application note

Document information

Info	Content
Keywords	GreenChip SR, TEA1761, Synchronous rectification, high efficiency, flyback, voltage regulation
Abstract	The TEA1761 is a member of the new generation of synchronous rectifier controller ICs for switched mode power supplies. Its high level of integration allows the design of a cost effective power supply with a very low number of external components. The TEA1761 is a controller IC dedicated for synchronous rectification on the secondary side of discontinuous conduction mode and quasi-resonant flyback converters. Besides electronics for synchronous rectification, circuitry for output voltage and output current regulation is integrated. The TEA1761 is fabricated in a Silicon On Insulator (SOI) process. This NXP SOI process makes a wide voltage range possible.

Revision history

Rev	Date	Description
Rev. 01	20080319	First edition

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1. Introduction

The TEA1761 is a controller for synchronous rectification, to be used in quasi-resonant and discontinuous conduction mode flyback converters. Besides control of the SR MOSFET, the TEA1761 contains the voltage reference and amplifiers to regulate and control the output voltage and output current of the power supply.

2. Application schematic TEA1761

[Figure 1](#) shows a typical synchronous rectification application using the TEA1761.

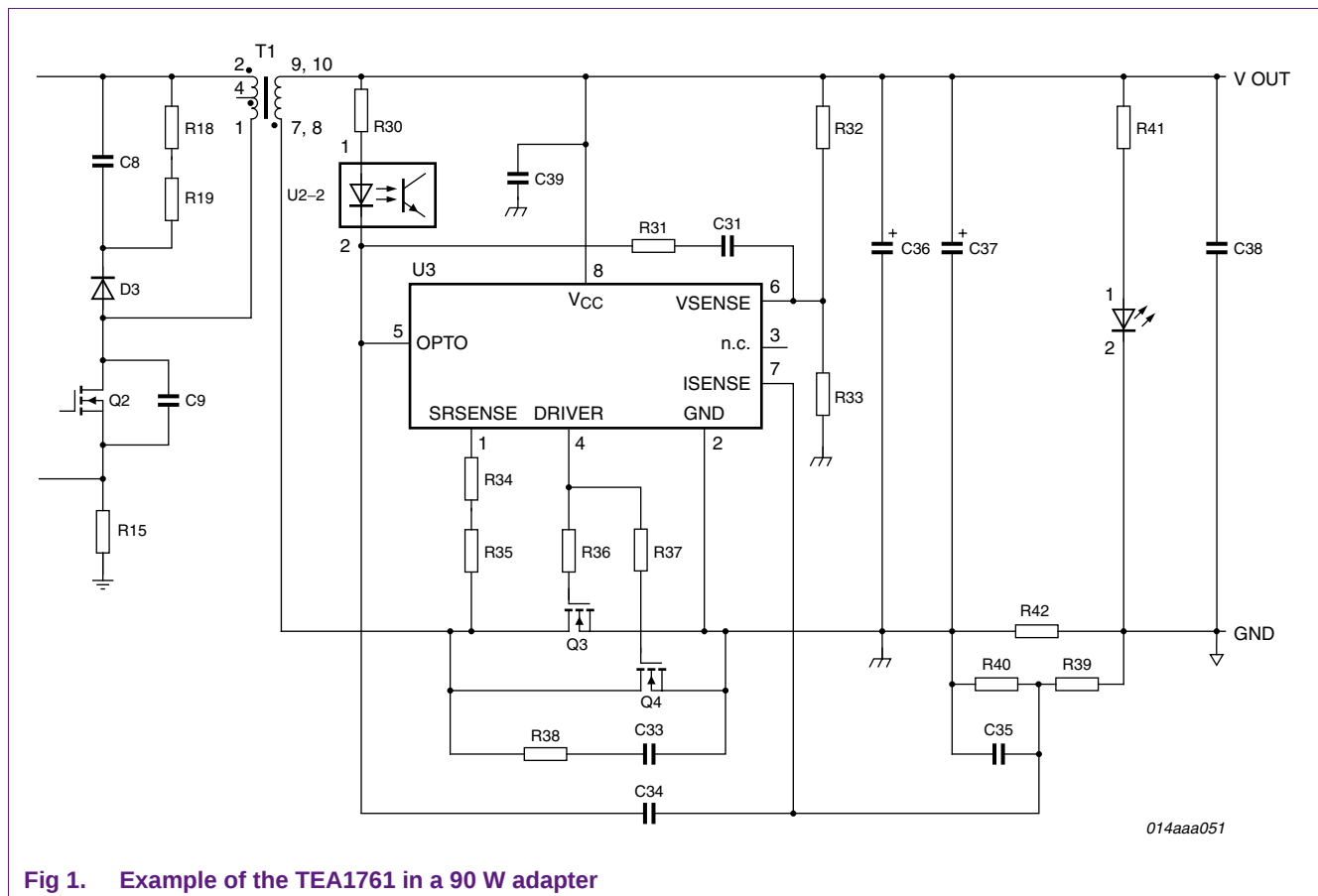


Fig 1. Example of the TEA1761 in a 90 W adapter

See [Table 1](#) in [Section 6.2](#) for the component values, which are relevant to the application's behavior.

3. Functional description and application

3.1 SR control

The TEA1761 uses the SRSENSE pin as an input to control the MOSFETs.

There is no adjustment necessary for the SR control.

The SR MOSFET is switched on when the voltage at the SRSENSE pin is lower than –310 mV.

When the voltage at the SRSENSE pin reaches –55 mV ($I_D \times R_{DS(on)}$), the driver decreases and regulates the gate voltage of the MOSFET in order to maintain the –55 mV at the SRSENSE pin.

When the voltage at the SRSENSE pin rises above –12 mV (typical), the SR MOSFET is switched off.

The synchronous rectification remains active in standby-mode, as long as the secondary stroke is less than 2 μ s (typical). The driver of the TEA1761 has been designed such that there is no additional power consumption in standby with the MOSFET active.

For the best performance it is advisable to connect the SRSENSE pin as close as possible to the drain of the MOSFETs. Also see [Section 6.1](#).

It is not necessary to place a resistor between the driver output and the MOSFET gate. If such a series resistor is required, e.g. for reasons of reducing switching noise, then it must be checked if the SR MOSFET is kept off under all circumstances, especially at high temperature of the SR MOSFET. At switch-on of the primary side MOSFET, the voltage at the drain of the SR MOSFET goes up with a high $\Delta V/\Delta t$. The steep $\Delta V/\Delta t$ causes a current flow through the C_{dg} capacitor, from gate to drain. This current increases the gate voltage of the MOSFET. If this rises above the threshold voltage, $V_{th(en)}$, the SR MOSFET is switched on. This should be prevented.

3.2 Function of resistors in series with pin SRSENSE

In the TEA1761 there is an ESD protection at every pin for handling during production. Because this ESD protection can still be triggered by an ESD event or test during normal operation, additional protection by a resistive path is recommended.

If the ESD protection circuit is activated by an external ESD event in the application, then there will be a short circuit between the SRSENSE pin and GND pin. In this event the IC could be damaged.

The function of the resistors (R34 and R35 in [Figure 1](#)) is to limit the current in the SRSENSE pin if the ESD protection is triggered. A total resistance value of 1 k Ω is sufficient to protect pin SRSENSE. Because of the peak power rating, two SMD 1206 resistors are used.

3.3 Output voltage regulation

The application of the voltage feedback circuit is similar to well known circuits using a TL431 or TSM103. The internal reference voltage is 2.5 V, accuracy within 1 %. A voltage divider (R32 and R33 in [Figure 1](#)) is used to set the output voltage of the application. The output voltage can be calculated with the equation:

$$V_o = 2.5V \times \frac{R_{32} + R_{33}}{R_{33}}$$

Or when V_o and R32 are known, for example $V_o = 19.5$ V and $R_{32} = 35.7$ k Ω , then

$$R_{33} = \frac{R_{32} \times V_{ref}}{(V_o - V_{ref})} = \frac{35.7k\Omega \times 2.5V}{(19.5V - 2.5V)} = 5.25k\Omega \Rightarrow 5.23k\Omega(1\%)$$

The phase and gain margin of the system can be set with a feedback network between the OPTO output and the VSENSE pin (R31 and C31 in [Figure 1](#)).

3.4 Output current limit

The output current of the application can be limited by sensing the voltage across a current-sense resistor (R42 in [Figure 2](#)). The internal reference voltage of the current-sense circuit is 50 mV. Therefore the voltage drop across the current-sense resistor must be more than 50 mV. The resistor divider (R39 and R40 in [Figure 1](#) and [Figure 2](#)) is used to adjust the actual output-current limit and to act as an RC filter in combination with C35.

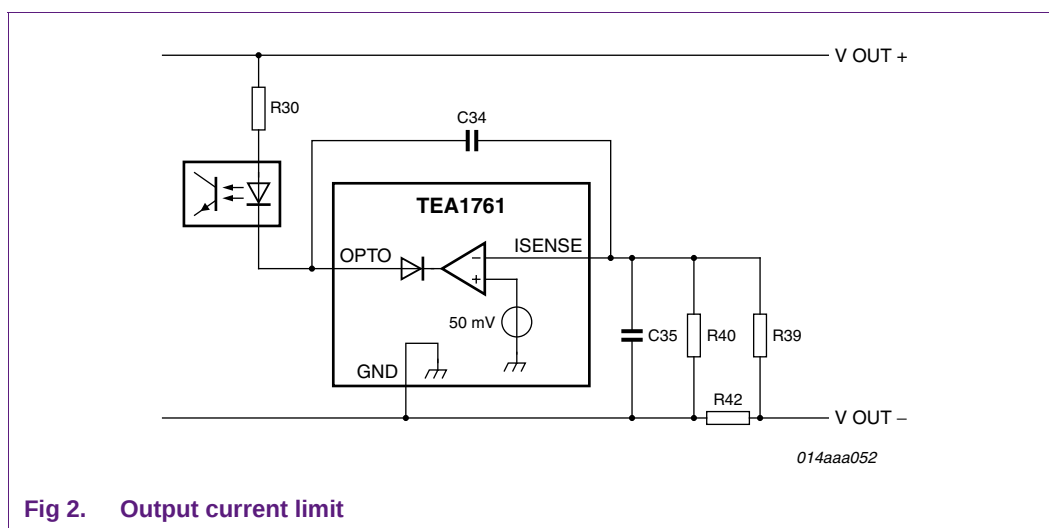


Fig 2. Output current limit

With the TEA1761 both signals for the voltage feedback and the current feedback are transferred through one OPTO coupler to the primary side of the application. When an output overcurrent occurs, the flyback controller at the primary side should limit the output power. A commonly used method is to do this by triggering the UnderVoltage Lock Out (UVLO) of the flyback controller.

To trigger the UVLO, three conditions must be met:

1. The tracking of the supply voltage (V_{CC}) of the flyback controller must be coupled very closely to the output voltage. This requires a well designed transformer with a low leakage inductance and a well designed peak clamp.
2. The output power must be decreased gradually to enable tracking of the flyback V_{CC} with the output voltage. To achieve this, the time constant of $R40 \times C35$ should be approximately 100 ms.
3. The number of turns on the primary side of the auxiliary winding must be kept as low as possible. This is necessary to trigger the UVLO of the flyback controller before the UVLO of the TEA1761 is reached.

The value of C34 should be chosen such that the output current limit operates correctly at different overload levels between the TEA1761 setting point and a real short circuit. Bouncing of the TEA1761 OPTO output should be prevented, as long as the flyback is switching. In practice, values between 470 pF and 22 nF have proven to give a good result in different applications.

For setting the required current limit, the following procedures can be used.

3.4.1 Adjusting the current limit in combination with the GreenChip II and other brands

1. Disable the ISENSE circuit of the TEA1761, by connecting pin ISENSE to ground.
2. Adjust the flyback current-sense resistor such that the adapter can deliver 130 % to 140 % of the nominal output current at a low mains voltage.
3. Adjust the OPP resistor (TEA1552, TEA1654 or TEA1533), or external OPP network (TEA1532) such that the adapter can deliver 130 % to 140 % of the nominal output current at a high mains voltage.
4. Enable the TEA1761 ISENSE circuit and adjust the voltage divider (R39 and R40 in [Figure 1](#)) such that the output current is limited to 120 % of the nominal output current. Some adjustment of the value of C35 may be necessary.
5. Adjust C34 such that there is no bouncing of the TEA1761 OPTO output during switching of the flyback.

3.4.2 Adjusting the current limit in combination with the GreenChip III TEA1750

1. Adjust the time-out circuit at the FBCTRL pin.
2. Disable the ISENSE circuit of the TEA1761, by connecting pin ISENSE to ground.
3. Adjust the flyback current-sense resistor such that the adapter can deliver 130 % to 140 % of the nominal output current at a low mains voltage.
4. Enable the TEA1761 ISENSE circuit and adjust the voltage divider (R39 and R40 in [Figure 1](#)) such that the output current is limited to 120 % of the nominal output current. Some tuning of the value of C35 could be necessary.
5. Adjust C34 such that there is no bouncing of the TEA1761 OPTO output during switching of the flyback.

3.5 OPTO output

The functions of the voltage feedback and the current feedback are combined to one open-drain OPTO output. It is possible to make two separate feedback circuits from this single output, one to pin VSENSE (R31 and C31 in [Figure 1](#)) and one to pin ISENSE (C34 in [Figure 1](#)).

3.6 V_{CC}

V_{startup} is typically 8.6 V and V_{CC(UVLO)} is typically 8.1 V. If necessary, a capacitor C39 can be placed between pin V_{CC} and pin GND to stabilize the supply voltage and to limit the noise at the IC ground track.

3.7 Driver output

Between 0 V and UVLO, an active current sink circuit keeps the external MOSFET(s) in an off-state.

3.8 Internal OverTemperature Protection (OTP)

The TEA1761 has an internal OverTemperature Protection at 150 °C. The IC will maximize the OPTO sink current at the moment the OTP level has been reached. This will limit (or shut down) the output power of the primary side controller.

4. Application examples

4.1 Using the TEA1761 with a 3.3 V or 5 V output

The TEA1761 has a start level of 8.6 V (typical). An extra secondary winding must be used to supply the IC when using the TEA1761 for a 3.3 V or 5 V output.

[Figure 3](#) gives the configuration of such a circuit.

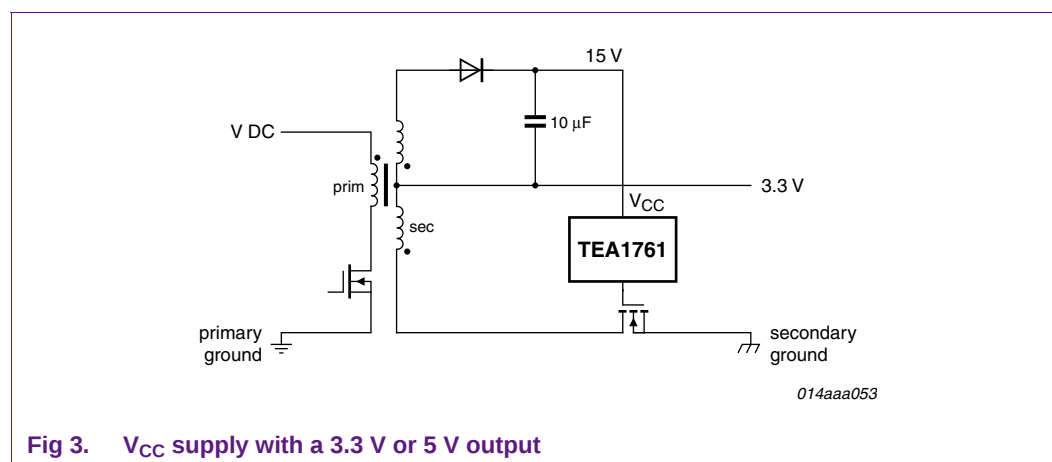


Fig 3. V_{CC} supply with a 3.3 V or 5 V output

In some cases, where the nominal output voltage is close to V_{startup} , the extra supply winding could be necessary for proper output current limiting behavior.

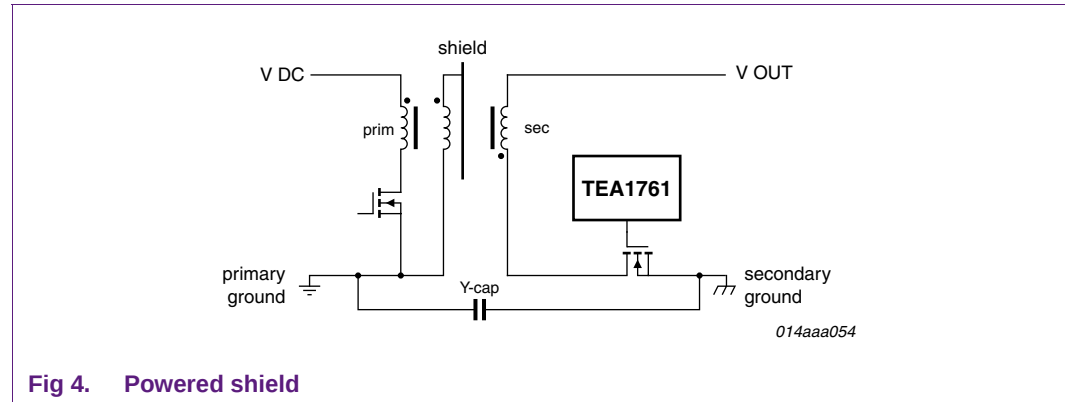
5. Meeting EMC requirements

In some applications, it can be more difficult to meet the CISPR 22 requirements with the synchronous rectification compared to a solution with Schottky diodes. This is caused by the placing of the SR MOSFETs in the secondary ground path instead of the “normal” placing of the Schottky diode in the positive voltage path. This problem is typical for this topology. There are two ways to solve this problem without increasing the common mode filtering.

5.1 The powered shield

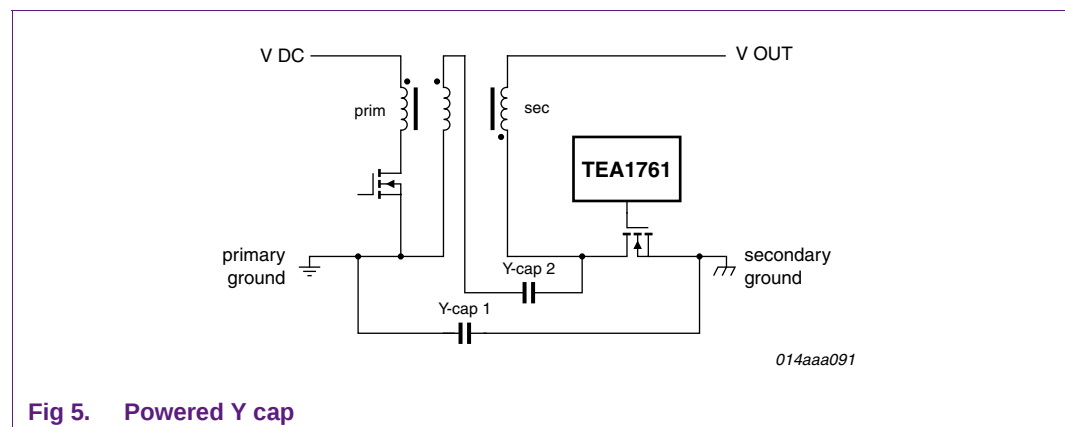
[Figure 4](#) shows the powered shield. In most transformer designs, the shielding between the primary and secondary windings is already present. All the present shields must be connected to an extra winding at the primary side. This winding injects a current into the

shielding. The phase of the injected current is opposite to the phase of the common mode current through the flyback transformer and will reduce the common mode current through the input and output cables by compensation. The exact number of turns of the shield winding should be determined experimentally. With the powered shield a significant reduction of the Y-cap value and thus leakage current is possible. In some cases the Y-capacitor even can be omitted.



5.2 The powered Y-cap

[Figure 5](#) shows the powered Y-cap which is an alternative to the powered shield solution. This solution needs an additional winding on the transformer and sometimes it also requires an additional Y-cap, to meet the ESD surge and fast transient tests. The extra winding at the primary side, injects current through a Y-cap into the secondary ground. The phase of the injected current is opposite to the phase of the common mode current through the flyback transformer and this will, by compensation, reduce the common mode current through the input and output cables. The exact required number of turns in the extra winding and the Y-cap value should be determined experimentally. Eight winding turns and a Y-cap with a value of 100 pF would be recommended as a good starting point.



6. Appendix

6.1 Layout considerations

The IC ground copper track should be as wide and as low ohmic as possible. The IC ground is used as a reference for the circuits, but also has to conduct the high current of the driver and the currents through the MOSFET C_{dg} .

The IC ground is used as a reference for the voltage and current regulation and for the control of the SR MOSFET. Therefore a compromise has to be made with respect to the connection of the IC ground to the surrounding circuits. It is advisable to connect the IC ground to the output electrolytic capacitor closest to the MOSFET source.

The SRSENSE pin must be connected as close as possible to the MOSFET drain pin to guarantee a proper detection of the MOSFET V_{DS} and thus control of the SR MOSFETs. It is advisable to reserve a separate copper track in the PCB layout for this function.

6.2 Bill of materials

Table 1. Bill of materials

Relevant component values for a 19.5 V / 4.62 A application with the TEA1761.

Description	Position
Resistor, SMD 0603 Thin Film Chip, 1 k Ω , 5 %	R30
Resistor, SMD 0603 Thin Film Chip, 10 k Ω , 5 %	R31, R39
Resistor, SMD 0603 Thin Film Chip, 35.7 k Ω , 1 %	R32
Resistor, SMD 0603 Thin Film Chip, 5.23 k Ω , 1 %	R33
Resistor, SMD 1206 Thin Film Chip, 560 Ω , 5 %	R34, R35
Resistor, SMD 0805 Thin Film Chip, 47 Ω , 5 %	R36, R37
Resistor, SMD 0603 Thin Film Chip, 51 k Ω , 5 %	R40
Resistor, Mu-Cu Wire, 10 m Ω , 1 %	R42
MLCC, SMD 0805, 1 μ F/50 V, Y5V	C39
MLCC, SMD 0805, 0.01 μ F/50 V, X7R	C31
MLCC, SMD 0805, 470 pF/50 V, X7R	C34
MLCC, SMD 0805, 2.2 μ F/10 V, X7R	C35

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