100dB, 24-Bit, 192 kHz Stereo Audio CODEC

GENERAL DESCRIPTION

ES7322 is a low cost high performance stereo audio CODEC. ES7322 performs stereo digital to analog conversion and analog to digital conversion continuously from 8 kHz to 200 kHz sampling frequency. ES7322 is ideal for high performance cost sensitive consumer audio applications.

ES7322 can accept I²S, left justified and right justified serial audio data formats up to 24-bit word length. ADC and DAC operate on independent sampling frequencies and clocks. The device uses advanced multi-bit delta-sigma modulation technique to convert data between digital and analog. The multi-bit delta-sigma modulators make the device with low sensitivity to clock jitter and low out of band noise.

ES7322 can operate either in the hardware mod or the software mode. In the hardware mode, pin M0, M1, M2 and M3 set the operation of the device. In the software mode, ES7322 provides SPI or 2-wire micro-controller interfaces to configure its operations.

APPLICATIONS

- DVD recorder
- Personal video recorder
- LCD and digital TVs
- Car audio
- AV receiver

FEATURES

ADC and DAC:

- 100 dB dynamic range
- –90 dB THD
- 8 kHz to 200 kHz sampling frequency
- I^2S, left justified and right justified audio data format, 16-24 bits
- 128, 192, 256, 384, 512, 768 and 1024 MCLK to LRCK ratios
- Independent ADC and DAC sampling frequencies and clocks
- Advanced multi-bit delta-sigma with low sensitivity to clock jitter
- Single power supply from 3V to 5.5V
- Hardware mode or SPI or 2-wire uC interface

ADC:

- 4-to-1 mux for analog inputs
- Direct 2 Vrms analog input
- ADC PGA from 11.5 dB to –11.5 dB in 0.5 dB per step
- Digital attenuation from 6.5 dB to 89.5 dB in 0.5 dB per step
- Optional high pass filter to remove analog DC offset

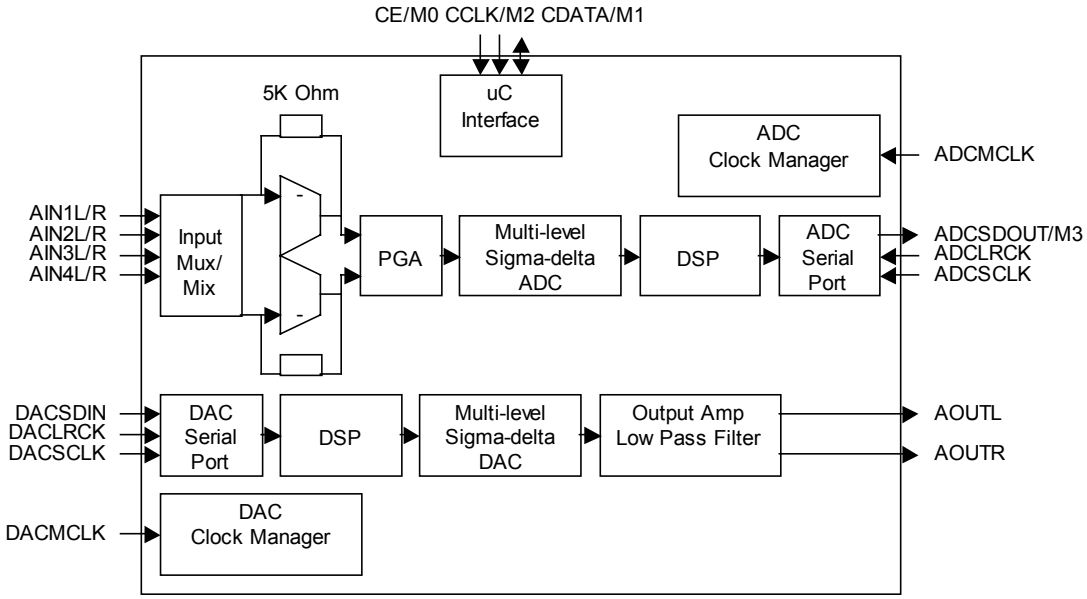
DAC:

- Digital volume control from 0 dB to 120 dB attenuation in 0.5 dB per step, with soft ramp and zero crossing transition
- De-emphasis filter for 32, 44.1 and 48 kHz sampling frequencies
- Selectable fast and slow roll-off filters

ORDERING INFORMATION

ES7322 -40°C ~ +85°C
SSOP-28, SOP-28

1 BLOCK DIAGRAM



2 PIN DESCRIPTIONS

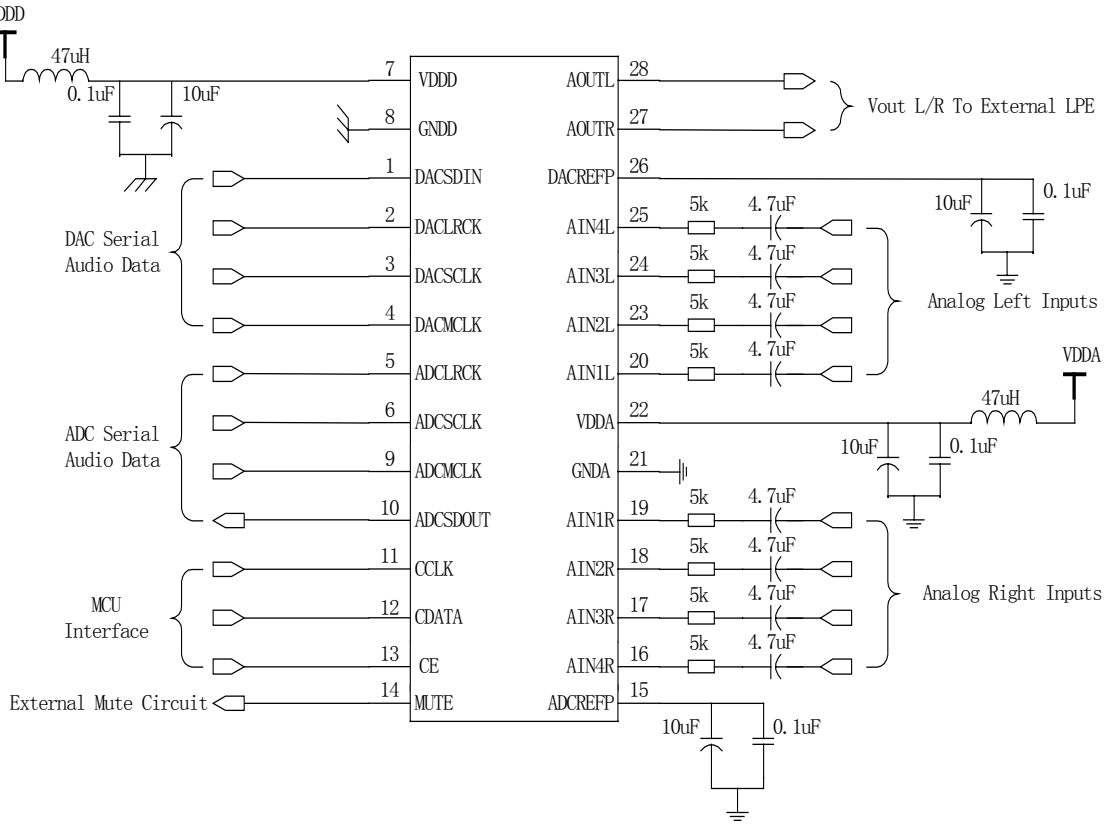
DACSDIN	1	28	AOUTL
DACLRCK	2	27	AOUTR
DACSCLK	3	26	DACREFP
DACMCLK	4	25	AIN4L
ADCLRCK	5	24	AIN3L
ADCSCLK	6	23	AIN2L
VDDD	7	22	VDDA
GNDD	8	21	GNDA
ADCMCLK	9	20	AIN1L
ADCSDOUT/M3	10	19	AIN1R
CCLK/M2	11	18	AIN2R
CDATA/M1	12	17	AIN3R
CE/M0	13	16	AIN4R
MUTE	14	15	ADCREFP

Pin	Pin Number	Input or Output	Pin Description
ADC Pin			
AIN1L/R	20, 19	I	Analog input 1 left and right channels
AIN2L/R	23, 18	I	Analog input 2 left and right channels
AIN3L/R	24, 17	I	Analog input 3 left and right channels
AIN4L/R	25, 16	I	Analog input 4 left and right channels
ADCMCLK	9	I	ADC master clock
ADCSDOUT/M3	10	O	ADC PCM serial data output
ADCLRCK	5	I	ADC PCM serial data left and right channel frame clock
ADCSCLK	6	I	ADC PCM serial data bit clock
DAC Pin			
DACMCLK	4	I	DAC master clock
DACSDIN	1	I	DAC PCM serial data input
DACLRCK	2	I	DAC PCM serial data left and right channel frame clock
DACSCLK	3	I	DAC PCM serial data bit clock
AOUTL/R	28, 27	O	DAC analog output left and right channels
MUTE	14	O	Mute pin, active when detect 8K zero input in both left and right channels or users choose to mute the DAC
Micro-controller Pin or Hardware Mode Pin			
CE/M0	13	I	SPI uC interface chip select or 2-wire AD0
CCLK/M2	11	I	SPI or 2-wire (I2C compatible) uC interface clock
CDATA/M1	12	SPI: I 2-wire: I or O	SPI or 2-wire (I2C compatible) uC interface data
Power and Filtering Pin			
VDDD/GNDD	7, 8		Digital power supply
VDDA/GNDA	22, 21		Analog power supply
ADCREFP/DACREFP	15, 26		Analog filtering pins

In the hardware mode, the mode pins function as the following:

Pin	Pin Number	Input or Output	Pin Description
M3	10	O	External pullup (47k resistor) – ADC and DAC I^2S serial data format External pulldown (47k resistor) – ADC and DAC LJ serial data format
M2	11	I	0 – no deemphasis 1 – 44.1 kHz deemphasis filter on
M1:M0	12, 13	I	00 – select AIN1 01 – select AIN2 10 – select AIN3 11 – select AIN4

3 RECOMMENDED APPLICATION CIRCUIT



4 AUDIO DATA SAMPLING FREQUENCY AND CLOCKS

According to the input serial audio data sampling frequency, the device can work in three speed modes: single speed, double speed or quad speed modes. The ranges of the sampling frequency in these three modes are listed in Table1. ADCSampleRate bits in ADC Control 2 register (RAM address 0x02) or DACSampleRate bits in DAC Control 2 register (RAM address 0x07) set the speed mode. By default, the device can detect the speed mode automatically when sampling rate falls within the Fs Auto Detection Ranges listed in Table1. In this auto detection mode, sampling frequency outside the specified ranges is not supported. ADC and DAC have separate auto detection so ADC and DAC sampling frequencies can be completely independent.

Table 1 Sampling Frequency and MCLK/LRCK Ratio

Speed Mode	Sampling Frequency	Fs Auto Detection Range	MCLK/LRCK Ratio
Single Speed	8kHz – 50kHz	8kHz – 50kHz	256, 384, 512, 768, 1024
Double Speed	50kHz – 100kHz	84kHz – 100kHz	128, 192, 256, 384, 512
Quad Speed	100kHz – 200kHz	167kHz – 200kHz	128, 192, 256

The device uses separate master clocks, LRCK clocks and SCLK clocks for

the ADC and DAC. The allowed MCLK/LRCK ratios in each speed mode are also listed in Table1. The device always detects MCLK/LRCK ratio automatically.

5 HARDWARE MODE

The device can operate in the hardware mode or the software mode. The default is the hardware mode. To change the hardware mode to the software mode, set SCPEn bit of Chip Control register (RAM address 0x00) to 1.

In the hardware mode, pin M3 sets I^2S or left justified ADC and DAC serial port mode, pin M2 sets DAC de-emphasis filter on or off, and pins M1 and pin M0 select one of the four ADC analog inputs.

Please refer to PIN DESCRIPTIONS section for detail settings.

6 POWER UP AND DOWN

The chip internal power on reset will reset the device when VDDD ramps from ground to supply voltage level. When VDDD and VDDA are present to the device, applying ADCMCLK and ADCLRCK will startup the ADC and applying DACMCLK and DACLRCK will start up the DAC.

During the DAC startup, DAC analog outputs ramp gradually from ground to mid level to minimize audible pop noise. This gradual ramp feature can be turned off by setting ClickFree bit of DAC Control 1 register (RAM address 0x06) to 0.

ADC and DAC can power up or down independently. In the software mode, ADC or DAC can power down through ADCPDN bit or DACPDN bit of Chip Control register (RAM address 0x00). In the hardware mode, ADC can power down by stopping ADCMCLK or ADCLRCK, and DAC can power down by stopping DACMCLK or DACLRCK.

7 MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard SPI and 2-wire micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers. Please see section 8 for the details of configuration register definition.

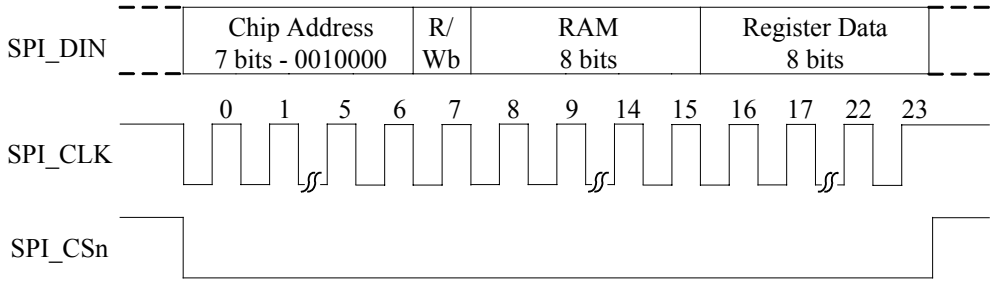
The identical device pins are used to configure either SPI or 2-wire interface. In SPI mode, pin CE, CCLK and CDATA function as SPI_CSn, SPI_CLK and SPI_DIN. In 2-wire mode, pin CE, CCLK and CDATA function as AD0, SCL and SDA. To select SPI mode, apply high to low transition signal to CE pin. Otherwise the device will operate in 2-wire interface mode.

7.1 SPI

ES7322 has a SPI (Serial Peripheral Interface) compliant synchronous serial slave controller inside the chip. It provides the ability to allow the external master SPI controller to access the internal registers, and thus control the operations of chip.

All lines on the SPI bus are unidirectional: The SPI_CLK is generated by the master controller and is primarily used to synchronize data transfer, the SPI_DIN line carries data from the master to the slave; SPI_CSn is generated by the master to select ES7322.

The timing diagram of this interface is given in Figure 1. The high to low transition at SPI_CSn pin indicates the SPI interface selected. Each write procedure contains 3 words, i.e. Chip Address plus R/W bit, internal register address and internal register data. Every word length is fixed at 8 bits. The input SPI_DIN data are sampled at the rising edge of SPI_CLK clock. The MSB bit in each word is transferred firstly. The transfer rate can be up to 10M bps.



RAM = Register Address Mapping

Figure 1 SPI Configuration Interface Timing Diagram

7.2 2-wire

2-wire interface is a bi-directional serial bus that uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. The timing diagram for data transfer of this interface is given in Figure 2. Data are transmitted synchronously to SCL clock on the SDA line on a byte-by-byte basis. Each bit in a byte is sampled during SCL high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the SDA low. The transfer rate of this interface can be up to 100k bps.

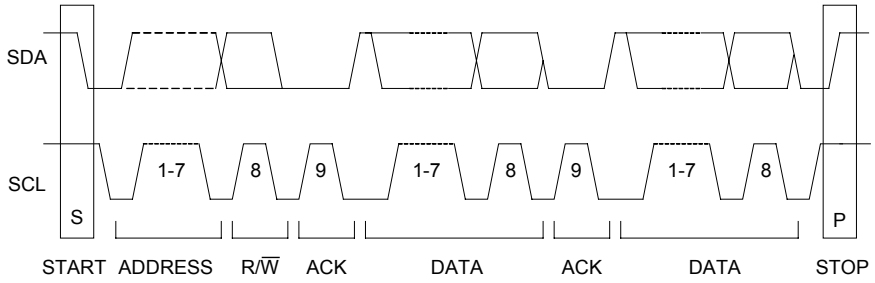


Figure 2 Complete Data Transfer for 2-wire Interface

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCL is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 001000x,where x equals AD0 (pin CE). The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCL is high.

In 2-wire interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 2 and Table 3. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register. There are no acknowledge bit after data to be written or read, this is the only difference from the I^2C protocol.

Table 2 Write Data to Register in 2-wire Interface Mode

Chip Address		R/W		Register Address		Data to be written
001000	AD0	0	ACK	RAM	ACK	DATA

Table 3 Read Data from Register in 2-wire Interface Mode

Chip Address		R/W		Register Address
001000	AD0	0	ACK	RAM
Chip Address		R/W		Data to be read
001000	AD0	1	ACK	DATA

8 CONFIGURATION REGISTER DEFINITION

SPI and 2-wire configuration interface share the same registers because there is only one interface active at any time. There are total of 11 user programmable 8-bit registers in this device. These registers control the operations of ADC and DAC. External master controller can access these

registers by using the slave address specified in RAM (Register Address Map) register as shown in the Table 2.

Table 2 Bit Content of Register Address Map

Bit Name	Bit	Description
RAM Address	7:0	The address of the register to be accessed: 0x00 – Chip Control (default) 0x01 – ADC Control 1 0x02 – ADC Control 2 0x03 – ADC Mute Control 0x04 – ADC Left Gain Control 0x05 – ADC Right Gain Control 0x06 – DAC Control 1 0x07 – DAC Control 2 0x08 – DAC Mute Control 0x09 – DAC Left Volume Control 0x0a – DAC Right Volume Control

8.1 Chip Control – 0x00

Bit Name	Bit	Description
SCPEn	7	0 – hardware mode (default) 1 – software (control port) mode
Reserved	6:5	Reserved
ADCPDN	4	0 – normal (default) 1 – ADC low power mode
Reserved	3	Reserved
DACPDN	2	0 – normal (default) 1 – DAC low power mode
Reserved	1:0	Reserved

8.2 ADC Control 1 – 0x01

Bit Name	Bit	Description
Reserved	7	Reserved
AINMIX	6:3	0000 – AIN1 input to ADC (default) xxx1 – AIN1 input ADC xx1x – AIN2 input ADC x1xx – AIN3 input ADC 1xxx – AIN4 input ADC
HPF	2	0 – ADC HPF enable (default) 1 – ADC HPF disable
Reserved	1:0	Reserved

8.3 ADC Control 2 – 0x02

Bit Name	Bit	Description
ADCSampleRate	7:6	00 – ADC speed mode auto detect (default) 01 –single speed mode 10 –double speed mode 11 –quad speed mode
ADCSPDataMode	5:3	000 – Left justified, up to 24 bit data 001 – I^2S, up to 24 bit data (default) 010 – Right justified, 16 bit data 011 – Reserved 100 – Reserved 101 – Right justified, 24 bit data 110 – Reserved 111 – Reserved
SCLKRatio	2:1	00 – 32 01 – 48 10 – 64 (default) 11 – 128
Reserved	0	Reserved

8.4 ADC Mute Control – 0x03

Bit Name	Bit	Description
ADCMute	7	0 – normal (default) 1 – mute ADC digital output
Reserved	6	Reserved
ADCRampRate	5:4	These bits define ADC gain control ramp rate: 00 – 0.5 dB per 4 LRCK (default) 01 – 0.5 dB per 8 LRCK 10 – 0.5 dB per 16 LRCK 11 – 0.5 dB per 32 LRCK
ADCL=R	3	0 – normal (default) 1 – both channel gain control is set by ADC Left Gain Control register
ADCSoftRamp	2	ADC soft ramp at mute or gain change: 0 – Disabled 1 – Enabled (default)
ADCZeroCrs	1	ADC mute or gain change at zero crossing signal level to minimize audible noise 0 – Disabled 1 – Enabled (default)
Reserved	0	Reserved

8.5 ADC Left Gain Control – 0x04

Bit Name	Bit	Description
ADCGainL	7:0	1110 1000 – 6.0 dB gain (PGA) 1110 1001 – 6.5 dB gain (PGA) 1110 1010 – 7.0 dB gain (PGA) 1110 1011 – 7.5 dB gain (PGA) 1110 1100 – 8.0 dB gain (PGA) 1110 1101 – 8.5 dB gain (PGA) 1110 1110 – 9.0 dB gain (PGA) 1110 1111 – 9.5 dB gain (PGA) 1111 0000 – 10.0 dB gain (PGA) 1111 0001 – 10.5 dB gain (PGA) 1111 0010 – 11.0 dB gain (PGA) 1111 0011 – 11.5 dB gain (PGA) 1111 0100 – 6.0 dB attenuation (PGA) 1111 0101 – 5.5 dB attenuation (PGA) 1111 0110 – 5.0 dB attenuation (PGA) 1111 0111 – 4.5 dB attenuation (PGA) 1111 1000 – 4.0 dB attenuation (PGA) 1111 1001 – 3.5 dB attenuation (PGA) 1111 1010 – 3.0 dB attenuation (PGA) 1111 1011 – 2.5 dB attenuation (PGA) 1111 1100 – 2.0 dB attenuation (PGA) 1111 1101 – 1.5 dB attenuation (PGA) 1111 1110 – 1.0 dB attenuation (PGA) 1111 1111 – 0.5 dB attenuation (PGA) **0000 0000 – no gain or attenuation (default)** 0000 0001 – 0.5 dB gain (PGA) 0000 0010 – 1.0 dB gain (PGA) 0000 0011 – 1.5 dB gain (PGA) 0000 0100 – 2.0 dB gain (PGA) 0000 0101 – 2.5 dB gain (PGA) 0000 0110 – 3.0 dB gain (PGA) 0000 0111 – 3.5 dB gain (PGA) 0000 1000 – 4.0 dB gain (PGA) 0000 1001 – 4.5 dB gain (PGA) 0000 1010 – 5.0 dB gain (PGA) 0000 1011 – 5.5 dB gain (PGA) 0000 1100 – 6.0 dB gain (PGA) 0000 1101 – 11.5 dB attenuation (PGA) 0000 1110 – 11.0 dB attenuation (PGA) 0000 1111 – 10.5 dB attenuation (PGA) 0001 0000 – 10.0 dB attenuation (PGA)

		0001 0001 – 9.5 dB attenuation (PGA) 0001 0010 – 9.0 dB attenuation (PGA) 0001 0011 – 8.5 dB attenuation (PGA) 0001 0100 – 8.0 dB attenuation (PGA) 0001 0101 – 7.5 dB attenuation (PGA) 0001 0110 – 7.0 dB attenuation (PGA) 0001 0111 – 6.5 dB attenuation (PGA) 0001 1000 – 6.0 dB attenuation (PGA) 0001 1001 – 6.5 dB attenuation (6 dB PGA + digital attenuation) 0001 1010 – 7.0 dB attenuation (6 dB PGA + digital attenuation) …….. 1011 1111 – 89.5 dB attenuation (6 dB PGA + digital attenuation)

8.6 ADC Right Gain Control – 0x05

Bit Name	Bit	Description
ADCGainR	7:0	Same as ADCGainL settings for ADC right channel

8.7 DAC Control 1 – 0x06

Bit Name	Bit	Description
Reserved	7:6	Reserved
ClickFree	5	0 – disable pop noise suppression power up and down 1 – enable pop noise suppression power up and down (default)
SlowFilter	4	0 – fast filter roll off (default) 1 – slow filter roll off
InvL InvR	3:2	0 – DAC analog output no phase inversion (default) 1 – DAC analog output 180 degree phase inversion
Reserved	1:0	Reserved

8.8 DAC Control 2 – 0x07

Bit Name	Bit	Description
DACSampleRate	7:6	00 – DAC speed mode auto detect (default) 01 – single speed mode 10 – double speed mode 11 – quad speed mode
DACSPDataMode	5:3	000 – Left justified, up to 24 bit data 001 – I^2S, up to 24 bit data (default) 010 – Right justified, 16 bit data 011 – Reserved 100 – Reserved 101 – Right justified, 24 bit data 110 – Reserved 111 – Reserved
DeEmphasisMode	2:1	00 – Deemphasis filter disabled (default) 01 – Deemphasis filter for Fs=32 KHz

		10 – Deemphasis filter for Fs=44.1 KHz 11 – Deemphasis filter for Fs=48 KHz
Reserved	0	Reserved

8.9 DAC Mute Control – 0x08

Bit Name	**Bit**	Description
DACMute	7	0 – unmute analog outputs for both channels (default) 1 – mute analog outputs for both channels
DACRampRate	6	These bits define volume control ramp rate: 00 – 0.5 dB per 4 LRCK (default) 01 – 0.5 dB per 8 LRCK 10 – 0.5 dB per 16 LRCK 11 – 0.5 dB per 32 LRCK
AutoMute	5	Auto mute function: long period of zero inputs (8k audio samples) will mute the analog output. Any single non-zero input will un-mute. 0 – disable 1 – enable (default)
DACL=R	4	0 – normal (default) 1 – both channel volume control is set by Left Volume Control register
DACSoftRamp	3	Soft ramp at mute and volume change: 0 – Disabled 1 – Enabled (default)
DACZeroCrs	1	Mute or volume change at zero crossing signal level to minimize audible noise 0 – Disabled 1 – Enabled (default)
Reserved	0	Reserved

8.10 DAC Left Volume Control – 0x09

Bit Name	Bit	Description
DACVolumeL	7:0	Digital volume control setting attenuates the signal in 0.5 dB incremental from 0 to –120 dB. Max setting is –120 dB. 0000 0000 – no attenuation (default) 0000 0001 – 0.5 dB attenuation 0000 0010 – 1.0 dB attenuation 0000 0011 – 1.5 dB attenuation ……..

8.11 DAC Right Volume Control – 0x0a

Bit Name	Bit	Description
DACVolumeR	7:0	Same as DACVolumeL settings for DAC right channel

9 Digital Audio Interface

The device provides three formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, SCLK and SDIN/SDOUT pins. The three formats are I^2S, left justified and right justified. In the hardware mode, the formats are selected through pin M3. In the software mode, the formats are selected by ADCSPDataMode bits of ADC Control 2 register (RAM address 0x02) or DACSPDataMode bits DAC Control 2 register (RAM address 0x07). DACSDIN is sampled by ES7322 on the rising edge of DACSCLK. ADC data is out on ADCSDOUT and changes on the falling edge of ADCSCLK. The relationship of SDATA (SDIN/SDOUT), SCLK and LRCK with the three formats is shown through Figure 3 to Figure 5.

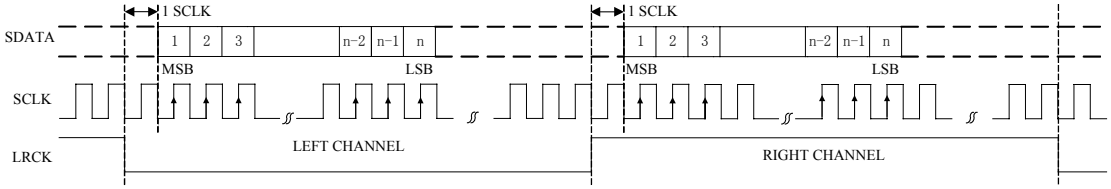


Figure 3 I2S Serial Audio Data Format Up To 24-bit

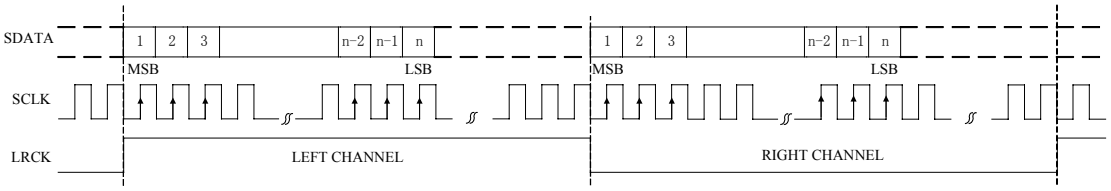


Figure 4 Left Justified Serial Audio Data Format Up To 24-bit

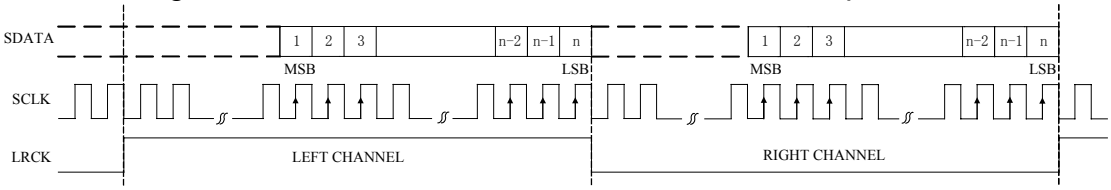


Figure 5 Right Justified Serial Audio Data Format Up To 24-bit

10 Analog Input Multiplex and Programmable Gain Control

ES7322 allows direct 2 Vrms inputs if external 5 KΩ resistors are used in serial with the analog input pins. Please refer to Figure 6. 1 Vrms inputs can directly apply to the analog input pins.

In the hardware mode, the analog input is selected through mode pins M1 and M0. In the software mode, the analog input is selected through AINMIX bits of ADC Control 1 register (RAM address 0x01). In the software mode, more than one input can apply to the analog input pins to achieve mixing effects.

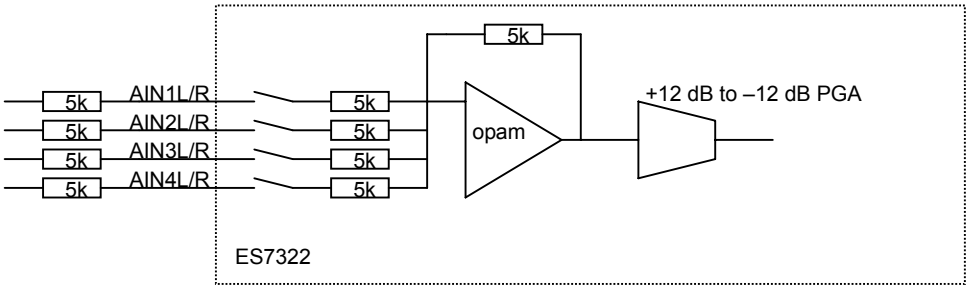


Figure 6 ADC Left and Right Inputs

The ADC has an analogue input PGA and digital gain control for each stereo channel. The analog PGA has a range of +12 dB to –12 dB gains in 0.5 dB per step. The digital gain control allows further attenuation (after the PGA) from 12.5 dB to 96 dB in 0.5 dB per step. ADC Left Gain Control register (RAM address 0x04) and ADC Right Gain Control register (RAM address 0x05) allow independent control of left and right channel gains.

Zero crossing detection and soft ramp control circuits are provided for the ADC gain control (ADC Mute Control register, RAM address 0x03). This feature minimizes the audible click and “zipper” noise as the gain values change.

11 DAC Fade In and Fade Out Transition

When DACMute bit in DAC Mute Control register (RAM address 0x08) is set, the analog outputs go to mute level (common mode voltage) gradually at the rate set by DACRampRate bits in the same register. Upon the release of the DACMute bit, the analog outputs go up gradually at the same rate set by DACRampRate bits. Please refer to Figure 7. The fade in and fade out feature can be set or disabled by DACSoftRamp bit in the same register.

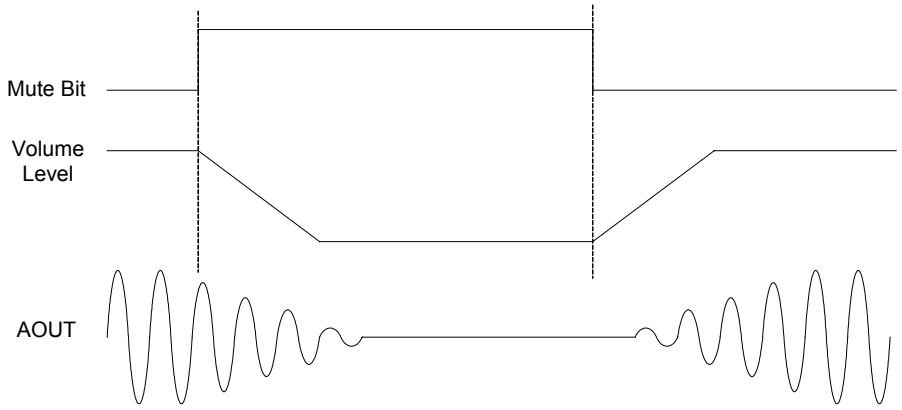


Figure 7 Fade In/Out Diagram

The fade in and fade out feature is also available when AutoMute bit in DAC Mute Control register (RAM address 0x08) is set to detect long stream of zero input data.

12 ELECTRICAL CHARACTERISTICS

12.1 Absolute Maximum Ratings

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+7.0V
Digital Supply Voltage Level	-0.3V	+7.0V
Input Voltage range	GNDD-0.3V	VDDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

12.2 Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNIT
Analog Supply Voltage Level	3.0	3.3 or 5	5.5	V
Digital Supply Voltage Level	3.0	3.3 or 5	5.5	V

12.3 ADC Analog and Filter Characteristics and Specifications

Test conditions are as the following unless otherwise specify: VDDA=+5.0V, VDDD=+5.0V, GNDA=0V, GNDD=0V, Ambient temperature=+25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Dynamic Range (Note 1)	85	95	100	dB
THD+N	-90	-86	-80	dB
Channel Separation (1KHz)	80	85	90	dB
Signal to Noise ratio	85	95	100	dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
Filter Frequency Response – Quad Speed				
Passband	0		0.2083	Fs
Stopband	0.7917			Fs

Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
Analog Input				
Full Scale Input Level (Note 2)		2*(VDDA/5)		Vrms
Input Impedance	10			KΩ

Note

1. The value is measured used A-weighted filter. If not use, the result will decrease 2-3 dB.

2. ES7322 allows direct 2 Vrms inputs if external 5 KΩ resistors are used in serial with the analog input pins. 1 Vrms inputs can directly apply to the analog input pins.

12.4 DAC Analog and Filter Characteristics and Specifications

Test conditions are as the following unless otherwise specify: VDDA=+5.0V, VDDD=+5.0V, GNDA=0V, GNDD=0V, Ambient temperature=+25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Dynamic Range (Note 1)	85	98	100	dB
THD+N	-90	-82	-75	dB
Channel Separation (1KHz)	80	85	90	dB
Signal to Noise ratio	85	97	100	dB
Interchannel Gain Mismatch		0.05		dB
Filter Frequency Response – Single Speed, Fast Roll-off Filter				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	53			dB
Filter Frequency Response – Double Speed, Fast Roll-off Filter				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	56			dB
Filter Frequency Response – Quad Speed, Fast Roll-off Filter				
Passband	0		0.2083	Fs
Stopband	0.7917			Fs
Passband Ripple			±0.006	dB
Stopband Attenuation	50			dB
Filter Frequency Response – Single Speed, Slow Roll-off Filter				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	65			dB
Filter Frequency Response – Double Speed, Slow Roll-off Filter				
Passband	0		0.2083	Fs

Stopband	0.7917			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	85			dB
Filter Frequency Response – Quad Speed, Slow Roll-off Filter				
Passband	0		0.1042	Fs
Stopband	0.8958			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	55			dB
De-emphasis Error at 1 KHz (Single Speed Mode Only)				
Fs = 32KHz Fs = 44.1KHz Fs = 48KHz			0.002 0.013 0.0009	dB
Analog Output				
Full Scale Output Level		0.7*VDDA		Vpp
Output Impedance		120		Ω
Load Resistance	2			KΩ
Load Capacitance			100	PF

Note

1. The value is measured used A-weighted filter.

12.5 DC Characteristics and Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
VDDD=VDDA=5.0V: VDDD Current VDDA Current VDDD=VDDA=3.3V: VDDD Current VDDA Current		 42 55 34 50		mA
Power Down Mode				
VDDD=VDDA=5.0V: VDDD Current VDDA Current VDDD=VDDA=3.3V: VDDD Current VDDA Current		 TBD TBD TBD TBD		mA
Digital Voltage Level				
Input High-level Voltage	2.0			V
Input Low-level Voltage			0.8	V
Output High-level Voltage		VDDD		V
Output Low-level Voltage		0		V
Mute Pin Drive Capability			3.0	mA

12.6 Serial Audio Port Switching Specifications

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			51.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz
LRCK duty cycle		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	T_{SCLKL}	15		ns
SCLK Pulse width high	T_{SCLKH}	15		ns
SCLK falling to LRCK edge	T_{SLR}	－10	10	ns
SCLK falling to SDOUT valid	T_{SDO}	0		ns
SDIN valid to SCLK rising setup time	T_{SDIS}	10		ns
SCLK rising to SDIN hold time	T_{SDIH}	10		ns

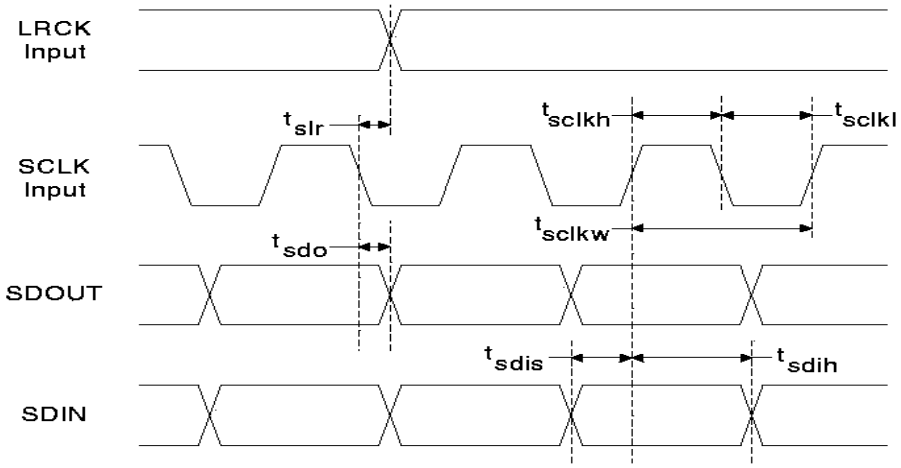


Figure 8 Serial Audio Port Timing

12.7 Serial Control Port Switching Specifications

PARAMETER	Symbol	MIN	MAX	UNIT
SPI Mode				
SPI_CLK clock frequency			10	MHz
SPI_CLK edge to SPI_CSn falling	T_{SPICS}	5		ns
SPI_CSn High Time Between transmissions	T_{SPISH}	500		ns
SPI_CSn falling to SPI_CLK edge	T_{SPISC}	10		ns
SPI_CLK low time	T_{SPICL}	45		ns
SPI_CLK high time	T_{SPICH}	45		ns
SPI_DIN to SPI_CLK rising setup time	T_{SPIDS}	10		ns
SPI_CLK rising to DATA hold time	T_{SPIDH}	15		ns
2-wire Mode				
SCL Clock Frequency	F_{SCL}		100	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7		us
Start Condition Hold Time	T_{TWSTH}	4.0		us

Clock Low time	T_{TWCL}	4.0		us
Clock High Time	T_{TWCH}	4.0		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7		us
SDA Hold Time from SCL Falling	T_{TWDH}	0.1		us
SDA Setup time to SCL Rising	T_{TWDS}	100		ns
Rise Time of SCL	T_{TWR}		25	us
Fall Time SCL	T_{TWF}		25	ns

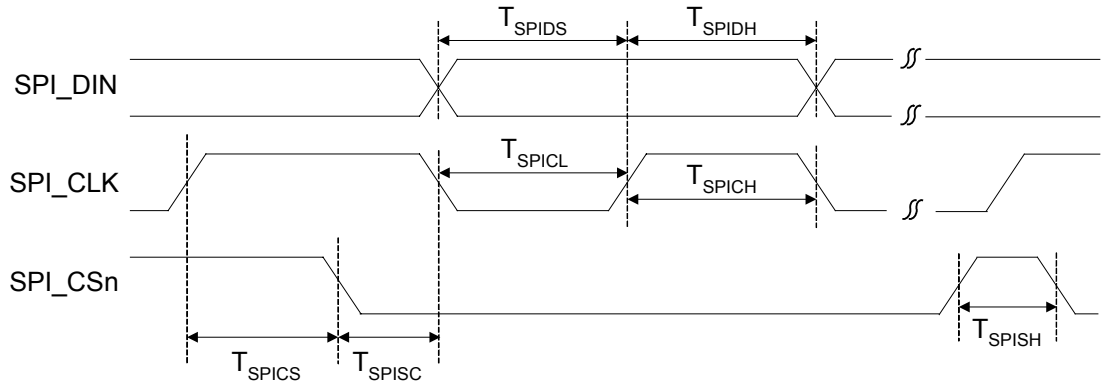


Figure 9 Serial Control Port SPI Timing

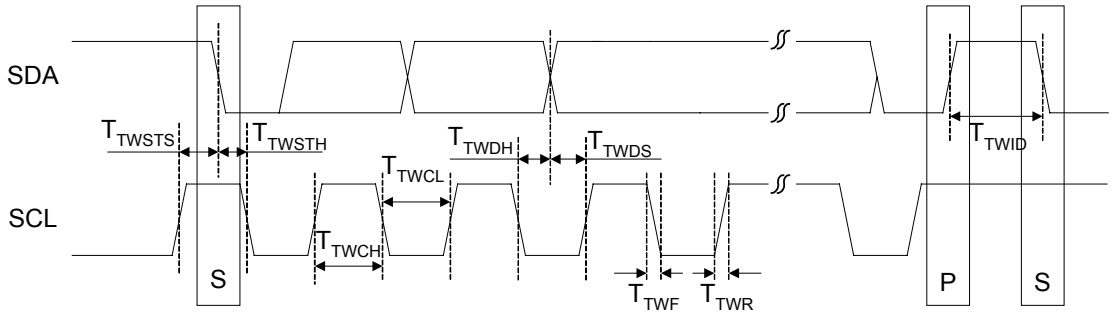
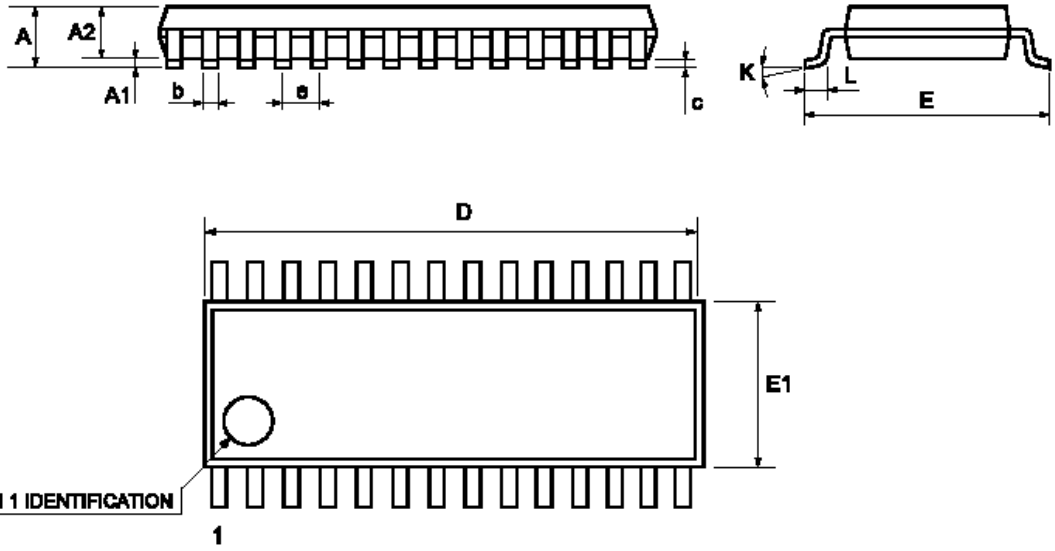


Figure 10 Serial Control Port 2-wire Timing

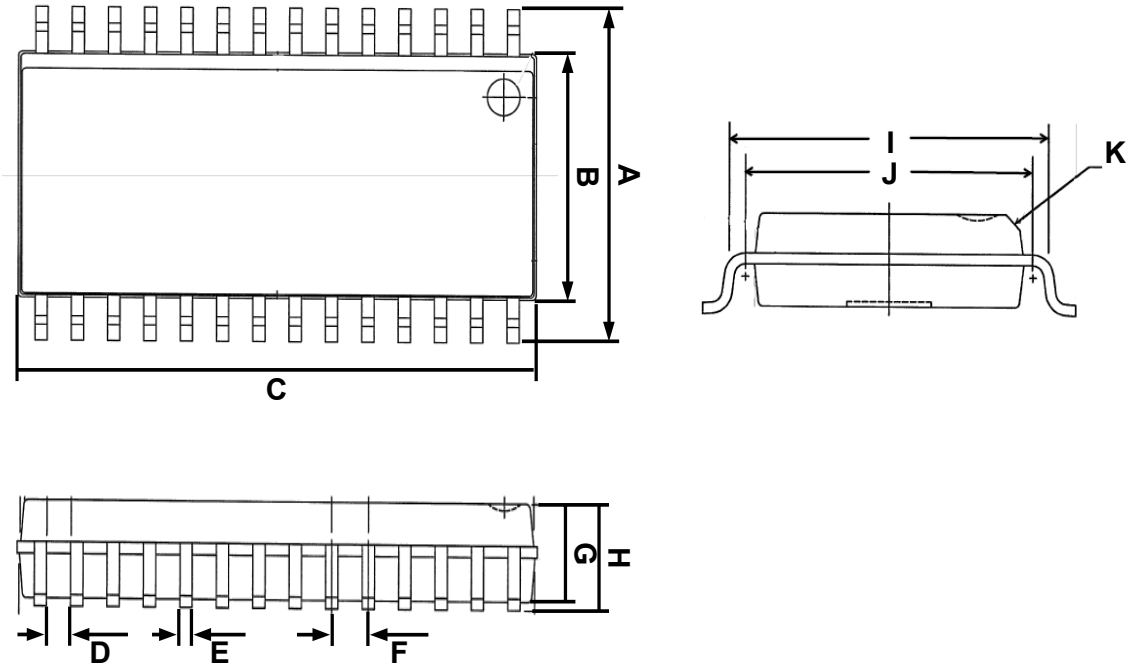
13 PACKAGE INFORMATION

13.1 28-pin SSOP Outline Dimensions



DIMENSIONS						
REF.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2			0.079
A1	0.050			0.002		
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22		0.38	0.009		0.015
c	0.09		0.25	0.004		0.010
D	9.9	10.2	10.5	0.390	0.402	0.413
E	7.4	7.8	8.2	0.291	0.307	0.323
E1	5	5.3	5.6	0.197	0.209	0.220
e		0.65			0.0256	
K	0°		10°	0°		10°
L	0.55	0.75	0.95	0.022	0.030	0.037

13.2 28-pin SOP Outline Dimensions



Symbols	Dimensions (inch)			Dimensions (mm)		
	Min	TYP	Max	Min	TYP	Max
A	0.406	---	0.414	10.31	---	10.51
B	0.293	---	0.295	7.45	---	7.49
C	0.708	---	0.712	17.98	---	18.08
D	---	0.034	---	---	0.87	---
E	---	0.017	---	---	0.43	---
F	---	0.050	---	---	1.27	---
G	0.091	---	0.093	2.32	---	2.36
H	0.098	---	0.102	2.50	---	2.59
I	0.340	---	0.348	8.64	---	8.84
J	0.316	---	0.324	8.03	---	8.23
K	---	0.015x45°	---	---	0.38x45°	---

14 ORDERING INFORMATION

Part Number	Package
ES7322-SO	28 pin SOP
ES7322-SS	28 pin SSOP

15 REVISION HISTORY

- V1.0 – initial release
- V2.0 – modified section 7.2 to address the differences between 2-wire mode and I^2C protocol
- V3.0 – modified section 8.5 and added SOP package information in section 13

16 CORPOARATION INFORMATION

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