# HMC669LP3 / 669LP3E

v04.0709

## GaAs PHEMT MMIC LNA w/ FAILSAFE BYPASS MODE, 1700 - 2200 MHz

### Typical Applications

The HMC669LP3(E) is ideal for:

- Cellular/3G and LTE/WiMAX/4G
- BTS & Infrastructure
- Repeaters and Femtocells
- Tower Mounted Amplifiers
- Test & Measurement Equipment

### Features

Noise Figure: 1.4 dB

Output IP3: +29 dBm

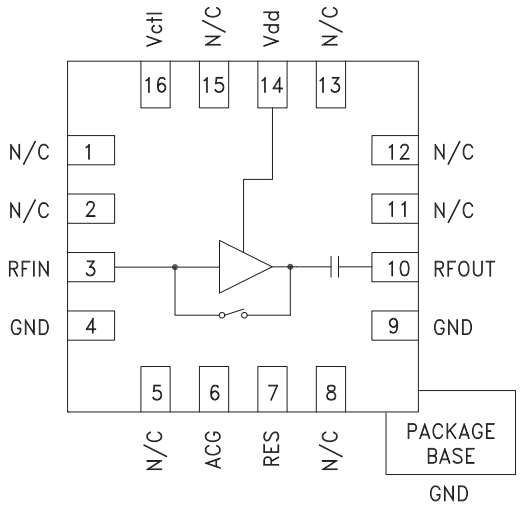
Gain: 17 dB

Failsafe Operation:
Bypass is enabled when LNA is unpowered

Single Supply: +3V or +5V

16 Lead 3x3mm QFN Package: 9 $mm^2$

### Functional Diagram




### General Description

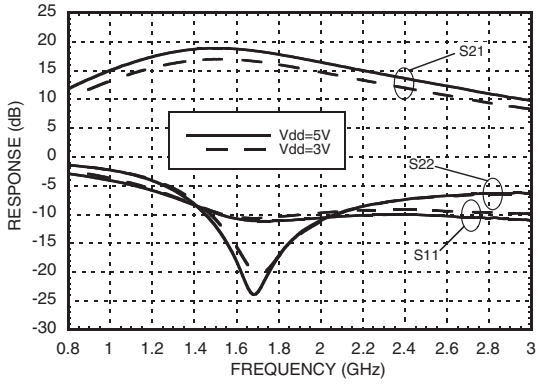
The HMC669LP3(E) is a versatile, high dynamic range GaAs MMIC Low Noise Amplifier that integrates a low loss LNA bypass mode on the IC. The amplifier is ideal for receivers and LNA modules operating between 1.7 and 2.2 GHz and provides 1.4 dB noise figure, 17 dB of gain and +29 dBm IP3 from a single supply of +5V @ 86mA. Input and output return losses are excellent and no external matching components are required. A single control line is used to switch between LNA mode and a low loss bypass mode. Failsafe topology also enables the LNA bidirectional bypass path when no DC power is available.

### Electrical Specifications, $T_A$ = +25° C, Rbias = 15 Ohm

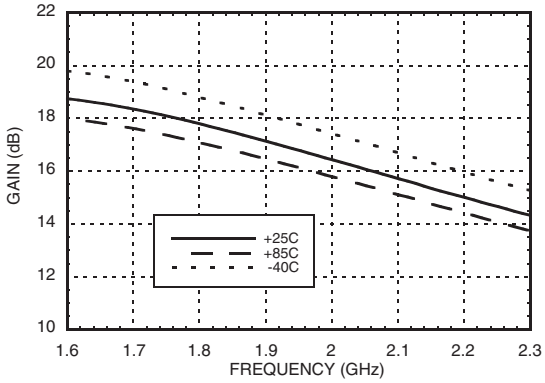
| Parameter | LNA Mode | | | | | | Bypass Mode | | | Failsafe Mode | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Vdd = +3V | | | Vdd = +5V | | | | | | | | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Frequency Range | 1.7 - 2.2 | | | 1.7 - 2.2 | | | 1.7 - 2.2 | | | 1.7 - 2.2 | | | GHz |
| Gain | 12 | 15 | | 14 | 17 | | -3 | -2.1 | | -3 | -2.1 | | dB |
| Gain Variation Over Temperature | | 0.015 | | | 0.014 | | | 0.0008 | | | 0.0008 | | dB / °C |
| Noise Figure | | 1.4 | 1.65 | | 1.4 | 1.65 | | | | | | | dB |
| Input Return Loss | | 10 | | | 11 | | | 12 | | | 12 | | dB |
| Output Return Loss | | 13 | | | 13 | | | 12 | | | 12 | | dB |
| Reverse Isolation | | 28 | | | 30 | | | - | | | - | | dB |
| Power for 1dB Compression (P1dB)[1] | | 11.5 | | | 12 | | | 21 | | | 24 | | dBm |
| Third Order Intercept (IP3)[2] | | 25 | | | 29 | | | 25 | | | 25 | | dBm |
| Supply Current (Idd) | | 49 | 59 | | 86 | 105 | | 0.04 | | | - | | mA |
| Switching Speed<br>LNA Mode to Bypass Mode<br>Bypass Mode to LNA Mode | | <br><br>100 | | | <br><br>100 | | | 80 | | | - | | <br>ns<br>ns |

[1] P1dB for LNA Mode is referenced to RFOUT while P1dB for Bypass and Failsafe Modes are referenced to RFIN.
[2] IP3 for LNA Mode is referenced to RFOUT while IP3 for Bypass and Failsafe Modes are referenced to RFIN.

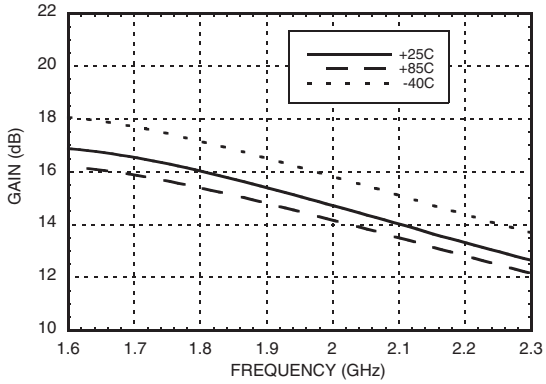
### LNA - Broadband Gain & Return Loss



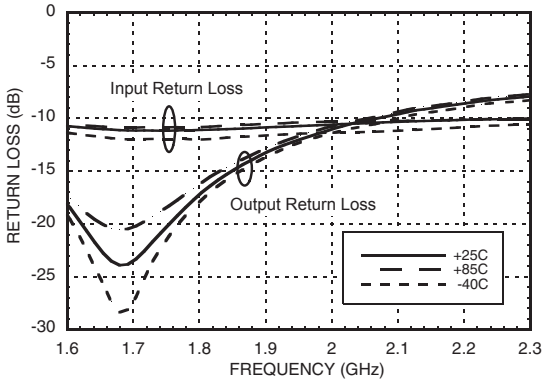

### LNA - Gain vs. Temperature [1]



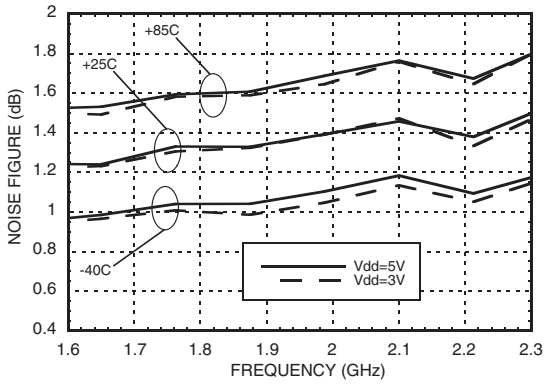

### LNA - Gain vs. Temperature [2]



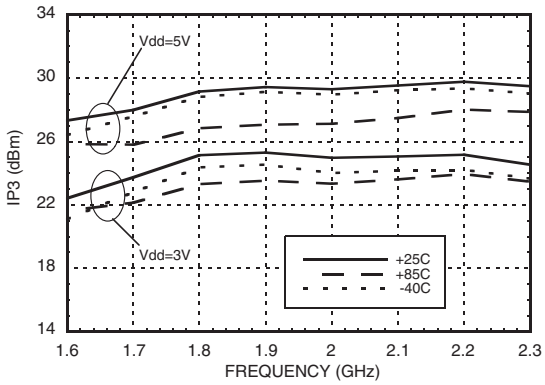

### LNA - Return Loss vs. Temperature [1]




### LNA - Noise Figure vs. Temperature [3]




### LNA - Output IP3 vs. Temperature, Output Power @ 0 dBm

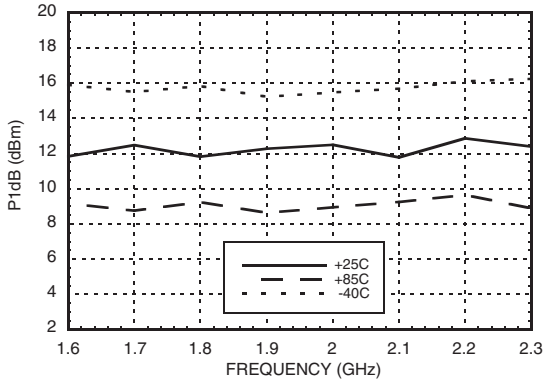



[1] Vdd = 5V [2] Vdd = 3V [3] Measurement reference plane shown on evaluation PCB drawing.

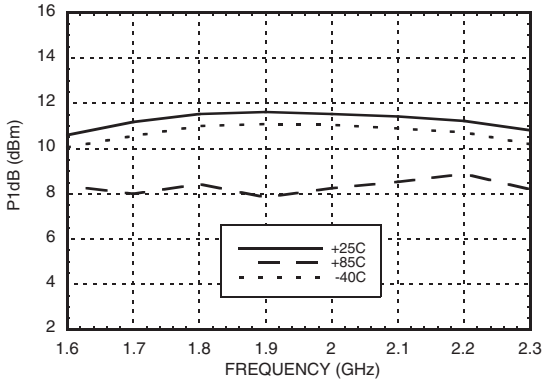
# HMC669LP3 / 669LP3E

## GaAs PHEMT MMIC LNA w/ FAILSAFE BYPASS MODE, 1700 - 2200 MHz

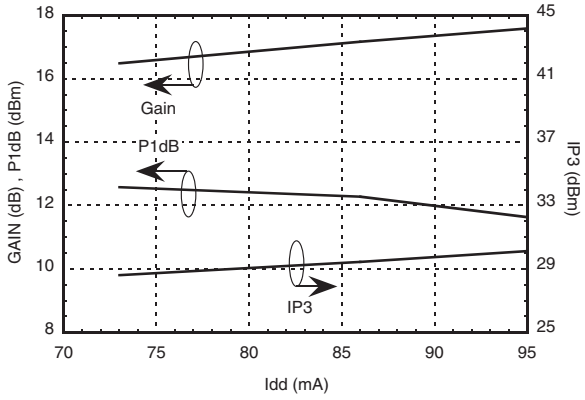
### LNA - Output P1dB vs. Temperature [1]



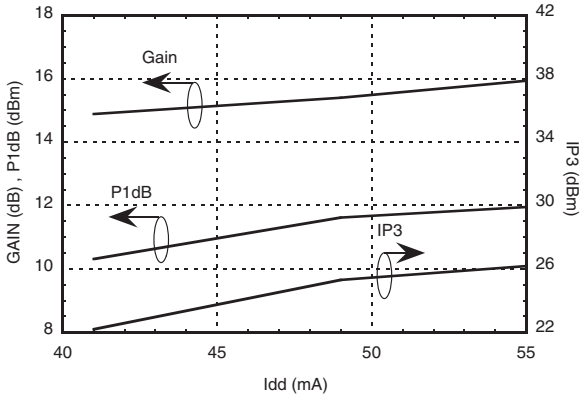

### LNA - Output P1dB vs. Temperature [2]



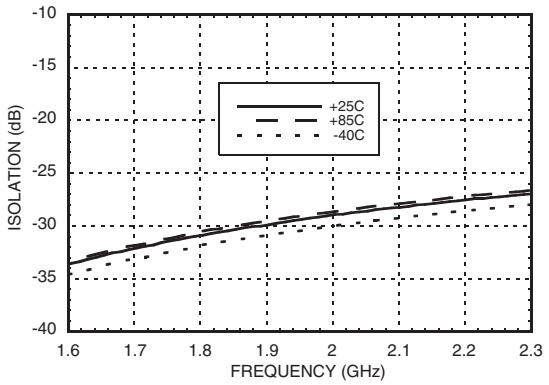

### LNA - Gain, P1dB, Output IP3 vs. Current [1] @ 1900 MHz



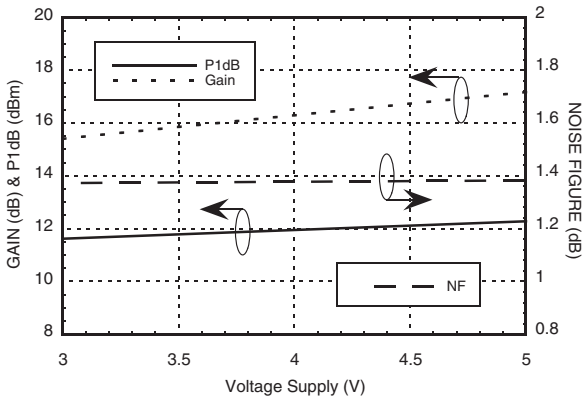

### LNA - Gain, P1dB, Output IP3 vs. Current [2] @ 1900 MHz




### LNA - Reverse Isolation vs. Temperature [1]

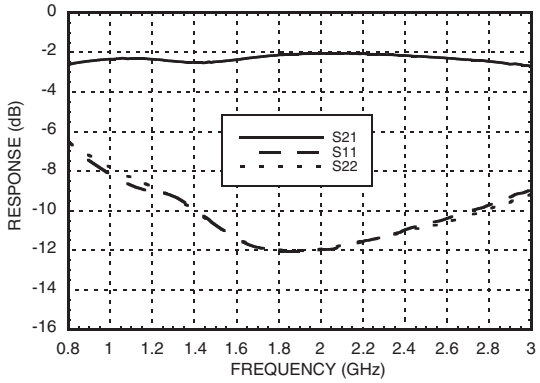



### LNA - Output P1dB, Gain & Noise Figure [3] vs. Vdd @ 1900 MHz

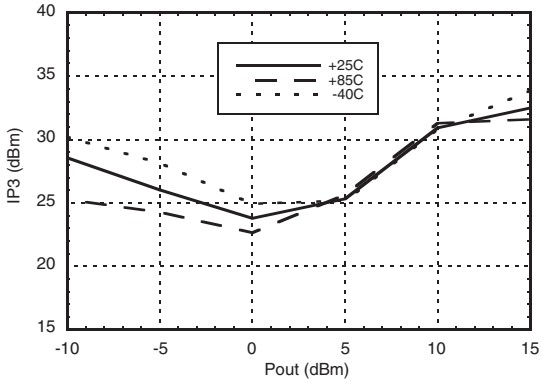



[1] Vdd = 5V [2] Vdd = 3V [3] Measurement reference plane shown on evaluation PCB drawing.

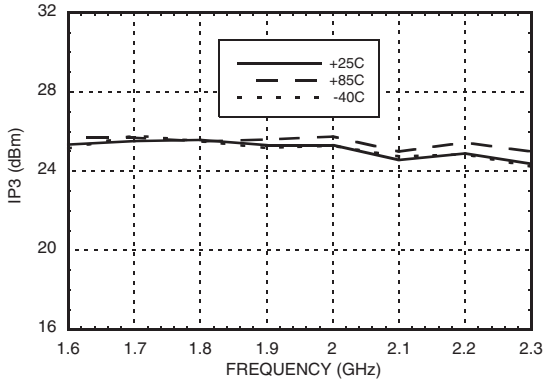
### Bypass Mode - Broadband Gain & Return Loss



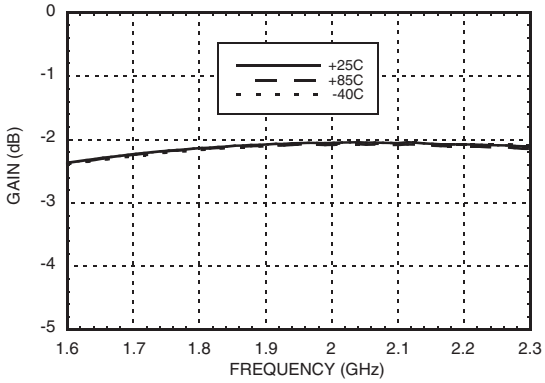

### Bypass Mode - Input IP3 vs. Output Power @ 1900 MHz



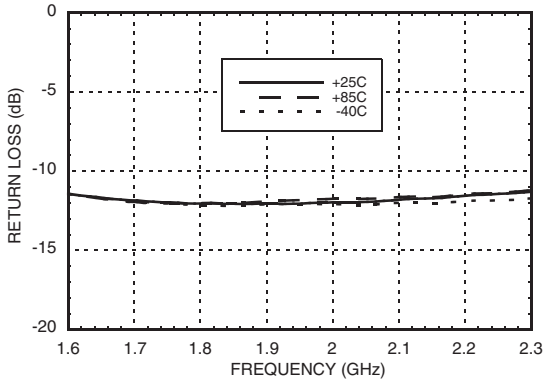

### Bypass Mode - Input IP3 vs. Temperature, Output Power @ 5 dBm



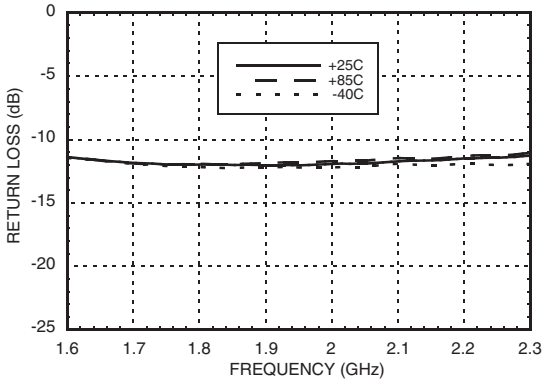

### Bypass Mode - Insertion Loss vs. Temperature



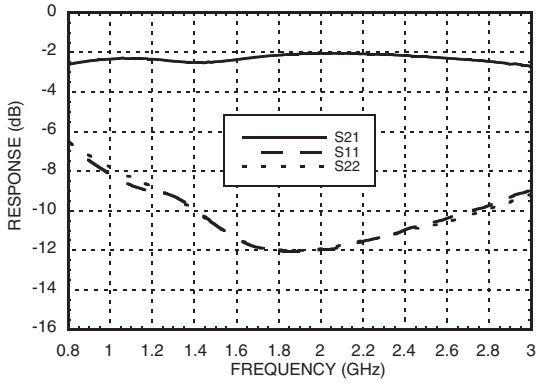

### Bypass Mode - Input Return Loss vs. Temperature



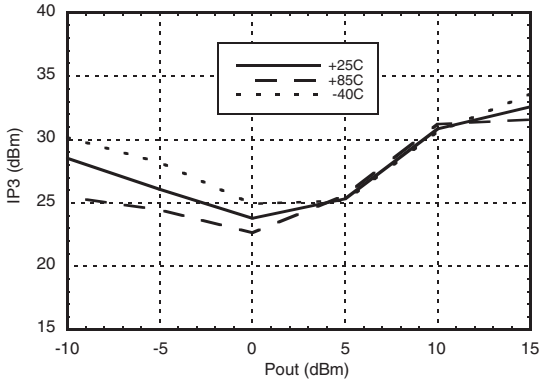

### Bypass Mode - Output Return Loss vs. Temperature



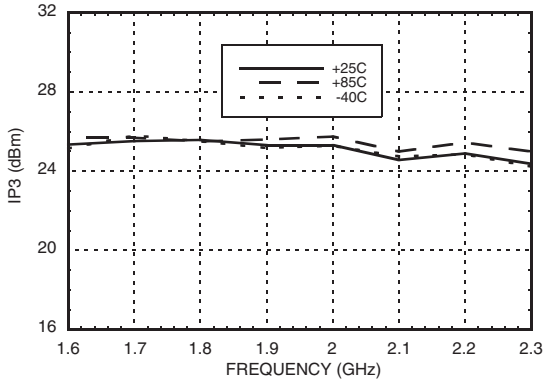
### Failsafe Mode - Broadband Gain & Return Loss



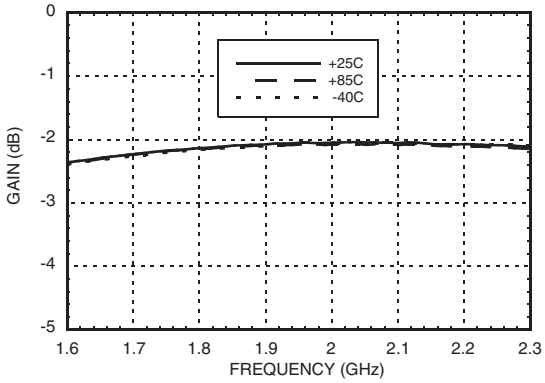

### Failsafe Mode - Input IP3 vs. Output Power @ 1900 MHz



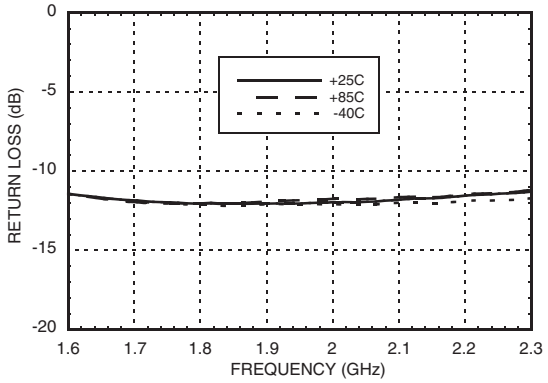

### Failsafe Mode - Input IP3 vs. Temperature, Output Power @ 5 dBm



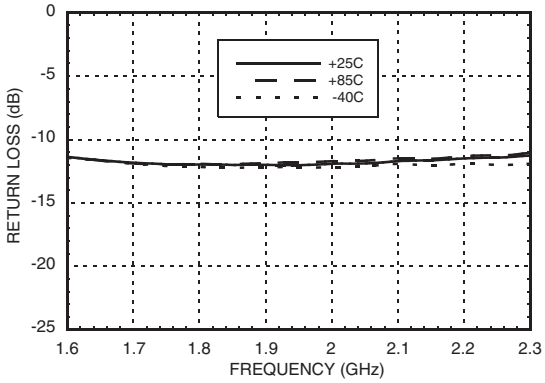

### Failsafe Mode - Insertion Loss vs. Temperature




### Failsafe Mode - Input Return Loss vs. Temperature




### Failsafe Mode - Output Return Loss vs. Temperature



## Absolute Maximum Ratings

| | |
|---|---|
| Drain Bias Voltage (Vdd) | +6 Vdc |
| Control Voltage (Vctl) | +6 Vdc |
| RF Input Power (RFIN) LNA Mode<br>Bypass / Fail safe Mode | +5 dBm<br>+20 dBm |
| Channel Temperature | 150 °C |
| Continuous Pdiss (T = 85 °C) (derate 10.71 mW/°C above 85 °C) | 0.70 W |
| Thermal Resistance (channel to ground paddle) | 93.33 °C/W |
| Storage Temperature | -65 to +150° C |
| Operating Temperature | -40 to +85° C |
| ESD Sensitivity (HBM) | Class 1A |

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

## Typical Supply Current vs. Vdd

| Rbias Ω | Idd (mA) | |
|---|---|---|
| | Vdd= 3V | Vdd= 5V |
| 0 | 55 | 95 |
| 15 | 49 | 86 |
| 47 | 41 | 73 |
| 180 [1] | 28 | 50 |

[1] Recommended maximum Rbias

## Truth Table

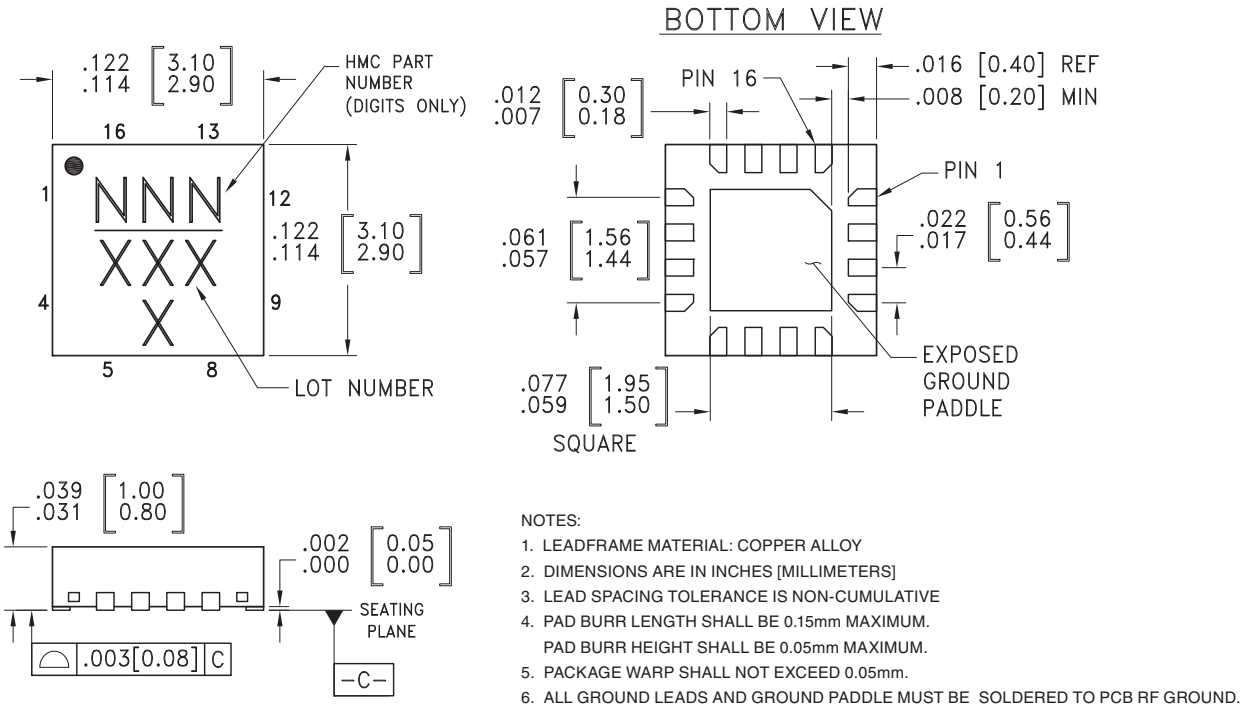
| | |
|---|---|
| LNA Mode | Vctl = Vdd = 3 to 5V |
| Bypass Mode | Vctl= 0V, Vdd = 3 to 5V |
| Failsafe Mode | Vctl = Vdd = N/C |

# HMC669LP3 / 669LP3E

## GaAs PHEMT MMIC LNA w/ FAILSAFE BYPASS MODE, 1700 - 2200 MHz



### Outline Drawing




NOTES:

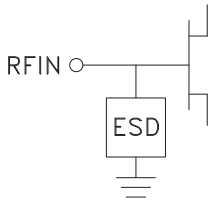
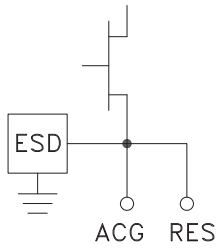
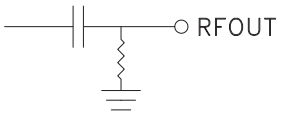
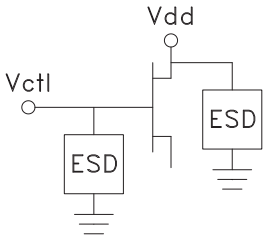
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

### Package Information

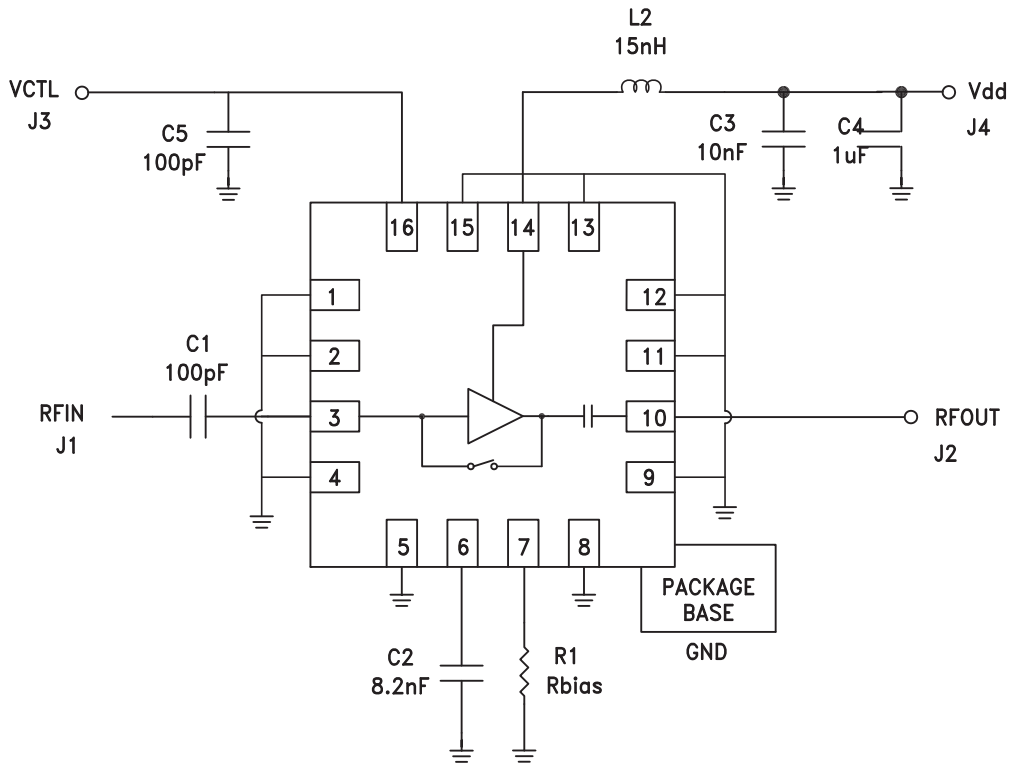
| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking [3] |
|---|---|---|---|---|
| HMC669LP3 | Low Stress Injection Molded Plastic | Sn/Pb Solder | MSL1 [1] | 669<br>XXXX |
| HMC669LP3E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 [2] | 669<br>XXXX |

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

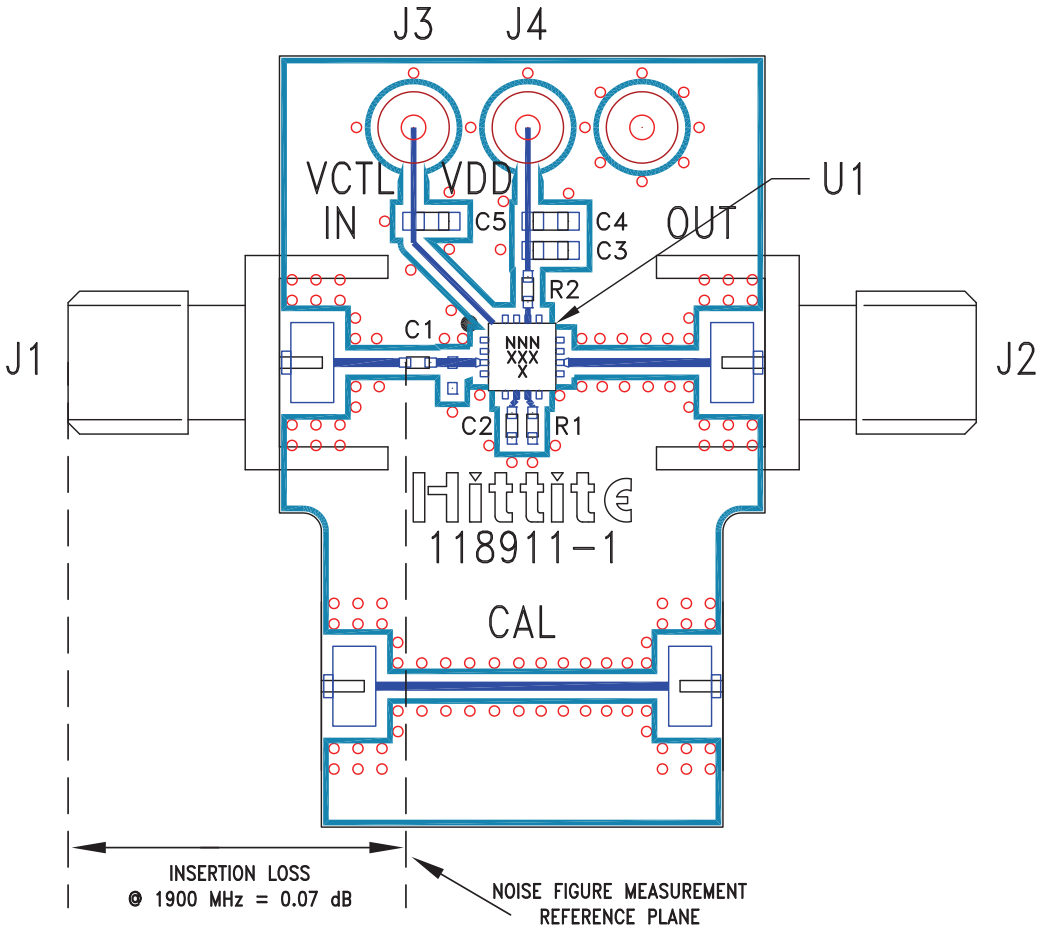
## Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1, 2, 5, 8, 11, 12, 13, 15 | N/C | These pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally. | |
| 3 | RFIN | This pin is DC coupled. Off-chip DC blocking capacitor required. |   |
| 4, 9 | GND | These pins and the exposed ground paddle must be connected to RF/DC ground. | |
| 6 | ACG | AC Ground. Attach bypass capacitor per application circuit. |   |
| 7 | RES | External resistor pin for current control. See table for external resistor value vs. bias current data. | |
| 10 | RFOUT | This pin is matched to 50 Ohms |   |
| 14 | Vdd | Power Supply voltage pin. External bypass capacitors required. |   |
| 16 | Vctl | Control voltage pin for LNA / Bypass Modes. Setting voltage equal to VDD enables LNA Mode. External Bypass capacitor required. | |

## Application Circuit



## Evaluation PCB




## List of Materials for Evaluation PCB 121923 [1]

| Item | Description |
|---|---|
| J1 - J2 | PCB Mount SMA Connector |
| J3 - J4 | DC Pin |
| C1 | 82 pF Capacitor, 0402 Pkg. |
| C2 | 8200 pF Capacitor, 0402 Pkg. |
| C3 | 10 nF Capacitor, 0603 Pkg. |
| C4 | 1 µF Capacitor, 0603 Pkg. |
| C5 | 100 pF Capacitor, 0603 Pkg. |
| R1 | 15 Ohm Resistor, 0402 Pkg. |
| R2 | 0 Ohm Resistor, 0402 Pkg. |
| U1 | HMC669LP3(E) Amplifier |
| PCB [2] | 118911 Evaluation Board |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.