T73LVP22

Dual 3.3V LVTTL/LVCMOS-to-Differential LVPECL Translator

Applications

- Multiple LVPECL clock sources

General Description

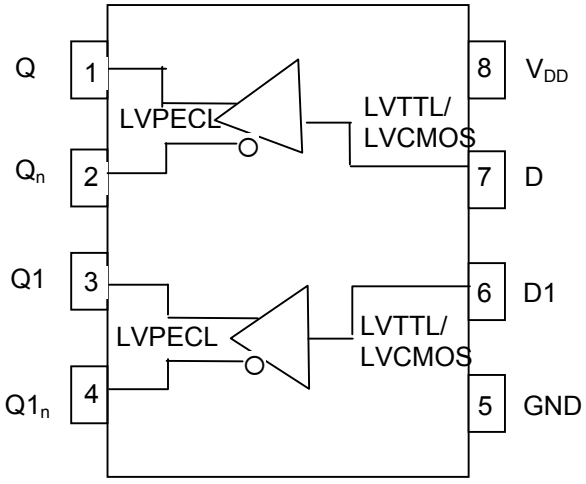
The TLSI T73LVP22 is a general-purpose dual LVTTL (LVCMOS)-to-differential LVPECL translator operating from a single +3.3V supply. The device has two independent channels that accept an LVTTL or LVCMOS input and provide differential LVPECL outputs referenced to the positive supply rail. The small 8-pin SOIC package makes it ideal for applications which require the translation of multiple clocks or data signals, and where cost, performance and size are of critical importance. The T73LVP22 is 100K PECL compatible **and is a pin-for-pin replacement for the MC100EPT22D.**

Features

- 350pS typical propagation delay
- Operating Frequency > 1 GHz
- Differential LVPECL outputs
- Flow-through pinout
- Q, Q1 outputs default low with input (D) open
- ESD rating >2000V (Human Body Model) or >200V (Machine Model)
- -40 °C to +85 °C operating temperature range
- Available in standard 8-pin SOIC package

Figure 1. Functional Block Diagrams & Pin Assignments (Top View)

8-pin SOIC



See page 4 for package outline drawing and ordering information.

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Table 1. Pin Description

Name	Description	Type	Pin #
Q, Q1	LVPECL data outputs	O	1, 3
Q_n, $Q1_n$	LVPECL complementary data outputs	O	2, 4
V_{DD}	Connect to +3.3V	P	8
D, D1	LVCMOS/LVTTL data inputs	I	7, 6
GND	Connect to ground	P	5

Legend: I = Input
O = Output
P = Power supply connection

Table 2. Absolute Maximum Ratings (each channel)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply voltage	Referenced to GND			+5.0	V
V_{IN}	Input voltage	Referenced to GND	-0.5		V_{DD}	V
I_{OUT}	Output current	Continuous			50	mA
T_{STG}	Storage temperature		-65		+150	^{o}C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3. Operating Conditions (each channel)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply Voltage		+3.0	+3.3	+3.6	V
T_A	Ambient Temperature		-40		+85	^{o}C
V_{IH}	Input HIGH Voltage		+2.0			V
V_{IL}	Input LOW Voltage				+0.8	V

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Table 4. DC Characteristics (each channel)

T_A = -40°C to +85°C, V_{DD} = +3.0V to +3.6V unless otherwise stated below.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	Input HIGH Current	V_{IN} =+2.7V				100	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V				1	µA
V_{IK}	Input Clamp Diode Voltage	I_{IN} = -18mA				-1.2	V
V_{OH}	Output HIGH Voltage(1, 2)	-40°C	V_{DD} = +3.3V	2220	2320	2420	mV
		+25°C		2220	2320	2420	mV
		+85°C		2220	2320	2420	mV
V_{OL}	Output LOW Voltage(1, 2)	-40°C	V_{DD} = +3.3V	1420	1520	1620	mV
		+25°C		1420	1520	1620	mV
		+85°C		1420	1520	1620	mV
I_{DD}	Power Supply Current	Total both channels, no load			46		mA

Notes: 1. The T73LVP22 is designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board.
2. Q, Q1 and Qn, Q1n outputs are loaded with 50 ohms to V_{DD}-2 volts.

Table 5. AC Characteristics (each channel)

T_A = -40°C to +85°C, V_{DD} = +3.0V to +3.6V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay (1)	To Output Differential		350	500	ps
t_{PHL}	Propagation Delay (1)	To Output Differential		350	500	ps
t_r/t_f	Output Rise/Fall time	20%-80%, Q/Q_n	80	130	200	ps
f_{MAX}	Maximum Input Frequency	LVTTL or LVCMOS input		> 1		GHz
f_{MAX}	Maximum Input Frequency (2)	750mV peak-to-peak sine wave centered around 1.5V		> 1		GHz

Notes: 1. Q, Q1 and Qn, Q1n outputs are loaded with 50 ohms to V_{DD}-2 volts.
2. Measured using a 750mV peak-to-peak, 50% duty cycle clock source.

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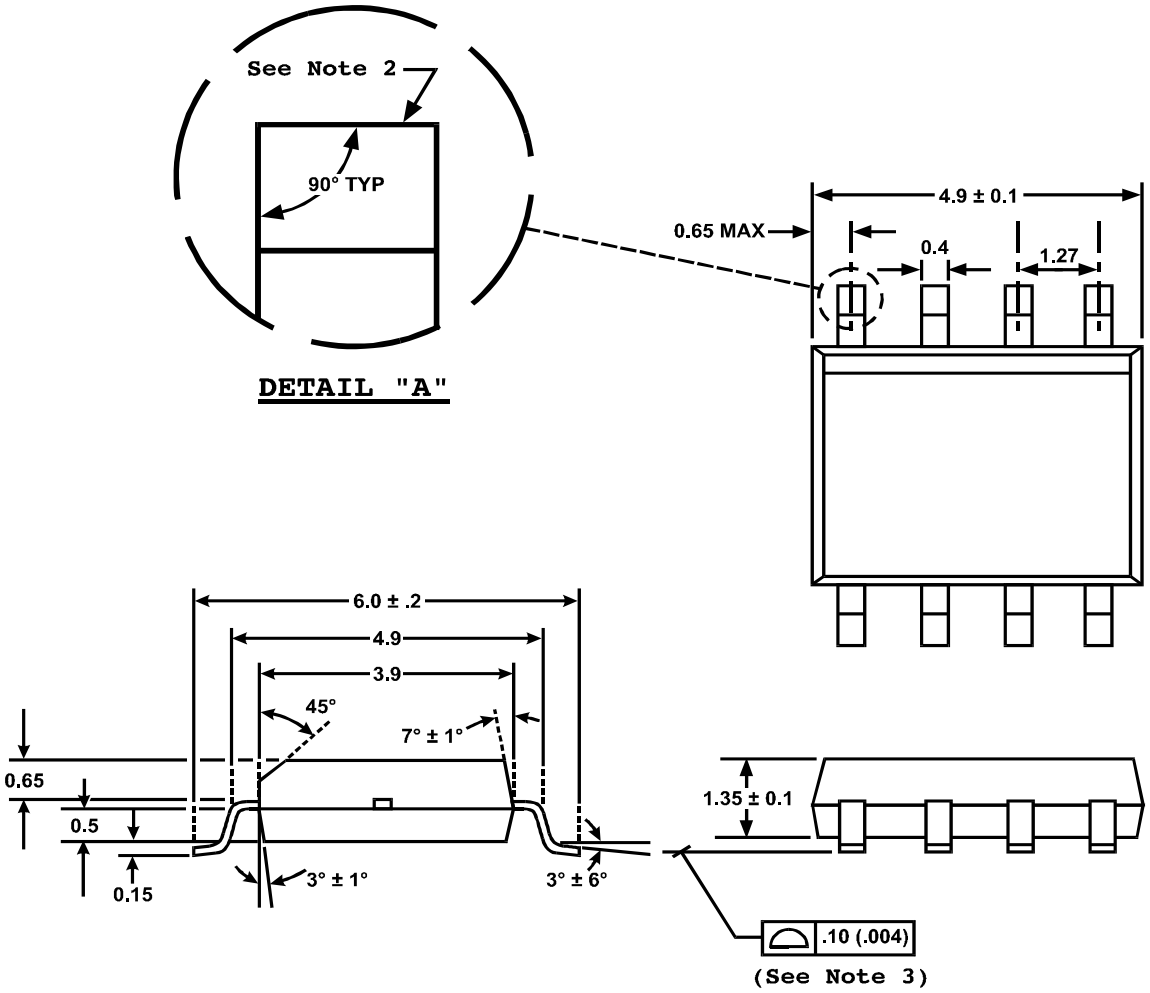
Figure 2. Package Outline (8-pin SOIC)



Note: 1) All dimensions are in mm.
2) All leads must be blunt cut. (See DETAIL "A")
3) Lead coplanarity not to exceed 0.004" maximum.

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Table 6. Ordering Information

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
T73LVP22-S08	T73LVP22	Tubes	8	SOIC	-40°C to +85°C
T73LVP22-S08-TNR	T73LVP22	Tape & Reel	8	SOIC	-40°C to +85°C

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