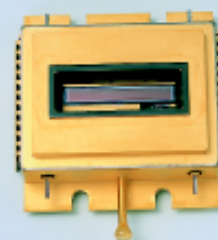


CCD area image sensor

S7847 series

High IR sensitivity, four-stage TE-cooled, front-illuminated FFT-CCDs



S7847 series is a family of FFT-CCD image sensors specifically designed for low-light-level detection in scientific applications. By using the binning operation, S7847 series can be used as a linear image sensor having a long aperture in the direction of the device length. This makes S7847 series ideally suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. S7847 series also features low noise and low dark signal (MPP mode operation). These enable low-light-level detection and long integration time, thus achieving a wide dynamic range. S7847 series has a pixel size of $24 \times 24 \mu\text{m}$ and is available in active area of $24.576 \text{ (H)} \times 2.976 \text{ (V)}$ and $24.576 \text{ (H)} \times 6.048 \text{ (V)}$ mm. A four-stage Peltier element is built into the same package for thermoelectric cooling. At room temperature operation, the device can be cooled down to -70°C with using forced air cooling. In addition, since both the CCD chip and Peltier element are hermetically sealed, no dry air is required, thus allowing easy handling.

Features

- 1024 (H) $\times$ 124 (V) and 1024 (H) $\times$ 252 (V) pixel format
- Pixel size: $24 \times 24 \mu\text{m}$
- 100 % fill factor
- Wide dynamic range
- Low dark current
- Low readout noise
- MPP operation
- Four-stage TE-cooled
- High IR response

Applications

- Astronomy
- Scientific measuring instrument
- Fluorescence spectrometer
- Raman spectrophotometer
- Optical and spectrophotometric analyzer
- For low-light-level detection requiring

Selection and order guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) $\times$ mm (V)]
S7847-1007	Four-stage	1044 $\times$ 128	1024 $\times$ 124	24.576 $\times$ 2.976
S7847-1008	TE-cooled	1044 $\times$ 256	1024 $\times$ 252	24.576 $\times$ 6.048

S7847 series has a hermetically-sealed package with AR-coated sapphire window.

General ratings

Parameter	Specification
CCD structure	Full frame transfer
Fill factor	100 %
Number of active pixels	S7847-1007 : 1024(H) $\times$ 124 (V) S7847-1008 : 1024(H) $\times$ 252 (V)
Pixel size	24 (H) $\times$ 24 (V) μm
Active area	S7847-1007: 24.576 (H) $\times$ 2.976 (V) mm S7847-1008: 24.576 (H) $\times$ 6.048 (V) mm
Vertical clock phase	2 phase
Horizontal clock phase	2 phase
Output circuit	One-stage MOSFET source follower
Package	28 pin metal package
Window	AR coated sapphire

■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+30	°C
Storage temperature	Tstg	-100	-	+70	°C
OD voltage	VOD	-0.5	-	+25	V
RD voltage	VRD	-0.5	-	+18	V
ISV voltage	VISV	-0.5	-	+18	V
ISH voltage	VISH	-0.5	-	+18	V
IGV voltage	VIG1V, VIG2V	-10	-	+15	V
IGH voltage	VIG1H, VIG2H	-10	-	+15	V
SG voltage	VSG	-10	-	+15	V
OG voltage	VOG	-10	-	+15	V
RG voltage	VRG	-10	-	+15	V
TG voltage	VTG	-10	-	+15	V
Vertical clock voltage	VP1V, VP2V	-10	-	+15	V
Horizontal clock voltage	VP1H, VP2H	-10	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit
Output transistor drain voltage	VOD	-	18	20	22	V
Reset drain voltage	VRD	-	11.5	12	12.5	V
Output gate voltage	VOG	-	1	3	5	V
Substrate voltage	VSS	-	-	0	-	V
Test point (vertical input source)	VISV	-	-	VRD	-	V
Test point (horizontal input source)	VISH	-	-	VRD	-	V
Test point (vertical input gate)	VIG1V, VIG2V	-	-8	0	-	V
Test point (horizontal input gate)	VIG1H, VIG2H	-	-8	0	-	V
Vertical shift register clock voltage	High	VP1VH, VP2VH	-	4	6	V
	Low	VP1VL, VP2VL	-	-9	-8	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	-	4	6	V
	Low	VP1HL, VP2HL	-	-9	-8	
Summing gate voltage	High	VSGH	-	4	6	V
	Low	VSGL	-	-9	-8	
Reset gate voltage	High	VRGH	-	4	6	V
	Low	VRGL	-	-9	-8	
Transfer gate voltage	High	VTGH	-	4	6	V
	Low	VTGL	-	-9	-8	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	80	2,000	kHz
Reset clock frequency	frg	-	-	80	2,000	kHz
Vertical shift register capacitance	S7847-1007	CP1V, CP2V	-	3,200	-	pF
	S7847-1008		-	6,400	-	
Horizontal shift register capacitance	CP1H, CP2H	-	-	300	-	pF
Summing gate capacitance	CSG	-	-	7	-	pF
Reset gate capacitance	CRG	-	-	7	-	pF
Transfer gate capacitance	CTG	-	-	150	-	pF
Transfer efficiency	CTE	*1	0.99995	0.99999	-	-
DC output level	Vout	*2	12	15	18	V
Output impedance	Zo	*2	-	3	-	kΩ
Power dissipation	P	*2, *3	-	15	-	mW

*1: Charge transfer efficiency per pixel, measured at half of the full well capacity.

*2: VOD=20 V, Load resistance =22 kΩ

*3: Power dissipation of the on-chip amplifier.

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage	Vsat	-	-	Fw × Sv	-	V
Full well capacity	Vertical	Fw	*4	150	300	ke ⁻
	Horizontal			300	600	
CCD conversion efficiency	Sv	*5	1.8	2.2	-	μV/e ⁻
Dark current (MPP mode)	+25 °C	DS	*6	-	4,000	e ⁻ /pixel/s
	0 °C			-	200	
	-70 °C			-	0.0015	
Readout noise	Nr	*7	-	6	12	e ⁻ rms
Dynamic range	Line binning	DR	*8	25,000	75,000	-
	Area scanning			12,500	37,500	
Spectral response range	λ	-	-	400 to 1,100	-	nm
Photo response non-uniformity	PRNU	*9	-	-	±10	%
Blemish	Point defects	-	*10	-	-	0
	Cluster defects		*11	-	-	
	Column defects		*12	-	-	

*4: Large horizontal full well for line binning operation.

*5: V_{DD} =20 V , Load resistance =22 kΩ

*6: Dark current nearly doubles for every 5 to7 °C increase in temperature.

*7: -40 °C, operating frequency is 80 kHz

*8: DR = Fw / Nr

*9: Measured at half of the full well capacity. PRNU (%) = noise / signal × 100, noise : fixed pattern noise (peak to peak)

*10: White spots > 3 % of full well at 0 °C after Ts=1 s, Black spots > 50 % reduction in response relative to adjacent pixels

*11: continuous 2 to 9 point defects

*12: continuous > 10 point defects

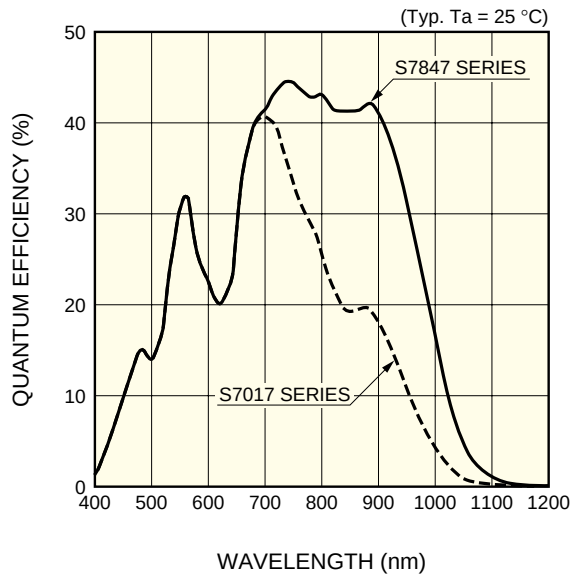
■ Pin connections

Pin no.	Symbol	Description	Remark
1	P-	TE-cooler-	
2	NC		
3	SS	Substrate (GND)	
4	NC		
5	ISV	Test point (vertical input source)	Shorted to RD
6	IG2V	Test point (vertical input gate-2)	Shorted to 0 V
7	IG1V	Test point (vertical input gate-1)	Shorted to 0 V
8	RG	Reset gate	
9	RD	Reset drain	
10	OS	Output transistor source	
11	OD	Output transistor drain	
12	OG	Output gate	
13	SG	Summing gate	Same timing as P2H
14	P+	TE-cooler+	
15	TSH1	Temperature sensor (hot side)	
16	TSC1	Temperature sensor (cool side)	
17	TSC2	Temperature sensor (cool side)	
18	P2H	CCD horizontal register clock-2	
19	P1H	CCD horizontal register clock-1	
20	IG2H	Test point (horizontal Input gate-2)	Shorted to 0 V
21	IG1H	Test point (horizontal Input gate-1)	Shorted to 0 V
22	ISH	Test point (horizontal Input source)	Shorted to RD
23	P2V	CCD vertical register clock-2	
24	P1V	CCD vertical register clock-1	
25	TG	Transfer gate	Same timing as P2 V *13
26	NC		
27	NC		
28	TSH2	Temperature sensor (hot side)	

*13: TG is an isolation gate between vertical register and horizontal resister.

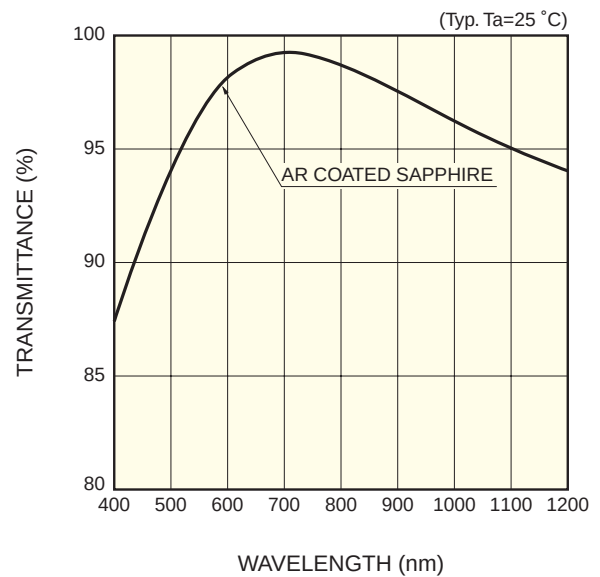
In standard operation, the same pulse of P2V should be applied to the TG.

■ Spectral response without window



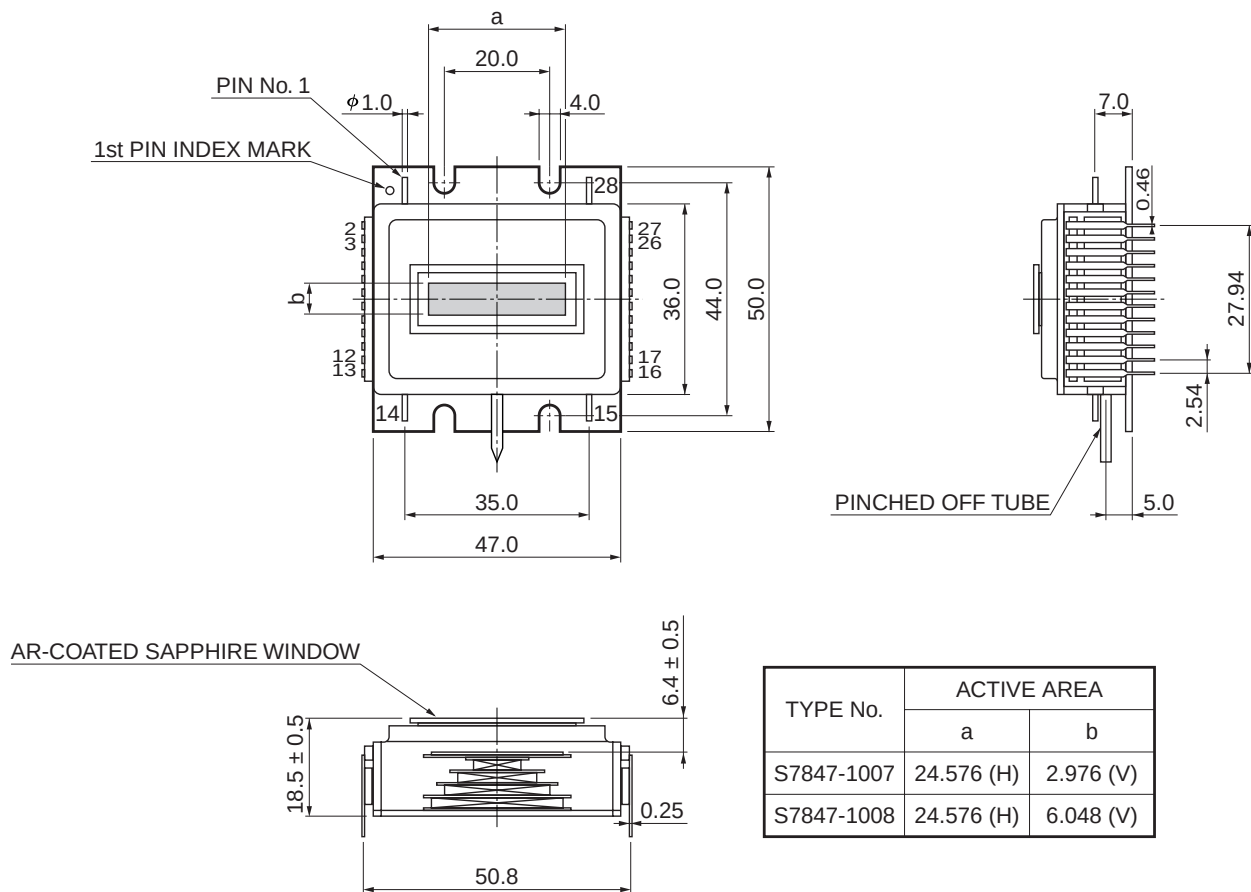
KMPDB0104EA

■ Spectral transmittance characteristic of window material



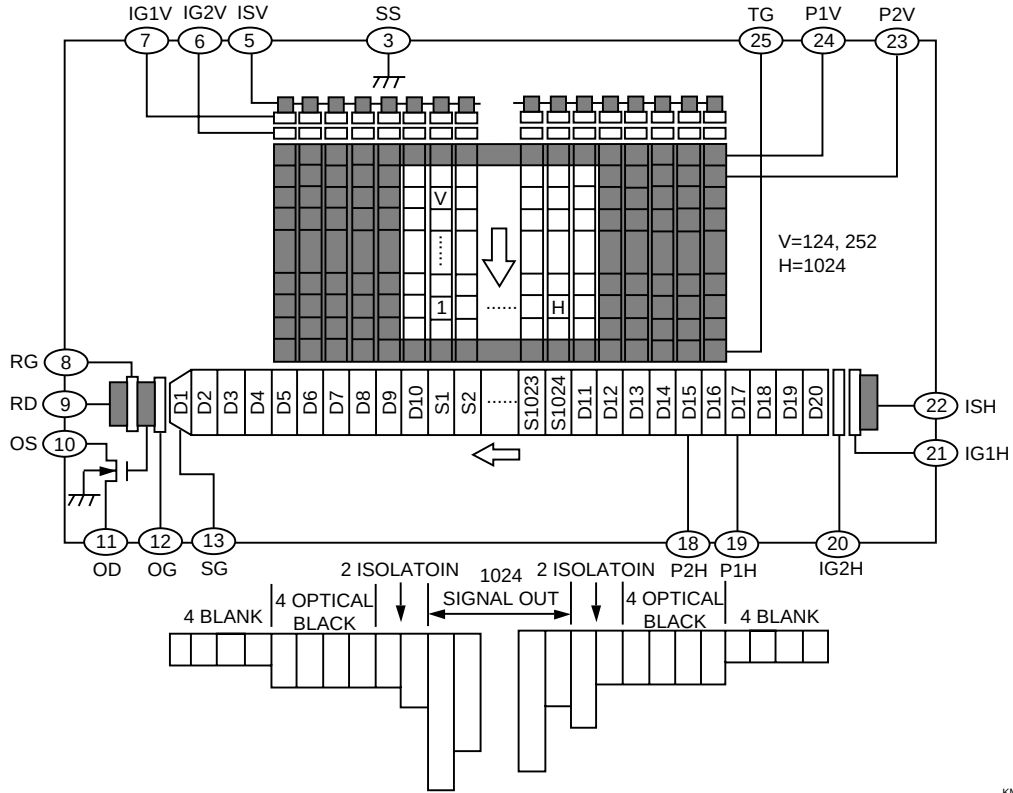
KMPDB0106EA

■ Dimensional outline (unit: mm)



KMPDA0099EA

■Device structure, line output format



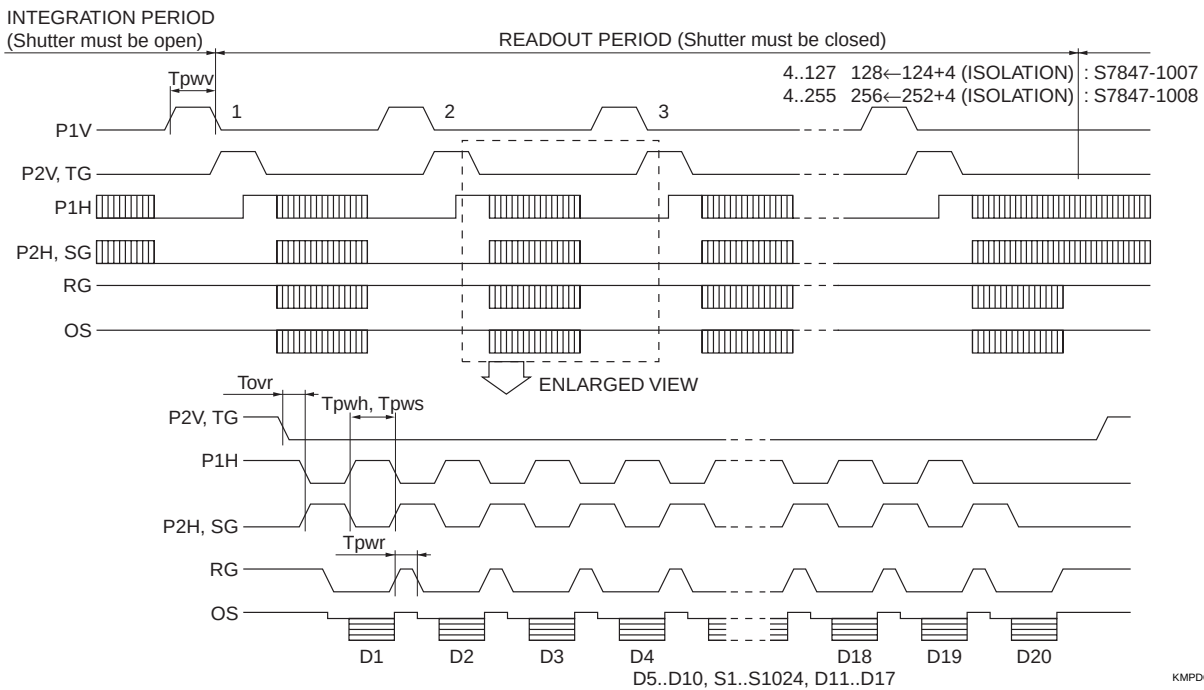
Pixel format

Left ← Horizontal Direction → Right						
Blank	Optical Black	Isolation	Effective	Isolation	Optical Black	Blank
4	4	2	1024	2	4	4

Top ← Vertical Direction → Bottom		
Isolation	Effective	Isolation
2	124 or 252	2

■ Timing chart

● Area scanning 1 (low dark current mode)

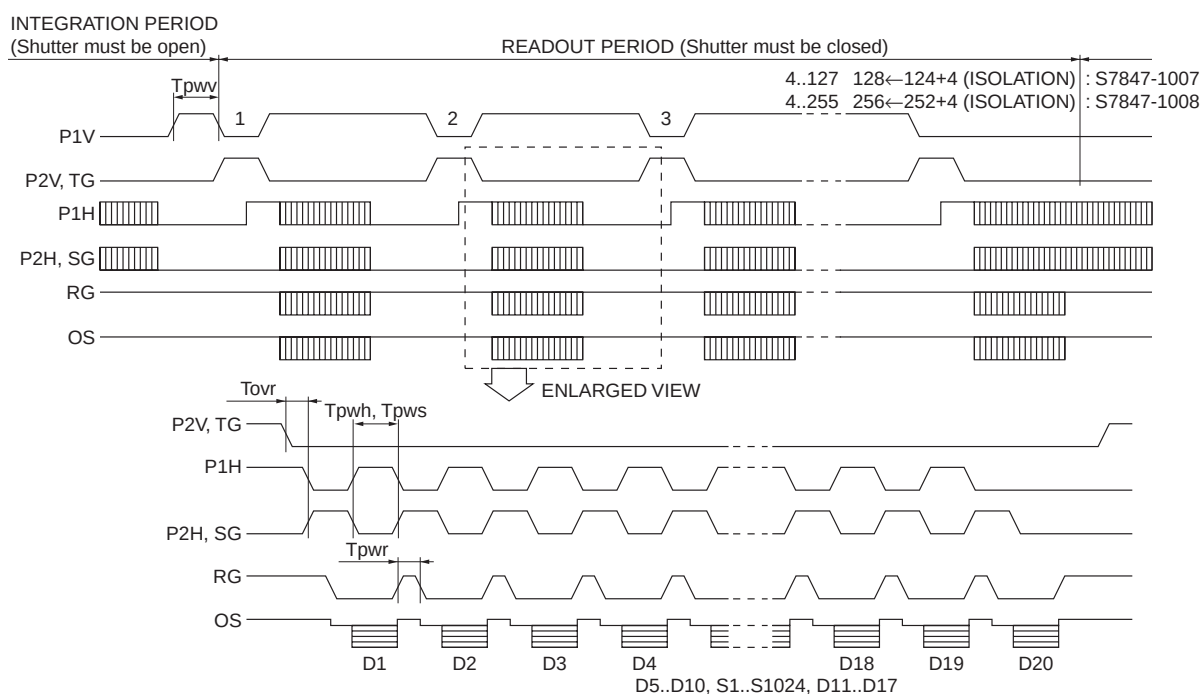


Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tp _{pwv}	*14	6 *15	-	-	μs
	Rise and fall time	Tp _{rv} , Tp _{fv}		200	-	-	ns
P1H, P2H	Pulse width	Tp _{wh}	*14	250	-	-	ns
	Rise and fall time	Tp _{rh} , Tp _{fh}		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tp _{ws}	-	250	-	-	ns
	Rise and fall time	Tp _{rs} , Tp _{fs}		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tp _{wr}	-	100	-	-	ns
	Rise and fall time	Tp _{rr} , Tp _{fr}		5	-	-	ns
TG - P1H	Overlap time	Tov _r	-	3	-	-	μs

*14: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

*15: In case of S7847-1007.

● Area scanning 2 (large full well mode)



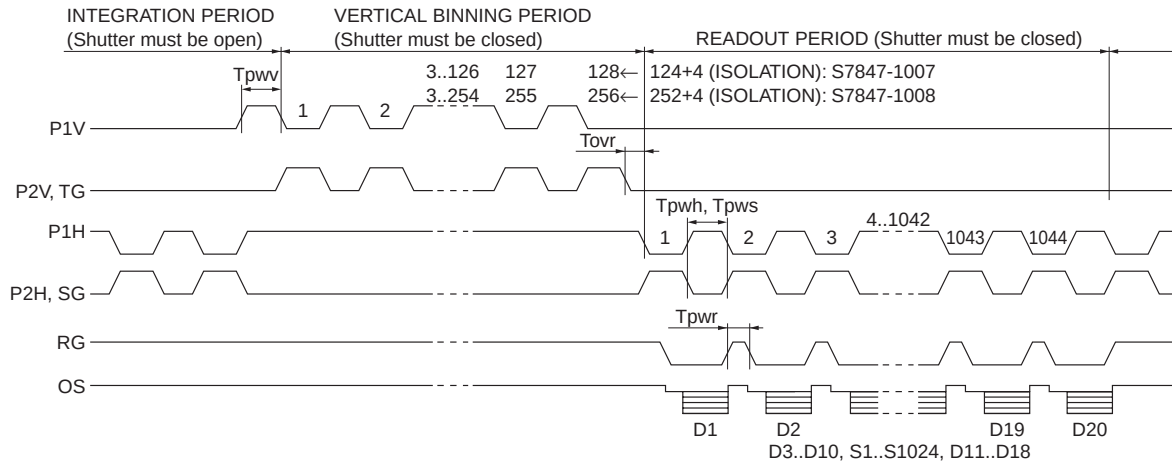
KMPDC0103EA

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tp _{pwv}	*16	6 *17	-	-	μs
	Rise and fall time	Tp _{rv} , Tp _{fv}		200	-	-	ns
P1H, P2H	Pulse width	Tp _{wh}	*16	250	-	-	ns
	Rise and fall time	Tp _{rh} , Tp _{fh}		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tp _{ws}	-	250	-	-	ns
	Rise and fall time	Tp _{rs} , Tp _{fs}		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tp _{wr}	-	100	-	-	ns
	Rise and fall time	Tp _{rr} , Tp _{fr}		5	-	-	ns
TG - P1H	Overlap time	Tov _r	-	3	-	-	μs

*16: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

*17: In case of S7847-1007.

● Line binning



KMPDC0089EA

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpww	*18	6 *19	-	-	μs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*18	250	-	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	250	-	-	ns
	Rise and fall time	Tprs, Tprfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	-	-	ns
	Rise and fall time	Tpr, Tprf		5	-	-	ns
TG – P1H	Overlap time	Tovr	-	3	-	-	μs

*18: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

*19: In case of S7847-1007.

■ Specifications of built-in TE-cooler

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal resistance	Rint	Ta=27 °C	-	1.6	-	Ω
Maximum current *20	I _{max}	Th *21=27 °C ΔT *22=ΔT _{max}	-	-	4.4	A
Maximum voltage	V _{max}	Th *21=27 °C ΔT=ΔT _{max} I=I _{max}	-	-	7.4	V
Maximum heat absorption *23	Q _{max}	Tc *24=Th *21=27 °C I=I _{max}	-	-	3.0	W
Maximum temperature at hot side	-		-	-	50	°C
CCD temperature	-	Ta=25 °C	-	-70	-50	°C

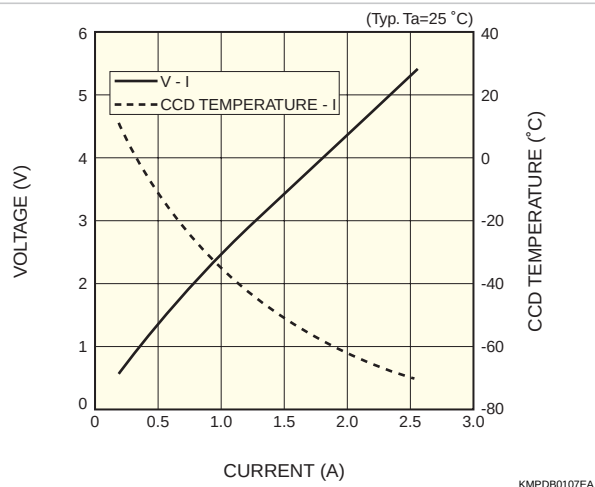
*20: If the current is greater than I_{max}, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not a damage threshold. To protect the thermoelectric cooler (Peltier element) and maintain stable operation, the supply current should be less than 60 % of this maximum current.

*21: Temperature at hot side of thermoelectric cooler.

*22: ΔT=Th - Tc

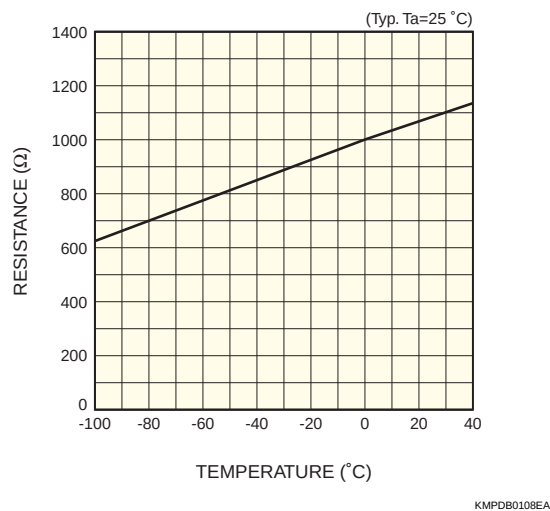
*23: This is a theoretical heat absorption level that offsets the temperature difference in the Peltier element when the maximum current is supplied to the unit.

*24: Temperature at cool side of thermoelectric cooler.



Specifications of built-in temperature sensors

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resistance at cool side	Rc	$T=0\text{ }^{\circ}\text{C}$	-	1,000	-	Ω
Temperature coefficient of resistance at cool side	-	-	-	0.00375	-	Ω/Ω
Resistance at hot side	Rh	$T=0\text{ }^{\circ}\text{C}$	-	1,000	-	Ω
Temperature coefficient of resistance at hot side	-	-	-	0.00385	-	Ω/Ω



Precaution for use (electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

Element cooling/heating temperature incline rate

Element cooling/heating temperature incline rate should be set at less than 5 K/min.

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HAMAMATSU PHOTONICS K.K., Solid State Division

1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81) 53-434-3311, Fax: (81) 53-434-5184, <http://www.hamamatsu.com>

U.S.A.: Hamamatsu Corporation: 360 Foothill Road, P.O.Box 6910, Bridgewater, N.J. 08807-0910, U.S.A., Telephone: (1) 908-231-0960, Fax: (1) 908-231-1218

Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49) 08152-3750, Fax: (49) 08152-2658

France: Hamamatsu Photonics France S.A.R.L.: 19, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: 33-(1) 69 53 71 00, Fax: 33-(1) 69 53 71 10

United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44) 1707-294888, Fax: (44) 1707-325777

North Europe: Hamamatsu Photonics Norden AB: Smidesvägen 12, SE-171 41 Solna, Sweden, Telephone: (46) 8-509-031-00, Fax: (46) 8-509-031-01

Italy: Hamamatsu Photonics Italia S.R.L.: Strada della Moia, 1/E, 20020 Arese, (Milano), Italy, Telephone: (39) 02-935-81-733, Fax: (39) 02-935-81-741