SN75LVDS83B FlatLink™ Transmitter

1 Features

- LVDS Display Series Interfaces Directly to LCD Display Panels With Integrated LVDS
- Package Options: 4.5-mm x 7-mm BGA, and 8.1-mm x 14-mm TSSOP
- 1.8-V Up to 3.3-V Tolerant Data Inputs to Connect Directly to Low-Power, Low-Voltage Application and Graphic Processors
- Transfer Rate up to 135 Mpps (Mega Pixel Per Second); Pixel Clock Frequency Range 10 MHz to 135 MHz
- Suited for Display Resolutions Ranging From HVGA up to HD With Low EMI
- Operates From a Single 3.3-V Supply and 170 mW (Typ.) at 75 MHz
- 28 Data Channels Plus Clock in Low-Voltage TTL to 4 Data Channels Plus Clock Out Low-Voltage Differential
- Consumes Less Than 1 mW When Disabled
- Selectable Rising or Falling Clock Edge Triggered Inputs
- ESD: 5-kV HBM
- Support Spread Spectrum Clocking (SSC)
- Compatible with all OMAP™ 2x, OMAP™ 3x, and DaVinci™ Application Processors

2 Applications

- LCD Display Panel Driver
- UMPC and Netbook PC
- Digital Picture Frame

3 Description

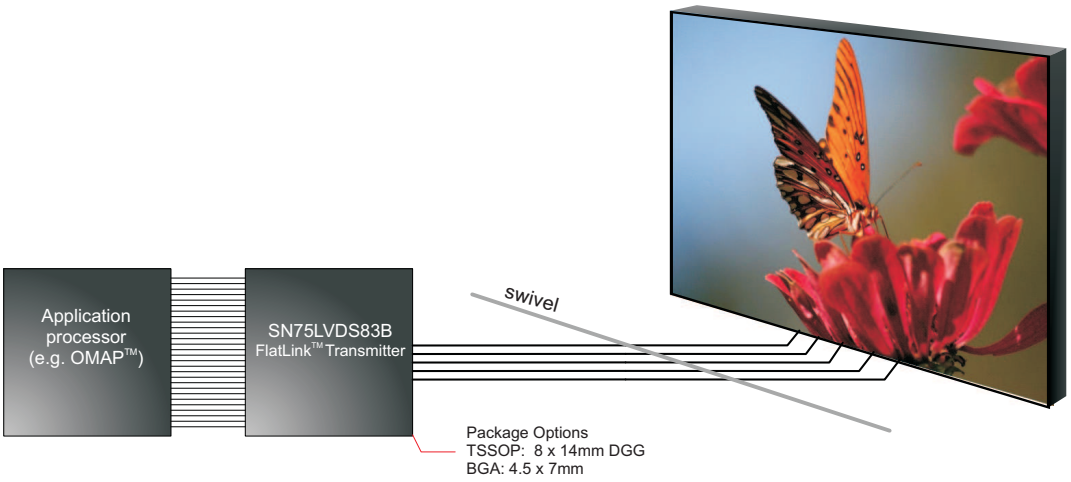
The SN75LVDS83B FlatLink™ transmitter contains four 7-bit parallel-load serial-out shift registers, a 7X clock synthesizer, and five Low-Voltage Differential Signaling (LVDS) line drivers in a single integrated circuit. These functions allow 28 bits of single-ended LVTTL data to be synchronously transmitted over five balanced-pair conductors for receipt by a compatible receiver, such as the SN75LVDS82 and LCD panels with integrated LVDS receiver.

When transmitting, data bits D0 through D27 are each loaded into registers upon the edge of the input clock signal (CLKIN). The rising or falling edge of the clock can be selected via the clock select (CLKSEL) pin. The frequency of CLKIN is multiplied seven times, and then used to unload the data registers in 7-bit slices and serially. The four serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN75LVDS83B	TSSOP (56)	14.00 mm x 5.10 mm
	BGA MICROSTAR JUNIOR (56)	7.00 mm x 4.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2011) to Revision C — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (October 2009) to Revision B — **Page**

- Added Storage temperature, T_s to ABSOLUTE MAXIMUM RATINGS ... 6
- Added Note 3 to DISSIPATION RATINGS ... 7
- Deleted max values for Supply current (average) ... 8
- Changed Enable time units from ns to µs ... 10
- Added Thermal Characteristics table ... 10
- Changed G7(LSB) to G7(MSB) in Figure 15 ... 21
- Added Note C to Figure 15 ... 21
- Added Note D to Figure 15 ... 21
- Added connection between GND and D23 to Figure 19 ... 25

Changes from Original (May 2009) to Revision A — **Page**

- Changed text and replaced TBDs in Note A and Note B of Figure 15 ... 21
- Changed Note B of Figure 16 - Replaced TBDs. ... 22
- Changed Note B of Figure 17 - Replaced TBDs. ... 23
- Changed Note C of Figure 18 - Replaced TBDs. ... 24
- Changed Figure 19 - removed 3 GND pin locations. ... 25
- Changed Figure 20 - removed 3 GND pin locations. ... 26

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5 Description (Continued)

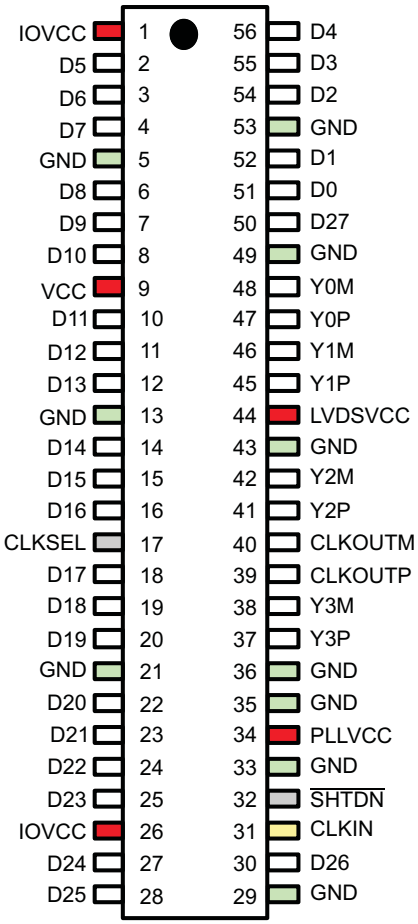
The SN75LVDS83B requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user intervention is selecting a clock rising edge by inputting a high level to CLKSEL or a falling edge with a low-level input, and the possible use of the Shutdown/Clear ($\overline{\text{SHTDN}}$). $\overline{\text{SHTDN}}$ is an active-low input to inhibit the clock, and shut off the LVDS output drivers for lower power consumption. A low-level on this signal clears all internal registers to a low-level.

The SN75LVDS83B is characterized for operation over ambient air temperatures of –10°C to 70°C.

Alternative device option: The SN75LVDS83A (SLLS980) is an alternative to the SN75LVDS83B for clock frequency range of 10MHz-100MHz only. The SN75LVDS83A is available in the TSSOP package option only.

6 Pin Configuration and Functions

56-PIN
DGG PACKAGE
(TOP VIEW)



DGG Pin List

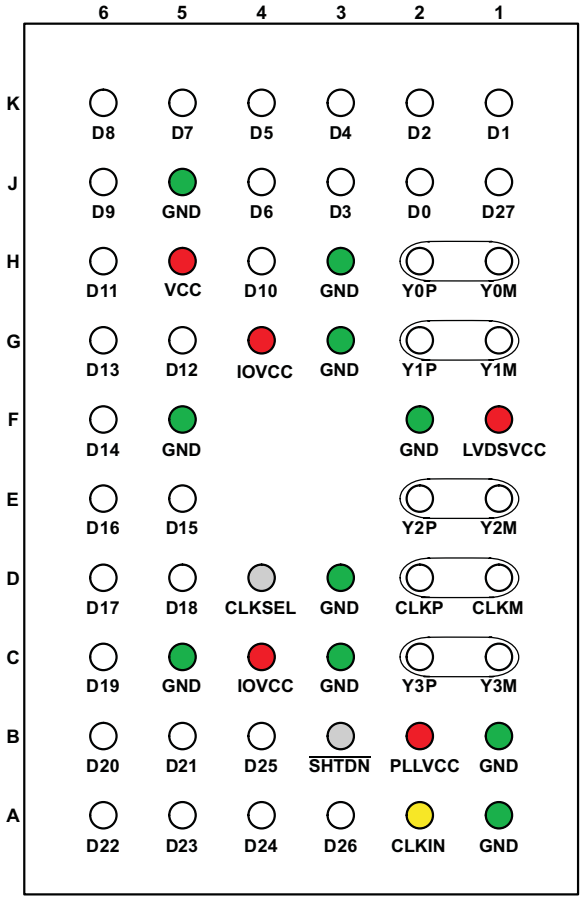
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	IOVCC	15	D15	29	GND	43	GND
2	D5	16	D16	30	D26	44	LVDSVCC
3	D6	17	CLKSEL	31	CLKIN	45	Y1P
4	D7	18	D17	32	$\overline{\text{SHTDN}}$	46	Y1M
5	GND	19	D18	33	GND	47	Y0P

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DGG Pin List (continued)

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
6	D8	20	D19	34	PLLVCC	48	Y0M
7	D9	21	GND	35	GND	49	GND
8	D10	22	D20	36	GND	50	D27
9	VCC	23	D21	37	Y3P	51	D0
10	D11	24	D22	38	Y3M	52	D1
11	D12	25	D23	39	CLKOUTP	53	GND
12	D13	26	IOVCC	40	CLKOUTM	54	D2
13	GND	27	D24	41	Y2P	55	D3
14	D14	28	D25	42	Y2M	56	D4

56-PIN
ZQL PACKAGE
(TOP VIEW)



ZQL Pin List

BALL	SIGNAL	BALL	SIGNAL	BALL	SIGNAL
A1	GND	A2	CLKIN	A3	D26
A4	D24	A5	D23	A6	D22
B1	GND	B2	PLLVCC	B3	$\overline{\text{SHTDN}}$
B4	D25	B5	D21	B6	D20
C1	Y3M	C2	Y3P	C3	GND
C4	IOVCC	C5	GND	C6	D19

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ZQL Pin List (continued)

BALL	SIGNAL	BALL	SIGNAL	BALL	SIGNAL
D1	CLKM	D2	CLKP	D3	GND
D4	CLKSEL	D5	D18	D6	D17
E1	Y2M	E2	Y2P	E3	ball not populated
E4	ball not populated	E5	D15	E6	D16
F1	LVDSVCC	F2	GND	F3	ball not populated
F4	ball not populated	F5	GND	F6	D14
G1	Y1M	G2	Y1P	G3	GND
G4	IOVCC	G5	D12	G6	D13
H1	Y0M	H2	Y0P	H3	GND
H4	D10	H5	VCC	H6	D11
J1	D27	J2	D0	J3	D3
J4	D6	J5	GND	J6	D9
K1	D1	K2	D2	K3	D4
K4	D5	K5	D7	K6	D8

Pin Functions

PIN	I/O	DESCRIPTION
Y0P, Y0M, Y1P, Y1M, Y2P, Y2M	LVDS Out	Differential LVDS data outputs. Outputs are high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted)
Y3P, Y3M		Differential LVDS Data outputs. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted). Note: if the application only requires 18-bit color, this output can be left open.
CLKP, CLKM		Differential LVDS pixel clock output. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted).
D0 – D27	CMOS IN with pulldn	Data inputs; supports 1.8 V to 3.3 V input voltage selectable by VDD supply. To connect a graphic source successfully to a display, the bit assignment of D[27:0] is critical (and not necessarily intuitive). For input bit assignment see Figure 15 to Figure 18 for details. Note: if application only requires 18-bit color, connect unused inputs D5, D10, D11, D16, D17, D23, and D27 to GND.
CLKIN		Input pixel clock; rising or falling clock polarity is selectable by Control input CLKSEL.
$\overline{\text{SHTDN}}$		Device shut down; pull low (de-assert) to shut down the device (low power, resets all registers) and high (assert) for normal operation.
CLKSEL		Selects between rising edge input clock trigger (CLKSEL = V_{IH}) and falling edge input clock trigger (CLKSEL = V_{IL}).
VCC	Power Supply(1)	3.3 V digital supply voltage
IOVCC		I/O supply reference voltage (1.8 V up to 3.3 V matching the GPU data output signal swing)
PLLVCC		3.3 V PLL analog supply
LVDSVCC		3.3 V LVDS output analog supply
GND		Supply ground for VCC, IOVCC, LVDSVCC, and PLLVCC.

(1) For a multilayer pcb, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

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7 Specifications

7.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Supply voltage range, VCC, IOVCC, LVDSVCC, PLLVCC(2)	–0.5	4	V
Voltage range at any output terminal	–0.5	VCC + 0.5	V
Voltage range at any input terminal	–0.5	IOVCC + 0.5	V
Continuous power dissipation	See *Dissipation Ratings*		

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) All voltages are with respect to the GND terminals.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human Body Model (HBM)(1) all pins		5	kV
		Charged Device Model (CDM)(2) all pins		500	V
		Machine Model (MM)(3) all pins		150	

(1) In accordance with JEDEC Standard 22, Test Method A114-A.
(2) In accordance with JEDEC Standard 22, Test Method C101.
(3) In accordance with JEDEC Standard 22, Test Method A115-A.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, VCC		3	3.3	3.6	V
LVDS output Supply voltage, LVDSVCC		3	3.3	3.6	
PLL analog supply voltage, PLLVCC		3	3.3	3.6	
IO input reference supply voltage, IOVCC		1.62	1.8 / 2.5 / 3.3	3.6	
Power supply noise on any VCC terminal				0.1	
High-level input voltage, V_{IH}	IOVCC = 1.8 V	IOVCC/2 + 0.3 V			V
	IOVCC = 2.5 V	IOVCC/2 + 0.4 V			
	IOVCC = 3.3 V	IOVCC/2 + 0.5 V			
Low-level input voltage, V_{IL}	IOVCC = 1.8 V			IOVCC/2 - 0.3 V	V
	IOVCC = 2.5 V			IOVCC/2 - 0.4 V	
	IOVCC = 3.3 V			IOVCC/2 - 0.5 V	
Differential load impedance, Z_L		90		132	Ω
Operating free-air temperature, T_A		–10		70	C

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7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ZQL			DGG			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
θ_{JA}	Junction-to-free-air thermal resistance	Low-K JEDEC test board, 1s (single signal layer), no air flow		85					°C/W
		High-K JEDEC test board, 2s2p (double signal layer, double buried power plane), no air flow		67.1			63.4		
θ_{JC}	Junction-to-case thermal resistance	Cu cold plate measurement process		25.2			15.9		°C/W
θ_{JB}	Junction-to-board thermal resistance	EIA/JESD 51-8		31.0			32.5		°C/W
ψ_{JT}	Junction-to-top of package	EIA/JESD 51-2		0.8			0.4		°C/W
ψ_{JB}	Junction-to-board	EIA/JESD 51-6		30.3			32.2		°C/W
T_A	Operating ambient temperature range		–10		70	–10		70	°C
T_J	Virtual junction temperature		0		105	0		105	°C

7.5 Dissipation Ratings

PACKAGE	CIRCUIT BOARD MODEL (1)	$T_{JA} \le 25°C$	DERATING FACTOR (2) ABOVE $T_{JA} = 25°C$	$T_{JA} = 70°C$ POWER RATING
DGG	Low-K	1111 mW	12.3 mW/°C	555 mW
ZQL		1034 mW	11.5 mW/°C	517 mW
DGG (3)	High-K	1730 mW	19 mW/°C	865 mW
ZQL		2000 mW	22 mW/°C	1000 mW

(1) In accordance with the High-K and Low-K thermal metric definitions of EIA/JESD51-2.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(3) DGG junction to case thermal resistance (θ_{JC}) is 15.4°C/W.

7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
V_T	Input voltage threshold	R_L = 100Ω, See Figure 7		IOVCC/2		V
$\lvert V_{OD}\rvert$	Differential steady-state output voltage magnitude		250		450	mV
$\Delta\lvert V_{OD}\rvert$	Change in the steady-state differential output voltage magnitude between opposite binary states			1	35	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 7 $t_{R/F}$ (Dx, CLKin) = 1ns	1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				35	mV
I_{IH}	High-level input current	V_{IH} = IOVCC			25	µA
I_{IL}	Low-level input current	V_{IL} = 0 V			±10	µA
I_{OS}	Short-circuit output current	V_{OY} = 0 V			±24	mA
		V_{OD} = 0 V			±12	mA
I_{OZ}	High-impedance state output current	V_O = 0 V to VCC			±20	µA
R_{pdn}	Input pull-down integrated resistor on all inputs (Dx, CLKSEL, $\overline{SHTDN}$, CLKIN)	IOVCC = 1.8 V		200		kΩ
		IOVCC = 3.3 V		100		
I_Q	Quiescent current (average)	disabled, all inputs at GND; $\overline{SHTDN}$ = V_{IL}		2	100	µA

(1) All typical values are at VCC = 3.3 V, T_A = 25°C.

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current (average)	$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), grayscale pattern (Figure 8) VCC = 3.3 V, f_{CLK} = 75 MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		51.9		mA
		$I_{(IOVCC)}$ with IOVCC = 3.3 V		0.4		
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.1		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), 50% transition density pattern (Figure 8), VCC = 3.3 V, f_{CLK} = 75 MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		53.3		mA
		$I_{(IOVCC)}$ with IOVCC = 3.3 V		0.6		
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.2		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), worst-case pattern (Figure 9), VCC = 3.6 V, f_{CLK} = 75 MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		63.7		mA
		$I_{(IOVCC)}$ with IOVCC = 3.3 V		1.3		
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.5		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), worst-case pattern (Figure 9), f_{CLK} = 100 MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		81.6		mA
		$I_{(IOVCC)}$ with IOVCC = 3.6 V		1.6		
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.6		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100Ω (5 places), worst-case pattern (Figure 9), f_{CLK} = 135 MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		102.2		mA
		$I_{(IOVCC)}$ with IOVCC = 3.6 V		2.1		
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.8		
C_I	Input capacitance			2		pF

7.7 Timing Requirements

PARAMETER		MIN	MAX	UNIT
Input clock period, t_c		7.4	100	ns
Input clock modulation	with modulation frequency 30 kHz		8%	
	with modulation frequency 50 kHz		6%	
High-level input clock pulse width duration, t_w		0.4 t_c	0.6 t_c	ns
Input signal transition time, t_t			3	ns
Data set up time, D0 through D27 before CLKIN (See Figure 6)		2		ns
Data hold time, D0 through D27 after CLKIN		0.8		ns

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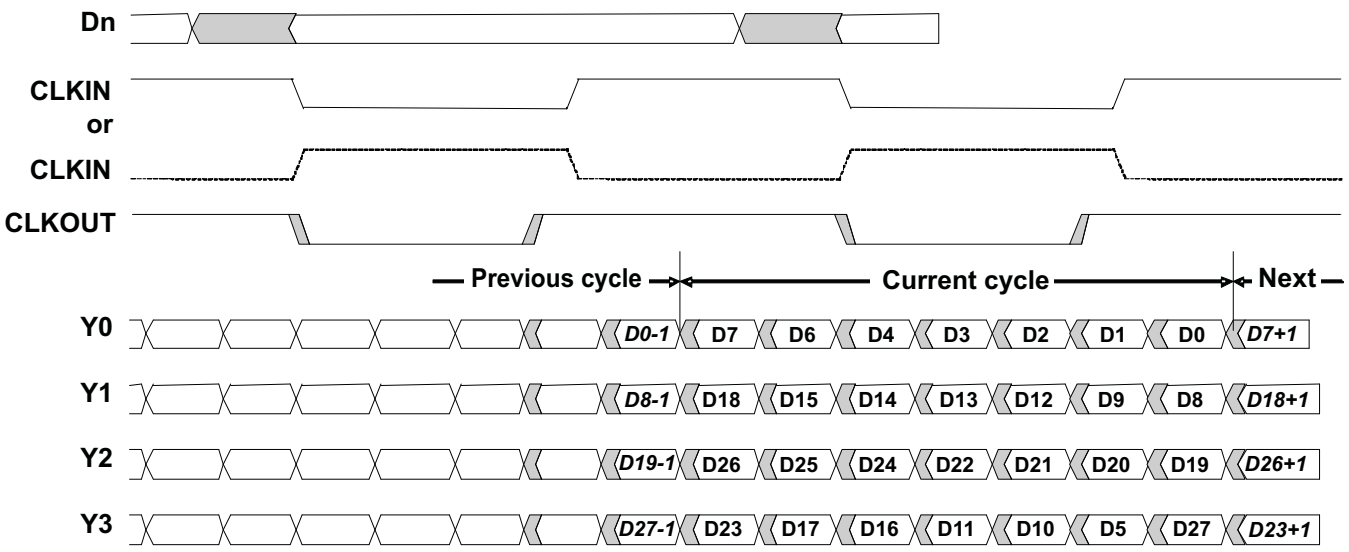


Figure 1. Typical SN75LVDS83B Load and Shift Sequences

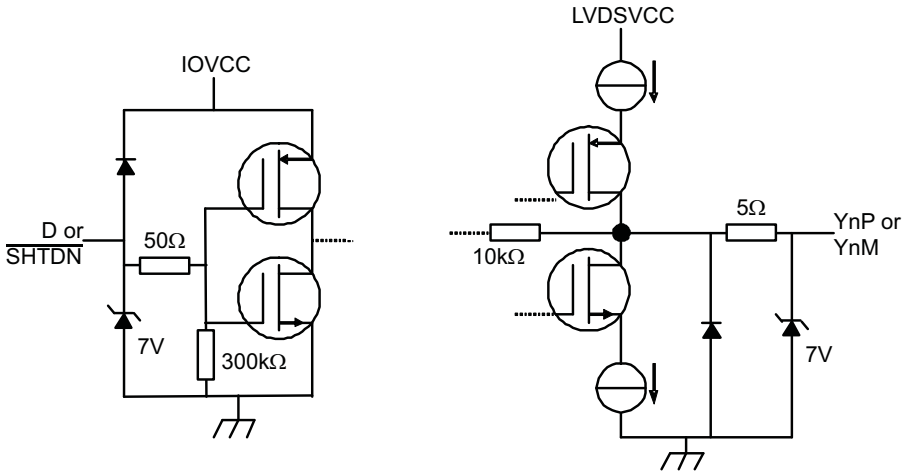


Figure 2. Equivalent Input and Output Schematic Diagrams

7.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_0	Delay time, CLKOUT↑ after Yn valid (serial bit position 0, equal D1, D9, D20, D5)	See Figure 10, t_C = 10ns, |Input clock jitter| < 25ps (2)	-0.1	0	0.1	ns
t_1	Delay time, CLKOUT↑ after Yn valid (serial bit position 1, equal D0, D8, D19, D27)		$^1/_7$ t_c - 0.1		$^1/_7$ t_c + 0.1	ns
t_2	Delay time, CLKOUT↑ after Yn valid (serial bit position 2, equal D7, D18, D26. D23)		$^2/_7$ t_c - 0.1		$^2/_7$ t_c + 0.1	ns
t_3	Delay time, CLKOUT↑ after Yn valid (serial bit position 3; equal D6, D15, D25, D17)		$^3/_7$ t_c - 0.1		$^3/_7$ t_c + 0.1	ns
t_4	Delay time, CLKOUT↑ after Yn valid (serial bit position 4, equal D4, D14, D24, D16)		$^4/_7$ t_c - 0.1		$^4/_7$ t_c + 0.1	ns
t_5	Delay time, CLKOUT↑ after Yn valid (serial bit position 5, equal D3, D13, D22, D11)		$^5/_7$ t_c - 0.1		$^5/_7$ t_c + 0.1	ns
t_6	Delay time, CLKOUT↑ after Yn valid (serial bit position 6, equal D2, D12, D21, D10)		$^6/_7$ t_c - 0.1		$^6/_7$ t_c + 0.1	ns
$t_{c(o)}$	Output clock period			t_c		ns
$\Delta t_{c(o)}$	Output clock cycle-to-cycle jitter (3)	t_C = 10ns; clean reference clock, see Figure 11		±26		ps
		t_C = 10ns with 0.05UI added noise modulated at 3MHz, see Figure 11		±44		
		t_C = 7.4ns; clean reference clock, see Figure 11		±35		
		t_C = 7.4ns with 0.05UI added noise modulated at 3MHz, see Figure 11		±42		
t_w	High-level output clock pulse duration			$^4/_7$ t_c		ns
$t_{r/f}$	Differential output voltage transition time (t_r or t_f)	See Figure 7		225	500	ps
t_{en}	Enable time, $\overline{SHTDN}$↑ to phase lock (Yn valid)	$f_{(clk)}$ = 135 MHz, See Figure 12		6		µs
t_{dis}	Disable time, $\overline{SHTDN}$↓ to off-state (CLKOUT high-impedance)	$f_{(clk)}$ = 135 MHz, See Figure 13		7		ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) |Input clock jitter| is the magnitude of the change in the input clock period.
(3) The output clock cycle-to-cycle jitter is the largest recorded change in the output clock period from one cycle to the next cycle observed over 15,000 cycles.Tektronix TDSJIT3 Jitter Analysis software was used to derive the maximum and minimum jitter value.

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7.9 Typical Characteristics

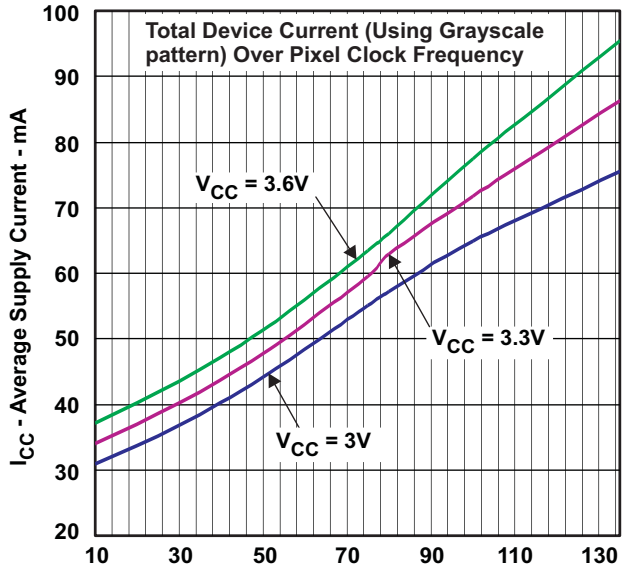


Figure 3. Average Grayscale I_{CC} vs Clock Frequency

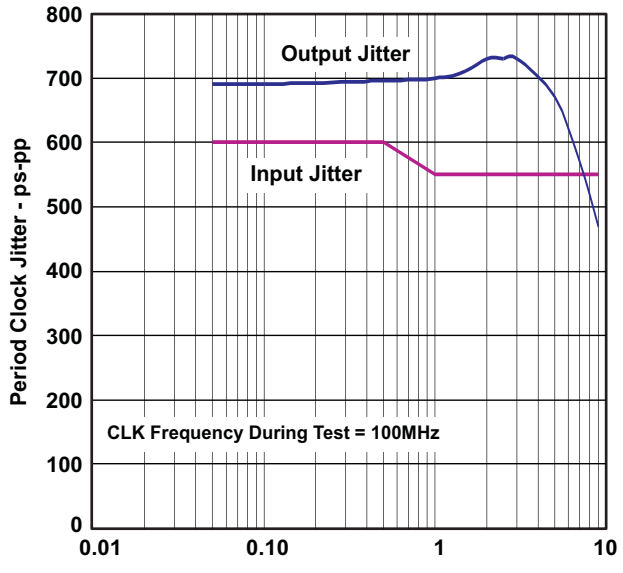


Figure 4. Output Clock Jitter vs Input Clock Jitter

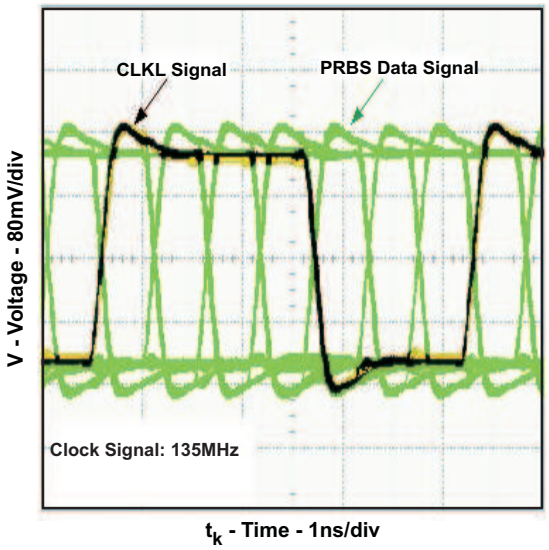
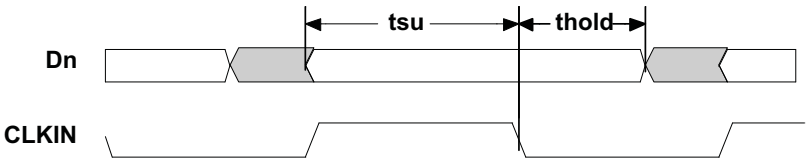


Figure 5. Typical PRBS Output Signal Over One Clock Period

8 Parameter Measurement Information



All input timing is defined at IOVDD / 2 on an input signal with a 10% to 90% rise or fall time of less than 3 ns. CLKSEL = 0 V.

Figure 6. Set Up and Hold Time Definition

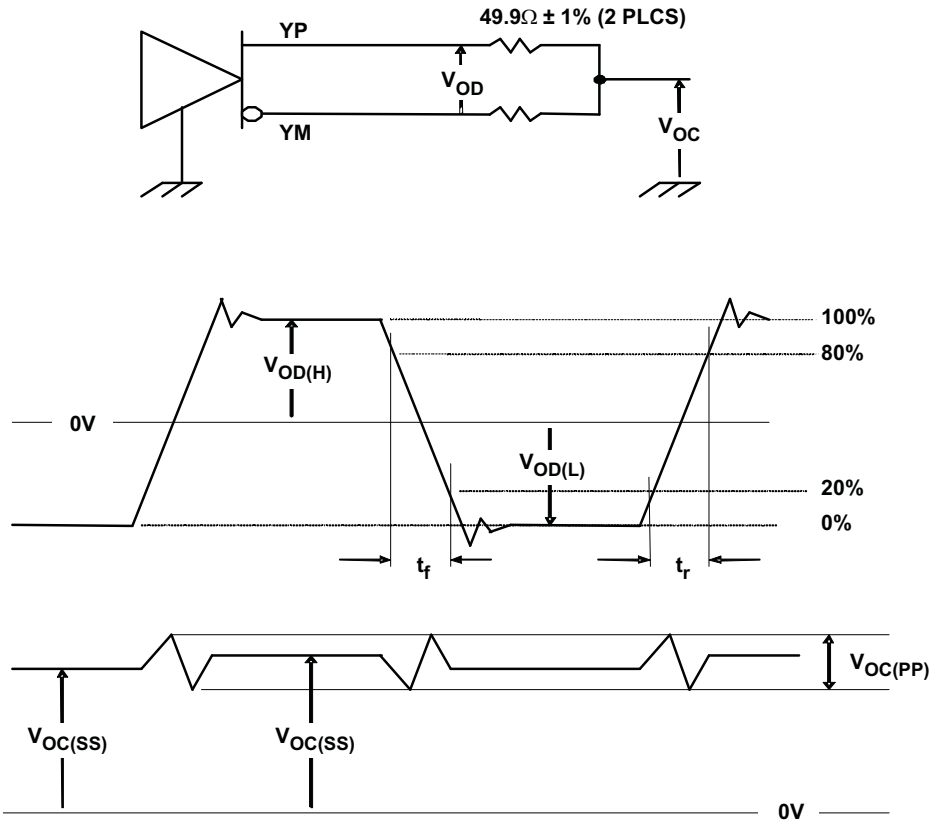
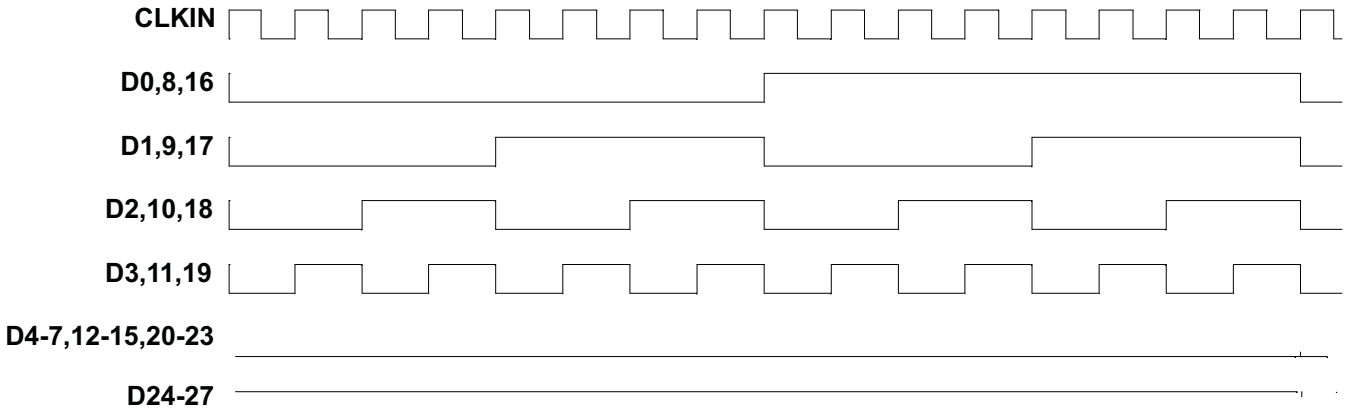


Figure 7. Test Load and Voltage Definitions for LVDS Outputs

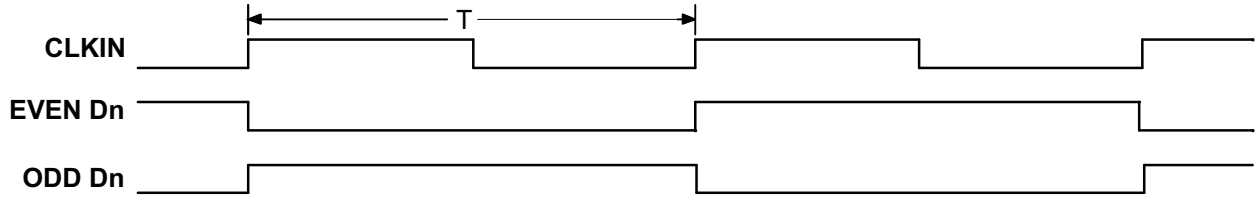
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Parameter Measurement Information (continued)



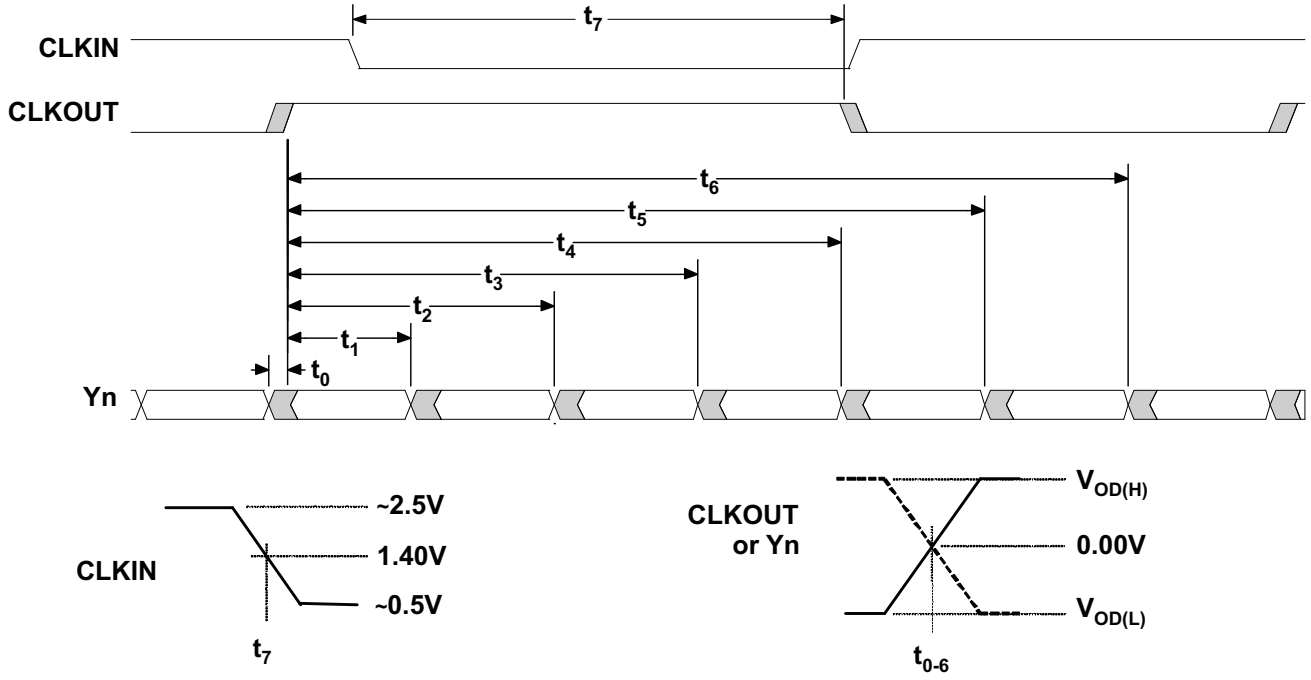
The 16 grayscale test pattern test device power consumption for a typical display pattern.

Figure 8. 16 Grayscale Test Pattern



The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs.

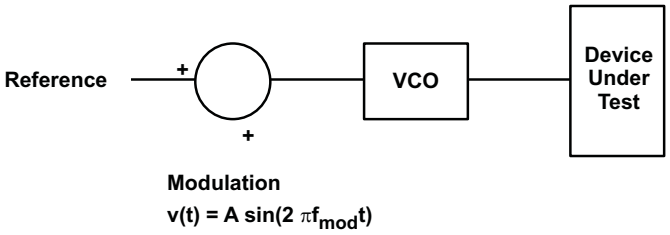
Figure 9. Worst-Case Power Test Pattern



CLKOUT is shown with CLKSEL at high-level.
CLKIN polarity depends on CLKSEL input level.

Figure 10. SN75LVDS83B Timing Definitions

Parameter Measurement Information (continued)



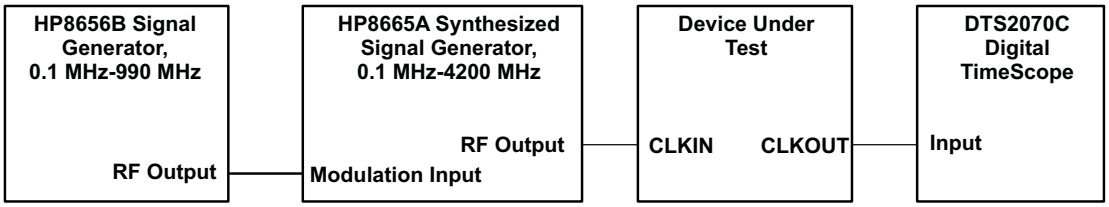


Figure 11. Output Clock Jitter Test Set Up

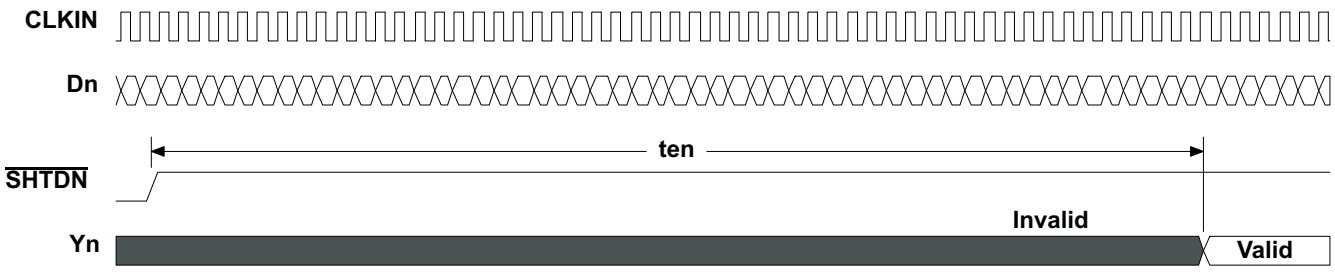


Figure 12. Enable Time Waveforms

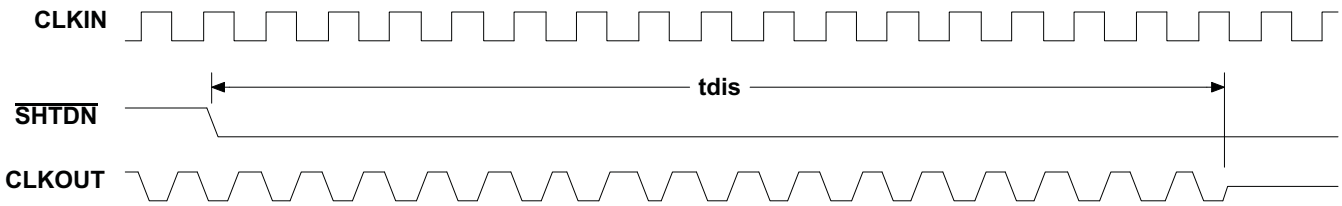


Figure 13. Disable Time Waveforms

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9 Detailed Description

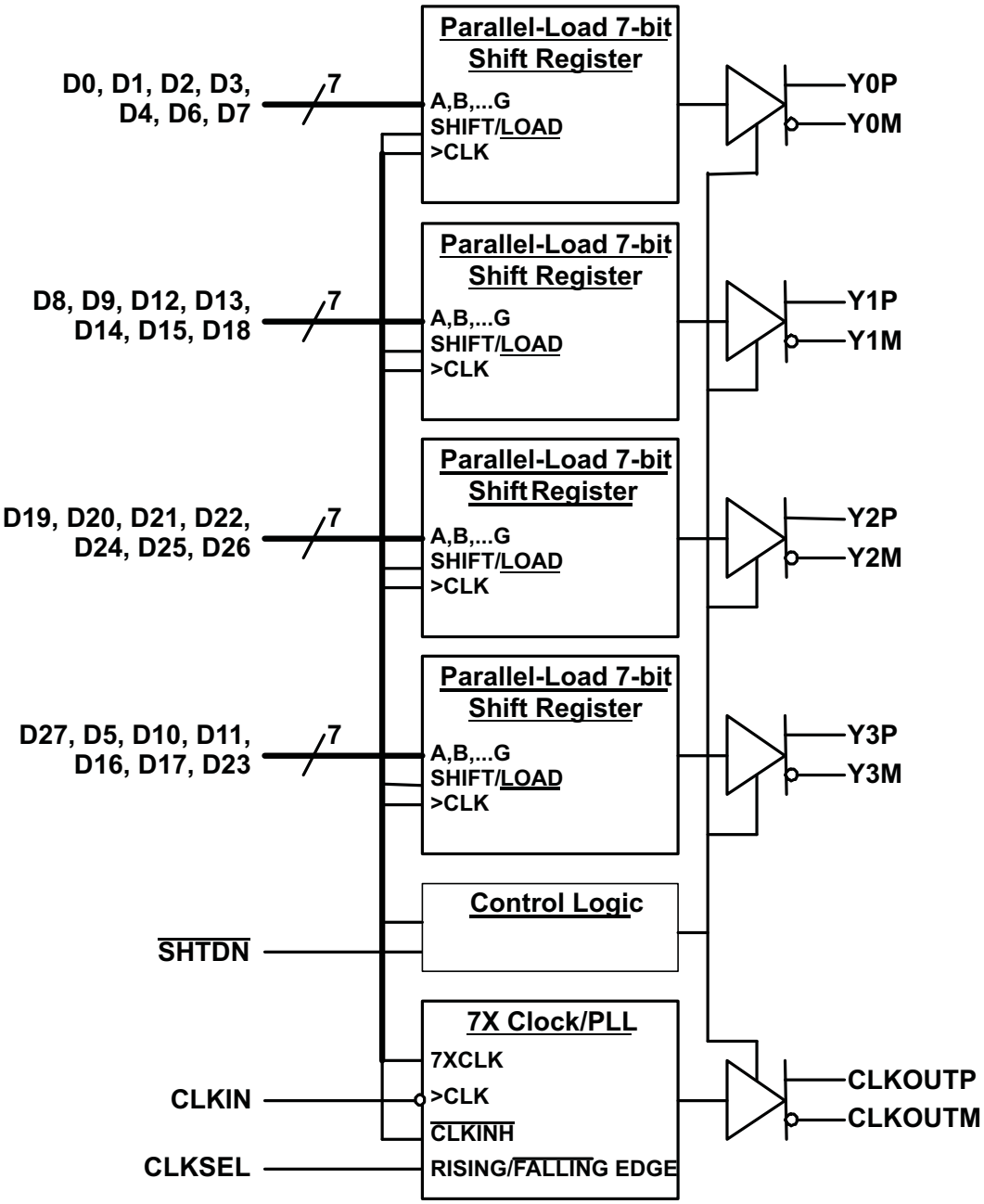
9.1 Overview

FlatLink™ is an LVDS SerDes data transmission system. The SN75LVDS83B takes in three (or four) data words each containing seven single-ended data bits and converts this to an LVDS serial output. Each serial output runs at seven times that of the parallel data rate. The deserializer (receiver) device operates in the reverse manner. The three (or four) LVDS serial inputs are transformed back to the original seven-bit parallel single-ended data. FlatLink™ devices are available in 21:3 or 28:4 SerDes ratios.

- The 21-bit devices are designed for 6-bit RGB video for a total of 18 bits in addition to three extra bits for horizontal synchronization, vertical synchronization, and data enable.
- The 28-bit devices are intended for 8-bit RGB video applications. Again, the extra four bits are for horizontal synchronization, vertical synchronization, data enable, and the remaining is the reserved bit. These 28-bit devices can also be used in 6-bit and 4-bit RGB applications as shown in the subsequent system diagrams.

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9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 TTL Input Data

The data inputs to the transmitter come from the graphics processor and consist of up to 24 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, an enable bit, and a spare bit. The data can be loaded into the registers upon either the rising or falling edge of the input clock selectable by the CLKSEL pin. Data inputs are 1.8 V to 3.3 V tolerant for the SN75LVDS83B and can connect directly to low-power, low-voltage application and graphic processors. The bit mapping is listed in Table 1.

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Feature Description (continued)

Table 1. Pixel Bit Ordering

	RED	GREEN	BLUE
LSB	R0	G0	B0
	R1	G1	B1
	R2	G2	B2
4-bit MSB	R3	G3	B3
	R4	G4	B4
6-bit MSB	R5	G5	B5
	R6	G6	B6
8-bit MSB	R7	G7	B7

9.3.2 LVDS Output Data

The pixel data assignment is listed in Table 2 for 24-bit, 18-bit, and 12-bit color hosts.

Table 2. Pixel Data Assignment

SERIAL CHANNEL	DATA BITS	8-BIT			6-BIT	4-BIT	
		FORMAT-1	FORMAT-2	FORMAT-3		NON-LINEAR STEP SIZE	LINEAR STEP SIZE
Y0	D0	R0D27	R2	R2	R0	R2	VCC
	D1	R1	R3	R3	R1	R3	GND
	D2	R2	R4	R4	R2	R0	R0
	D3	R3	R5	R5	R3	R1	R1
	D4	R4	R6	R6	R4	R2	R2
	D6	R5	R7	R7	R5	R3	R3
	D7	G0	G2	G2	G0	G2	VCC
Y1	D8	G1	G3	G3	G1	G3	GND
	D9	G2	G4	G4	G2	G0	G0
	D12	G3	G5	G5	G3	G1	G1
	D13	G4	G6	G6	G4	G2	G2
	D14	G5	G7	G7	G5	G3	G3
	D15	B0	B2	B2	B0	B2	VCC
	D18	B1	B3	B3	B1	B3	GND
Y2	D19	B2	B4	B4	B2	B0	B0
	D20	B3	B5	B5	B3	B1	B1
	D21	B4	B6	B6	B4	B2	B2
	D22	B5	B7	B7	B5	B3	B3
	D24	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
	D25	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
	D26	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
Y3	D27	R6	R0	GND	GND	GND	GND
	D5	R7	R1	GND	GND	GND	GND
	D10	G6	G0	GND	GND	GND	GND
	D11	G7	G1	GND	GND	GND	GND
	D16	B6	B0	GND	GND	GND	GND
	D17	B7	B1	GND	GND	GND	GND
	D23	RSVD	RSVD	GND	GND	GND	GND
CLKOUT	CLKIN	CLK	CLK	CLK	CLK	CLK	CLK

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9.4 Device Functional Modes

9.4.1 Input Clock Edge

The transmission of data bits D0 through D27 occurs as each are loaded into registers upon the edge of the CLKIN signal, where the rising or falling edge of the clock may be selected via CLKSEL. The selection of a clock rising edge occurs by inputting a high level to CLKSEL, which is achieved by populating pull-up resistor to pull CLKSEL=high. Inputting a low level to select a clock falling edge is achieved by directly connecting CLKSEL to GND.

9.4.2 Low Power Mode

The SN75LVDS83B can be put in low-power consumption mode by active-low input SHTDN#. Connecting pin SHTDN# to GND will inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low-level on this signal clears all internal registers to a low-level. Populate a pull-up to VCC on SHTDN# to enable the device for normal operation.

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10 Application and Implementation

10.1 Application Information

This section describes the power up sequence, provides information on device connectivity to various GPU and LCD display panels, and offers a PCB routing example.

10.2 Typical Application

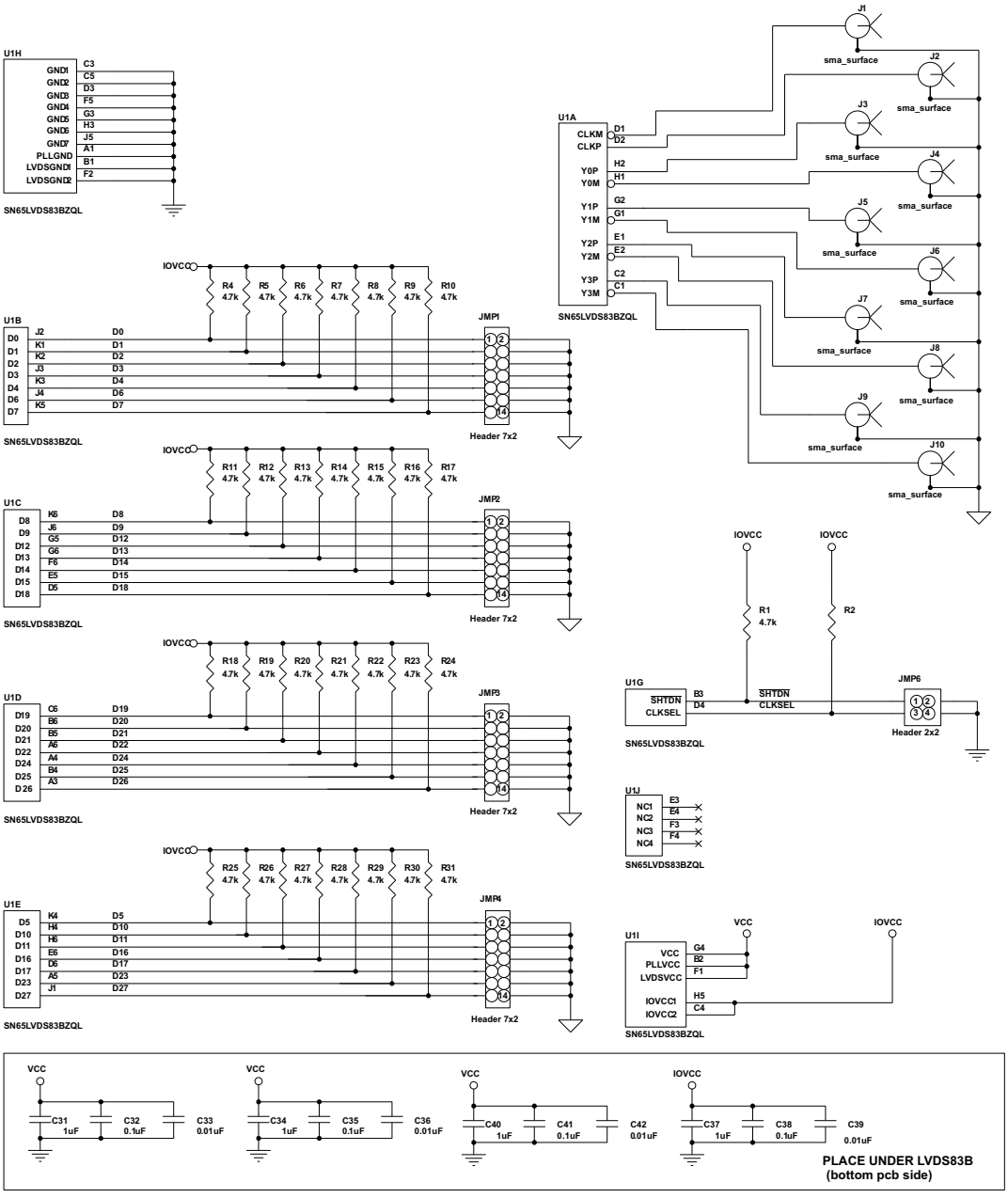


Figure 14. Schematic Example (SN75LVDS83B Evaluation Board)

Typical Application (continued)

10.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
VCC	3.3 V
VCCIO	1.8 V
CLKIN	Falling edge
SHTDN#	High
Format	18-bit GPU to 24-bit LCD

10.2.2 Detailed Design Procedure

10.2.2.1 Power Up Sequence

The SN75LVDS83B does not require a specific power up sequence.

It is permitted to power up IOVCC while VCC, VCCPLL, and VCCLVDS remain powered down and connected to GND. The input level of the $\overline{\text{SHTDN}}$ during this time does not matter as only the input stage is powered up while all other device blocks are still powered down.

It is also permitted to power up all 3.3V power domains while IOVCC is still powered down to GND. The device will not suffer damage. However, in this case, all the I/Os are detected as logic HIGH, regardless of their true input voltage level. Hence, connecting $\overline{\text{SHTDN}}$ to GND will still be interpreted as a logic HIGH; the LVDS output stage will turn on. The power consumption in this condition is significantly higher than standby mode, but still lower than normal mode.

The user experience can be impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended:

Power up sequence (SN75LVDS83B $\overline{\text{SHTDN}}$ input initially low):

1. Ramp up LCD power (maybe 0.5ms to 10ms) but keep backlight turned off.
2. Wait for additional 0-200ms to ensure display noise won't occur.
3. Enable video source output; start sending black video data.
4. Toggle LVDS83B shutdown to $\overline{\text{SHTDN}} = V_{IH}$.
5. Send >1ms of black video data; this allows the LVDS83B to be phase locked, and the display to show black data first.
6. Start sending true image data.
7. Enable backlight.

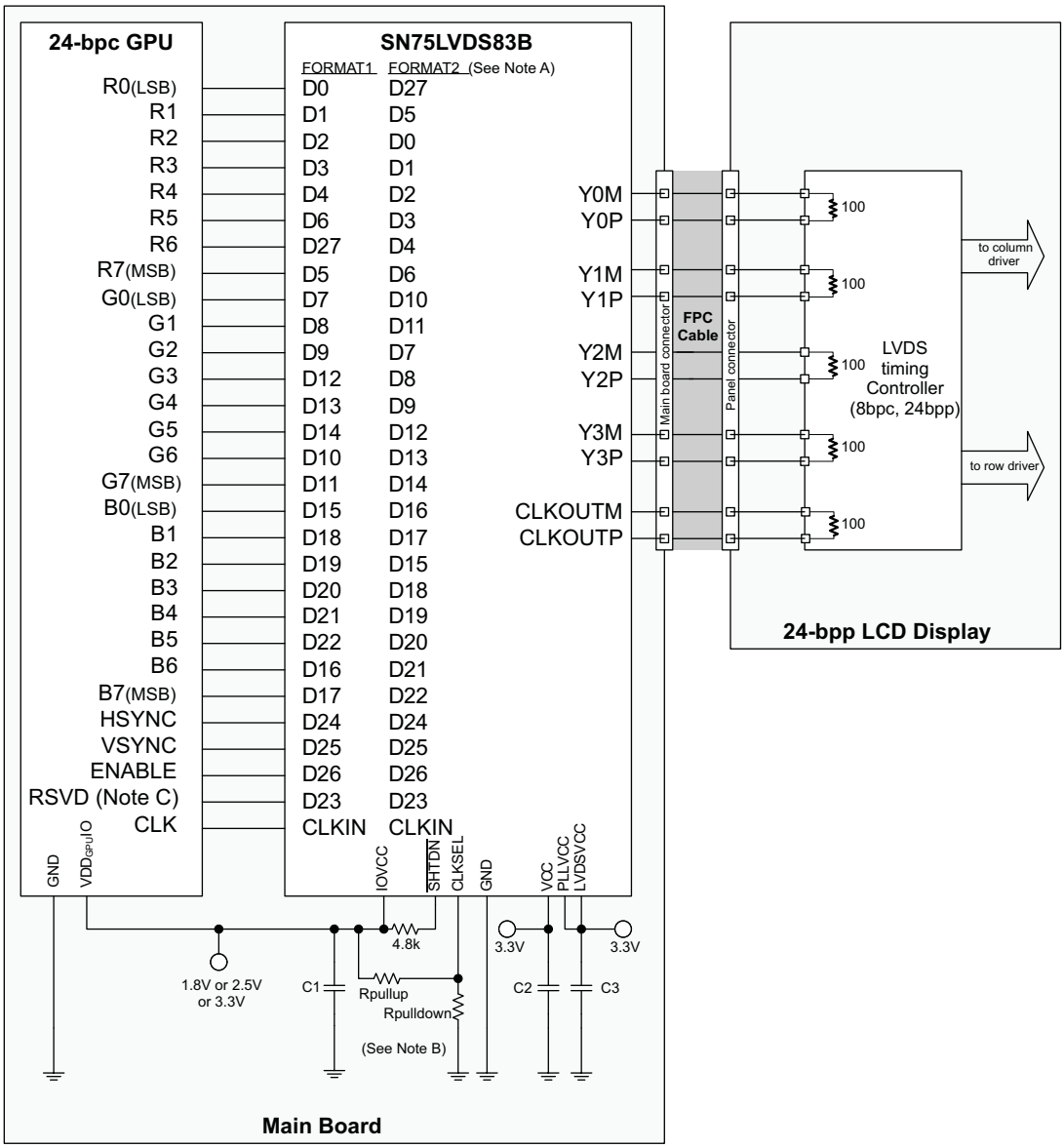
Power Down sequence (SN75LVDS83B $\overline{\text{SHTDN}}$ input initially high):

1. Disable LCD backlight; wait for the minimum time specified in the LCD data sheet for the backlight to go low.
2. Video source output data switch from active video data to black image data (all visible pixel turn black); drive this for >2 frame times.
3. Set SN75LVDS83B input $\overline{\text{SHTDN}}$ = GND; wait for 250ns.
4. Disable the video output of the video source.
5. Remove power from the LCD panel for lowest system power.

10.2.2.2 Signal Connectivity

While there is no formal industry standardized specification for the input interface of LVDS LCD panels, the industry has aligned over the years on a certain data format (bit order). Figure 15 through Figure 18 show how each signal should be connected from the graphic source through the SN75LVDS83B input, output and LVDS LCD panel input. Detailed notes are provided with each figure.

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Note A. **FORMAT**: The majority of 24-bit LCD display panels require the two most significant bits (2 MSB) of each color to be transferred over the 4th serial data output Y3. A few 24-bit LCD display panels require the two LSBs of each color to be transmitted over the Y3 output. The system designer needs to verify which format is expected by checking the LCD display data sheet.

- Format 1: use with displays expecting the 2 MSB to be transmitted over the 4th data channel Y3. This is the dominate data format for LCD panels.
- Format 2: use with displays expecting the 2 LSB to be transmitted over the 4th data channel.

Note B. **Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

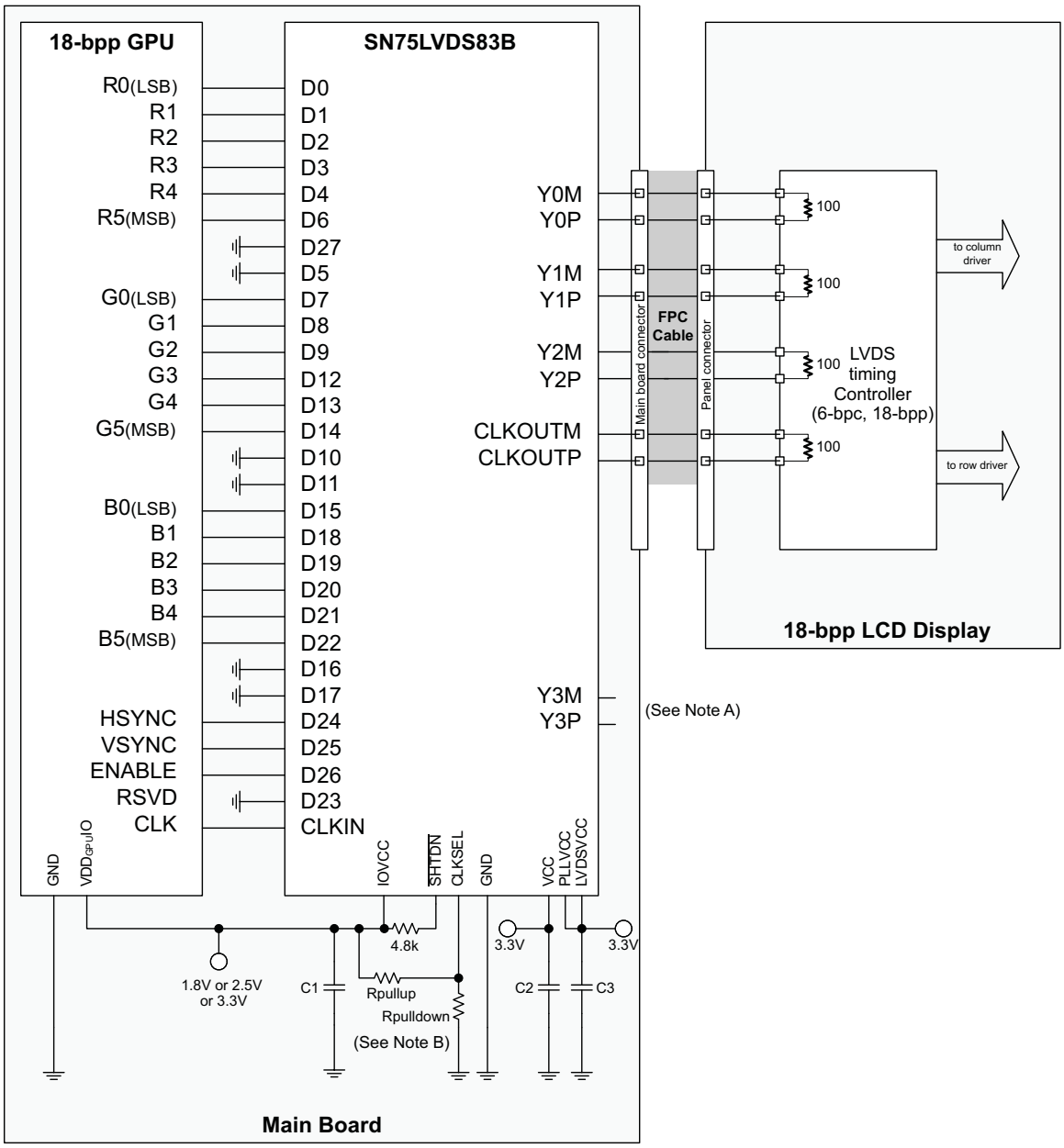
- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Note C. If RSVD is not driven to a valid logic level, then an external connection to GND is recommended.

Note D. RSVD must be driven to a valid logic level. All unused SN75LVDS83B inputs must be tied to a valid logic level.

Figure 15. 24-Bit Color Host to 24-Bit LCD Panel Application

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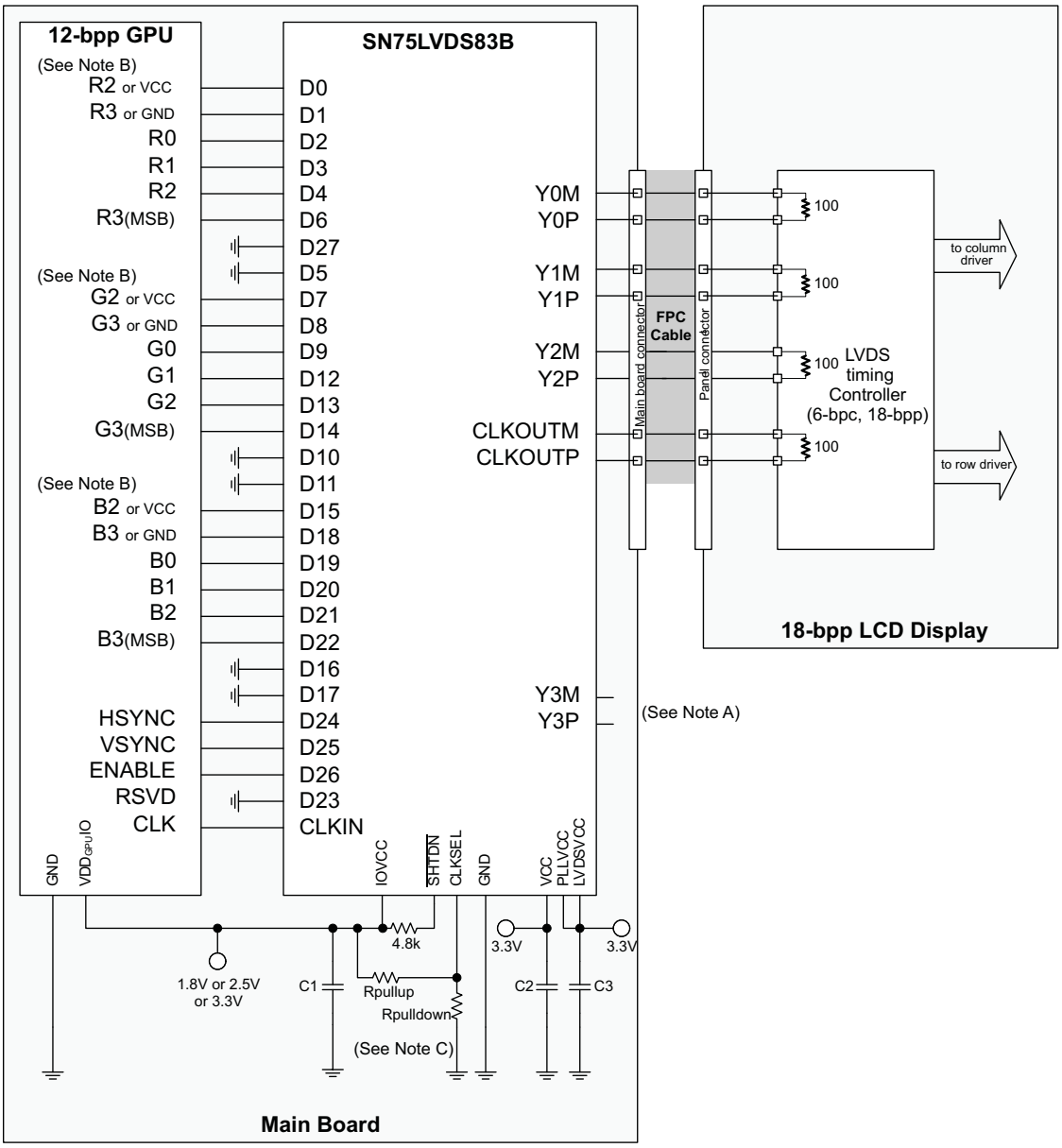
Note A. Leave output Y3 NC.

Note B.**Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Figure 16. 18-Bit Color Host to 18-Bit Color LCD Panel Display Application

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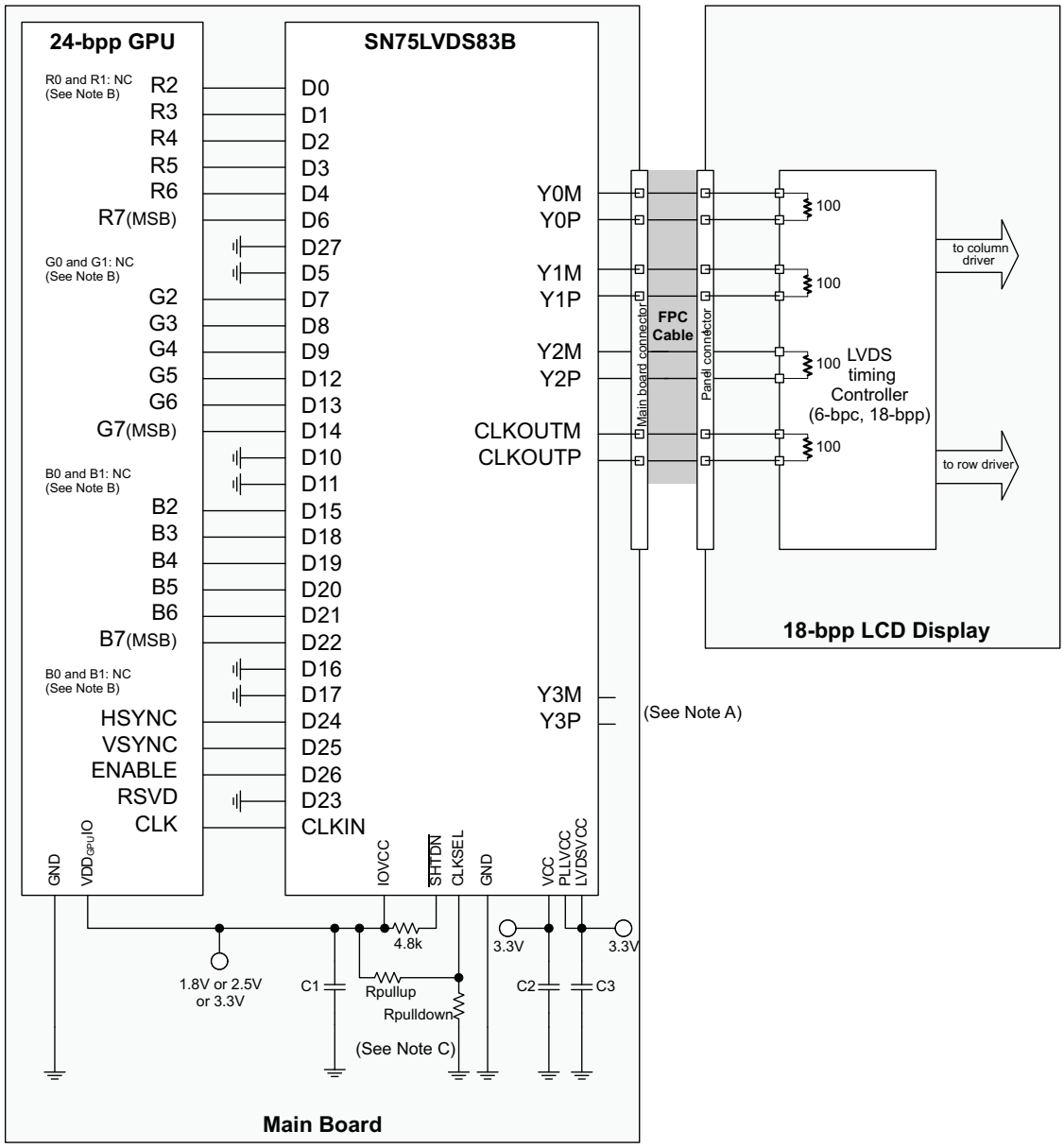
Note A. Leave output Y3 N.C.

Note B. **R3, G3, B3**: this MSB of each color also connects to the 5th bit of each color for increased dynamic range of the entire color space at the expense of none-linear step sizes between each step. For linear steps with less dynamic range, connect D1, D8, and D18 to GND.
R2, G2, B2: these outputs also connects to the LSB of each color for increased, dynamic range of the entire color space at the expense of none-linear step sizes between each step. For linear steps with less dynamic range, connect D0, D7, and D15 to VCC.

Note C.**Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Figure 17. 12-Bit Color Host to 18-Bit Color LCD Panel Display Application



Note A. Leave output Y3 NC.

Note B. **R0, R1, G0, G1, B0, B1**: For improved image quality, the GPU should dither the 24-bit output pixel down to18-bit per pixel.

NoteC.**Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling cap for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling cap for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling cap for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Figure 18. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application

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10.2.2.3 PCB Routing

Figure 19 and Figure 20 show a possible breakout of the data input and output signals from the BGA package.

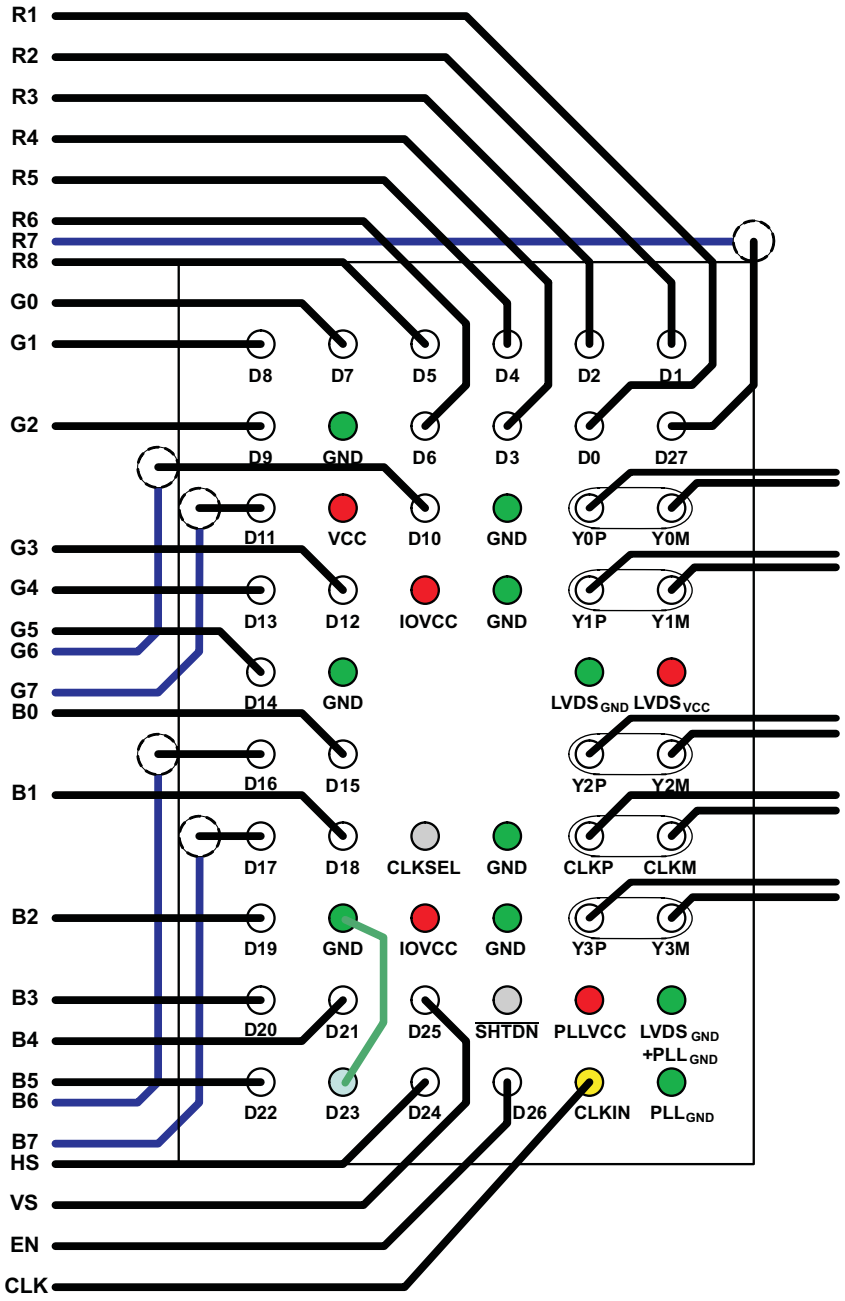


Figure 19. 24-Bit Color Routing (See Figure 15 for the Schematic)

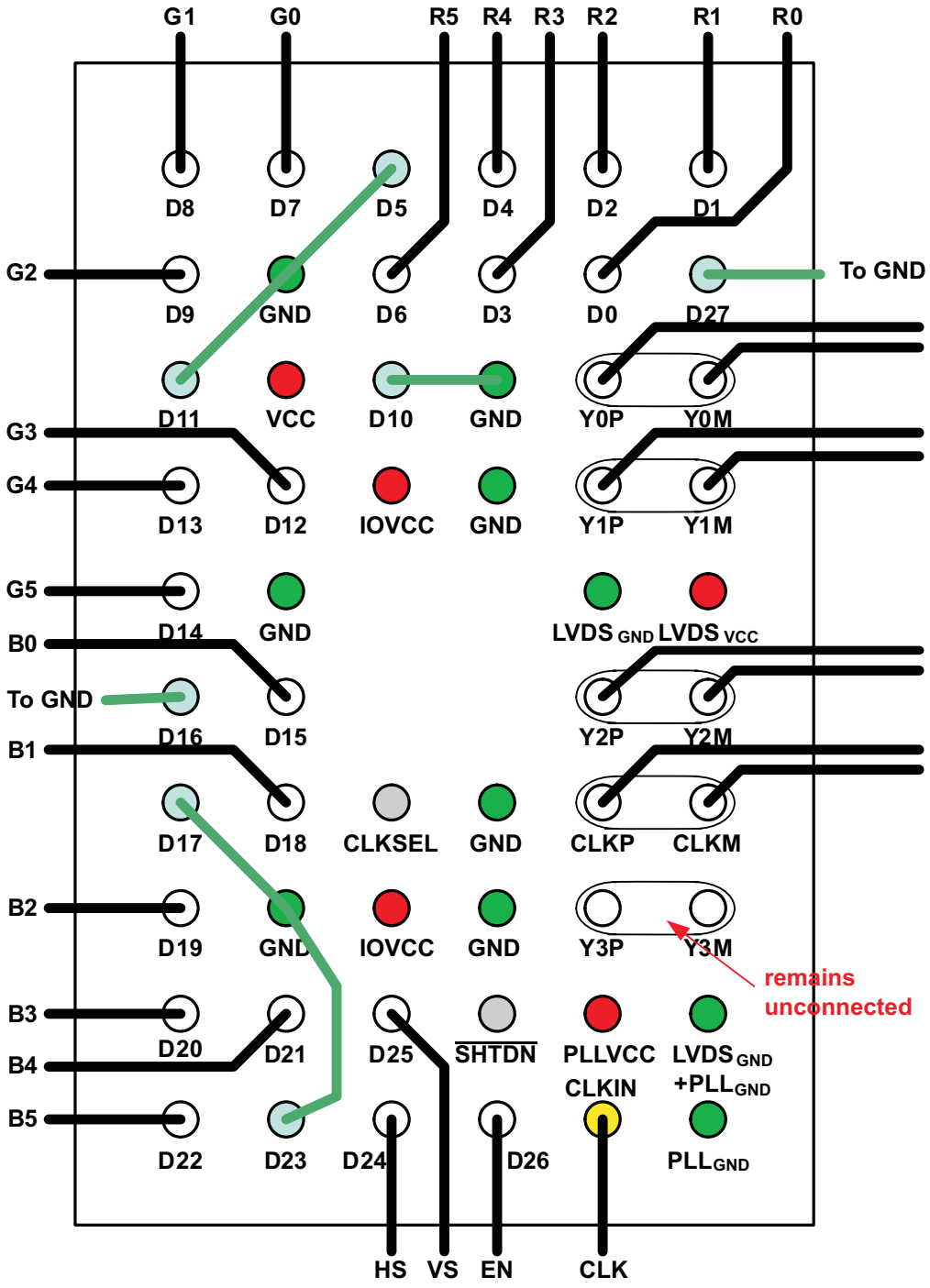


Figure 20. 18-Bit Color Routing (See Figure 16, Figure 17, and Figure 18 for the Schematic)

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10.2.3 Application Curve

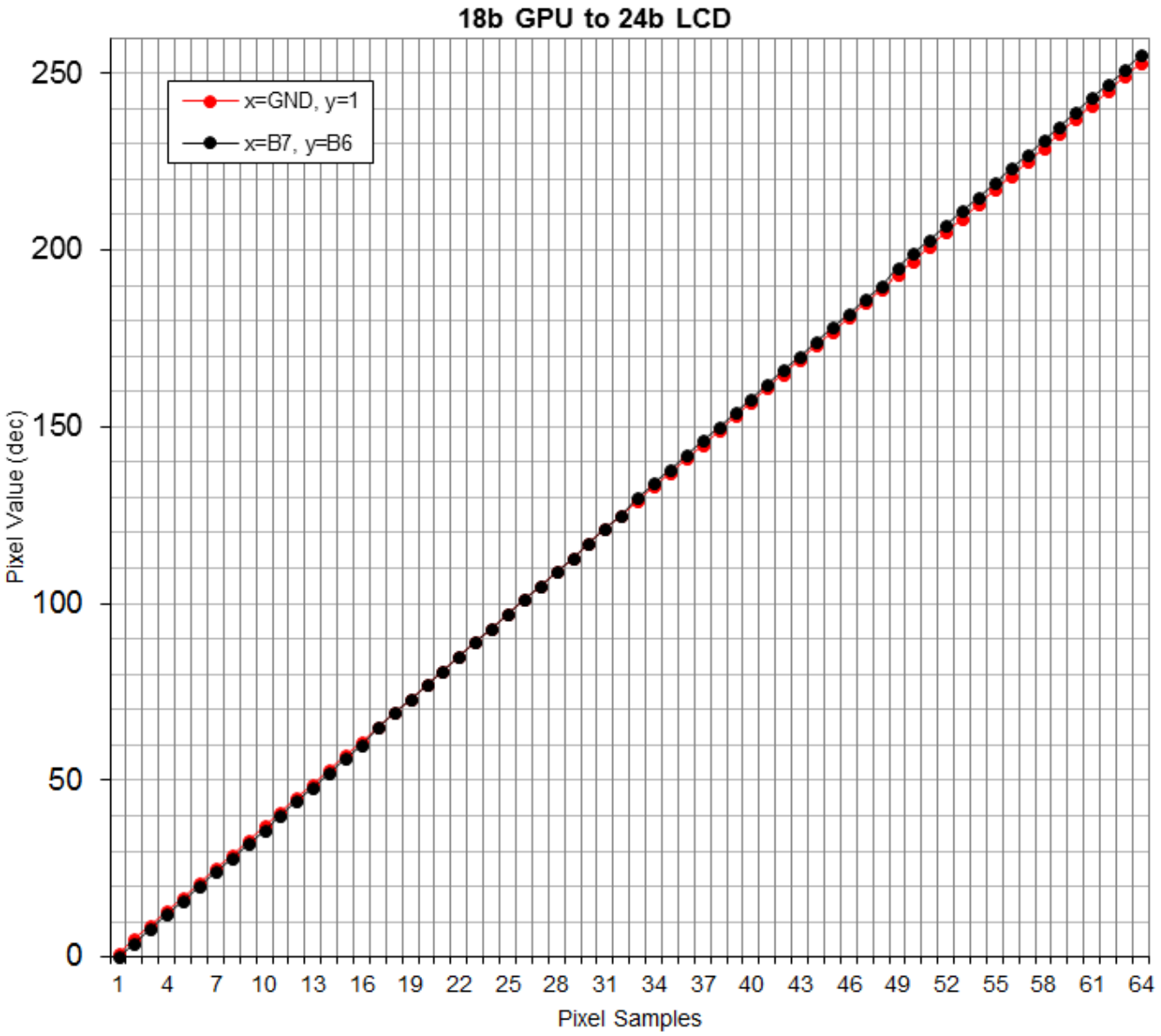


Figure 21. 18b GPU to 24b LCD

11 Power Supply Recommendations

Power supply PLL, IO, and LVDS pins must be uncoupled from each.

12 Layout

12.1 Layout Guidelines

12.1.1 Board Stackup

There is no fundamental information about how many layers should be used and how the board stackup should look. Again, the easiest way the get good results is to use the design from the EVMs of Texas Instruments. The magazine *Elektronik Praxis* has published an article with an analysis of different board stackups. These are listed in Table 3. Generally, the use of microstrip traces needs at least two layers, whereas one of them must be a GND plane. Better is the use of a four-layer PCB, with a GND and a VCC plane and two signal layers. If the circuit is complex and signals must be routed as stripline, because of propagation delay and/or characteristic impedance, a six-layer stackup should be used.

Table 3. Possible Board Stackup on a Four-Layer PCB

	MODEL 1	MODEL 2	MODEL 3	MODEL 4
Layer 1	SIG	SIG	SIG	GND
Layer 2	SIG	GND	GND	SIG
Layer 3	VCC	VCC	SIG	VCC
Layer 4	GND	SIG	VCC	SIG
Decoupling	Good	Good	Bad	Bad
EMC	Bad	Bad	Bad	Bad
Signal Integrity	Bad	Bad	Good	Bad
Self Disturbance	Satisfaction	Satisfaction	Satisfaction	High

12.1.2 Power and Ground Planes

A complete ground plane in high-speed design is essential. Additionally, a complete power plane is recommended as well. In a complex system, several regulated voltages can be present. The best solution is for every voltage to have its own layer and its own ground plane. But this would result in a huge number of layers just for ground and supply voltages. What are the alternatives? Split the ground planes and the power planes? In a mixed-signal design, e.g., using data converters, the manufacturer often recommends splitting the analog ground and the digital ground to avoid noise coupling between the digital part and the sensitive analog part. Take care when using split ground planes because:

- Split ground planes act as slot antennas and radiate.
- A routed trace over a gap creates large loop areas, because the return current cannot flow beside the signal, and the signal can induce noise into the nonrelated reference plane (Figure 22).
- With a proper signal routing, crosstalk also can arise in the return current path due to discontinuities in the ground plane. Always take care of the return current (Figure 23).

For Figure 23, do not route a signal referenced to digital ground over analog ground and vice versa. The return current cannot take the direct way along the signal trace and so a loop area occurs. Furthermore, the signal induces noise, due to crosstalk (dotted red line) into the analog ground plane.

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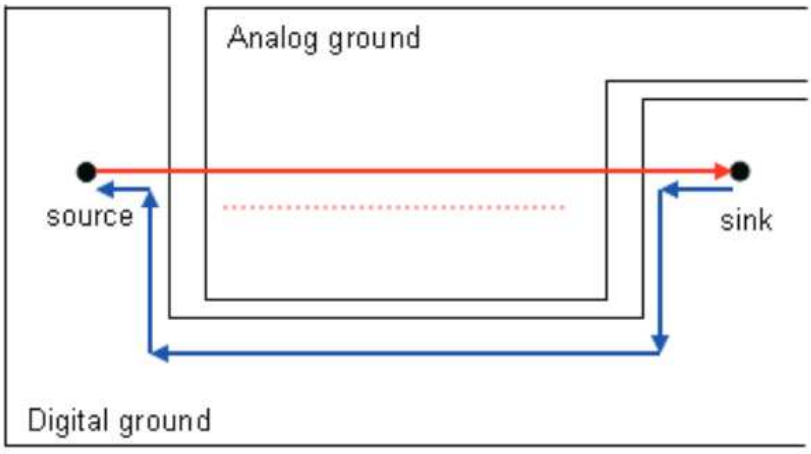


Figure 22. Loop Area and Crosstalk Due to Poor Signal Routing and Ground Splitting

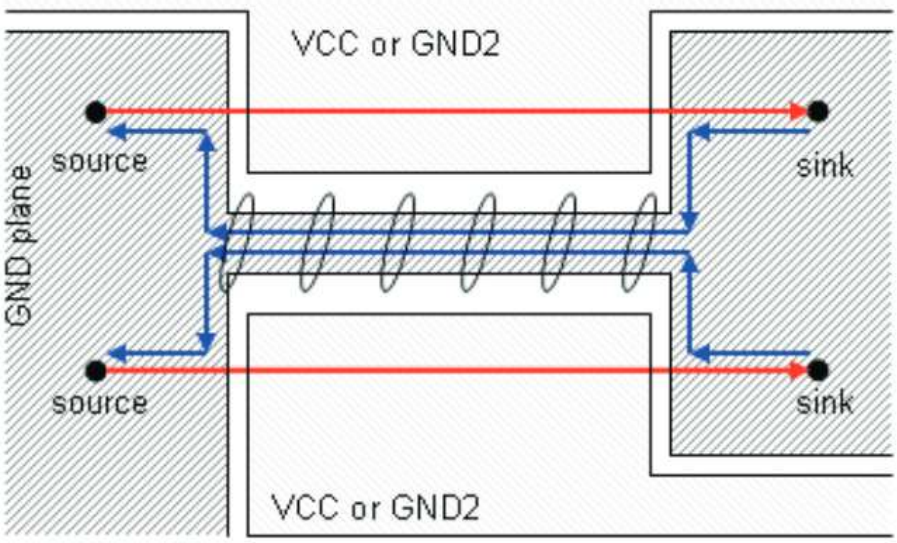


Figure 23. Crosstalk Induced by the Return Current Path

12.1.3 Traces, Vias, and Other PCB Components

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner, and the characteristic impedance changes. This impedance change causes reflections.

- Avoid right-angle bends in a trace and try to route them at least with two 45° corners. To minimize any impedance change, the best routing would be a round bend (see Figure 24).
- Separate high-speed signals (e.g., clock signals) from low-speed signals and digital from analog signals; again, placement is important.
- To minimize crosstalk not only between two signals on one layer but also between adjacent layers, route them with 90° to each other.

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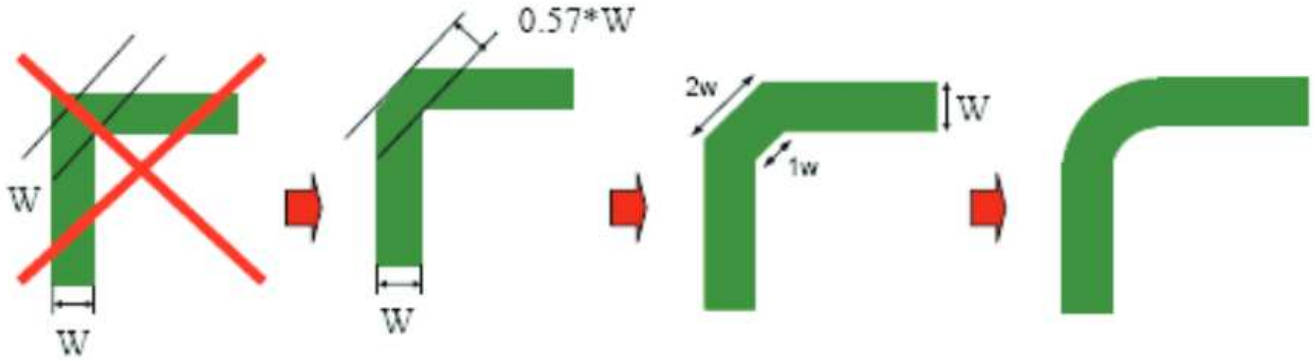


Figure 24. Poor and Good Right Angle Bends

12.2 Layout Example

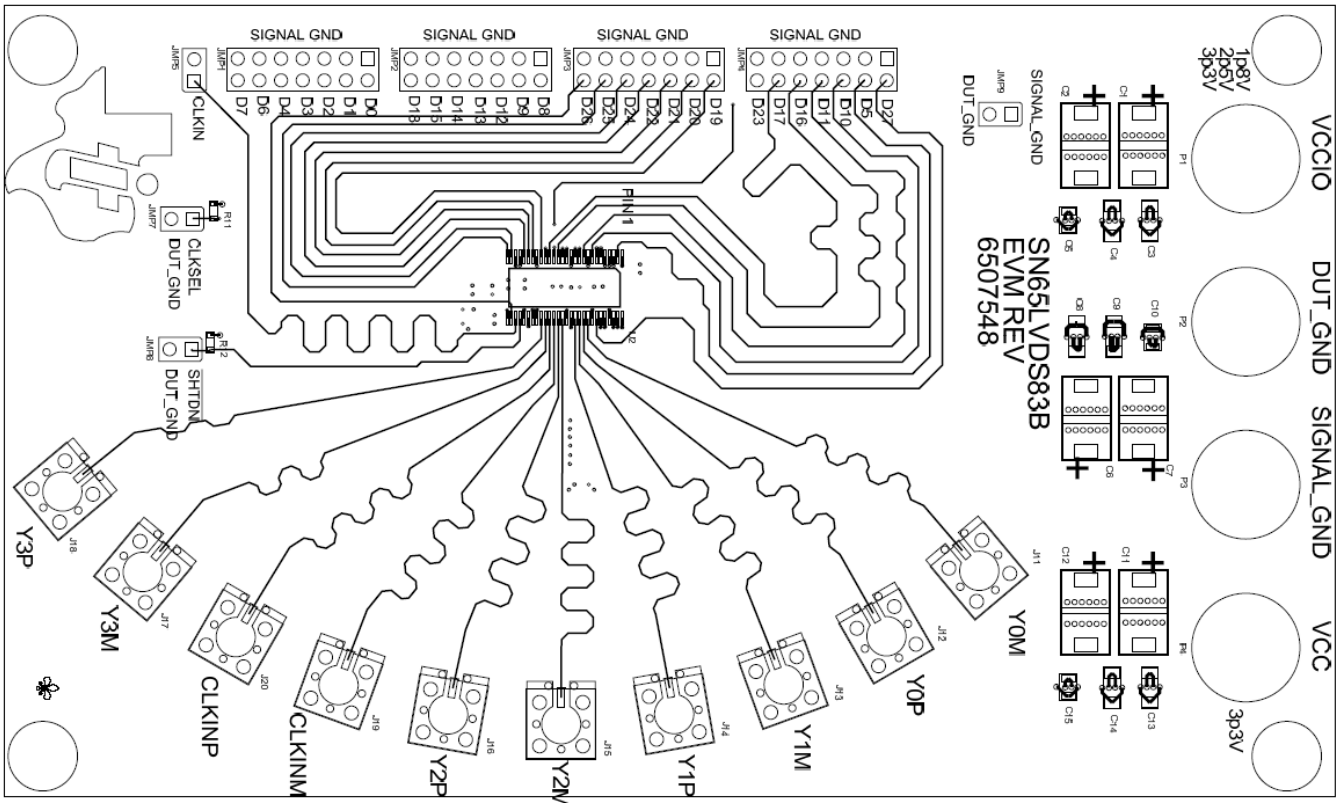


Figure 25. SN75LVDS83B EVM Top Layer – TSSOP Package

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Layout Example (continued)

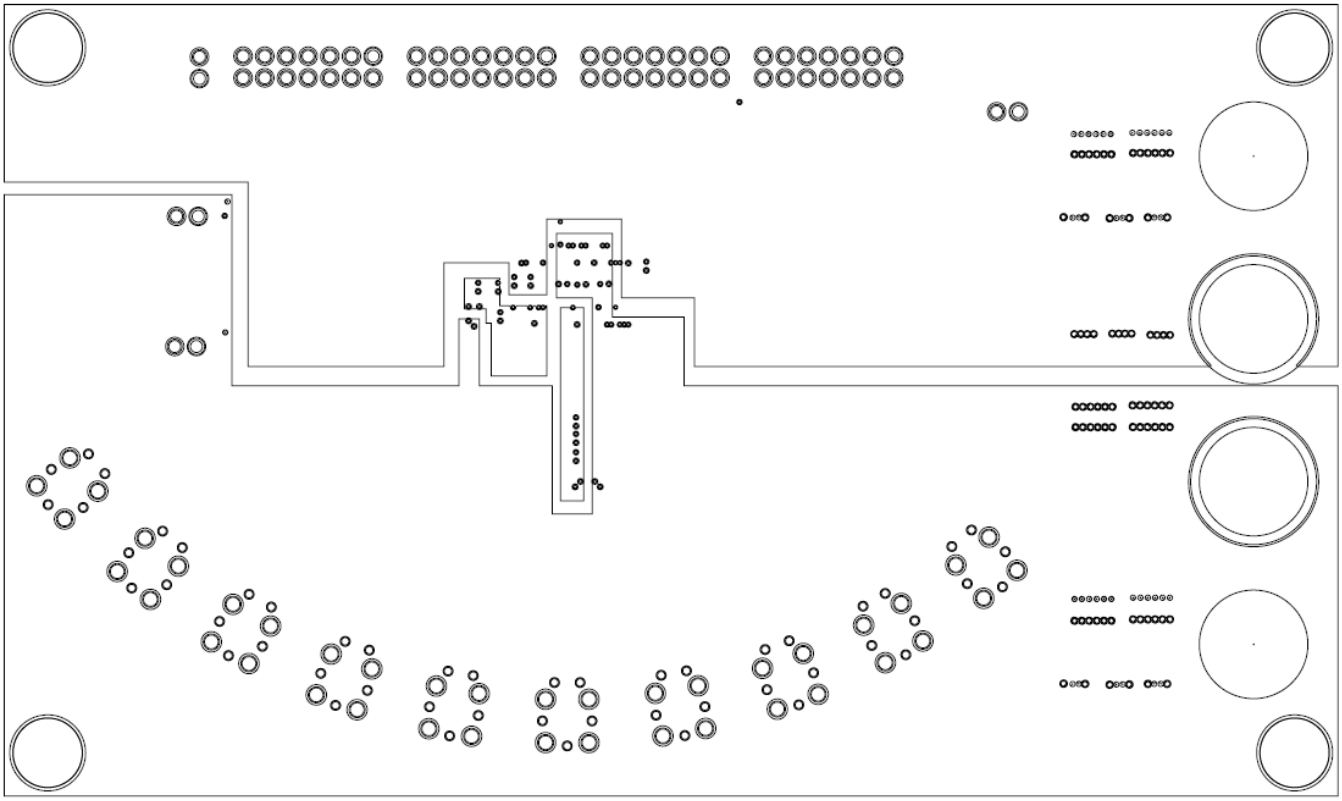


Figure 26. SN75LVDS83B EVM VCC Layer – TSSOP Package

13 Device and Documentation Support

13.1 Trademarks

OMAP, DaVinci, FlatLink are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA02272DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-10 to 70	LVDS83B	Samples
SN75LVDS83BDGG	ACTIVE	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-10 to 70	LVDS83B	Samples
SN75LVDS83BDGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-10 to 70	LVDS83B	Samples
SN75LVDS83BZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	-10 to 70	LVDS83B	Samples
SNSNYLVDSZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	-10 to 70	LVDS83B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

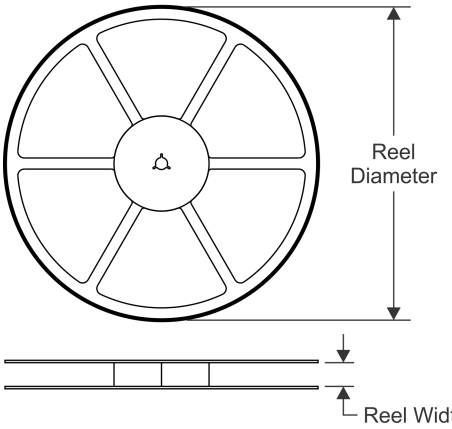
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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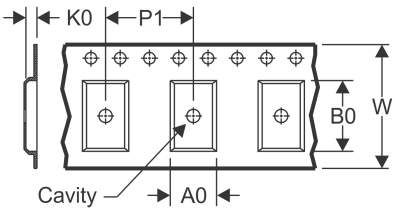
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

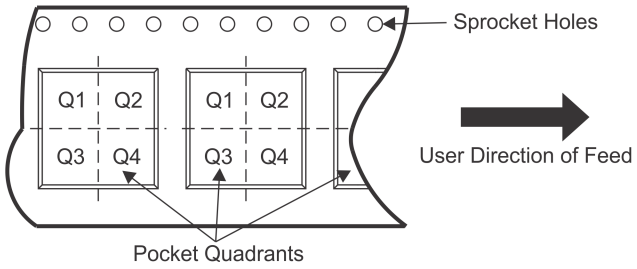


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

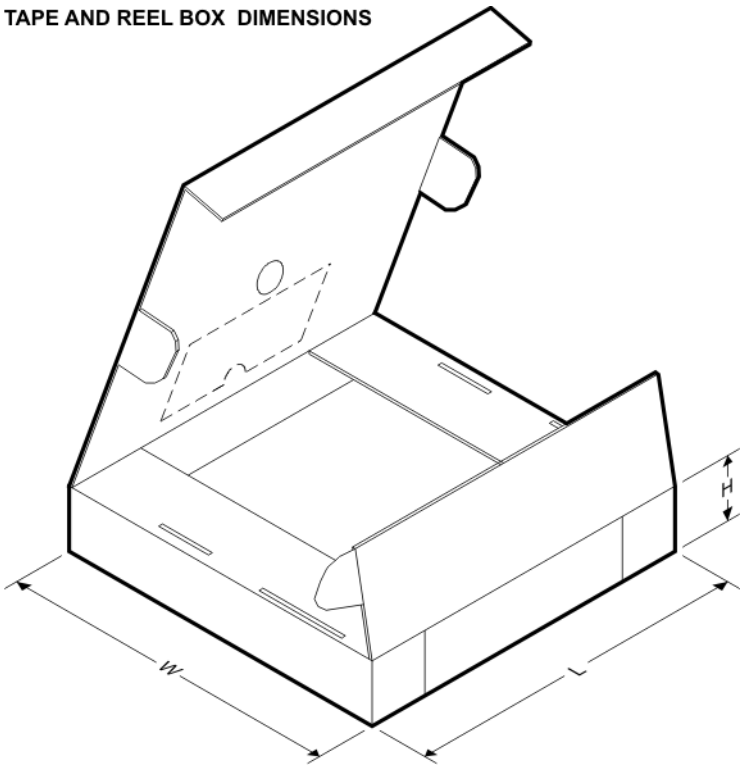
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVDS83BDGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN75LVDS83BZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

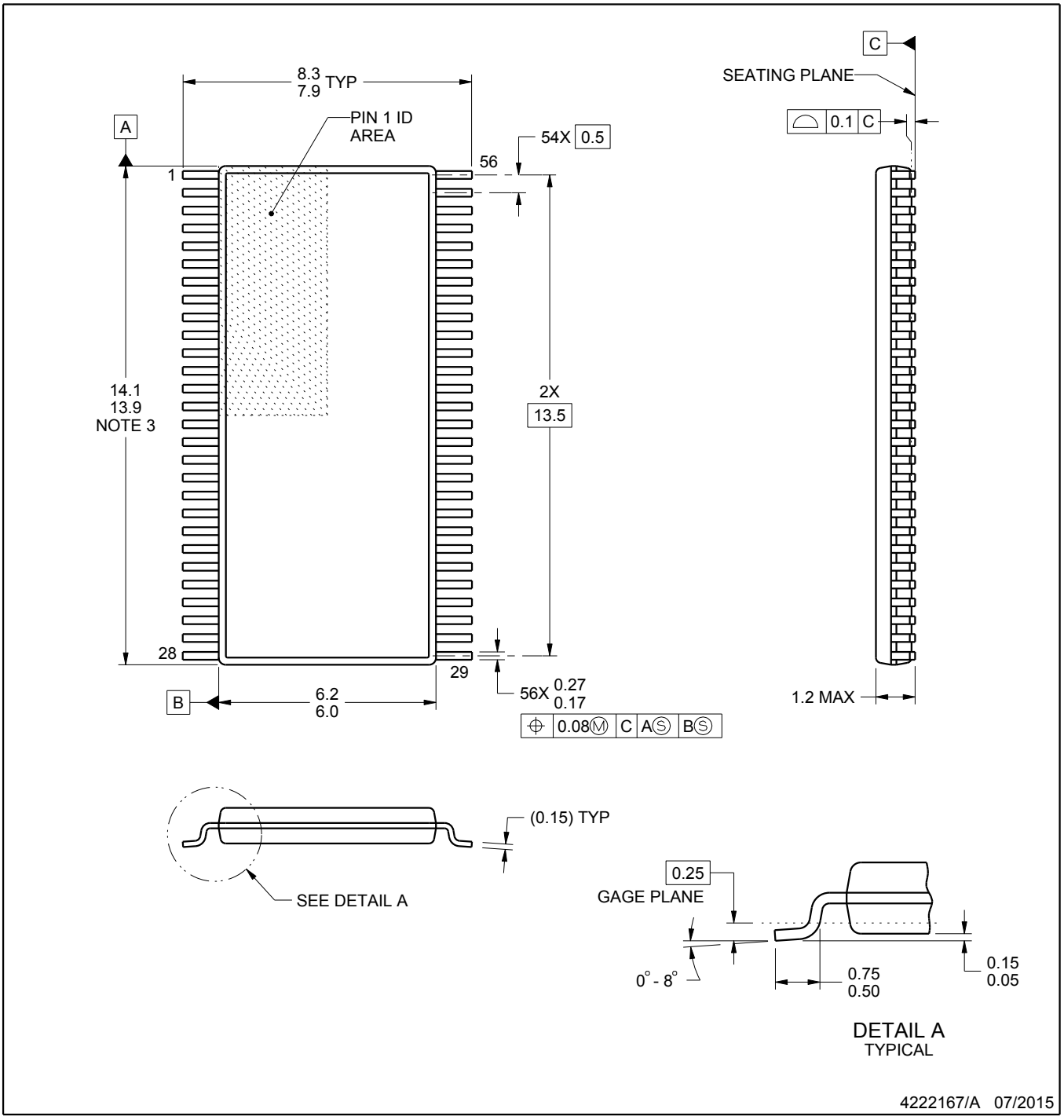
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVDS83BDGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN75LVDS83BZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	336.6	336.6	28.6

PACKAGE OUTLINE

DGG0056A

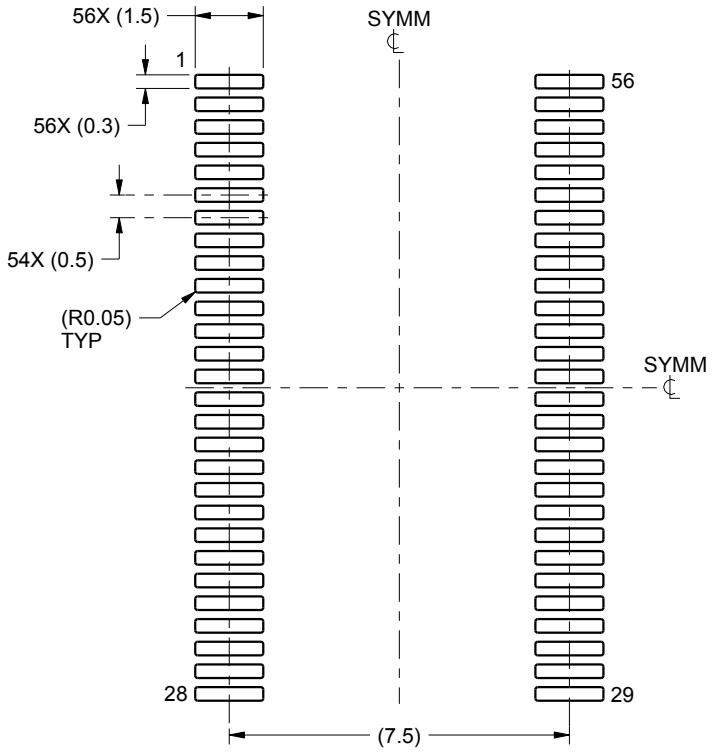
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

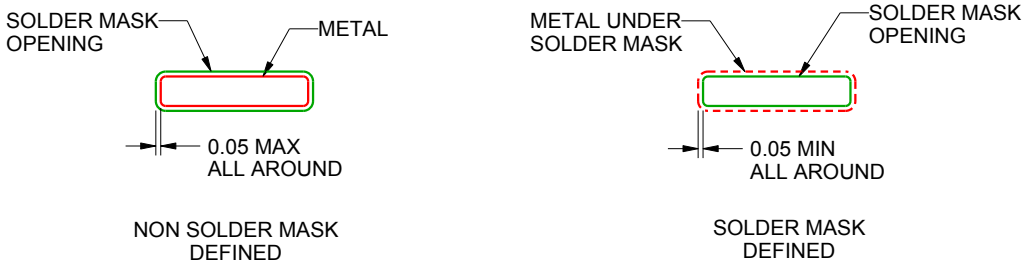


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

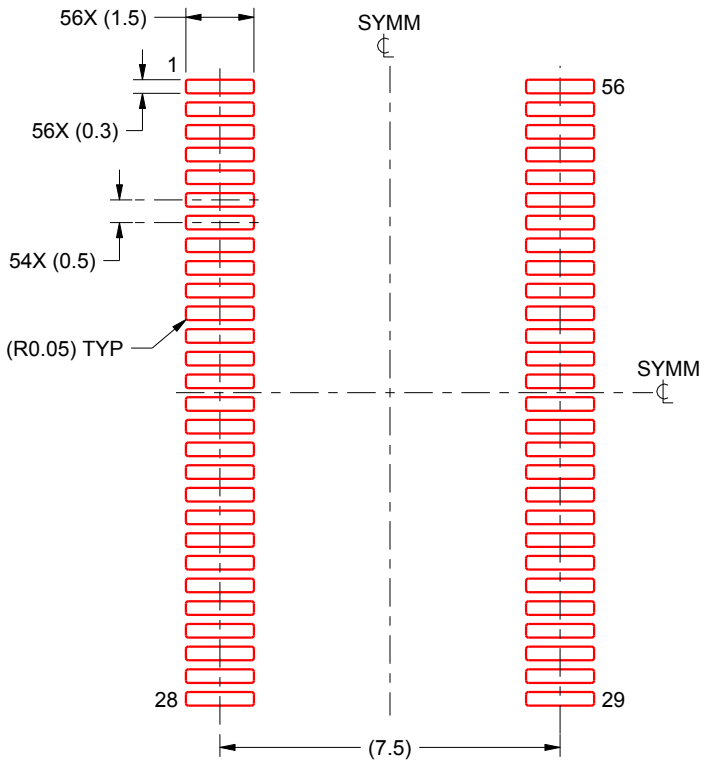


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

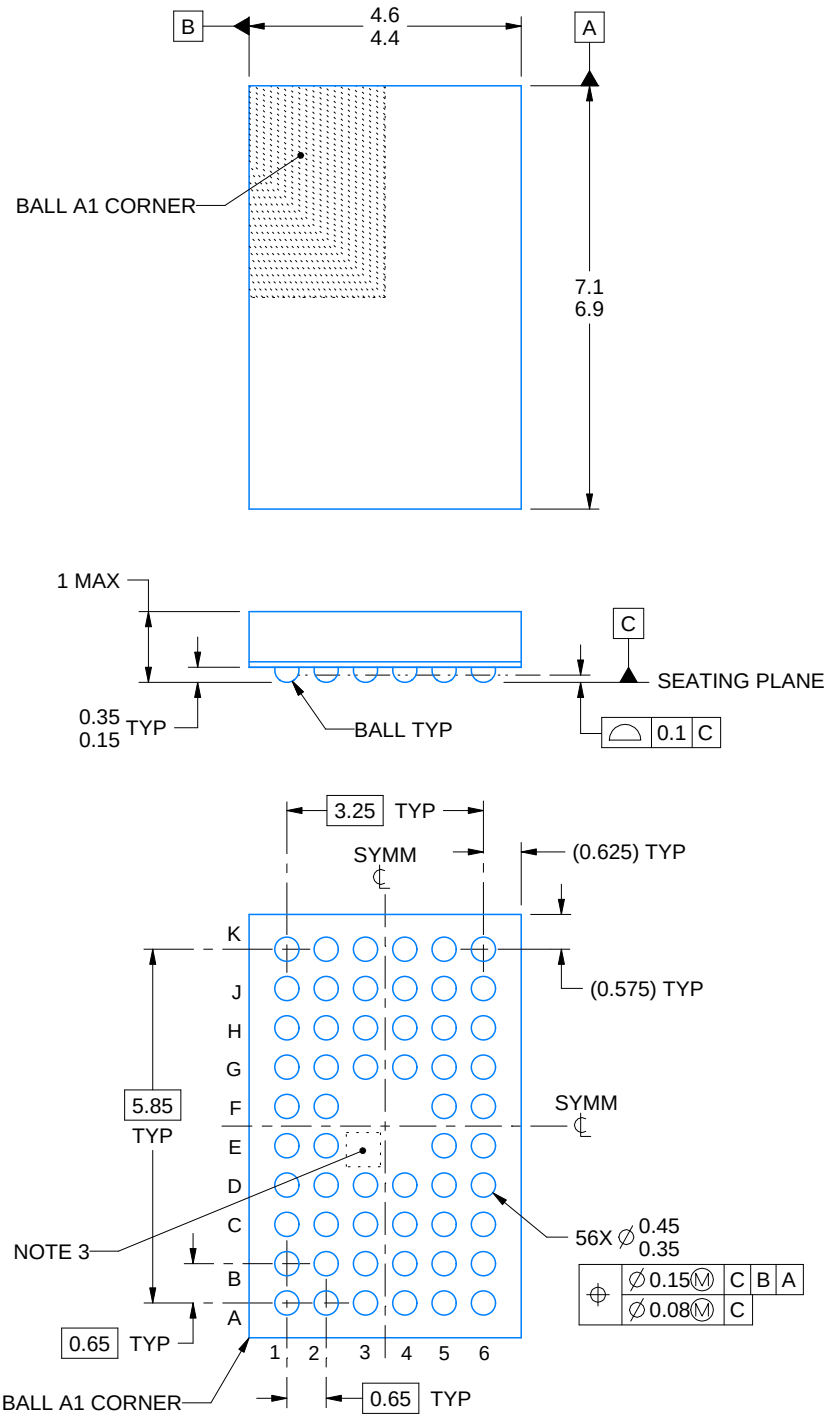
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

ZQL0056A

JRBGA - 1 mm max height

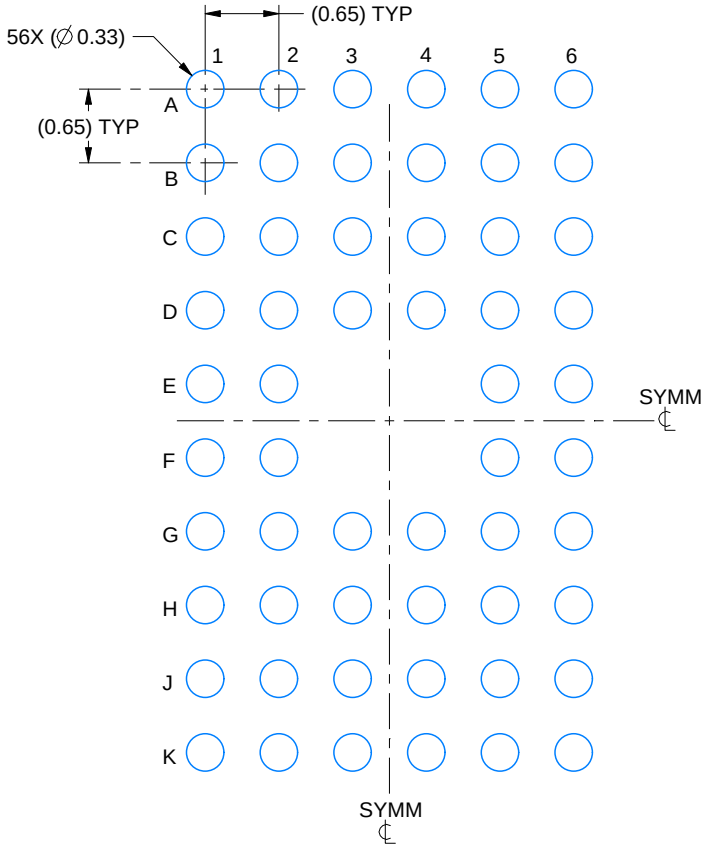
PLASTIC BALL GRID ARRAY



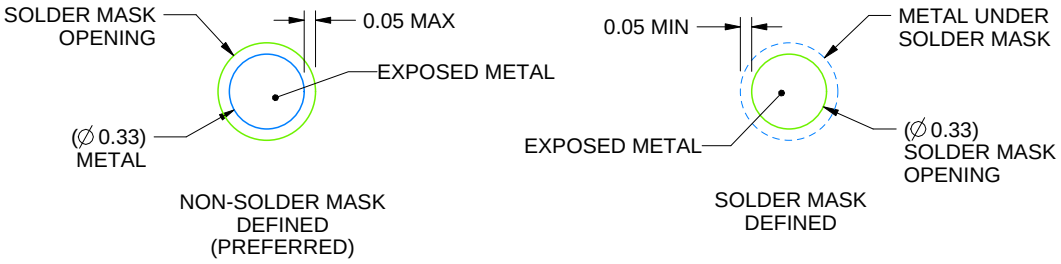
4219711/B 01/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. No metal in this area, indicates orientation.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

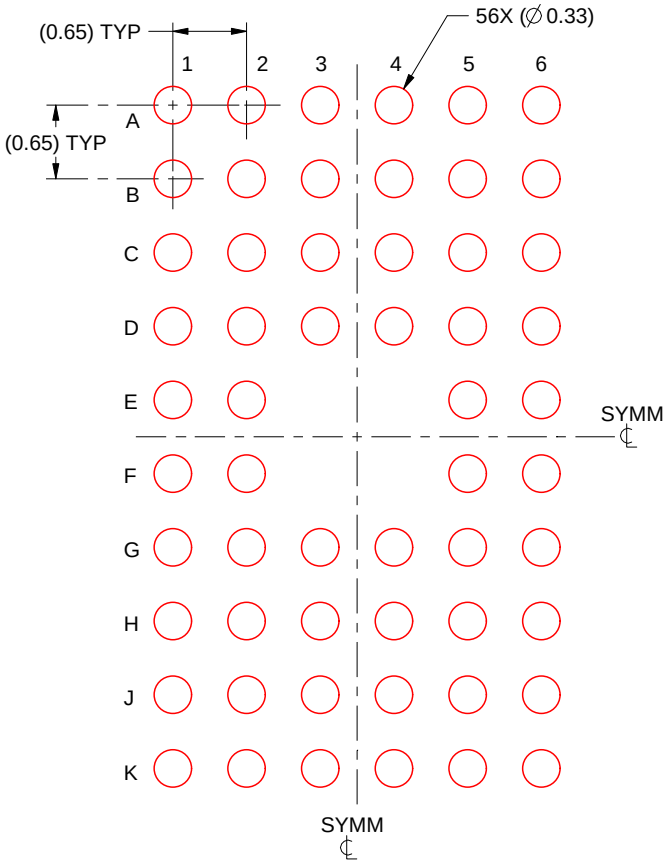


SOLDER MASK DETAILS
NOT TO SCALE

4219711/B 01/2017

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4219711/B 01/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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