2SK3070(L),2SK3070(S)

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

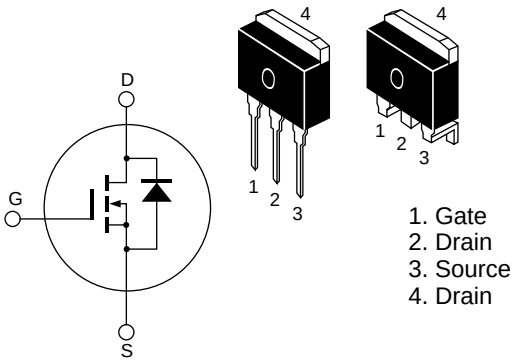
ADE-208-684G (Z)
8th. Edition
February 1999

Features

- Low on-resistance
  $R_{DS(on)}$ = 4.5 mΩ typ.
- Low drive current
- 4 V gate drive device can be driven from 5 V source

Outline

LDPAK



1. Gate
2. Drain
3. Source
4. Drain

Hitachi semiconductor

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	40	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	75	A
Drain peak current	$I_{D(pulse)}$ Note1	300	A
Body-drain diode reverse drain current	I_{DR}	75	A
Avalanche current	I_{AP} Note3	50	A
Avalanche energy	E_{AR} Note3	333	mJ
Channel dissipation	Pch Note2	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

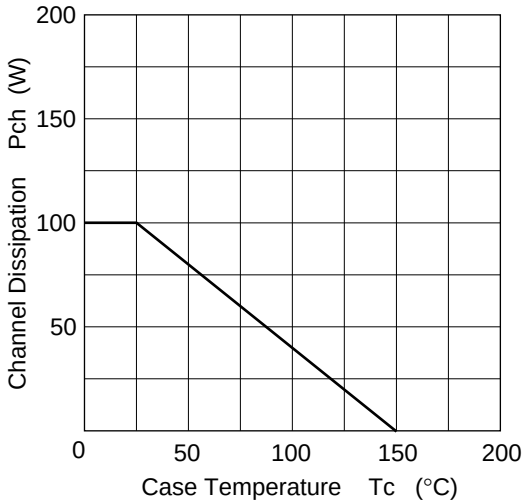
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	µA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	10	µA	V_{DS} = 40 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	I_D = 1 mA, V_{DS} = 10 V Note1
Static drain to source on state	$R_{DS(on)}$	—	4.5	5.8	mΩ	I_D = 40 A, V_{GS} = 10 V Note1
resistance		—	6.5	10	mΩ	I_D = 40 A, V_{GS} = 4 V Note1
Forward transfer admittance	$\|y_{fs}\|$	50	80	—	S	I_D = 40 A, V_{DS} = 10 V Note1
Input capacitance	Ciss	—	6800	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1300	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	380	—	pF	f = 1 MHz
Total gate charge	Qg	—	130	—	nc	V_{DD} = 25 V
Gate to source charge	Qgs	—	25	—	nc	V_{GS} = 10 V
Gate to drain charge	Qgd	—	30	—	nc	I_D = 75 A
Turn-on delay time	$t_{d(on)}$	—	60	—	ns	V_{GS} = 10 V, I_D = 40 A
Rise time	t_r	—	300	—	ns	R_L = 0.75 Ω
Turn-off delay time	$t_{d(off)}$	—	550	—	ns	
Fall time	t_f	—	400	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.05	—	V	I_F = 75 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	90	—	ns	I_F = 75 A, V_{GS} = 0 diF/ dt = 50 A/ µs

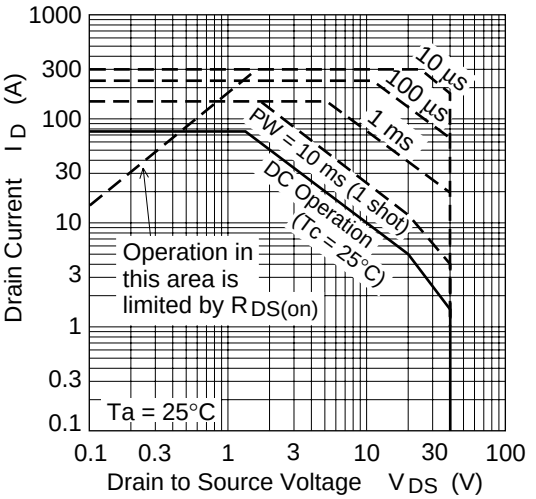
Note: 1. Pulse test

Main Characteristics

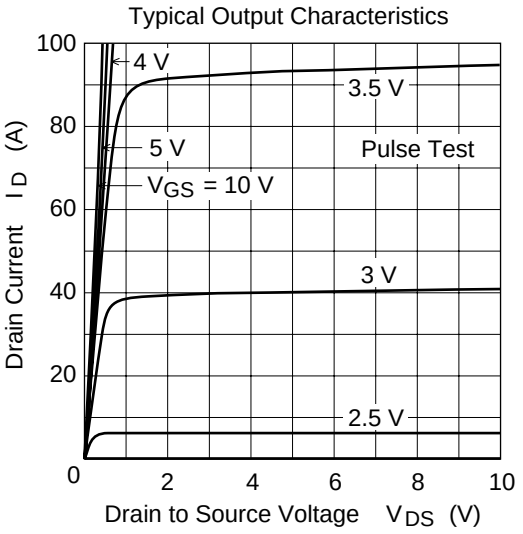
Power vs. Temperature Derating



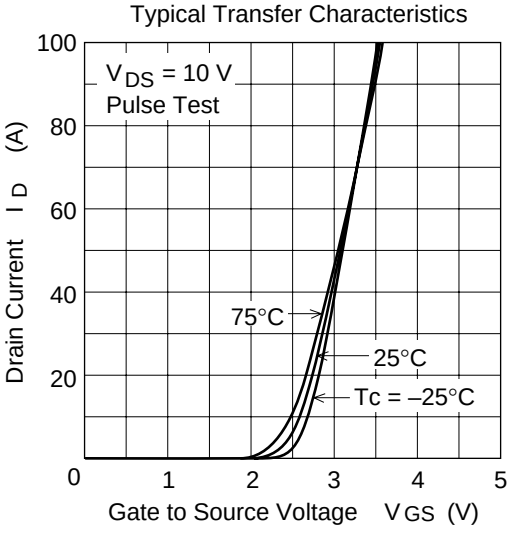
Maximum Safe Operation Area



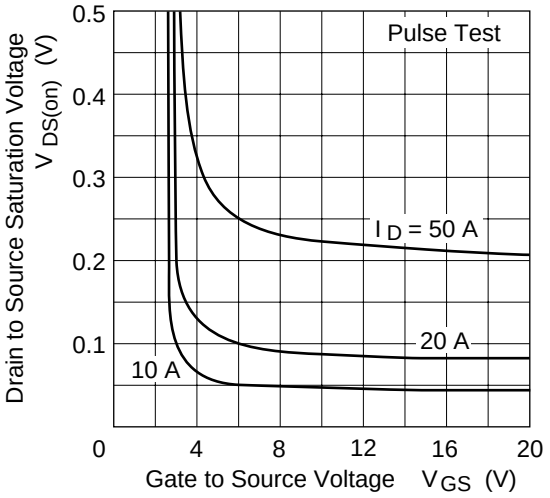
Typical Output Characteristics



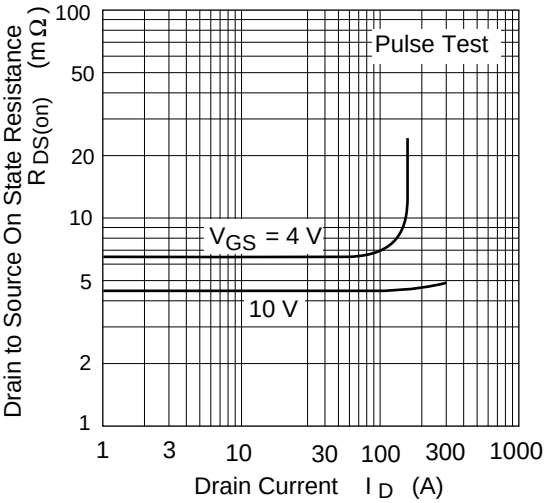
Typical Transfer Characteristics



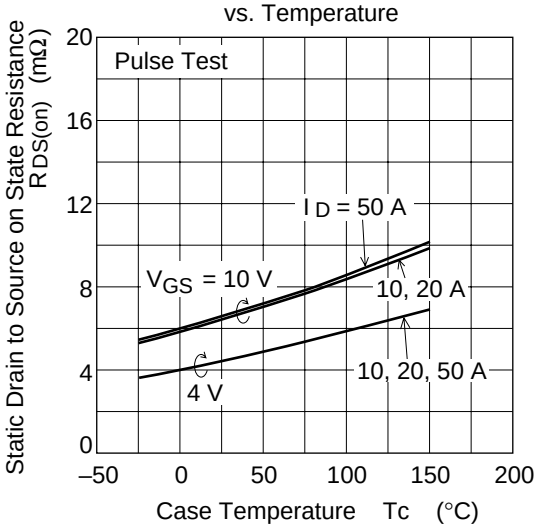
Drain to Source Saturation Voltage vs. Gate to Source Voltage



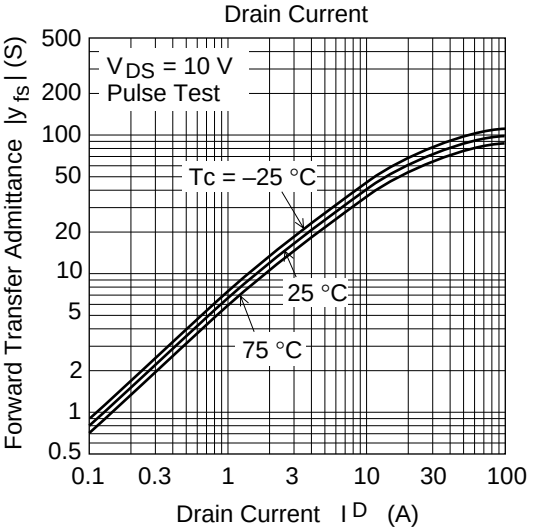
Static Drain to Source on State Resistance vs. Drain Current



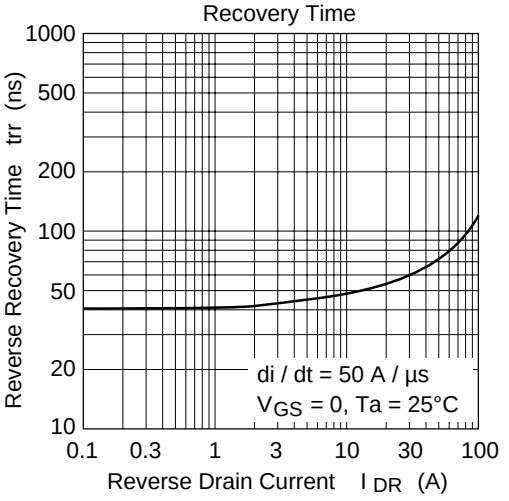
Static Drain to Source on State Resistance vs. Temperature



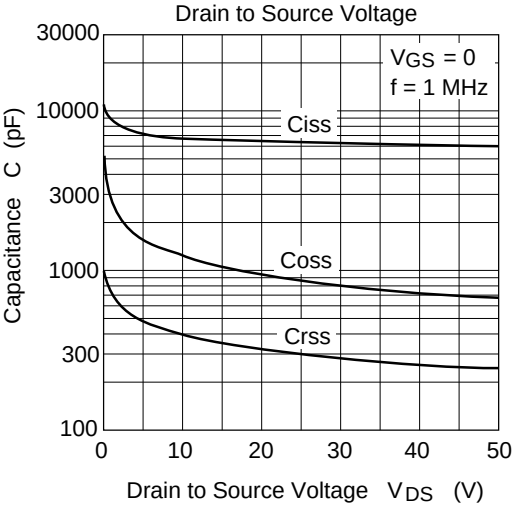
Forward Transfer Admittance vs. Drain Current



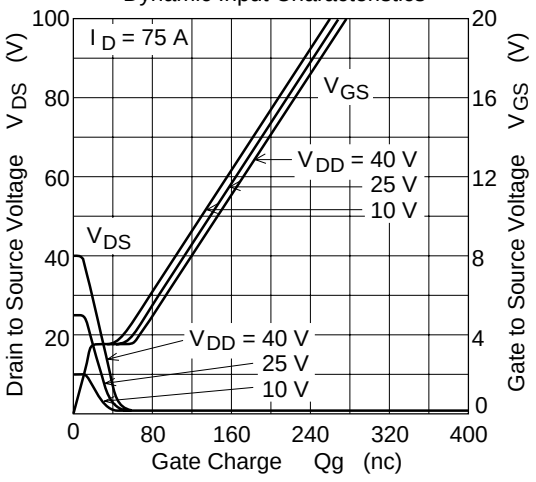
Body–Drain Diode Reverse Recovery Time



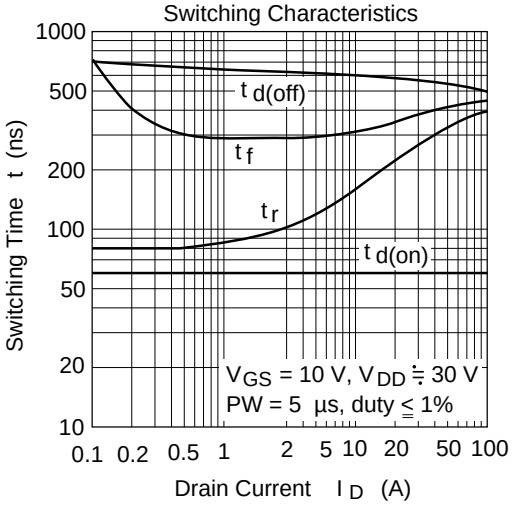
Typical Capacitance vs. Drain to Source Voltage



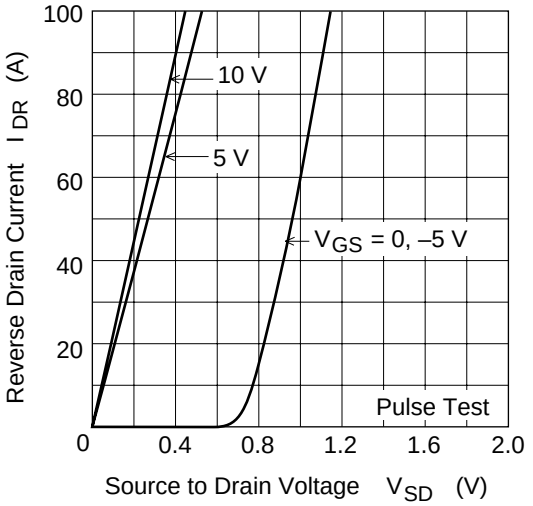
Dynamic Input Characteristics



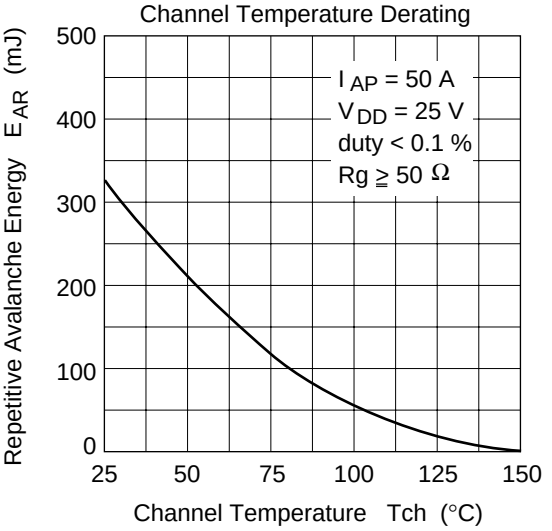
Switching Characteristics



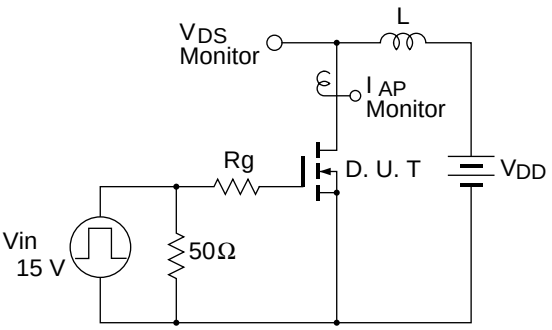
Reverse Drain Current vs.
Source to Drain Voltage



Maximun Avalanche Energy vs.
Channel Temperature Derating

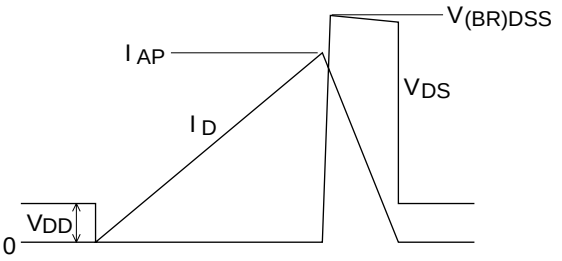


Avalanche Test Circuit

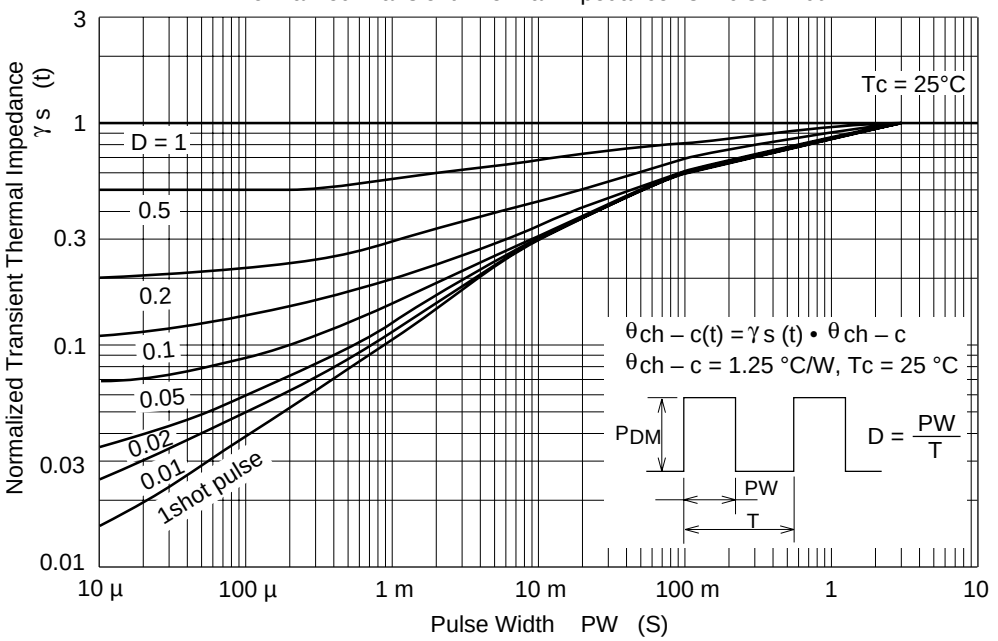


Avalanche Waveform

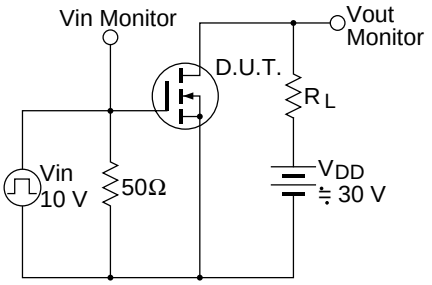
$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}^{2} \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



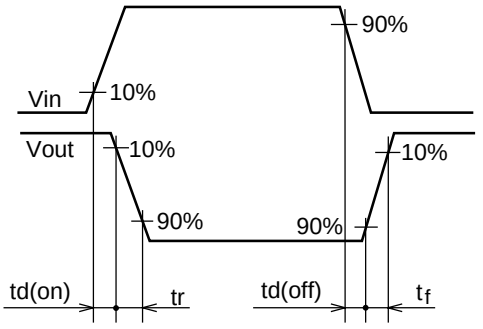
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

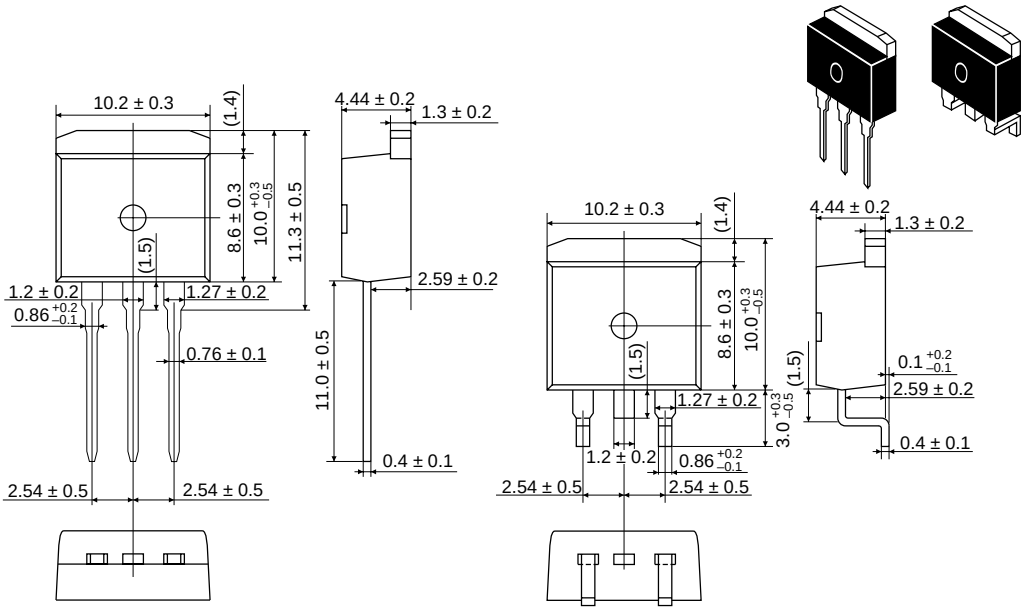


Waveform



Package Dimensions

Unit: mm



Ⓛ type

Ⓢ type

Hitachi Code	LDPAK
EIAJ	—
JEDEC	—

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HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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