RF3300-2

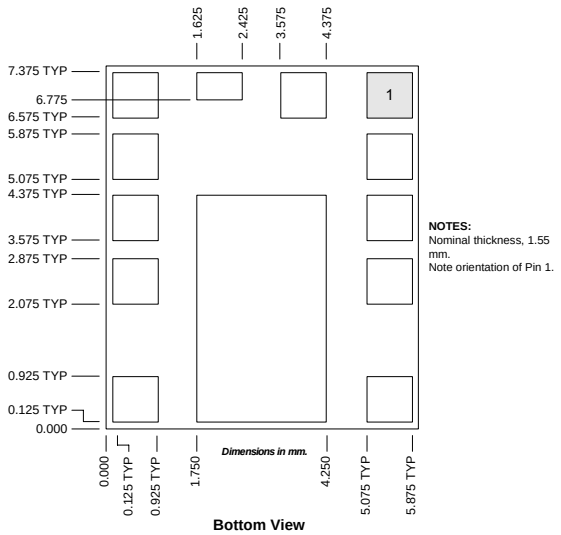
3V 900MHz LINEAR AMPLIFIER MODULE

Typical Applications

- 3V CDMA/AMPS Cellular Handsets
- 3V CDMA2000/1X Cellular Handsets
- Spread-Spectrum Systems
- Designed for Compatibility with Qualcomm Chipsets

Product Description

The RF3300-2 is a high-power, high-efficiency linear amplifier module targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 3V CDMA/AMPS handheld digital cellular equipment, spread-spectrum systems, and other applications in the 824MHz to 849MHz band. The RF3300-2 has a digital control line for low power application to reduce the current drain. The device is self-contained with 50Ω input and output that is matched to obtain optimum power, efficiency, and linearity characteristics. The RF3300-2 contains a temperature compensating bias circuit to improve performance over temperature.

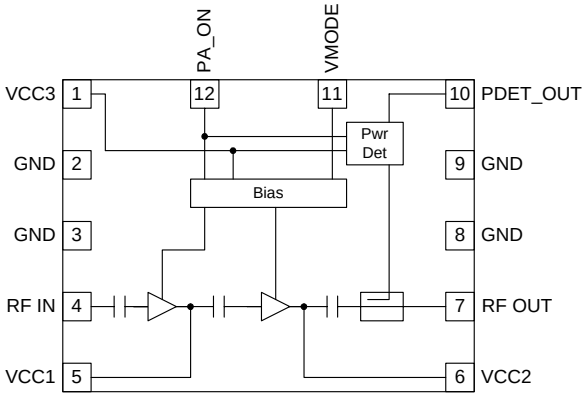


Bottom View

Package Style: Module (6mmx7.5mm)

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS
- ☐ InGaP/HBT
- ☐ GaN HEMT
- ☑ SiGe Bi-CMOS



Functional Block Diagram

Features

- Single 3V Supply with Internal V_{REF}
- Integrated Power Detect Circuit
- 27dB Linear Gain
- 55mA Idle Current
- Temperature Compensating Bias Circuit
- Integrated PA Enable Switch

Ordering Information

RF3300-2	3V 900MHz Linear Amplifier Module
RF3300-2 PCBA	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage ($P_{OUT} \leq 31.5$dBm)	+5.2	V_{DC}
Control Voltage (PA_ON)	+3.6	V_{DC}
Input RF Power	+10	dBm
Mode Voltage (V_{MODE})	+3.6	V_{DC}
Operating Case Temperature	-30 to +110	℃
Storage Temperature	-30 to +150	℃

Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Power State (V_{MODE} Low)					Typical Performance at V_{CC}=3.2V, PA_ON=High, T_{AMB}=25°C, Frequency=824MHz to 849MHz (unless otherwise specified)
Frequency Range	824		849	MHz	
Linear Gain		27		dB	See Gain versus Power chart.
Second Harmonic		-40		dBc	
Third Harmonic		-40		dBc	
Maximum Linear Output Power (CDMA Modulation)	28			dBm	
Total Linear Efficiency		33		%	V_{CC}=3.2V, P_{OUT}=28dBm (room temperature)
Adjacent Channel Power Rejection		-48	-46	dBc	ACPR@885kHz, P_{OUT}=Max P_{OUT}
		-60	-59	dBc	ACPR@1980kHz, P_{OUT}=Max P_{OUT}
Input VSWR		1.8:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. >-70dBc
Noise Power		-135		dBm/Hz	At 45MHz offset.
Low Power State (V_{MODE} High)					Typical Performance at V_{CC}=3.2V, PA_ON=High, T_{AMB}=25°C, Frequency=824MHz to 849MHz (unless otherwise specified)
Frequency Range	824		849	MHz	
Linear Gain		24.5		dB	
Second Harmonic		-40		dBc	
Third Harmonic		-35		dBc	
Maximum Linear Output Power (CDMA Modulation)	16			dBm	
Adjacent Channel Power Rejection		-46.5	-44.0	dBc	ACPR@885kHz, P_{OUT}=Max P_{OUT}. See ACPR versus Power chart.
		-62	-59	dBc	ACPR@1980kHz, P_{OUT}=Max P_{OUT}
Input VSWR		1.8:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. >-70dBc

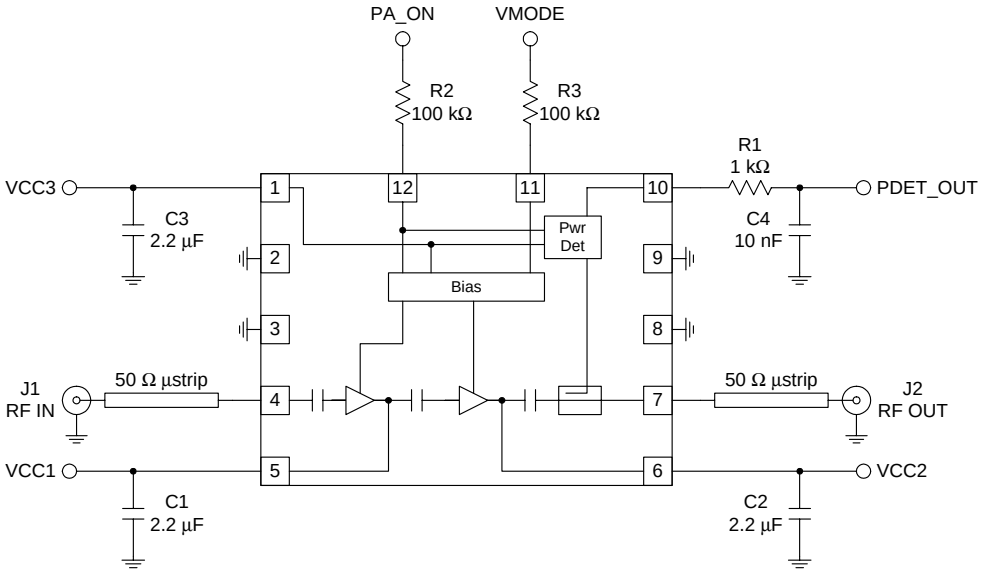
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
FM Mode					Typical Performance at V_{CC}=3.2V, PA_ON=High, T_{AMB}=25°C, Frequency=824MHz to 849MHz (unless otherwise specified)
Frequency Range	824		849	MHz	
Gain		27		dB	
Second Harmonic		-40		dBc	
Third Harmonic		-40		dBc	
Max CW Output Power		31.5		dBm	
Total Efficiency (AMPS mode)		48		%	V_{CC}=3.2V, P_{OUT}=31.5dBm (room temperature)
Input VSWR		1.8:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. >-70dBc
DC Supply					
Supply Voltage Range	3.2	3.7	4.2	V	
Quiescent Current		100	120	mA	V_{MODE}=Low
		55	70	mA	V_{MODE}=High
PA_ON Current		0.1		µA	V_{MODE}=High
V_{MODE} Current		0.1		µA	
Turn On/Off Time			<40	µs	PA_ON switch from Low to High, I_{CC} to within 90% of the final value, P_{OUT} within 1dB of the final value
Total Current (Power Down)		35	60	µA	PA_ON=Low, V_{MODE}=Low
PA_ON “Low” Voltage Range	0		0.5	V	
PA_ON “High” Voltage Range	1.7	2.7	3.6	V	Must not exceed V_{CC}.
V_{MODE} “Low” Voltage Range	0		0.5	V	
V_{MODE} “High” Voltage Range	1.7	2.7	3.6	V	Must not exceed V_{CC}.
Gain Settle Time			6	µs	PA_ON switched from low to high, P_{OUT} within 1dB of the final value.
			6	µs	PA_ON switched from high to low, P_{OUT} within 1dB of the final value.
Internal Power Detector					
PDET Output Voltage		1.8		V	P_{OUT}=28dBm, V_{MODE}=Low, CDMA Mode
		1		V	P_{OUT}=16dBm, V_{MODE}=High, CDMA Mode
		2.1		V	P_{OUT}=31.5dBm, V_{MODE}=Low, FM Mode

Pin	Function	Description	Interface Schematic
1	VCC3	Bias circuit and HDET power supply. A low frequency decoupling capacitor (2.2μF) is required. Type: P	
2	GND	Ground connection. Connect to the GND_SLUG pin. For best performance, keep traces physically short and connect immediately to ground plane. Type: P	
3	GND	Ground connection. Connect to the GND_SLUG pin. For best performance, keep traces physically short and connect immediately to ground plane. Type: P	
4	RF IN	RF input internally matched to 50Ω. This input is internally AC-coupled. Type: A, I	
5	VCC1	First stage power supply. A low frequency decoupling capacitor (2.2μF) is required. Type: P	
6	VCC2	Output stage power supply. A low frequency decoupling capacitor (2.2μF) is required. Type: P	
7	RF OUT	RF output internally matched to 50Ω. This input is internally AC-coupled. Type: A, O	
8	GND	Ground connection. Connect to the GND_SLUG pin. For best performance, keep traces physically short and connect immediately to ground plane. Type: P	
9	GND	Ground connection. Connect to the GND_SLUG pin. For best performance, keep traces physically short and connect immediately to ground plane. Type: P	
10	PDET_OUT	Power detector output. Type: A, O	
11	VMODE	Gain step control. When this pin is High, the module is in low power mode, and the amplifier's current is reduced. When this pin is Low, the module is in high power mode. Voltage should not be applied to this pin before VCC3 is applied. Type: D, I	
12	PA_ON	Device enable control. When this pin is High, the device is on. When this pin is Low, the device is off. Voltage should not be applied to this pin before VCC3 is applied. Type: D, I	
13	GND_SLUG	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Note: Where Type code is: I=Input; O=Output; A=Analog; D=Digital; P=Power

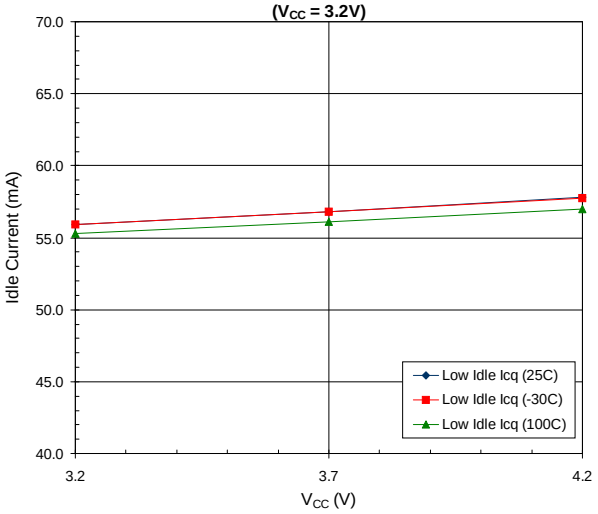
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

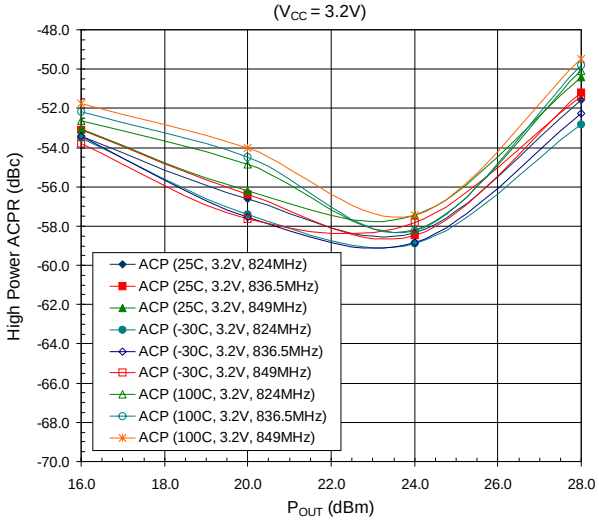


NOTE:
Resistors R2 and R3 are provided on the evaluation board to protect against power sequencing issues. (Refer to pin descriptions 11 and 12.) These resistors are not needed when the VCC3 is connected to the handset battery.

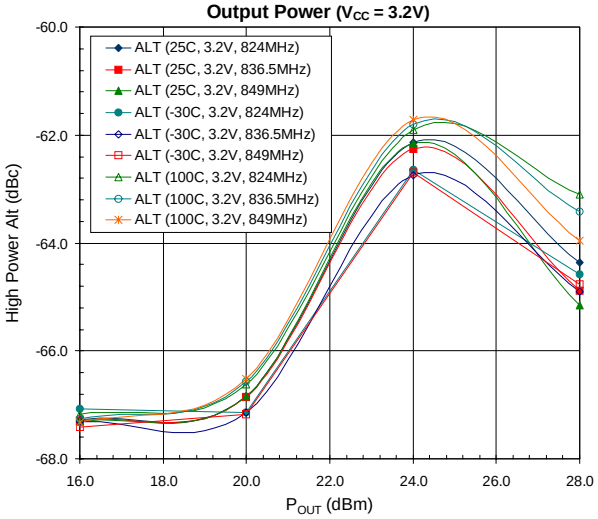
Low Power Idle Current versus V_{CC}
(V_{CC} = 3.2V)



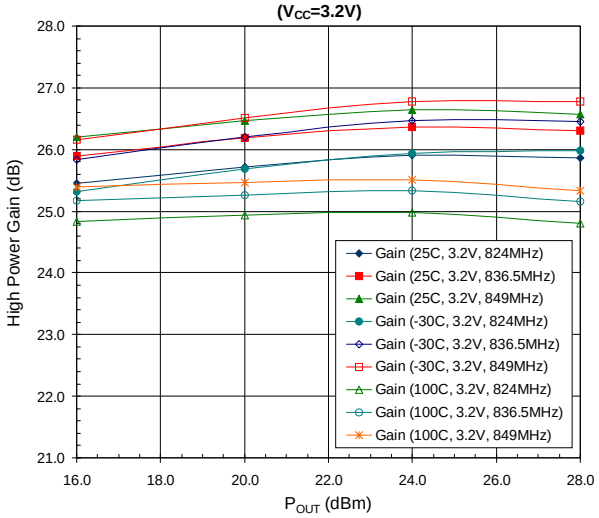
High Power Adjacent Channel Power Versus Output Power
(V_{CC} = 3.2V)



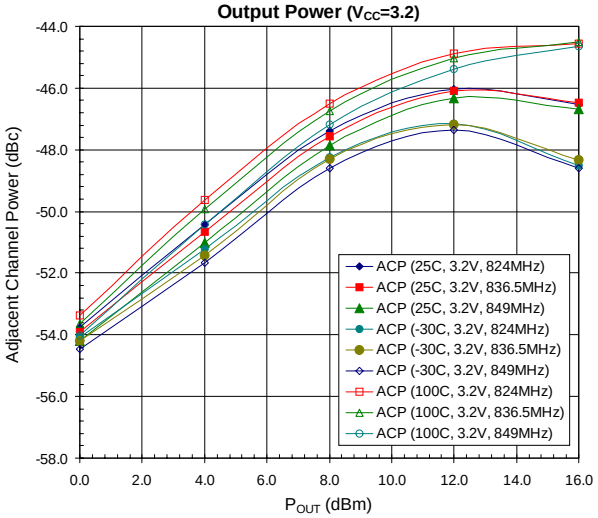
High Power Alternate Channel Power versus Output Power (V_{CC} = 3.2V)



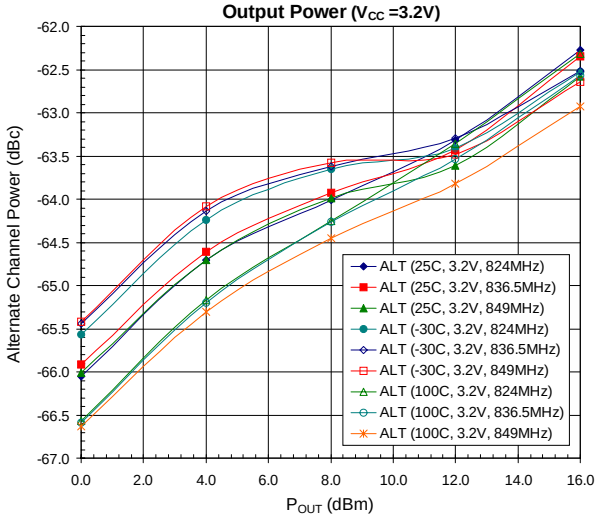
High Power CDMA Gain versus Output Power (V_{CC}=3.2V)

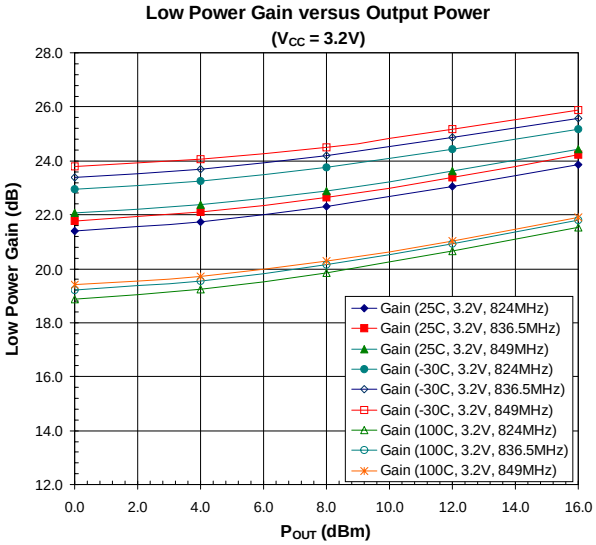


Low Power Adjacent Channel Power versus Output Power (V_{CC}=3.2)



Low Power Alternate Channel Power versus Output Power (V_{CC} =3.2V)




Low Power Gain versus Output Power
(VCC = 3.2V)
Low Power Gain (dB)
28.0
26.0
24.0
22.0
20.0
18.0
16.0
14.0
12.0
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
POUT (dBm)
Gain (25C, 3.2V, 824MHz)
Gain (25C, 3.2V, 836.5MHz)
Gain (25C, 3.2V, 849MHz)
Gain (-30C, 3.2V, 824MHz)
Gain (-30C, 3.2V, 836.5MHz)
Gain (-30C, 3.2V, 849MHz)
Gain (100C, 3.2V, 824MHz)
Gain (100C, 3.2V, 836.5MHz)
Gain (100C, 3.2V, 849MHz)