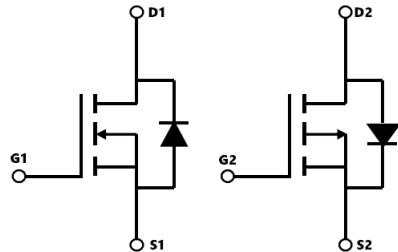


30V N+P-Channel Enhancement Mode MOSFET**Description**

The AO4606 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

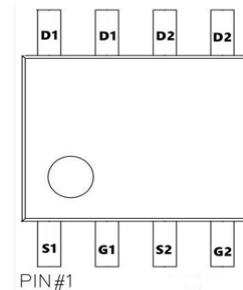
**General Features**

$V_{DS} = 30V$ $I_D = 6A$

$R_{DS(ON)} < 28m\Omega$ @ $V_{GS}=10V$ $R_{DS(ON)} < 42m\Omega$ @ $V_{GS}=4.5V$

$V_{DS} = -30V$ $I_D = -7.6A$

$R_{DS(ON)} < 32m\Omega$ @ $V_{GS}=10V$ $R_{DS(ON)} < 40m\Omega$ @ $V_{GS}=4.5V$

**Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)**

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
VDS	Drain-Source Voltage	30	-30	V
VGS	Gate-Source Voltage	± 20	± 20	V
$I_D@T_c=25^\circ C$	Continuous Drain Current, V_{GS} @ 10V ¹	6	-7.6	A
$I_D@T_c=100^\circ C$	Continuous Drain Current, V_{GS} @ 10V ¹	4.5	-5.9	A
IDM	Pulsed Drain Current ²	20	-15	A
EAS	Single Pulse Avalanche Energy ³	22	45	mJ
IAS	Avalanche Current	21	-30	A
$P_D@T_c=25^\circ C$	Total Power Dissipation ⁴	2.0	2.0	W
TSTG	Storage Temperature Range	-55 to 150	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	62	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	5	°C/W

30V N+P-Channel Enhancement Mode MOSFET

N-Channel Electrical Characteristics ($T_J=25^\circ C$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	---	---	V
$\frac{\partial BV_{DSS}}{\partial T_J}$	BVDSS Temperature Coefficient	Reference to $25^\circ C, I_D=1mA$	---	0.023	---	$V/^\circ C$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=10A$	---	19	28	$m\Omega$
		$V_{GS}=4.5V, I_D=5A$	---	28	42	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	1.7	2.5	V
$\frac{\partial V_{GS(th)}}{\partial T_J}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.2	---	$mV/^\circ C$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ C$	---	---	1	uA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ C$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=10A$	---	16	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	2.5	5	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=20V, V_{GS}=4.5V, I_D=10A$	---	7.2	---	nC
Q_{gs}	Gate-Source Charge		---	1.4	---	
Q_{gd}	Gate-Drain Charge		---	2.2	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3, I_D=5A$	---	4.1	---	ns
T_r	Rise Time		---	9.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	15.5	---	
T_f	Fall Time		---	6.0	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	---	572	---	pF
C_{oss}	Output Capacitance		---	81	---	
C_{rss}	Reverse Transfer Capacitance		---	65	---	
I_s	Continuous Source Current ^{1,5}	$V_G=V_D=0V, \text{Force Current}$	---	---	10	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	20	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ C$	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=21A$
- 4 .The power dissipation is limited by $150^\circ C$ junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

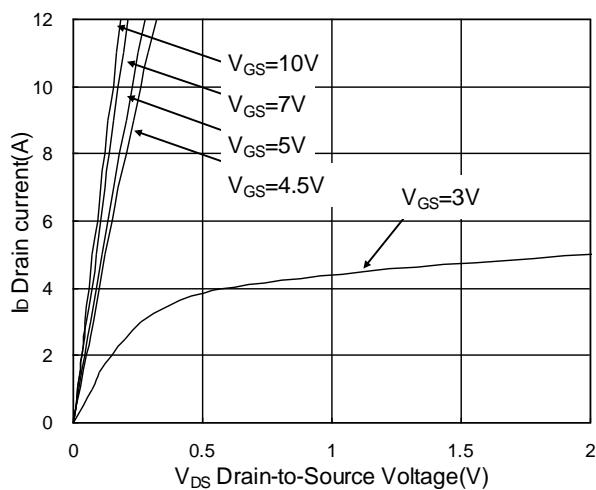
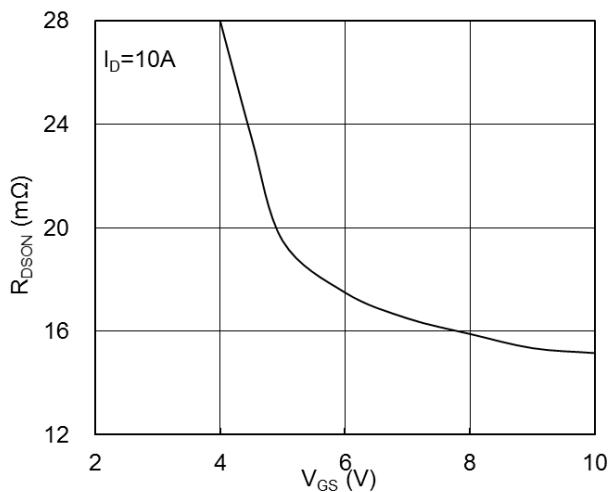
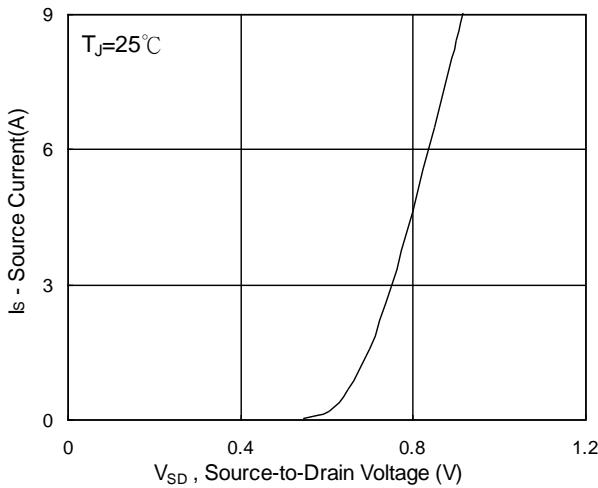
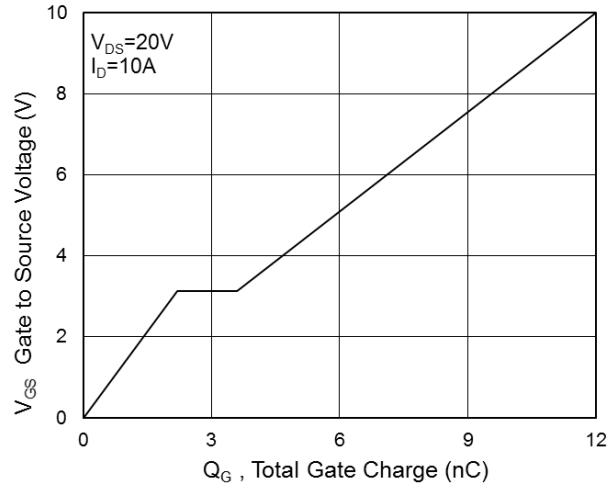
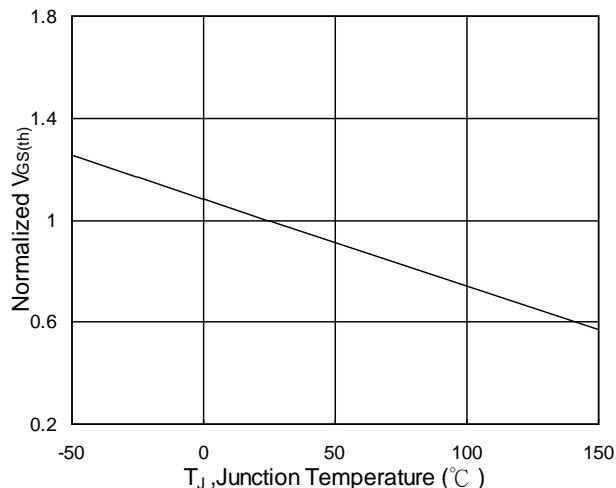
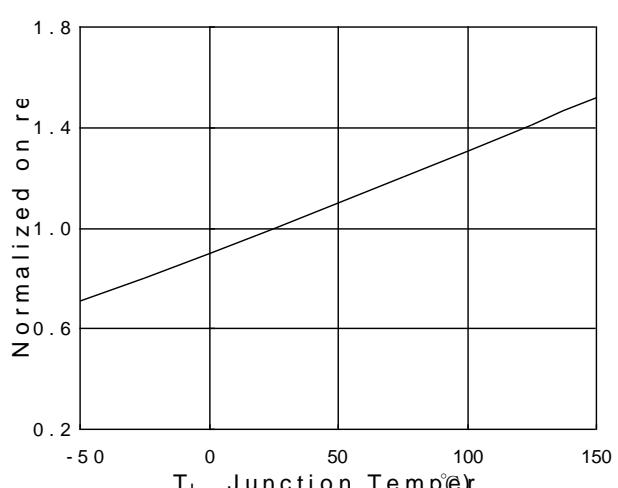
30V N+P-Channel Enhancement Mode MOSFET

P-Channel Electrical Characteristics ($T_J=25^\circ C$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	---	---	V
$\frac{\partial BV_{DSS}}{\partial T_J}$	BV_{DSS} Temperature Coefficient	Reference to $25^\circ C, I_D=-1mA$	---	-0.021	---	$V/^\circ C$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-7A$	---	24	32	$m\Omega$
		$V_{GS}=-4.5V, I_D=-5A$	---	32	40	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	-1.6	-2.5	V
$\frac{\partial V_{GS(th)}}{\partial T_J}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.2	---	$mV/^\circ C$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-24V, V_{GS}=0V, T_J=25^\circ C$	---	---	1	μA
		$V_{DS}=-24V, V_{GS}=0V, T_J=55^\circ C$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5V, I_D=-7A$	---	15	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$		15	30	
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-20V, V_{GS}=-4.5V, I_D=-7A$	---	9.8	---	nC
Q_{gs}	Gate-Source Charge		---	2.2	---	
Q_{gd}	Gate-Drain Charge		---	3.4	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3, I_D=-5A$	---	16.4	---	ns
T_r	Rise Time		---	20.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	55	---	
T_f	Fall Time		---	10	---	
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$	---	930	---	pF
C_{oss}	Output Capacitance		---	148	---	
C_{rss}	Reverse Transfer Capacitance		---	115	---	
I_s	Continuous Source Current ^{1,5}	$V_G=V_D=0V, \text{Force Current}$	---	---	-7.6	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	-15	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^\circ C$	---	---	-1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZcopper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data sh.The power dissipation is limited by ows Max. rating
4. The test condition is $V_{150^\circ C}$ junction temperature $=-25 V, V_{GS}=-10V, L=0.1mH, I_{AS}=-30A$
- 5 .The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

30V N+P-Channel Enhancement Mode MOSFET**N-Channel Typical Characteristics****Fig.1 Typical Output Characteristics****Fig.2 On-Resistance vs Gate-Source Voltage****Fig.3 Forward Characteristics of Reverse****Fig.4 Gate-Charge characteristics****Fig.5 Normalized $V_{GS(th)}$ vs T_J** **Fig.6 Normalized $R_{DS(on)}$ vs T_J**

30V N+P-Channel Enhancement Mode MOSFET

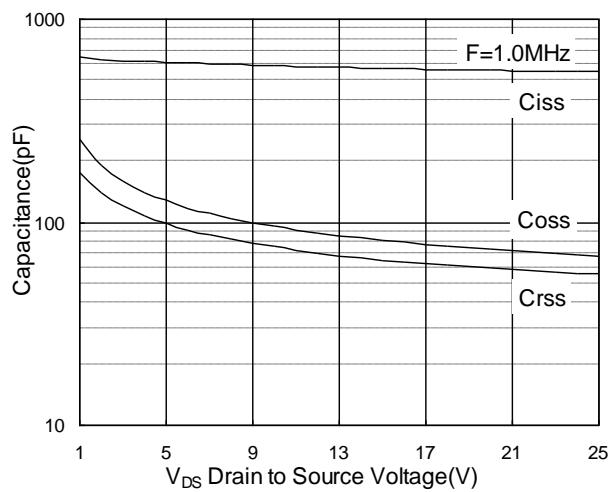


Fig.7 Capacitance

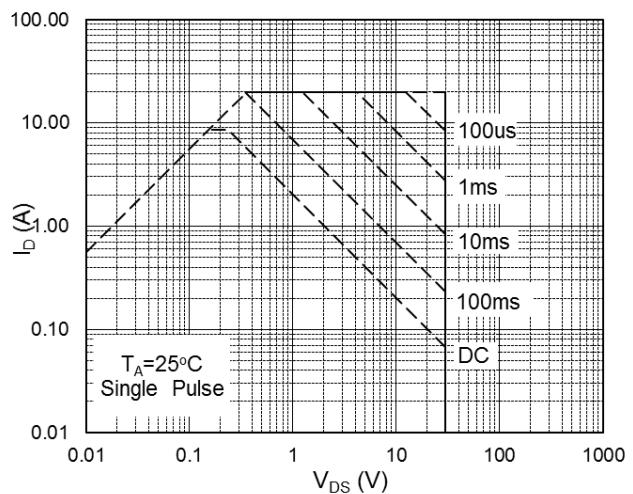


Fig.8 Safe Operating Area

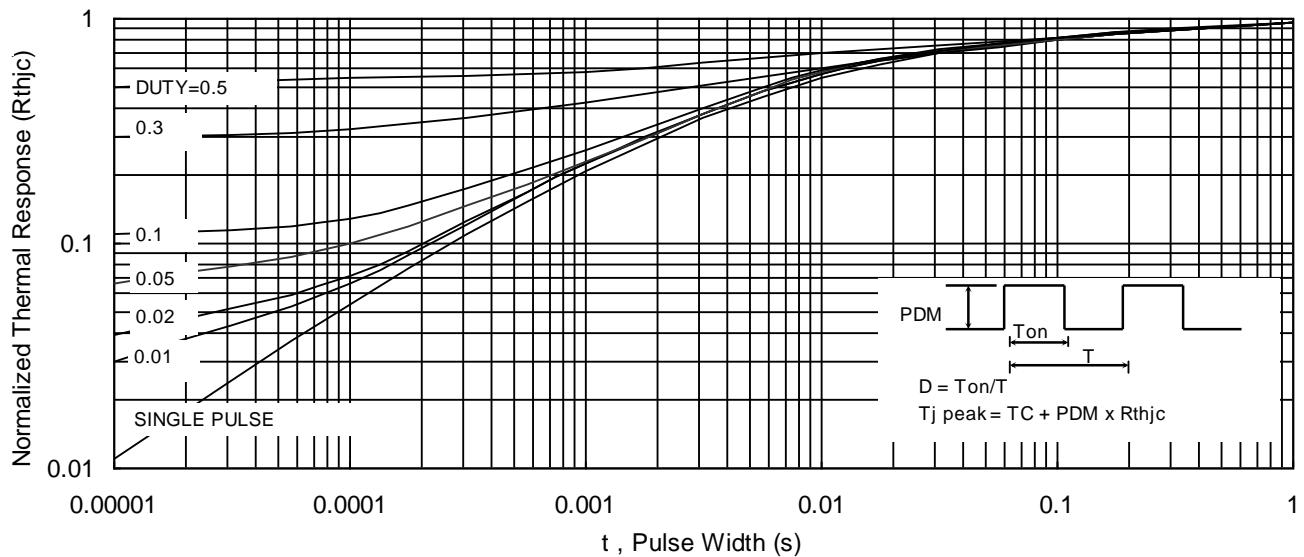


Fig.9 Normalized Maximum Transient Thermal Impedance

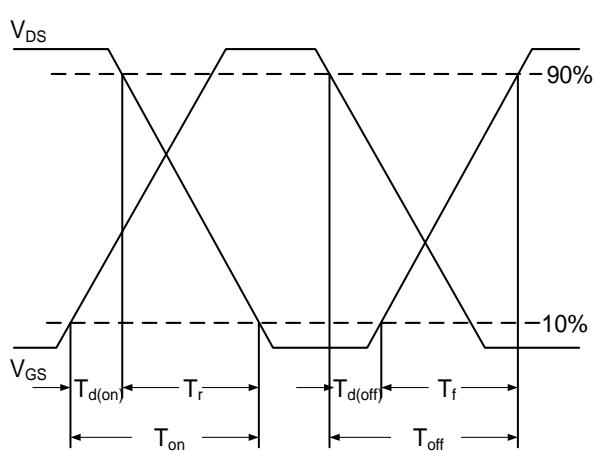


Fig.10 Switching Time Waveform

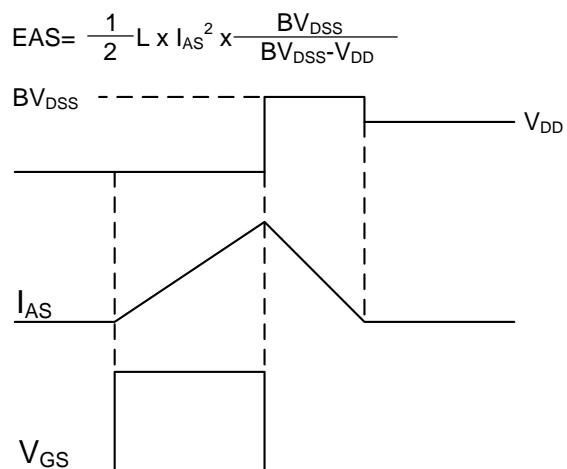


Fig.11 Unclamped Inductive Waveform

P-Channel Typical Characteristics

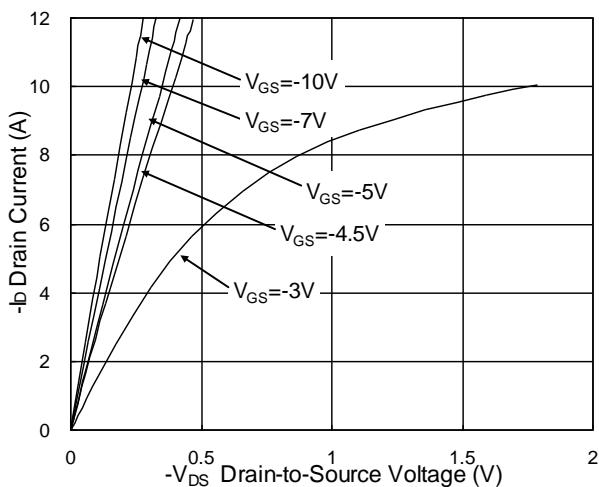


Fig.1 Typical Output Characteristics

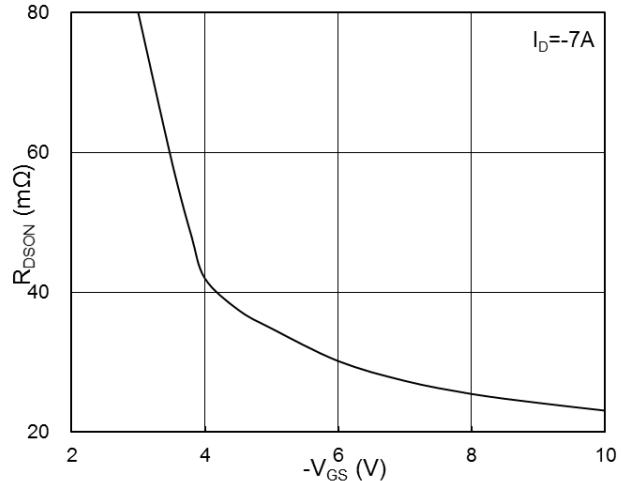


Fig.2 On-Resistance vs Gate-Source Voltage

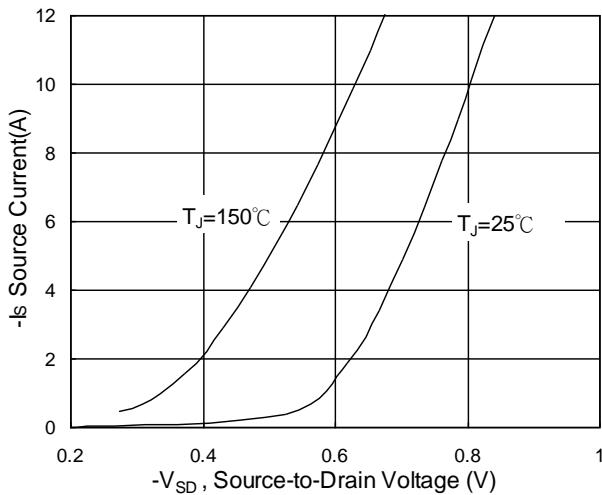


Fig.3 Forward Characteristics of Reverse

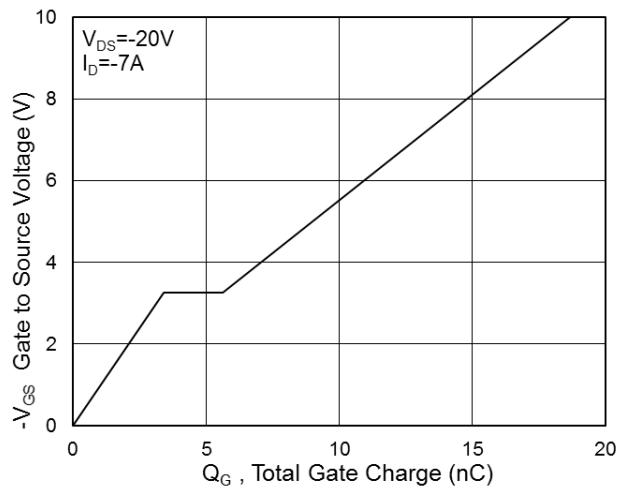


Fig.4 Gate-Charge Characteristics

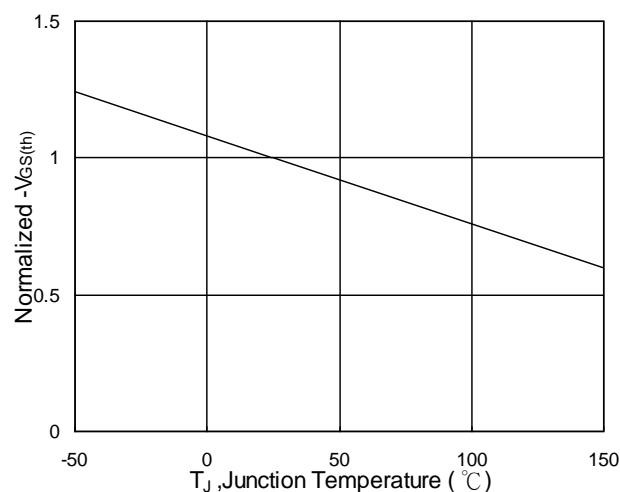


Fig.5 Normalized $V_{GS(th)}$ vs T_J

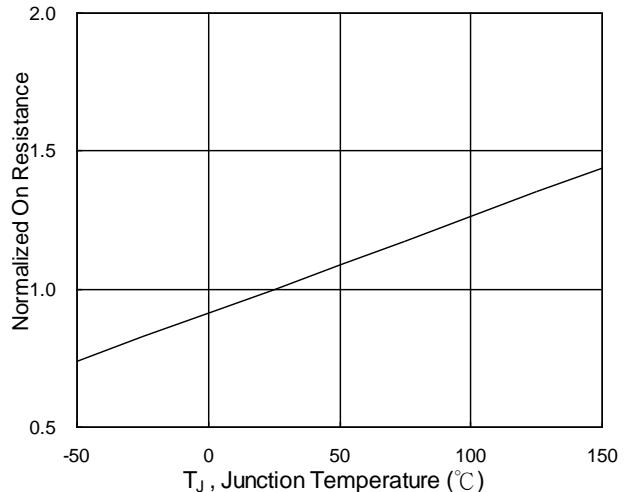


Fig.6 Normalized $R_{DS(on)}$ vs T_J

30V N+P-Channel Enhancement Mode MOSFET

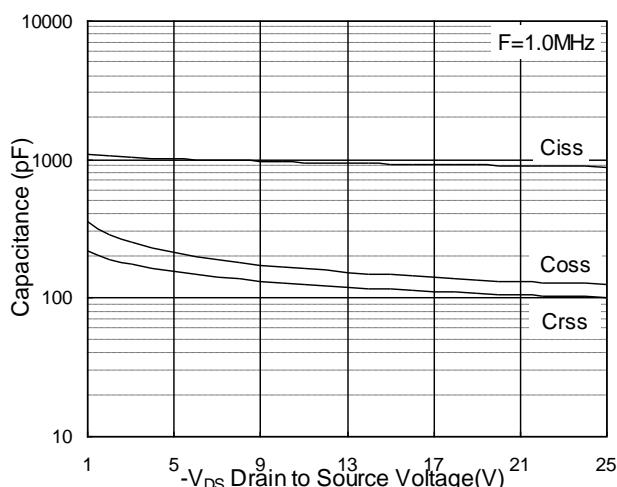


Fig.7 Capacitance

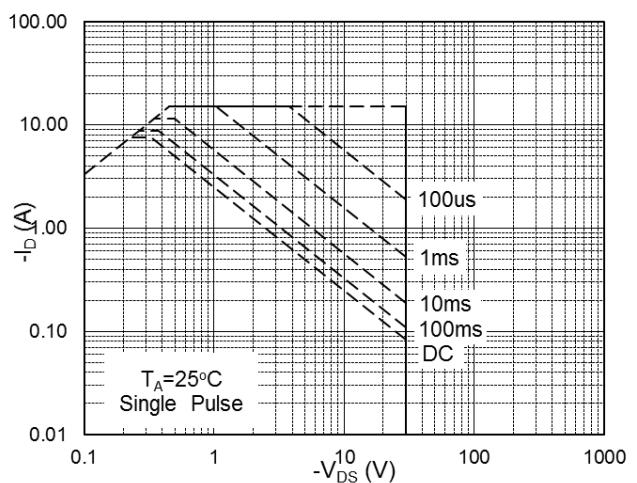


Fig.8 Safe Operating Area

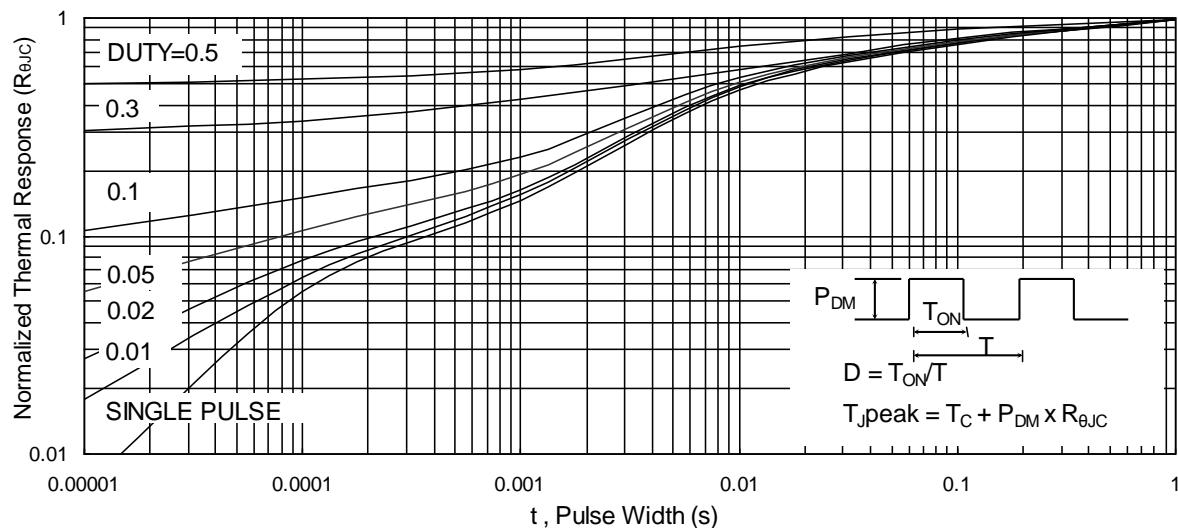


Fig.9 Normalized Maximum Transient Thermal Impedance

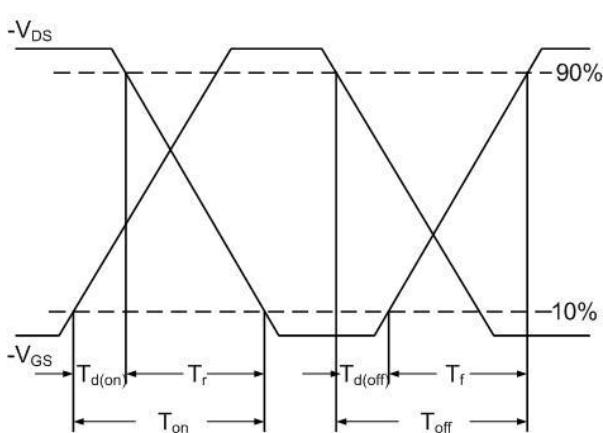


Fig.10 Switching Time Waveform

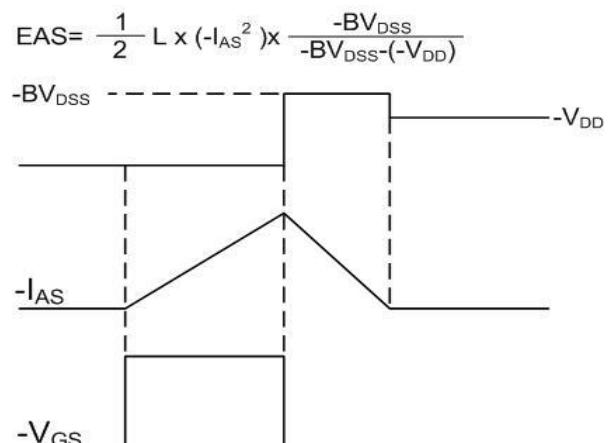
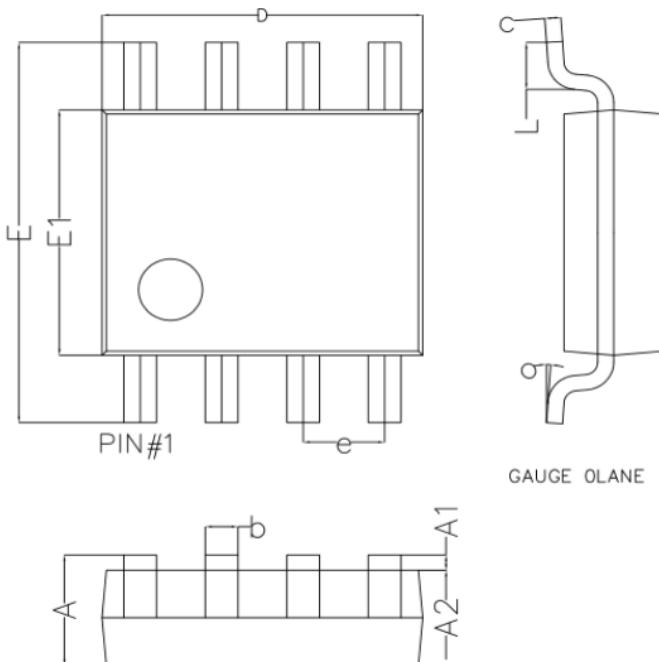


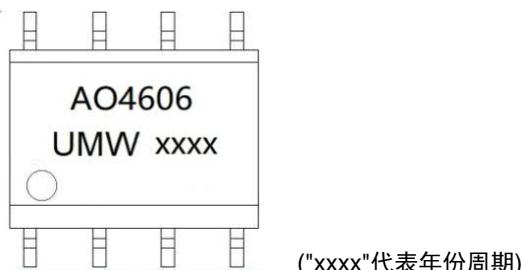
Fig.11 Unclamped Inductive Waveform

Package Mechanical Data-SOP-8



Symbol	Dim in mm		
	Min	Nor	Max
A	1.350	1.550	1.750
A1	0.100	0.175	0.250
A2	1.350	1.450	1.550
b	0.330	0.420	0.510
c	0.170	0.210	0.250
D	4.800	4.900	5.000
e	1.270 (BSC)		
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.400	0.835	1.2700
O	0°	4°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW AO4406	SOP-8	3000	Tape and reel