Audio Switching Amplifier

AD1994

OBSOLETE

FEATURES

Integrated stereo modulator and power stage
<0.005% THD + N
105 dB dynamic range (A-weighted)
2 × 25 W output power (6 Ω, 10% THD + N)
1 × 50 W output power (3 Ω, 10% THD + N)
R_{DS-ON} < 0.3 Ω (per transistor)
PSRR > 65 dB
On-off-mute pop noise suppression
EMI optimized modulator
Short-circuit protection
Overtemperature protection
Low cost DMOS process

APPLICATIONS

Advanced televisions
Compact multimedia systems
Minicomponents

GENERAL DESCRIPTION

The AD1994 is a 2-channel, bridge tied load (BTL), switching audio power amplifier with integrated Σ-Δ modulator. The modulator accepts a single-ended, analog input signal and converts it to a switching waveform to drive speakers directly. One of the two modulators can control both output stages providing twice the current and almost twice the efficiency for single-channel applications. Both modulators can also control external power devices for arbitrarily high output power. A digital, microprocessor-compatible interface provides control of reset, mute, and PGA gain, as well as feedback signals for thermal and overcurrent error conditions. The output stage can operate over a power supply voltages range of 8 V to 20 V. The analog modulator and digital logic operate from a 5 V supply.

FUNCTIONAL BLOCK DIAGRAM

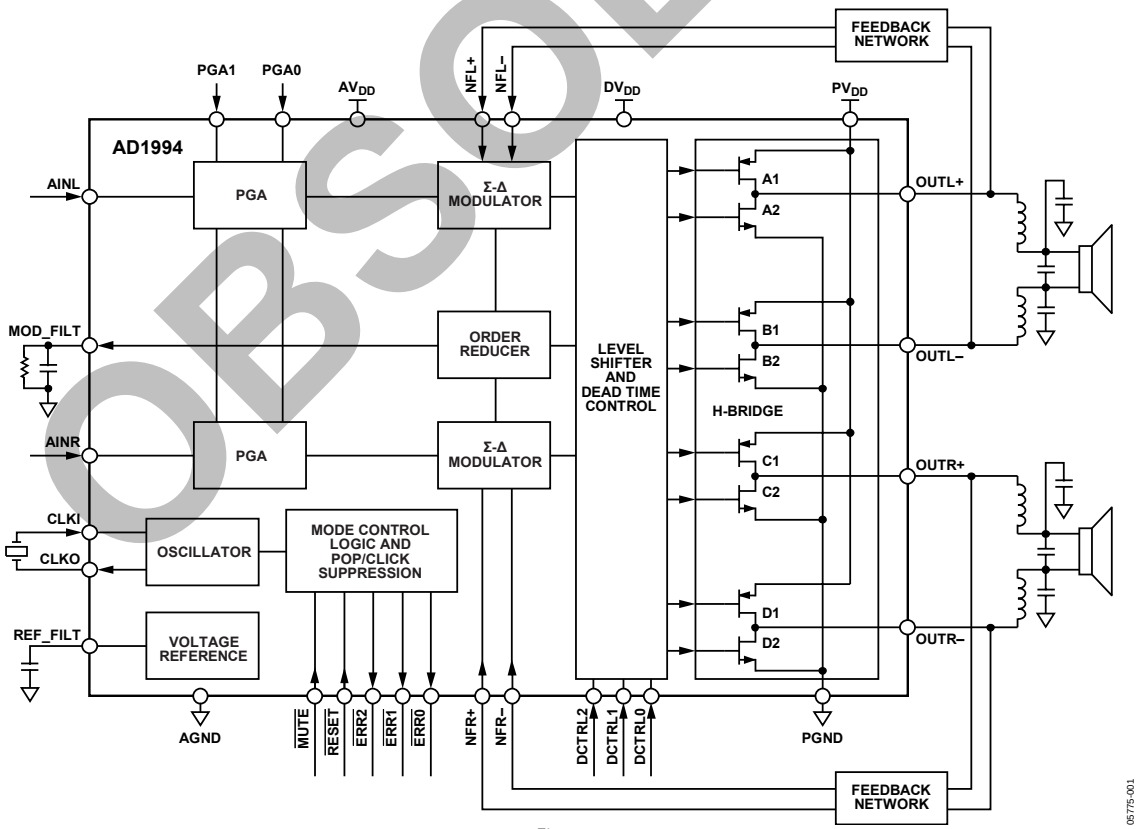


Figure 1.

Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113
©2006 Analog Devices, Inc. All rights reserved.

TABLE OF CONTENTS

Features 1
Applications 1
General Description 1
Functional Block Diagram 1
Revision History 2
Specifications 3
Absolute Maximum Ratings 5
ESD Caution 5
Pin Configuration and Function Descriptions 6
Typical Performance Characteristics 8
Theory of Operation 15
Overview 15
Σ-Δ Modulator 15
$\overline{\text{MUTE}}$ and $\overline{\text{RESET}}$ 15
Mono Mode 16
Modulator Mode 16
Gain Structure 16
Power Stage 17
Clocking 18
Protection Circuits and Error Reporting 19
Application Circuits 20
Outline Dimensions 21
Ordering Guide 21

OBSOLETE

REVISION HISTORY

2/06—Revision 0: Initial Version

SPECIFICATIONS

Test conditions, unless otherwise specified.

Table 1.

Parameter	Ratings
SUPPLY VOLTAGES	
AV_{DD}	5 V
DV_{DD}	5 V
PV_{DD}	12 V
AMBIENT TEMPERATURE	25°C
LOAD IMPEDANCE	6 Ω
CLOCK FREQUENCY	12.288 MHz
PGA GAIN	0 dB
MEASUREMENT BANDWIDTH	20 Hz to 20 kHz

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
R_{DS-ON}					
Per High-Side Transistor		260	355	mΩ	T = 25°C
Per Low-Side Transistor		210	265	mΩ	T = 25°C
MAXIMUM CURRENT THROUGH OUTx		5		A	Peak
THERMAL WARNING ACTIVE		135		°C	Die temperature
THERMAL SHUTDOWN ACTIVE		150		°C	Die temperature
RESTORE TEMPERATURE AFTER THERMAL SHUTDOWN		120		°C	Die temperature

Table 3. Performance Specifications

Parameter	Typ	Unit	Test Conditions/Comments
TOTAL HARMONIC DISTORTION AND NOISE (THD + N)	0.003	%	PGA = 0 dB, P_O = 1 W, 1 kHz
	0.006	%	PGA = 6 dB, P_O = 1 W, 1 kHz
	0.01	%	PGA = 12 dB, P_O = 1 W, 1 kHz
	0.02	%	PGA = 18 dB, P_O = 1 W, 1 kHz
SIGNAL-TO-NOISE RATIO (SNR)	105	dB	1 kHz, A-weighted, 0 dB referred to 1% THD + N output
DYNAMIC RANGE (DNR)	105	dB	1 kHz, A-weighted, –60 dB referred to 1% THD + N output
CROSSTALK (LEFT-TO-RIGHT OR RIGHT-TO-LEFT)	–100	dB	PGA = 0 dB, P_O = 5 W, 1 kHz

Table 4. DC Specifications

Parameter	Typ	Unit	Test Conditions/Comments
INPUT IMPEDANCE	20	kΩ	AINL, AINR input pins
OUTPUT DC OFFSET	±4	mV	Independent of PGA setting

OBSOLETE

Table 5. Power Supplies

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG SUPPLY, AV_{DD}	4.5	5.0	5.5	V	
DIGITAL SUPPLY, DV_{DD}	4.5	5.0	5.5	V	
POWER TRANSISTOR SUPPLY, PV_{DD}	6.5	8 to 20	22.5	V	
RESET/POWER-DOWN CURRENT					$\overline{\text{RESET}}$ held low
AV_{DD}		0.6	1	µA	5 V
DV_{DD}		7.5	11	µA	5 V
PV_{DD}		19	40	µA	12 V
QUIESCENT CURRENT					Inputs grounded, nonoverlap = minimum
AV_{DD}		20		mA	5 V
DV_{DD}		5.5		mA	5 V
PV_{DD}		30		mA	12 V
OPERATING CURRENT					V_{IN} = 1 V rms, R_L = 6 Ω, P_O = 1 W
AV_{DD}		20	27	mA	5 V
DV_{DD}		5.5	7	mA	5 V
PV_{DD}		218	260	mA	12 V

Table 6. Digital I/O

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT LOGIC HIGH	2.0			V	
INPUT LOGIC LOW			0.8	V	
OUTPUT LOGIC HIGH	2.4			V	@ 4 mA
OUTPUT LOGIC LOW			0.4	V	@ 4 mA
LEAKAGE CURRENT ON DIGITAL OUTPUTS			10	µA	

Table 7. Digital Timing

Parameter	Typ	Unit	Test Conditions/Comments
t_{MD}	10	µs	Delay after $\overline{\text{MUTE}}$ is asserted until output stops switching
t_{UD}	34	µs	Delay after $\overline{\text{MUTE}}$ is deasserted until output starts switching

OBSOLETE

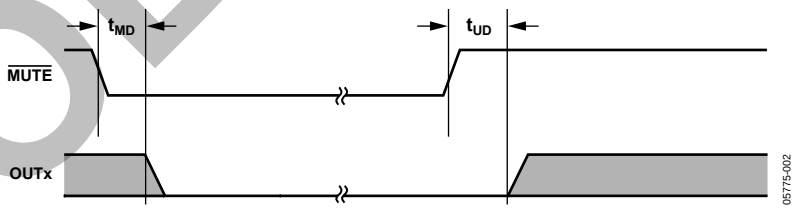


Figure 2. Mute and Unmute Delay Timing

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
AVDD, DVDD to AGND, DGND	−0.3 V to +6.5 V
PVDDx to PGNDx[1]	−0.3 V to +30.0 V
AGND to DGND to PGNDx	−0.3 V to +0.3 V
AVDD, to DVDD	−0.5 V to +0.5 V
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Maximum Junction Temperature	150°C
Thermal Resistance	
θ_{JA}	19.2°C/W
θ_{JC} (at the Exposed Pad Surface)	0.9°C/W
θ_{JB} (on JEDEC Standard PCB)	9.7°C/W

[1] Including any induced voltage due to inductive load.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OBSOLETE

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

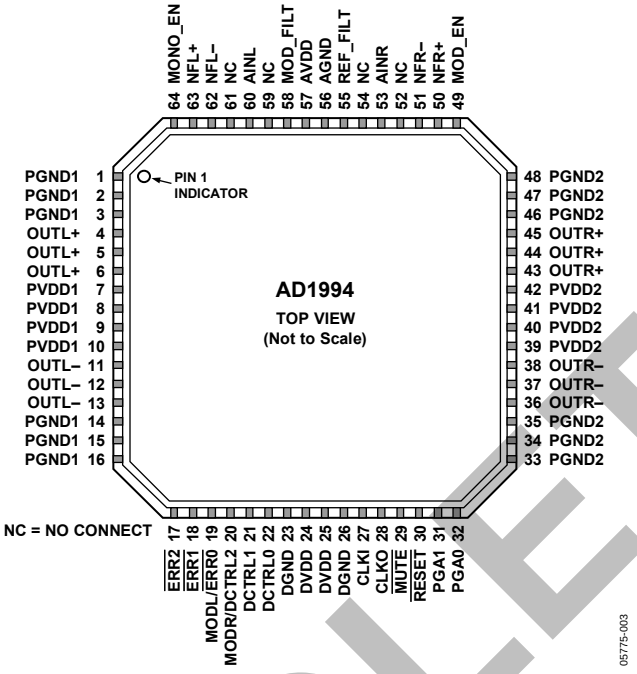


Figure 3. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	In/Out	Description
1, 2, 3	PGND1		Negative Power Supply. Used for the A2 and B2 high power transistors.
4, 5, 6	OUTL+	O	Output of Transistor Pair A1 and A2.
7, 8, 9, 10	PVDD1		Positive Power Supply. Used for the A1 and B1 high power transistors.
11, 12, 13	OUTL–	O	Output of Transistor Pair B1 and B2.
14, 15, 16	PGND1		Negative Power Supply. Used for the A2 and B2 high power transistors.
17	$\overline{\text{ERR2}}$	O	Active Low Thermal Shutdown.
18	$\overline{\text{ERR1}}$	O	Active Low Thermal Warning Error Output.
19	MODL/$\overline{\text{ERR0}}$	O	Active Low Overcurrent Error Output/Modulator Output Left.
20	MODR/DCTRL2	I/O	Nonoverlap Time Setting MSB/Modulator Output Right.
21	DCTRL1	I	Nonoverlap Time Setting.
22	DCTRL0	I	Nonoverlap Time Setting LSB.
23, 26	DGND		Negative Power Supply for Low Power Digital Circuitry.
24, 25	DVDD		Positive Power Supply for Low Power Digital Circuitry.
27	CLKI	I	Clock Input for 256 × f_S Audio Modulator Clock.
28	CLKO	O	Inverted Version of CLKI for Use with an External XTAL Oscillator.
29	$\overline{\text{MUTE}}$	I	Active Low Mute Input.
30	$\overline{\text{RESET}}$	I	Active Low Reset Input.
31	PGA1	I	PGA Gain Control MSB.
32	PGA0	I	PGA Gain Control LSB.
33, 34, 35	PGND2		Negative Power Supply for High Power Transistors C2 and D2.
36, 37, 38	OUTR–	O	Output of Transistor Pair D1 and D2.
39, 40, 41, 42	PVDD2		Positive Power Supply for High Power Transistors C1 and D1.
43, 44, 45	OUTR+	O	Output of Transistor Pair C1 and C2.
46, 47, 48	PGND2		Negative Power Supply for High Power Transistors C2 and D2.
49	MOD_EN	I	Modulator Mode Enable Pin when Pulled to Logic High.

OBSOLETE

Pin No.	Mnemonic	In/Out	Description
50	NFR+	I	Right Channel Negative Feedback—Noninverting Input.
51	NFR–	I	Right Channel Negative Feedback—Inverting Input.
52	NC		No Connection—Should Be Left Floating.
53	AINR	I	Analog Input for Right Channel.
54	NC		No Connection—Should Be Left Floating.
55	REF_FILT	O	Filter Pin for Band Gap Reference—Should Be Bypassed to AGND.
56	AGND		Negative Power Supply for Low Power Analog Circuitry.
57	AVDD		Positive Power Supply for Low Power Analog Circuitry.
58	MOD_FILT	O	Modulator Filter Pin—Used to Set Time Constant of Modulator Order Reduction Circuit.
59	NC		No Connection—Should Be Left Floating.
60	AINL	O	Analog Input for Left Channel.
61	NC		No connection—Should Be Left Floating.
62	NFL–	I	Left Channel Negative Feedback—Inverting Input.
63	NFL+	I	Left Channel Negative Feedback—Noninverting Input.
64	MONO_EN	I	Mono Mode Enable Pin—When Pulled Up to Logic High.

OBSOLETE

TYPICAL PERFORMANCE CHARACTERISTICS

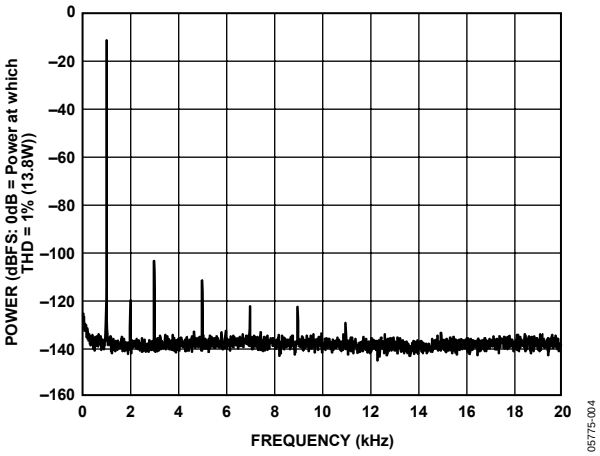


Figure 4. 1 W Output Power into 4 Ω Load

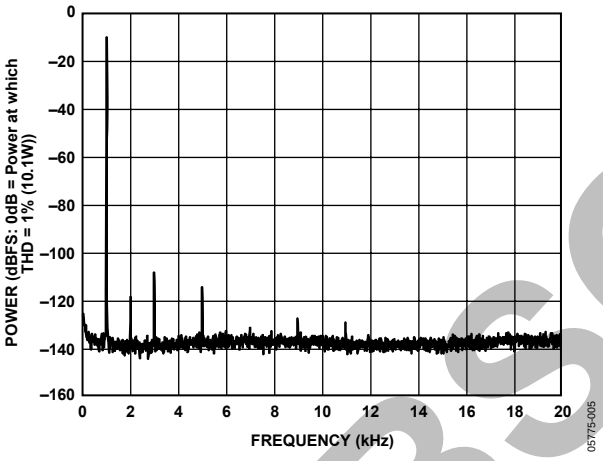


Figure 5. 1 W Output Power into 6 Ω Load

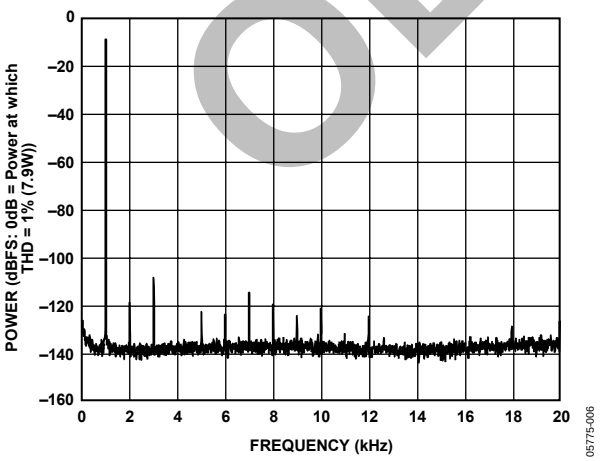


Figure 6. 1 W Output Power into 8 Ω Load

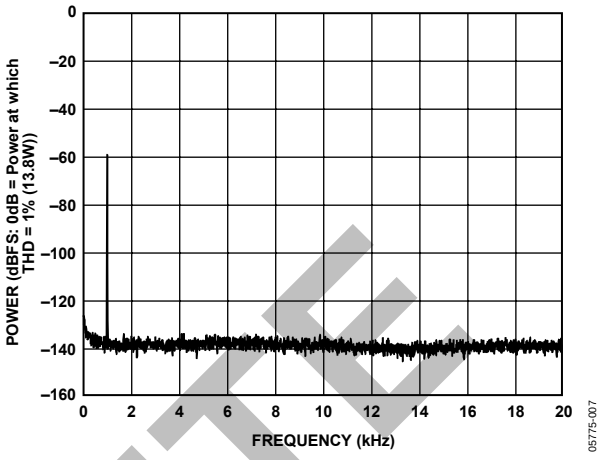


Figure 7. –60 dBFS Output Power into 4 Ω Load

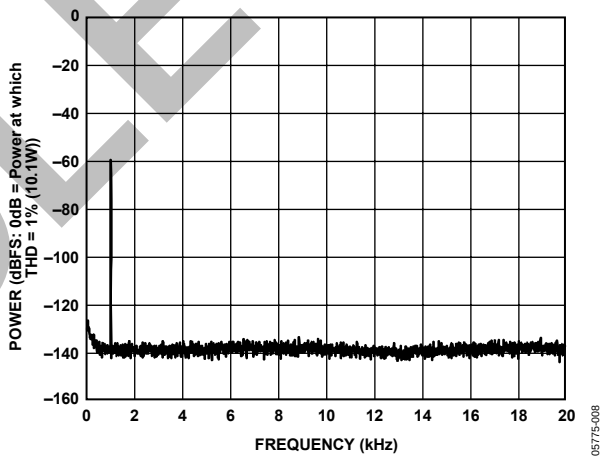


Figure 8. –60 dBFS Output Power into 6 Ω Load

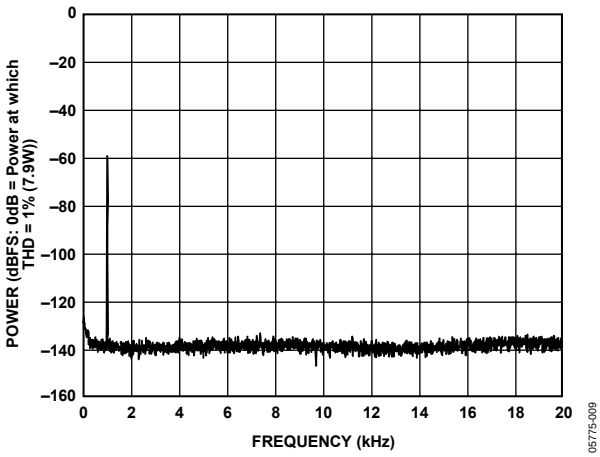


Figure 9. –60 dBFS Output Power into 8 Ω Load

OBSOLETE

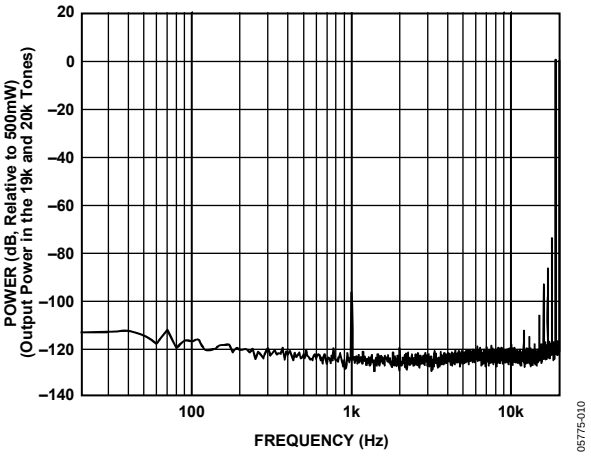


Figure 10. IMD for 19 kHz/20 kHz Twin-Tone Stimulus with 1 W Total Output Power

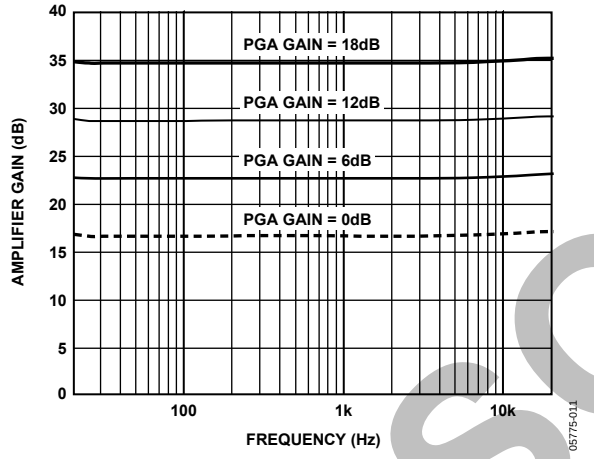


Figure 11. Amplifier Gain vs. Frequency, 6 Ω Load, PVDD = 12 V

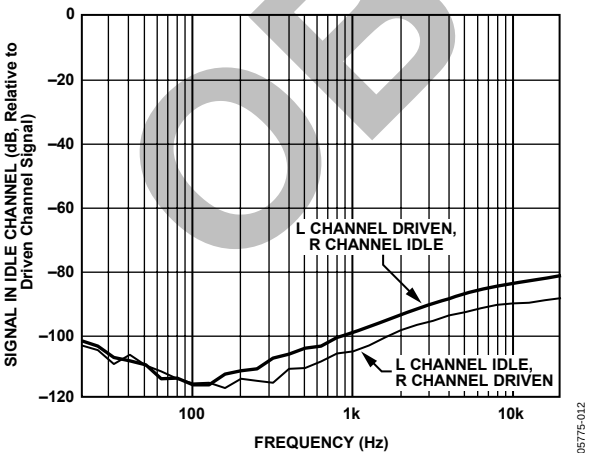


Figure 12. Channel Separation vs. Frequency, Driven Channel Has 1 W Output Power into 6 Ω Load

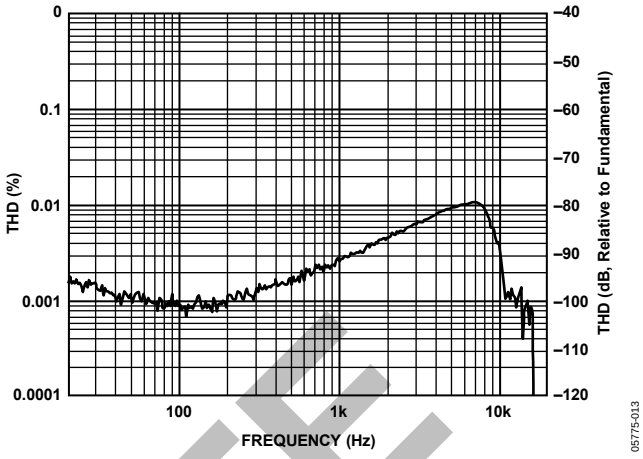


Figure 13. THD vs. Frequency, 1 W Output Power into 4 Ω Load, PVDD = 12 V

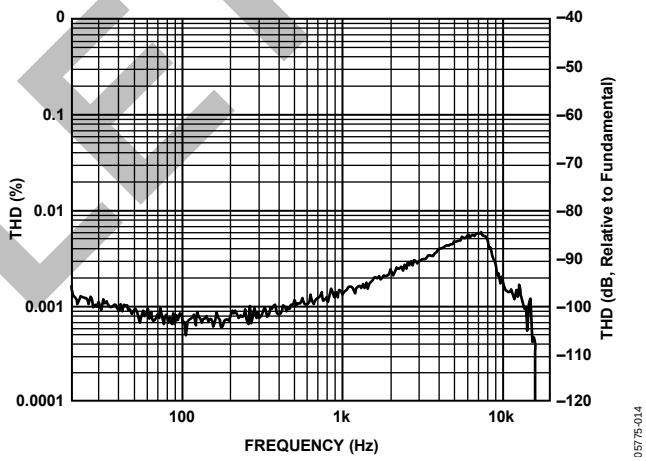


Figure 14. THD vs. Frequency, 1 W Output Power into 6 Ω Load, PVDD = 12 V

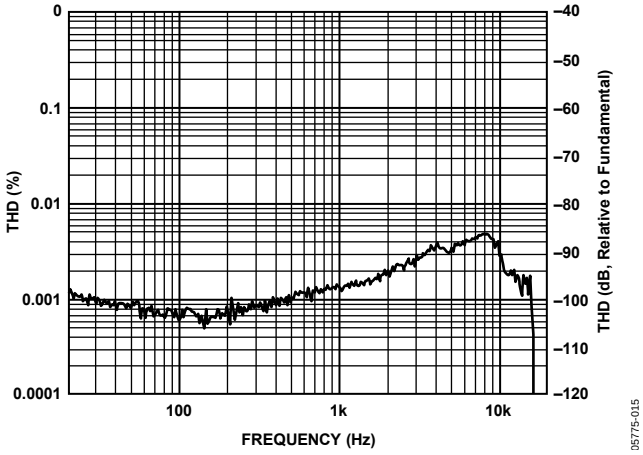


Figure 15. THD vs. Frequency, 1 W Output Power into 8 Ω Load, PVDD = 12 V

OBSOLETE

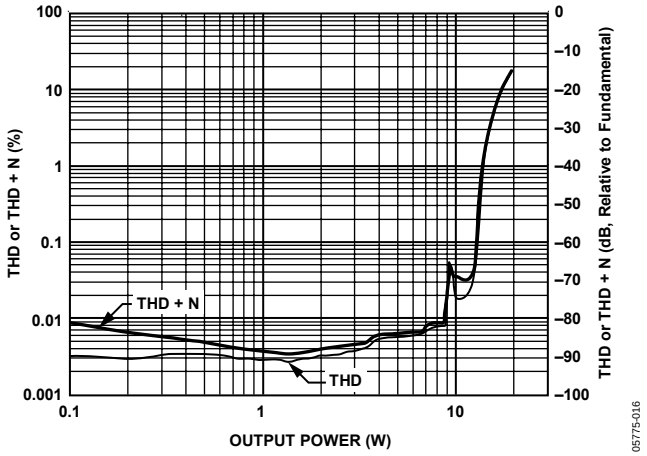


Figure 16. THD and THD + N vs. Output Power, 1 kHz Sine, 4 Ω Load, PVDD = 12 V

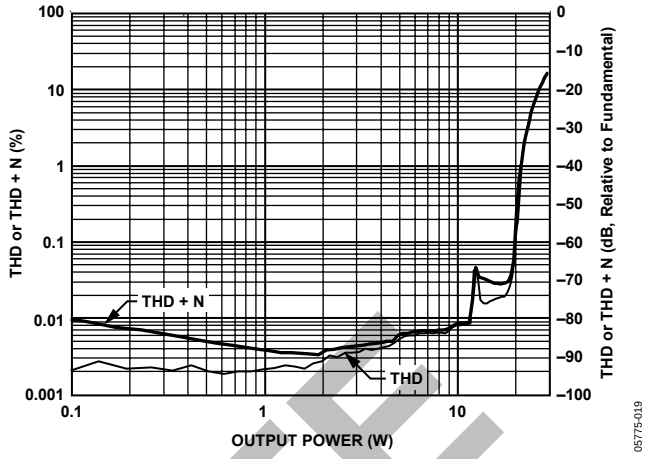


Figure 19. THD and THD + N vs. Output Power, 1 kHz Sine, 4 Ω Load, PVDD = 15 V

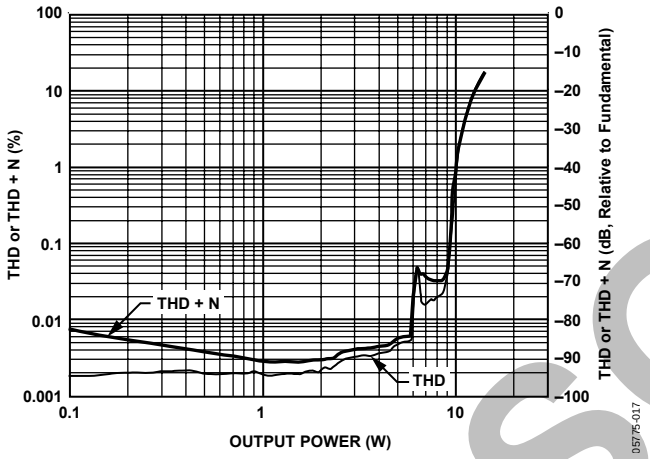


Figure 17. THD and THD + N vs. Output Power, 1 kHz Sine, 6 Ω Load, PVDD = 12 V

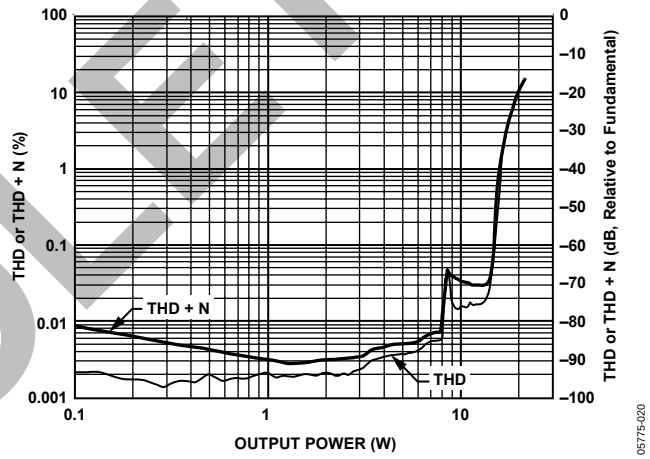


Figure 20. THD and THD + N vs. Output Power, 1 kHz Sine, 6 Ω Load, PVDD = 15 V

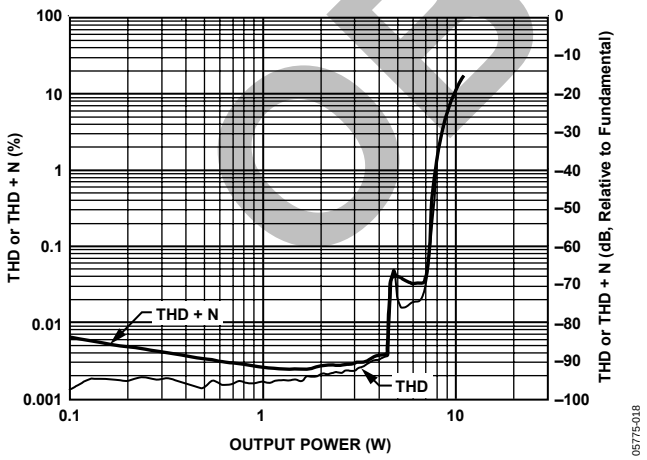


Figure 18. THD and THD + N vs. Output Power, 1 kHz Sine, 8 Ω Load, PVDD = 12 V

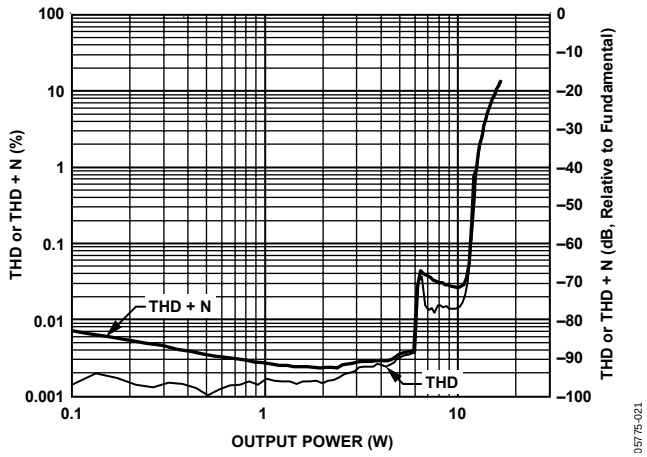


Figure 21. THD and THD + N vs. Output Power, 1 kHz Sine, 8 Ω Load, PVDD = 15 V

OBSOLETE

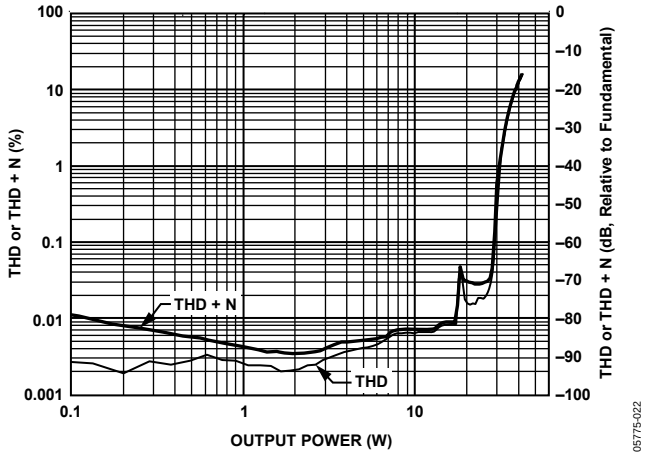


Figure 22. THD and THD + N vs. Output Power, 1 kHz Sine, 4 Ω Load, PVDD = 18 V

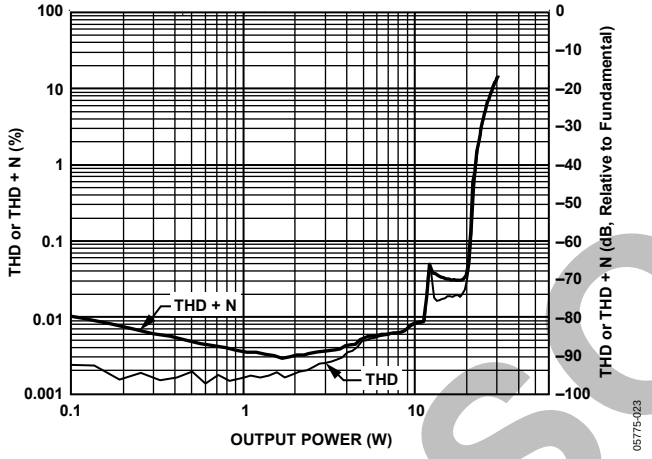


Figure 23. THD and THD + N vs. Output Power, 1 kHz Sine, 6 Ω Load, PVDD = 18 V

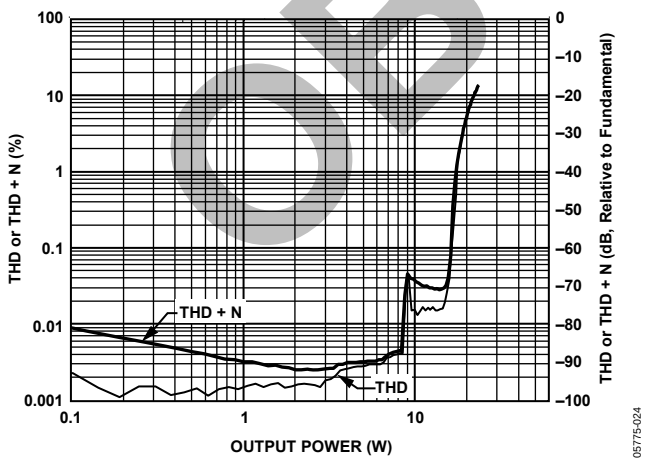


Figure 24. THD and THD + N vs. Output Power, 1 kHz Sine, 8 Ω Load, PVDD = 18 V

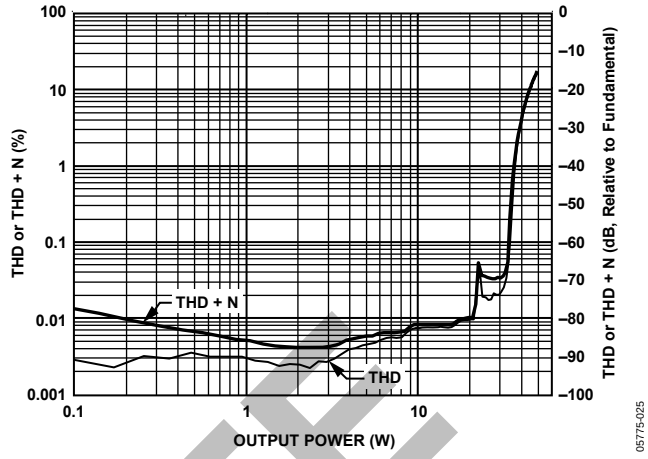


Figure 25. THD and THD + N vs. Output Power, 1 kHz Sine, 4 Ω Load, PVDD = 20 V

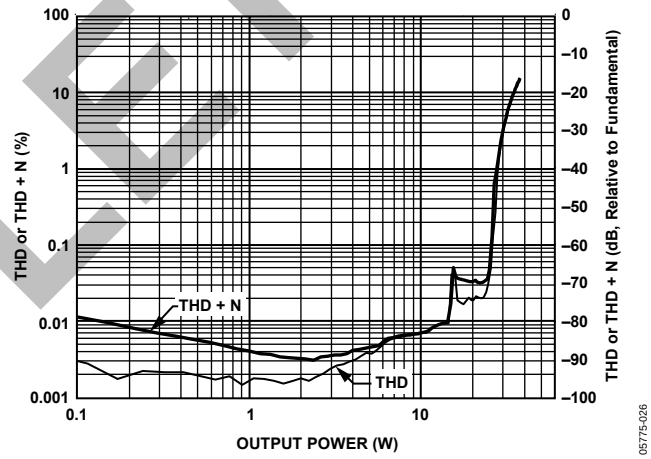


Figure 26. THD and THD + N vs. Output Power, 1 kHz Sine, 6 Ω Load, PVDD = 20 V

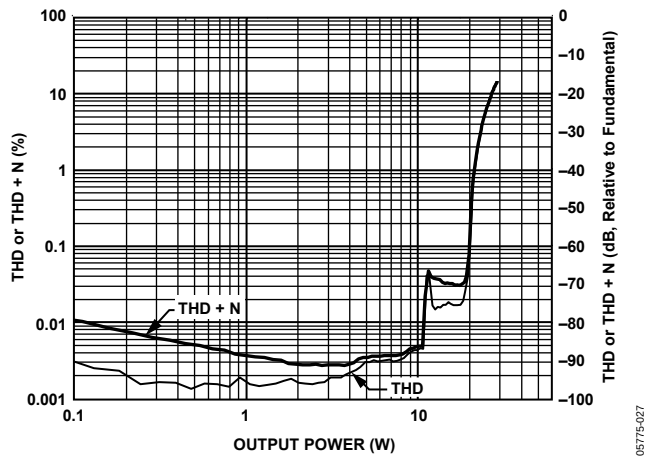


Figure 27. THD and THD + N vs. Output Power, 1 kHz Sine, 8 Ω Load, PVDD = 20 V

OBSOLETE

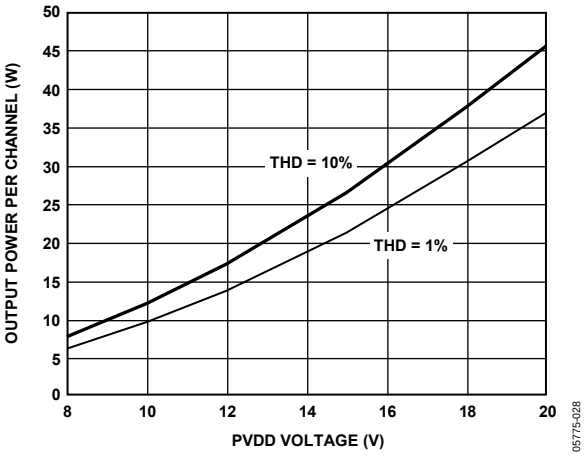


Figure 28. Maximum Power vs. PVDD, Stereo Mode, 4 Ω Load

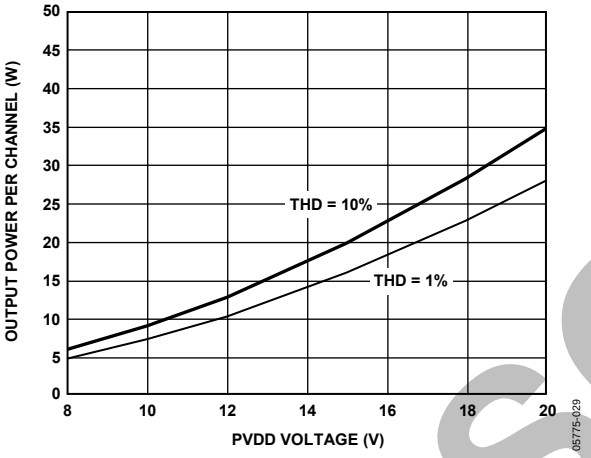


Figure 29. Maximum Power vs. PVDD, Stereo Mode, 6 Ω Load

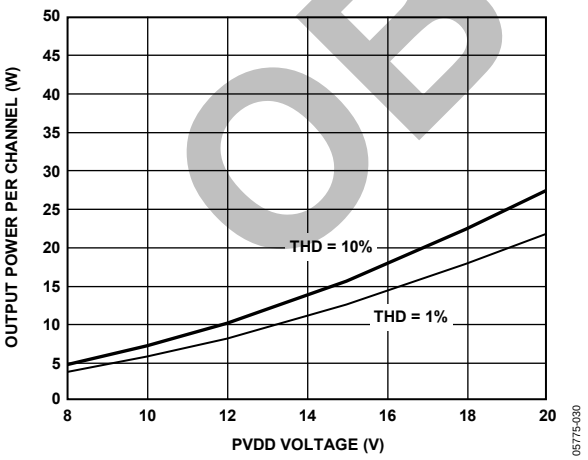


Figure 30. Maximum Power vs. PVDD, Stereo Mode, 8 Ω Load

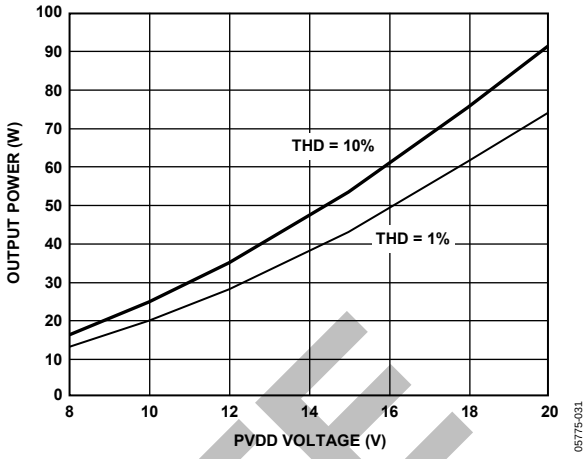


Figure 31. Maximum Power vs. PVDD, Mono Mode, 2 Ω Load

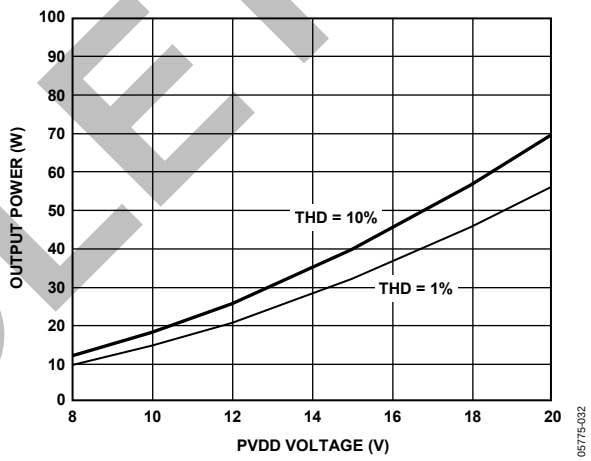


Figure 32. Maximum Power vs. PVDD, Mono Mode, 3 Ω Load

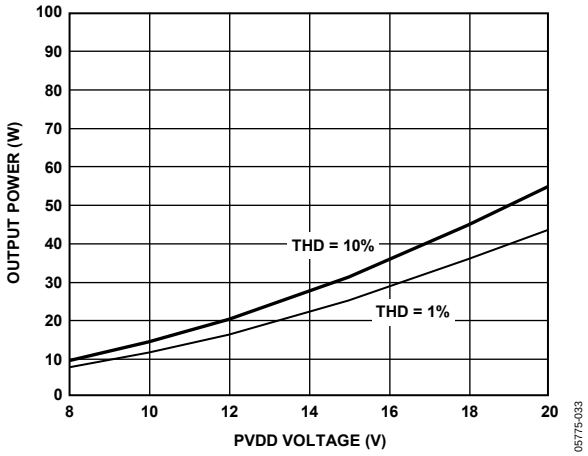


Figure 33. Maximum Power vs. PVDD, Mono Mode, 4 Ω Load

OBSOLETE

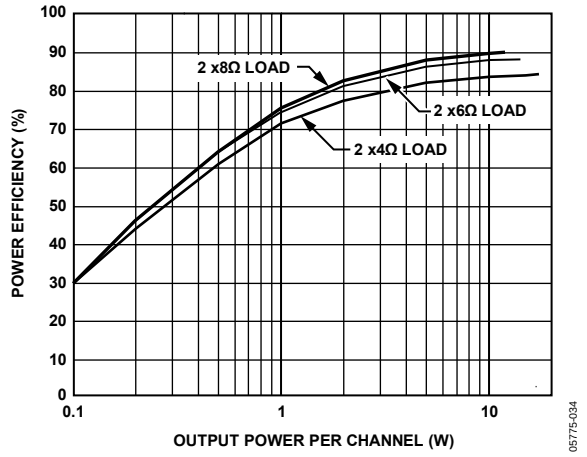


Figure 34. Power Efficiency vs. Output Power, Stereo Mode, PVDD = 12 V

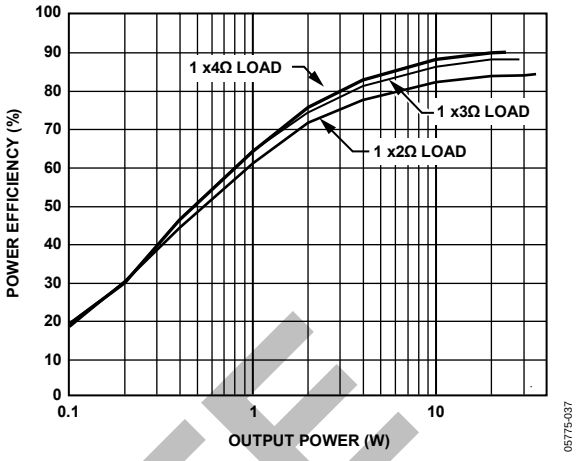


Figure 37. Power Efficiency vs. Output Power, Mono Mode, PVDD = 12 V

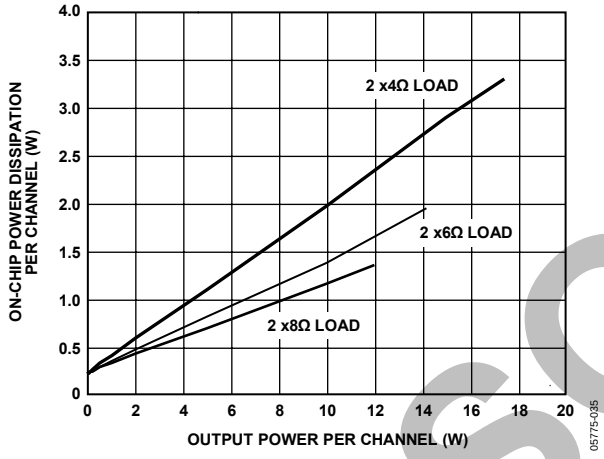


Figure 35. On-Chip Power Dissipation vs. Output Power, Stereo Mode, PVDD = 12 V

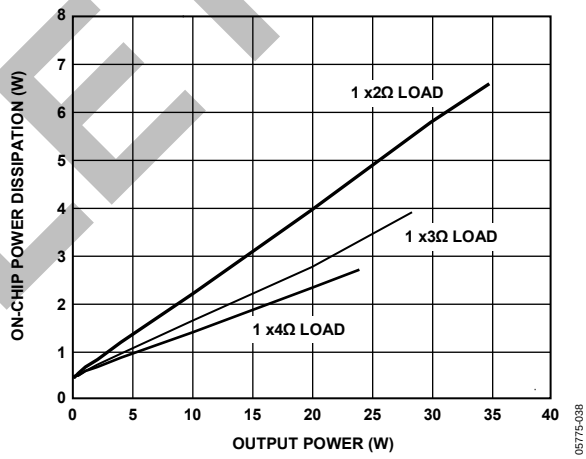


Figure 38. On-Chip Power Dissipation vs. Output Power, Mono Mode, PVDD = 12 V

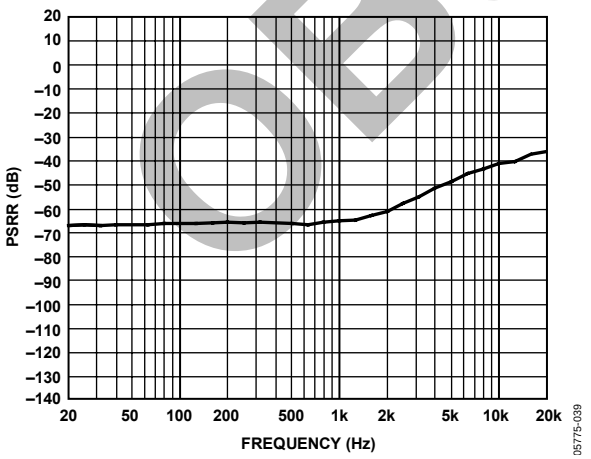


Figure 36. Power Supply Rejection Ratio (PSRR) vs. Frequency

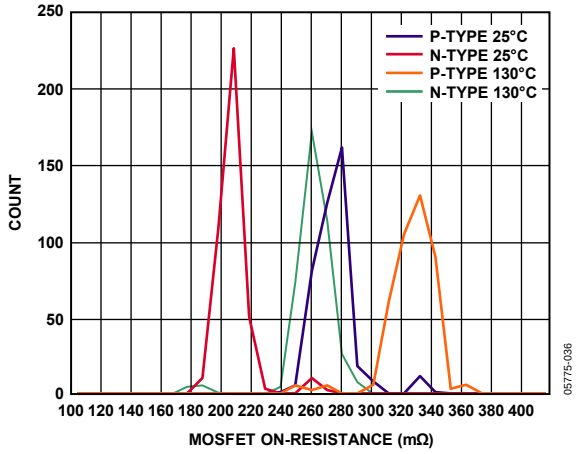


Figure 39. Histogram Showing Manufacturing Variation of R_{DS-ON} of the Output MOSFETS at 25°C and 130°C

OBSOLETE

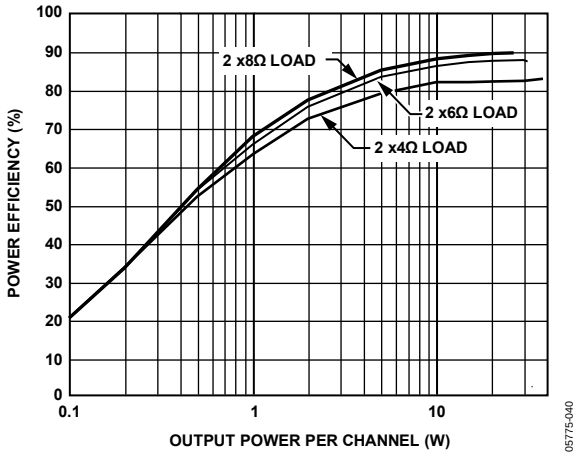


Figure 40. Power Efficiency vs. Output Power, Stereo Mode, PVDD = 18 V

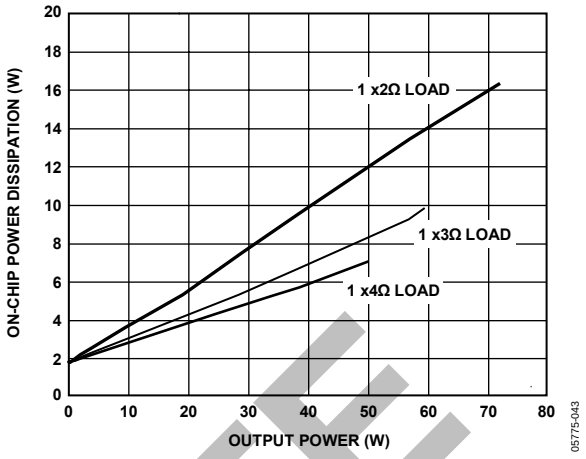


Figure 42. On-Chip Power Dissipation vs. Output Power, Mono Mode, PVDD = 18 V

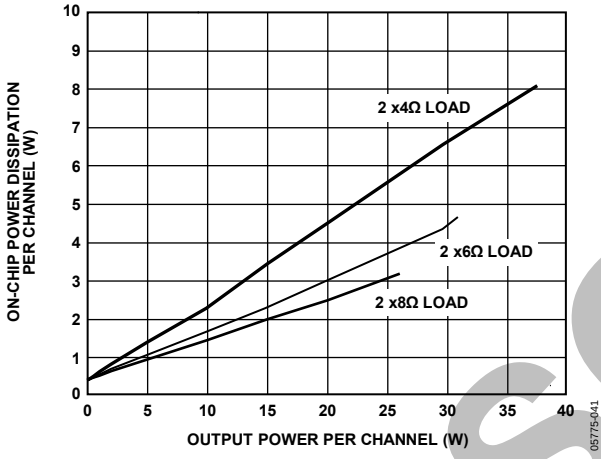


Figure 41. On-Chip Power Dissipation vs. Output Power, Stereo Mode, PVDD = 18 V

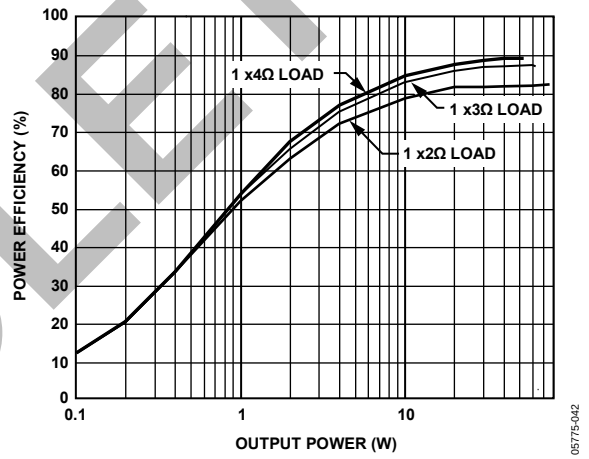


Figure 43. Power Efficiency vs. Output Power, Mono Mode, PVDD = 18 V

OBSOLETE

THEORY OF OPERATION

OVERVIEW

The AD1994 is a 2-channel, high performance, switching, audio power amplifier. Each of the two Σ-Δ modulators converts a single-ended analog input into a 2-level pulse stream that controls the differential, full H-bridge, power output stage. The combination of an Σ-Δ modulator and a switching power stage provides an inherently linear and efficient means of amplifying the entire range of audio frequencies. The AD1994 also offers warning and protection circuits for overcurrent and over-temperature conditions, as well as silent turn-on and turn-off transitions.

Σ-Δ MODULATOR

The AD1994 is a switching type, also known as a Class-D, audio power amplifier. This class of amplifiers maximizes efficiency by only using its power output devices in full-on or full-off states. While most Class-D amplifiers use some variation of pulse-width modulation (PWM), the AD1994 uses Σ-Δ modulation to determine the switching pattern of the output devices. This provides a number of important benefits. Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM frequency band as pulse-width modulators (PWM) often do. In addition, the 1-bit quantizer produces excellent linearity across the full amplitude range.

Σ-Δ modulators require feedback to generate an error signal with respect to the input. The feedback voltages for the AD1994 modulators come from the outputs of the power devices and before the passive low-pass filters (see Figure 45). This compensates for nonlinear behavior in the power stage, such as nonoverlap time, mismatched rise and fall times, and propagation delays. It also reduces sensitivity to both dc and transient changes of the power supply voltage.

Σ-Δ modulators operate in discrete time. As with all time-quantized systems, the Nyquist frequency is equal to half of the sampling frequency and input signals above that point aliases back into the base band. The AD1994 sampling frequency (master clock) is equal to half the frequency of the input clock, approximately 6 MHz, so images only alias for input frequencies above approximately 3 MHz. This is far enough above the audio band that bandwidth and aliasing are not a problem in real applications.

The AD1994 implements a seventh-order, Σ-Δ modulator with a 1-bit quantizer. Traditionally, higher-order designs such as this are not suitable for driving a Class-D amplifier because of stability problems at higher modulation factors. The modulator design of the AD1994 is unusual in that it is stable to 90% modulation. To allow the amplifier to drive even further, the AD1994 dynamically reverts from seventh order to second order above a fixed modulation threshold. The second-order modulator is unconditionally stable, including during prolonged voltage clipping conditions, enabling stable operation at full modulation. The dynamic-order reduction circuit uses the high-order modulator, except during the crests of the highest waveform peaks. During these peaks, the quantization noise increases, but the SNR is still quite high. These modulator order transitions are fast and smooth enough to avoid audible artifacts.

The modulator has a noise shaping effect, and SNR is increased in the audio band by shifting the quantization noise upward in frequency. For a nominal input clock frequency of 12.288 MHz, the noise floor rises sharply above 20 kHz. The actual clock frequency used in an application circuit can deviate from this rate by as much as ±10%, and the corner frequency of the noise scales proportionately. The frequency at which the quantization noise dominates the output determines the amplifier's practical bandwidth.

The expected transition rate at the output of a typical seventh-order, Σ-Δ modulator would be high enough to negate much of the efficiency benefit of a switching amplifier. However, the AD1994 incorporates a proprietary, dynamic, switching rate, reduction scheme that lowers that average switching frequency by approximately a factor of four. This results in slightly increased output energy between 450 kHz and 500 kHz and efficiency on par with other Class-D amplifiers. This low-Q spectral boost is an artifact of the noise shaping and is in no way related to the carrier frequency visible in the spectrum of PWM Class-D amplifiers.

$\overline{\text{MUTE}}$ AND $\overline{\text{RESET}}$

When power is applied and the $\overline{\text{RESET}}$ pin remains asserted, the AD1994 is in its lowest power consumption mode. The analog modulator is not running, and the power stage is tri-stated. On deasserting the $\overline{\text{RESET}}$ pin, the modulator begins a start-up sequence that includes initialization of the modulator, the protection circuits, and other functions.

Once the start-up sequence is complete, the amplifier is in a state in which the modulator is running, but the output stage is not driven. When $\overline{\text{MUTE}}$ is deasserted, the output is started using a soft-start sequence that avoids any audible pop or click noise in the output signal.

The output power transistors do not switch while $\overline{\text{MUTE}}$ remains asserted. Unlike the analog mute circuits found on some amplifiers that can be limited in their attenuation by the control logic or crosstalk, the mute attenuation on the AD1994 is greater than its dynamic range. The noise floor of the output signal also drops while in $\overline{\text{MUTE}}$ because the output transistors are not switching.

OBSOLETE

Power-Up Sequencing

Careful power-up is necessary when using the AD1994 to ensure correct operation and to avoid possible latch-up issues. The AD1994 should be powered up with $\overline{\text{RESET}}$ and $\overline{\text{MUTE}}$ held low until all the power supplies have stabilized. Once the supplies have stabilized, bring the AD1994 out of $\overline{\text{RESET}}$ by bringing $\overline{\text{RESET}}$ high.

Begin the soft unmute sequence by bringing $\overline{\text{MUTE}}$ high at least 1 sec after the $\overline{\text{RESET}}$ rising edge. The amplifier produces audio using a shorter start-up sequence (as shown in Table 7), but the amplifier can produce an audible pop or click noise as the output starts switching. This is because the ac coupling capacitors at the analog input have a long time constant. If $\overline{\text{MUTE}}$ is deasserted substantially less than 1 sec after deasserting $\overline{\text{RESET}}$, then these capacitors may not have charged to a steady state. They need ample time to settle at a bias voltage of V_{REF}, the reference voltage for the single-ended inputs, or the amplifier starts with a slight dc offset.

MONO MODE

The power supply voltage and the limited current that the output transistors can source combine to dictate that maximum total output power of the AD1994. For higher impedance loads, the system is voltage limited, and for lower impedance loads, the system is current limited. In normal stereo operation, each output is driven by four MOSFET devices arranged in a full H-bridge configuration, also known as bridge-tied load (BTL). This provides the maximum differential output voltage swing, equal to twice the voltage of the power supply. However, operating in mono mode doubles the maximum achievable output current.

When MONO_EN (Pin 64) is logic level high at the rising edge of $\overline{\text{RESET}}$, the right channel modulator is disabled, and the left channel modulator is used to drive both the left and right output stages in parallel. When using mono mode, connect OUTL+ directly to OUTR+, connect OUTL− directly to OUTR−, and use the combined differential pair to a drive a single load. Connect the feedback pair to the positive and negative feedback input of the left modulator. The right channel feedback pins are unused in mono mode. The $R_{DS\text{-}ON}$ of the power FETs drops to half of its value in stereo operation because the devices are in parallel, and the AD1994 delivers its full current capability to a single channel.

Note that the practical effect of mono mode depends greatly on the load impedance. If the load is 4 Ω or greater, the efficiency of the amplifier increases due to the reduced effective resistance of power FETs, and the amplifier dissipates less heat. However, the amount of real power delivered to the load does not increase because the system is voltage limited (that is, the output waveform voltage clips before current limiting occurs).

When the load impedance is substantially less than 4 Ω, the system would be current limited if configured for normal stereo operation, and the amplifier would enter the overcurrent error state when a nominal input signal is applied. Under these conditions, the amount of real power delivered to the load increases in mono mode. The minimum recommended impedance in mono mode is 2 Ω (as compared to 4 Ω for stereo operation), so the effective power delivered to a single channel can be as much as twice the maximum achievable in stereo mode.

For reactive loads, the impedance can only be below the recommended threshold over a small portion of the amplifier's bandwidth. In these cases, the amplifier can enter overcurrent shutdown in response to even small input signals in those frequency bands. When designing a system, use the minimum load impedance over the entire range of amplified frequencies when calculating current output rather than the average or nominal load impedance ratings often cited by loudspeaker driver manufacturers.

MODULATOR MODE

The AD1994 is capable of operating as a modulator for controlling external power devices. When MOD_EN (Pin 49) is logic level high at the rising edge of $\overline{\text{RESET}}$, both the left and right internal power stages are disabled. The error output flags ($\overline{\text{ERR2}}$, $\overline{\text{ERR1}}$, and $\overline{\text{ERR0}}$) and the nonoverlap delay inputs (DCNTL2, DCNTL1, and DCNTL0) no longer have meaning because they apply only to the internal power stages. The logic level outputs from the two modulators appear on Pin 19 (MODL) and Pin 20 (MODR).

GAIN STRUCTURE

Analog Input Levels

The AD1994 has single-ended inputs for the left and right channels. The analog input section uses an internal amplifier to bias the input signal to the reference level, V_{REF}, which is nominally equal to $AV_{DD}/2$. A dc-blocking capacitor, as shown in Figure 44, prevents this bias voltage from affecting the signal source. In combination with the nominal 20 kΩ input impedance, the value of this capacitor should be large enough to produce a flat frequency response at the lowest input frequency of interest. Note that the amplifier is capable of dc-coupled operation if the circuit includes some means to account for this bias voltage.

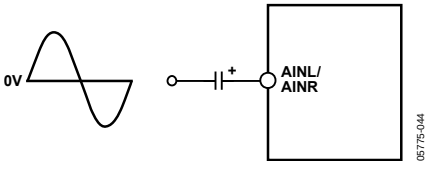


Figure 44. AC-Coupled Input Signal

OBSOLETE

Setting the Modulator Gain

The AD1994 modulator uses a combination of the input signal and feedback from the power output stage to calculate its two-state output pattern. The feedback input nodes are part of the internal analog circuit that operates from the AV_{DD} (nominal 5 V) power supply. Because the voltage measured at the power outputs is nominally between 0 V and PV_{DD}, and thus beyond the 0 V to AV_{DD} range, a voltage divider is required to scale the feedback to an appropriate level.

Resistor voltage dividers should sense the voltage on each side of the differential output and provide these feedback signals to the modulator, as shown in Figure 45.

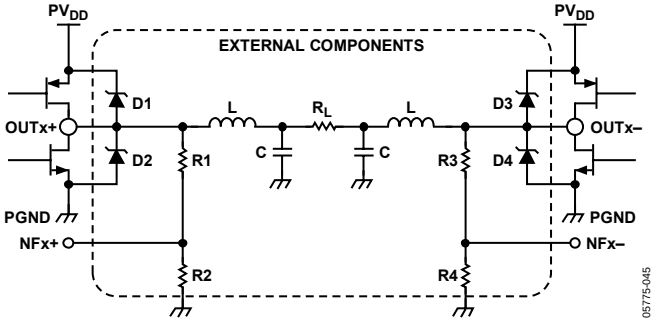


Figure 45. H-Bridge Configuration

The resistor values should satisfy the following equation to maintain modulator stability.

$$Gain = \frac{R1 + R2}{R2} = \frac{R3 + R4}{R4} = \frac{PV_{DD}}{3.635}$$

Selecting a gain that meets this criterion ensures that the modulator remains in a stable operating condition.

The ratio of the resistances sets the gain rather than the absolute values. However, the dividers provide a path from the high voltage supply to ground; therefore, the values should be large enough to produce negligible loss due to quiescent current.

The chip contains a calibration circuit to minimize voltage offsets at the speaker, which helps to minimize clicks and pops when muting or unmuting. Optimal performance is achieved for the offset calibration circuit when the feedback divider resistors sum to 6 kΩ, that is, (R1 + R2) = 6 kΩ, and (R3 + R4) = 6 kΩ.

Table 10. Recommended Feedback Resistor Values

PV_{DD} (V)	R1 (kΩ)	R2 (kΩ)	Gain
12	4.2	1.8	3.3 (+10.4 dB)
15	4.55	1.45	4.1 (+12.3 dB)
18	4.8	1.2	5.0 (+14.0 dB)
20	4.91	1.09	5.5 (+14.8 dB)

Programmable Gain Amplifier (PGA)

The Σ-Δ modulator itself requires a fixed gain for a given value of PV_{DD} to maintain optimal stability. This gain can be appropriate, but many applications require more gain to account for low source signal levels. The AD1994 includes a programmable gain amplifier (PGA) to boost the overall amplifier gain. PGA1 (Pin 31) and PGA0 (Pin 32) select one of four PGA gain values, as shown in Table 11.

Table 11. PGA Gain Settings

PGA1	PGA0	PGA Gain (dB)
0	0	0
0	1	6
1	0	12
1	1	18

The AD1994 incorporates a single-ended-to-differential converter for each channel in the analog front-end section. The PGA is also part of this analog front-end, and it affects the analog input signal before it enters the Σ-Δ modulator. The PGA1 and PGA0 pins are continuously monitored and allow the gain to be changed at any time.

POWER STAGE

The H-Bridge

The output stage of the AD1994 includes four integrated MOSFET devices arranged in a full H-bridge, as shown in Figure 45. The P-Type, high-side transistor of one leg and the N-Type, low-side transistor of the opposite leg switch on and off as a pair producing a total voltage swing across the load of $-PV_{DD}$ to $+PV_{DD}$. The drive is floating and differential, and it is important that neither output terminal be shorted to ground.

The power supply for the output stage of the AD1994, PV_{DD}, should be in the 8 V to 20 V range and should be capable of supplying enough current to drive the load. Connect the power supply across the PVDD and PGND pins. The feedback pins, NFR+, NFR−, NFL+, and NFL−, supply negative feedback to the modulator as described in the Setting the Modulator Gain section.

OBSOLETE

Output Transistor Nonoverlap Time

The AD1994 allows the user to select from one of eight different nonoverlap times, as shown in Figure 46. Nonoverlap time prevents or minimizes the period during which both the high-side and low-side devices are on simultaneously due to propagation delays and nonzero rise and fall times. If both the upper and lower portions of a half-bridge conduct simultaneously, there is a path directly from the power supply to ground and an induced current flow known as shoot-through. However, introducing this delay increases distortion by pushing the switching pattern further from an ideal two-state waveform. Selecting the nonoverlap delay requires a compromise between distortion and efficiency. The logic levels on the three delay control pins, DCTRL2, DCTRL1, and DCTRL0, set the nonoverlap time according to Table 12. The state of DCTRL[2:0] is read on the rising edge of $\overline{\text{RESET}}$ and should not be changed while $\overline{\text{RESET}}$ is logic high.

Table 12. Nonoverlap Time Settings

DCTRL2	DCTRL1	DCTRL0	Nonoverlap Time (ns)[1]
0	0	0	62
0	0	1	49
0	1	0	37
0	1	1	24
1	0	0	15
1	0	1	13.5
1	1	0	12
1	1	1	9

[1] Values are typical and are not production tested.

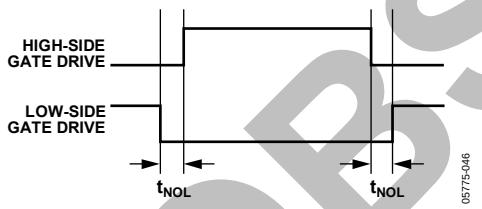


Figure 46. Half-Bridge Nonoverlap Delay Timing

The shortest setting (DCTRL[2:0] = 111) or the second shortest setting (DCTRL[2:0] = 111) is recommended for most applications. These two settings allow a small trade-off between efficiency and distortion. Longer nonoverlap times generally increase distortion while providing little or no decrease in shoot-through current.

CLOCKING

The AD1994 Σ-Δ modulator requires an external clock source with a nominal frequency of 12.288 MHz. This clock can come from a crystal or from an existing clock signal in the application circuit. The discrete time portions of the modulator run internally at 6.144 MHz, corresponding to 128 × f_S, where f_S = 48 kHz.

As mentioned in the Σ-Δ Modulator section, the modulator has a noise-shaping effect such that SNR is increased within the audio band by shifting modulator quantization noise upward in frequency. For external clock frequency of 12.288 MHz, the modulator's noise-shaping works in a manner that results in a flat noise floor at the amplifier output for frequencies 20 kHz and below. Above 20 kHz, the amplifier noise rises due to the spectral shaping of the modulator quantization noise. At very high frequencies, the noise floor levels off and decreases due to poles in the modulator noise-transfer function and in the external LC filter.

The clock frequency does not have to be exactly equal to 12.288 kHz and can vary by up to ±10%. For other rates, the noise corner scales linearly with frequency. When the modulator runs at a rate lower than nominal, the average power stage switching frequency decreases, the efficiency increases slightly, and the noise floor begins to rise at a slightly lower frequency. Likewise, a faster clock gives slightly increased bandwidth and slightly lower efficiency.

Using a Crystal Oscillator

The AD1994 can use a crystal connected to the CLKI and CLKO pins as a master clock source, as shown in Figure 47. The CLKI and CLKO pins connect to an internal inverter to create a full resonator. The typical values shown work in many applications, but the crystal manufacturer should provide the exact type and value of the capacitors and the resistor.

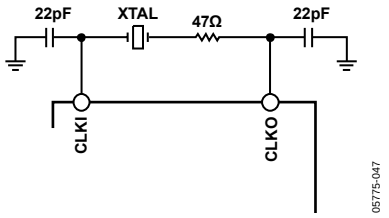


Figure 47. Crystal Connection

Using an External Clock Source

If a clock signal of the appropriate frequency already exists in the application circuit, connect it directly to CLKI and leave CLKO floating. The logic levels of the square wave should be compatible with those defined in Specifications section.

Large amounts of jitter on the clock input degrade performance. Whenever possible, avoid passing the clock signal though programmable logic and other circuits with unknown or variable propagation delay. In general, clock signals suitable for audio ADCs or DACs are also appropriate for use with the AD1994.

OBSOLETE

Clocking Multiple Amplifiers in Parallel

If there are multiple AD199x family amplifiers connected to the same PV_{DD} supply, use the same clock source (or synchronous derivatives) for each amplifier as previously described. Avoid clocking amplifiers from similar but asynchronous clocks if they use the same power supply because this can result in beat frequencies.

PROTECTION CIRCUITS AND ERROR REPORTING

Thermal Protection

The AD1994 features thermal protection. When the die temperature exceeds approximately 135°C, the thermal warning error output ($\overline{ERR1}$) is asserted. If the die temperature exceeds approximately 150°C, the thermal shutdown error output ($\overline{ERR2}$) is asserted. If this occurs, the part shuts down to prevent damage to the part. When the die temperature drops below approximately 120°C, the part returns to normal operation automatically and negates both error outputs.

Overcurrent Protection

The AD1994 features over current or short-circuit protection. If the current through any power transistors exceeds approximately 4 A, the part enters a mute state and the overcurrent error output ($\overline{ERR0}$) is asserted. This is a latched error and does not clear automatically. Restore normal operation and clear the error condition by either asserting and then negating $\overline{RESET}$ or by asserting and then negating $\overline{MUTE}$.

OBSOLETE

APPLICATION CIRCUITS

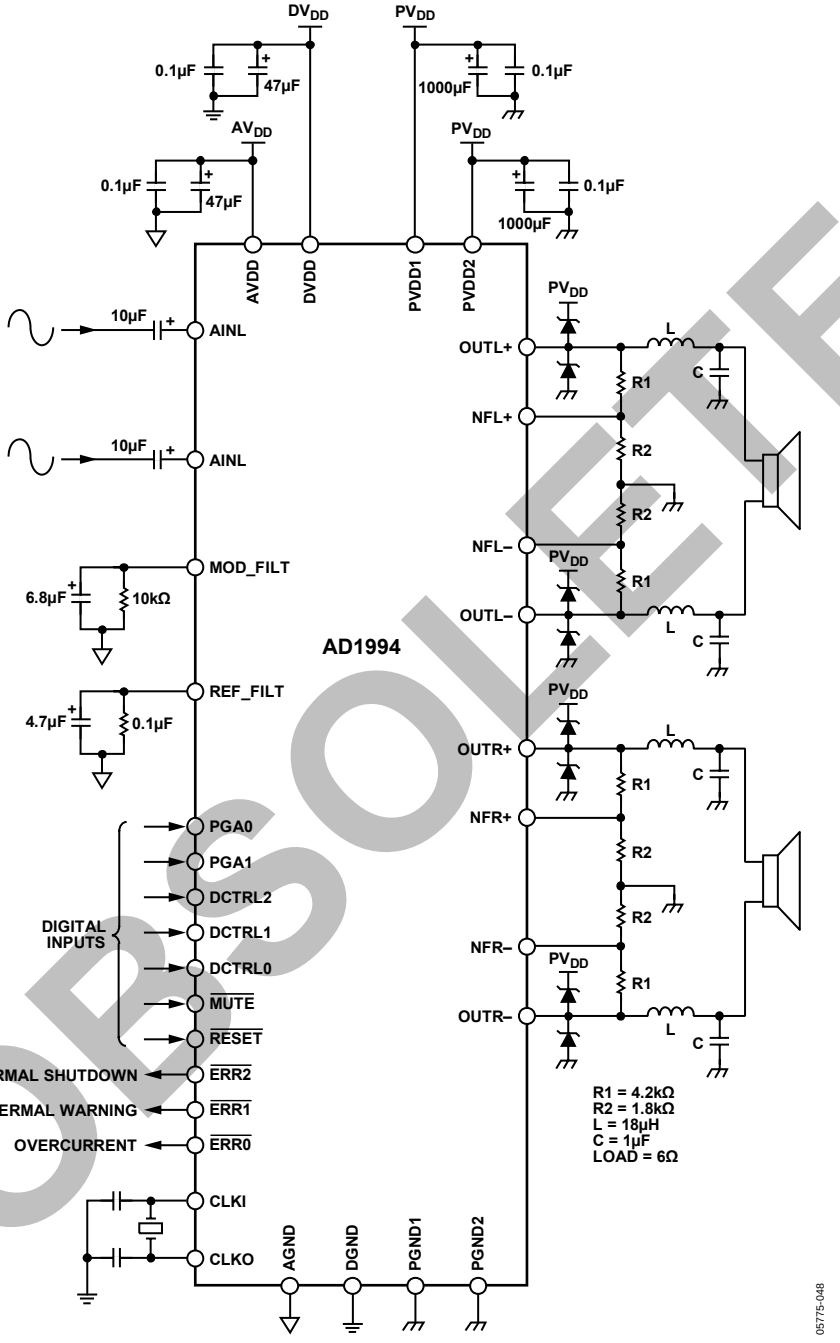


Figure 48. Typical Stereo Circuit

OBSOLETE

OUTLINE DIMENSIONS

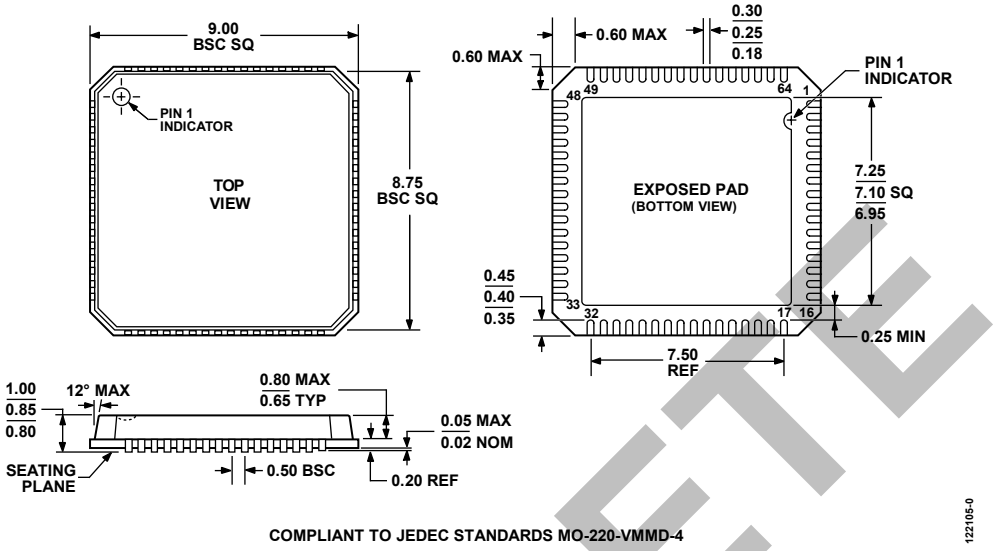


Figure 49. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-3)
Dimension shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1994ACPZ[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-3
AD1994ACPZRL[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ), 13″ Tape and Reel	CP-64-3
AD1994ACPZRL7[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ), 7″ Tape and Reel	CP-64-3
EVAL-AD1994EB		Evaluation Board	

[1] Z = Pb-free part.

OBSOLETE

NOTES

OBSOLETE

NOTES

OBSOLETE

NOTES

OBSOLETE

©2006 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D05775-0-2/06(0)