CS61535A

T1/E1 Line Interface

Features

- Provides Analog PCM Line Interface for T1 and E1 Applications
- Provides Line Driver, and Data and Clock Recovery Functions
- Transmit Side Jitter Attenuation Starting at 6 Hz, with > 300 UI of Jitter Tolerance
- Low Power Consumption (typically 175 mW)
- B8ZS/HDB3/AMI Encoders/Decoders
- 14 dB of Transmitter Return Loss
- Compatible with SONET, M13 , CCITT G.742, and Other Asynchronous Muxes

General Description

The CS61535A combines the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply.

The device features a transmitter jitter attenuator making it ideal for use in asynchronous multiplexor systems with gapped transmit clocks. The CS61535A provides a matched, constant impedance output stage to insure signal quality on mismatched, poorly terminated lines.

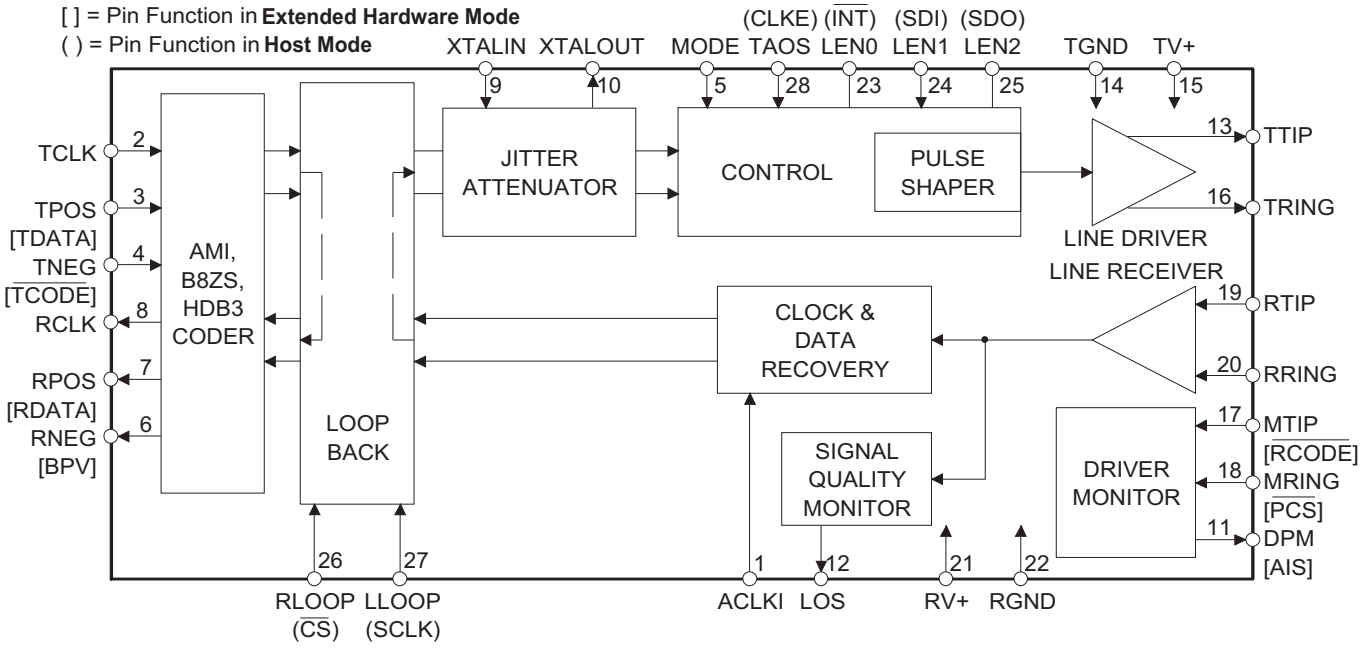
The IC uses a digital Delay-Locked-Loop clock and data recovery circuit which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance.

Applications

- Interfacing network transmission equipment such as SONET multiplexor and M13 to a DSX-1 cross connect.
- Interfacing customer premises equipment to a CSU.
- Interfacing to E1 links.

Ordering Information

CS61535A-IL1Z 28 Pin PLCC (Lead-free)



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ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply (referenced to RGND,TGND=0V)		RV+ TV+	- -	6.0 (RV+) + 0.3	V V
Input Voltage, Any Pin	(Note 1)	V_{in}	RGND-0.3	(RV+) + 0.3	V
Input Current, Any Pin	(Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature		T_A	-40	85	°C
Storage Temperature		T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:
1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
DC Supply	(Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature		T_A	-40	25	85	°C
Power Consumption	(Notes 4, 5)	P_C	-	290	350	mW
Power Consumption	(Notes 4, 6)	P_C	-	175	-	mW

Notes:
3. TV+ must not exceed RV+ by more than 0.3V.
4. Power consumption while driving line load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF load.
5. Assumes 100% ones density and maximum line length at 5.25V.
6. Assumes 50% ones density and 300ft. line length at 5.0V.

DIGITAL CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage Pins 1-4, 17, 18, 23-28 (Notes 7, 8, 9)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage Pins 1-4, 17, 18, 23-28 (Notes 7, 8, 9)	V_{IL}	-	-	0.8	V
High-Level Output Voltage (I_{OUT} = -40 µA) Pins 6-8, 11, 12, 25 (Notes 7, 8, 10)	V_{OH}	4.0	-	-	V
Low-Level Output Voltage (I_{OUT} = 1.6 mA) Pins 6-8, 11, 12, 23, 25 (Notes 7, 8, 10)	V_{OL}	-	-	0.4	V
Input Leakage Current (Except Pin 5)		-	-	±10	µA
Low-Level Input Voltage, Pin 5	V_{IL}	-	-	0.2	V
High-Level Input Voltage, Pin 5	V_{IH}	(RV+) - 0.2	-	-	V
Mid-Level Input Voltage, Pin 5 (Note 11)	V_{IM}	2.3	-	2.7	V

Notes:
7. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40µA).
8. In Host Mode, pin 23 is an open drain output and pin 25 is a tristate output.
9. Pins 17 and 18 of the CS61535A are digital inputs in the Extended Hardware Mode.
10. Output drivers will drive CMOS logic levels into a CMOS load.
11. As an alternative to supplying a 2.3-to-2.7V input, this pin may be left floating.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Jitter Attenuator					
Jitter Attenuation Curve Corner Frequency (Note 12)		-	6	-	Hz
T1 Jitter Attenuation in Remote Loopback (Note 13)					
Jitter Freq. [Hz]	Amplitude [UIpp]				
10	10	3.0	6.0	-	dB
100	10	20	30	-	dB
500	10	35	35	-	dB
1k	5	40	50	-	dB
10k, 40k	0.3	40	50	-	dB
E1 Jitter Attenuation in Remote Loopback (Note 14)					
Jitter Freq. [Hz]	Amplitude [UIpp]				
10	1.5	3.0	6.0	-	dB
100	1.5	20	32	-	dB
400	1.5	30	43	-	dB
1k	1.5	35	50	-	dB
10k, 100k	0.2	35	50	-	dB
Attenuator Input Jitter Tolerance (Note 15)		12	23	-	UI

Notes:
12. Not production tested. Parameters guaranteed by design and characterization.
13. Attenuation measured at the demodulator output of an HP3785B with input jitter equal to 3/4 of measured jitter tolerance using a measurement bandwidth of 1 Hz (10<f<100Hz), 4Hz (100<f<1000 Hz) and 10 Hz (f> 1kHz) centered around the jitter frequency. With a 2^{15}-1 PRBS data pattern. Crystal must meet specifcations in Appendix A.
14. Jitter measured at the demodulator output of an HP3785A using a measurement bandwidth not to exceed 20 Hz centered around the jitter frequency. With a 2^{15}-1 PRBS data pattern. Crystal must meet specifications in Appendix A.
15. Output jitter increases significantly when attenuator input jitter tolerance is exceeded.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Transmitter					
AMI Output Pulse Amplitudes	(Note 16)				
E1, 75 Ω	(Note 17)	2.14	2.37	2.6	V
E1, 120 Ω	(Note 18)	2.7	3.0	3.3	V
T1, FCC Part 68	(Note 19)	2.7	3.0	3.3	V
T1, DSX-1	(Note 20)	2.4	3.0	3.6	V
E1 Zero (space) level (LEN2/1/0 = 0/0/0)					
75Ω application	(Note 17)	-0.237	-	0.237	V
120Ω application	(Note 18)	-0.3	-	0.3	V
Recommended Output Load at TTIP and TRING		-	75	-	Ω
Jitter Added During Remote Loopback	(Note 21)				
10Hz - 8kHz		-	0.005	0.02	UI
8kHz - 40kHz		-	0.008	0.025	UI
10Hz - 40kHz		-	0.010	0.025	UI
Broad Band		-	0.015	0.05	UI
Power in 2kHz band about 772kHz	(Notes 12, 16)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (referenced to power in 2kHz band at 772kHz)	(Notes 12, 16)	-29	-38	-	dB
Positive to Negative Pulse Imbalance	(Notes 12, 16)				
T1, DSX-1		-	0.2	0.5	dB
E1 amplitude at center of pulse		-5	-	5	%
E1 pulse width at 50% of nominal amplitude		-5	-	5	%
Transmitter Return Loss	(Notes 12, 16, 22)				
51 kHz to 102 kHz		8	-	-	dB
102 kHz to 2.048 MHz		14	-	-	dB
2.048 MHz to 3.072 MHz		10	-	-	dB
Transmitter Short Circuit Current	(Notes 12, 23)	-	-	50	mA RMS

Notes:
16. Using a 0.47 µF capacitor in series with the primary of a transformer recommended in the Applications Section.
17. Amplitude measured at the transformer (CS61535A-1:1 or 1:1.26) output across a 75 Ω load for line length setting LEN2/1/0 = 0/0/0.
18. Amplitude measured at the transformer (CS61535A-1:1.26) output across a 120 Ω load for line length setting LEN2/1/0 = 0/0/0.
19. Amplitude measured at the transformer (CS61535A-1:1.15) output across a 100 Ω load for line length setting LEN2/1/0 = 0/1/0.
20. Amplitude measured across a 100 Ω load at the DSX-1 cross-connect for line length settings LEN2/1/0 = 0/1/1, 1/0/0, 1/0/1, 1/1/0 and 1/1/1 after the length of #22 AWG ABAM equivalent cable specified in Table 3. The CS61535A requires a 1:1.15 transformer.
21. Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.
22. Return loss = 20 $\log_{10}$ ABS((z_1 +z_0)/(z_1-z_0)) where z_1 = impedance of the transmitter, and z_0 = impedance of line load. Measured with a repeating 1010 data pattern with LEN2/1/0 = 0/0/0 and a 1:1 transformer terminated with a 75Ω load, or a 1:1.26 transformer terminated with a 120Ω load.
23. Measured broadband through a 0.5 Ω resistor across the secondary of a 1:1.26 transformer during the transmission of an all ones data pattern for LEN2/1/0 = 0/0/0.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter		Min	Typ	Max	Units
Driver Performance Monitor					
MTIP/MRING Sensitivity: Differential Voltage Required for Detection		-	0.60	-	V
Receiver					
RTIP/RRING Input Impedance		-	50k	-	Ω
Sensitivity Below DSX (0dB = 2.4V)		-13.6	-	-	dB
Data Decision Threshold					
T1, DSX-1	(Note 24)	60	65	70	% of peak
T1, DSX-1	(Note 25)	53	65	77	% of peak
T1, FCC Part 68 and E1	(Note 26)	45	50	55	% of peak
Data Decision Threshold	T1	-	65	-	% of peak
	E1	-	50	-	% of peak
Allowable Consecutive Zeros before LOS		160	175	190	bits
Receiver Input Jitter Tolerance	(Note 27)				
10kHz - 100kHz		0.4	-	-	UI
2kHz		6.0	-	-	UI
10Hz and below		300	-	-	UI
Loss of Signal Threshold	(Note 28)	0.25	0.30	0.50	V

Notes:
24. For input amplitude of 1.2 V_{pk} to 4.14 V_{pk}.
25. For input amplitude of 0.5 V_{pk} to 1.2 V_{pk} and from 4.14 V_{pk} to RV+.
26. For input amplitude of 1.05 V_{pk} to 3.3 V_{pk}.
27. Jitter tolerance increases at lower frequencies. See Figure 11.
28. LOS goes high after 160 to 190 consecutive zeros are received. A zero is output on RPOS and RNEG (or RDATA) for each bit period where the input signal amplitude remains below the data decision threshold. The analog input squelch circuit operates when the input signal amplitude above ground on the RTIP and RRING pins falls within the squelch range long enough for the internal slicing threshold to decay within this range. Operation of the squelch causes zeros to be output on RPOS and RNEG as long as the input amplitude remains below 0.25V. During receive LOS, pulses greater than 0.25V in amplitude may be output on RPOS and RNEG. LOS returns low after the ones density reaches 12.5% (based upon 175 bit periods starting with a one and containing less than 100 consecutive zeros) as prescribed in ANSI T1.231-1993.

T1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 29)	f_c	-	6.176000	-	MHz
ACLKI Duty Cycle		t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency	(Note 30)	f_{aclki}	-	1.544	-	MHz
RCLK Duty Cycle	(Notes 31, 32)	t_{pwh1}/t_{pw1}	- -	78 29	- -	% %
RCLK Cycle Width	(Note 32)	t_{pw1} t_{pwh1} t_{pwl1}	320 130 100	648 190 458	980 240 850	ns ns ns
Rise Time, All Digital Outputs	(Note 33)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 33)	t_f	-	-	85	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling	(Note 34)	t_{su1}	150	274	-	ns
RDATA Valid Before RCLK Falling	(Note 35)	t_{su1}	150	274	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Note 31)	t_{su1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Falling	(Note 34)	t_{h1}	150	274	-	ns
RDATA Valid After RCLK Falling	(Note 35)	t_{h1}	150	274	-	ns
RPOS/RNEG Valid After RCLK Rising	(Note 31)	t_{h1}	150	274	-	ns
TCLK Frequency		f_{tclk}	-	1.544	-	MHz
TCLK Pulse Width	(Notes 12, 31, 34, 36, 37) (Notes 35, 36, 37)	t_{pwh2}	80 150	- -	500 500	ns ns

Notes:
29. Crystal must meet specifications described in Appendix A.
30. ACLKI provided by an external source or TCLK, but *not* RCLK.
31. Hardware Mode, or Host Mode (CLKE = 0).
32. RCLK cycle width will vary with extent by which pulses displaced by jitter. Specified under worst case jitter conditions: 0.4 UI AMI data displacement for T1 and 0.2 UI AMI data displacement for E1.
33. At max load of 1.6 mA and 50 pF.
34. Host Mode (CLKE = 1).
35. Extended Hardware Mode.
36. The maximum TCLK burst rate is 5 MHz and t_{pw2}(min) = 200 ns. The maximum gap size that can be tolerated on TCLK is 12 VI.
37. The transmitted pulse width does not depend on the TCLK duty cycle.

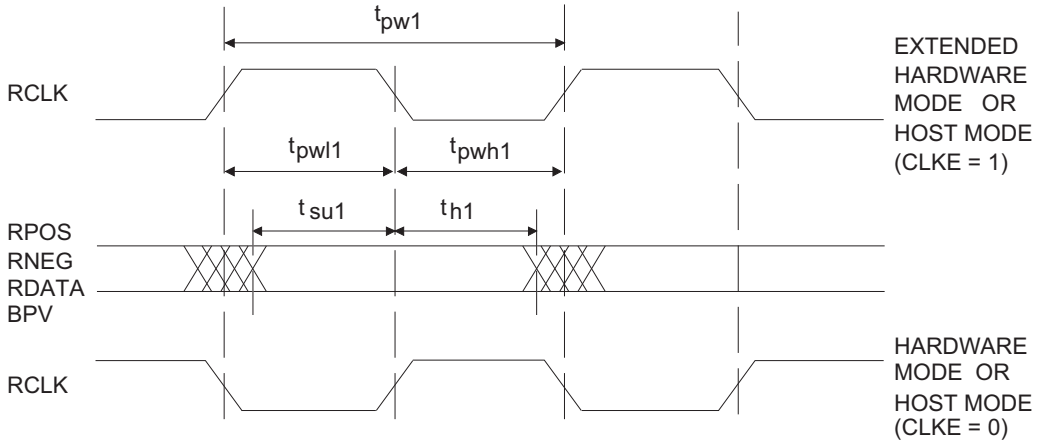


Figure 1. Recovered Clock and Data Switching Characteristics

E1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 29)	f_c	-	8.192000	-	MHz
ACLKI Duty Cycle		t_{pwh3}/t_{pw3}	40	-	60	%
ACLKI Frequency	(Note 30)	f_{aclki}	-	2.048	-	MHz
RCLK Duty Cycle	(Notes 31, 32)	t_{pwh1}/t_{pw1}	-	29	-	%
RCLK Cycle Width	(Note 32)	t_{pw1} t_{pwh1} t_{pwl1}	310 90 120	488 140 348	670 190 500	ns ns ns
RCLK Cycle Width	(Note 32)	t_{pw1} t_{pwh1} t_{pwl1}	320 - 100	488 348 140	670 - -	ns ns ns
Rise Time, All Digital Outputs	(Note 33)	t_r	-	-	85	ns
Fall Time, All Digital Outputs	(Note 33)	t_f	-	-	85	ns
TPOS/TNEG (TDATA) to TCLK Falling Setup Time		t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG (TDATA) Hold Time		t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Falling	(Note 34)	t_{su1}	100	194	-	ns
RDATA Valid Before RCLK Falling	(Note 35)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid Before RCLK Rising	(Note 31)	t_{su1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Falling	(Note 34)	t_{h1}	100	194	-	ns
RDATA Valid After RCLK Falling	(Note 35)	t_{h1}	100	194	-	ns
RPOS/RNEG Valid After RCLK Rising	(Note 31)	t_{h1}	100	194	-	ns
TCLK Frequency		f_{tclk}	-	2.048	-	MHz
TCLK Pulse Width	(Notes 31, 34, 36, 37) (Notes 35, 36, 37)	t_{pwh2}	80 150	- -	340 340	ns ns

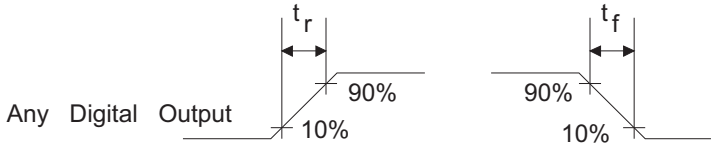


Figure 2. Signal Rise and Fall Characteristics

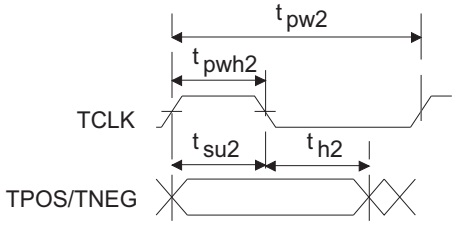


Figure 3a. Transmit Clock and Data Switching Characteristics

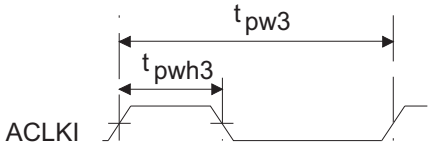


Figure 3b. Alternate External Clock Characteristics

SWITCHING CHARACTERISTICS (TA = -40° to 85°C; TV+, RV+ = ±5%;
Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
SDI to SCLK Setup Time		t_{dc}	50	-	-	ns
SCLK to SDI Hold Time		t_{cdh}	50	-	-	ns
SCLK Low Time		t_{cl}	240	-	-	ns
SCLK High Time		t_{ch}	240	-	-	ns
SCLK Rise and Fall Time		t_r, t_f	-	-	50	ns
CS to SCLK Setup Time		t_{cc}	50	-	-	ns
SCLK to CS Hold Time	(Note 38)	t_{cch}	50	-	-	ns
CS Inactive Time		t_{cwh}	250	-	-	ns
SCLK to SDO Valid	(Note 39)	t_{cdv}	-	-	200	ns
CS to SDO High Z		t_{cdz}	-	100	-	ns
Input Valid To PCS Falling Setup Time		t_{su4}	50	-	-	ns
PCS Rising to Input Invalid Hold Time		t_{h4}	50	-	-	ns
PCS Active Low Time		t_{pcsl}	250	-	-	ns

Notes: 38. For CLKE = 0, $\overline{CS}$ must remain low at least 50 ns after the 16th falling edge of SCLK.
39. Output load capacitance = 50pF.

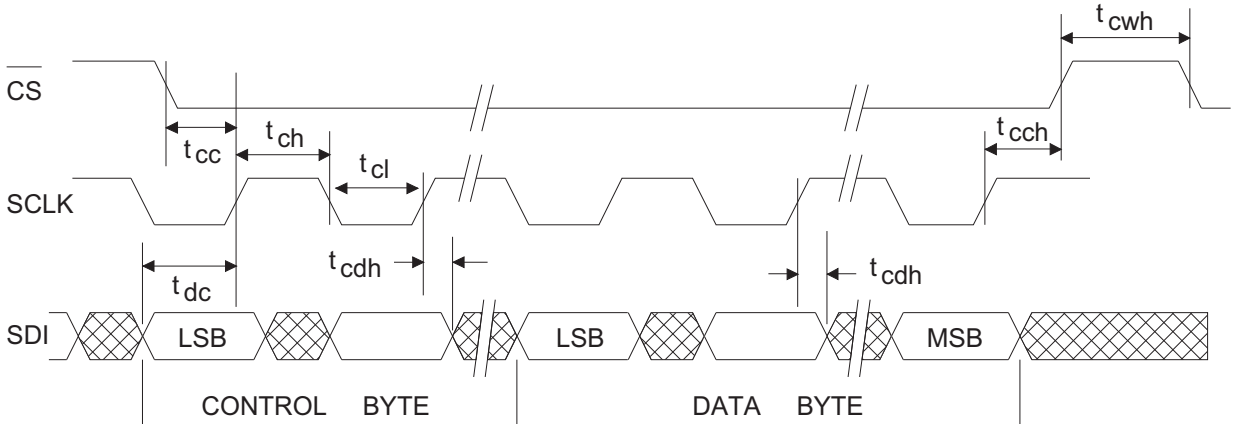


Figure 4. Serial Port Write Timing Diagram

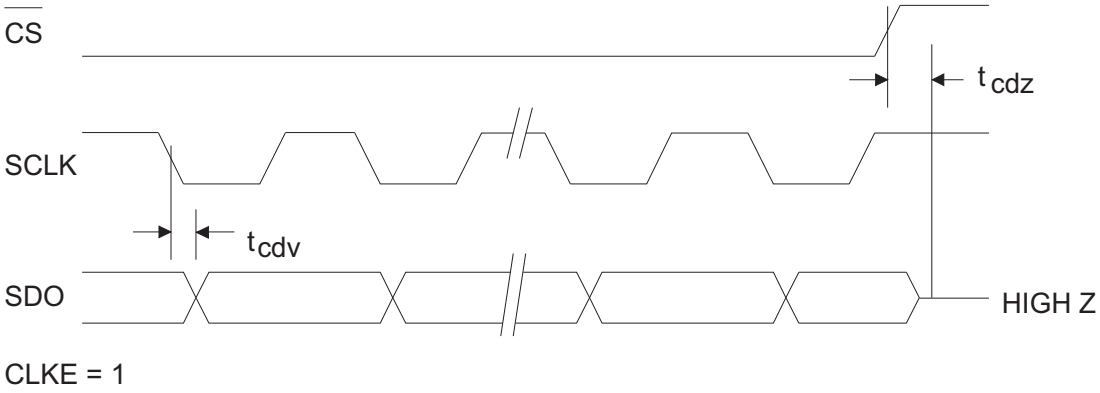


Figure 5. Serial Port Read Timing Diagram

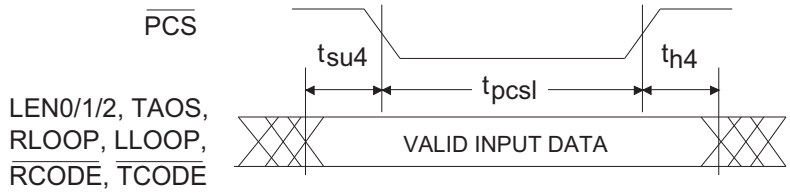


Figure 6. Extended Hardware Mode Parallel Chip Select Timing Diagram

THEORY OF OPERATION

Enhancements in CS61535A

The CS61535A provides higher performance and more features than the CS61535 including:

- 50% lower power consumption,
- Internally matched transmitter output impedance for improved signal quality,
- Optional AMI, B8ZS, HDB3 encoder/decoder or external line coding support,
- Receiver AIS (unframed all ones) detection,
- ANSI T1.231-1993 compliant receiver Loss of Signal (LOS) handling,
- Transmitter TTIP and TRING outputs are forced low when TCLK is static,
- The Driver Performance Monitor operates over a wider range of input signal levels.
- Elimination of the requirement that a reference clock be input on the ACLKI pin.

Existing designs using the CS61535 can be converted to the higher performance, pin-compatible CS61535A if the transmit transformer is replaced by a pin-compatible transformer with a new turns ratio and the 4.4 Ω resistor used in E1 75 Ω applications is shorted.

Introduction to Operating Modes

The CS61535A supports three operating modes which are selected by the level of the MODE pin as shown in Tables 1 and 2, Figure 7, and Figures A1-A3 of the Applications section.

The CS61535A modes are Hardware Mode, Extended Hardware Mode, and Host Mode. In Hardware and Extended Hardware Modes, discrete pins are used to configure and monitor the device. The Extended Hardware Mode provides a parallel chip select input which latches the control inputs allowing individual ICs to be configured using a common set of control lines. In the Host Mode, an external processor monitors and configures the device through a serial interface. There are thirteen multi-function pins whose functionality is determined by the operating mode (see Table 2).

Transmitter

The transmitter takes data from a T1 (or E1) terminal, attenuates jitter, and produces pulses of appropriate shape. The transmit clock, TCLK, and transmit data, TPOS & TNEG or TDATA, are supplied synchronously. Data is sampled on the falling edge of the input clock, TCLK.

Either T1 (DSX-1 or Network Interface) or E1 G.703 pulse shapes may be selected. Pulse shaping and signal level are determined by "line length select" inputs as shown in Table 3. The

	MODE		
	HARDWARE	EXTENDED HARDWARE	HOST
MODE-PIN INPUT LEVEL	<0.2V	FLOAT, or 2.5V	>(RV+) - 0.2V
CONTROL METHOD	INDIVIDUAL CONTROL LINES	INDIVIDUAL CONTROL LINES & PARALLEL CHIP SELECT	SERIAL µ-PROCESSOR PORT
LINE CODE ENCODER & DECODER	NONE	AMI, B8ZS, HDB3	NONE
AIS DETECTION	NO	YES	NO
DRIVER PERFORMANCE MONITOR	YES	NO	YES

Table 1. Differences in Operating Modes

		MODE		
FUNCTION	PIN	HARDWARE	EXTENDED HARDWARE	HOST
TRANSMITTER	3	TPOS	TDATA	TPOS
	4	TNEG	$\overline{\text{TCODE}}$	TNEG
RECEIVER/DPM	6	RNEG	BPV	RNEG
	7	RPOS	RDATA	RPOS
	11	DPM	AIS	DPM
	17	MTIP	$\overline{\text{RCODE}}$	MTIP
	18	MRING	-	MRING
CONTROL	18	-	$\overline{\text{PCS}}$	-
	23	LEN0	LEN0	$\overline{\text{INT}}$
	24	LEN1	LEN1	SDI
	25	LEN2	LEN2	SDO
	26	RLOOP	RLOOP	$\overline{\text{CS}}$
	27	LLOOP	LLOOP	SCLK
	28	TAOS	TAOS	CLKE

Table 2. Pin Definitions

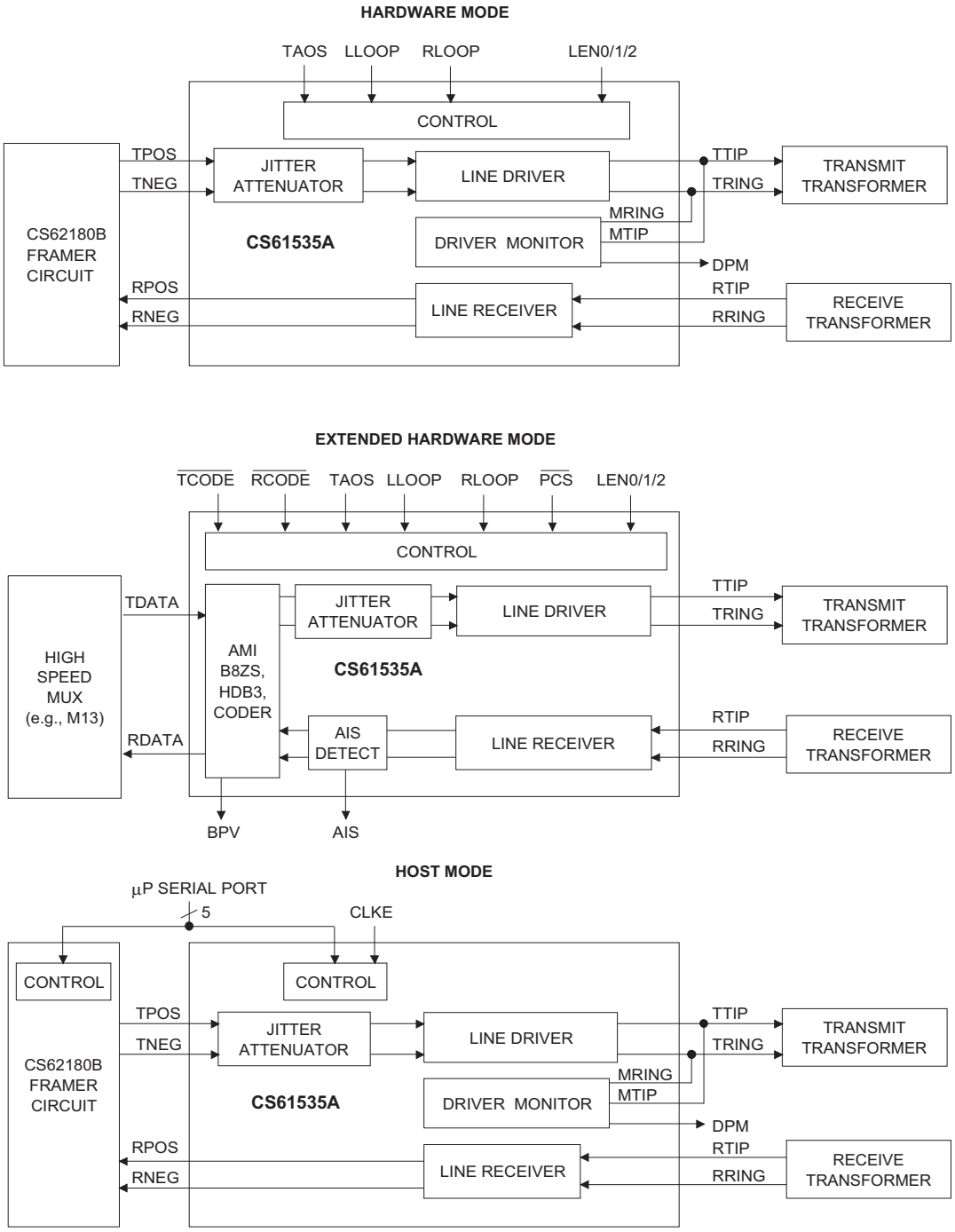


Figure 7. Overview of Operating Modes

LEN2	LEN1	LEN0	OPTION SELECTED	APPLICATION
0	1	1	0-133 FEET	DSX-1 ABAM (AT&T 600B or 600C)
1	0	0	133-266 FEET	
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	
0	0	1	AT&T CB113 (CS61535A only)	REPEATER
0	0	0	CCITT G.703	2.048 MHz E1
0	1	0	FCC Part 68, Option A	CSU NETWORK INTERFACE
0	1	1	ANSI T1.403	

Table 3. Line Length Selection

CS61535A line driver is designed to drive a 75 Ω equivalent load.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the transmitter to the DSX-1 cross connect) are selectable. The five partition arrangement meets ANSI T1.102-1993 requirements when using ABAM cable. A typical output pulse is shown in Figure 8. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

For T1 Network Interface applications, additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS61535A automatically adjusts the pulse width based upon the "line length" selection made.

The E1 G.703 pulse shape is supported with line length selection LEN2/1/0=0/0/0. The pulse width will meet the G.703 pulse shape template shown in Figure 9, and specified in Table 4.

For E1 applications, the CS61535A driver provides 14 dB of return loss during the transmission of both marks and spaces. This improves signal quality by minimizing reflections off the transmitter. Similar levels of return loss are provided for T1 applications.

The CS61535A transmitter will detect a failed TCLK, and will force the TTIP and TRING outputs low.

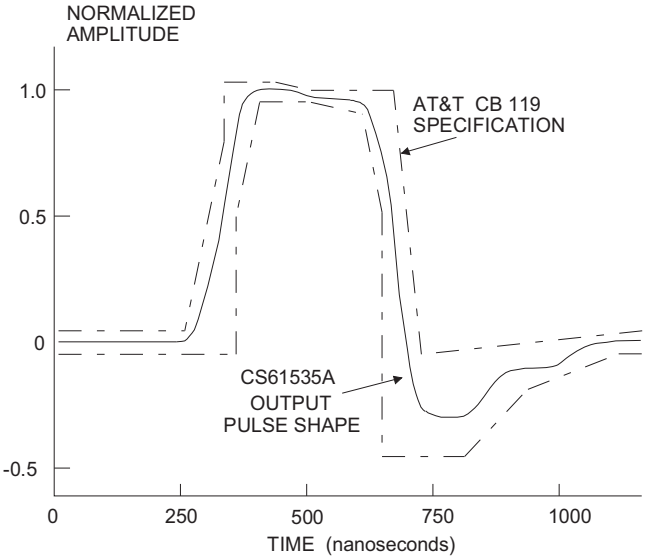


Figure 8. Typical Pulse Shape at DSX-1 Cross Connect

	For coaxial cable, 75Ω load and transformer specified in Application Section.	For shielded twisted pair, 120Ω load and transformer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ±0.237 V	0 ±0.30 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05*	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05*	

* When configured with a 0.47 µF nonpolarized capacitor in series with the TX transformer primary as shown in Figures A1, A2 and A3.

Table 4. CCITT G.703 Specifications

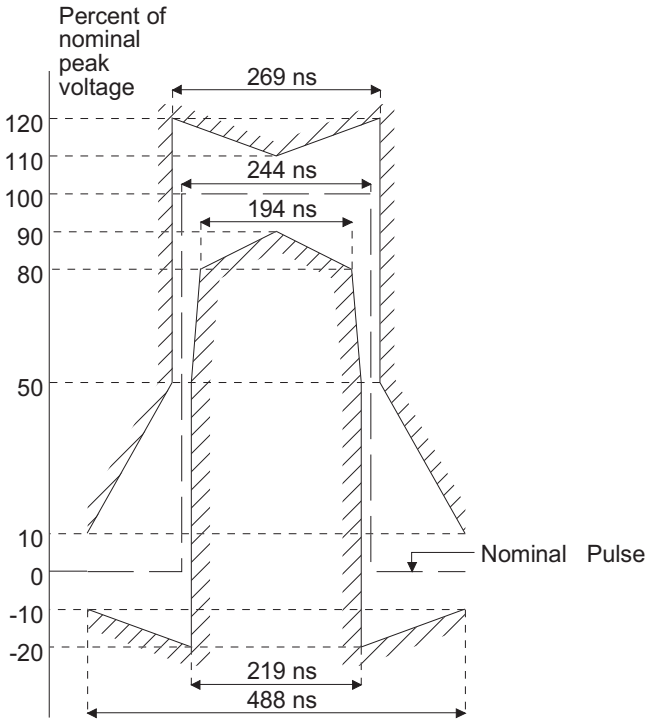


Figure 9 . Mask of the Pulse at the 2048 kbps Interface

When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter stabilizes within 22 bit periods. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Jitter Attenuator

The jitter attenuator is designed to reduce wander and jitter in the transmit clock signal. It consists of a 32 bit FIFO, a crystal oscillator, a set of load capacitors for the crystal, and control logic. The jitter attenuator exceeds the jitter attenuation requirements of Publications 43802 and REC. G.742. A typical jitter attenuation curve is shown in Figure 10.

The jitter attenuator works in the following manner. Data on TPOS and TNEG (or TDATA) are written into the jitter attenuator's FIFO by TCLK. The rate at which data is read out of the FIFO and transmitted is determined by the oscillator. Logic circuits adjust the capacitive loading on the crystal to set its oscillation frequency to the average of the TCLK frequency. Signal jitter is absorbed in the FIFO.

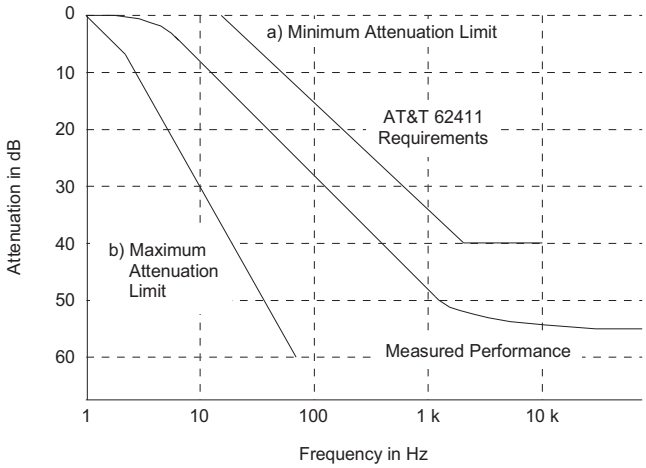


Figure 10. Typical Jitter Attenuation Curve

Jitter Tolerance of Jitter Attenuator

The FIFO in the jitter attenuator is designed to neither overflow nor underflow. If the jitter amplitude becomes very large, the read and write pointers may get very close together. Should the pointers attempt to cross, the oscillator's divide by four circuit adjusts by performing a divide by 3 1/2 or divide by 4 1/2 to prevent the overflow or underflow. When a divide by 3 1/2 or 4 1/2 occurs, the data bit will be driven onto the line either an eighth bit period early or an eighth bit period late.

When the TCLK frequency is close to the center frequency of the crystal oscillator, the high frequency jitter tolerance is 23 UI before the divide by 3 1/2 or 4 1/2 circuitry is activated. As the center frequency of the oscillator and the TCLK frequency deviate from one another, the jitter tolerance is reduced. As this frequency deviation becomes large, the maximum jitter tolerance at high frequencies is reduced to 12 UI before the underflow/overflow circuitry is activated. In application, it is unlikely that the oscillator center frequency will be precisely aligned with the

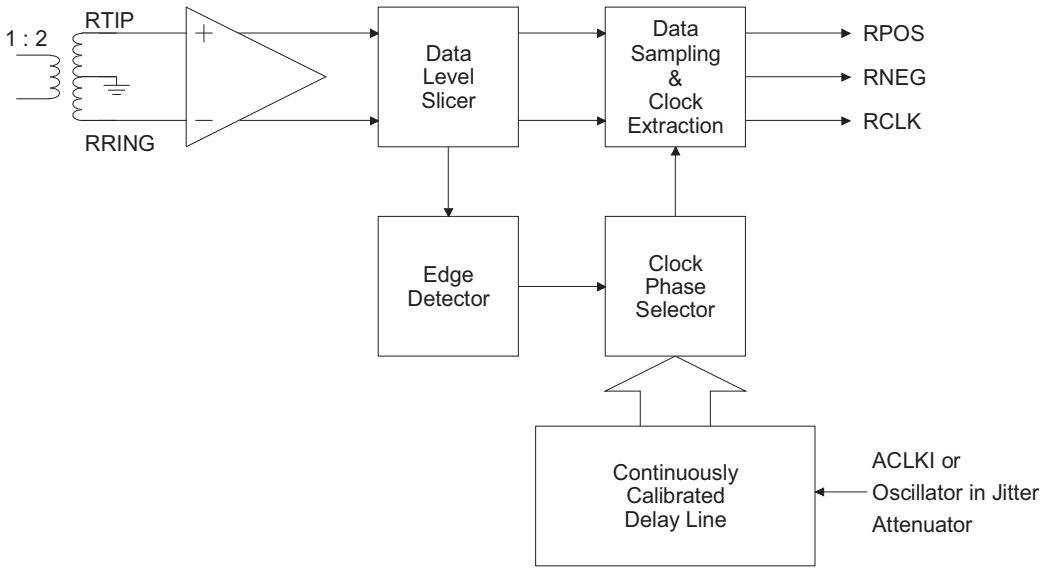


Figure 11. Receiver Block Diagram

TCLK frequency due to allowable TCLK tolerance, part to part variations, crystal to crystal variations, and crystal temperature drift. The oscillator tends to track low frequency jitter so jitter tolerance increases as jitter frequency decreases.

The crystal frequency must be 4 times the nominal signal frequency: 6.176 MHz for 1.544 MHz operation; 8.192 MHz for 2.048 MHz applications. Internal capacitors load the crystal, controlling the oscillation frequency. The crystal must be designed so that over operating temperature, the oscillator frequency range exceeds the system frequency tolerance. To obtain optimum performance, the crystal used must meet the specifications in Appendix A.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of ACLKI. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG (or TDATA) inputs are ignored. A TAOS request will be ignored if remote loopback is in effect. ACLKI jitter will be attenuated. TAOS is not available on the CS61535A when ACLKI is grounded.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center-tapped on the IC side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, 62411 amended, TR-TSY-000170, and CCITT REC. G.823.

A block diagram of the receiver is shown in Figure 11. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for E1, 65% of peak for T1; with the slicing level selected by LEN2/1/0).

The receiver uses an edge detector and a continuously calibrated delay line to generate the recovered clock. The delay line divides its reference clock, ACLKI or the jitter attenuator's oscillator, into 13 equal divisions or phases. Continuous calibration assures timing accuracy, even if temperature or power supply voltage fluctuate.

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The output from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data. The jitter tolerance of the receiver exceeds that shown in Figure 12.

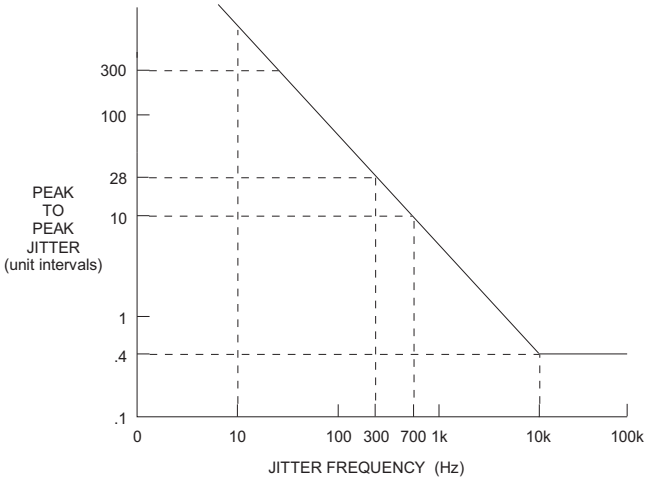


Figure 12. Input Jitter Tolerance of Receiver

The CS61535A outputs a clock immediately upon power-up. The clock recovery circuit is calibrated, and the device will lock onto the AMI data input immediately. If loss of signal occurs, the RCLK frequency will equal the ACLKI frequency.

In the Hardware Mode, data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock. In the Extended Hardware Mode, data at RDATA is stable and may be sampled on the falling edge of the recovered clock. In the Host Mode, CLKE determines the clock polarity for which output data is stable and valid as shown in Table 5.

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW (<0.2V)	X	RPOS RNEG	RCLK RCLK	Rising Rising
HIGH (>(V+) - 0.2V)	LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH (>(V+) - 0.2V)	HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising
MIDDLE (2.5V)	X	RDATA	RCLK	Falling

X = Don't care

Table 5. Data Output/Clock Relationship

Jitter and Recovered Clock

The CS61535A are designed for error free clock and data recovery from an AMI encoded data stream in the presence of more than 0.4 unit intervals of jitter at high frequency. The clock recovery circuit is also tolerant of long strings of zeros. The edge of an incoming data bit causes the circuitry to choose a phase from the delay line which most closely corresponds with the arrival time of the data edge, and that clock phase triggers a pulse which is typically 140 ns in duration. This phase of the delay line will continue to be selected until a data bit arrives which is closer to another of the 13 phases, causing a new phase to be selected. The largest jump allowed along the delay line is six phases.

When an input signal is jitter free, the phase selection will occasionally jump between two adjacent phases resulting in RCLK jitter with an amplitude of 1/13 UIpp. These single phase jumps are due to differences in frequency of the incoming data and the calibration clock input to ACLKI. For T1 operation of the CS61535A, the instantaneous period can be 14/13 * 648 ns = 698 ns (1,662,769 Hz) or 12/13 * 648 ns = 598 ns (1,425,231 Hz) when adjacent clock phases are chosen. As long as the same phase is chosen, the

period will be 648 ns. Similar calculations hold for the E1 rate.

The clock recovery circuit is designed to accept at least 0.4 UI of jitter at the receiver. Since the data stream contains information only when ones are transmitted, a clock/data recovery circuit must assume a zero when no signal is measured during a bit period. Likewise, when zeros are received, no information is present to update the clock recovery circuit regarding the trend of a signal which is jittered. The result is that two ones that are separated by a string of zeros can exhibit maximum deviation in pulse arrival time. For example, one half of a period of jitter at 100 kHz occurs in 5 µs, which is 7.7 T1 bit periods. If the jitter amplitude is 0.4 UI, then a one preceded by seven zeros can have maximum displacement in arrival time, i.e. either 0.4 UI too early or 0.4 UI too late. For the CS61535A, the data recovery circuit correctly assigns a received bit to its proper clock period if it is displaced by less than 6/13 of a bit period from its optimal location. Theoretically, this would give a jitter tolerance of 0.46 UI. The actual jitter tolerance of the CS61535A is only slightly less than the ideal.

In the event of a maximum jitter hit, the RCLK clock period immediately adjusts to align itself with the incoming data and prepare to accurately place the next one, whether it arrives one period later, or after another string of zeros and is displaced by jitter. For a maximum early jitter hit, RCLK will have a period of 7/13 * 648 ns = 349 ns (2,865,961 Hz). For a maximum late jitter hit, RCLK will have a period of 19/13 * 648 ns = 947 ns (1,055,880 Hz).

Loss of Signal

Receiver loss of signal is indicated upon receiving 175 consecutive zeros. A digital counter counts received zeros based on RCLK cycles. A zero input is determined either when zeros are received, or when the received signal amplitude drops below a 0.3 V peak threshold.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. If the serial interface is used, the LOS bit will be set and an interrupt is issued on INT. LOS will go low (and flag the INT pin again if serial I/O is used) when a valid signal is detected. Note that in the Host Mode, LOS is simultaneously available from both the register and pin 12.

In a loss of signal state, the RCLK frequency will be equal to the ACLKI frequency since ACLKI is being used to calibrate the clock recovery circuit. Received data is output on RPOS and RNEG (or RDATA) regardless of LOS status. The LOS returns to logic zero when the ones density reaches 12.5% (based upon 175 bit periods staring with a one and containing less than 100 consecutive zeros) as prescribed in ANSI T1.231-1993. A power-up or manual reset will also set LOS high.

Local Loopback

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG (or TDATA) and outputs it at RCLK, RPOS and RNEG (or RDATA). Local loopback is selected by taking pin 27 high, or LLOOP may be selected using the serial interface. The data on the transmitter inputs is transmitted on the line unless TAOS is selected to cause the transmission of an all ones signal instead. Receiver inputs are ignored when local loopback is in effect. The jitter attenuator is not included in the local loopback data path. Selection of local loopback overrides the chip's loss of signal response.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the jitter attenuator and back out on the line via TTIP and TRING. The recovered incoming signals are also sent to RCLK, RPOS and RNEG (or

RDATA). Remote loopback is selected by taking pin 26 high, or RLOOP may be selected using the serial interface. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

In the CS61535A Extended Hardware Mode, remote loopback occurs before the line code encoder/decoder, insuring that the transmitted signal matches the received signal, even in the presence of received bipolar violations. The recovered data will also be decoded and output on RDATA if $\overline{\text{RCODE}}$ is low.

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the Hardware and Host Modes of the CS61535A are able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure. In the Host Mode, DPM is available from both the register and pin 11.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if the absolute difference between MTIP and MRING does not transition above or below a threshold level within a time-out period.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring device, rather than having it monitor its own performance.

Line Code Encoder/Decoder

In Extended Hardware Mode, three line codes are available: AMI, B8ZS and HDB3. The input to the encoder is TDATA. The outputs from the decoder are RDATA and BPV (Bipolar Violation Strobe). The encoder and decoder are selected using pins LEN2, LEN1, LEN0, $\overline{\text{TCODE}}$ and $\overline{\text{RCODE}}$ as shown in Table 6.

		LEN 2/1/0	
		000	010-111
$\overline{\text{TCODE}}$ (Transmit Encoder Selection)	LOW	HDB3 Encoder	B8ZS Encoder
	HIGH	AMI Encoder	
$\overline{\text{RCODE}}$ (Receiver Decoder Selection)	LOW	HDB3 Decoder	B8ZS Decoder
	HIGH	AMI Decoder	

Table 6. Selection of Encoder/Decoder

Alarm Indication Signal

In Extended Hardware Mode, the receiver sets the output pin AIS high when less than 9 zeros are detected out of 8192 bit periods. AIS returns low when 9 or more zeros are detected out of 8192 bits.

Parallel Chip Select

In Extended Hardware Mode, $\overline{\text{PCS}}$ can be used to gate the digital control inputs: $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS. Inputs are accepted on these pins only when $\overline{\text{PCS}}$ is low. Changes in inputs will immediately change the operating state of the device. Therefore, when cycling $\overline{\text{PCS}}$ to update the operating state, the digital control inputs should be stable for the entire $\overline{\text{PCS}}$ low period. The control inputs are ignored when $\overline{\text{PCS}}$ is high.

Power On Reset / Reset

Upon power-up, the CS61535A is held in a static state until the supply crosses a threshold of ap-

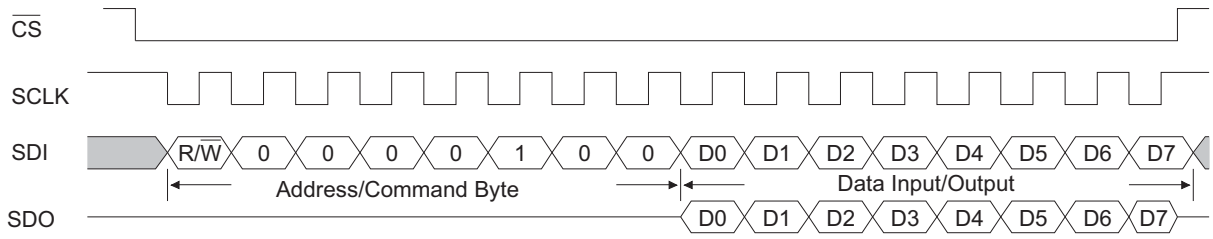


Figure 13. Input/Output Timing

proximately three Volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by ACLKI (or by the crystal oscillator if ACLKI is not present). The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function foregoes any requirement to reset the line interface when in operation. However, a reset function is available which will clear all registers.

In the Hardware and Extended Hardware modes, a reset request is made by simultaneously setting both RLOOP and LLOOP high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP and LLOOP). In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. In either mode, a reset will set all registers to 0 and set LOS high.

Serial Interface

In the Host Mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One eight-bit register can be written to via the SDI pin or read from the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). SCLK may be either high or low when $\overline{CS}$ initially goes low. Address and input data bits are clocked in on the rising edge of SCLK. Data on SDO is valid and stable on the falling edge of SCLK when CLKE is low, and on the rising edge of SCLK when CLKE is high. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no sooner than 50 ns after the rising edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{CS}$ may go high any time to terminate the output.

Figure 13 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 0, data output from the serial port, SDO, is valid on the falling edge of SCLK. For CLKE = 1, data bit D7 is held to the falling edge of the 16th clock cycle; for CLKE = 0, data bit D7 is held to the rising edge of the 17th clock cycle. SDO goes to a high

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADD0	LSB of address, Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0

Table 7. Address/Command Byte

impedance state either after bit D7 is output or at the end of the hold period of data bit D7.

An address/command byte, shown in Table 7, precedes a data register. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The CS61535A responds to address 16 (0010000). The last bit is ignored.

The data register, shown in Table 8, can be written to the serial port. Data is input on the eight clock cycles immediately following the address/command byte. Bits 0 and 1 are used to clear an interrupt issued from the $\overline{INT}$ pin, which occurs in response to a loss of signal or a problem with the output driver. If bits 0 or 1 are true, the corresponding interrupt is suppressed. So if a loss of signal interrupt is cleared by writing a 1 to bit 0, the interrupt will be reenabled by writing a 0 to bit 0. This holds for DPM as well.

LSB: first bit in	0	clr LOS	Clear Loss of Signal
	1	clr DPM	Clear Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Lenght Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB: last bit in	7	TAOS	Transmit All Ones Select

Table 8. Input Data Register

Writing a "1" to either "Clear LOS" or "Clear DPM" over the serial interface has three effects:

1) the current interrupt on the serial interface will be cleared. (Note that simply reading the register bits will not clear the interrupt),

2) output data bits 5, 6 and 7 will be reset as appropriate,

3) future interrupts for the corresponding LOS or DPM will be prevented from occuring).

LSB: first bit in	0	LOS	Loss of Signal
	1	DPM	Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Lenght Select

Table 9. Output Data Bits 0 - 4

Bits 5	6	7	Status
0	0	0	Reset has occurred or no program input.
0	0	1	TAOS in effect.
0	1	0	LLOOP in effect.
0	1	1	TAOS/LLOOP in effect.
1	0	0	RLOOP in effect
1	0	1	DPM changed state since last "clear DPM" occured.
1	1	0	LOS changed state since last "clear LOS" occured.
1	1	1	LOS and DPM have changed state since last "clear LOS" and "clear DPM".

Table 10. Coding for Serial Output Bits 5, 6, 7

Writing a "0" to either "Clear LOS" or "Clear DPM" enables the corresponding interrupt for LOS or DPM.

Output data from the serial interface is presented as shown in Tables 9 and 10. Bits 2, 3 and 4 can be read to verify line length selection. Bits 5, 6 and 7 must be decoded. Codes 101, 110 and 111 (bits 5, 6 and 7) indicate LOS and DPM state changes. Writing a "1" to the "Clear LOS" and/or "Clear DPM" bits in the register also resets status bits 5, 6, and 7.

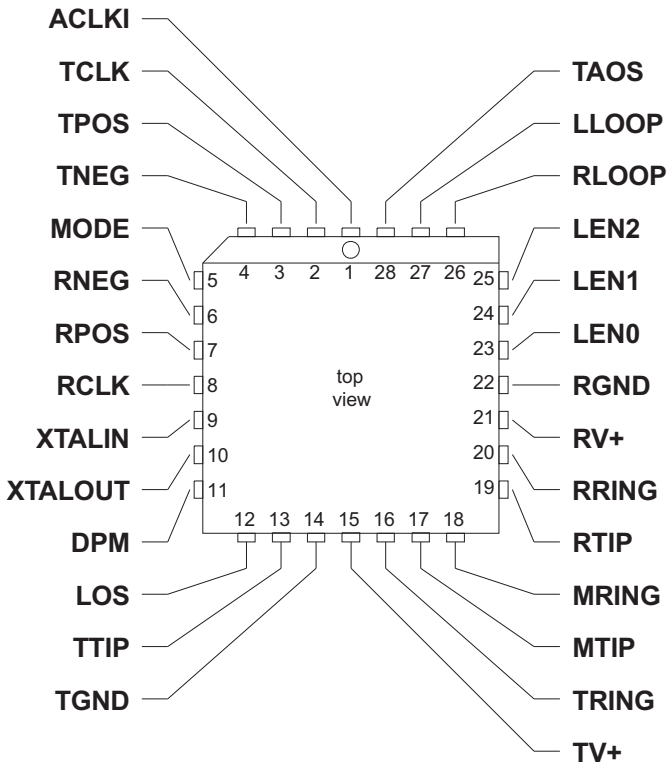
SDO goes to a high impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bidirectional I/O port.

Power Supply

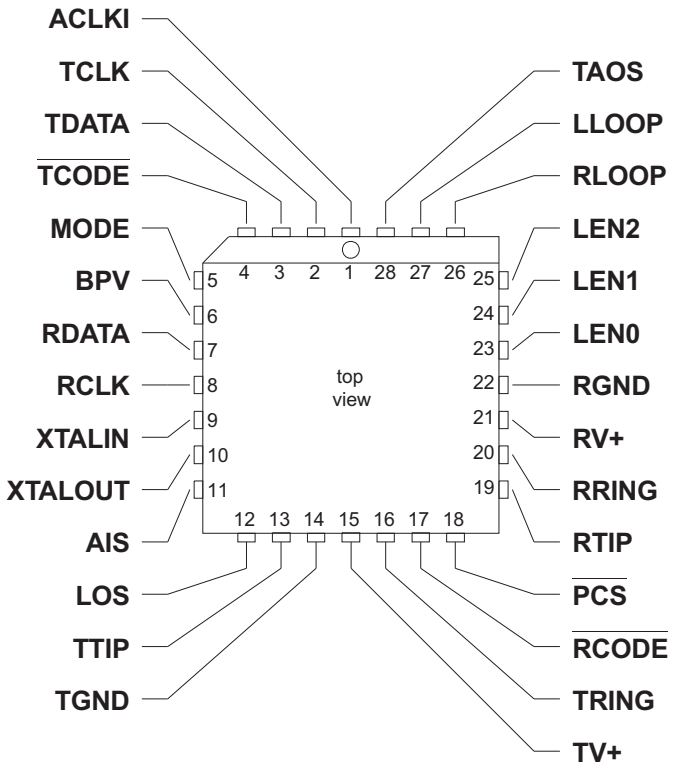
The device operates from a single +5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. These pins should be connected externally near the device and decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 1.0 µF capacitor should be connected between TV+ and TGND, and a 0.1 µF capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 µF tantalum capacitor should be added close to the RV+/RGND supply. Wire wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

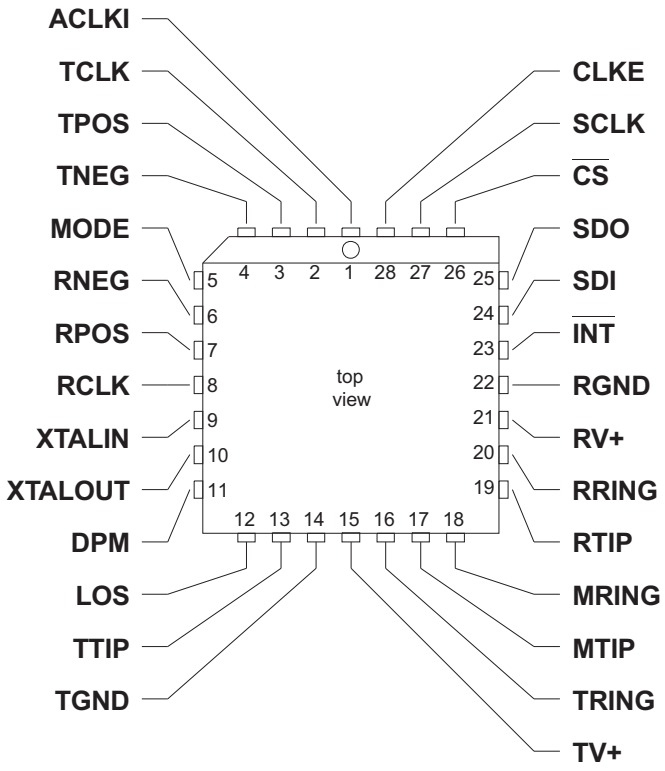
Hardware Mode Pinout



Extended Hardware Mode Pinout



Host Mode Pinout



Power Supplies

RGND - Ground, Pin 22.
Power supply ground for all subcircuits except the transmit driver; typically 0 Volts.

RV+ - Power Supply, Pin 21.
Power supply for all subcircuits except the transmit driver; typically +5 Volts.

TGND - Ground, Transmit Driver, Pin 14.
Power supply ground for the transmit driver; typically 0 Volts.

TV+ - Power Supply, Transmit Driver, Pin 15.
Power supply for the transmit driver; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3 V.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.
A 6.176 MHz (or 8.192 MHz) crystal should be connected across these pins. If a 1.544 MHz (or 2.048 MHz) clock is provided on ACLKI (pin 1), the jitter attenuator may be disabled by tying XTALIN, Pin 9 to RV+ through a 1 kΩ resistor, and floating XTALOUT, Pin 10.
Overdriving the oscillator with an external clock is not supported. See Appendix A for crystal specifications.

Control

ACLKI - Alternate External Clock Input, Pin 1.
The CS61535A does not require a clock signal to be input on ACLKI when a crystal is connected between pins 9 and 10. If a clock is not provided on ACLKI, this input must be grounded. If ACLKI is grounded, the oscillator in the jitter attenuator is used to calibrate the clock recovery circuit and TAOS is not available.

CLKE - Clock Edge, Pin 28. (Host Mode)
Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

$\overline{\text{CS}}$ - Chip Select, Pin 26. (Host Mode)
This pin must transition from high to low to read or write the serial port.

$\overline{\text{INT}}$ - Receive Alarm Interrupt, Pin 23. (Host Mode)
Goes low when LOS or DPM change state to flag the host processor. $\overline{\text{INT}}$ is cleared by writing "Clear LOS" or "Clear DPM" to the register. $\overline{\text{INT}}$ is an open drain output and should be tied to the power supply through a resistor.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25. (Hardware and Extended Hardware Modes)

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 3 for information on line length selection. Also controls the receiver slicing level and the line code in Extended Hardware Mode.

LLOOP - Local Loopback, Pin 27. (Hardware and Extended Hardware Modes)

Setting LLOOP to a logic 1 routes the transmit clock and data through to the receive clock and data pins. TPOS/TNEG (or TDATA) are still transmitted unless overridden by a TAOS request. Inputs on RTIP and RRING are ignored.

MODE - Mode Select, Pin 5.

Driving the MODE pin high puts the CS61535A line interface in the Host Mode. In the host mode, a serial control port is used to control the CS61535A line interface and determine its status. Grounding the MODE pin puts the CS61535A line interface in the Hardware Mode, where configuration and status are controlled by discrete pins. Floating the MODE pin or driving it to +2.5 V puts the CS61535A in Extended Hardware Mode, where configuration and status are controlled by discrete pins. When floating MODE, there should be no external load on the pin. MODE defines the status of 13 pins (see Table 2).

$\overline{\text{PCS}}$ - Parallel Chip Select, Pin 18. (Extended Hardware Mode)

Setting $\overline{\text{PCS}}$ high causes the CS61535A line interface to ignore the $\overline{\text{TCODE}}$, $\overline{\text{RCODE}}$, LEN0, LEN1, LEN2, RLOOP, LLOOP and TAOS inputs.

$\overline{\text{RCODE}}$ - Receiver Decoder Select, Pin 17. (Extended Hardware Mode)

Setting $\overline{\text{RCODE}}$ low enables B8ZS or HDB3 zero substitution in the receiver decoder. Setting $\overline{\text{RCODE}}$ high enables the AMI receiver decoder (see Table 8).

RLOOP - Remote Loopback, Pin 26. (Hardware and Extended Hardware Modes)

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator (if active) and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG (or RDATA). Any TAOS request is ignored.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

SCLK - Serial Clock, Pin 27. (Host Mode)

Clock used to read or write the serial port registers. SCLK can be either high or low when the line interface is selected using the $\overline{\text{CS}}$ pin.

SDI - Serial Data Input, Pin 24. (Host Mode)

Data for the on-chip register. Sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25. (Host Mode)

Status and control information from the on-chip register. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or after bit D7 is output.

TAOS - Transmit All Ones Select, Pin 28. (Hardware and Extended Hardware Modes)

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by ACLKI.

$\overline{\text{TCODE}}$ - Transmitter Encoder Select, Pin 4. (Extended Hardware Mode)

Setting $\overline{\text{TCODE}}$ low enables B8ZS or HDB3 zero substitution in the transmitter encoder. Setting $\overline{\text{TCODE}}$ high enables the AMI transmitter encoder .

Data

RCLK - Recovered Clock, Pin 8.

The receiver recovered clock is output on this pin.

RDATA - Receive Data - Pin 7. (Extended Hardware Mode)

Data recovered from the RTIP and RRING inputs is output at this pin, after being decoded by the line code decoder. RDATA is NRZ. RDATA is stable and valid on the falling edge of RCLK.

RPOS, RNEG - Receive Positive Data, Receive Negative Data, Pins 6 and 7. (Hardware and Host Modes)

The receiver recovered NRZ digital data is output on these pins. In the Hardware Mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the Host Mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 5. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RCLK and RPOS/RNEG or RDATA.

TCLK - Transmit Clock, Pin 2.

The1.544 MHz (or 2.048 MHz) transmit clock is input on this pin. TPOS/TNEG or TDATA are sampled on the falling edge of TCLK.

TDATA - Transmit Data, Pin 3. (Extended Hardware Mode)

Transmitter NRZ input data which passes through the line code encoder, and is then driven on to the line through TTIP and TRING. TDATA is sampled on the falling edge of TCLK.

TPOS, TNEG - Transmit Positive Data, Transmit Negative Data, Pins 3 and 4. (Hardware and Host Modes)

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins. In the CS61535A, this output is designed to drive a 75 Ω load. A 1:1, 1:1.15 or 1:1.26 transformer is required as shown in Figure A1.

Status

AIS - Alarm Indication Signal, Pin 11. (Extended Hardware Mode)

AIS goes high when unframed all-ones condition (blue alarm) is detected, using the detection criteria of less than three zeros out of 2048 bit periods.

BPV- Bipolar Violation Strobe, Pin 6. (Extended Hardware Mode)

BPV strobes high when a bipolar violation is detected in the received signal. B8ZS (or HDB3) zero substitutions are not flagged as bipolar violations if the B8ZS (or HDB3) decoder has been enabled.

DPM - Driver Performance Monitor, Pin 11. (Hardware and Host Modes)

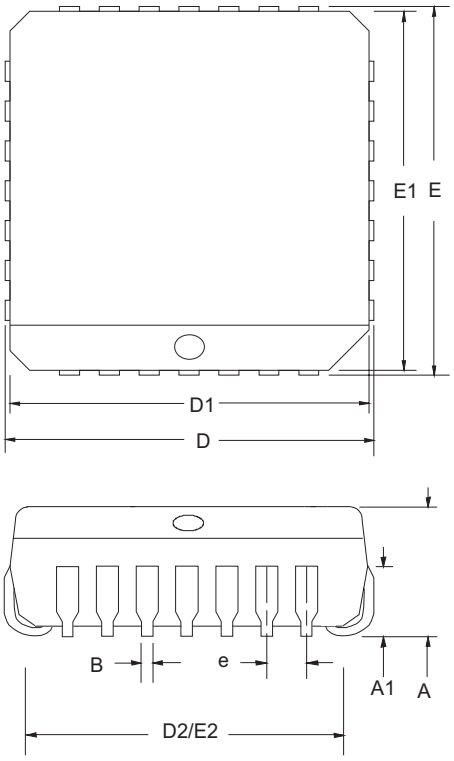
DPM goes high if no activity is detected on MTIP and MRING.

LOS - Loss of Signal, Pin 12.

LOS goes high when 175 consecutive zeros have been received. For the CS61535A, LOS returns low when the ones density reaches 12.5% (based upon 175 bit periods starting with a one and containing less than 100 consecutive zeros) as prescribed by ANSI T1.231-1993.

MTIP, MRING - Monitor Tip, Monitor Ring, Pins 17 and 18. (Hardware and Host Modes)

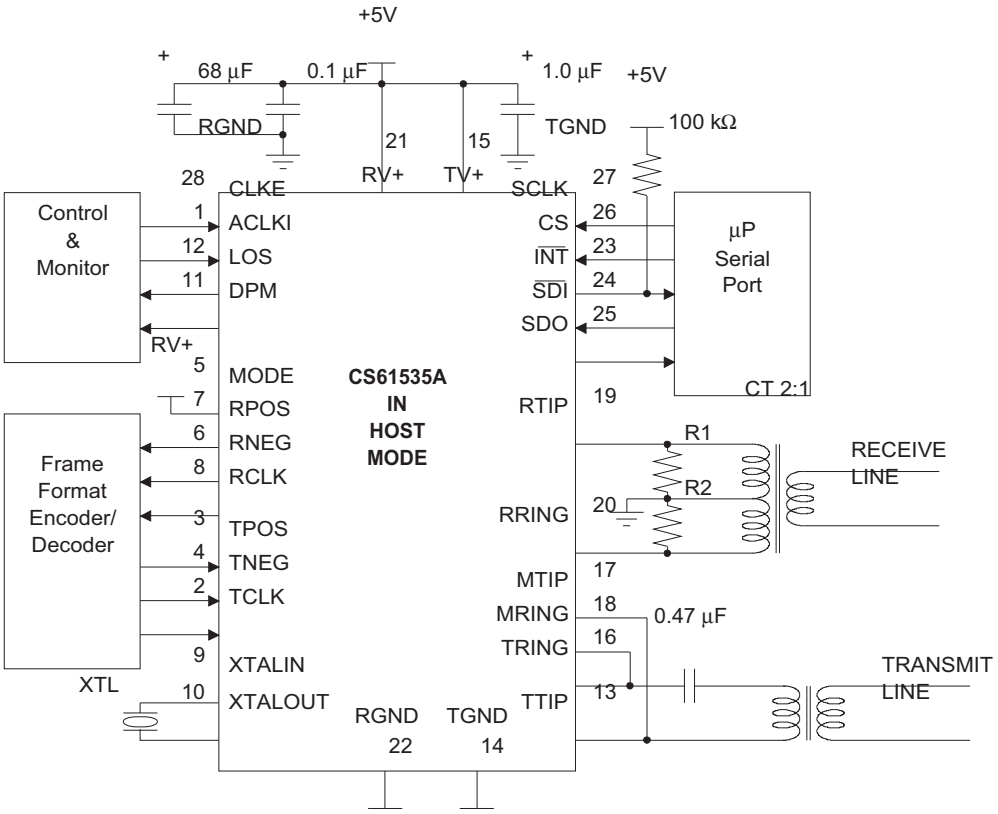
These pins are normally connected to TTIP and TRING and monitor the output of a CS61535A. If the $\overline{\text{INT}}$ pin in the host mode is used, and the monitor is not used, writing "Clear DPM" to the serial interface will prevent an interrupt from the driver performance monitor.



28-pin PLCC

DIM	28					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.20	4.45	4.57	0.165	0.175	0.180
A1	2.29	2.79	3.04	0.090	0.110	0.120
B	0.33	0.41	0.53	0.013	0.016	0.021
D/E	12.32	12.45	12.57	0.485	0.490	0.495
D1/E1	11.43	11.51	11.58	0.450	0.453	0.456
D2/E2	9.91	10.41	10.92	0.390	0.410	0.430
e	1.19	1.27	1.35	0.047	0.050	0.053

APPLICATIONS



DEVICE	FREQUENCY	CABLE	R1&2	Transmit
	MHz	Ω	Ω	Transformer
CS61535A	1.544	100	200	1:1.15
	2.048	120	240	1:1.26
	2.048	75	150	1:1

Figure A1. Host Mode Configuration

Line Interface

Figures A1-A3 show the typical configurations for interfacing the I.C. to a line through transmit and receive transformers.

The receiver transformer is center tapped and center grounded with resistors between the center tap and each leg on the I.C. side. These resistors provide the termination for the line.

Figures A1-A3 show a 0.47 µF capacitor in series with the transmit transformer primary. This capacitor is needed to prevent any buildup in the core of the transformer due to any DC imbalance that may be present at the differential outputs, TTIP and TRING. If DC saturates the transformer, a DC offset will result during the transmission of a space (zero) as the transformer tries to dump the charge and return to equilibrium. The blocking capacitor will keep DC current from flowing in the transformer.

Selecting an Oscillator Crystal

Specific crystal parameters are required for proper operation of the CS61535A. Refer to

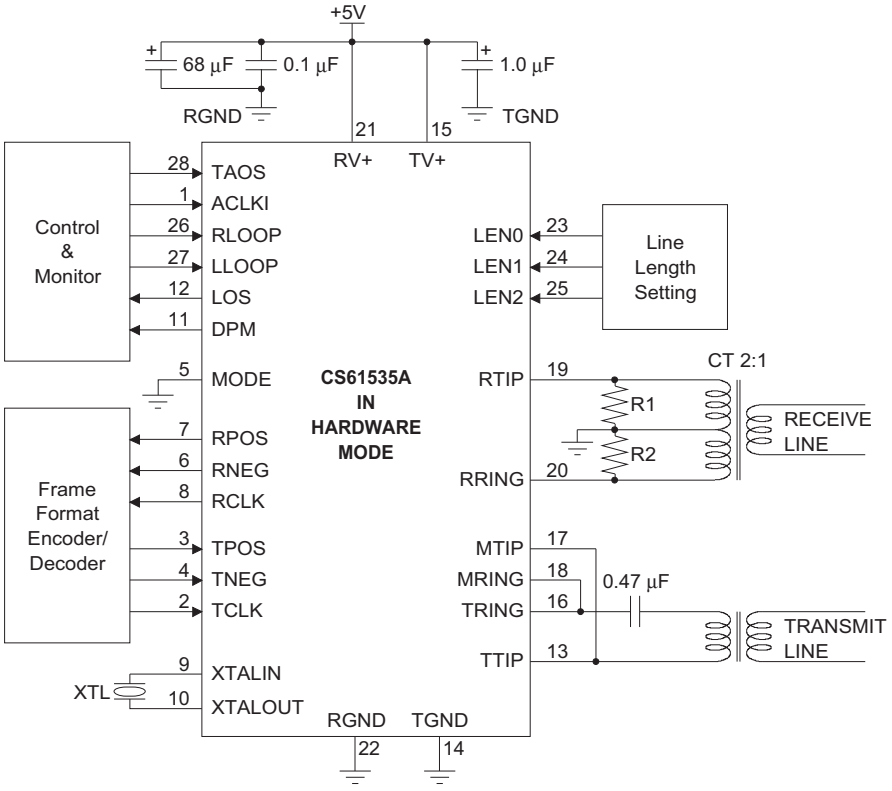


Figure A2. Hardware Mode Configuration

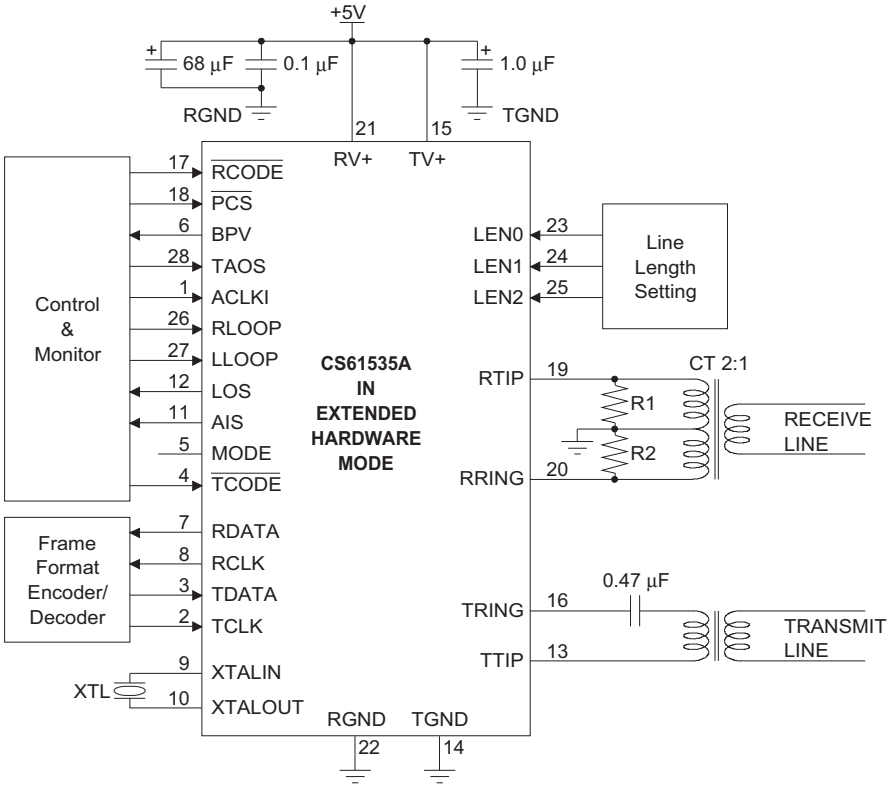


Figure A3. Extended Hardware Mode Configuration

Appendix A for crystal specifications.

Using the CS61535A for SONET

The CS61535A can be applied to SONET VT1.5 and VT 2.0 interface circuits as shown in Figure A5. The SONET data rate is 51.84 MHz, and has 6480 bits per frame (125 us per frame). An individual T1 frame (193 bits per frame) or PCM-30 frame (256 bits per frame) has its data mapped into the 6480 bit SONET frame. The mapping does not result in a uniform spacing between sucessive T1 (or E1) bits. Rather, for locked VT applications, gaps as large as 24 T1 bit periods or 32 E1 bit periods can exist between successive bits. With floating VTs, the gaps can be even larger.

The circuit in Figure A5 eliminates the demultiplexing jitter in a two-step approach. The first step uses a FIFO which is filled at a 51.84 MHz rate (when T1 or E1 bits are present), and which is emptied at a sub-multiple of the 51.84 rate. The FIFO is emptied only when it contains data. When the FIFO is empty the output clock is not pulsed.

The sub-multiple rate chosen should be slightly faster than the target rate (1.544 or 2.048 MHz), but as close to the target rate as possible. For

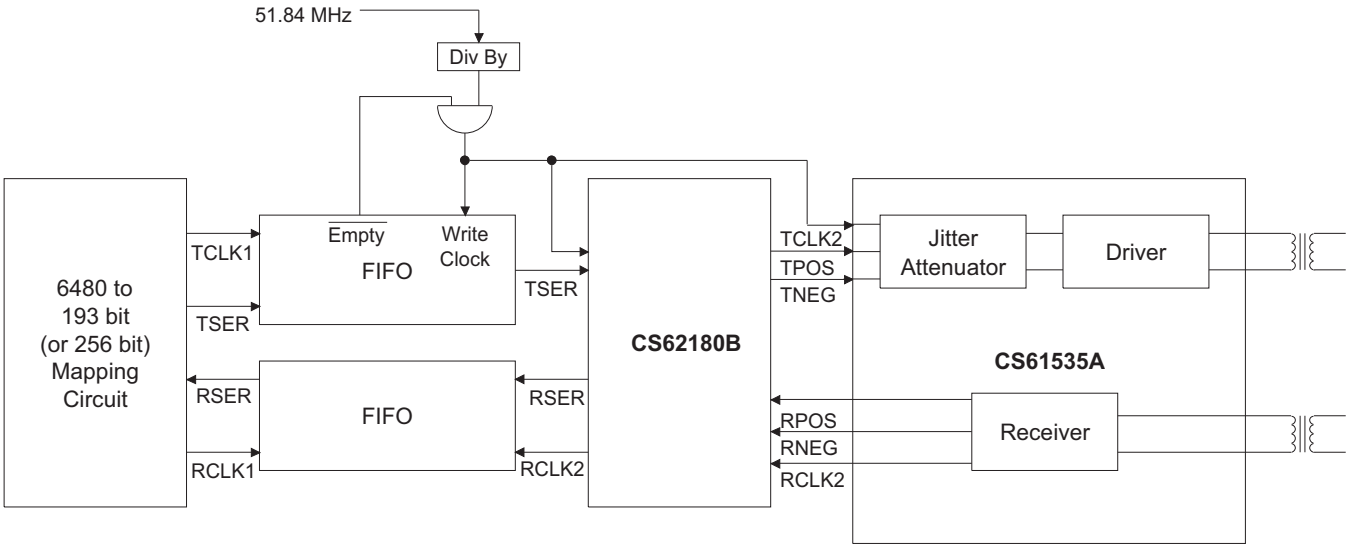


Figure A5. SONET Application

locked VT operation, Table A1 shows potential sub-multiple data rates, and the impact on those rates on the maximum gap in the output clock of the FIFO, and depth of FIFO required. FIFO depth will have to be increased for floating VT operation, with 8 bits of FIFO depth being added for each pointer alignment change that can occur.

The objective that should be met in picking a FIFO depth and clock divider is keep the maximum gap on the output of the FIFO at 12 bits or less. Twelve bits is the maximum jitter which can be input to the CS61535A's jitter attenuator without causing the overflow/underflow protection circuit to operate. The CS61535A then removes the remaining jitter from the signal.

The receive path also requires a bit mapping (from 193 or 256 bits to 6480 bits). This mapping requires an input buffer with the same depth as use on the transmit path. This buffer also absorbs the output jitter generated by the CS61535A's digital clock recovery.

Transformers

Recommended transmitter and receiver transformer specifications for the CS61535A are shown in Table A2. The transformers in Table A3 have been tested and recommended for use with the CS61535A. Refer to the "Telecom Transformer Selection Guide" for detailed schematics which show how to connect the line interface IC with a particular transformer.

In applications with the CS61535A where it is advantageous to use a single transmitter transformer for both 75Ω and 120Ω E1 applications, a 1:1.26 transforer may be used. Although transmitter return loss will be reduced for 75Ω applications, the pulse amplitude will be correct across a 75 Ω load.

Target Rate (MHz)	Clock Divider	Resultant Rate (MHz)	Maximum Gap		FIFO Depth Required
			(µs)	bits	
1.544	32	1.620	6.2	10	21
1.544	33	1.571	3.9	6	26
2.048	25	2.074	3.4	7	34

Table A1. Locked VT FIFO Analysis

Parameter	CS61535A Receiver	CS61535A Transmitter
Turns Ratio	1:2 CT ± 5%	1:1 ± 1.5 % for 75 Ω E1 1:1.15 ± 5 % for 100 Ω T1 1:1.26 ± 1.5 % for 120 Ω E1
Primary Inductance	600 µH min. @ 772 kHz	1.5 mH min. @ 772 kHz
Primary Leakage Inductance	1.3 µH max. @ 772 kHz	0.3 µH max. @ 772 kHz
Secondary Leakage Inductance	0.4 µH max. @ 772 kHz	0.4 µH max. @ 772 kHz
Interwinding Capacitance	23 pF max.	18 pF max.
ET-constant	16 V-µs min. for T1 12 V-µs min. for E1	16 V-µs min. for T1 12 V-µs min. for E1

Table A2. Transformer Specifications

Application	Turns Ratio(s)	Manufacturer	Part Number	Package Type
RX: T1 & E1	1:2CT	Pulse Engineering	PE-65351	1.5 kV through-hole, single
		Schott	67129300	
		Bel Fuse	0553-0013-HC	
TX: T1	1:1.15	Pulse Engineering	PE-65388	1.5 kV through-hole, single
		Schott	67129310	
		Bel Fuse	0553-0013-RC	
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65389	1.5 kV through-hole, single
		Schott	67129320	
		Bel Fuse	0553-0013-SC	
RX &TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65565	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-7J	
RX &TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65566	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-8J	
RX &TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65765	1.5 kVsurface-mount, dual
		Bel Fuse	S553-0013-06	
RX &TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65766	1.5 kV surface-mount, dual
		Bel Fuse	S553-0013-07	
RX : T1 & E1	1:2CT	Pulse Engineering	PE-65835	3 kV through-hole, single EN60950, EN41003 approved
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65839	3 kV through-hole, single EN60950, EN41003 approved

Table A3. Recommended Transformers For The CS61535A

APPENDIX A. RECOMMENDED CRYSTAL SPECIFICATIONS

Cirrus Logic telecommunication devices that offer jitter attenuation require crystals with specifications for frequency pullability. The crystal oscillation frequency is dictated by capacitive loading, which is controlled by the chip. Therefore, the crystals must meet the following specifications.

6.176 MHz Crystal Performance Specifications

Parameter			Min	Typ	Max	Units
Total Frequency Range		(Note 1)	-	370	390	ppm
Operating Frequency	C_{load} = 11.6 pF	(Note 2)	6.176803	-	-	MHz
	C_{load} = 19.0 pF	(Note 3)	6.175846	6.176000	6.176154	MHz
	C_{load} = 37.0 pF	(Note 2)	-	-	6.175197	MHz

8.192 MHz Crystal Performance Specifications

Parameter			Min	Typ	Max	Units
Total Frequency Range		(Note 1)	-	210	245	ppm
Operating Frequency	C_{load} = 11.6 pF	(Note 2)	8.192410	-	-	MHz
	C_{load} = 19.0 pF	(Note 3)	8.191795	8.192000	8.192205	MHz
	C_{load} = 37.0 pF	(Note 2)	-	-	8.191590	MHz

Notes: 1. With C_{load} varying from 11.6 to 37.0 pF at a given temperature.

2. Measured at -40 to 85°C.

3. Measured with Saunders 150D meter at 25 °C.

REVISION HISTORY

Revision	Date	Changes
F3	Jul '09	Removed development system info. (No longer supported). Removed PDIP option. Changed PLCC package option to lead-free.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **http://www.cirrus.com**

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