KM93C46 CMOS EEPROM

1K Bit Serial Electrically Erasable PROM

FEATURES

- **Operating temperature range**
  - **KM93C46: Commercial**
  - **KM93C46I: Industrial**
- **Single 5 Volt supply**
- **High performance advanced CMOS technology**
  - **Reliable floating gate technology**
- **64 x 16 serial read/write memory**
- **TTL compatible**
- **Low power dissipation**
  - **Standby current: 250μA (TTL)**
  - **Active current: 3 mA (TTL)**
- **Self-timed programming cycle**
- **Device status signal during programming**
- **100,000 Cycle Endurance**
- **Available in plastic DIP and SOP**

GENERAL DESCRIPTION

The KM93C46 is a CMOS 5V-Only 1,024 bit non-volatile, sequential EEPROM. It is fabricated with the well defined floating gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

The KM93C46 is organized as 64 registers of 16 bits each, which can be read/written serially by a microprocessor. It operates in a self-timed mode with the DO pin indicating the READY/$\overline{\text{BUSY}}$ status of the device.

The KM93C46 is designed for applications up to 100,000 erase/write cycles per word and over 10 years of data retention.

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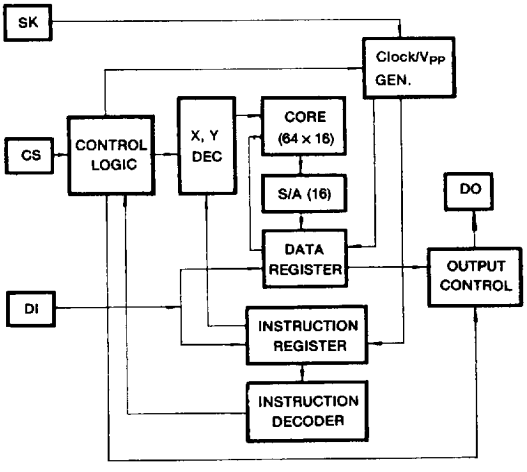
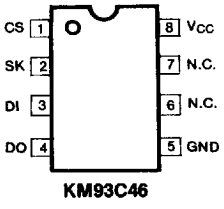
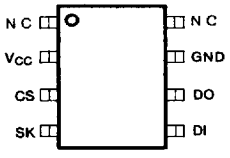
FUNCTIONAL BLOCK DIAGRAM



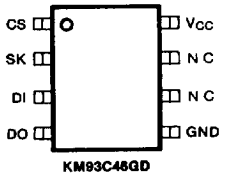
PIN CONFIGURATION



KM93C46



KM93C46G (SC46)



KM93C46GD (C46D)

Pin Name	Pin Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
N.C.	No Connection
V_{CC}	Power Supply
GND	Ground

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ABSOLUTE MAXIMUM RATINGS*

Item		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}	−0.3 to 7.0	V
Temperature Under Bias	Commercial	T_{bias}	−10 to +125	°C
	Industrial		−65 to +150	
Storage Temperature		T_{stg}	−65 to +150	°C

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

KM93C46 $T_A = 0$ to 70°C, Voltages referenced to V_{SS}
KM93C46I $T_A = -40$ to 85°C, Voltages referenced to V_{SS}

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Max	Unit
Operating Voltage	V_{CC}		4.5	5.5	V
Operating Current (DC)	I_{CC1}	$V_{CC} = 5.5V$, CS = 2.0V, SK = 2.0V		1	mA
Operating Current (AC)	I_{CC2}	$V_{CC} = 5.5V$, $f_{SK} = 1MHz$		3	mA
Standby Current (TTL)	I_{SB1}	$V_{CC} = 5.5V$, CS = 0.8V		250	μA
Standby Current (CMOS)	I_{SB2}	$V_{CC} = 5.5V$, CS = 0V		100	μA
Input Voltage Levels	V_{IL} V_{IH}		−0.3 2.0	0.8 $V_{CC}+0.3$	V V
Output Voltage Levels	V_{OL} V_{OH}	$I_{OL} = 2.1mA$ $I_{OH} = -400\mu A$	 2.4	0.4	V V
Input Leakage Current	I_{LI}	$V_{IN} = 5.5V$		10	μA
Output Leakage Current	I_{LO}	$V_{OUT} = 5.5V$, CS = 0V		10	μA

INSTRUCTION SET FOR MODE SELECTION

Instruction	SB	OP Code	Address	Data	Comment
READ	1	10	A5A4A3A2A1A0	D_{OUT}	Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15-D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0	—	Erase register A5A4A3A2A1A0
EWEN	1	00	11XXXX	—	Erase/Write enable
EWDS	1	00	00XXXX	—	Erase/Write disable
ERAL	1	00	10XXXX	—	Erase all registers
WRAL	1	00	01XXXX	D15-D0	Write all registers

The KM93C46 provides 7 instructions as shown. Note that all the instructions start with a logic "1" start bit, and following 8 bits carry the OP code and the 6-bit address for 1 of 64, 16-bit registers.

AC TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and C_L=100pF

AC OPERATING CHARACTERISTICS

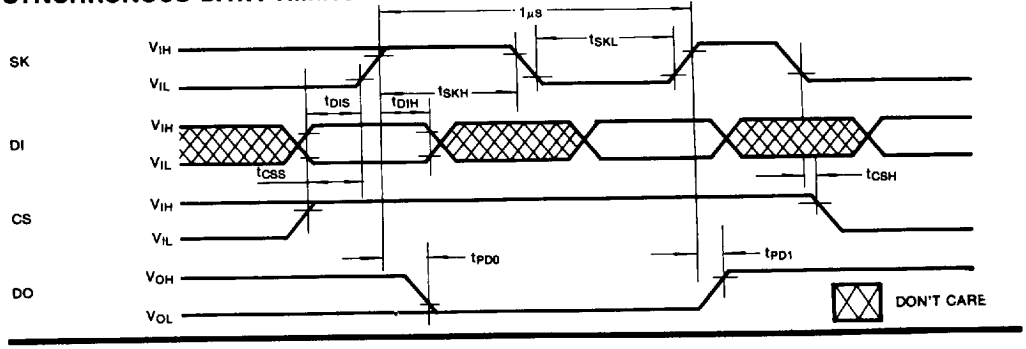
KM93C46 T_A=0°C to 70°C, V_{CC}=5V±10%, unless otherwise noted.
KM93C46I T_A= −40°C to 85°C, V_{CC}=5V±10%, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Max	Unit
SK Frequency	f_{SK}		—	1.0	MHz
SK High Time	t_{SKH}	(Note 1)	500		ns
SK Low Time	t_{SKL}	(Note 1)	250		ns
Chip Select Setup Time	t_{CSS}		50		ns
Chip Select Hold Time	t_{CSH}		0		ns
Data Setup Time	t_{DIS}		150		ns
Data Hold Time	t_{DIH}		150		ns
Output High Delay Time	t_{PD1}	V_{OL}=0.8V, V_{OH}=2.0V		500	ns
Output Low Delay Time	t_{PD0}	V_{IL}=0.45V, V_{IH}=2.4V		500	ns
Self-Timed Program Cycle Time	$t_{E/W}$			10	ms
Min CS Low Time	t_{CS}	(Note 2)	250		ns
Rising Edge of CS to Status Valid	t_{SV}			500	ns
Falling Edge of CS to D_{OUT} High-Z	t_{OH}, t_{IH}			100	ns

Note 1: The SK frequency spec, specifies a minimum SK clock period of 1μs, therefore in a SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 1μs.
e.g., if t_{SKL}=250ns then the minimum t_{SKH}=750ns in order to meet the SK frequency specification.
Note 2: CS must be brought low for a minimum 250ns(t_{CS}) between consecutive instruction cycles.

TIMING DIAGRAMS

SYNCHRONOUS DATA TIMING



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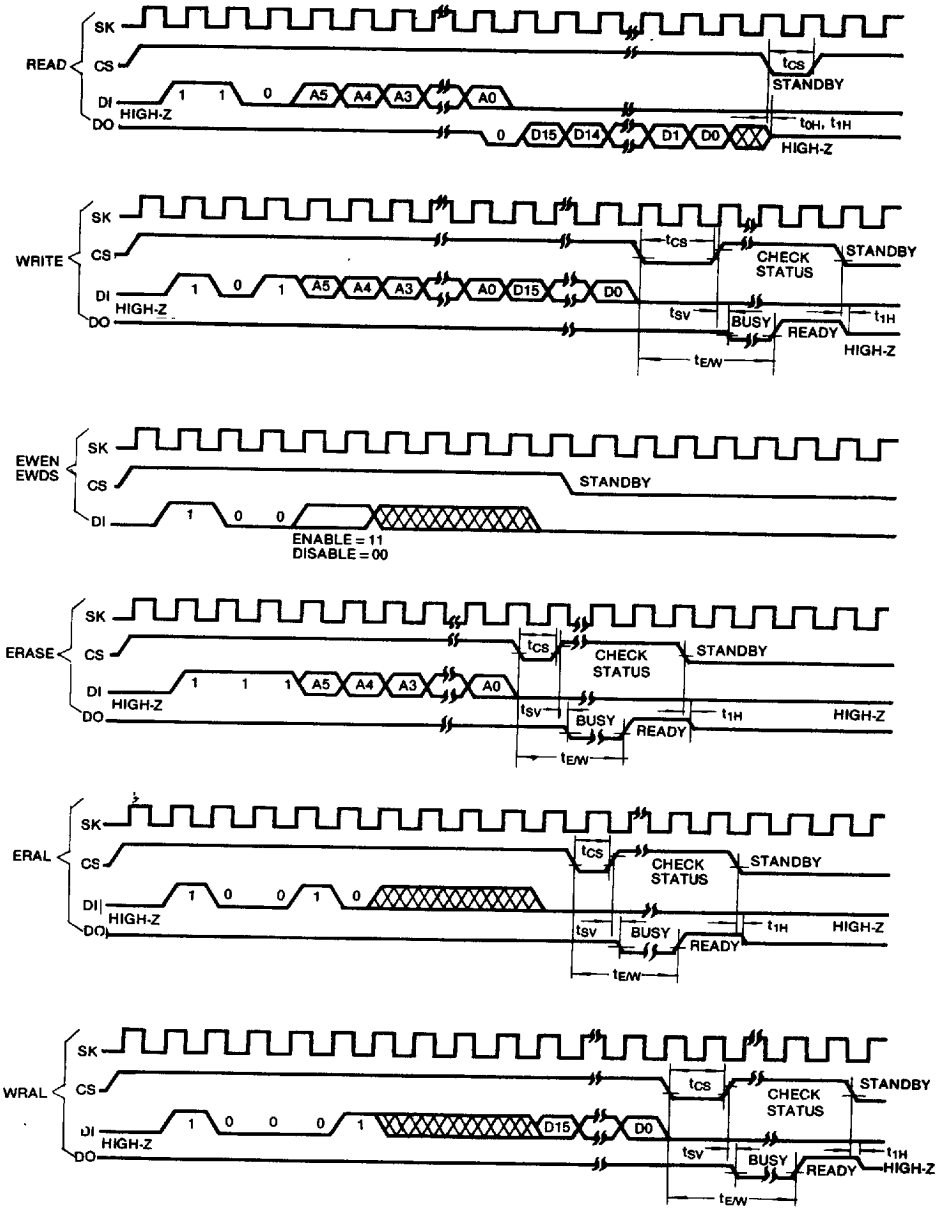
TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING



DEVICE OPERATION

The KM93C46 is a 1K bit CMOS serial I/O EEPROM used with microcontrollers for non-volatile memory applications. The on-chip programming voltage generator allows user to use a single 5V power supply. The erase and write cycle of the KM93C46 is self-timed with the ready/$\overline{busy}$ status of the chip indicated at the DO pin. All the operations of the chip are preceded by two OP code bits, facilitating inherent protection against false writes. The DO pin is high-Z except for the read period and the ready/$\overline{busy}$ indication period to eliminate bus contention.

READ

After a read instruction and address set is received, low to high transition of the SK clock produces output data at DO pin. A dummy bit (logical "0") proceeds the 16 bit data output string.

EWEN / EWDS

The KM93C46 is at the erase/write disable (EWDS) state during the power-up period to protect against accidental distrubance. After the power up period, the erase/write operation must be preceded by an erase/write enable (EWEN) operation. The erase/write enable (EWEN) mode is maintained until an erase/write disable (EWDS) operation is executed or V_{CC} is removed from the part. Execution of the READ operation is independent of both EWEN and EWDS instructions

ERASE

Before a write cycle, an erase cycle need to be operated to reset the EEPROM cells to the "erase ' state. The chip starts the self-timed erase cycle by dropping CS low after an erase instruction and address set is input The chip s ready/$\overline{busy}$ status is indicated at the DO pin by bringing CS high during erase cycle

WRITE

The write operation is started by sequentially loading its instruction, address, and data set. After the last bit of data is input on the DI pin, CS must be brought low before the rising edge of the SK clock. This falling edge of CS initiates the self-timed write cycle. Like the erase operation, write cycle has the ready/$\overline{busy}$ function.

ERAL (chip erase)

Entire memory array is erased, i.e., logical "1" state, by this chip erase (ERAL) operation. The chip erase cycle is identical to the erase cycle except for different OP code.

WRAL (chip write)

The entire array needs to be erased before this chip write mode operation. Data given during this mode are written to all cells in the corresponding column simultaneously

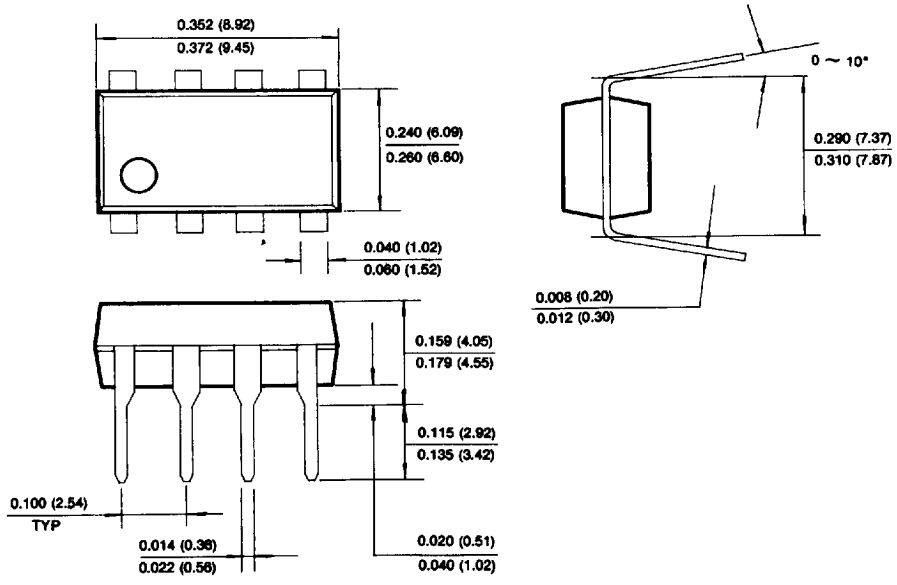
READY / $\overline{BUSY}$

The ready/$\overline{busy}$ status of the KM93C46 during all the self-timed programming cycle (erase, write, chip erase, chip write) is indicated at the DO pin. Bringing the CS pin high, after self-timed programming cycle has been initiated, will produce logic '0' at the DO pin if the chip is still programming and a logic '1' if the programming cycle has been completed.

PACKAGE DIMENSIONS

8 PIN PLASTIC DUAL IN LINE PACKAGE

unit: inches (millimeters)



8 PIN PLASTIC SMALL OUT LINE PACKAGE