Never stop thinking

# TLE4699

Low Drop Out Linear Voltage Regulator
5 V Fixed Output Voltage

## Data Sheet

Rev. 1.0, 2010-11-30

## Automotive Power

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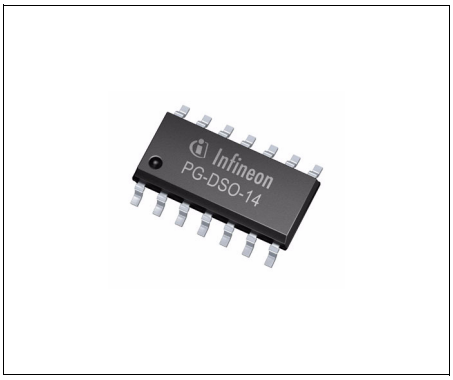
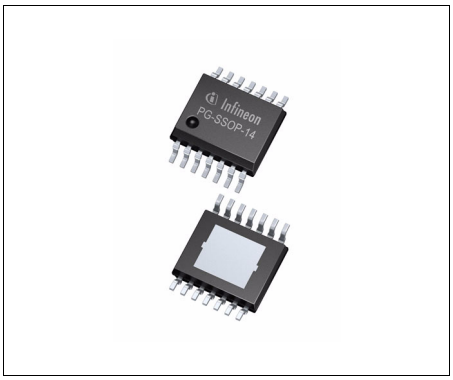
**Low Drop Out Linear Voltage Regulator** **TLE4699**
**5 V Fixed Output Voltage**

# 1 Overview




**PG-DSO-14**




**PG-SSOP-14 EP**

### Features

- Output Voltage 5 V ± 2%
- Current Capability 200 mA
- Ultra Low Current Consumption
- Very Low Drop Out Voltage
- Enable Function: Below 1µA Current Consumption in off mode
- Reset Circuit Sensing the Output Voltage
  with Programmable Switching Threshold and Delay Time
- Reset Output Active Low Down to $V_Q$ = 1 V
- Integrated Early Warning Comparator
- Excellent Line Transient Robustness
- Maximum Input Voltage -42 V ≤ $V_I$ ≤ +45 V
- Reverse Polarity Protection
- Short Circuit Protected
- Overtemperature Shutdown
- Automotive Temperature Range -40 °C ≤ $T_j$ ≤ 150 °C
- Available in a small thermally enhanced PG-SSOP-14 EP package
- Green Product (RoHS Compliant)
- AEC Qualified

### Description

The TLE4699 is a monolithic integrated low drop out fixed output voltage regulator for loads up to 200 mA. An input voltage of up to 45 V is regulated to an output voltage of 5 V. The integrated reset as well as several protection circuits, combined with a wide operating temperature range offered by the TLE4699 make it suitable for supplying microprocessor systems in automotive environments.

The early warning function supervises the voltage at pin SI. Modifying the reset threshold is possible by an optional resistor divider.

The TLE4699 is available in a PG-DSO-14 package which makes it pin-compatible to the TLE4299 as well as in a small thermally enhanced PG-SSOP-14 EP exposed pad package.

| Type | Package | Marking |
|---|---|---|
| TLE4699GM | PG-DSO-14 | TLE4699 |
| TLE4699E | PG-SSOP-14 EP | TLE4699 |

# 2 Block Diagram

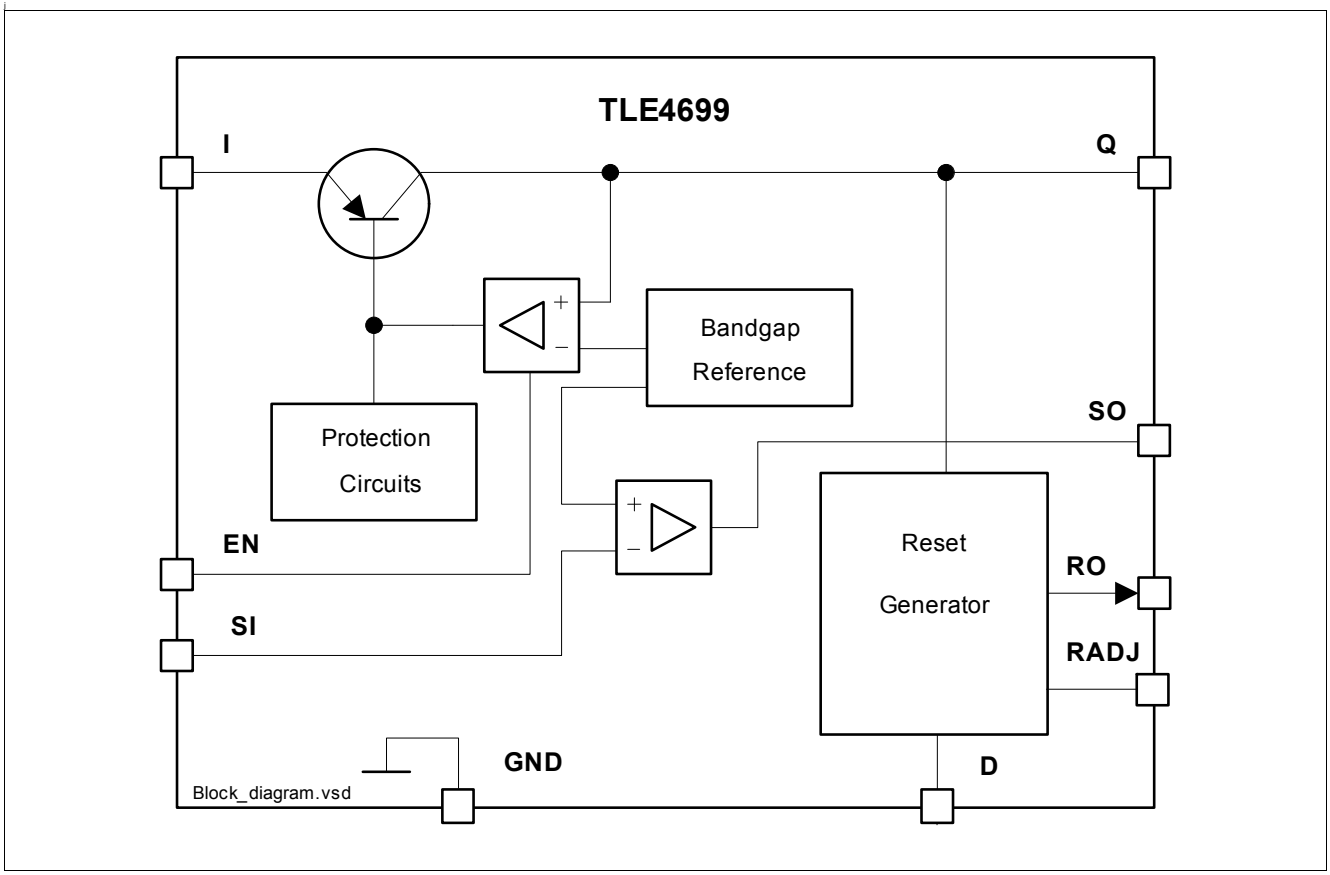



**Figure 1 Block Diagram TLE4699**

# 3 Pin Configuration

## 3.1 Pin Assignment TLE4699GM (PG-DSO-14)

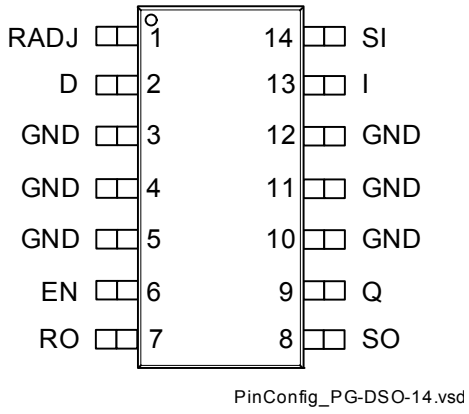



**Figure 2 Pin Configuration PG-DSO-14 Package (top view)**

## 3.2 Pin Definitions and Functions TLE4699GM (PG-DSO-14)

| Pin | Symbol | Function |
|---|---|---|
| 1 | RADJ | **Reset Threshold Adjust**<br>Connect an external voltage divider to adjust reset threshold;<br>Connect to GND for using internal threshold. |
| 2 | D | **Reset Delay**<br>Connect a ceramic capacitor from D (Pin 2) to GND for reset delay time adjustment;<br>Leave open, if the reset function is not needed. |
| 3, 4, 5 | GND | **Ground**<br>Connect all pins to heat sink area. |
| 6 | EN | **Enable**<br>High signal enables the regulator;<br>Low signal disables the regulator;<br>Connect to I if the enable function is not needed |
| 7 | RO | **Reset Output**<br>Open collector output with an internal pull-up resistor to the output Q;<br>An additional external pull-up resistor to the output Q is optional;<br>Leave open if the reset function is not needed. |
| 8 | SO | **Sense Output**<br>Open collector output with an internal pull-up resistor to the output Q;<br>An additional external pull-up resistor to the output Q is optional;<br>Leave open if the sense function is not needed. |
| 9 | Q | **5 V Regulator Output**<br>Connect a capacitor between Q (Pin 9) and GND close to the IC pins, respecting the values given for its capacitance $C_Q$ and ESR in the table **Chapter 4.2 Functional Range**. |
| 10, 11, 12 | GND | **Ground**<br>Connect all pins to heat sink area. |

| Pin | Symbol | Function |
|---|---|---|
| 13 | I | **Regulator Input and IC Supply**<br>for compensating line influences, a capacitor to GND close to the IC pin is recommended. |
| 14 | SI | **Sense Input**<br>Connect the voltage rail to be monitored;<br>Connect to Q if the sense comparator is not needed. |

## 3.3 Pin Assignment TLE4699E

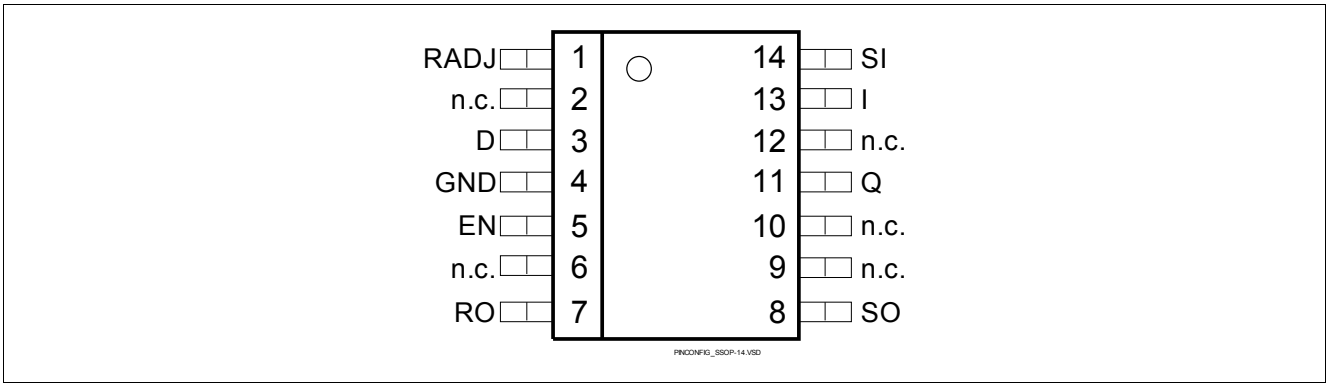



**Figure 3 Pin Configuration PG-SSOP-14 EP Package (top view)**

## 3.4 Pin Definitions and Functions TLE4699E (PG-SSOP-14 EP)

| Pin | Symbol | Function |
|---|---|---|
| 1 | RADJ | **Reset Threshold Adjust**<br>Connect an external voltage divider to adjust reset threshold;<br>Connect to GND for using internal threshold. |
| 3 | D | **Reset Delay**<br>Connect a ceramic capacitor from D (Pin 3) to GND for reset delay time adjustment;<br>Leave open, if the reset function is not needed. |
| 4 | GND | **Ground**<br>Connect to heat sink area. |
| 5 | EN | **Enable**<br>High signal enables the regulator;<br>Low signal disables the regulator;<br>Connect to I if the enable function is not needed |
| 7 | RO | **Reset Output**<br>Open collector output with an internal pull-up resistor to the output Q;<br>An additional external pull-up resistor to the output Q is optional;<br>Leave open if the reset function is not needed. |
| 8 | SO | **Sense Output**<br>Open collector output with an internal pull-up resistor to the output Q;<br>An additional external pull-up resistor to the output Q is optional;<br>Leave open if the sense function is not needed. |
| 11 | Q | **5 V Regulator Output**<br>Connect a capacitor between Q (Pin 11) and GND close to the IC pins, respecting the values given for its capacitance $C_Q$ and ESR in the table **Chapter 4.2 Functional Range**. |
| 13 | I | **Regulator Input and IC Supply**<br>For compensating line influences, a capacitor to GND close to the IC pin is recommended. |
| 14 | SI | **Sense Input**<br>Connect the voltage rail to be monitored;<br>Connect to Q if the sense comparator is not needed. |

| Pin | Symbol | Function |
|---|---|---|
| 2, 6, 9, 10, 12 | n.c. | **Not connected**<br>Internally not connected; Connection to PCB GND recommended. |
| PAD | | **Exposed Pad**<br>Attach the exposed pad on package bottom to the heatsink area on circuit board; Connect to GND |

# 4 General Product Characteristics

## 4.1 Absolute Maximum Ratings

**Absolute Maximum Ratings [1)]**

$T_j$ = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| **Voltage Rating** | | | | | | |
| 4.1.1 | Regulator Input and IC Supply I | $V_I$ | -42 | 45 | V | – |
| 4.1.2 | Enable Input EN | $V_{EN}$ | -42 | 45 | V | – |
| 4.1.3 | Sense Input SI | $V_{SI}$ | -42 | 45 | V | – |
| 4.1.4 | Regulator Output Q | $V_Q$ | -1 | 7 | V | – |
| 4.1.5 | Sense Output SO | $V_{WI}$ | -0.3 | 7 | V | – |
| 4.1.6 | Reset Output RO | $V_{RO}$ | -0.3 | 7 | V | – |
| 4.1.7 | Reset Delay D | $V_D$ | -0.3 | 7 | V | – |
| 4.1.8 | Reset Switching Threshold Adjust RADJ | $V_{RADJ}$ | -0.3 | 7 | V | – |
| **Temperatures** | | | | | | |
| 4.1.9 | Junction Temperature | $T_j$ | -40 | 150 | °C | – |
| 4.1.10 | Storage Temperature | $T_{stg}$ | -55 | 150 | °C | – |
| **ESD Susceptibility** | | | | | | |
| 4.1.11 | ESD Resistivity | $V_{ESD}$ | -4 | 4 | kV | HBM [2)] |
| 4.1.12 | ESD Resistivity | $V_{ESD}$ | -1500 | 1500 | V | CDM [3)] |

1) Not subject to production test, specified by design.

2) ESD susceptibility, Human Body Model “HBM” according to AEC-Q100-002-JESD 22-A114.

3) ESD susceptibility, Charged Device Model “CDM” according to ESDA STM5.3.1.

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

| Pos. | Parameter | Symbol | Limit Values | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| 4.2.1 | Input Voltage Range for Normal Operation | $V_{I(nor)}$ | $V_Q + V_{dr}$ | 45 | V | 1) |
| 4.2.2 | Extended Input Voltage Range | $V_{I(ext)}$ | 3.3 | 45 | V | 2) |
| 4.2.3 | Input Voltage Transient Immunity | $dV_I/dt$ | -10 | 20 | V/µs | $dV_I \leq 10$ V; $V_I > 9$ V; No trigger of RO.3) |
| 4.2.4 | Junction Temperature | $T_j$ | -40 | 150 | °C | – |
| 4.2.5 | Output Capacitor Requirements | $C_Q$ | 10 | – | µF | –4) |
| 4.2.6 | | $ESR_{CQ}$ | – | 3 | Ω | –5) |

1) For specification of the input voltage $V_Q$ and the drop out voltage $V_{dr}$ see **Chapter 5 Voltage Regulator**.

2) The output voltage VQ will follow the input voltage, but is outside the specified range. For details see **Chapter 5 Voltage Regulator**.

3) Transient measured directly at the input pin. Not subject to production test, specified by design.

4) Not subject of production test, specified by design.

The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

5) Relevant ESR value at $f$ = 10 kHz

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 4.3 Thermal Resistance

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| **TLE4699GM Package PG-DSO-14** | | | | | | | |
| 4.3.1 | Junction to Soldering Point[1)] | $R_{thJSP}$ | – | 27 | – | K/W | Pins 3-5 and 10-12 fixed to $T_A$ |
| 4.3.2 | Junction to Ambient | $R_{thJA}$ | – | 112 | – | K/W | Footprint only[2)] |
| 4.3.3 | | | – | 73 | – | K/W | 300 mm² PCB heat sink area[2)] |
| 4.3.4 | | | – | 65 | – | K/W | 600 mm² PCB heat sink area[2)] |
| 4.3.5 | | | – | 63 | – | K/W | 2s2p PCB [3)] |
| **TLE4699E Package PG-SSOP-14 EP** | | | | | | | |
| 4.3.6 | Junction to Soldering Point[1)] | $R_{thJSP}$ | – | 10 | – | K/W | – |
| 4.3.7 | Junction to Ambient[1)] | $R_{thJA}$ | – | 140 | – | K/W | Footprint only[2)] |
| 4.3.8 | | | – | 63 | – | K/W | 300 mm² PCB heat sink area[2)] |
| 4.3.9 | | | – | 53 | – | K/W | 600 mm² PCB heat sink area[2)] |
| 4.3.10 | | | | 47 | | K/W | 2s2p PCB[3)] |

1) Not subject to production test, specified by design

2) Specified $R_{thJA}$ value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 x 70µm Cu).

3) Specified $R_{thJA}$ value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

# 5 Voltage Regulator

## 5.1 Description Voltage Regulator

The output voltage $V_Q$ is controlled by comparing a portion of it to an internal reference and driving a PNP pass transistor accordingly. Saturation control as a function of the load current prevents any oversaturation of the pass element. The control loop stability depends on the output capacitor $C_Q$, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table "**"Functional Range" on Page 10** have to be maintained. For details see also the typical performance graph "Output Capacitor Series Resistor $ESR_{CQ}$ vs. Output Current $I_Q$". Also, the output capacitor shall be sized to buffer load transients.

An input capacitor $C_I$ is not needed for the control loop stability, but recommended to buffer line influences. Connect the capacitors close to the IC terminals.

Protection circuitry prevent the IC as well as the application from destruction in case of catastrophic events. These safeguards contain output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at input voltages above $V_I$ = 22 V.

The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, a junction temperature above 150 °C is outside the maximum rating and therefore reduces the IC lifetime.

The TLE4699 allows a negative supply voltage. However, several small currents are flowing into the IC increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity condition.

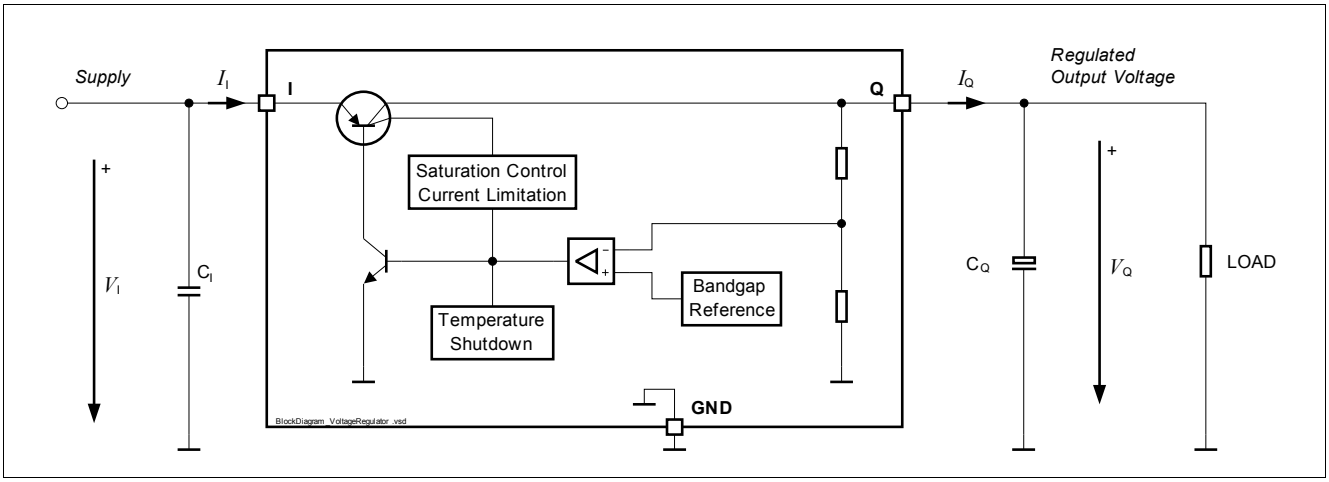



**Figure 4 Block Diagram Voltage Regulator Circuit**

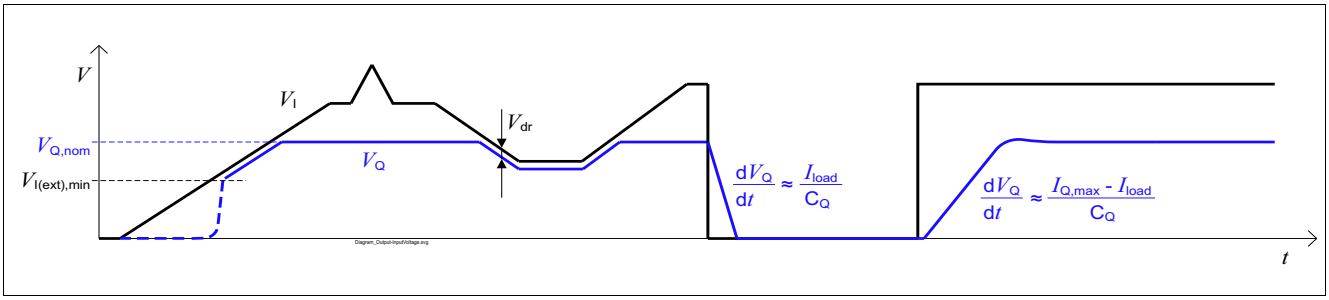



**Figure 5 Output Voltage vs. Input Voltage**

## 5.2 Electrical Characteristics Voltage Regulator

**Electrical Characteristics: Voltage Regulator**

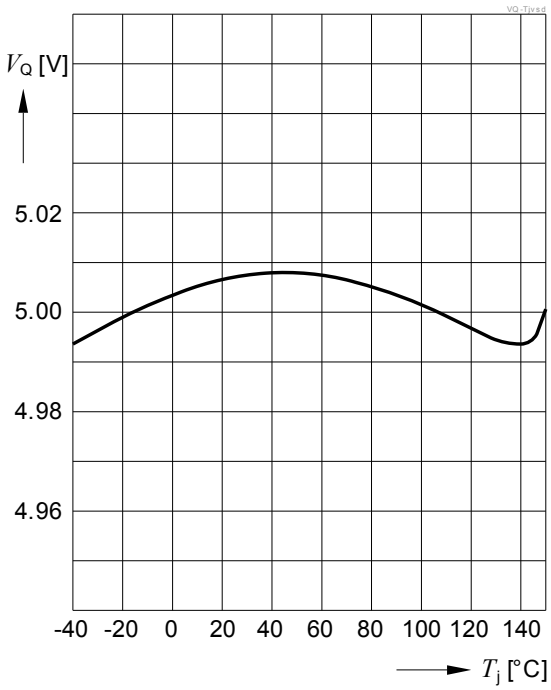
$V_I$ = 13.5 V, $T_j$ = -40 °C to +150 °C,
all voltages with respect to ground, direction of currents as shown in **Figure 4** (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 5.2.1 | Output Voltage | $V_Q$ | 4.9 | 5.0 | 5.1 | V | 0 mA ≤ $I_Q$ ≤ 200 mA; 8 V ≤ $V_I$ ≤ 18 V |
| 5.2.2 | | | | | | | 0 mA ≤ $I_Q$ ≤ 150 mA; 6 V ≤ $V_I$ ≤ 18 V |
| 5.2.3 | | | | | | | 0 mA ≤ $I_Q$ ≤ 100 mA; 18V ≤ $V_I$ ≤ 32 V $T_j$ ≤ 105 °C 1) 2) |
| 5.2.4 | | | | | | | 0 mA ≤ $I_Q$ ≤ 10 mA; 32 V ≤ $V_I$ ≤ 45 V $T_j$ ≤ 105 °C 1) 2) |
| 5.2.5 | | | | | | | 0.3 mA ≤ $I_Q$ ≤ 100 mA; 18 V ≤ $V_I$ ≤ 32 V 1) |
| 5.2.6 | | | | | | | 0.3 mA ≤ $I_Q$ ≤ 10 mA; 32 V ≤ $V_I$ ≤ 45 V 1) |
| 5.2.7 | Load Regulation steady-state | $\lvert dV_{Q,load}\rvert$ | – | 5 | 30 | mV | $I_Q$ = 1 mA to 150 mA; $V_I$ = 6 V |
| 5.2.8 | Line Regulation steady-state | $\lvert dV_{Q,line}\rvert$ | – | 2 | 20 | mV | $V_I$ = 6 V to 32 V; $I_Q$ = 5 mA |
| 5.2.9 | Power Supply Ripple Rejection | $PSRR$ | 60 | 65 | – | dB | $f_{ripple}$ = 100 Hz; $V_{ripple}$ = 1 Vpp 2) |
| 5.2.10 | Drop out Voltage $V_{dr}$ = $V_I$ - $V_Q$ | $V_{dr}$ | – | 90 | 200 | mV | $I_Q$ = 50 mA 3) |
| 5.2.11 | | | – | 160 | 350 | mV | $I_Q$ = 150 mA 3) |
| 5.2.12 | Output Current Limitation | $I_{Q,max}$ | 201 | 350 | 500 | mA | 0 V ≤ $V_Q$ ≤ 4.8 V |
| 5.2.13 | Reverse Current | $I_Q$ | -1.5 | -0.7 | – | mA | $V_I$ = 0 V; $V_Q$ = 5 V |
| 5.2.14 | Reverse Current at Negative Input Voltage | $I_I$ | -2 | -1 | – | mA | $V_I$ = -16 V; $V_Q$ = 0 V |
| 5.2.15 | | | -5 | -3,5 | – | mA | $V_I$ = -42 V; $V_Q$ = 0 V |
| 5.2.16 | Overtemperature Shutdown Threshold | $T_{j,sd}$ | 151 | – | 200 | °C | $T_j$ increasing 2) |
| 5.2.17 | Overtemperature Shutdown Threshold Hysteresis | $T_{j,hy}$ | – | 20 | – | K | $T_j$ decreasing 2) |

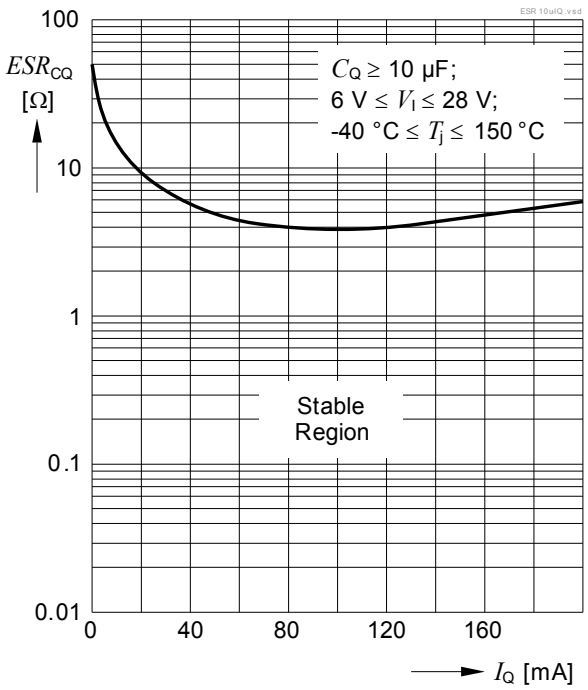
1) See typical performance graph for details.
2) Parameter not subject to production test; specified by design.
3) Measured when the output voltage $V_Q$ has dropped 100 mV from its nominal value.

## 5.3 Typical Performance Characteristics Voltage Regulator

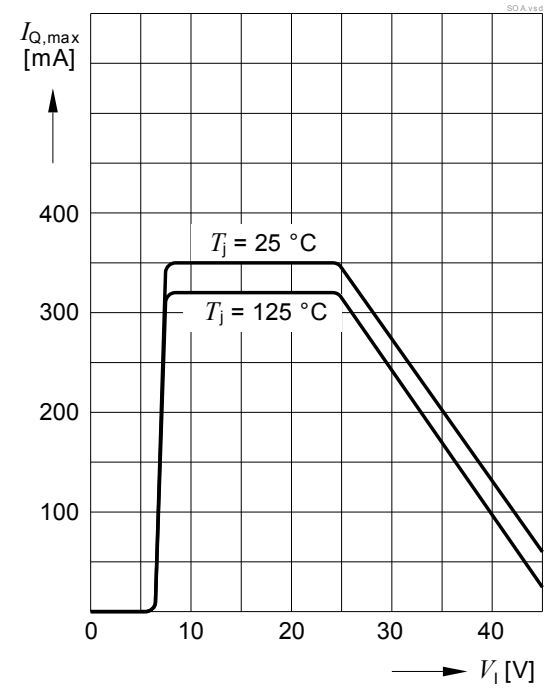
**Output Voltage $V_Q$ vs. Junction Temperature $T_j$**



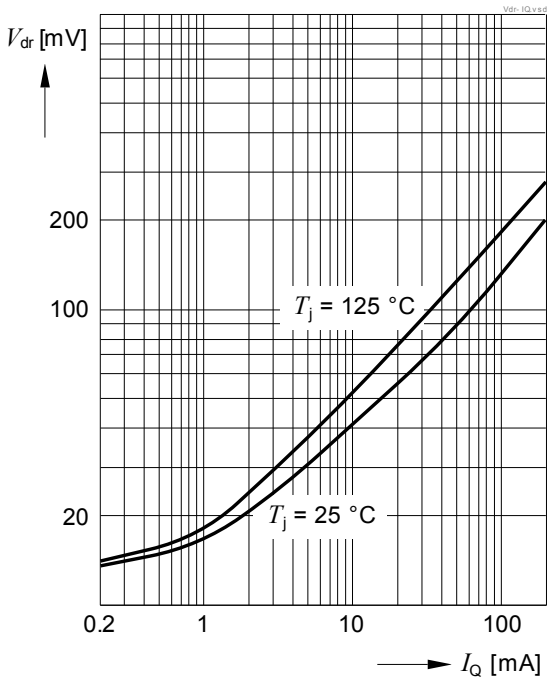

**Output Capacitor Series Resistor $ESR_{CQ}$ vs. Output Current $I_Q$**



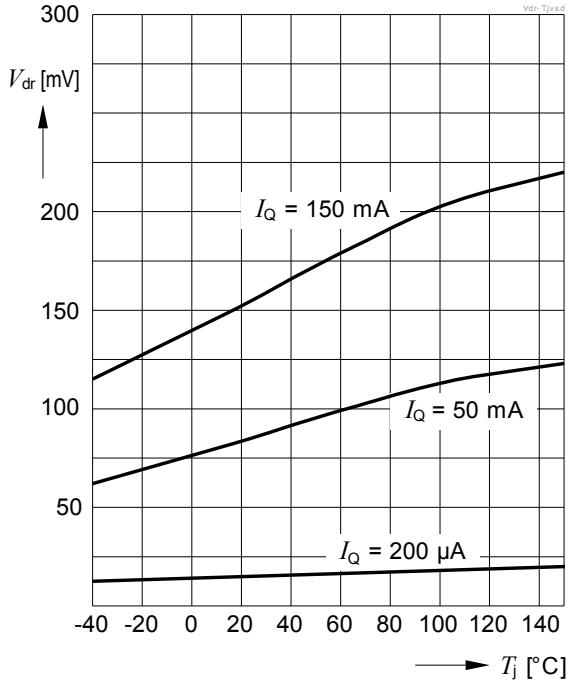

**Output Current Limitation $I_{Q,max}$ vs. Input Voltage $V_I$**



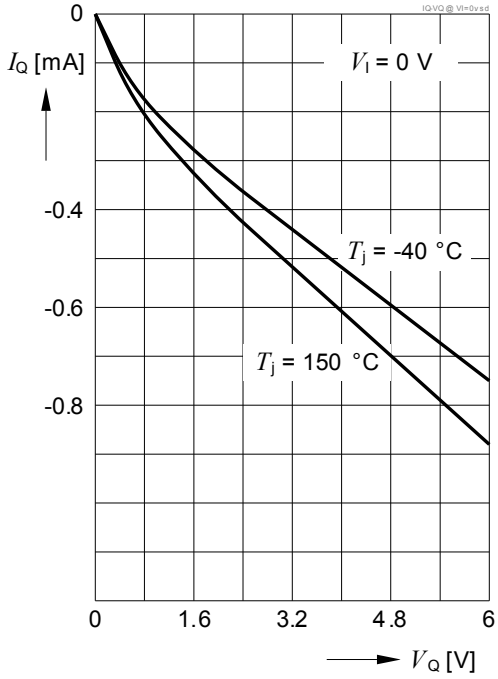
**Dropout Voltage $V_{dr}$ vs.
Output Current $I_Q$**



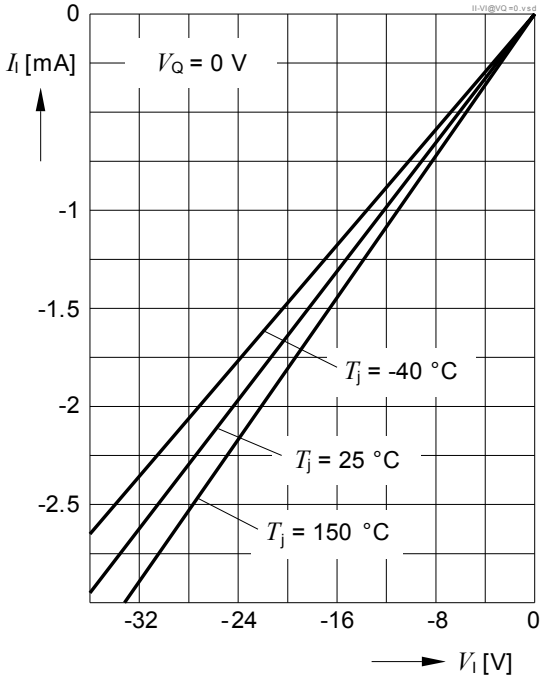

**Dropout Voltage $V_{dr}$ vs.
Junction Temperature $T_j$**




**Reverse Output Current $I_Q$ vs.
Output Voltage $V_Q$**




**Reverse Current $I_I$ vs.
Input Voltage $V_I$**



# 6 Current Consumption

## 6.1 Electrical Characteristics Current Consumption

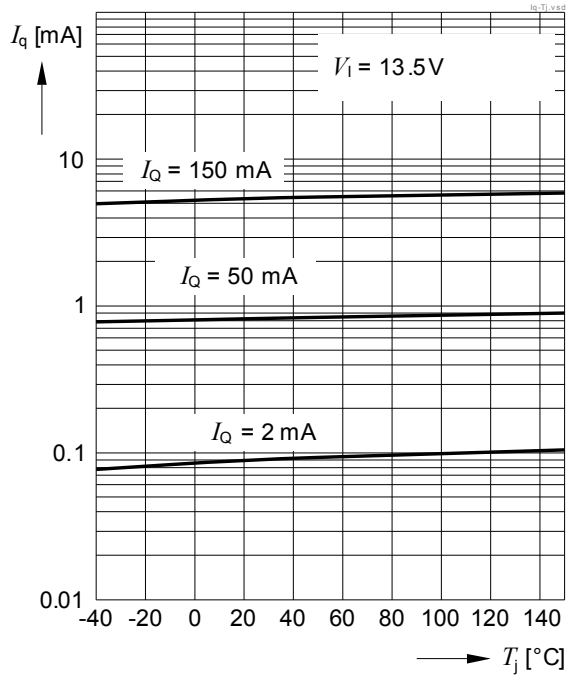
**Electrical Characteristics: Current Consumption**

$V_I$ = 13.5 V, $T_j$ = -40 °C to +150 °C, all voltages with respect to ground, direction of currents as shown in **Figure 6 "Parameter Definition" on Page 18** (unless otherwise specified)

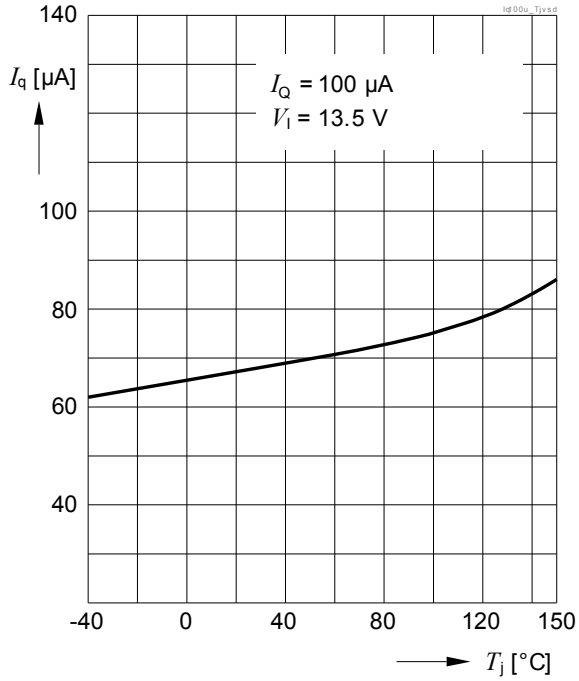
| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 6.1.1 | Current Consumption $I_q = I_I - I_Q$ | $I_{q,on}$ | – | 65 | 100 | µA | $I_Q \leq 200$ µA; $T_j \leq 25$ °C<br>Enable on |
| 6.1.2 | | | – | 80 | 105 | µA | $I_Q \leq 200$ µA; $T_j \leq 85$ °C<br>Enable on |
| 6.1.3 | | | – | 1.0 | 2.0 | mA | $I_Q$ = 50 mA<br>Enable on |
| 6.1.4 | | | – | 5 | 10 | mA | $I_Q$ = 150 mA<br>Enable on |
| 6.1.5 | Current Consumption $I_{q,off} = I_I$ | $I_{q,off}$ | – | – | 1 | µA | $T_j \leq 25$ °C<br>$V_{EN}$ = 0V |
| 6.1.6 | | | – | – | 2 | µA | $T_j \leq 85$ °C<br>$V_{EN}$ = 0V |

## 6.2 Typical Performance Characteristics Current Consumption

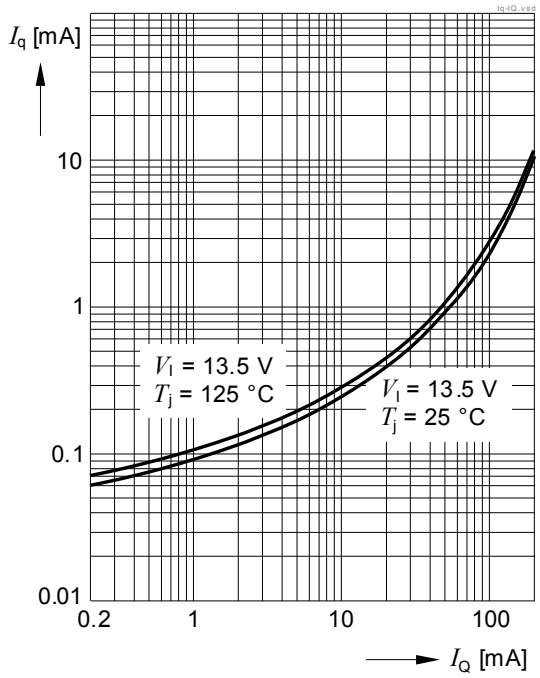
**Current Consumption $I_q$ vs. Junction Temperature $T_j$**



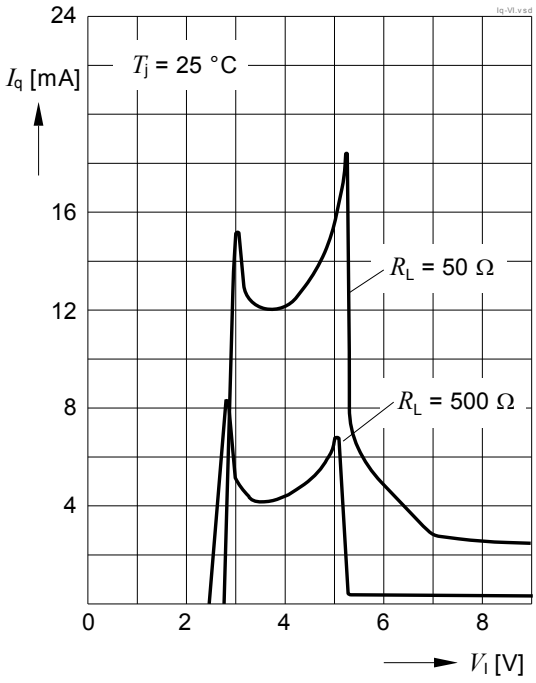

**Current Consumption $I_q$ vs. Junction Temperature $T_j$**




**Current Consumption $I_q$ vs. Output Current $I_Q$**




**Current Consumption $I_q$ vs. Input Voltage $V_I$**



# 7 Enable Function

## 7.1 Description Enable Function

The TLE4699 can be turned on or turned off via the EN Input. With voltage levels higher than $V_{EN,high}$ applied to the EN Input the device will be completely turned on. A voltage level lower than $V_{EN,low}$ sets the device to low quiescent current mode. In this condition the device is turned off and is not functional. The Enable Input has an build in hysteresis to avoid toggling between ON/OFF state, if signals with slow slope are applied to the input.

## 7.2 Electrical Characteristics Enable Function

**Electrical Characteristics: Enable Function**

$V_I$ = 13.5 V, $T_j$ = -40 °C to +150 °C, all voltages with respect to ground, direction of currents as shown in **Figure 6** (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 7.2.1 | Enable<br>Low Signal Valid | $V_{EN,low}$ | – | – | 0.8 | V | – |
| 7.2.2 | Enable<br>High Signal Valid | $V_{EN,high}$ | 2.4 | – | – | V | $V_Q > V_{Q.min}$ |
| 7.2.3 | Enable<br>Threshold Hysteresis | $V_{EN,hyst}$ | 50 | – | – | mV | – |
| 7.2.4 | Enable<br>Input current | $I_{EN}$ | – | 1 | 2 | µA | $V_{EN}$ = 5 V |
| 7.2.5 | Enable<br>internal pull-down resistor | $R_{EN}$ | 3.2 | 4.7 | 6.2 | MΩ | – |

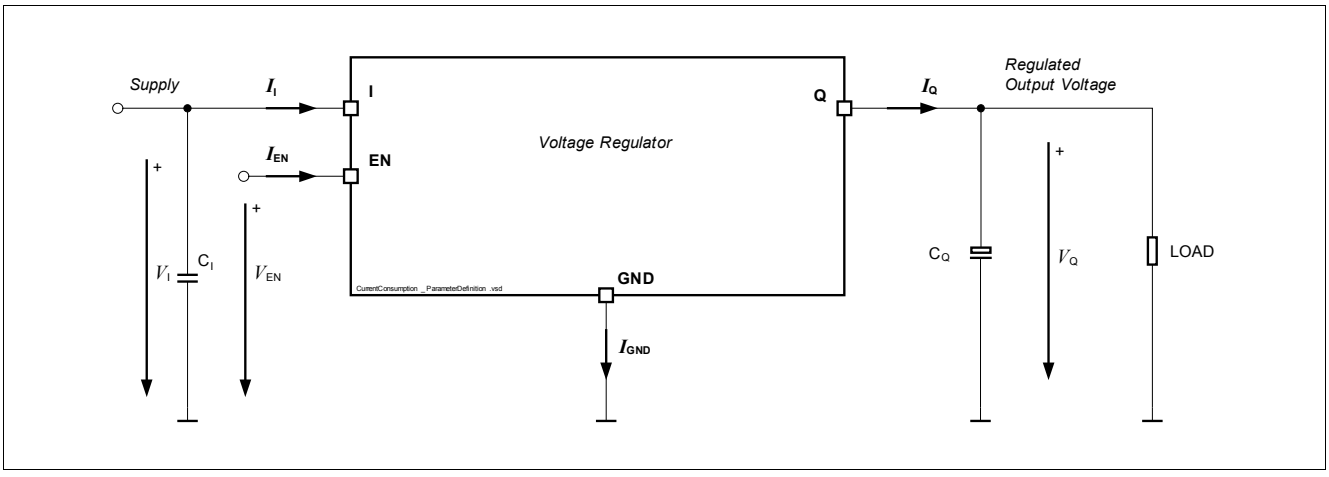
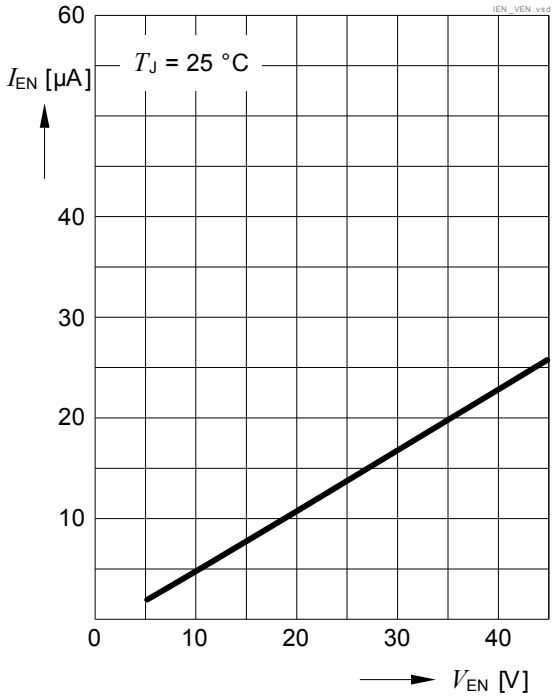


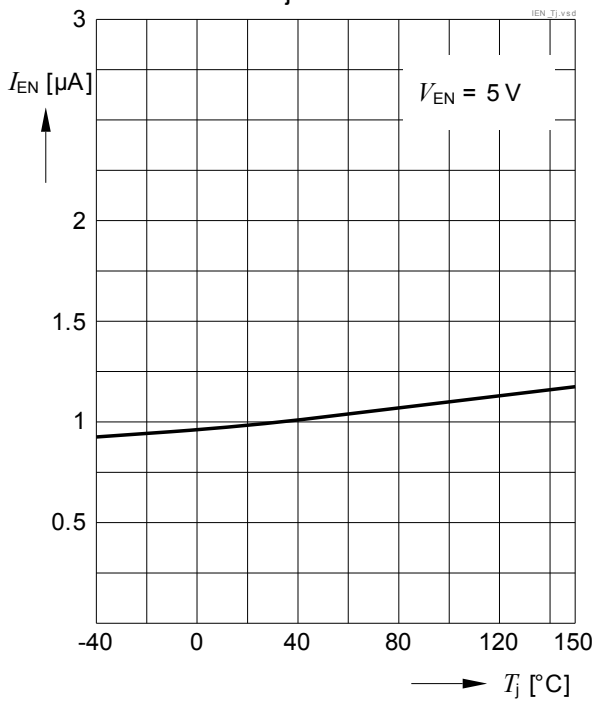

**Figure 6 Parameter Definition**

## 7.3 Typical Performance Characteristics Enable Input

**Enable Input Current $I_{EN}$ vs. Enable Input Voltage $V_{EN}$**




**Enable Input Current vs. Junction Temperature $T_j$**



# 8 Reset Function

## 8.1 Description Reset Function

The reset function contains several features:

**Output Undervoltage Reset:**

An output undervoltage condition is indicated by setting the reset output “RO” to “low”. This signal might be used to reset a microcontroller during a low supply voltage condition.

**Power-On Reset Delay Time**

The power-on reset delay time $t_{d,PWR\text{-}ON}$ allows a microcontroller and oscillator to start up. This delay time is the time period from exceeding the upper reset switching threshold $V_{RT,hi}$ until the reset is released by switching the reset output “RO” from “low” to “high”. The power-on reset delay time $t_{d,PWR\text{-}ON}$ is defined by an external delay capacitor $C_D$ connected to pin “D”, which is charged up by the delay capacitor charge current $I_{D,ch}$ starting from $V_D$ = 0 V.

In case a power-on reset delay time $t_{d,PWR\text{-}ON}$ different from the value for $C_D$ = 100nF is required, the delay capacitor’s value can be derived from the specified value given in **Item 8.2.15**:

$$C_D = \frac{t_{d,PWR\text{-}ON}}{t_{d,PWR\text{-}ON,100nF}} \times 100nF$$

with

- $t_{d,PWR\text{-}ON}$: Desired power-on reset delay time
- $t_{d,PWR\text{-}ON,100nF}$: Power-on reset delay time specified in **Item 8.2.15**
- $C_D$: Delay capacitor required

The formula is valid for $C_D \geq$ 10 nF.For a precise calculation consider also the delay capacitor’s tolerance.

**Undervoltage Reset Delay Time**

Unlike the power-on reset delay time, the undervoltage reset delay $t_d$ time considers a short output undervoltage event, where the delay capacitor $C_D$ is assumed to be discharged to $V_D = V_{DST,lo}$ only before the charging sequence starts. Therefore, the undervoltage reset delay time $t_d$ is defined by the delay capacitor charge current $I_{D,ch}$ starting from $V_D = V_{DST,lo}$ and the external delay capacitor $C_D$.

A delay capacitor $C_D$ for a different undervoltage reset delay time as specified in **Item 8.2.14** can be calculated similar as above:

$$C_D = \frac{t_d}{t_{d,100nF}} \times 100nF$$

with

- $t_d$: Desired reset delay time
- $t_{d,100nF}$: Reset delay time specified in **Item 8.2.14**
- $C_D$: Delay capacitor required

The formula is valid for $C_D \geq$ 10 nF.For a precise calculation consider also the delay capacitor’s tolerance.

### Reset Reaction Time

In case the output voltage of the regulator drops below the output undervoltage lower reset threshold $V_{RT,lo}$, the delay capacitor $C_D$ is discharged rapidly. Once the delay capacitor's voltage has reached the lower delay switching threshold $V_{DST,lo}$, the reset output RO will be set to "low".

Additionally to the delay capacitor discharge time $t_{rr,d}$ an internal time $t_{rr,int}$ applies. Hence the total reset reaction time $t_{rr,total}$ becomes:

$$t_{rr,total} = t_{rr,int} + t_{rr,d}$$

with

- $t_{rr,total}$: total reset reaction time
- $t_{rr,int}$: Internal reset reaction time; see **Item 8.2.16**
- $t_{rr,d}$: Delay capacitor discharge time. For a capacitor $C_D$ different from the value specified in **Item 8.2.17**, see typical performance graphs.

### Reset Output "RO"

The reset output "RO" is an open collector output with an integrated pull-up resistor. In case a lower-ohmic "RO" signal is desired, an external pull-up resistor to the output "Q" can be connected. Since the maximum "RO" sink current is limited, the optional external resistor $R_{RO,ext}$ must not below as specified in **Item 8.2.8**.

### Reset Output "RO" Low for $V_Q \geq 1$ V

In case of an undervoltage reset condition reset output "RO" is held "low" for $V_Q \geq 1$ V, even if the input voltage $V_I$ is 0 V. This is achieved by supplying the reset circuit from the output capacitor.

### Reset Adjust Function

The undervoltage reset switching threshold can be adjusted according to the application's needs by connecting an external voltage divider ($R_{ADJ1}$, $R_{ADJ2}$) at pin "RADJ". For selecting the default threshold connect pin "RADJ" to GND. The reset adjustment range is given in **Item 8.2.6**.

When dimensioning the voltage divider, take into consideration that there will be an additional current constantly flowing through the resistors.

With a voltage divider connected, the reset switching threshold $V_{RT,new}$ is calculated as follows

$$V_{RT,new} = V_{RADJ,th} \times \frac{R_{ADJ,1} + R_{ADJ,2}}{R_{ADJ,2}}$$

with

- $V_{RT,new}$: Desired reset switching threshold.
- $R_{ADJ,1}$, $R_{ADJ,2}$: Resistors of the external voltage divider, see **Figure 7**.
- $V_{RADJ,th}$: Reset adjust switching threshold given in **Item 8.2.5**.

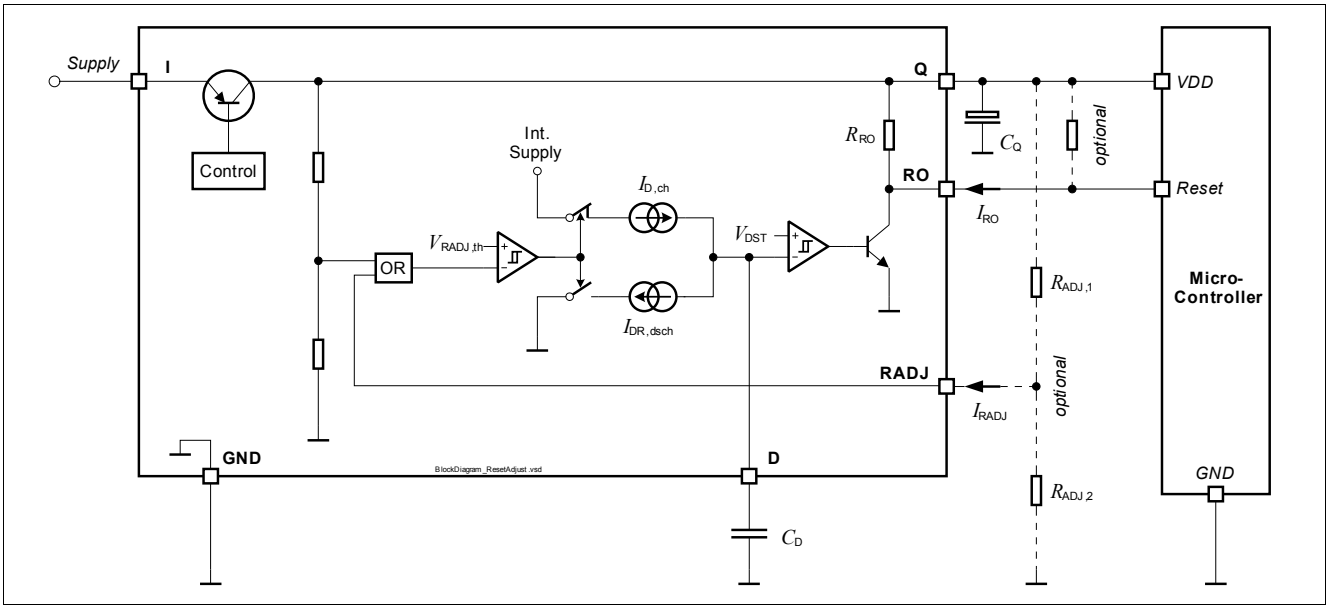



**Figure 7 Block Diagram Reset Circuit**

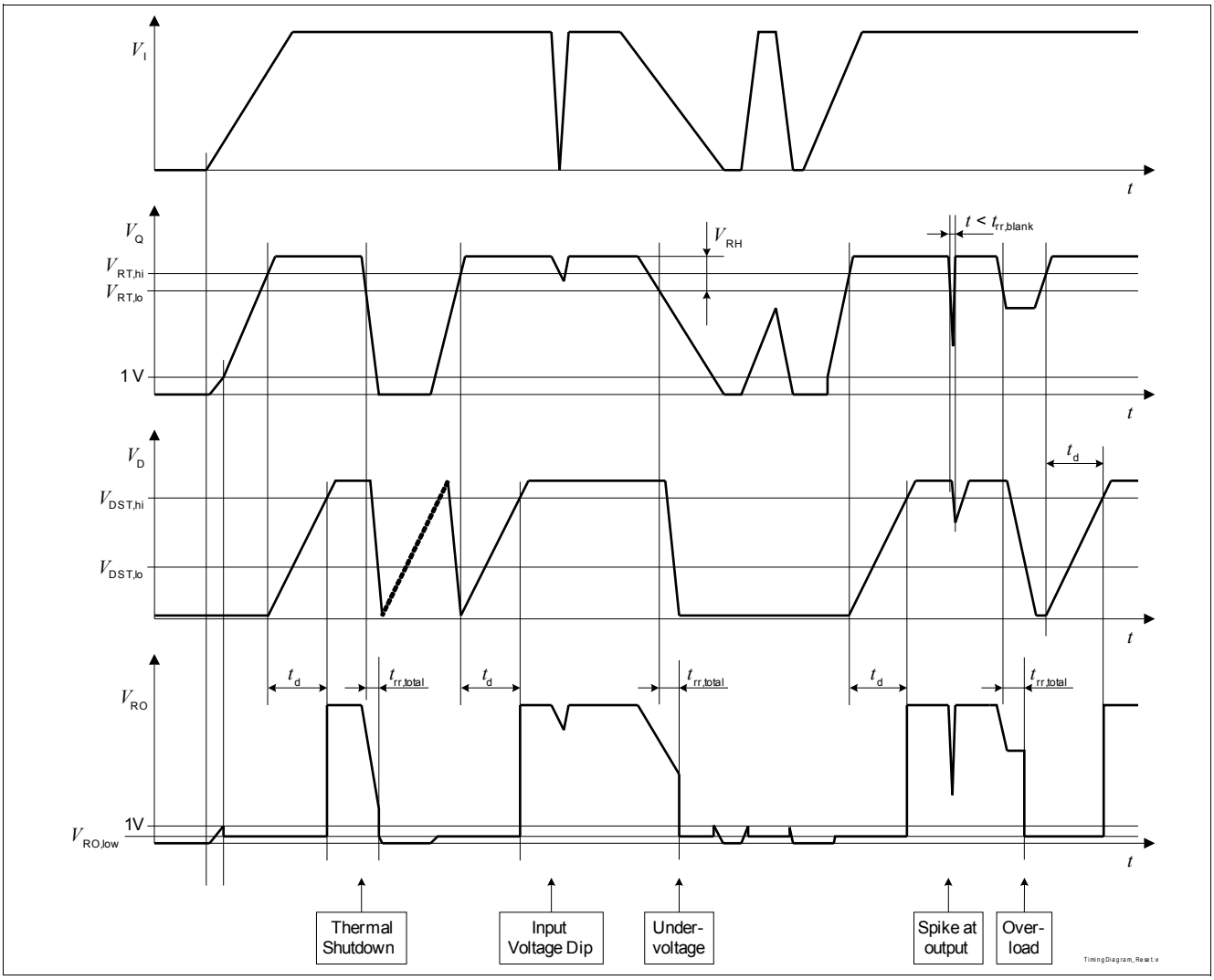



**Figure 8 Timing Diagram Reset**

## 8.2 Electrical Characteristics Reset Function

**Electrical Characteristics: Reset Function**

$V_I$ = 13.5 V, $T_j$ = -40 °C to +150 °C,
all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified).

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| **Output Undervoltage Reset Comparator Default Values (Pin RADJ = GND)** | | | | | | | |
| 8.2.1 | Output Undervoltage Reset Lower Switching Threshold | $V_{RT,lo}$ | 4.6 | 4.7 | 4.8 | V | $V_I$ = 0 V<br>$V_Q$ decreasing<br>RADJ = GND |
| 8.2.2 | Output Undervoltage Reset Upper Switching Threshold | $V_{RT,hi}$ | 4.7 | 4.8 | 4.9 | V | $V_I$ within operating range<br>$V_Q$ increasing<br>RADJ = GND |
| 8.2.3 | Output Undervoltage Reset Switching Hysteresis | $V_{RT,hy}$ | 60 | 120 | – | mV | $V_I$ within operating range<br>RADJ = GND. |
| 8.2.4 | Output Undervoltage Reset Headroom | $V_{RH}$ | 250 | 300 | – | mV | Calculated Value:<br>$V_Q$ - $V_{RT,lo}$<br>$V_I$ within operating range<br>$I_Q$ = 50 mA<br>RADJ = GND |
| **Reset Threshold Adjustment** | | | | | | | |
| 8.2.5 | Reset Adjust Lower Switching Threshold | $V_{RADJ,th}$ | 1.17 | 1.195 | 1.22 | V | $V_I$ = 0 V<br>3.2 V ≤ $V_Q$ < 5 V |
| 8.2.6 | Reset Adjustment Range [1] | $V_{RT,range}$ | 3.20 | – | 4.70 | V | – |
| **Reset Output RO** | | | | | | | |
| 8.2.7 | Reset Output Low Voltage | $V_{RO,low}$ | – | 0.2 | 0.4 | V | $V_I$ = 0 V;<br>1 V ≤ $V_Q$ ≤ $V_{RT,low}$<br>$R_{RO,ext}$ = 3.3 kΩ |
| 8.2.8 | Reset Output External Pull-up Resistor to Q | $R_{RO,ext}$ | 3 | – | – | kΩ | $V_I$ = 0 V;<br>1 V ≤ $V_Q$ ≤ $V_{RT,low}$<br>$V_{RO}$ = 0.4 V |
| 8.2.9 | Reset Output Internal Pull-up Resistor | $R_{RO}$ | 20 | 30 | 40 | kΩ | internally connected to Q |
| **Reset Delay Timing** | | | | | | | |
| 8.2.10 | Upper Delay Switching Threshold | $V_{DST,hi}$ | – | 1.21 | – | V | – |
| 8.2.11 | Lower Delay Switching Threshold | $V_{DST,lo}$ | – | 0.30 | – | V | – |
| 8.2.12 | Delay Capacitor Charge Current | $I_{D,ch}$ | – | 3.5 | – | µA | $V_D$ = 1 V |
| 8.2.13 | Delay Capacitor Reset Discharge Current | $I_{DR,dsch}$ | – | 80 | – | mA | $V_D$ = 1 V |
| 8.2.14 | Undervoltage Reset Delay Time | $t_{d,100nF}$ | 16 | 23 | 30 | ms | Calculated value;<br>$C_D$ = 100 nF [2];<br>$C_D$ discharged to $V_{DST,lo}$ |

**Electrical Characteristics: Reset Function** (cont'd)

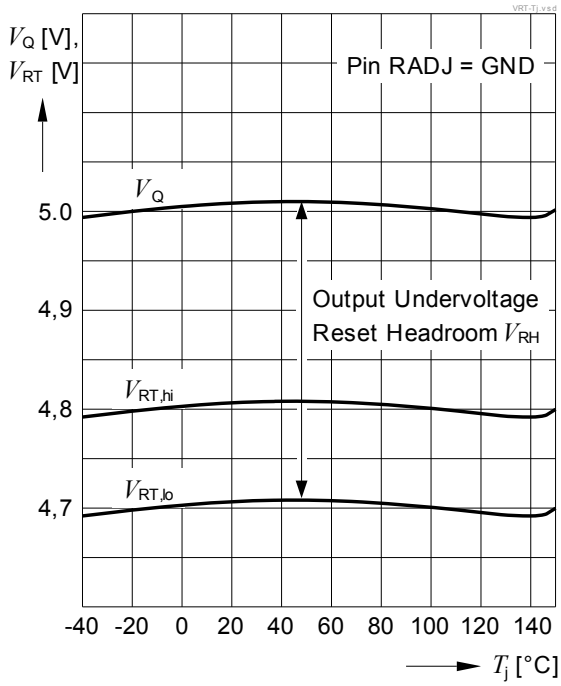
$V_I$ = 13.5 V, $T_j$ = -40 °C to +150 °C,
all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified).

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| 8.2.15 | Power-on Reset Delay Time | $t_{d,PWR-ON,100nF}$ | 20 | 31 | 40 | ms | Calculated value; $C_D$ = 100 nF 2); $C_D$ discharged to 0 V |
| 8.2.16 | Internal Reset Reaction Time | $t_{rr,int}$ | – | 9 | 15 | µs | $C_D$ = 0 nF |
| 8.2.17 | Delay Capacitor Discharge Time | $t_{rr,d,100nF}$ | – | 1.5 | 3 | µs | $C_D$ = 100 nF 2) |
| 8.2.18 | Total Reset Reaction Time | $t_{rr,total,100nF}$ | – | 10.5 | 18 | µs | Calculated Value: $t_{rr,d,100nF}$ + $t_{rr,int}$; $C_D$ = 100 nF 2) |

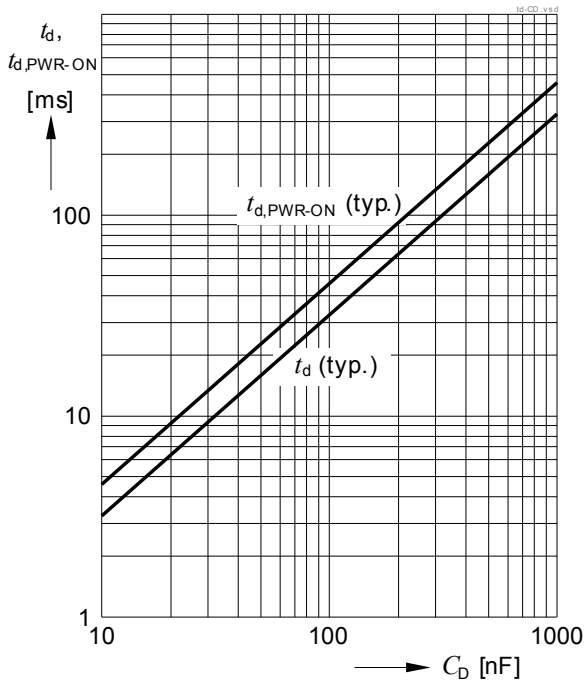
1) Related Parameters ($V_{RT,hi}$, $V_{RT,hy}$) are scaled linear when the Reset Switching Threshold is modified.
2) For programming a different delay and reset reaction time, see **Chapter 8.1**.

## 8.3 Typical Performance Characteristics Reset Function

**Undervoltage Reset Switching Thresholds $V_{RT,lo}$, $V_{RT,hi}$ vs. $T_j$**




**Reset Delay Time $t_d$, $t_{d,PWR-ON}$ vs. Delay Capacitor $C_D$**



# 9 Early Warning Function

## 9.1 Description Early Warning Function

The additional sense comparator provides an early warning function: Any voltage (e.g. the input voltage) can be monitored, an undervoltage condition is indicated by setting the comparator's output to low. The use of an external voltage divider makes this comparator very flexible in the application.

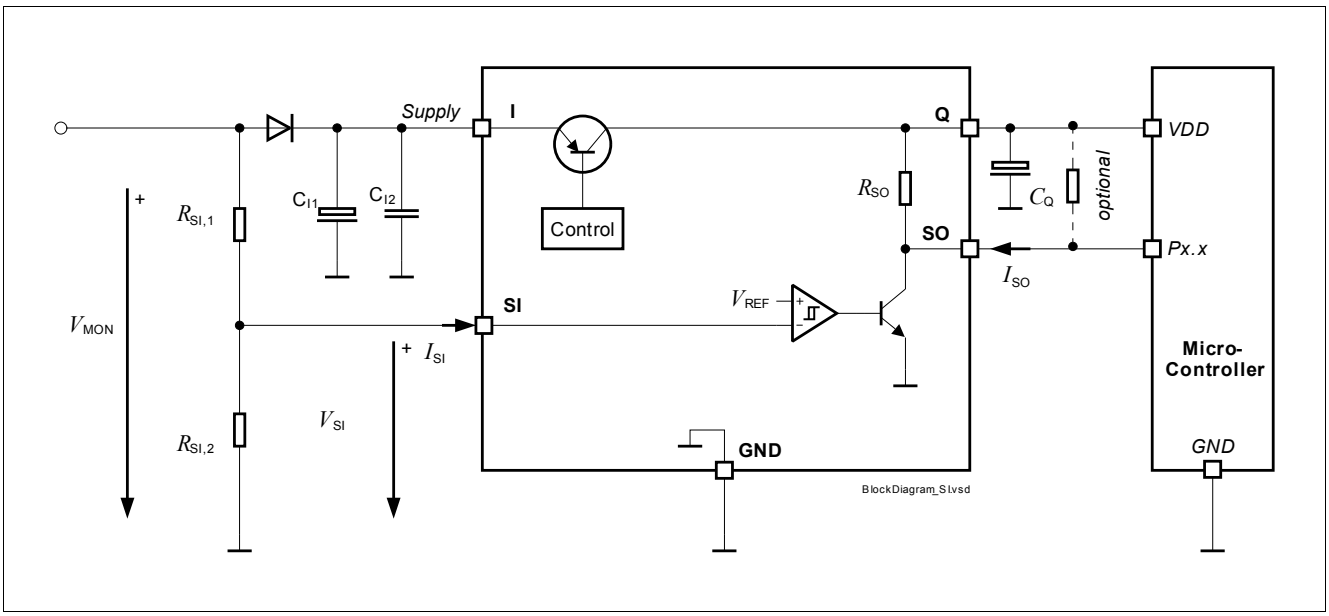



**Figure 9 Diagram**

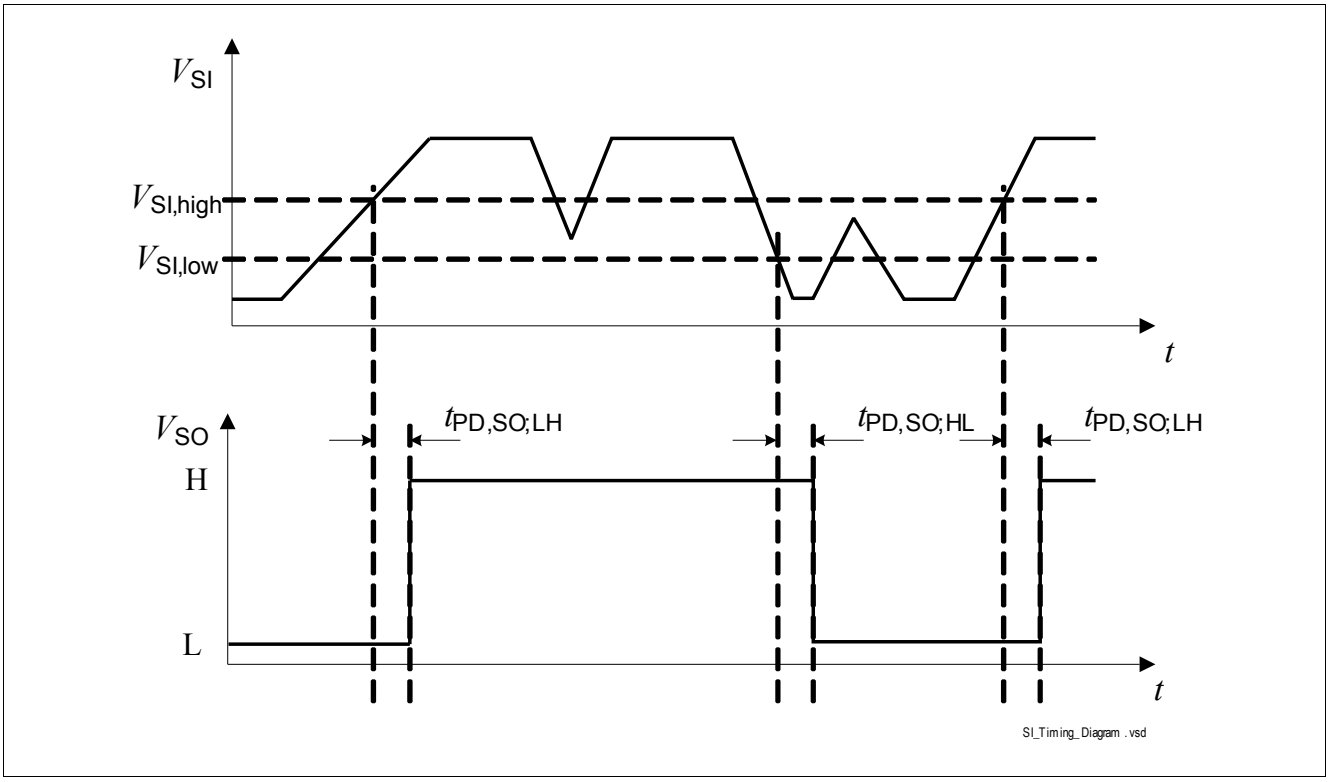



**Figure 10 Timing Diagram**

### Early Warning Resistor Divider Adjust

The switching threshold can be set to the application's needs by connecting an external voltage divider ($R_{SI,1}$, $R_{SI,2}$) at pin "SI". If the Early Warning function is not needed, it is recommend to connect the SI pin to the output voltage pin Q.

When dimensioning the voltage divider, take into consideration that there will be an additional current constantly flowing through the resistors.

With a voltage divider connected, the upper switching threshold for the monitored voltage $V_{MON,high}$ is calculated as follows

$$V_{MON,high} = V_{SI,high} \times \frac{R_{SI,1} + R_{SI,2}}{R_{SI,2}}$$

with

- $V_{MON,high}$: Desired reset switching threshold.
- $R_{SI,1}$, $R_{SI,2}$: Resistors of the external voltage divider, see **Figure 9**.
- $V_{SI,high}$: Sense threshold high given in **Item 9.2.1**.The lower switching threshold for the monitored voltage $V_{MON,low}$ is calculated as follows

$$V_{MON,low} = V_{SI,low} \times \frac{R_{SI,1} + R_{SI,2}}{R_{SI,2}}$$

with

- $V_{mon,high}$: Desired reset switching threshold.
- $R_{SI,1}$, $R_{SI,2}$: Resistors of the external voltage divider, see **Figure 9**.
- $V_{SI,high}$: Reset adjust switching threshold given in **Item 9.2.2**.

### Sense Output "SO"

The sense output "SO" is an open collector output with an integrated pull-up resistor. In case a lower-ohmic "SO" signal is desired, an external pull-up resistor to the output "Q" can be connected.

## 9.2 Electrical Characteristics Early Warning Function

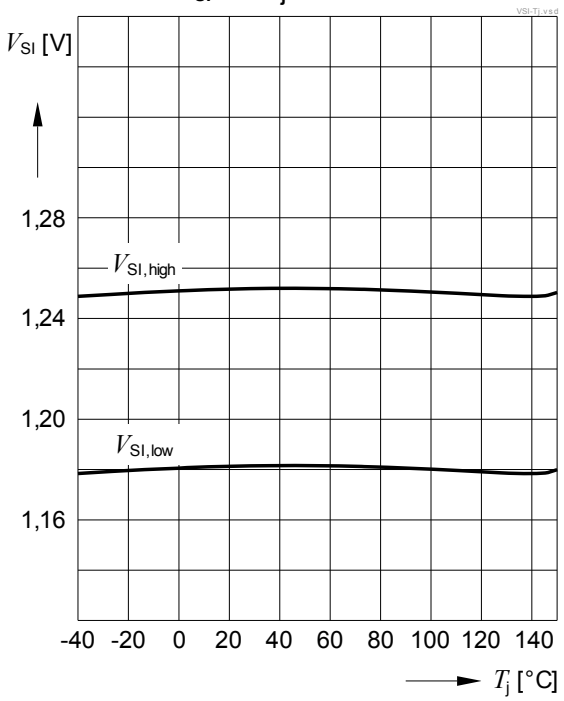
**Electrical Characteristics: Early Warning Function**

$V_I$ = 13.5 V, $T_j$ = -40 °C to +150 °C, all voltages with respect to ground, direction of currents as shown in **Figure 9** (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| **Sense Comparator Input** | | | | | | | |
| 9.2.1 | Sense threshold high | $V_{SI,high}$ | 1.22 | 1.25 | 1.28 | V | – |
| 9.2.2 | Sense threshold low | $V_{SI,low}$ | 1.16 | 1.185 | 1.21 | V | – |
| 9.2.3 | Sense input switching hysteresis | $V_{SI,hy}$ | – | 65 | – | mV | – |
| 9.2.4 | Sense input current | $I_{SI}$ | -1 | 0.1 | 1 | µA | – |
| **Sense Comparator Output** | | | | | | | |
| 9.2.5 | Sense output low voltage | $V_{SO,low}$ | – | 0.2 | 0.4 | V | – |
| 9.2.6 | Maximum sink current capability | $I_{SO,max}$ | 1.5 | – | – | mA | – |
| 9.2.7 | Internal sense pull up resistor | $R_{SO}$ | 10 | 20 | 40 | kΩ | – |
| 9.2.8 | Sense high reaction time | $t_{PD,SO,HL}$ | – | 5 | 10 | µs | – |
| 9.2.9 | Sense low reaction time | $t_{PD,SO,LH}$ | – | 5 | 10 | µs | – |

## 9.3 Typical Performance Characteristics Early Warning Function

**Sense threshold $V_{SI}$ vs. $T_j$**



# 10 Package Outlines

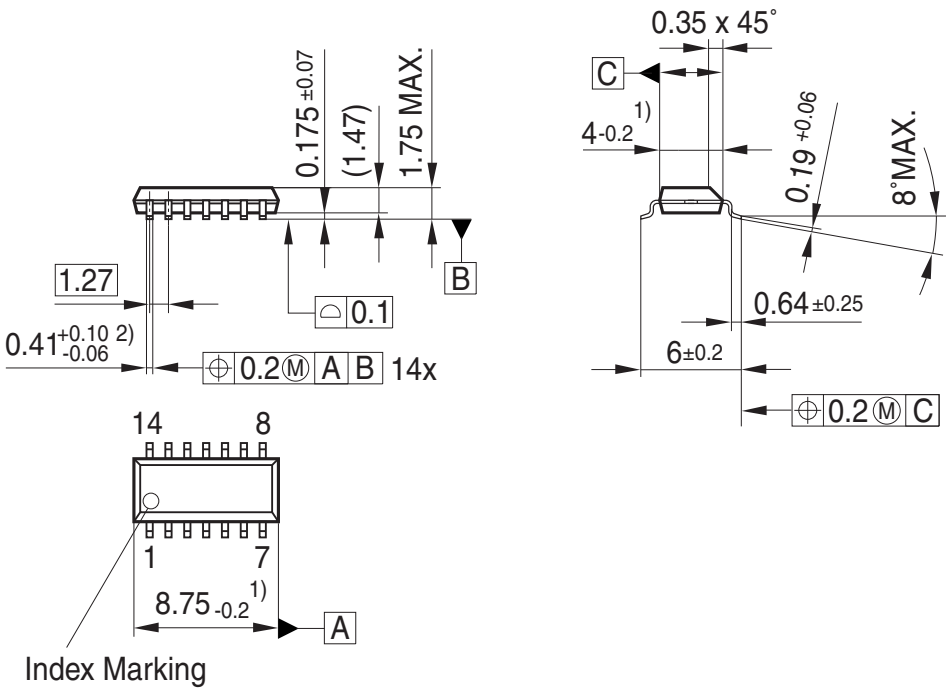



**Figure 11 Outline PG-DSO-14**

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

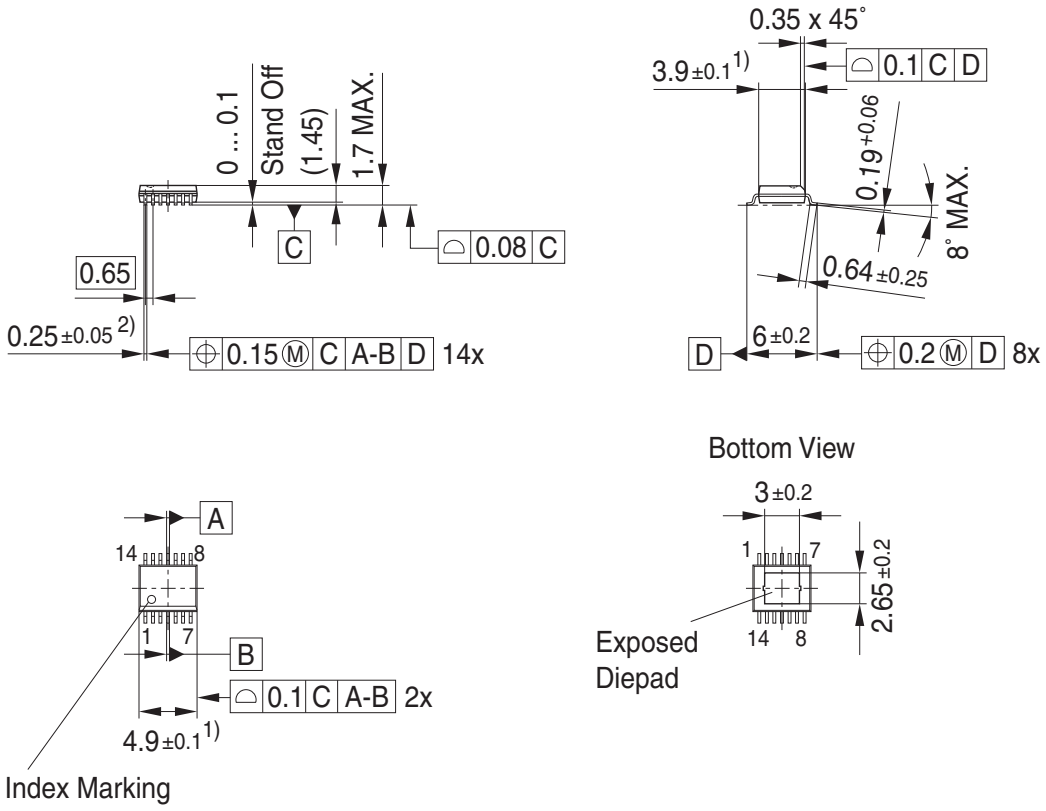



**Figure 12 Outline PG-SSOP-14 EP**

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on packages, please visit our website:
**http://www.infineon.com/packages**.

Dimensions in mm

# 11 Revision History

| Revision | Date | Changes |
|---|---|---|
| 1.0 | 2010-11-30 | Data sheet |

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