LM2642 Two-Phase Synchronous Step-Down Switching Controller

Check for Samples: LM2642

FEATURES

- **Two Synchronous Buck Regulators**
- **180° Out of Phase Operation**
- **4.5V to 30V Input Range**
- **Power Good Function Monitors Ch.1**
- **37µA Shutdown Current**
- **0.04% (typical) Line and Load Regulation Error**
- **Current Mode Control With or Without a Sense Resistor**
- **Independent Enable/Soft-start Pins Allow Simple Sequential Startup Configuration.**
- **Configurable for Single Output Parallel Operation. (See Figure 3).**
- **Adjustable Cycle-by-Cycle Current Limit**
- **Input Under-voltage Lockout**
- **Output Over-voltage Latch Protection**
- **Output Under-voltage Protection with Delay**
- **Thermal Shutdown**
- **Self Discharge of Output Capacitors When the Regulator is OFF**
- **TSSOP package**

APPLICATIONS

- **Embedded Computer Systems**
- **High End Gaming Systems**
- **Set-top Boxes**
- **WebPAD**

DESCRIPTION

The LM2642 consists of two current mode synchronous buck regulator controllers with a switching frequency of 300kHz.

The two switching regulator controllers operate 180° out of phase. This feature reduces the input ripple RMS current, thereby significantly reducing the required input capacitance. The two switching regulator outputs can also be paralleled to operate as a dual-phase single output regulator.

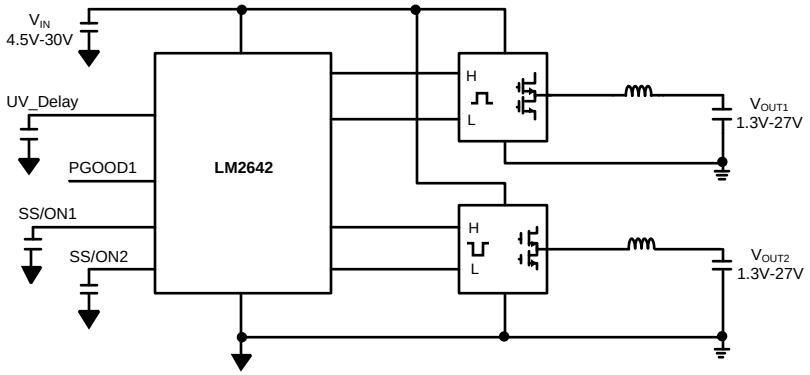
The output of each channel can be independently adjusted from 1.3 to V_{IN}• maximum duty cycle. An internal 5V rail is also available externally for driving bootstrap circuitry.

Current-mode feedback control assures excellent line and load regulation and a wide loop bandwidth for excellent response to fast load transients. Current is sensed across either the Vds of the top FET or across an external current-sense resistor connected in series with the drain of the top FET. Current limit is independently adjustable for each channel.

The LM2642 features analog soft-start circuitry that is independent of the output load and output capacitance. This makes the soft-start behavior more predictable and controllable than traditional soft-start circuits.

A PGOOD1 pin is provided to monitor the dc output of channel 1. Over-voltage protection is available for both outputs. A UV-Delay pin is also available to allow delayed shut off time for the IC during an output under-voltage event.

BLOCK DIAGRAM



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CONNECTION DIAGRAM

TOP VIEW

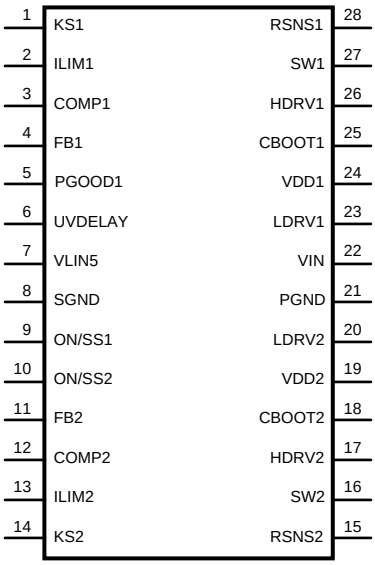


Figure 1. 28-Lead TSSOP

PIN DESCRIPTIONS

KS1 (Pin 1) The positive (+) Kelvin sense for the internal current sense amplifier of Channel 1. Use a separate trace to connect this pin to the current sense point. It should be connected to VIN as close as possible to the node of the current sense resistor. When no current-sense resistor is used, connect as close as possible to the drain node of the upper MOSFET.

ILIM1 (Pin 2) Current limit threshold setting for Channel 1. It sinks a constant current of 10 µA, which is converted to a voltage across a resistor connected from this pin to VIN. The voltage across the resistor is compared with either the VDS of the top MOSFET or the voltage across the external current sense resistor to determine if an over-current condition has occurred in Channel 1.

COMP1 (Pin 3) Compensation pin for Channel 1. This is the output of the internal transconductance amplifier. The compensation network should be connected between this pin and the signal ground, SGND (Pin 8).

FB1 (Pin 4) Feedback input for channel 1. Connect to VOUT through a voltage divider to set the channel 1 output voltage.

PGOOD1 (Pin 5) An open-drain power-good output for Channel 1. It is 'LOW' (low impedance to ground) whenever the output voltage of Channel 1 falls outside of a +15% to -9% window. PGOOD1 stays latched in a 'LOW' state during OVP or UVP on either channel. It will recover to a 'HIGH' state (high impedance to ground) after a Channel 1 output under-voltage event (<91%) when the output returns to within 6% of its nominal value. See Operation Descriptions for details.

UV_DELAY (Pin 6) A capacitor from this pin to ground sets the delay time for UVP. The capacitor is charged from a 5µA current source. When UV_DELAY charges to 2.3V (typical), the system immediately latches off. Connecting this pin to ground will disable the output under-voltage protection.

VLIN5 (Pin 7) The output of an internal 5V LDO regulator derived from VIN. It supplies the internal bias for the chip and supplies the bootstrap circuitry for gate drive. Bypass this pin to signal ground with a minimum of 4.7µF capacitor.

SGND (Pin 8) The ground connection for the signal-level circuitry. It should be connected to the ground rail of the

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system.

ON/SS1 (Pin 9) Channel 1 enable pin. This pin is internally pulled up to one diode drop above VLIN5. Pulling this pin below 1.2V (open-collector type) turns off Channel 1. If both ON/SS1 and ON/SS2 pins are pulled below 1.2V, the whole chip goes into *shut down mode*. Adding a capacitor to this pin provides a soft-start feature that minimizes inrush current and output voltage overshoot.

ON/SS2 (Pin 10) Channel 2 enable pin. See the description for Pin 9, ON/SS1. May be connected to ON/SS1 for simultaneous startup or for parallel operation.

FB2 (Pin 11) Feedback input for channel 2. Connect to VOUT through a voltage divider to set the Channel 2 output voltage.

COMP2 (Pin 12) Compensation pin for Channel 2. This is the output of the internal transconductance amplifier. The compensation network should be connected between this pin and the signal ground SGND (Pin 8).

ILIM2 (Pin 13) Current limit threshold setting for Channel 2. See ILIM1 (Pin 2).

KS2 (Pin 14) The positive (+) Kelvin sense for the internal current sense amplifier of Channel 2. See KS1 (Pin 1).

RSNS2 (Pin 15) The negative (-) Kelvin sense for the internal current sense amplifier of Channel 2. Connect this pin to the low side of the current sense resistor that is placed between VIN and the drain of the top MOSFET. When the Rds of the top MOSFET is used for current sensing, connect this pin to the source of the top MOSFET. Always use a separate trace to form a Kelvin connection to this pin.

SW2 (Pin 16) Switch-node connection for Channel 2, which is connected to the source of the top MOSFET of Channel 2. It serves as the negative supply rail for the top-side gate driver, HDRV2.

HDRV2 (Pin 17) Top-side gate-drive output for Channel 2. HDRV is a floating drive output that rides on the corresponding switching-node voltage.

CBOOT2 (Pin 18) Bootstrap capacitor connection. It serves as the positive supply rail for the Channel 2 top-side gate drive. Connect this pin to VDD2 (Pin 19) through a diode, and connect the low side of the bootstrap capacitor to SW2 (Pin16).

VDD2 (Pin 19) The supply rail for the Channel 2 low-side gate drive. Connected to VLIN5 (Pin 7) through a 4.7Ω resistor and bypassed to power ground with a ceramic capacitor of at least 1µF. Tie this pin to VDD1 (Pin 24).

LDRV2 (Pin 20) Low-side gate-drive output for Channel 2.

PGND (Pin 21) The power ground connection for both channels. Connect to the ground rail of the system.

VIN (Pin 22) The power input pin for the chip. Connect to the positive (+) input rail of the system. This pin must be connected to the same voltage rail as the top FET drain (or the current sense resistor when used).

LDRV1 (Pin 23) Low-side gate-drive output for Channel 1.

VDD1 (Pin 24) The supply rail for Channel 1 low-side gate drive. Tie this pin to VDD2 (Pin 19).

CBOOT1 (Pin 25) Bootstrap capacitor connection. It serves as the positive supply rail for Channel 1 top-side gate drive. See CBOOT2 (Pin 18).

HDRV1 (Pin 26) Top-side gate-drive output for Channel 1. See HDRV2 (Pin 17).

SW1 (Pin 27) Switch-node connection for Channel 1. See SW2 (Pin16).

RSNS1 (Pin 28) The negative (-) Kelvin sense for the internal current sense amplifier of Channel 1. See RSNS2 (Pin 15).

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ABSOLUTE MAXIMUM RATINGS (1)

Voltages from the indicated pins to SGND/PGND:	
VIN, ILIM1, ILIM2, KS1, KS2	−0.3V to 32V
SW1, SW2, RSNS1, RSNS2	−0.3 to (V_{IN} + 0.3)V
FB1, FB2, VDD1, VDD2	−0.3V to 6V
PGOOD, COMP1, COMP2, UV Delay	−0.3V to (VLIN5 +0.3)V
ON/SS1, ON/SS2 (2)	−0.3V to (VLIN5 +0.6)V
CBOOT1 to SW1, CBOOT2 to SW2	−0.3V to 7V
LDRV1, LDRV2	−0.3V to (VDD+0.3)V
HDRV1 to SW1, HDRV2 to SW2	−0.3V
HDRV1 to CBOOT1, HDRV2 to CBOOT2	+0.3V
Power Dissipation (T_A = 25°C), (3)	1.1W
Ambient Storage Temperature Range	−65°C to +150°C
Soldering Dwell Time, Temperature (4) Wave Infrared Vapor Phase	 4 sec, 260°C 10sec, 240°C 75sec, 219°C
ESD Rating (5)	2kV

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Range indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) ON/SS1 and ON/SS2 are internally pulled up to one diode drop above VLIN5. Do not apply an external pull-up voltage to these pins. It may cause damage to the IC.

(3) The maximum allowable power dissipation is calculated by using $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$, where T_{JMAX} is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of the specified package. The 1.1W rating results from using 125°C, 25°C, and 90.6°C/W for T_{JMAX}, T_A, and θ_{JA} respectively. A θ_{JA} of 90.6°C/W represents the worst-case condition of no heat sinking of the 28-pin TSSOP. A thermal shutdown will occur if the temperature exceeds the maximum junction temperature of the device.

(4) For detailed information on soldering plastic small-outline packages, see the TI website at www.ti.com/packaging.

(5) For testing purposes, ESD was applied using the human-body model, a 100pF capacitor discharged through a 1.5kΩ resistor.

OPERATING RATINGS (1)

VIN (VLIN5 tied to VIN)	4.5V to 5.5V
VIN (VIN and VLIN5 separate)	5.5V to 30V
Junction Temperature	−40°C to +125°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Range indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, GND = PGND = 0V, VLIN5 = VDD1 = VDD2. Limits appearing in **boldface** type apply over the specified operating junction temperature range, (-20°C to +125°C, if not otherwise specified). Specifications appearing in plain type are measured using low duty cycle pulse testing with T_A = 25°C (1), (2). Min/Max limits are specified by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
System						
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	VIN = 15V, V_{compx} = 0.5V to 1.5V		0.04		%
$\Delta V_{OUT}/V_{OUT}$	Line Regulation	5.5V ≤ VIN ≤ 30V, V_{compx} =1.25V		0.04		%
V_{FB1_FI2}	Feedback Voltage	5.5V ≤ VIN ≤ 30V	**1.215**	1.238	**1.260**	V
		0°C to 125°C	**1.217**		**1.259**	
		-40°C to 125°C	**1.212**		**1.261**	
I_{VIN}	Input Supply Current	V_{ON_SSx} > 2V 5.5V ≤ VIN ≤ 30V		1.0	**2.0**	mA
		Shutdown (3) V_{ON_SS1} = V_{ON_SS2}= 0V		37	**110**	µA
VLIN5	VLIN5 Output Voltage (4)	IVLIN5 = 0 to 25mA, 5.5V ≤ VIN ≤ 30V	**4.70**	5	**5.30**	V
		-40°C to 125°C	**4.68**		**5.30**	
V_{CLos}	Current Limit Comparator Offset (VILIMX −VRSNSX)			±2	±7.0	mV
I_{CL}	Current Limit Sink Current		**9**	10	**11**	µA
		-40°C to 125°C	**8.67**		**11**	
I_{ss_SC1}, I_{ss_SC2}	Soft-Start Source Current	V_{ON_ss1} = V_{ON_ss2} = 1.5V (on)	**0.5**	2	**5.0**	µA
I_{ss_SK1}, I_{ss_SK2}	Soft-Start Sink Current	V_{ON_ss1} = V_{ON_ss2} = 2V	**2**	5.2	**10**	µA
V_{ON_SS1}, V_{ON_SS2}	Soft-Start On Threshold		**0.7**	1.12	**1.4**	V
V_{SSTO}	Soft-Start Timeout Threshold	(5)		3.3		V
$I_{sc_uvdelay}$	UV_DELAY Source Current	UV-DELAY = 2V	**2**	5	**9**	µA
$I_{sk_uvdelay}$	UV_DELAY Sink Current	UV-DELAY = 0.4V	**0.2**	0.48	**1.2**	mA
$V_{UVDelay}$	UV_DELAY Threshold Voltage			2.3		V
V_{UVP}	FB1, FB2, Under Voltage Protection Latch Threshold	As a percentage of nominal output voltage (falling edge)	**75**	80	**86**	%
	Hysteresis			4		%
V_{OVP}	V_{OUT} Overvoltage Shutdown Latch Threshold	As a percentage measured at V_{FB1}, V_{FB2}	**107**	113	**122**	%
V_{pwrbad}	Regulator Window Detector Thresholds (PGOOD1 from High to Low)	As a percentage of output voltage	**86.5**	90.3	**94.5**	%
V_{pwrgd}	Regulator Window Detector Thresholds (PGOOD1 from Low to High)		**91.5**	94	**97.0**	%
S_{wx_R}	SW1, SW2 ON-Resistance	V_{SW1} = V_{SW2} = 2V	420	480	535	Ω
Gate Drive						
I_{CBOOT}	CBOOTx Leakage Current	V_{CBOOT1} = V_{CBOOT2} = 7V		10		nA

(1) A typical is the center of characterization data measured with low duty cycle pulse tsting at T_A = 25°C. Typicals are not ensured.
(2) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with T_A = T_J = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) Both switching controllers are off. The linear regulator VLIN5 remains on.
(4) The output voltage at the VLIN5 pin may be as high as 5.9V in shutdown mode (ON/SS1 = ON/SS2 = 0V).
(5) When SS1 and SS2 pins are charged above this voltage and either of the output voltages at Vout1 or Vout2 is still below the regulation limit, the under voltage protection feature is initialized.

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ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, V_{IN} = 15V, GND = PGND = 0V, VLIN5 = VDD1 = VDD2. Limits appearing in **boldface** type apply over the specified operating junction temperature range, (-20°C to +125°C, if not otherwise specified). Specifications appearing in plain type are measured using low duty cycle pulse testing with T_A = 25°C (1), (2). Min/Max limits are specified by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{SC_DRV}	HDRVx and LDRVx Source Current	V_{CBOOT1} = V_{CBOOT2} = 5V, VSWx=0V, HDRVx=LDRVx=2.5V		0.5		A
I_{sk_HDRV}	HDRVx Sink Current	V_{CBOOTx} = VDDx = 5V, V_{SWx} = 0V, HDRVX = 2.5V		0.8		A
I_{sk_LDRV}	LDRVx Sink Current	V_{CBOOTx} = VDDx = 5V, V_{SWx} = 0V, LDRVX = 2.5V		1.1		A
R_{HDRV}	HDRV1 & 2 Source On-Resistance	V_{CBOOT1} = V_{CBOOT2} = 5V, V_{SW1} = V_{SW2} = 0V		3.1		Ω
	HDRV1 & 2 Sink On-Resistance			1.5		Ω
R_{LDRV}	LDRV1 & 2 Source On-Resistance	V_{CBOOT1} = V_{CBOOT2} = 5V, V_{SW1} = V_{SW2} = 0V V_{DD1} = V_{DD1} = 5V		3.1		Ω
	LDRV1 & 2 Sink On-Resistance			1.1		Ω
Oscillator						
F_{osc}	Oscillator Frequency		**260**	300	**340**	kHz
		-40°C to 125°C	**257.5**		**340**	
Don_max	Maximum On-Duty Cycle	V_{FB1} = V_{FB2} = 1V, Measured at pins HDRV1 and HDRV2	**96**	98		%
		-40°C to 125°C	**95.64**			
T_{on_min}	Minimum On-Time			166		ns
SS_{OT_delta}	HDRV1 and HDRV2 Delta On Time	ON/SS1 = ON/SS2 = 2V		20	150	ns
Error Amplifier						
I_{FB1}, I_{FB2}	Feedback Input Bias Current	V_{FB1_FIX} = 1.5V, V_{FB2_FIX} = 1.5V		65	**±200**	nA
I_{comp1_SC}, I_{comp2_SC}	COMP Output Source Current	V_{FB1_FIX} = V_{FB2_FIX} = 1V, V_{COMP1} = V_{COMP2} = 1V	**18**	113		µA
		0°C to 125°C	**32**			
		-40°C to 125°C	**6**			
I_{comp1_SK}, I_{comp2_SK}	COMP Output Sink Current	V_{FB1_FIX} = V_{FB2_FIX} = 1.5V and V_{COMP1} = V_{COMP2} = 0.5V	**18**	108		µA
		0°C to 125°C	**32**			
		-40°C to 125°C	**6**			
gm1, gm2	Transconductance			650		µmho
GI_{SNS1}, GI_{SNS2}	Current Sense Amplifier (1&2) Gain	V_{COMPx} = 1.25V	4.2	5.2	7.5	
Voltage References and Linear Voltage Regulators						
UVLO	VLIN5 Under-voltage Lockout Threshold Rising	ON/SS1, ON/SS2 transition from low to high	**3.6**	4.0	**4.4**	V
Logic Outputs						
I_{OL}	PGOOD Low Sink Current	V_{PGOOD} = 0.4V	**0.60**	0.95		mA
I_{OH}	PGOOD High Leakage Current	V_{PGOOD} = 5V		5	**200**	nA

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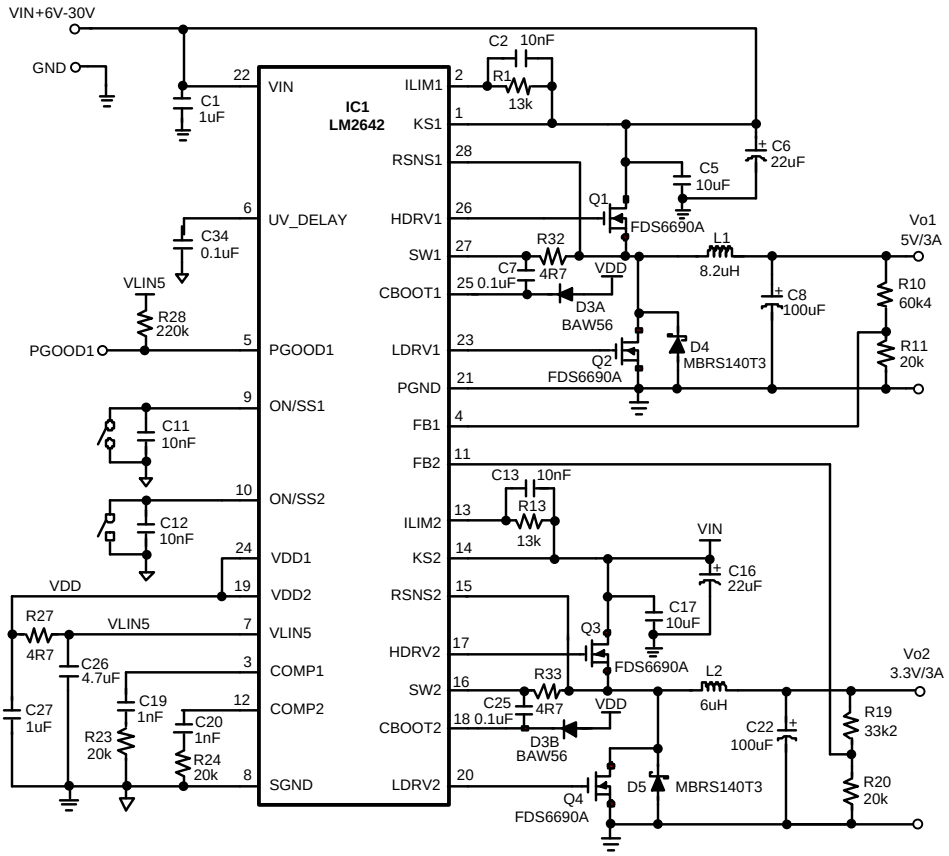


Figure 2. Typical 2 Channel Application Circuit

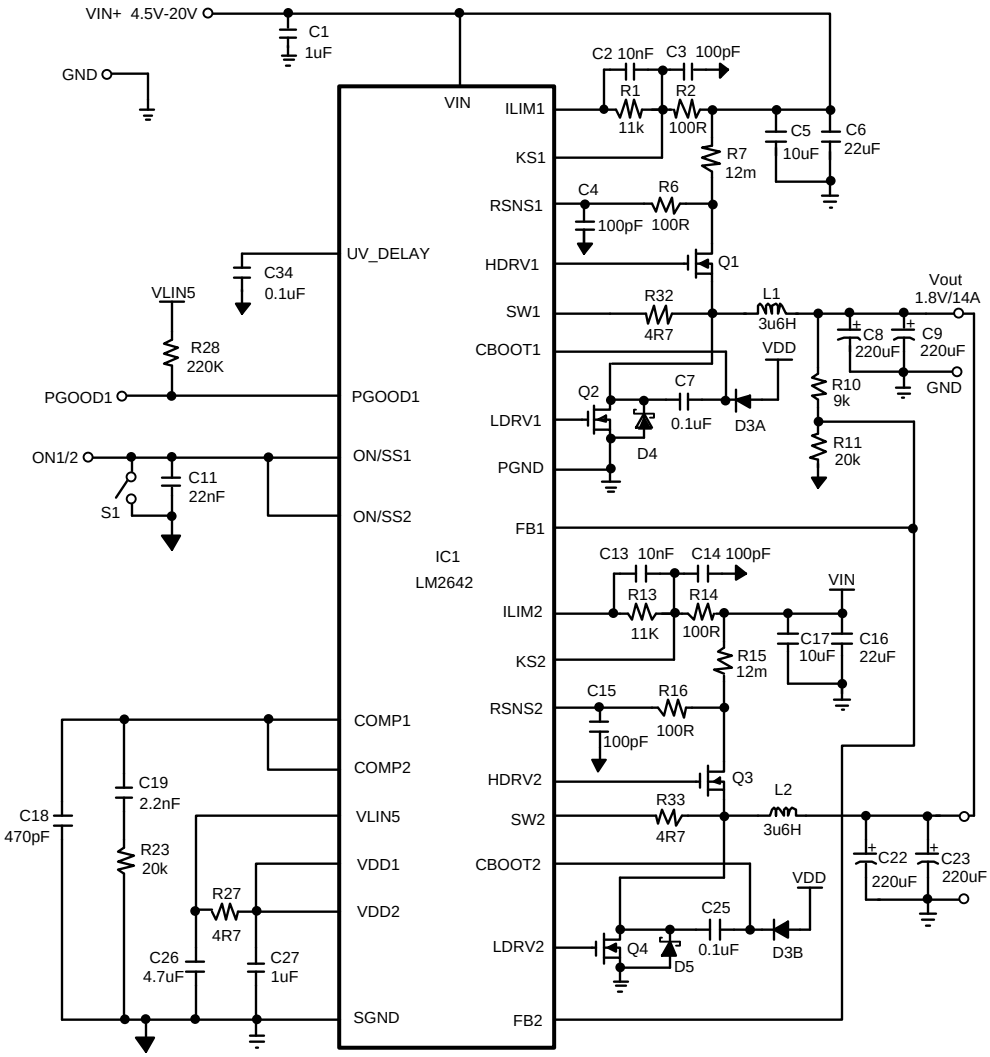
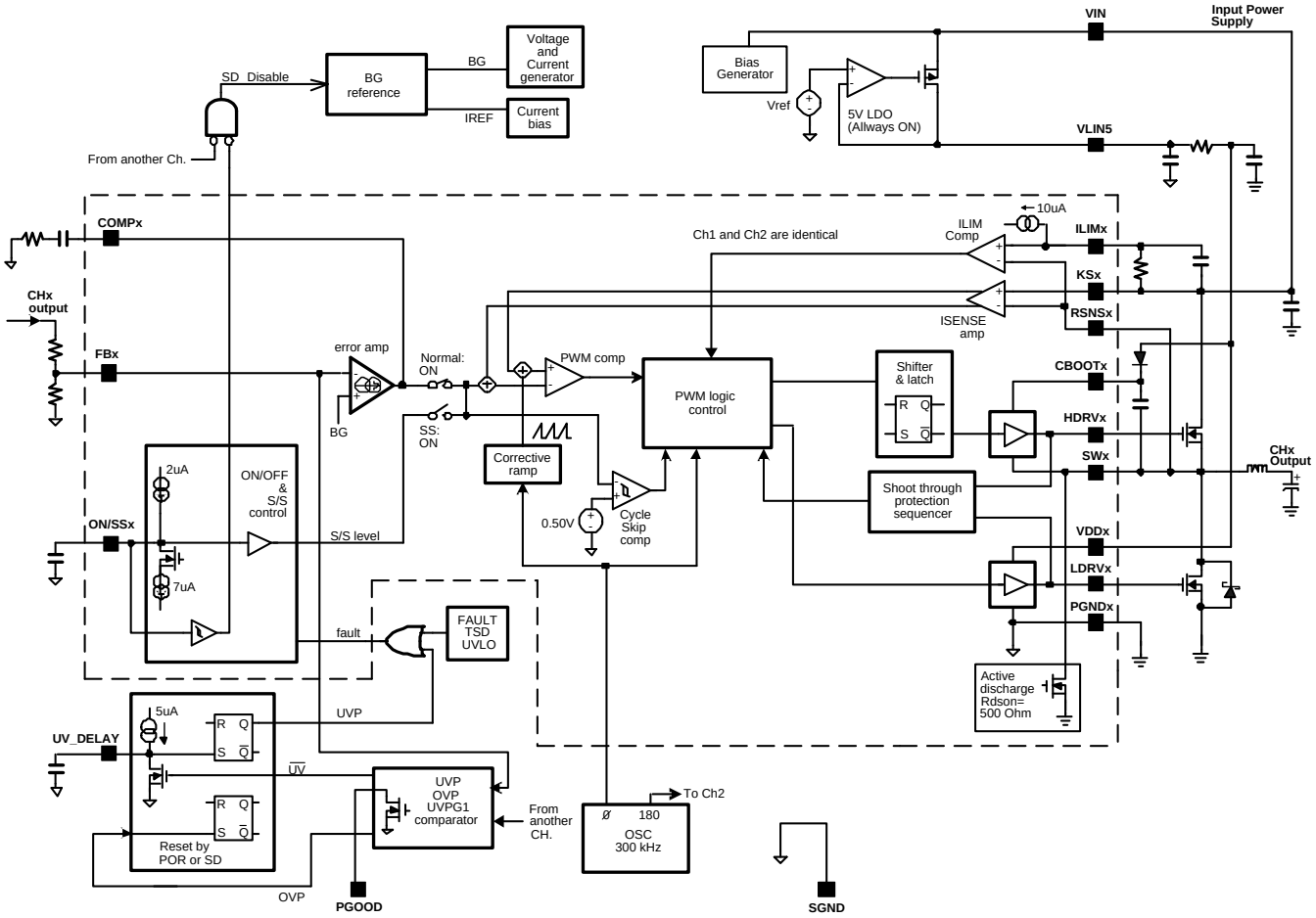


Figure 3. Typical Single Channel Application Circuit

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BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

Softstart Waveforms
(I_{LOAD1} = I_{LOAD2} = 0A)

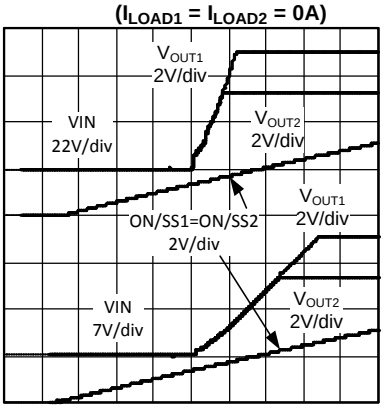


Figure 4.

Power On and PGOOD1 Waveforms
(I_{LOAD1} = I_{LOAD2} = 0A)

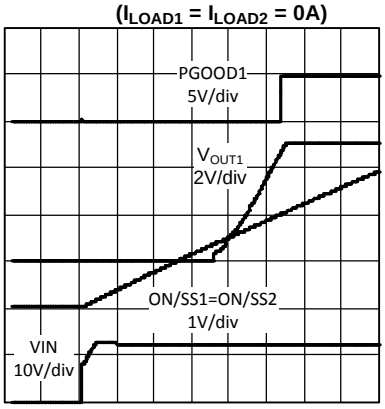


Figure 5.

UVP Startup Waveforms

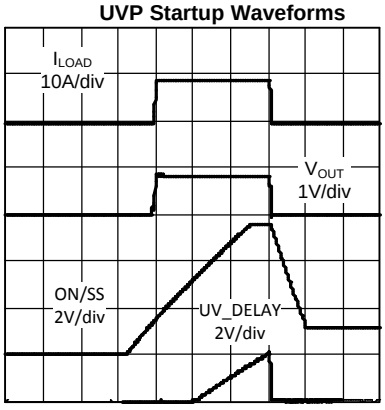


Figure 6.

Over-Current and UVP Shutdown
(I_{LOAD2} = 0A)

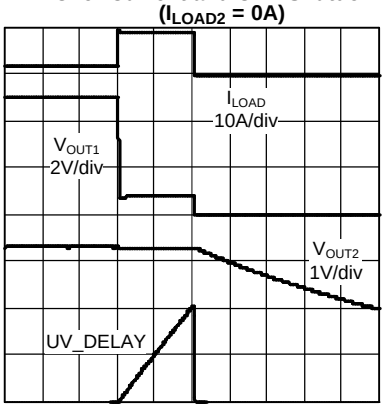


Figure 7.

Shutdown Waveforms
(I_{LOAD1} = I_{LOAD2} = 0A)

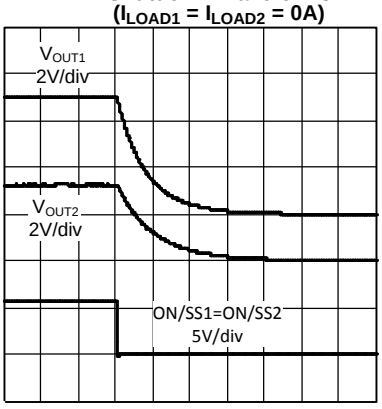


Figure 8.

Ch.1 Load Transient Response
$5V_{OUT}$, $12V_{IN}$

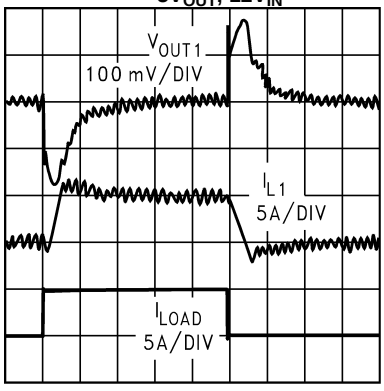


Figure 9.

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Ch.2 Load Transient Response
3.3V_{OUT}, 12V_{IN}

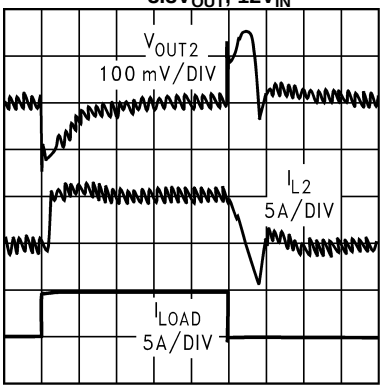


Figure 10.

Load Transient Response
Parallel Operation 1.8V_{OUT}, 12V_{IN}

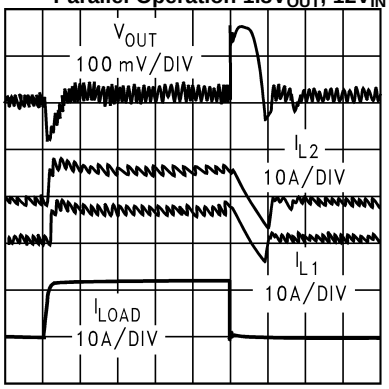


Figure 11.

Input Supply Current
vs
Temperature
(Shutdown Mode V_{IN} = 15V)

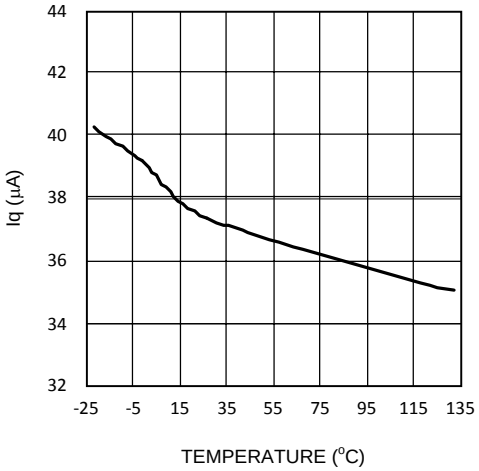


Figure 12.

Input Supply Current
vs
V_{IN}
Shutdown Mode (25°C)

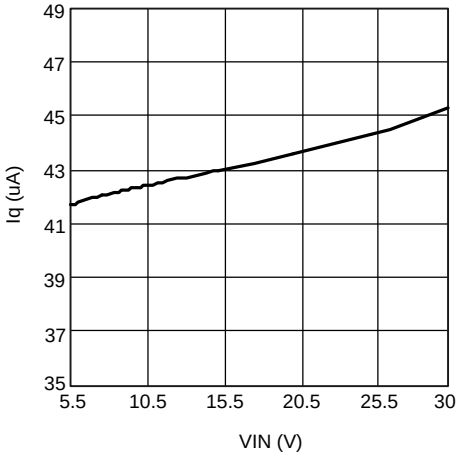


Figure 13.

VLIN5
vs
Temperature

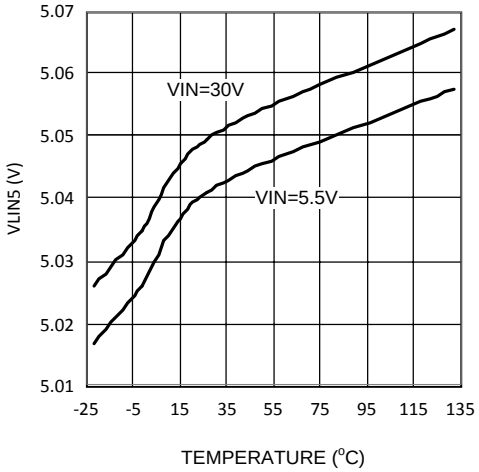


Figure 14.

VLIN5
vs
V_{IN} (25°C)

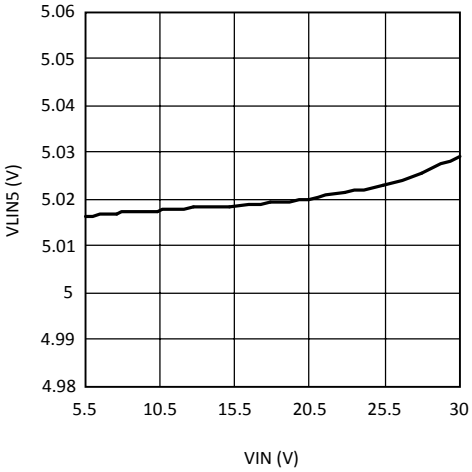


Figure 15.

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FB Reference Voltage vs Temperature

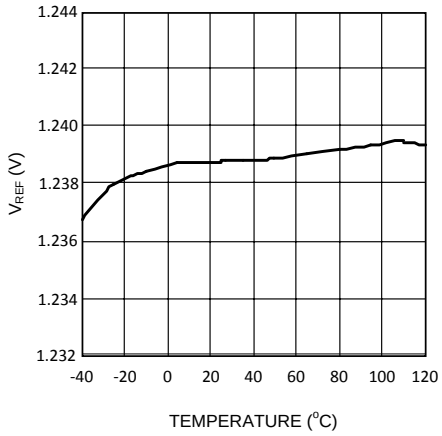


Figure 16.

Operating Frequency vs Temperature

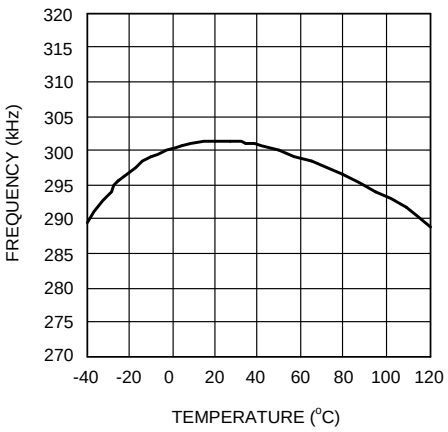


Figure 17.

Error Amplifier Gain vs Temperature

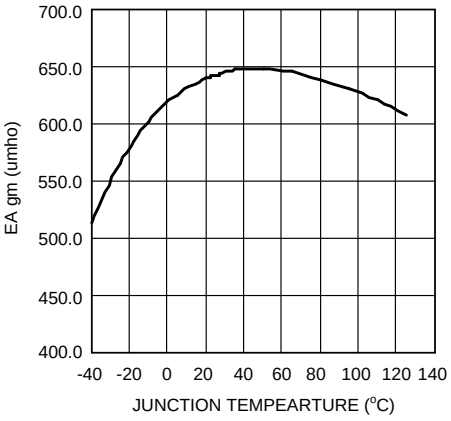


Figure 18.

Efficiency vs Load Current Ch.1 = 5V, Ch.2 = Off

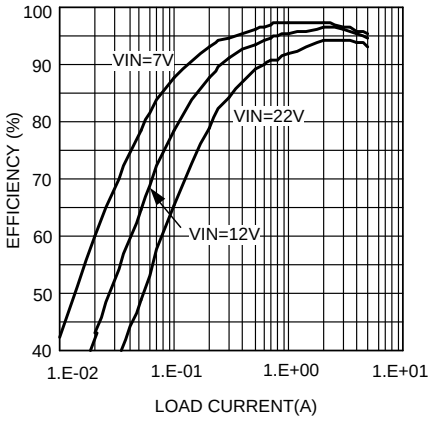


Figure 19.

Efficiency vs Load Current Ch.2 = 2.5V, Ch.1 = Off

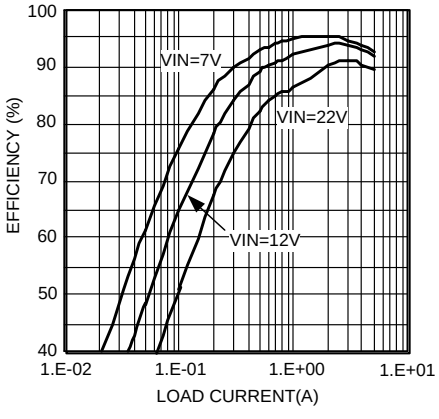


Figure 20.

Efficiency vs Load Current Ch.2 = 3.3V, Ch.1 = Off

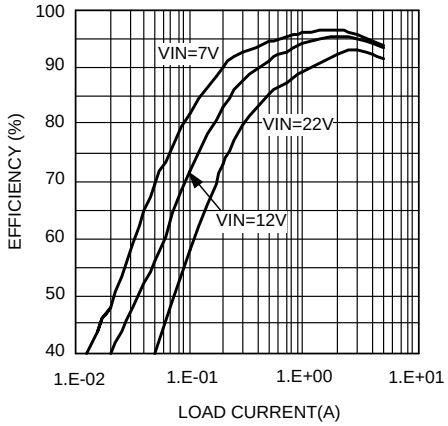


Figure 21.

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APPLICATION INFORMATION

OPERATION DESCRIPTIONS

SOFT START

The ON/SS1 pin has dual functionality as both channel enable and soft start control. The soft start block diagram is shown in Figure 22.

The LM2642 will remain in shutdown mode while both soft start pins are grounded.In a normal application (with a soft start capacitor connected between the ON/SS1 pin and SGND) soft start functions as follows. As the input voltage rises (note: Iss starts to flow when VIN ≥ 2.2V), the internal 5V LDO starts up, and an internal 2µA current charges the soft start capacitor. During soft start phase, the error amplifier output voltage at the COMPx pin is clamped at 0.55V and the duty cycle is controlled only by the soft start voltage. As the SSx pin voltage ramps up, the duty cycle increases proportional to the soft start ramp, causing the output voltage to ramp up. The rate at which the duty cycle increases depends on the capacitance of the soft start capacitor. The higher the capacitance, the slower the output voltage ramps up. When the corresponding output voltage exceeds 98% (typical) of the set target voltage, the regulator switches from soft start to normal operating mode. At this time, the 0.55V clamp at the output of the error amplifier releases and peak current feedback control takes over. Once in peak current feedback control mode, the output of the error amplifier will travel within the 0.5V and 2V window to achieve PWM control. See Figure 23.

During soft start, over-voltage protection and current limit remain in effect. The under voltage protection feature is activated when the ON/SS pin exceeds the timeout threshold (3.3V typical). If the ON/SSx capacitor is too small, the duty cycle may increase too rapidly, causing the device to latch off due to output voltage overshoot above the OVP threshold. This becomes more likely in applications requiring low output voltage, high input voltage and light load. A capacitance of 10nF is recommended at each soft start pin to provide a smooth monotonic output ramp.

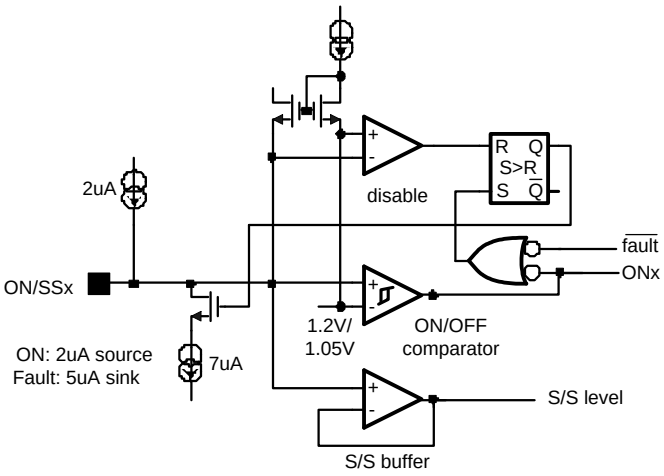


Figure 22. Soft Start and ON/OFF

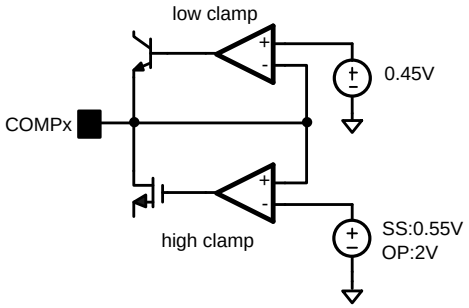


Figure 23. Voltage Clamp at COMPx Pin

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SEQUENTIAL STARTUP

Sequential startup can be implemented by simply connecting PGOOD1 to SS/ON2. Once channel 1 has reached 94% of nominal, PGOOD1 will go high, thus enabling SS/ON2. In this mode of operation, channel 2 will be controlled by the state of channel 1. If channel 1 falls out of the PGOOD1 window, channel 2 will be switched off immediately.

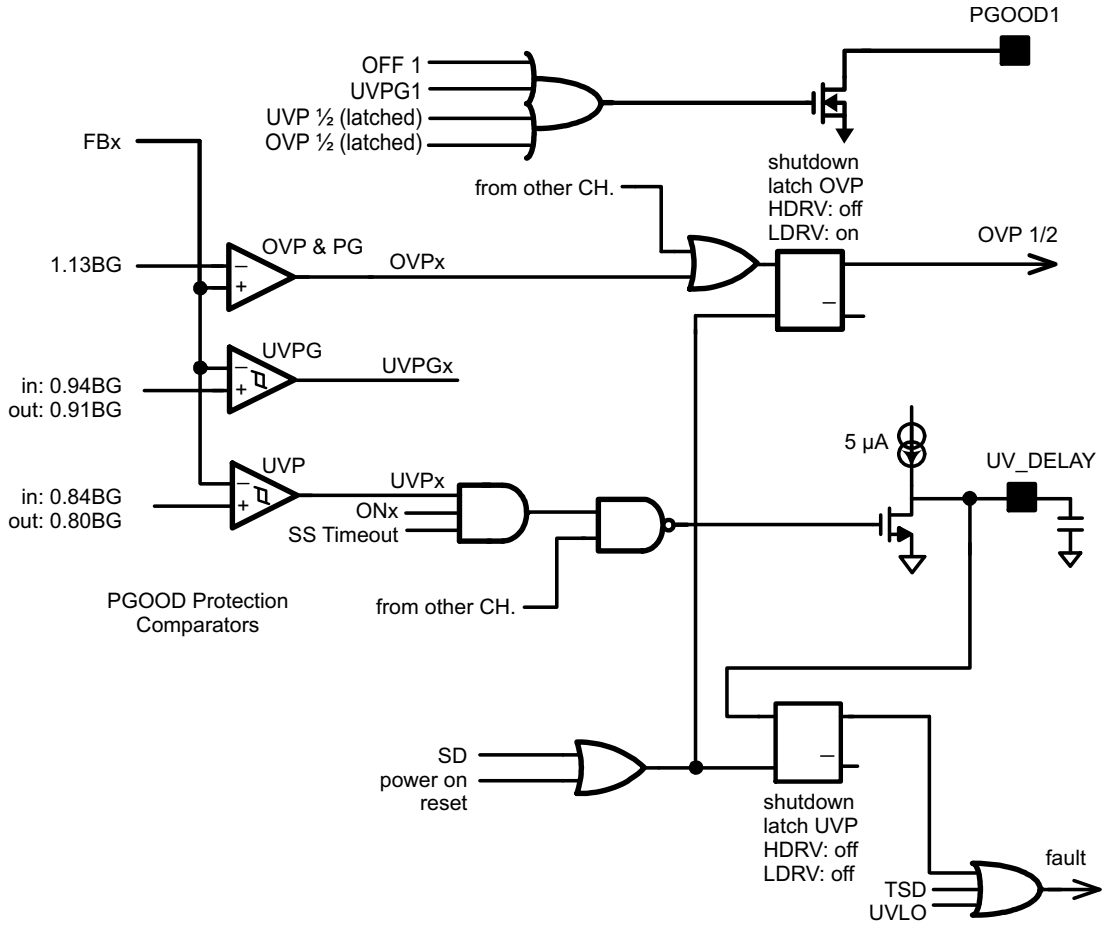


Figure 24. PGOOD, OVP and UVP

OVER VOLTAGE PROTECTION (OVP)

If the output voltage on either channel rises above 113% of nominal, over voltage protection activates. Both channels will latch off, and the PGOOD1 pin will go low. When the OVP latch is set, the high side FET driver, HDRVx, is immediately turned off and the low side FET driver, LDRVx, is turned on to discharge the output capacitor through the inductor. To reset the OVP latch, either the input voltage must be cycled, or both channels must be switched off.

UNDER VOLTAGE PROTECTION (UVP) AND UV DELAY

If the output voltage on either channel falls below 80% of nominal, under voltage protection activates. As shown in Figure 24, an under-voltage event will shut off the UV_DELAY MOSFET, which will allow the UV_DELAY capacitor to charge at 5uA (typical). At the UV_DELAY threshold (2.3V typical) both channels will latch off. Also, UV_DELAY will be disabled and the UV_DELAY pin will return to 0V. During UVP, both the high side and low side FET drivers will be turned off. If no capacitor is connected to the UV_DELAY pin, the UVP latch will be activated immediately. To reset the UVP latch, either the input voltage must be cycled, or both ON/SS pins must be pulled low. The UVP function can be disabled by connecting the UV_DELAY pin to ground.

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POWER GOOD

A power good pin (PGOOD1) is available to monitor the output status of Channel 1. As shown in Figure 24, the pin connects to the output of an open drain MOSFET, which will remain open while Channel 1 is within operating range. PGOOD1 will go low (low impedance to ground) under the following four conditions:

1. Channel 1 is turned off
2. Channel 1 output falls below 90.3% of nominal (UVPG1)
3. OVP on either channel
4. UVP on either channel

When on, the PGOOD1 pin is capable of sinking 0.95mA (typical). If an OVP or UVP condition occurs, both channels will latch off, and the PGOOD1 pin will be latched low. During a UVPG1 condition, however, PGOOD1 will not latch off. The pin will stay low until Channel 1 output voltage returns to 94% (typical) of nominal. See Vpwrgd in the Electrical Characteristics table.

OUTPUT CAPACITOR DISCHARGE

Each channel has an embedded 480Ω MOSFET with the drain connected to the SWx pin. This MOSFET will discharge the output capacitor of its channel if its channel is off, or the IC enters a fault state caused by one of the following conditions:

1. UVP
2. UVLO
3. Thermal shut-down (TSD)

If an output over voltage event occurs, the HDRVx will be turned off and LDRVx will be turned on immediately to discharge the output capacitor of both channels through the inductor.

BOOTSTRAP DIODE SELECTION

The bootstrap diode and capacitor form a supply that floats above the switch node voltage. VLIN5 powers this supply, creating approximately 5V (minus the diode drop) which is used to power the high side FET drivers and driver logic. When selecting a bootstrap diode, Schottky diodes are preferred due to their low forward voltage drop, but care must be taken for circuits that operate at high ambient temperature. The reverse leakage of some Schottky diodes can increase by more than 1000x at high temperature, and this leakage path can deplete the charge on the bootstrap capacitor, starving the driver and logic. Standard PN junction diodes and fast rectifier diodes can also be used, and these types maintain tighter control over reverse leakage current across temperature.

SWITCHING NOISE REDUCTION

Power MOSFETs are very fast switching devices. In synchronous rectifier converters, the rapid increase of drain current in the top FET coupled with parasitic inductance will generate unwanted Ldi/dt noise spikes at the source node of the FET (SWx node) and also at the VIN node. The magnitude of this noise will increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI), and can also cause problems in device performance. Therefore, it must be suppressed using one of the following methods.

It is strongly recommended to add R-C filters to the current sense amplifier inputs as shown in Figure 26. This will reduce the susceptibility to switching noise, especially during heavy load transients and short on time conditions. The filter components should be connected as close as possible to the IC. Note that these filters should be used when a current sense resistor is used.

As shown in Figure 25, adding a resistor in series with the SWx pin will slow down the gate drive (HDRVx), thus slowing the rise and fall time of the top FET, yielding a longer drain current transition time.

Usually a 3.3Ω to 4.7Ω resistor is sufficient to suppress the noise. Top FET switching losses will increase with higher resistance values.

Small resistors (1-5 ohms) can also be placed in series with the HDRVx pin or the CBOOTx pin to effectively reduce switch node ringing. A CBOOT resistor will slow the rise time of the FET, whereas a resistor at HDRV will reduce both rise and fall times.

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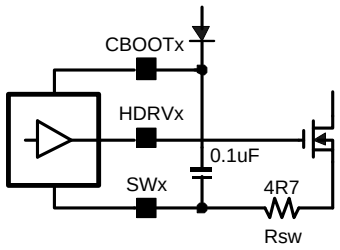


Figure 25. SW Series Resistor

CURRENT SENSING AND LIMITING

As shown in Figure 26, the KSx and RSNSx pins are the inputs of the current sense amplifier. Current sensing is accomplished either by sensing the Vds of the top FET or by sensing the voltage across a current sense resistor connected from VIN to the drain of the top FET. The advantage of sensing current across the top FET are reduced parts count, cost and power loss, whereas using a current sense resistor improves the current sense accuracy. Keeping the differential current-sense voltage below 200mV ensures linear operation of the current sense amplifier. Therefore, the Rdson of the top FET or the current sense resistor must be small enough so that the current sense voltage does not exceed 200mV when the top FET is on. There is a leading edge blanking circuit that forces the top FET on for at least 166ns. Beyond this minimum on time, the output of the PWM comparator is used to turn off the top FET. Additionally, a minimum voltage of at least 50mV across Rsns is recommended to ensure a high SNR at the current sense amplifier.

Assuming a maximum of 200mV across Rsns, the current sense resistor can be calculated as follows:

$$R_{sns\ max} = \frac{200\ mV}{I_{max} + \frac{1}{2} I_{rip}} \tag{1}$$

where Imax is the maximum expected load current, including overload multiplier (ie:120%), and Irip is the inductor ripple current (See equation 7). The above equation gives the maximum allowable value for Rsns. Switching losses will increase with Rsns, thus lowering efficiency.

The peak current limit is set by an external resistor connected between the ILIMx pin and the KSx pin. An internal 10µA current sink on the ILIMx pin produces a voltage across the resistor to set the current limit threshold which is compared to the current sense voltage. A 10nF capacitor across this resistor is required to filter unwanted noise that could improperly trip the current limit comparator.

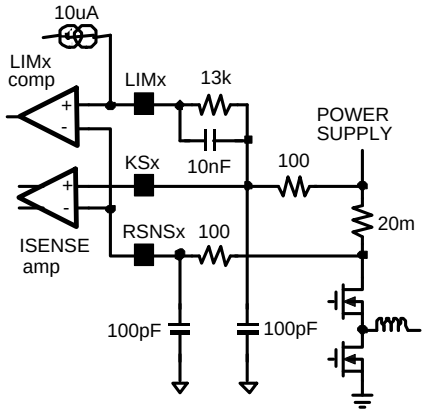


Figure 26. Current Sense and Current Limit

Current limit is activated when the inductor current is high enough to cause the voltage at the RSNSx pin to be lower than that of the ILIMx pin. This toggles the comparator, thus turning off the top FET immediately. The comparator is disabled either when the top FET is turned off or during the leading edge blanking time. The equation for current limit resistor, R_{lim}, is as follows:

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$$R_{lim} = \frac{(I_{lim} + \frac{1}{2} I_{rip}) R_{sns}}{10\ \mu A} \quad (2)$$

Where Ilim is the load current at which the current limit comparator will be tripped.

When sensing current across the top FET, replace Rsns with the Rdson of the FET. This calculated Rlim value specifies that the minimum current limit will not be less than Imax. It is recommended that a 1% tolerance resistor be used.

When sensing across the top FET, Rdson will show more variation than a current sense resistor, largely due to temperature. Rdson will increase proportional to temperature according to a specific temperature coefficient. Refer to the manufacturer's datasheet to determine the range of Rdson values over operating temperature or see the Component Selection section (equation 12) for a calculation of maximum Rdson. This will prevent Rdson variations from prematurely setting off the current limit comparator as the operating temperature increases.

To ensure accurate current sensing, special attention in board layout is required. The KSx and RSNSx pins require separate traces to form a Kelvin connection to the corresponding current sense nodes.

INPUT UNDER VOLTAGE LOCKOUT (UVLO)

The input under-voltage lock out threshold, which is sensed via the VLIN5 internal LDO output, is 4.0V (typical). Below this threshold, both HDRVx and LDRVx will be turned off and the internal 480Ω MOSFETs will be turned on to discharge the output capacitors through the SWx pins. During UVLO, the ON/SS pins will sink 5mA to discharge the soft start capacitors and turn off both channels. As the input voltage increases again above 4.0V, UVLO will be de-activated, and the device will restart again from soft start phase. If the voltage at VLIN5 remains below 4.5V, but above the 4.0V UVLO threshold, the device cannot be ensured to operate within specification.

If the input voltage is between 4.0V and 5.2V, the VLIN5 pin will not regulate, but will follow approximately 200mV below the input voltage.

DUAL-PHASE PARALLEL OPERATION

In applications with high output current demand, the two switching channels can be configured to operate as a two-180° out of phase converter to provide a single output voltage with current sharing between the two switching channels. This approach greatly reduces the stress and heat on the output stage components while lowering input ripple current. The sum of inductor ripple current is also reduced which results in lowering output ripple voltage. Figure 3 shows an example of a typical two-phase circuit. Because precision current sense is the primary design criteria to ensure accurate current sharing between the two channels, both channels must use external sense resistors for current sensing. To minimize the error between the error amplifiers of the two channels, tie the feedback pins FB1 and FB2 together and connect to a single voltage divider for output voltage sensing. Also, tie the COMP1 and COMP2 together and connect to the compensation network. ON/SS1 and ON/SS2 must be tied together to enable and disable both channels simultaneously.

COMPONENT SELECTION

OUTPUT VOLTAGE SETTING

The output voltage for each channel is set by the ratio of a voltage divider as shown in Figure 27. The resistor values can be determined by the following equation:

$$R_1 = \frac{R_2}{\left(\frac{V_{nom}}{V_{fb}} - 1\right)} \quad (3)$$

Where Vfb=1.238V. Although increasing the value of R1 and R2 will increase efficiency, this will also decrease accuracy. Therefore, a maximum value is recommended for R2 in order to keep the output within .3% of Vnom. This maximum R2 value should be calculated first with the following equation:

$$R_{2\ max} = \frac{.3\% \cdot V_{nom}}{200\ nA} \quad (4)$$

Where 200nA is the maximum current drawn by FBx pin.

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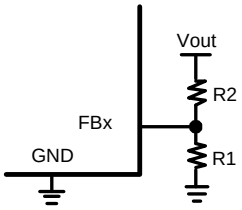


Figure 27. Output Voltage Setting

Example: Vnom=5V, Vfb=1.238V, Ifbmax=200nA.

$$R_{2\ max} = \frac{.003 \cdot 5V}{200\ nA} = 75\ k\Omega \tag{5}$$

Choose 60K

$$R_1 = \frac{60k}{\left(\frac{5V}{1.238V} - 1\right)} = 19.75\ k\Omega \cong 20\ k\Omega \tag{6}$$

The output voltage is limited by the maximum duty cycle as well as the minimum on time. Figure 28 shows the limits for input and output voltages. The recommended maximum output voltage is approximately 1V less than the nominal input voltage. At 30V input, the minimum output is approximately 2.3V and the maximum is approximately 27V.

For input voltages below 5.5V, VLIN5 must be connected to Vin through a small resistor (approximately 4.7 ohm). This will ensure that VLIN5 does not fall below the UVLO threshold.

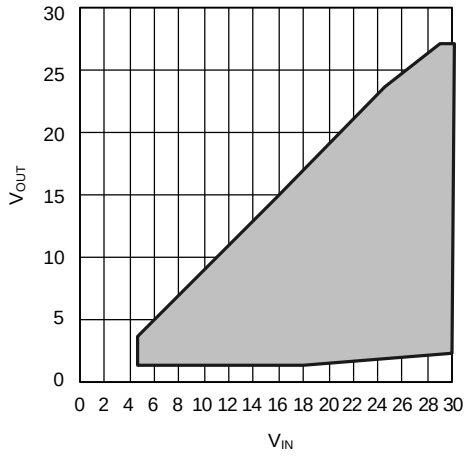


Figure 28. Available Output Voltage Range

OUTPUT CAPACITOR SELECTION

In applications that exhibit large and fast load current swings, the slew rate of such a load current transient may be beyond the response speed of the regulator. Therefore, to meet voltage transient requirements during worst-case load transients, special consideration should be given to output capacitor selection. The total combined ESR of the output capacitors must be lower than a certain value, while the total capacitance must be greater than a certain value. Also, in applications where the specification of output voltage regulation is tight and ripple voltage must be low, starting from the required output voltage ripple will often result in fewer design iterations.

ALLOWED TRANSIENT VOLTAGE EXCURSION

The allowed output voltage excursion during a load transient (ΔVc_s) is:

$$\Delta V_{c_s} = (\delta\% - \varepsilon\%) \cdot V_{nom} - \tfrac{1}{2} V_{rip}. \tag{7}$$

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Where ±δ% is the output voltage regulation window and ±ε% is the output voltage initial accuracy.

Example: Vnom = 5V, δ% = 7%, ε% = 3.4%, Vrip = 40mV peak to peak.

$$\Delta V_{c_s} = (7\% - 3.4\%) \times 5V - \frac{40\,mV}{2}$$
$$= 160\,mV. \quad (8)$$

Since the ripple voltage is included in the calculation of ΔVc_s, the inductor ripple current should not be included in the worst-case load current excursion. That is, the worst-case load current excursion should be simply maximum load current change specification, ΔIc_s.

MAXIMUM ESR CALCULATION

Unless the rise and fall times of a load transient are slower than the response speed of the control loop, if the total combined ESR (Re) is too high, the load transient requirement will not be met, no matter how large the capacitance.

The maximum allowed total combined ESR is:

$$R_{e_max} = \frac{\Delta V_{c_s}}{\Delta I_{c_s}} \quad (9)$$

Example: ΔVc_s = 160mV, ΔIc_s = 3A. Then Re_max = 53.3mΩ.

Maximum ESR criterion can be used when the associated capacitance is high enough, otherwise more capacitors than the number determined by this criterion should be used in parallel.

MINIMUM CAPACITANCE CALCULATION

In a switch mode power supply, the minimum output capacitance is typically dictated by the load transient requirement. If there is not enough capacitance, the output voltage excursion will exceed the maximum allowed value even if the maximum ESR requirement is met. The worst-case load transient is an unloading transient that happens when the input voltage is the highest and when the present switching cycle has just finished. The corresponding minimum capacitance is calculated as follows:

$$C_{min} = \frac{L \cdot \left[\Delta V_{c_s} - \sqrt{(\Delta V_{c_s})^2 - (\Delta I_{c_s} \cdot R_e)^2}\right]}{V_{nom} \cdot R_e^2} \quad (10)$$

Notice it is already assumed the total ESR, Re, is no greater than Re_max, otherwise the term under the square root will be a negative value. Also, it is assumed that L has already been selected, therefore the minimum L value should be calculated before Cmin and after Re (see Inductor Selection below). Example: Re = 20mΩ, Vnom = 5V, ΔVc_s = 160mV, ΔIc_s = 3A, L = 8μH

$$C_{min} = \frac{8\,\mu H \cdot \left[160\,mV - \sqrt{(160\,mV)^2 - (3A \times 20\,m\Omega)^2}\right]}{5 \times (20\,m\Omega)^2}$$
$$= 47\,\mu F. \quad (11)$$

Generally speaking, Cmin decreases with decreasing Re, ΔIc_s, and L, but with increasing Vnom and ΔVc_s.

INDUCTOR SELECTION

The size of the output inductor can be determined from the desired output ripple voltage, Vrip, and the impedance of the output capacitors at the switching frequency. The equation to determine the minimum inductance value is as follows:

$$L_{min} = \frac{V_{in} - V_{nom}}{f \cdot V_{in}} \cdot \frac{V_{nom} \cdot R_e}{V_{rip}} \quad (12)$$

In the above equation, Re is used in place of the impedance of the output capacitors. This is because in most cases, the impedance of the output capacitors at the switching frequency is very close to Re. In the case of ceramic capacitors, replace Re with the true impedance.

Example: Vin (max)= 30V, Vnom = 5.0V, Vrip = 40mV, Re =20mΩ, f = 300kHz

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$$L_{min} = \frac{30V - 5.0V}{300\,kHz \cdot 30V} \cdot \frac{5.0V \cdot 20\,m\Omega}{40\,mV}$$

$$L_{min} = 7\,\mu H \quad (13)$$

Lmin = 7µH

The actual selection process usually involves several iterations of all of the above steps, from ripple voltage selection, to capacitor selection, to inductance calculations. Both the highest and the lowest input and output voltages and load transient requirements should be considered. If an inductance value larger than Lmin is selected, make sure that the Cmin requirement is not violated.

Priority should be given to parameters that are not flexible or more costly. For example, if there are very few types of capacitors to choose from, it may be a good idea to adjust the inductance value so that a requirement of 3.2 capacitors can be reduced to 3 capacitors.

Since inductor ripple current is often the criterion for selecting an output inductor, it is a good idea to double-check this value. The equation is:

$$I_{rip} = \frac{(V_{in} - V_{nom})}{f \cdot L} \cdot D \quad (14)$$

Where D is the duty cycle, defined by V_{nom}/V_{in}.

Also important is the ripple content, which is defined by Irip /Inom. Generally speaking, a ripple content of less than 50% is ok. Larger ripple content will cause too much loss in the inductor.

Example: Vin = 12V, Vnom = 5.0V, f = 300kHz, L = 8µH

$$I_{rip} = \frac{12V - 5.0V}{300\,kHz \cdot 8\,\mu H} \cdot \frac{5.0V}{12V} = 1.22A \quad (15)$$

Given a maximum load current of 3A, the ripple content is 1.2A / 3A = 40%.

When choosing the inductor, the saturation current should be higher than the maximum peak inductor current and the RMS current rating should be higher than the maximum load current.

INPUT CAPACITOR SELECTION

The fact that the two switching channels of the LM2642 are 180° out of phase will reduce the RMS value of the ripple current seen by the input capacitors. This will help extend input capacitor life span and result in a more efficient system. Input capacitors must be selected that can handle both the maximum ripple RMS current at highest ambient temperature as well as the maximum input voltage. In applications in which output voltages are less than half of the input voltage, the corresponding duty cycles will be less than 50%. This means there will be no overlap between the two channels' input current pulses. The equation for calculating the maximum total input ripple RMS current for duty cycles under 50% is:

$$I_{irrm} = \sqrt{I_1^2 D_1 (1 - D_1) + I_2^2 D_2 (1 - D_2) - 2 I_1 I_2 D_1 D_2} \quad (16)$$

where I1 is maximum load current of Channel 1, I2 is the maximum load current of Channel 2, D1 is the duty cycle of Channel 1, and D2 is the duty cycle of Channel 2.

Example: Imax_1 = 3.6A, Imax_2 = 3.6A, D1 = 0.42, and D2 = 0.275

$$I_{irrm} = \left[(3.6A)^2 \cdot 0.42 \cdot (1 - 0.42) + (3.6A)^2 \cdot 0.275 \cdot (1 - 0.275) - 2 \cdot 3.6A \cdot 3.6A \cdot 0.42 \cdot 0.275\right]^{.5} = 1.66A. \quad (17)$$

Choose input capacitors that can handle 1.66A ripple RMS current at highest ambient temperature. In applications where output voltages are greater than half the input voltage, the corresponding duty cycles will be greater than 50%, and there will be overlapping input current pulses. Input ripple current will be highest under these circumstances. The input RMS current in this case is given by:

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$$I_{irrm} = \left[\begin{array}{l} \left[I_1 (1 - D_1) + I_2 (1 - D_2) \right]^2 (D_1 + D_2 - 1) \\ + \left[I_1 (1 - D_1) - I_2 (D_2) \right]^2 (1 - D_2) + \\ \left[I_2 (1 - D_2) - I_1 (D_1) \right]^2 (1 - D_1) \end{array} \right]^{.5} \quad (18)$$

Where, again, I1 and I2 are the maximum load currents of channel 1 and 2, and D1 and D2 are the duty cycles. This equation should be used when both duty cycles are expected to be higher than 50%.

Input capacitors must meet the minimum requirements of voltage and ripple current capacity. The size of the capacitor should then be selected based on hold up time requirements. Bench testing for individual applications is still the best way to determine a reliable input capacitor value. The input capacitor should always be placed as close as possible to the current sense resistor or the drain of the top FET.

MOSFET SELECTION

BOTTOM FET SELECTION

During normal operation, the bottom FET is switching on and off at almost zero voltage. Therefore, only conduction losses are present in the bottom FET. The most important parameter when selecting the bottom FET is the on resistance (Rdson). The lower the on resistance, the lower the power loss. The bottom FET power loss peaks at maximum input voltage and load current. The equation for the maximum allowed on resistance at room temperature for a given FET package, is:

$$R_{dson_max} = \frac{1}{I_{max}^2 \cdot \left(1 - \frac{V_{nom}}{V_{in_max}}\right)} \times \frac{T_{j_max} - T_{a_max}}{\left[1 + TC \cdot (T_{j_max} - 25°C/W)\right] \cdot R_{\theta ja}} \quad (19)$$

where Tj_max is the maximum allowed junction temperature in the FET, Ta_max is the maximum ambient temperature, $R_{\theta ja}$ is the junction-to-ambient thermal resistance of the FET, and TC is the temperature coefficient of the on resistance which is typically in the range of 10,000ppm/°C.

If the calculated Rdson_max is smaller than the lowest value available, multiple FETs can be used in parallel. This effectively reduces the Imax term in the above equation, thus reducing Rdson. When using two FETs in parallel, multiply the calculated Rdson_max by 4 to obtain the Rdson_max for each FET. In the case of three FETs, multiply by 9.

$$R_{ds_max} = \frac{1}{(3.6A)^2 \cdot \left(1 - \frac{5V}{30V}\right)} \times \frac{100°C - 60°C}{\left[1 + 0.01/°C \cdot (100°C - 25°C)\right] \cdot 60°C/W} = 35.3\,m\Omega \quad (20)$$

If the selected FET has an Rds value higher than 35.3Ω, then two FETs with an Rdson less than 141mΩ (4 x 35.3mΩ) can be used in parallel. In this case, the temperature rise on each FET will not go to Tj_max because each FET is now dissipating only half of the total power.

TOP FET SELECTION

The top FET has two types of losses: switching loss and conduction loss. The switching losses mainly consist of crossover loss and bottom diode reverse recovery loss. Since it is rather difficult to estimate the switching loss, a general starting point is to allot 60% of the top FET thermal capacity to switching losses. The best way to precisely determine switching losses is through bench testing. The equation for calculating the on resistance of the top FET is thus:

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$$R_{ds_max} = \frac{V_{in_min} \cdot .4}{I_{max}^2 \cdot V_{nom}} \times \frac{T_{j_max} - T_{a_max}}{\left[1 + TC \cdot (T_{j_max} - 25°C/W)\right] \cdot R_{\theta ja}} \quad (21)$$

Example: Tj_max = 100°C, Ta_max = 60°C, Rqja = 60°C/W, Vin_min = 5.5V, Vnom = 5V, and Iload_max = 3.6A.

$$R_{ds_max} = \frac{5.5V \times .4}{(3.6A)^2 \times 5V} \times \frac{100°C - 60°C}{\left[1 + 0.01/°C \cdot (100°C - 25°C)\right] \cdot 60°C/W} = 13\,m\Omega \quad (22)$$

When using FETs in parallel, the same guidelines apply to the top FET as apply to the bottom FET.

LOOP COMPENSATION

The general purpose of loop compensation is to meet static and dynamic performance requirements while maintaining stability. Loop gain is what is usually checked to determine small-signal performance. Loop gain is equal to the product of control-output transfer function and the output-control transfer function (the compensation network transfer function). Generally speaking it is a good idea to have a loop gain slope that is -20dB /decade from a very low frequency to well beyond the crossover frequency. The crossover frequency should not exceed one-fifth of the switching frequency, i.e. 60kHz in the case of LM2642. The higher the bandwidth is, the faster the load transient response speed will potentially be. However, if the duty cycle saturates during a load transient, further increasing the small signal bandwidth will not help. Since the control-output transfer function usually has very limited low frequency gain, it is a good idea to place a pole in the compensation at zero frequency, so that the low frequency gain will be relatively large. A large DC gain means high DC regulation accuracy (i.e. DC voltage changes little with load or line variations). The rest of the compensation scheme depends highly on the shape of the control-output plot.

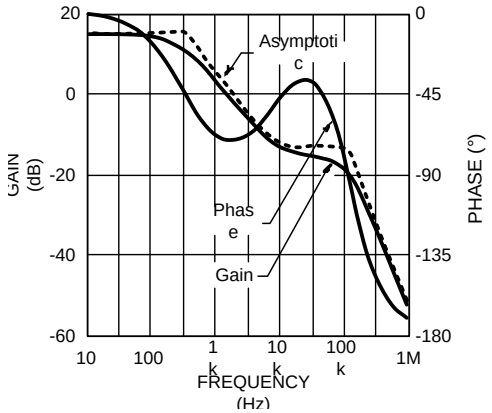


Figure 29. Control-Output Transfer Function

As shown in Figure 29, the control-output transfer function consists of one pole (fp), one zero (fz), and a double pole at fn (half the switching frequency). The following can be done to create a -20dB /decade roll-off of the loop gain: Place the first pole at 0Hz, the first zero at fp, the second pole at fz, and the second zero at fn. The resulting output-control transfer function is shown in Figure 30.

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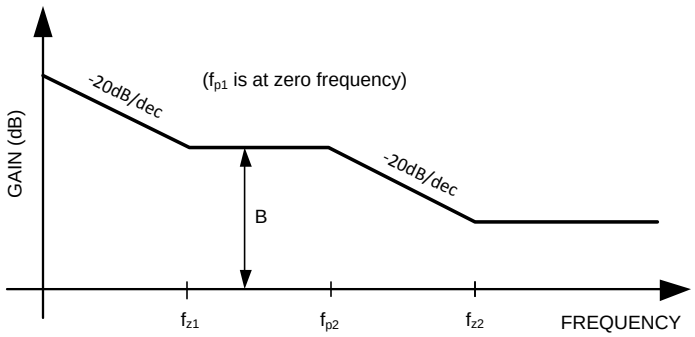


Figure 30. Output-Control Transfer Function

The control-output corner frequencies, and thus the desired compensation corner frequencies, can be determined approximately by the following equations:

$$f_z = \frac{1}{2\pi R_e C_o} \tag{23}$$

$$f_p = \frac{1}{2\pi R_o C_o} + \frac{.5}{2\pi L f C_o} \tag{24}$$

Since fp is determined by the output network, it will shift with loading (Ro) and duty cycle. First determine the range of frequencies (fpmin/max) of the pole across the expected load range, then place the first compensation zero within that range.

Example: R_e = 20mΩ, C_o = 100µF, R_{omax} = 5V/100mA = 50Ω, R_{omin} = 5V/3A = 1.7Ω:

$$f_z = \frac{1}{2\pi \cdot 20\,m\Omega \cdot 100\,\mu F} = 80\,kHz \tag{25}$$

$$f_{p\,min} = \frac{1}{2\pi \cdot 50\Omega \cdot 100\,\mu F} + \frac{.5}{2\pi \cdot 300k \cdot 8\mu \cdot 100\,\mu F} = 363\,Hz \tag{26}$$

$$fp\ max = \frac{1}{2\pi \cdot 1.7\Omega \cdot 100\mu F} + \frac{.5}{2\pi \cdot 300k \cdot 8\mu \cdot 100\mu F} = 1.27kHz \tag{27}$$

Once the fp range is determined, R_{c1} should be calculated using:

$$R_{c1} = \frac{B}{gm}\left(\frac{R_1 + R_2}{R_1}\right) \tag{28}$$

Where B is the desired gain in V/V at fp (fz1), gm is the transconductance of the error amplifier, and R1 and R2 are the feedback resistors. A gain value around 10dB (3.3v/v) is generally a good starting point.

Example: B = 3.3 v/v, gm=650 m, R1 = 20 KΩ, R2 = 60.4 KΩ:

$$R_{c1} = \frac{3.3}{650\mu}\left(\frac{20k + 60.4k}{20k}\right) = 20.4\,k\Omega \cong 20\,k\Omega \tag{29}$$

Bandwidth will vary proportional to the value of Rc1. Next, Cc1 can be determined with the following equation:

$$C_{c1} = \frac{1}{2\pi \cdot f_p \cdot R_{c1}} \tag{30}$$

Example: fpmin = 363 Hz, Rc1=20 KΩ:

$$C_{c1} = \frac{1}{2\pi \cdot 363\,Hz \cdot 20\,k\Omega} \cong 22\,nF \tag{31}$$

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The value of C_{c1} should be within the range determined by Fpmin/max. A higher value will generally provide a more stable loop, but too high a value will slow the transient response time.

The compensation network (Figure 31) will also introduce a low frequency pole which will be close to 0Hz.

A second pole should also be placed at fz. This pole can be created with a single capacitor Cc2 and a shorted Rc2 (see Figure 31). The minimum value for this capacitor can be calculated by:

$$C_{c2\ min} = \frac{1}{2\pi \cdot f_z \cdot R_{c1}} \tag{32}$$

Cc2 may not be necessary, however it does create a more stable control loop. This is especially important with high load currents and in current sharing mode.

Example: fz = 80 kHz, Rc1 = 20 KΩ:

$$C_{c2\ min} = \frac{1}{2\pi \cdot 80\ kHz \cdot 20\ k\Omega} \cong 100\ pF \tag{33}$$

A second zero can also be added with a resistor in series with Cc2. If used, this zero should be placed at fn, where the control to output gain rolls off at -40dB/dec. Generally, fn will be well below the 0dB level and thus will have little effect on stability. Rc2 can be calculated with the following equation:

$$R_{c2} = \frac{1}{2\pi \cdot f_n \cdot C_{c2}} \tag{34}$$

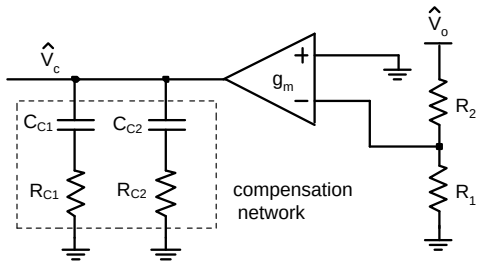


Figure 31. Compensation Network

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REVISION HISTORY

Changes from Revision H (April 2013) to Revision I	Page
• Changed layout of National Data Sheet to TI format	24

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2642MTC	NRND	TSSOP	PW	28	48	TBD	Call TI	Call TI	-40 to 125	LM2642MTC	
LM2642MTC/NOPB	ACTIVE	TSSOP	PW	28	48	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	LM2642MTC	Samples
LM2642MTCX	NRND	TSSOP	PW	28	2500	TBD	Call TI	Call TI	-40 to 125	LM2642MTC	
LM2642MTCX/NOPB	ACTIVE	TSSOP	PW	28	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	LM2642MTC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

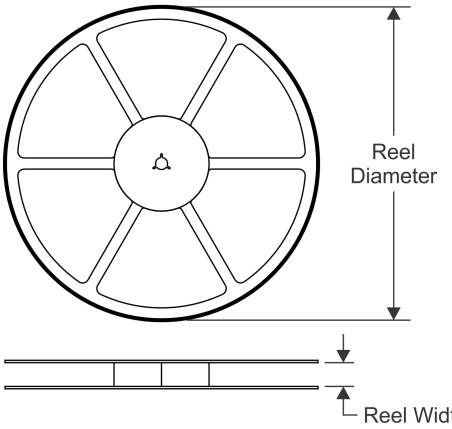
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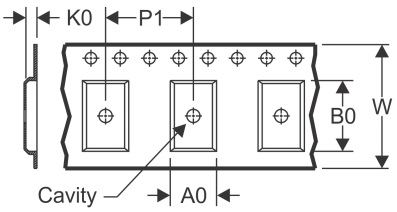
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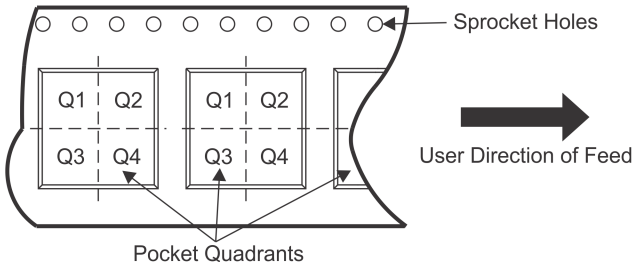


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

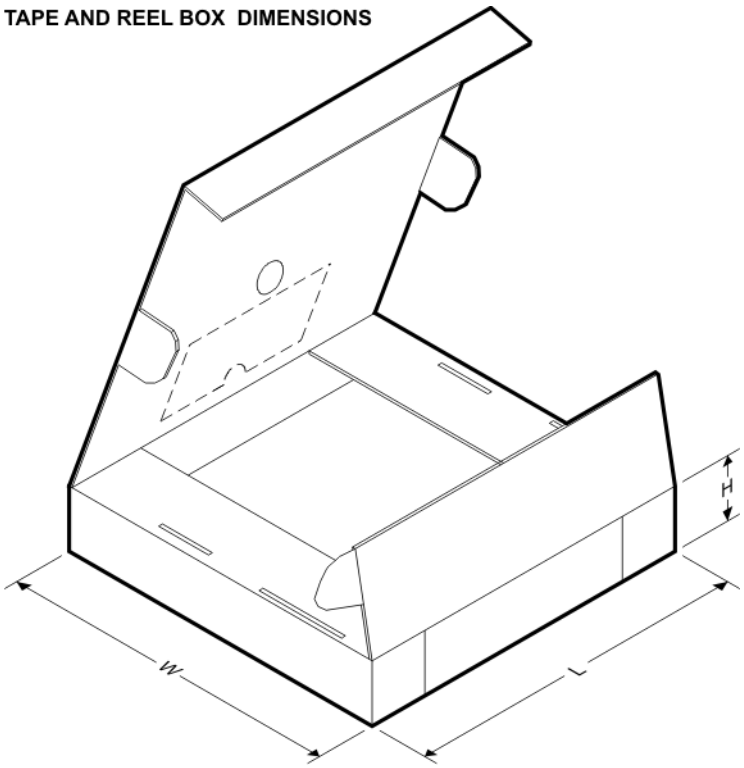
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2642MTCX	TSSOP	PW	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LM2642MTCX/NOPB	TSSOP	PW	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1

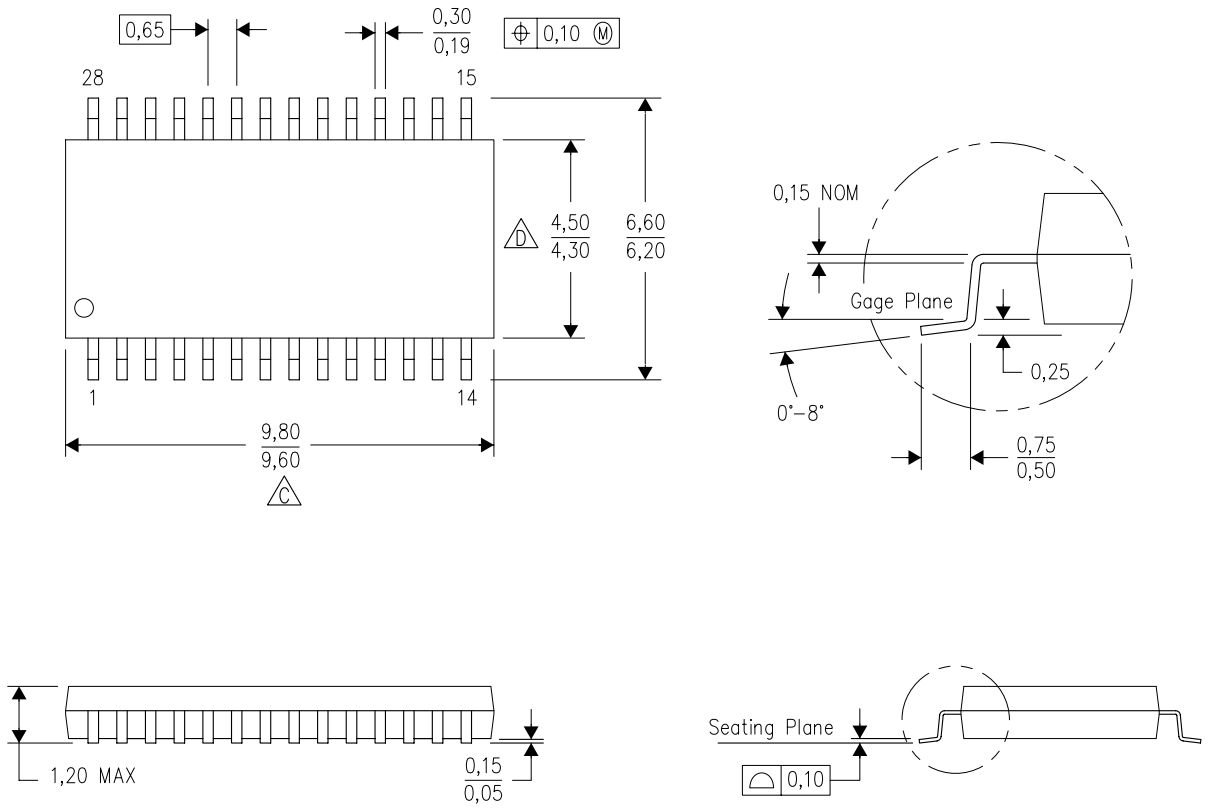
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2642MTCX	TSSOP	PW	28	2500	367.0	367.0	38.0
LM2642MTCX/NOPB	TSSOP	PW	28	2500	367.0	367.0	38.0

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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