ALC5623

I²S AUDIO CODEC + HEADPHONE AMPLIFIER

DATASHEET

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek ALC5623 Audio Codec IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2008/04/08	First release
1.1	2008/11/13	Revised Table 3, page 8. Revised section 10 Application Circuit, page 63.
1.2	2009/07/21	Revised Table 80, page 58. Revised section 11 Mechanical Dimensions, page 64.

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1. General Description

The ALC5623 is a highly-integrated I²S/PCM interface audio codec with multiple input/output ports and is designed for mobile computing and communications. It provides a Stereo Hi-Fi DAC for playback and Stereo ADC for recording via the I²S/PCM interface.

To reduce component count, the device can connect directly to:

- MONO or stereo differential analog inputs
- LINE_IN stereo single-ended analog inputs
- AUX_IN single-ended analog inputs
- Stereo Headphone Output
- Single-ended stereo configurable to AUXOUT or BTL MONO_OUT
- Stereo LINE_OUT; single-ended or Bridge-Tied Load (BTL) configurable

Multiple analog input and output pins are provided for seamless integration with analog connected wireless communication devices. Differential input/output connections efficiently reduce noise interference, providing better sound quality. Additionally, a flexible hardware 5-band equalizer with configurable gain, bandwidth, and center frequency, enriches the sound experience.

The ALC5623 AVDD operates at supply voltages from 2.3V to 3.6V. DVDD operates from 1.71V to 3.6V. To extend battery life, each section of the device can be powered down individually under software control. Leakage current in maximum power saving state is less than 10μA.

The ALC5623 is available in a 5x5mm 'Green' QFN-32 package, making it ideal for use in handheld portable systems.

2. Features

- Digital-to-Analog Converter with 92dB SNR and –85dB THD+N
- Analog-to-Digital Converter with 85dB SNR and –80dB THD+N
- Two analog stereo single-ended inputs, LINE-IN_L/R and AUXIN_L/R
- Stereo differential analog microphone inputs, with boost pre-amplifiers (+20/+30dB)
- Single-ended or Bridge-Tied Load (BTL) configurable stereo LINE_OUT
- Stereo headphone output with on-chip 45mW headphone driver (AVDD=3.3V, 16Ω load)
- Differential MONO_OUT configurable to AUXOUT (AVDD=3.3V, 32Ω load)
- Audio jack insert detection and microphone switch detection
- Power management and enhanced power saving
- Supports digital 5-band equalizer (EQ)
- Supports digital spatial sound and pseudo stereo effect
- Supports pop noise suppression
- Internal PLL can receive wide range of clock input
- Digital power supplies from 1.71V to 3.6V
- Analog power and headphone power supplied from 2.3V to 3.6V
- Supports soft-mute function
- 32-pin QFN package

3. System Applications

- Tablet PC system/Ultra-Mobile PC (UMPC)
- Personal Digital Assistants (PDA) or PDA Phone
- Multimedia Phone Applications
- Portable Navigation Device (PND)
- Bluetooth Headphone

4. Block Diagrams

4.1. Function Block

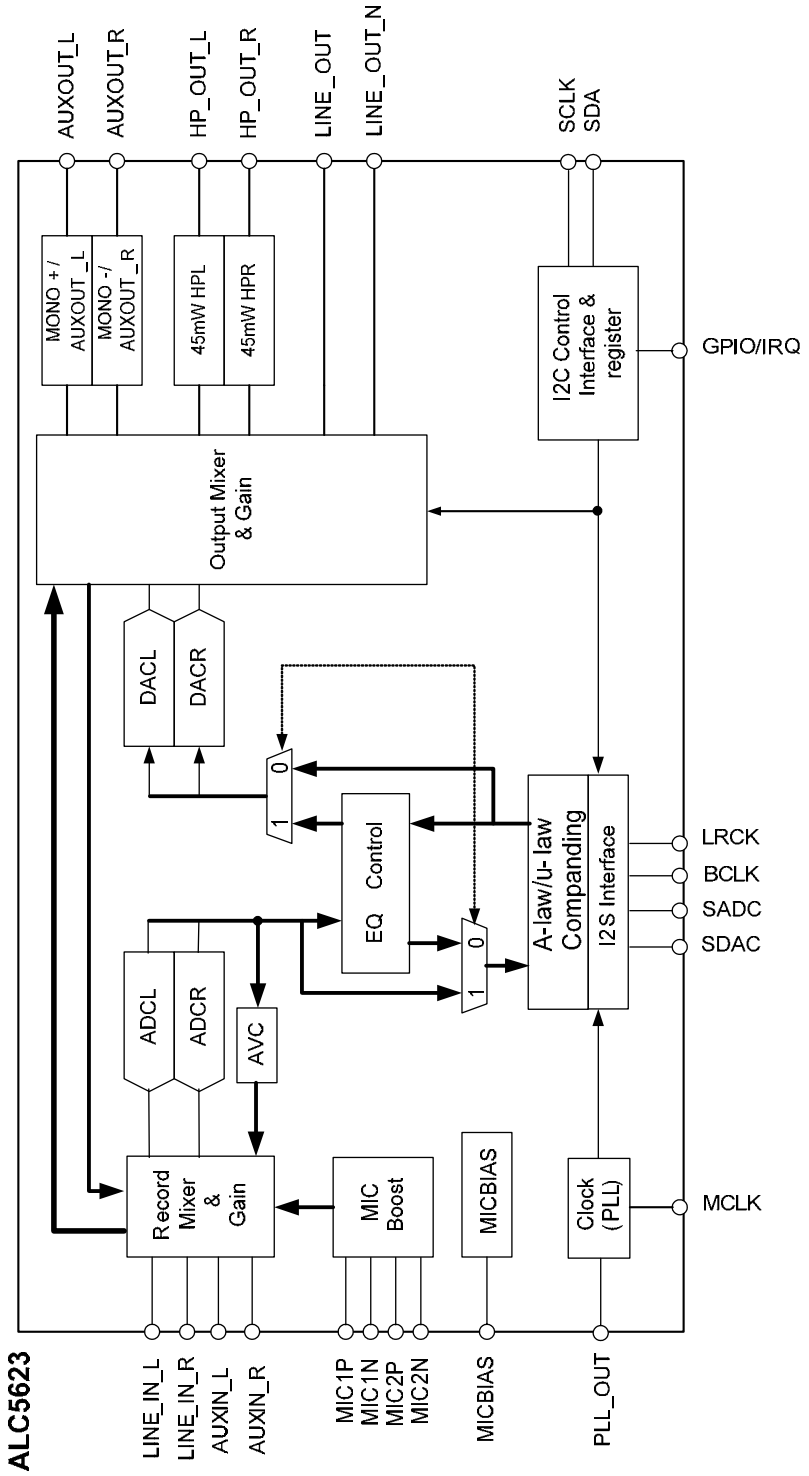


Figure 1. Block Diagram

4.2. Audio Mixer Path

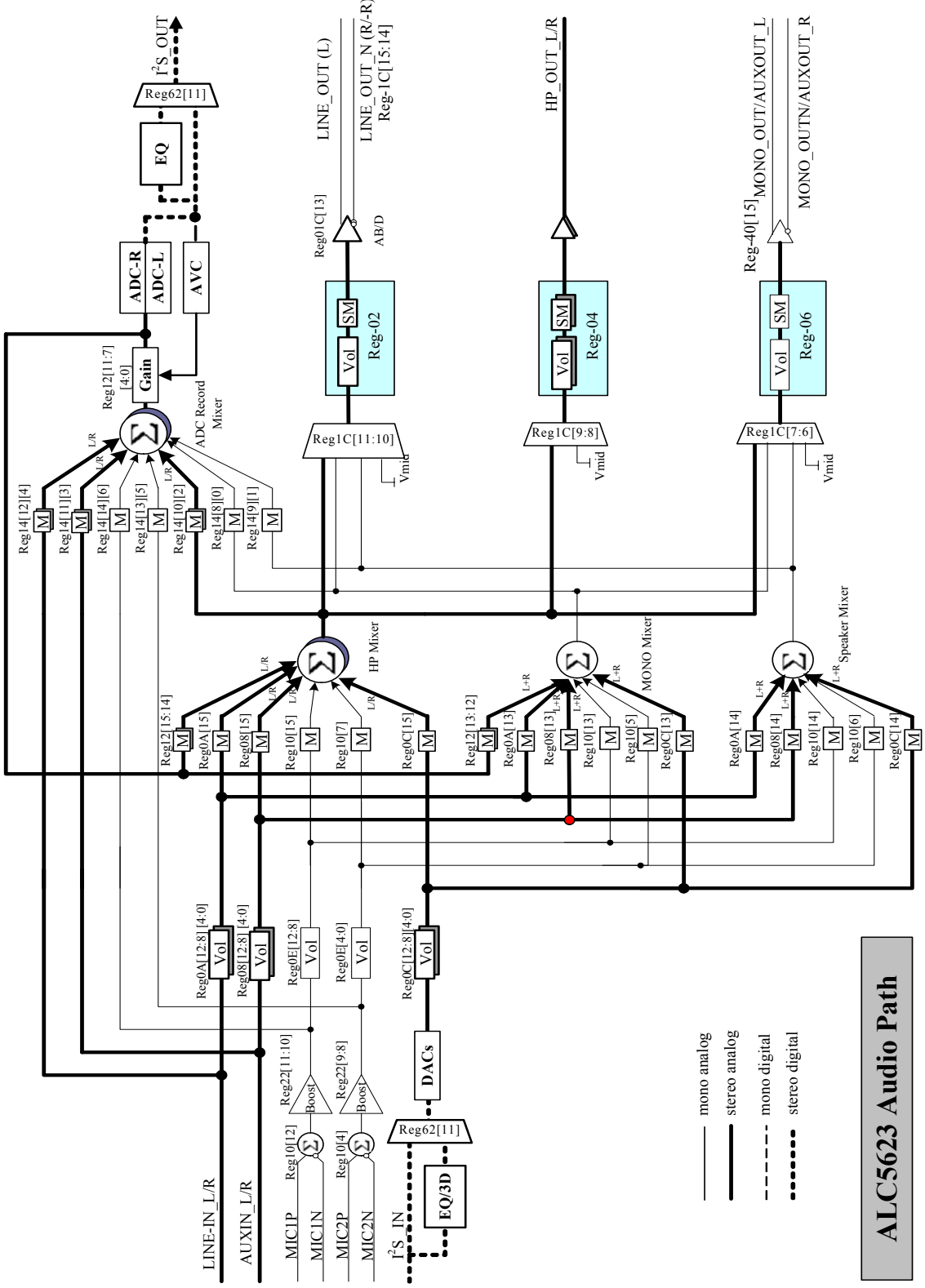


Figure 2. Audio Mixer Path

5. Pin Assignments

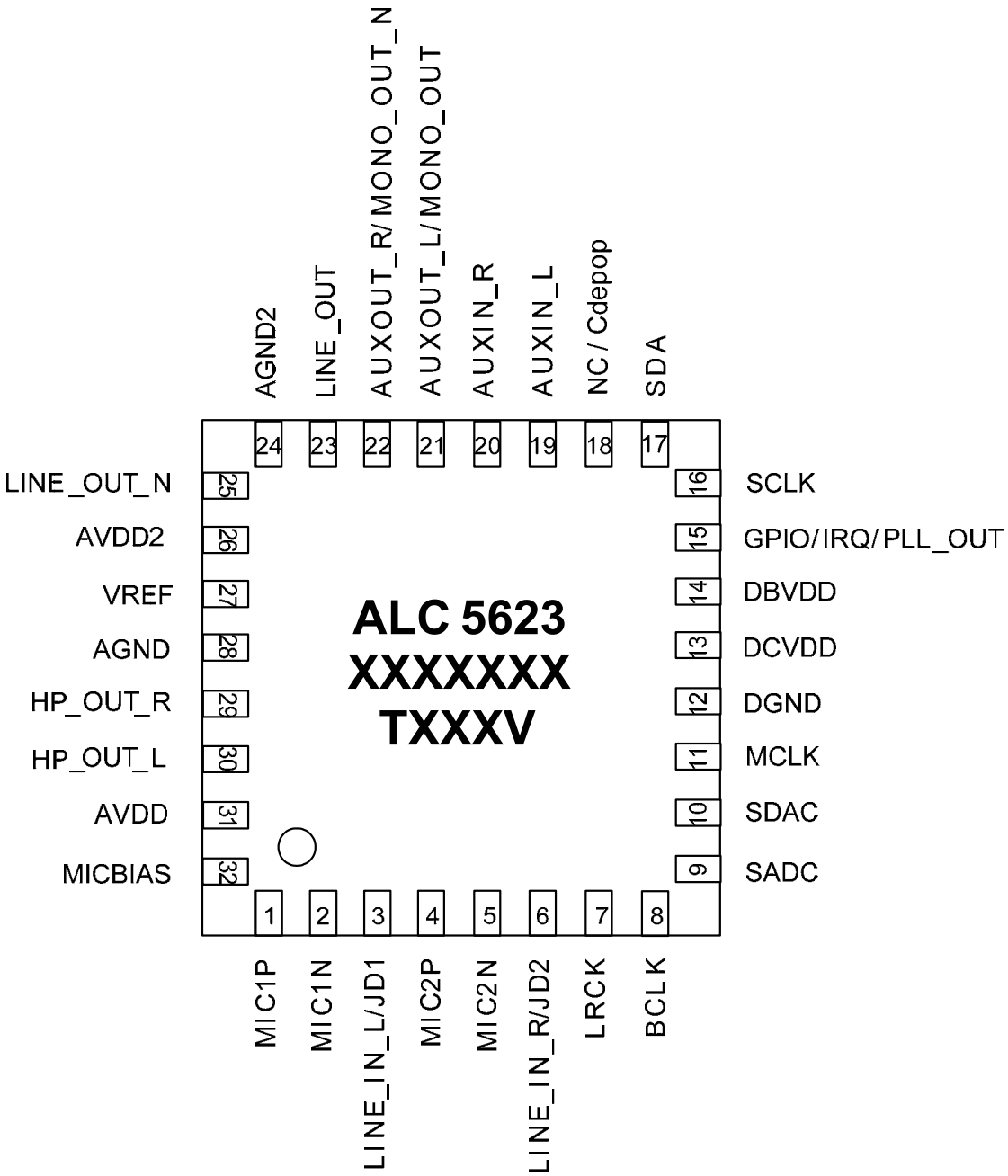


Figure 3. Pin Assignments

5.1. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 3.

6. Pin Descriptions

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
LRCK	IO	7	Digital Audio Synchronous Signal	Master: V_{OL} =0.1*DVDD, V_{OH} =0.9*DVDD Slave: Schmitt trigger
BCLK	IO	8	Digital Audio Serial Clock	Master: V_{OL} =0.1*DVDD, V_{OH} =0.9*DVDD Slave: Schmitt trigger
SADC	O	9	Serial ADC Data Output	V_{OL} =0.1*DVDD, V_{OH} =0.9*DVDD
SDAC	I	10	Serial DAC Data Input	Schmitt trigger
MCLK	I	11	Master Clock Input	Schmitt trigger
GPIO/ IRQ/ PLL_OUT	IO/ O/ O	15	General Purpose Input And Output/ Interrupt Output/ PLL Output	GPIO: Input/Output IRQOUT: Output PLL_OUT: Output
SCLK	I	16	I^2C Clock	Schmitt trigger
SDA	IO	17	I^2C Data	Schmitt trigger
				Total: 8 Pins

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
MIC1P	I	1	First Mic Positive Input	Analog Input (1Vrms)
MIC1N	I	2	First Mic Negative Input	Analog Input (1Vrms)
LINE_IN_L/JD1	I	3	Line Input Left Channel/Jack Detect Input_1	Analog Input (1Vrms)
MIC2P	I	4	Second Mic Positive Input	Analog Input (1Vrms)
MIC2N	I	5	Second Mic Negative Input	Analog Input (1Vrms)
LINE_IN_R/JD2	I	6	Line Input Right Channel/Jack Detect Input_2	Analog Input (1Vrms)
AUXIN_L	I	19	Auxiliary Input Left Channel	Analog Input (1Vrms)
AUXIN_R	I	20	Auxiliary Input Right Channel	Analog Input (1Vrms)
AUXOUT_L/ MONO_OUT	O	21	Positive Mono Output/Auxiliary Output Left Channel	Analog Output (1Vrms)
AUXOUT_R/ MONO_OUT_N	O	22	Negative Mono Output/Auxiliary Output Right Channel	Analog Output (1Vrms)
LINE_OUT	O	23	LINE Output	Analog Output(1Vrms)
LINE_OUT_N	O	25	Negative LINE Output	Analog Output (1Vrms)
HP_OUT_R	O	29	Headphone Output Right Channel	Analog Output (1Vrms)
HP_OUT_L	O	30	Headphone Output Left Channel	Analog Output (1Vrms)
				Total: 14 Pins

6.3. Filter/Reference

Table 3. Filter/Reference

Name	Type	Pin	Description	Characteristic Definition
NC/Cdepop	IO	18	NC/De-Pop Capacitor	0.1µf capacitor to analog ground
VREF	O	27	Internal Reference Voltage	4.7µf capacitor to analog ground
MICBIAS	O	32	MIC BIAS Voltage Output	Programmable Analog DC output with 3mA drive
				Total: 3 Pins

6.4. Power/Ground

Table 4. Power/Ground

Name	Type	Pin	Description	Characteristic Definition
DGND	P	12	Digital GND	-
DCVDD	P	13	Digital VDD	1.71V~3.6V (Core)
DBVDD	P	14	Digital VDD	1.71V~3.6V (IO Buffer)
AGND2	P	24	Analog GND	-
AVDD2	P	26	Analog VDD	2.3V~3.6V
AGND	P	28	Analog GND	-
AVDD	P	31	Analog VDD	2.3V~3.6V
Exposed_GND	P	Exposed Pad	Exposed GND Must be connected to system DGND	-
				Total: 8 Pins

Note: DBVDD ≥ DCVDD. AVDD2 = AVDD ≥ DCVDD.

7. Functional Description

7.1. Power

The ALC5623 has many power blocks. AVDD and AVDD2 operates between 2.3V and 3.6V. DBVDD and DCVDD operate between 1.71V and 3.6V. The ALC5623 must handle ratio control between the different power blocks. The power supplier limit conditions are DBVDD ≥ DCVDD, and AVDD2 ≥ AVDD ≥ DCVDD.

7.2. Reset

There are two types of reset operation: Power-On Reset (POR) and Register reset.

Table 5. Reset Operation

Reset Type	Trigger Condition	CODEC Response
POR	Monitor digital power supply voltage reach V_{POR}	Power-On Reset. Resets all hardware logic and all registers to default values.
Register Reset	Write Reg-00h	Resets all registers to default values except PLL related register

7.2.1. Power-On Reset (POR)

When powered on, DCVDD passes through the V_{POR} band of the ALC5623 (V_{PORH}~V_{PORL}). A Power-On Reset (POR) will generate an internal reset signal (POR reset 'LOW') to reset the whole chip.

Table 6. Power-On Reset Voltage

Symbol	Min	Typical	Max	Unit
V_{POR_ON}	1.0	-	1.6	V
V_{POR_OFF}	-	1.3	-	V

Note: V_{POR_OFF} must be below V_{POR_ON}.

7.3. Clocking

The Audio SYSCLK can be selected from MCLK or PLL. The PLL clock source can be selected from MCLK or BCLK. The ALC5623 only supports 256Fs or 384Fs as Audio SYSCLK (used as Stereo I²S clock).

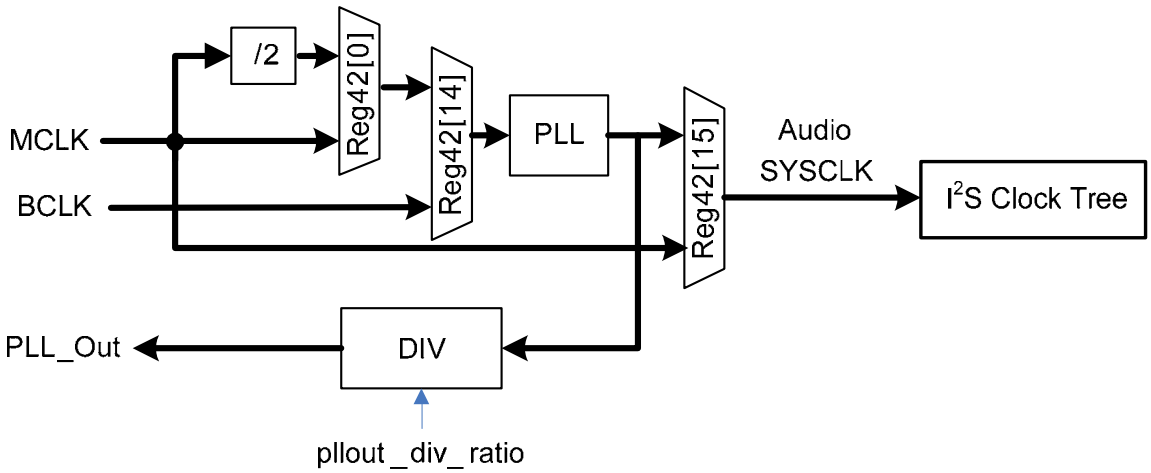


Figure 4. Audio SYSCLK

7.3.1. Phase-Locked Loop

A Phase-Locked Loop (PLL) is used to provide a flexible input clock from 2.048MHz to 40MHz. Typical choices are 2.048MHz, 4.096MHz, and 13MHz. The source of the PLL can be set to MCLK or BCLK by setting pll_sour_sel (Reg42[14]).

The source clock of MCLK must be able to drive I²C, and F/W can setup PLL to output the desired frequency as the SYSCLK.

The PLL transmit formula is: F_{OUT} = (MCLK * (N+2)) / ((M+2) * (K+2)) {Typical K=2}

Table 7. Clock Setting Table for 48K (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	66	7	98.222	2	24.555
3.6864	78	1	98.304	2	24.576
2.048	94	0	98.304	2	24.576
4.096	70	1	98.304	2	24.576
12	80	8	98.4	2	24.6
15.36	81	11	98.068	2	24.517
16	78	11	98.462	2	24.615
19.2	80	14	98.4	2	24.6
19.68	78	14	98.4	2	24.6

Table 8. Clock Setting Table for 44.1K (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	68	8	91	2	22.75
3.6864	72	1	90.931	2	22.733
2.048	86	0	90.112	2	22.528
4.096	64	1	90.112	2	22.528
12	66	7	90.667	2	22.667
15.36	63	9	90.764	2	22.691
16	66	10	90.667	2	22.667
19.2	64	12	90.514	2	22.629
19.68	67	13	90.528	2	22.632

After a Cold Reset, PLL related Registers are reset to default values, however, they are not reset to default values after a soft-reset (write Reg00).

7.3.2. I²S Stereo Data Interface

The ALC5623 supports the I²S digital interface for Stereo Audio. The stereo audio digital interface is used to input data to the stereo DAC or output data from the stereo ADC. The Stereo Audio Digital Interface can be configured as Master mode or Slave mode. For the Stereo I²S Interface, the source system clock is always input from MCLK. Refer to section 12 Appendix A: Stereo I²S Clock Table, page 65 for details.

Master Mode

In master mode (stereo_i2s_mode_sel=0), BCLK and LRCK are configured as output. When sel_sysclk=0, MCLK is used as Stereo SYSCLK. When PLL is enabled and sel_sysclk=1, MCLK is suggested to provide frequencies shown in Table 7 Clock Setting Table for 48K (Unit: MHz) and Table 8 Clock Setting Table for 44.1K (Unit: MHz). PLL can be configured to support 44.1K and 48K base sampling rate.

Slave Mode

In slave mode (stereo_i2s_mode_sel=1), BCLK/LRCK is configured as input. MCLK should provide the BCLK synchronized clock externally as the Stereo_SYSCLK.

Note: The ALC5623 does not support different sample rates between SDAC and SADC in Stereo_I2S/PCM.

7.4. Digital Data Interface

7.4.1. Stereo I²S/PCM Interface

The stereo I²S/PCM interface can be configured as Master mode or Slave mode. Four audio data formats are supported:

- PCM mode
- Left justified mode
- Right justified mode
- I²S mode

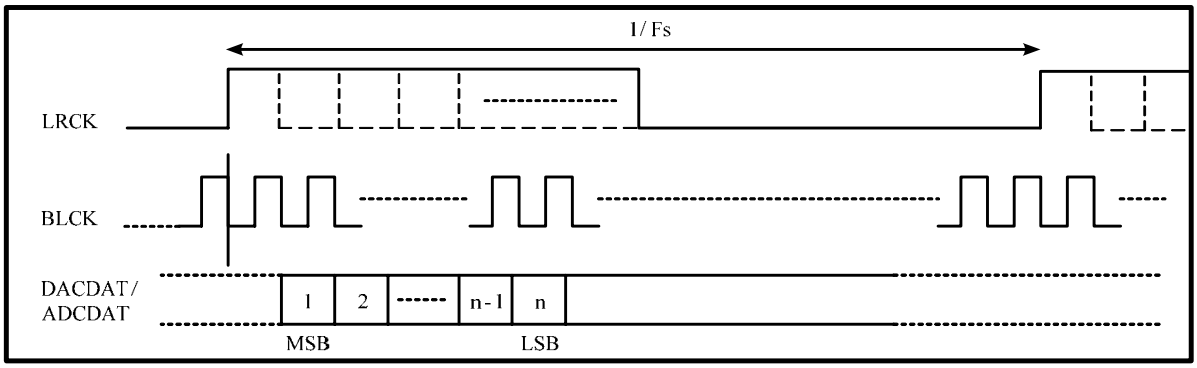


Figure 5. PCM Mono Data Mode A Format (stereo_i2s_bclk_polarity_ctrl=0, pcm_mode_sel=0)

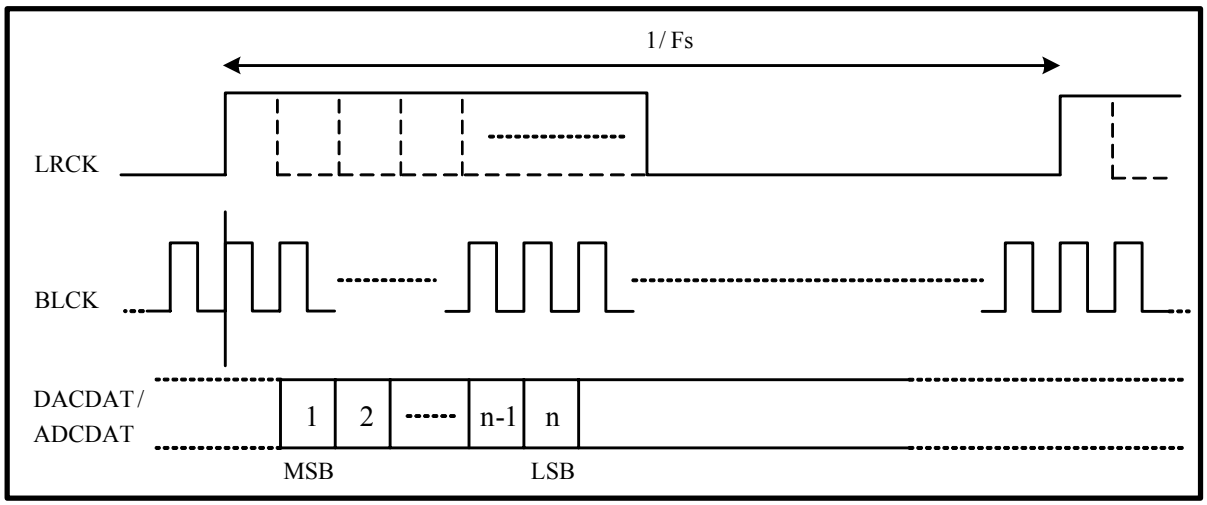


Figure 6. PCM Mono Data Mode A Format (stereo_i2s_bclk_polarity_ctrl=1, pcm_mode_sel=0)

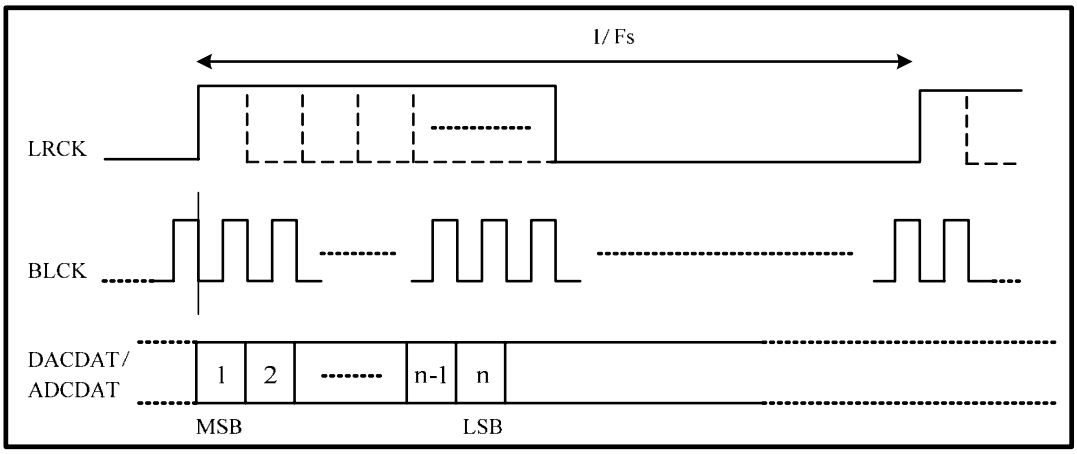


Figure 7. PCM Mono Data Mode B Format (stereo_i2s_bclk_polarity_ctrl=0, pcm_mode_sel=1)

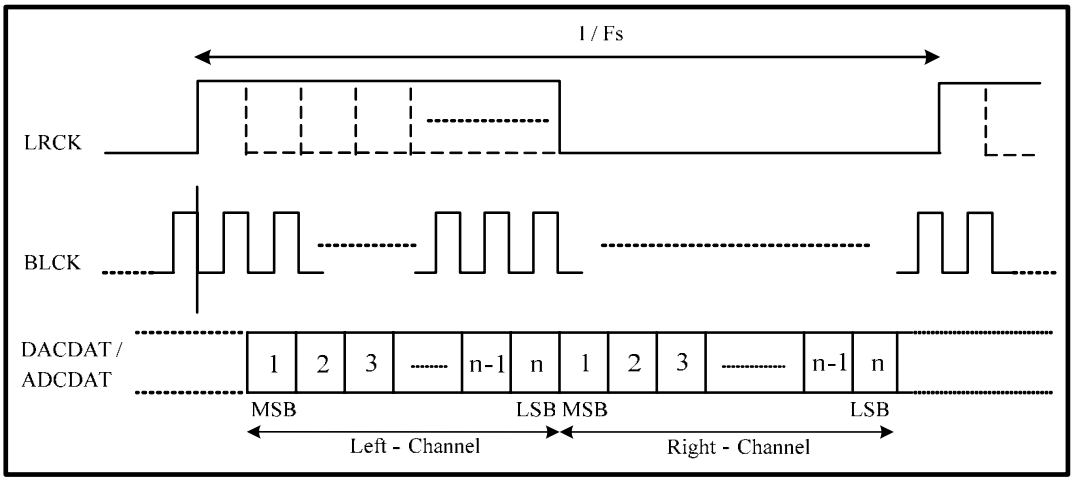


Figure 8. PCM Stereo Data Mode A Format (stereo_i2s_bclk_polarity_ctrl=0, pcm_mode_sel=0)

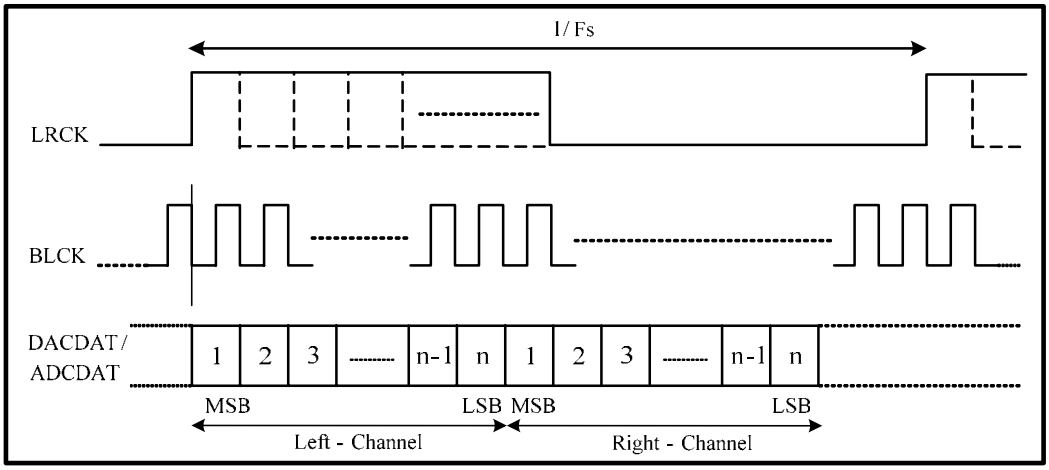


Figure 9. PCM Stereo Data Mode B Format (stereo_i2s_bclk_polarity_ctrl=0, pcm_mode_sel=1)

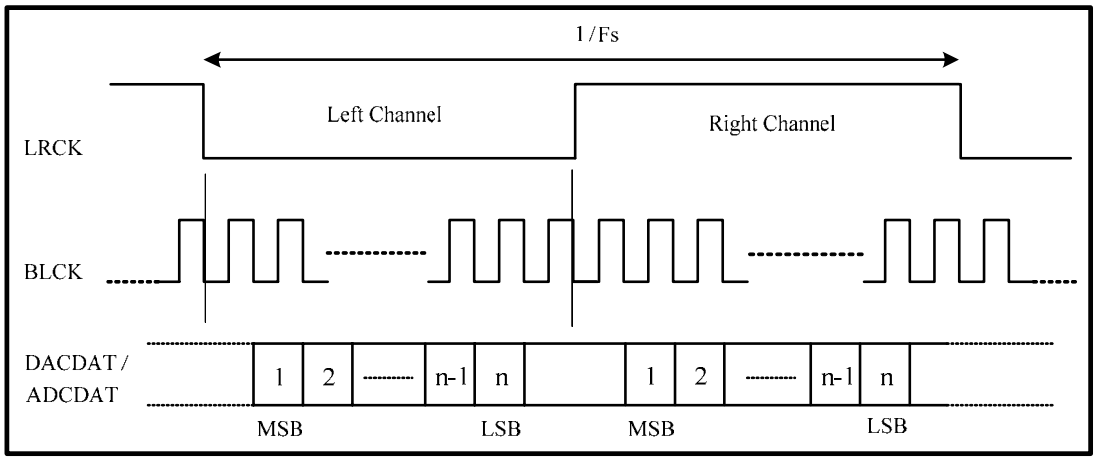


Figure 10. I²S Data Format (stereo_i2s_bclk_polarity_ctrl=0)

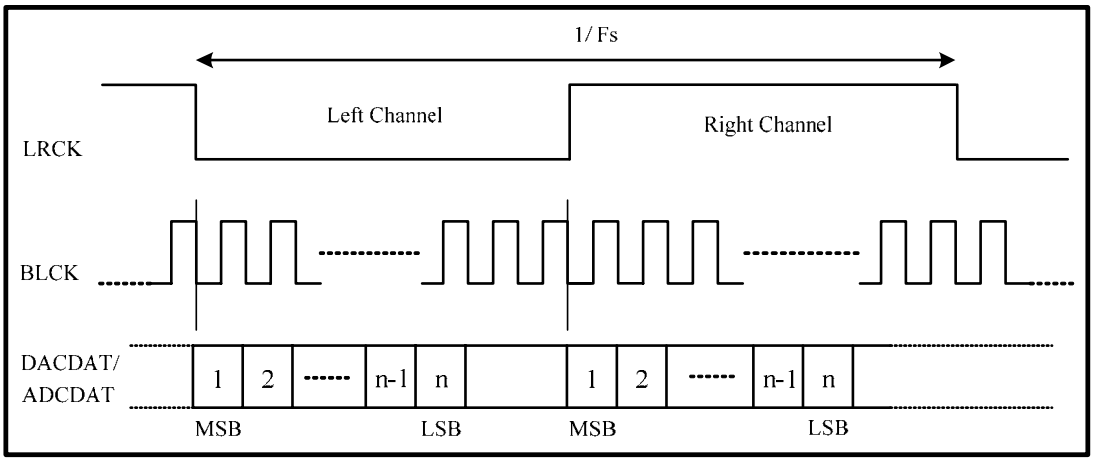


Figure 11. Left Justified Data Format (stereo_i2s_bclk_polarity_ctrl=0)

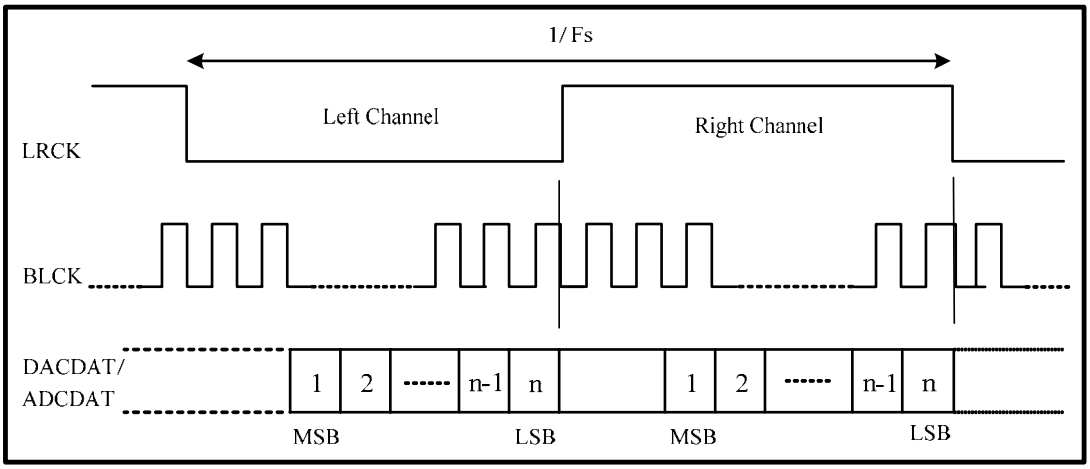


Figure 12. Right Justified Data Format (stereo_i2s_bclk_polarity_ctrl=0)

7.5. Audio Data Path

7.5.1. Vref

Vref is the reference voltage for all analog blocks. An external 1µF Capacitor connected to AGND is required. The default status of Vref is enabled after power on. Driver can set Index-39[11]=0b in order to enable power control bit of Reg-3C[13]:pow_vref.

7.5.2. Stereo ADC

The stereo ADC is used for recording stereo sound. The sample rate of the stereo ADC is independent of the stereo DAC sample rate. In order to save power, the left and right ADC can be powered down separately by setting adc_l_vol and adc_r_vol

The sample rate of the Stereo ADC is the same as the sample rate of Stereo DAC (described in the following section).

7.5.3. Stereo DAC

The stereo DAC can be configured to different sample rates by driving 256Fs/384Fs into audio SYSCLK with setting divider properly (Reg36). adda_osr is used to control the over sample rate clock divider of the DA filter to 128Fs or 64Fs.

Performance of 128Fs is better than 64Fs but with much higher power consumption. Refer to section 12 Appendix A: Stereo I^{2}S Clock Table, page 65 for detailed settings.

dac_l_vol & dac_r_vol can be used to control the DAC output volume.

7.6. Mixers

The ALC5623 supports four mixers for all audio function requirements:

- Headphone mixer for 2 channels
- MONO mixer
- Speaker mixer
- ADC record mixer

7.6.1. Headphone Mixer

The headphone mixer is used to drive stereo output, including HP_OUT_L/R, LINE_OUT, and MONO_OUT (AUXOUT_L/R). The output of the headphone mixer can be input to the ADC record mixer.

The following signals can be mixed into the headphone mixer:

- LINE-IN_L/R (Controlled by Reg0A)
- AUXIN_L/R (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Stereo DAC output (Controlled by Reg0C)
- ADC record mixer output (Controlled by Reg12 & Reg14).

When the LINE_OUT source is from the HP_mixer, LINE_OUT can be configured to L/R, L+R, and L/LN by setting lio_outn_source. The HP mixer can be powered down by setting pow_mix_hp_l and pow_mix_hp_r.

7.6.2. MONO Mixer

The MONO mixer is used to drive MONO_OUT (AUXOUT_L/R) and LINE_OUT. The output of the MONO mixer can be input to the ADC record mixer. The output of the MONO mixer is two channels with the same signal.

The following signals can be mixed into the MONO mixer:

- LINE-IN_L/R (Controlled by Reg0A)
- AUXIN_L/R (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)

- Stereo DAC output (Controlled by Reg0C)
- ADC record mixer output (Controlled by Reg12 & Reg14).

Note: The MONO mixer can be powered down by setting pow_mix_mono.

7.6.3. Speaker Mixer

The speaker mixer is the same as the MONO mixer and is used to drive MONO_OUT (AUXOUT_L/R) and LINE_OUT. The output of the speaker mixer can be input to the ADC record mixer. The output of the speaker mixer is two channels with the same signal.

The following signals can be mixed into the speaker mixer:

- LINE-IN_L/R (Controlled by Reg0A)
- AUXIN_L/R (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22 & Reg10)
- Stereo DAC output (Controlled by Reg0C)

Note: The speaker mixer can be powered down by setting pow_mix_spk.

7.6.4. ADC Record Mixer

The ADC record mixer is used to mix analog signals as input to the Stereo ADC for recording. Output of the ADC record mixer can be input to the headphone mixer, MONO mixer, and speaker mixer.

The following signals can be mixed into the ADC record mixer:

- LINE-IN_L/R (Controlled by Reg0A)
- AUXIN_L/R (Controlled by Reg08)
- MIC1P/N and MIC2P/N (Controlled by Reg22)
- Headphone mixer output
- MONO mixer output
- Speaker mixer output

Note: The ADC record mixer can be powered down by setting pow_mix_adc_rec_l & pow_mix_adc_rec_r.

7.7. Analog Audio Input Path

The ALC5623 supports four Analog Audio Input paths:

- Line_IN_L/R
- AUXIN_L/R
- MIC1
- MIC2

7.7.1. Line Input

LINE_IN_L and LINE_IN_R provide 2-channel stereo single-ended input that can be mixed into any analog output mixer and ADC record mixer.

The LINE_IN_L/R volume and mute are controlled by Reg0A.
pow_li_l_vol and pow_li_r_vol can be used to power down LINE_IN volume control.

LINE_IN_L is pin shared to JD1 and can be configured by lineinl_pin_sharing.
LINE_IN_R is pin shared to JD2 and can be configured by lineinr_pin_sharing.

7.7.2. AUXiliary Input

AUXIN_L and AUXIN_R provide 2-channel stereo single-ended input that can be mixed into the ADC record mixer and any analog output mixer.

AUXIN_L/R volume and mute are controlled by Reg08.
pow_auxin_l_vol and pow_auxin_r_vol can be used to power down AUXIN_L/R volume control.

7.7.3. Microphone Input

MIC1P/N and MIC2P/N provide 2-channel stereo differential or single-ended input, via mic1_diff_ctrl and mic2_diff_ctrl, that can be mixed into the ADC record mixer, or any analog output mixer. MIC1P and MIC2P are main inputs when differential mode is disabled.

The ALC5623 microphone input boost provides 20/30dB boost, set by mic1_boost_ctrl (for MIC1) and mic2_boost_ctrl (for MIC2). The MIC1/2 volume and mute are controlled by Reg0E.

pow_mic1_vol & pow_mic2_vol can be used to power down the MIC1/2 volume control path.
pow_mic1_admixer & pow_mic2_admixer can be used to power down the MIC1/2 admixer path.

7.8. Analog Audio Output Data Path

The ALC5623 supports three Analog Audio output paths:

- LINE_OUT
- HP_OUT_L/R
- MONO_OUT (AUX_OUT_L/R).

7.8.1. LINE Output

LINE_OUT provides one channel mono Differential output and can be configured to two-channel stereo single-ended output

The LINE_OUT source is selected in lio_vol_in_sel. Sources are shown below:

- Vmid
- Headphone left mixer
- Speaker mixer
- MONO mixer

The LINE_OUT volume and mute are controlled by Reg02. Also, Reg3E[12]: pow_lineout can be used to power down LINE output. pow_LineOut_amp (Reg3C[15]) is used to power down the Line Out Amplifier.

LINE_OUT supports a softmute function and a zero cross detect function which can be enable at lio_l_soft-mute_en/lio_r_soft-mute_en and lio_l_dezero/lio_r_dezero depends on the setting of lio_vol_in_sel. If LINE_OUT is configured to differential, only lio_l_soft-mute_en and lio_l_dezero can be used to control softmute and zero cross of LINE_OUT.

7.8.2. Headphone Output

HP_OUT_L/R provides stereo single-ended output. The source of HP_OUT_L/R can be selected from hp_l_in_sel & hp_r_in_sel (Reg1C[9:8]).

- Vmid
- Headphone mixer

The HP_OUT_L/R volume and mute are controlled by Reg04.

pow_hp_l_vol (Reg3E[10]) and pow_hp_r_vol (Reg3E[9])can be used to power down the HP output volume

HP_OUT supports soft-mute and zero cross detect function, which can be individually enabled at hp_l_softmute_en/ hp_r_softmute_en and hp_l_dezero/ hp_r_dezero

7.8.3. MONO Output

MONO_OUT provides one-channel differential MONO_OUT or stereo single-ended AUXOUT_L/R via se_diff_auxout.

The MONO/AUXOUT source can be selected from Reg1C[7:6], mono_in_sel. Sources are shown below.

- Vmid
- Headphone mixer (L+R)
- Speaker mixer
- MONO mixer

The MONO/AUXOUT output signal depends on the setting of se_diff_auxout & mono_in_sel.

Table 9. MONO/AUXOUT Output Signal Table

mono_in_sel	se_diff_auxout	MONO/AUXOUT Output Signal
Vmid	Differential Mode	Vmid
	Single-Ended Mode	Vmid
HP mixer (L/R)	Differential Mode	L/LN
	Single-Ended Mode	L/R
Speaker mixer (L+R)	Differential Mode	(L+R)/(L+R)N
	Single-Ended Mode	(L+R)/(L+R)
MONO mixer	Differential Mode	(L+R)/(L+R)N
	Single-Ended Mode	(L+R)/(L+R)

MONO/AUXOUT volume and mute are controlled by Reg08.

pow_aux_outl_vol (Reg3E[14]) and pow_aux_outr_vol (Reg3E[13])can be used to power down the volume of MONO/AUXOUT.

If MONO/AUXOUT is configured to stereo single-ended AUXOUT, the soft-mute and zero cross detect function of MONO/AUXOUT can be enabled at AUXO_l_softmute_en/AUXO_r_softmute_en and AUXO_l_dezero/AUXO_r_dezero.

If MONO/AUX is configured to mono differential MONO_OUT, only AUXO_l_softmute_en and AUXO_l_dezero can be used to control soft-mute and zero cross of MONO/AUXOUT.

7.9. AVC Control

The Automatic Volume Control (AVC) function dynamically adjusts the input signal quantized by the ADC to an expected sound level by setting THmax, THmin, and THnonact (see Figure 14 AVC Behavior, page 22.

When the average level of input signal is higher than THmax, the AVC will decrease the selected analog gain to attenuate the quantized Pulse Code Modulation (PCM) signal to a lower amplitude than THmax.

When the average level of input signal is lower than THmin and higher than Thnonact., the AVC will increase the selected analog gain to amplify the input signal. The quantized Pulse Code Modulation (PCM) signal is then set to a higher amplitude than THmin. The quantized PCM has an average level between THmin and THmax.

In order not to output a strong amplified signal when the gain detector input level is transiting from a very small signal to a normal signal, the AVC block will limit the selected analog gain to unit gain (=0dB) when the input level of the gain detector is lower than THnonact.

The AVC reference source channel and target channel can be individually set by Reg68: AVC Control.

The AVC block diagram and behavior is shown in Figure 13 and Figure 14, respectively.

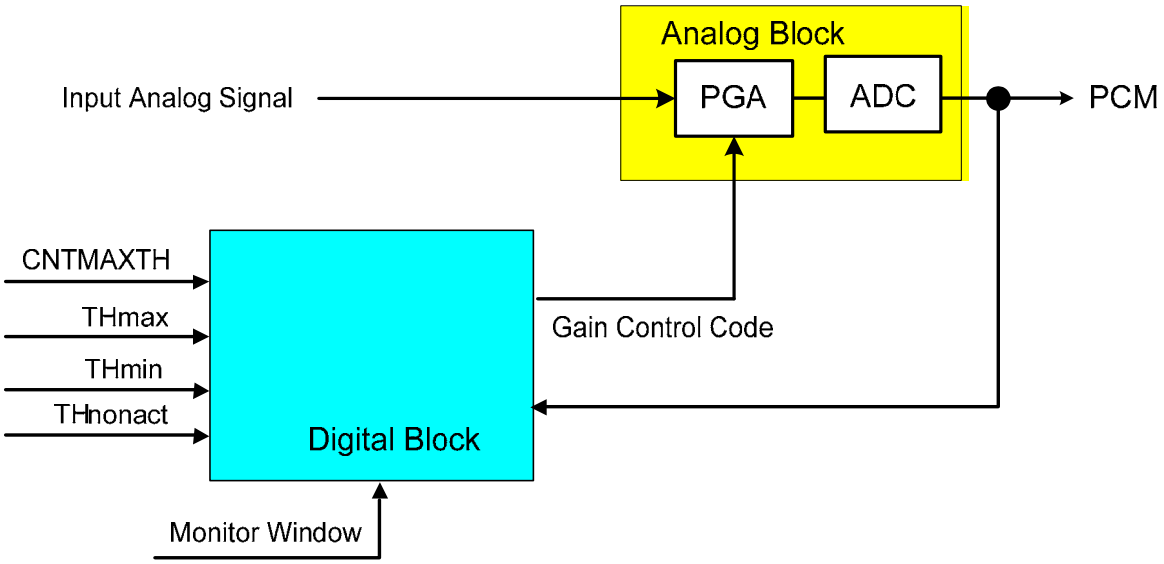


Figure 13. Auto Volume Control Block Diagram

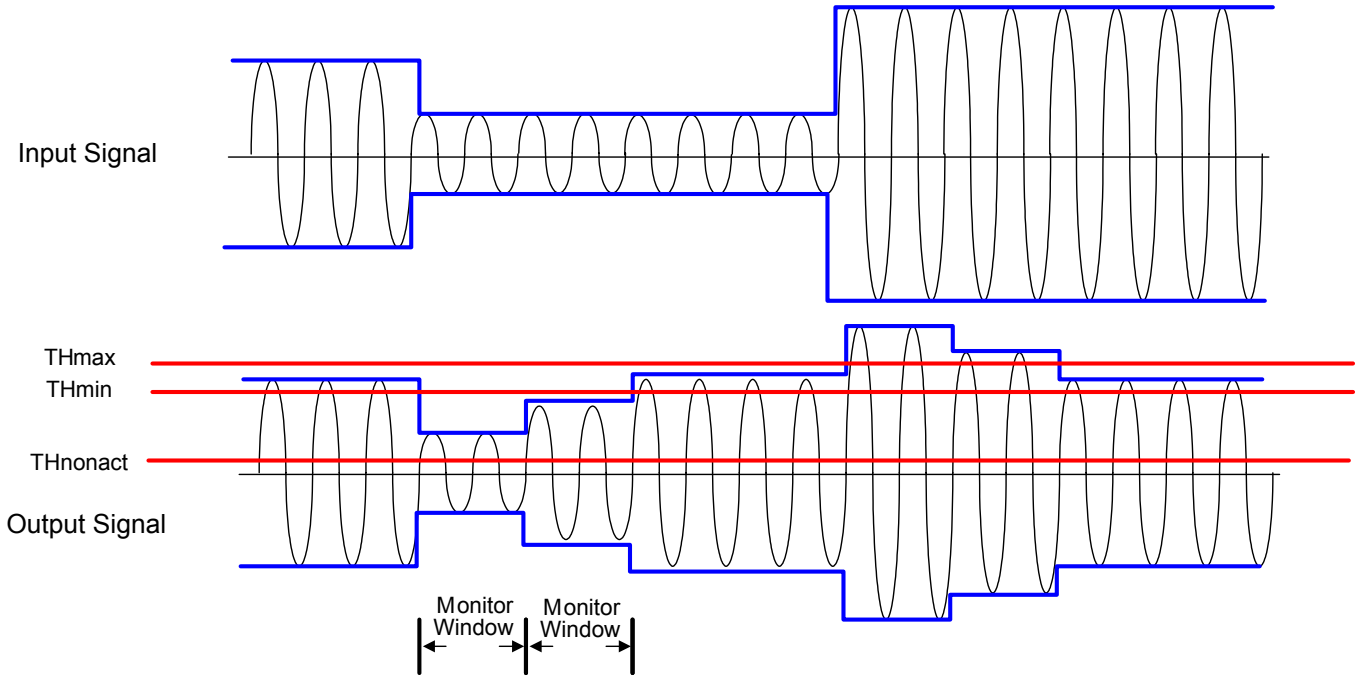


Figure 14. AVC Behavior

7.10. Hardware Sound Effects

The Sound Effect block is composed of Pseudo Stereo, Spatial 3D, and Equalizer blocks. The Pseudo Stereo block is used to convert a MONO source into virtualized stereo output. The Spatial 3D block is a surround sound generator with adjustable amplitude (Gain) and surround depth (Ratio). The Equalizer block can be used to compensate for speaker response, or to make environment sound effects, e.g., 'Pub', 'Live', 'Rock',… etc..

7.10.1. Equalizer Block

The Equalizer block cascades 5 bands of equalizer to compensate for speaker response and to emulate environment sound. One high-pass filter cascaded in the front end is used to drop low frequency tone, which has a larger amplitude and may damage a mini speaker.

The high-pass filter can also be used to adjust Treble strength with gain control. A low-pass filter with gain control can adjust the Bass strength. Three bands of bi-quad bandpass filters are used to emulate environment sounds.

To avoid PCM sample saturation, a digital volume control has 0 ~18dB attenuation in the front of equalizer is required. A –3~+18dB digital gain control after equalizer is used to compensate PCM output to suitable level.

The Equalizer source of the ALC5623 can be selected from DAC or ADC. If Equalizer parameters will be dynamically changed, the driver should set EQ Mode Change enable and disable after the EQ parameters have been set to new values.

7.10.2. Pseudo Stereo and Spatial 3D Sound

There are two spatial effects in post-processing; the Pseudo-Stereo Effect + Spatial Effect, and the Stereo Expansion Effect. The Pseudo-Stereo Effect + Spatial Effect converts a MONO signal to a stereo signal by changing the phase and amplitude of the original signal followed by enhancing the spatial effect. The Stereo Expansion Effect enhances the spatial effect when the input signal is Stereo.

7.11. I²C Control Interface

I²C is a 2-wire half-duplex serial communication interface, supporting only slave mode. The host must support MCLK during register access.

7.11.1. Addressing Setting

Table 10. Addressing Setting

(MSB)			BIT				(LSB)
0	0	1	1	0	1	0	RW

7.11.2. Complete Data Transfer

Data Transfer over I²C Control Interface

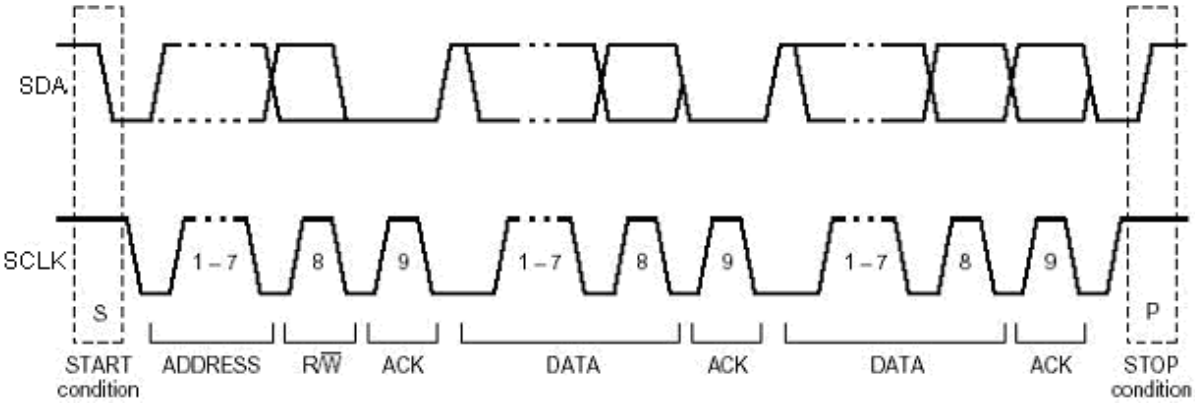


Figure 15. Data Transfer Over I²C Control Interface

Write WORD Protocol

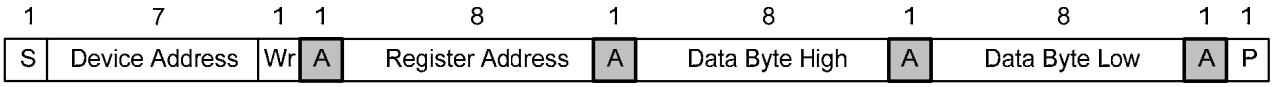
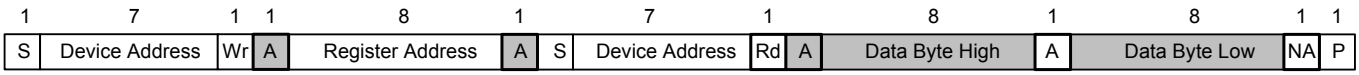


Figure 16. Write WORD Protocol

Read WORD Protocol



S: Start Condition
A: 0 for ACK, 1 for NACK
Slave Address: 7-bit Device Address
Data Byte: 16-bit Mixer data
Wr: 0 for Write Command
☐: Master-to-Slave
Rd: 1 for Read Command
☐: Slave-to-Master
Command Code: 8-bit Register Address

Figure 17. Read WORD Protocol

7.12. Odd-Addressed Register Access

The ALC5623 will return '0000h' when odd-addressed and unimplemented registers are read.

7.13. Power Management

The ALC5623 supports a grouped power down control register (Reg26). More detailed Power Management control is supported in Reg 3A, 3C, and 3E. Each particular block will only be active when both Reg26 and Reg3A/3C/3E are set to 'Enable'.

7.14. GPIO and Jack Detect Function

The GPIO pin of the ALC5623 can be configured to PLL_OUT and IRQ_Output by setting Reg-56[1:0]: gpio_pin_sharing.

The ALC5623 supports one GPIO that can be configured as Input/Output by Reg4C when gpio_pin_sharing =00'b. When the GPIO is configured as Input, the status will be indicated in Reg54[1]. When the GPIO is configured as Output, Reg5C[1] is used to drive GPIO to High (1b) or Low (0b). The status can be read in Reg54[1].

In addition, the ALC5623 supports Jack Detect (JD1/JD2) to switch ON/OFF the Analog Output (Headphone Out, LINE Out, and AUXOUT_L/R).

JD1 and JD2 can be pin-shared from LINE_IN_R/L and are used to enable specified Analog audio output configured in the Reg-5Ah Jack Detect Control Register.

GPIO & JD input can be configured as sticky by setting Reg50, change polarity by setting Reg4E, and wake-up by setting Reg52 in order to generate the interrupt (IRQ). The driver can write each bit of Reg54 to '1' to clear each IRQ status flag.

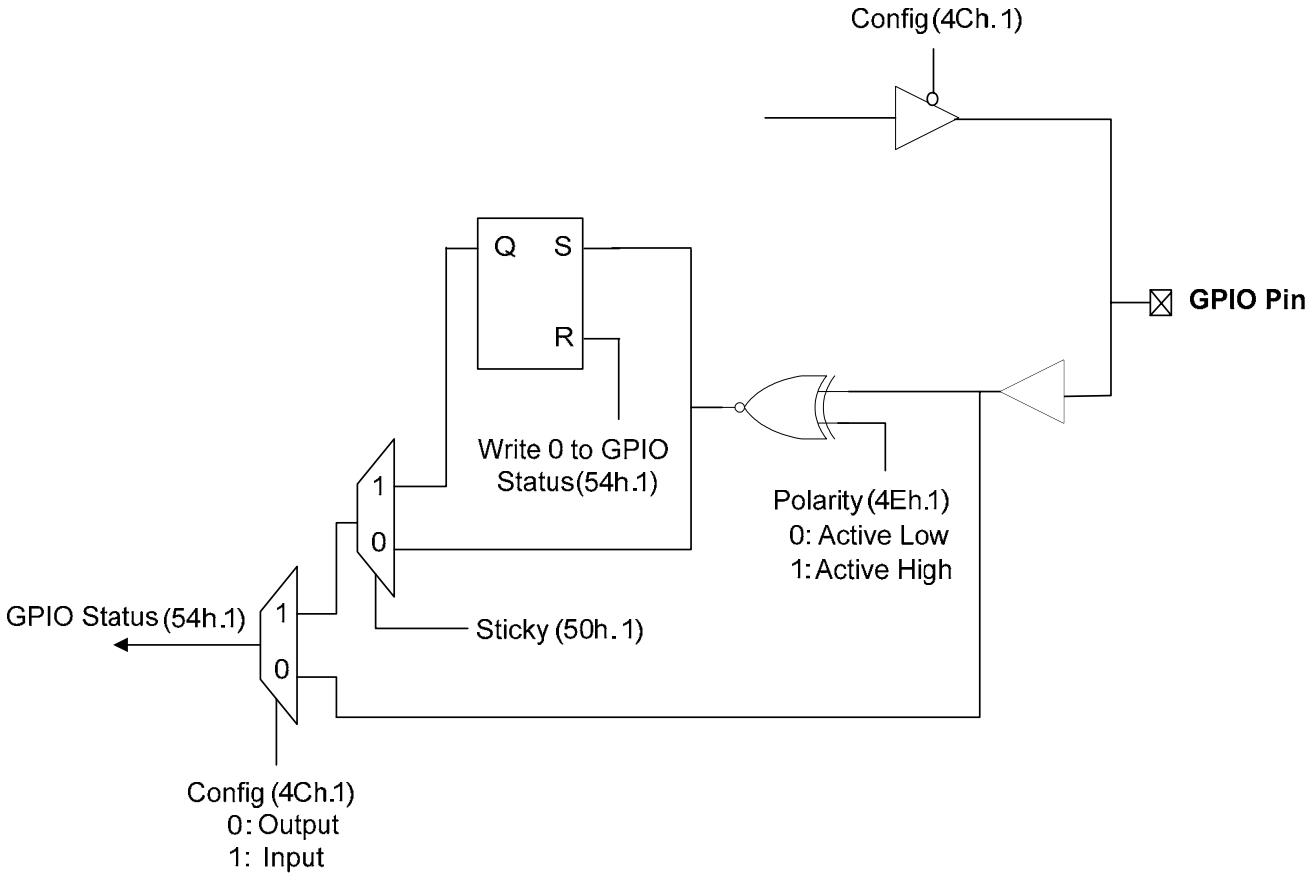


Figure 18. GPIO Implementation

7.15. Internal Event Signal Interrupt

Independent of GPIOs, an Internal Event Signal (MICBIAS short detect) is handled the same as a Jack Detect and is treated as an Interrupt source. The application of an Internal Event Signal is the same as that of a GPIO.

Interrupt request (IRQ) can be configured as:

- Sticky by setting Reg50
- Changed polarity by setting Reg4E
- Wake-up by setting Reg52

The driver can write each bit of Reg54 to '1' to clear each IRQ status flag.

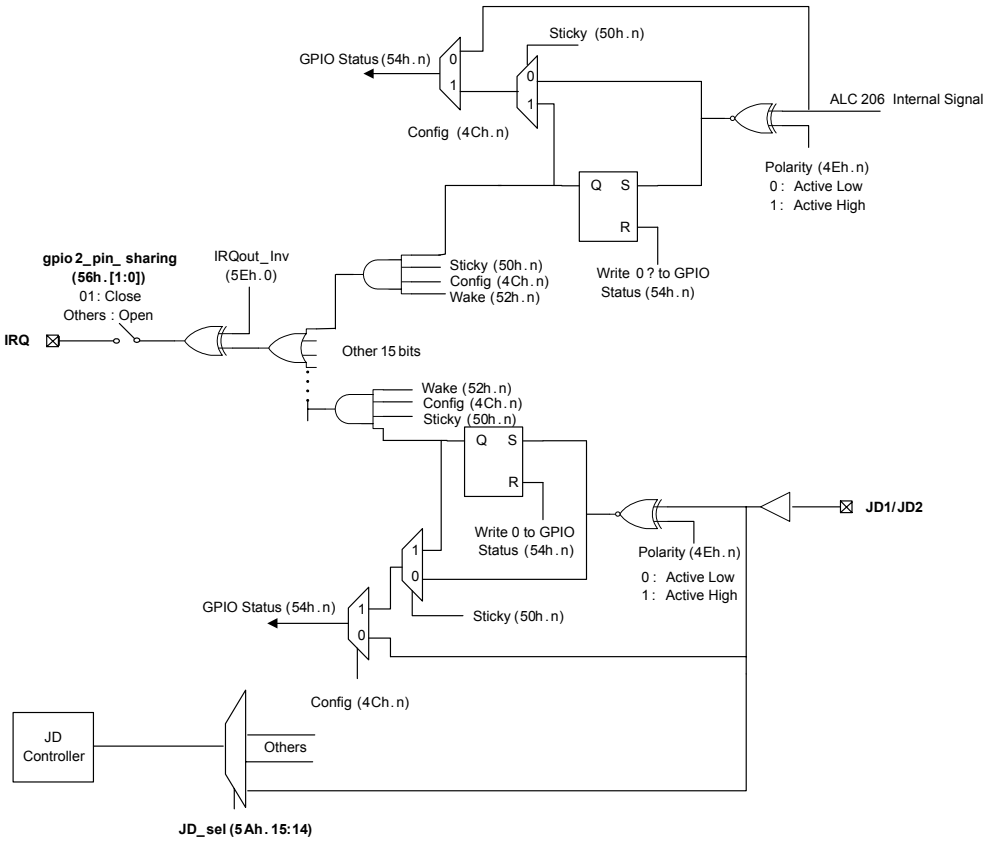


Figure 19. Jack Detect and IRQ Logic

7.16. Headphone Depop

The ALC5623 provides a headphone depop mechanism in order to eliminate the pop noise of headphone out. An external 1µF Capacitor is required in this application. Refer to the ALC5623 Application Note for details.

8. Mixer Registers List

Accessing odd numbered registers, or reading unimplemented registers, will return a 0.

8.1. Reg-00h: Reset

Default: 59B4h

Table 11. Reg-00h: Reset

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0'h	Reserved. Read as 0
REG-00_b14_b10	14:10	R	16'h	SE[4:0]=10110b
REG-00_b9	9	R	0'h	No Support for 20-Bit ADC
REG-00_b8	8	R	1'h	Supports 16-Bit ADC
REG-00_b7	7	R	1'h	Supports 16-Bit DAC
REG-00_b6	6	R	0'h	No Support for 18-Bit DAC
REG-00_b5	5	R	1'h	Support for Loudness
REG-00_b4	4	R	1'h	Headphone Output Support
Reserved	3	R	0'h	Reserved
REG-00_b2	2	R	1'h	Supports EQ Control
Reserved	1	R	0'h	Reserved. Read as 0
REG-00_b0	0	R	0'h	Dedicated MIC PCM Input is Not Supported

Note: Writes to this register will reset all registers to their default values except PLL related registers. The written data will be ignored.

8.2. Reg-02h: Line Output Volume

Default: 8080h

Table 12. Reg-02h: Line Output Volume

Name	Bits	Read/Write	Reset State	Description
lio_l_mute	15	RW	1'h	Mute LINE_OUT Left Control 0: On 1: Mute (-∞ dB)
lio_l_dezero	14	RW	0'h	LINE_OUT Left Zero Cross Detector Control 0: Disable 1: Enable
lio_l_soft-mute_en	13	RW	0'h	LINE_OUT Left_Softmute Enable 0: Disable 1: Enable
lio_l_vol	12:8	RW	0'h	LINE_OUT Left Output Volume (LIOL[4:0]) in 1.5dB steps

Name	Bits	Read/Write	Reset State	Description
lio_r_mute	7	RW	1'h	Mute LINE_OUT Right Control 0: On 1: Mute (-∞ dB) *Note: Not used when in differential mode (Reg1C[11:10])*
lio_r_dezero	6	RW	0'h	LINE_OUT Right Zero Cross Detector Control 0: Disable 1:Enable *Note: Not used when in differential mode (Reg1C[11:10])*
lio_r_soft-mute_en	5	RW	0'h	LINE_OUT Right_Softmute Enable 0: Disable 1: Enable *Note: Not used when in differential mode (Reg1C[11:10])*
lio_r_vol	4:0	RW	0'h	LINE_OUT Right Output Volume (LIOR[4:0]) in 1.5dB Steps *Note: Not used when in differential mode (Reg1C[11:10])*

Note: For LIOR/LIOL, 00h: 0dB attenuation 1Fh: 46.5dB attenuation

8.3. Reg-04h: Headphone Output Volume

Default: 8080h

Table 13. Reg-04h: Headphone Output Volume

Name	Bits	Read/Write	Reset State	Description
hp_l_mute	15	RW	1'h	Mute HP Left Control 0: On 1: Mute Left Channel (-∞ dB)
hp_l_dezero	14	RW	0'h	HP Left Zero Cross Detector Control 0: Disable 1: Enable
hp_l_soft-mute_en	13	RW	0'h	HP Left Channel Softmute Enable 0: Disable 1: Enable
hp_l_vol	12:8	RW	0'h	Headphone Output Left Volume (HPL[4:0]) in 1.5dB Steps
hp_r_mute	7	RW	1'h	Mute HP Right Control 0: On 1: Mute Right Channel (-∞ dB)
hp_r_dezero	6	RW	0'h	HP Right Zero Cross Detector Control 0: Disable 1: Enable
hp_r_soft-mute_en	5	RW	0'h	HP Right Channel Softmute Enable 0: Disable 1: Enable
hp_r_vol	4:0	RW	0'h	Headphone Output Right Volume (HPR[4:0]) in 1.5dB Steps

Note: For HPR/HPL, 00h: 0dB attenuation 1Fh: 46.5dB attenuation

8.4. Reg-06h: MONO_OUT/AUXOUT Volume

Default: 8080h

Table 14. Reg-06h: MONO_OUT/AUXOUT Volume

Name	Bits	Read/Write	Reset State	Description
AUXO_l_mute	15	RW	1'h	Mute Left Control 0: On 1: Mute Left Channel (-∞ dB)
AUXO_l_dezero	14	RW	0'h	Left Zero Cross Detector Control 0: Disable 1: Enable
AUXO_l_soft-mute _en	13	RW	0'h	AUXOUT Left Channel Softmute Enable 0: Disable 1: Enable
AUXO_l_vol	12:8	RW	0'h	AUXOUT Output Left Volume (AUXOLV[4:0]) In 1.5dB Steps
AUXO_r_mute	7	RW	1'h	Mute Right Control 0: On 1: Mute Right Channel (-∞ dB) *Note: Not used when in differential mode*
AUXO_r_dezero	6	RW	0'h	Right Zero Cross Detector Control 0: Disable 1: Enable *Note: Not used when in differential mode*
AUXO_r_soft-mute _en	5	RW	0'h	AUXOUT Right Channel Softmute Enable 0: Disable 1: Enable *Note: Not used when in differential mode*
AUXO_r_vol	4:0	RW	0'h	AUXOUT Output Right Volume (AUXORV[4:0]) in 1.5dB Steps *Note: Not used when in differential mode*

Note: For AUXOL/R, 00h: 0dB attenuation 1Fh: 46.5dB attenuation

8.5. Reg-08h: AUXIN Volume

Default: E808h

Table 15. Reg-08h: AUXIN Volume

Name	Bits	Read/Write	Reset State	Description
auxi2hp_mute	15	RW	1'h	Mute AUXIN Volume Output to Headphone Mixer Control 0: On 1: Mute
auxi2spk_mute	14	RW	1'h	Mute AUXIN Volume Output to Speaker Mixer Control 0: On 1: Mute
auxi2mono_mute	13	RW	1'h	Mute AUXIN Volume Output to Mono Mixer Control 0: On 1: Mute
auxi_l_vol	12:8	RW	08'h	AUXIN Left Volume (AUXI LV [4:0]) in 1.5dB Steps
Reserved	7:5	R	0'h	Reserved
auxi_r_vol	4:0	RW	8'h	AUXIN Right Volume (AUXIRV [4:0]) in 1.5dB Steps

Note: For AUXIRV/AUXI LV, 00h: +12dB gain 08h: 0dB attenuation 1Fh: 34.5dB attenuation

8.6. Reg-0Ah: LINE_IN Volume

Default: E808h

Table 16. Reg-0Ah: LINE_IN Volume

Name	Bits	Read/Write	Reset State	Description
li2hp_mute	15	RW	1'h	Mute LINE_IN Volume Output to Headphone Mixer Control 0: On 1: Mute
li2spk_mute	14	RW	1'h	Mute LINE_IN Volume Output to Speaker Mixer Control 0: On 1: Mute
li2MONO_mute	13	RW	1'h	Mute LINE_IN Volume Output to MONO Mixer Control 0: On 1: Mute
li_l_vol	12:8	RW	08'h	LINE_IN Left Volume (NLV[4:0]) in 1.5dB Steps
Reserved	7:5	R	0'h	Reserved
li_r_vol	4:0	RW	8'h	LINE_IN Right Volume (NRV[4:0]) in 1.5dB Steps

Note: For NRV/NLV, 00h: +12dB gain
08h: 0dB attenuation
1Fh: 34.5dB attenuation

8.7. Reg-0Ch: STEREO DAC Volume

Default: E808h

Table 17. Reg-0Ch: STEREO DAC Volume

Name	Bits	Read/Write	Reset State	Description
dac2hp_mute	15	RW	1'h	Mute DAC Volume Output to Headphone Mixer Control 0: On 1: Mute (-∞dB)
dac2spk_mute	14	RW	1'h	Mute DAC Volume Output to Speaker Mixer Control 0: On 1: Mute (-∞dB)
dac2MONO_mute	13	RW	1'h	Mute DAC Volume Output to MONO Mixer Control 0: On 1: Mute (-∞dB)
dac_l_vol	12:8	RW	08'h	PCM Left DAC Volume (PLV[4:0]) in 1.5dB Steps
Reserved	7:5	R	0'h	Reserved
dac_r_vol	4:0	RW	8'h	PCM Right DAC Volume (PRV[4:0]) in 1.5dB Steps

Note: For PRV/PLV, 00h: +12dB gain
08h: 0dB attenuation
1Fh: 34.5dB attenuation

8.8. Reg-0Eh: MIC Volume

Default: 0808h

Table 18. Reg-0Eh: MIC Volume

Name	Bits	Read/Write	Reset State	Description
Reserved	15:13	R	0'h	Reserved
mic1_vol	12:8	RW	08'h	MIC1 Volume (M1V[4:0]) in 1.5dB Steps
Reserved	7:5	R	0'h	Reserved
mic2_vol	4:0	RW	8'h	MIC2 Volume (M2V[4:0]) in 1.5dB Steps

Note: For M2V/M1V, 00h: +12dB gain
08h: 0dB attenuation
1Fh: 34.5dB attenuation

8.9. Reg-10h: MIC Routing Control

Default: E0E0h

Table 19. Reg-10h: MIC Routing Control

Name	Bits	Read/Write	Reset State	Description
mic12hp_mute	15	RW	1'h	Mute MIC1 Volume Output to Headphone Mixer 0: On 1: Mute
mic12spk_mute	14	RW	1'h	Mute MIC1 Volume Output to Speaker Mixer 0: On 1: Mute
mic12MONO_mute	13	RW	1'h	Mute MIC1 Volume Output to MONO Mixer 0: On 1: Mute
mic1_diff_ctrl	12	RW	0'h	MIC1 Differential Input Control 0: Disable 1: Enable
Reserved	11:8	R	0'h	Reserved
mic22hp_mute	7	RW	1'h	Mute MIC2 Volume Output to Headphone Mixer 0: On 1: Mute
mic22spk_mute	6	RW	1'h	Mute MIC2 Volume Output to Speaker Mixer 0: On 1: Mute
mic22MONO_mute	5	RW	1'h	Mute MIC2 Volume Output to MONO Mixer 0: On 1: Mute
mic2_diff_ctrl	4	RW	0'h	MIC2 Differential Input Control 0: Disable 1: Enable
Reserved	3:0	R	0'h	Reserved

8.10. Reg-12h: ADC Record Gain

Default: F58Bh

Table 20. Reg-12h: ADC Record Gain

Name	Bits	Read/Write	Reset State	Description
adc2hp_l_mute	15	RW	1'h	Mute Left Gain Output to Headphone Mixer Control 0: On 1: Mute (-∞dB)
adc2hp_r_mute	14	RW	1'h	Mute Right Gain Output to Headphone Mixer Control 0: On 1: Mute (-∞dB)
adc2MONO_l_mute	13	RW	1'h	Mute Left Gain Output to MONO Mixer Control 0: On 1: Mute (-∞dB)
adc2MONO_r_mute	12	RW	1'h	Mute Right Gain Output to MONO Mixer Control 0: On 1: Mute (-∞dB)
adc_l_vol	11:7	RW	0B'h	ADC Record Gain Left Channel (LRG[4:0]) in 1.5dB Steps 00h: -16.5dB attenuation 0Bh: 0dB gain 1Fh: 30dB gain
adc_l_dezero	6	RW	0'h	ADC_L Zero-Cross Detector Control 0: Disable 1: Enable
adc_r_dezero	5	RW	0'h	ADC_R Zero-Cross Detector Control 0: Disable 1: Enable
adc_r_vol	4:0	RW	0B'h	ADC Record Gain Right Channel (RRG[4:0]) in 1.5dB Steps 00h: -16.5dB attenuation 0Bh: 0dB gain 1Fh: 30dB gain

8.11. Reg-14h: ADC Record Mixer Control

Default: 7F7Fh

Table 21. Reg-14h: ADC Record Mixer Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15	R	0'h	Reserved
adcrec_l_mute	14:8	RW	7F'h	Left Mixer Mute Control 0: On 1: Mute (-∞dB) Bit 14: MIC1 Bit 13: MIC2 Bit 12: LINE_IN_L Bit 11: AUXIN_L Bit 10: Headphone Mixer Left Channel Bit 9: Speaker Mixer Bit 8: MONO Mixer
Reserved	7	R	0'h	Reserved
adcrec_r_mute	6:0	RW	7F'h	Right Mixer Mute Control 0: On 1: Mute (-∞dB) Bit 6: MIC1 Bit 5: MIC2 Bit 4: LINE_IN_R Bit 3: AUXIN_R Bit 2: Headphone Mixer Right Channel Bit 1: Speaker Mixer Bit 0: MONO Mixer

8.12. Reg-16h: Avol Soft Volume Control Time

Default: 0000h

Table 22. Reg-16h: Avol Soft Volume Control Time

Name	Bits	Read/Write	Reset State	Description
Reserved	15:4	R	000'h	Reserved
soft_volume_ctrl_avol	3:0	RW	1010'b	Soft Volume Control Time (Default=1001b) 0000: 1 SVSYNC 0001: 2 SVSYNC 0010: 4 SVSYNC 0011: 8 SVSYNC 0100: 16 SVSYNC 0101: 32 SVSYNC 0110: 64 SVSYNC 0111: 128 SVSYNC 1000: 256 SVSYNC 1001: 512 SVSYNC 1010: 1024 SVSYNC Others: Reserved

Note: SVSYNC=1/Fs, Step:-1.5dBFS

8.13. Reg-1Ch: Output Mixer Control

Default: D000h

Table 23. Reg-1Ch: Output Mixer Control

Name	Bits	Read/Write	Reset State	Description
lio_outn_source	15:14	RW	3'h	LINE_Out_N Source Select 00: RN, lio_vol_in_sel='01'; -(L+R), lio_vol_in_sel='10' or '11' 01: RP, lio_vol_in_sel='01'; L+R, lio_vol_in_sel='10' or '11' 10: LN, lio_vol_in_sel='01'; -(L+R), lio_vol_in_sel='10' or '11' 11: Vmid
Reserved	13:12	RW	1'h	Reserved
lio_vol_in_sel	11:10	RW	00'h	LINE_OUT Volume Output Input Select 00: VMID (No input) 01: HP Mixer 10: Speaker mixer (diff out) 11: MONO Mixer (diff out)
hp_l_in_sel	9	RW	0'h	HPL Volume Output Input Select 0: VMID (No input) 1: HP Left Mixer
hp_r_in_sel	8	RW	0'h	HPR Volume Output Input Select 0: VMID (No input) 1: HP Right Mixer
mono_in_sel	7:6	RW	0'h	MONO/AUX Output Volume Input Select 00: VMID (No input) 01: HP Mixer (AUX→L/R, Mono→L+R) 10: Speaker mixer 11: MONO Mixer
Reserved	5:0	R	0'h	Reserved

8.14. Reg-22h: Microphone Control

Default: 0000h

Table 24. Reg-22h: Microphone Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:12	R	0'h	Reserved
mic1_boost_ctrl	11:10	RW	0'h	MIC1 Boost Control 00: Bypass 01: +20dB 10: +30dB 11: Reserved
mic2_boost_ctrl	9:8	RW	0'h	MIC2 Boost Control 00: Bypass 01: +20dB 10: +30dB 11: Reserved
Reserved	7:6	R	0'h	Reserved. Read as 0
mic1_bias_voltage_ctrl	5	RW	0'h	MICBIAS1 Output Voltage Control 0: 0.9*AVDD 1: 0.75*AVDD
Reserved	4:2	R	0'h	Reserved. Read as 0
mic_bias_threshold	1:0	RW	0'h	MICBIAS1/2 Short Current Detector Threshold 00: 600µA 01: 1200µA 1x: 1800µA

8.15. Reg-34h: Digital Audio Interface Control

Default: 8000h

Table 25. Reg-34h: Audio Interface

Name	Bits	Read/Write	Reset State	Description
stereo_i2s_mode_sel	15	RW	1'h	Main Serial Data Port Mode Selection 0: Master 1: Slave
pcm_mode_sel	14	RW	0'h	PCM Mode Select 0: Mode A 1: Mode B
Reserved	13:8	RW	0'h	Reserved
stereo_i2s_bclk_polarity_ctrl	7	RW	0'h	Stereo I^2S BCLK Polarity Control 0: Normal 1: Invert
Reserved	6	RW	0'h	Reserved
adclrckswap	5	RW	0'b	ADC Data L/R Swap 0: ADC data appear at left phase of LRCK 1: ADC data appear at right phase of LRCK *Note: Supported in I^2S & PCM*
daclrckswap	4	RW	0'b	DAC Data L/R Swap 0: DAC data appear at left phase of LRCK 1: DAC data appear at right phase of LRCK *Note: Supported in I^2S & PCM*

Name	Bits	Read/Write	Reset State	Description
stereo_i2s_data_len_sel	3:2	RW	0'h	Data Length Selection 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits
stereo_i2s_data_format_sel	1:0	RW	0'h	Stereo PCM Data Format Selection 00: I²S format 01: Right justified 10: Left justified 11: PCM format

8.16. Reg-36Ah: Stereo AD/DA Clock Control

Default: 166Dh

Table 26. Reg-36h: Stereo AD/DA Clock Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15	RW	0'h	Reserved
i2s_pre_div	14:12	RW	1'h	I2S_Pre_Div 000b: ÷1 001b: ÷2 010b: ÷4 011b: ÷8 100b: ÷16 101b: ÷32 Others: Reserved
i2s_sclk_div	11:9	RW	011'b	I2S_BCLK_Div 000b: ÷1 (MCLK=BCLK) 001b: ÷2 010b: ÷3 011b: ÷4 100b: ÷6 101b: ÷8 110b: ÷12 111b: ÷16
i2s_wclk_div_pre	8:5	RW	0011'b	I2S_WCLK_Div_pre 0000b: ÷1 0001b: ÷2 0010b: ÷3 …….. 1101b: ÷14 1110b: ÷15 1111b: ÷16
i2s_wclk_div	4:2	RW	011'b	I2S_WCLK_Div 000b: ÷2 001b: ÷4 010b: ÷8 011b: ÷16 100b: ÷32 Others: Reserved
adda_filter_clk	1	RW	0'b	Stereo ADDA Filter Clock Select 0b: 256Fs 1b: 384Fs
adda_osr	0	RW	1'b	Stereo ADDA Over Sample Rate Select 0b: Low 1b: High

8.17. Reg-38h: Companding Control

Default: 0000h

Table 27. Reg-38h: Companding Control

Name	Bits	Read/Write	Reset State	Description
word_length_8	15	RW	0'b	0: OFF 1: Device works in 8 bits mode when in PCM mode B
Reserved	14:4	RW	0'h	Reserved
adc_comp	3:2	RW	00'b	ADC Companding (for ADC DAT Output) 00: OFF 01: μ-Law 10: A-Law 11: Reserved
dac_comp	1:0	RW	00'b	DAC Companding (for DAC DAT Input) 00: OFF 01: μ-Law 10: A-Law 11: Reserved

8.18. Reg-3Ah: Power Management Addition 1

Default: 0000h

Table 28. Reg-3Ah: Power Management Addition 1

Name	Bits	Read/Write	Reset State	Description
Main_i2s_en	15	RW	0'h	I^2S Digital Interface Enable 0: Disable 1: Enable
pow_zcd	14	RW	0'h	All Zero Cross Detect Power Down 0: Disable 1: Enable
Reserved	13:12	RW	0'h	Reserved
pow_mic1_bias	11	RW	0'h	Microphone1 Bias 0: Disable 1: Enable microphone1 bias
pow_mic1_bias_det_ctrl	10	RW	0'h	MICBIAS1 Short Current Detector Control 0: Disable 1: Enable
Reserved	9	RW	0'h	Reserved
pow_softgen	8	RW	0'h	Power on Softgen 1: Power on 0: Power down *Note: Refer to the ALC5623 application note for detailed de-pop sequence information.*
Reserved	7	RW	0'h	Reserved
pow_dpbuf_hp	6	RW	0'h	Power on Headphone Depop Buffer 1: Power on 0: Power down *Note: Refer to the ALC5623 application note for detailed de-pop sequence information.*
en_hp_out_amp	5	RW	0'h	Headphone Output Amplifier Buffer 1: Enable HP Output buffer for normal loading >KΩ 0: Disable (DPOP mode)

Name	Bits	Read/Write	Reset State	Description
en_hp_enhance_amp	4	RW	0'h	Headphone Enhance Output Buffer 1: Enable HP Output buffer for small R loading (<100Ω) 0: Disable (DPOP mode or normal loading mode)
Reserved	3	RW	0'h	Reserved
pow_dpbuf_aux	2	RW	0'h	AUX Power on Depop Buffer 1: Power on 0: Power down *Note: Refer to the ALC5623 application note for detailed de-pop sequence information.*
en_aux_out_amp	1	RW	0'h	AUX Output Amplifier Buffer 1: Enable AUX Output buffer for normal loading (>KΩ) 0: Disable (DPOP mode)
en_aux_enhance_amp	0	RW	0'h	Enhanced AUX Amplifier Output Buffer 1: Enable AUX Output buffer for small R loading (<100Ω) 0: Disable (DPOP mode or normal loading mode)

8.18.1. Headphone Output Amplifier Configuration

Table 29. Headphone Output Amplifier Configuration

en_hp_out_amp	en_hp_enhance_amp	Description
0'b	0'b	HP Output OFF
0'b	1'b	Not Used
1'b	0'b	HP Output for Normal Loading (>Kohm)
1'b	1'b	HP Output for Small R Loading (<100ohm)

8.18.2. Auxiliary Output Amplifier Configuration

Table 30. Auxiliary Output Amplifier Configuration

en_aux_out_amp	en_aux_enhance_amp	Description
0'b	0'b	AUX Output OFF
0'b	1'b	Not Used
1'b	0'b	AUX Output for Normal Loading (>Kohm)
1'b	1'b	AUX Output for small R Loading (<100ohm)

8.19. Reg-3Ch: Power Management Addition 2

Default: 0000h

Table 31. Reg-3Ch: Power Management Addition 2

Name	Bits	Read/Write	Reset State	Description
pow_LineOut_amp	15	RW	0'h	Line Out Power 0: Power off 1: Power on
Reserved	14	R/W	0'b	Reserved
pow_vref	13	RW	0'h	VREF of All Analog Circuits 0: Disable 1: Enable *Note: This bit works only if Index-39[11]=0b.*
pow_pll	12	RW	0'h	PLL 0: Disable 1: Enable
Reserved	11	RW	0'h	Reserved. Must be kept to 0.
pow_dac_ref	10	RW	0'h	Power DAC Reference Circuit (Vref+/Vref-) 0: Disable 1: Enable
pow_dac_l	9	RW	0'h	Left Stereo DAC Filter Clock 0: Disable 1: Enable
pow_dac_r	8	RW	0'h	Right Stereo DAC Filter Clock 0: Disable 1: Enable
pow_adc_l	7	RW	0'h	Left Stereo ADC Filter Clock and Input Gain 0: Disable 1: Enable
pow_adc_r	6	RW	0'h	Right Stereo ADC Filter Clock and Input Gain 0: Disable 1: Enable
pow_mix_hp_l	5	RW	0'h	Left Headphone Mixer 0: Disable 1: Enable
pow_mix_hp_r	4	RW	0'h	Right Headphone Mixer 0: Disable 1: Enable
pow_mix_spk	3	RW	0'h	Speaker Mixer 0: Disable 1: Enable
pow_mix_mono	2	RW	0'h	MONO Mixer 0: Disable 1: Enable
pow_mix_adc_rec_l	1	RW	0'h	Left ADC Record Mixer 0: Disable 1: Enable
pow_mix_adc_rec_r	0	RW	0'h	Right ADC Record Mixer 0: Disable 1: Enable

8.20. Reg-3Eh: Power Management Addition 3

Default: 0000h

Table 32. Reg-3Eh: Power Management Addition 3

Name	Bits	Read/Write	Reset State	Description
pow_main_bias	15	RW	0'h	Main Bias Analog Circuit 0: Disable 1: Enable
pow_aux_outl_vol	14	RW	0'h	AUXOUT_L(Mono_P) Volume Control & AUX_L Amplifier 0: Disable 1: Enable
pow_aux_outr_vol	13	RW	0'h	AUXOUT_R(Mono_N) Volume Control & AUX_R Amplifier 0: Disable 1: Enable
pow_lineout	12	RW	0'h	LINE_OUT Output 0: Disable 1: Enable
Reserved	11	RW	0'h	Reserved
pow_hp_l_vol	10	RW	0'h	HP_OUT_L Volume Control (Amp) 0: Disable 1: Enable
pow_hp_r_vol	9	RW	0'h	HP_OUT_R Volume Control (Amp) 0: Disable 1: Enable
Reserved	8	RW	0'h	Reserved
pow_li_l_vol	7	RW	0'h	LINE_IN Left Volume Control 0: Disable 1: Enable
pow_li_r_vol	6	RW	0'h	LINE_IN Right Volume Control 0: Disable 1: Enable
pow_auxin_l_vol	5	RW	0'h	AUXIN Left Volume Control 0: Disable 1: Enable
pow_auxin_r_vol	4	RW	0'h	AUXIN Right Volume Control 0: Disable 1: Enable
pow_mic1_vol	3	RW	0'h	MIC1 Boost + Differential Mixer + Volume Amp Control 0: Disable 1: Enable
pow_mic2_vol	2	RW	0'h	MIC2 Boost+ Differential Mixer + Volume Amp Control 0: Disable 1: Enable
pow_mic1_admixer	1	RW	0'h	MIC1 AD Boost + AD Differential Mixer 0: Disable 1: Enable
pow_mic2_admixer	0	RW	0'h	MIC2 AD Boost + AD Differential Mixer 0: Disable 1: Enable

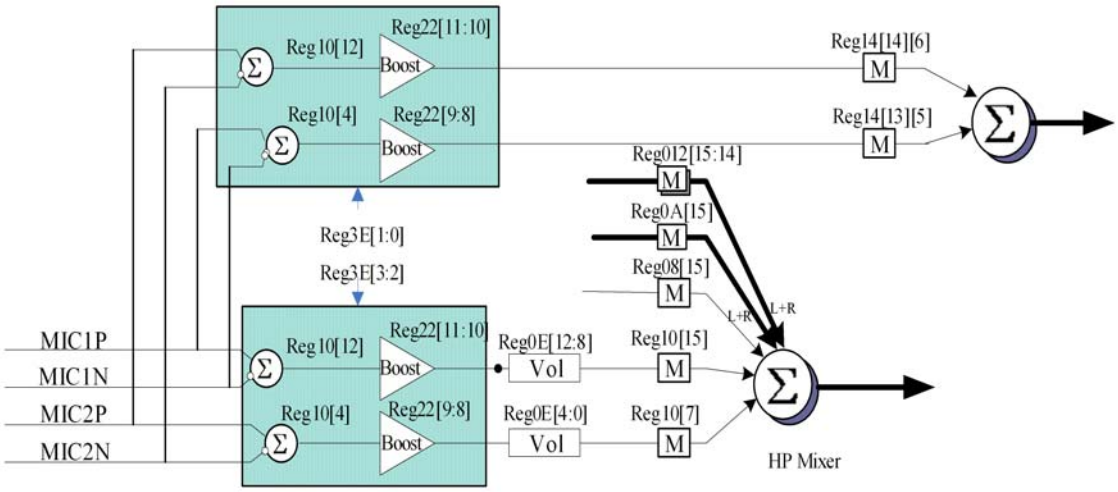


Figure 20. Power Control to MIC Input

8.21. Reg-40h: Additional Control Register

Default: 5300h

Table 33. Reg-40h: Additional Control Register

Name	Bits	Read/ Write	Reset State	Description
se_diff_auxout	15	RW	0'b	AUXOUT Selection of Single-Ended or Differential Mode 0: Differential Mode 1: Single-Ended Mode
lio_amp_ctrl	14:12	RW	5'h	Line Out Amplifier VMID Ratio Control (Output Gain Control) 000: 2.25 Vdd 001: 2.00 Vdd 010: 1.75 Vdd 011: 1.5 Vdd 100: 1.25 Vdd 101: 1 Vdd Others: Not allowed *Note: Only used when AVDD is not equal to AVDD2.*
Reserved	11:10	R	0'h	Reserved
dac_hpf_en	9	R/W	1'h	STEREO DAC High Pass Filter 0: Disable 1: Enable
adc_hpf_en	8	R/W	1'h	STEREO ADC High Pass Filter 0: Disable 1: Enable
Reserved	7:6	R	0'h	Reserved
digital_vol_boost	5:4	RW	0'b	Digital Volume Boost 00: 0dB 01: 6dB 10: 12dB 11: 18dB
se_btl_lio	3	RW	0'b	LINE_OUT Selection of Single-Ended or Bridge-Tied Load (BTL). 0: Differential Mode 1: Single-Ended Mode
Reserved	2:0	RW	0'h	Reserved

8.22. Reg-42h: Global Clock Control Register

Default: 0000h

Table 34. Reg-42h: Global Clock Control Register

Name	Bits	Read/Write	Reset State	Description
sel_sysclk	15	RW	0'h	Clock Source MUX Control 0: MCLK 1: PLL Output
pll_sour_sel	14	RW	0'h	PLL Source Select 0: From MCLK 1: From BLCK
Reserved	13:3	RW	0'h	Reserved
pllout_div_ratio	2:1	RW	0'b	PLL Output Division Ratio (Divider of PLL Output to GPIO 00: ÷1 01: ÷2 10: ÷4 11: ÷8
pll_pre_div	0	RW	0'b	PLL Pre-Divider 0b: ÷1 1b: ÷2

8.23. Reg-44h: PLL Control Register

8.23.1. Reg-44h: PLL Control Register

Default: 0000h

Table 35. Reg-44h: PLL Control Register

Name	Bits	Read/Write	Reset State	Description
pll_n_code	15:8	RW	00'h	N[7:0] Code for Analog PLL 00000000: Div 2 00000001: Div 3 …….. 11111111: Div 257
pll_m_bypass	7	RW	0'h	Bypass PLL M 0b: No bypass 1b: Bypass
pll_k_code	6:4	RW	0'h	K[2:0] Code for Analog PLL 000: Div 2 001: Div 3 …… 111: Div 9
pll_m_code	3:0	RW	0'h	M[3:0] Code for Analog PLL 0000: Div 2 0001: Div 3 …… 1111: Div 17

*Note: The PLL1 transmit formula is FOUT = (MCLK * (N+2))/((M+2) * (K+2)) {Typical K=2}*

8.23.2. PLL Clock Setting Table for 48K: (Unit: MHz)

Table 36. PLL Clock Setting Table for 48K: (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	66	7	98.222	2	24.555
3.6864	78	1	98.304	2	24.576
2.048	94	0	98.304	2	24.576
4.096	70	1	98.304	2	24.576
12	80	8	98.4	2	24.6
15.36	81	11	98.068	2	24.517
16	78	11	98.462	2	24.615
19.2	80	14	98.4	2	24.6
19.68	78	14	98.4	2	24.6

8.23.3. PLL Clock Setting Table for 44.1K: (Unit: MHz)

Table 37. PLL Clock Setting Table for 44.1K: (Unit: MHz)

MCLK	N	M	F_{VCO}	K	F_{OUT}
13	68	8	91	2	22.75
3.6864	72	1	90.931	2	22.733
2.048	86	0	90.112	2	22.528
4.096	64	1	90.112	2	22.528
12	66	7	90.667	2	22.667
15.36	63	9	90.764	2	22.691
16	66	10	90.667	2	22.667
19.2	64	12	90.514	2	22.629
19.68	67	13	90.528	2	22.632

8.24. Reg-4Ah: GPIO_Output Pin Control

Default: 0000h

Table 38. Reg-4Ch: GPIO_Output Pin Control

Name	Bits	Read/Write	Reset State	Description
Reserved	15:2	R	0000'h	Reserved
gpio_out_status	1	RW	0'h	GPIO Output Pin Control 0b: Drive Low 1b: Drive High
Reserved	0	R	0'h	Reserved. Read as 0

8.25. Reg-4Ch: GPIO Pin Configuration

Default: 1C0Eh

Table 39. Reg-4Ch: GPIO Pin Configuration

Name	Bits	Read/Write	Reset State	Description
Reserved	15:11	R	03'b	Reserved
mic1_short_det_conf	10	RW	1'h	MICBIAS Short Current Status Source Configuration 0: Bypass 1: Normal
Reserved	9:4	R	0'h	Reserved
jd2_conf	3	RW	1'h	Jack Detect 2 Status Source Configuration 0: Bypass 1: Normal
jd1_conf	2	RW	1'h	Jack Detect 2 Status Source Configuration 0: Bypass 1: Normal
gpio_conf	1	RW	1'h	GPIO Pin Configuration 0: Bypass 1: Input
Reserved	0	R	0'h	Reserved. Read as 0

8.26. Reg-4Eh: GPIO Pin Polarity

Default: 1C0Eh

Table 40. Reg-4Eh: GPIO Pin Polarity

Name	Bits	Read/Write	Reset State	Description
Reserved	15:11	R	03'b	Reserved
mic1_short_det_polarity	10	RW	1'h	MICBIAS Short Current Detect Polarity 0: Low Active 1: High Active
Reserved	9:4	R	0'h	Reserved
jd2_polarity	3	RW	1'h	Jack Detect 2 Pin Polarity 0: Low Active 1: High Active
jd1_polarity	2	RW	1'h	Jack Detect 1 Pin Polarity 0: Low Active 1: High Active
gpio_polarity	1	RW	1'h	GPIO Pin Polarity 0: Low Active 1: High Active
Reserved	0	R	0'h	Reserved. Read as 0

8.27. Reg-50h: GPIO Pin Sticky

Default: 0000h

Table 41. Reg-50h: GPIO Pin Sticky

Name	Bits	Read/Write	Reset State	Description
Reserved	15:11	R	00'b	Reserved
mic1_short_det_sticky_en	10	RW	0'h	MICBIAS Short Current Detect Sticky Enable 0: Not sticky 1: Sticky
Reserved	9:4	R	0'h	Reserved
jd2_sticky_En	3	RW	0'h	Jack Detect 2 Pin Sticky Enable 0: Not sticky 1: Sticky
jd1_sticky_En	2	RW	0'h	Jack Detect 1 Pin Sticky Enable 0: Not sticky 1: Sticky
gpio_sticky_En	1	RW	0'h	GPIO Pin Sticky Enable 0: Not sticky 1: Sticky
Reserved	0	R	0'h	Reserved. Read as 0

8.28. Reg-52h: GPIO Pin Wake-Up

Default: 0000h

Table 42. Reg-52h: GPIO Pin Wake-Up

Name	Bits	Read/Write	Reset State	Description
Reserved	15:11	R	00'b	Reserved
mic1_short_det_wakeup_en	10	RW	0'h	MICBIAS Short Current Detect Wake-Up Enable 0: No wake-up 1: Wake up
Reserved	9:4	R	0'h	Reserved
jd2_wakeup_en	3	RW	0'h	Jack Detect 2 Pin Wake-Up Enable 0: No wake-up 1: Wake up
jd1_wakeup_en	2	RW	0'h	Jack Detect 1 Pin Wake-Up Enable 0: No wake-up 1: Wake up
gpio_wakeup_en	1	RW	0'h	GPIO Pin Wake-Up Enable 0: No wake-up 1: Wake up
Reserved	0	R	0'h	Reserved. Read as 0

8.29. Reg-54h: GPIO Pin Status

Default: 0002h

Table 43. Reg-54h: GPIO Pin Status

Name	Bits	Read/Write	Reset State	Description
Reserved	15:11	R	00'b	Reserved
mic1_short_det_status	10	R	0'h	MICBIAS Short Current Detect Status Read: Return status Write: Writing '0' clears the sticky bit
Reserved	9:4	R	0'h	Reserved
jd2_status	3	R	0'h	Jack Detect 2 Pin Status Read: Returns status of JD2 pin Write: Writing '0' clears sticky bit
jd1_status	2	R	0'h	Jack Detect 1 Pin Status Read: Return status of JD1 pin Write: Writing '0' clears sticky bit
gpio_status	1	R	1'h	GPIO Pin Status Read: Returns status of each GPIO pin Write: Writing '0' clears the sticky bit
Reserved	0	R	0'h	Reserved. Read as 0

8.30. Reg-56h: Pin Sharing

Default: 0000h

Table 44. Reg-56h: Pin Sharing

Name	Bits	Read/Write	Reset State	Description
lineinl_pin_sharing	15	RW	0'b	LINE_IN_L Pin Sharing 0: LINE_IN_L 1: JD1
lineinr_pin_sharing	14	RW	0'h	LINE_IN_R Pin Sharing 0: LINE_IN_R 1: JD2
Reserved	13:2	RW	000'h	Reserved
gpio_pin_sharing	1:0	RW	00'b	GPIO Pin Sharing 00: GPIO 01: IRQ_Out 10: Reserved 11: PLL_Out

8.31. Reg-58h: Over-Current Status

Default: 0000h

Table 45. Reg-58h: Over-Current Status

Name	Bits	Read/Write	Reset State	Description
ovc_micbias1_status	15	R	0'h	MICBIAS Over-Current 0: Normal 1: Over-current
Reserved	14:0	R	0'h	Reserved

8.32. Reg-5Ah: Jack Detect Control Register

Default: 0000h

Table 46. Reg-5Ah: Jack Detect Control Register

Name	Bits	Read/Write	Reset State	Description
jd_sel	15:14	RW	0'h	Jack Detect Select 00: OFF 01: GPIO 10: JD1 11: JD2
Reserved	13:12	RW	0'b	Reserved
jd_H_Out	11:8	RW	0'h	Output Enable when Selected Jack Detect is 'High' xxx1: Headphone Out xx1x: AUXOUT_L x1xx: AUXOUT_R 1xxx: Line Out
jd_L_Out	7:4	RW	0'h	Output Enable when Selected Jack Detect is 'Low' xxx1: Headphone Out xx1x: AUXOUT_L x1xx: AUXOUT_R 1xxx: Line Out
Reserved	3:0	RW	0'b	Reserved

8.33. Reg-5Eh: MISC Control

Default: 0000h

Table 47. Reg-5Eh: MISC Control

Name	Bits	Read/Write	Reset State	Description
en_vref_fast	15	RW	0'b	Enable Fast Vref 0: Enable fast Vref 1: Disable fast Vref *Note: To improve PSRR, en_vref_fast should be disabled before playback/record.*
Reserved	14:11	RW	0'b	Reserved. Must be kept to 0.
en_dp3_hp	10	RW	0'h	Enable Depop Mode 3 of HP_Out 0: Disable 1: Enable
en_dp2_hp	9	RW	0'h	Enable Depop Mode 2 of HP_Out 0: Disable 1: Enable
en_dp1_hp	8	RW	0'h	Enable Depop Mode 1 of HP_Out 0: Disable 1: Enable
Reserved	7	RW	0'h	Reserved
en_dp3_aux	6	RW	0'h	Enable Depop Mode 3 of AUX_Out 0: Disable 1: Enable
en_dp2_aux	5	RW	0'h	Enable Depop Mode 2 of AUX_Out 0: Disable 1: Enable
en_dp1_aux	4	RW	0'h	Enable Depop Mode 1 of AUX_Out 0: Disable 1: Enable
main_dac_l_mute	3	RW	0'h	Mute Main DAC Left Input 0: On 1: Mute (-∞ dB)

Name	Bits	Read/Write	Reset State	Description
main_dac_r_mute	2	RW	0'h	Mute Main DAC Right Input 0: On 1: Mute (-∞ dB)
Reserved	1	RW	0'h	Reserved
irqout_inv_ctrl	0	RW	0'h	IRQOUT Inverter Control 0: Normal 1: Invert

8.34. Reg-60h: Stereo and Spatial Effect Block Control

Default: 0497h

Table 48. Reg-60h: Stereo and Spatial Effect Block Control

Name	Bits	Read/Write	Reset State	Description
spatial_ctrl_enable	15	RW	0'b	Spatial Enable 0b: Disable (clear internal state) 1b: Enable
apf_en	14	RW	0'h	Enable All Pass Filter APF(z), EN-APF 0: Disable (bypass) and reset 1: Enable all pass filter. The coefficient a1 is loaded from REG_MX64.[7:0]
pseudo_stereo_en	13	RW	0'h	Enable Pseudo Stereo Block, EN-PSB 0: Disabled 1: Enabled
en_3d	12	RW	0'h	Enable Stereo Expansion Block , EN-SEB 0: Disable 1: Enabled. Load 3D Ratio from ratio_parm_3d, and 3D Gain from gain_parm_3d
gain_parm_3d_l	11:9	RW	2'h	3D Gain Parameter Left (SEG2) 000: Gain=1.0 001: Gain=1.25 010: Gain=1.5 011: Gain=1.75 100: Gain=2 Others: Reserved
gain_parm_3d_r	8:6	RW	2'h	3D Gain Parameter Right (SEG1) 000: Gain=1.0 001: Gain=1.25 010: Gain=1.5 011: Gain=1.75 100: Gain=2 Others: Reserved
ratio_parm_3d_l	5:4	RW	1'h	3D Ratio Parameter Left (DP2) 00: Ratio=0.0 01: Ratio=0.66 10:Ratio=1.0 11:Reserved
ratio_parm_3d_r	3:2	RW	1'h	3D Ratio Parameter Right (DP1) 00: Ratio=0.0 01: Ratio=0.66 10:Ratio=1.0 11:Reserved
apf_parm_a1	1:0	RW	3'h	All Pass Filter Parameter a1 in 2's Complement 1.7 Format (-1.0~0.99) 00: Reserved 01: 32kHz sample rate or lower 10: 44.1kHz sample rate 11: 48kHz sample rate

Note: Writes to SEGn and DPn will be ignored when the Spatial effect control bit is enabled. This means individual Spatial coefficients cannot be modified when Spatial is enabled.

8.35. Reg-62h: EQ Control

Default: 0000h

Table 49. Reg-62h: EQ Control

Name	Bits	Read/Write	Reset State	Description
eq_all_en	15	RW	0'b	EQ Block Control 0b: Disable 1b: Enable
eq_HPF_mode	14	RW	0'b	EQ High Frequency Shelving Filter Mode 0: High Frequency Shelving Filter 1: -20dB/decade (HPF)
Reserved	13:12	R	0'h	Reserved
Eq_source	11	RW	0'b	EQ Source 0: DAC path 1: ADC path
Reserved	10:5	R	00'h	Reserved
eq_hpf_en	4	RW	0'b	EQ High Pass Filter (HPF) Control 0: Disabled (bypass) and reset 1: Enabled
eq_bpf3_en	3	RW	0'b	EQ Band-3 (BP3) Control 0: Disabled and reset 1: Enabled.
eq_bpf2_en	2	RW	0'b	EQ Band-2 (BP2) Control 0: Disabled and reset 1: Enabled.
eq_bpf1_en	1	RW	0'b	EQ Band-1 (BP1) Control 0: Disabled and reset 1: Enabled.
eq_lpf_en	0	RW	0'b	EQ Low Pass Filter (LPF) Control 0: Disabled and reset 1: Enabled.

8.36. Reg-66h: EQ Mode Change Enable

Default: 0000h

Table 50. Reg-66h: EQ Mode Change Enable

Name	Bits	Read/Write	Reset State	Description
Reserved	15:5	RW	0'h	Reserved
eq_hpf_chg_en	4	RW	0'b	EQ High Pass Filter (HPF) Mode Change Enable 0: Disable 1: Enable
eq_bpf3_chg_en	3	RW	0'b	EQ Band-3 (BP3) Mode Change Enable 0: Disable 1: Enable
eq_bpf2_chg_en	2	RW	0'b	EQ Band-2 (BP2) Mode Change Enable 0: Disable 1: Enable
eq_bpf1_chg_en	1	RW	0'b	EQ Band-1 (BP1) Mode Change Enable 0: Disable 1: Enable
eq_lpf_chg_en	0	RW	0'b	EQ Low Pass Filter (LPF) Mode Change Enable 0: Disable 1: Enable

Note: To enable an EQ mode change, the driver should set the new EQ parameters (Index00~Index0C) before setting this register to 'Enable'. After the EQ parameter has been changed, the driver should set this register to 'Disable'.

8.37. Reg-68h: AVC Control

Default: 000Bh

Table 51. Reg-68h: AVC Control

Name	Bits	Read/Write	Reset State	Description
avc_en	15	RW	0'b	Auto Volume Control (AVC) Enable 0: Disable AVC 1: Enable AVC
avc_ref_ch	14	RW	0'b	AVC Reference Channel Selection 0: Left Channel 1: Right Channel
Nonact_reg_action	13	RW	0'b	Gain Action of Non-Active Region 0: Keep Previous Gain 1: Unit Gain
Nonact_feedback_sel	12	RW	0'b	Non-Active Threshold Gain Feedback Selection 0: No gain feedback 1: Gain feedback
Reserved	11:5	RW	0'h	Reserved
monitor_window	4:0	RW	0B'h	Monitor Window Control (Unit: 2^(n+1) samples) (default:01011b) 00000b: 2^(1) sample 00001b: 2^(2) samples 00010b: 2^(3) samples 10000b: 2^(17) samples Others: Reserved. Maximum=10000000000000000=2^17

8.38. Reg-6Ah: Index Address

Default: 0000h

Table 52. Reg-6Ah: Index Address

Name	Bits	Read/Write	Reset State	Description
Reserved	15:7	R	0'h	Reserved
index_addr	6:0	RW	0'h	Index Address

8.39. Reg-6Ch: Index Data

Default: 0000h

Table 53. Reg-6Ch: Index Data

Name	Bits	Read/Write	Reset State	Description
index_data	15:0	RW	0'h	Index Data

8.40. Index-00h: EQ Band-0 Coefficient (LP0: a1)

Default: 0000h

Table 54. Index-00h: EQ Band-0 Coefficient (LP0: a1)

Bit	Type	Function
15:0	RW	2's complement in 3.13 formats (The range is from –4~3.99, the a1 should be in -2~1.99)

Note: For low pass filter for Bass control – LP0 has filter coefficient a1 and gain Ho must be set (see Table 55).

8.41. Index-01h: EQ Band-0 Gain (LP0: Ho)

Default: 0000h

Table 55. Index-01h: EQ Band-0 Gain (LP0: Ho)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from –4~3.99, the Ho should be in -4~3.99)

8.42. Index-02h: EQ Band-1 Coefficient (BP1: a1)

Default: 0000h

Table 56. Index-02h: EQ Band-1 Coefficient (BP1: a1)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from –4~3.99, the a1 should be in -2~1.99)

8.43. Index-03h: EQ Band-1 Coefficient (BP1: a2)

Default: 0000h

Table 57. Index-03h: EQ Band-1 Coefficient (BP1: a2)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from –4~3.99, the a1 should be in -2~1.99)

8.44. Index-04h: EQ Band-1 Gain (BP1: Ho)

Default: 0000h

Table 58. Index-04h: EQ Band-1 Gain (BP1: Ho)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from –4~3.99, the Ho should be in -4~3.99)

8.45. Index-05h: EQ Band-2 Coefficient (BP2: a1)

Default: 0000h

Table 59. Index-05h: EQ Band-2 Coefficient (BP2: a1)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from –4~3.99, the a1 should be in -2~1.99)

8.46. Index-06h: EQ Band-2 Coefficient (BP2: a2)

Default: 0000h

Table 60. Index-06h: EQ Band-2 Coefficient (BP2: a2)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from –4~3.99, the a2 should be in -2~1.99)

8.47. Index-07h: EQ Band-2 Gain (BP2: Ho)

Default: 0000h

Table 61. Index-07h: EQ Band-2 Gain (BP2: Ho)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from –4~3.99, the Ho should be in -4~3.99)

8.48. Index-08h: EQ Band-3 Coefficient (BP3: a1)

Default: 0000h

Table 62. Index-08h: EQ Band-3 Coefficient (BP3: a1)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from –4~3.99, the a1 should be in -2~1.99)

8.49. Index-09h: EQ Band-3 Coefficient (BP3: a2)

Default: 0000h

Table 63. Index-09h: EQ Band-3 Coefficient (BP3: a2)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from –4~3.99, the a2 should be in -2~1.99)

8.50. Index-0Ah: EQ Band-3 Gain (BP3: Ho)

Default: 0000h

Table 64. Index-0Ah: EQ Band-3 Gain (BP3: Ho)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from –4~3.99, the Ho should be in -4~3.99)

8.51. Index-0Bh: EQ Band-4 Coefficient (HPF: a1)

Default: 0000h

Table 65. Index-0Bh: EQ Band-4 Coefficient (HPF: a1)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from –4~3.99, the a1 should be in -2~1.99)

8.52. Index-0Ch: EQ Band-4 Gain (HPF: Ho)

Default: 0000h

Table 66. Index-0Ch: EQ Band-4 Gain (HPF: Ho)

Bit	Type	Function
15:0	RW	2's complement in 3.13 format (The range is from –4~3.99, the Ho should be in -2~1.99)

8.53. Index-11h: EQ Input Volume Control

Default: 0000h

Table 67. Index-11h: EQ Input Volume Control

Bit	Type	Function
15:2	-	Reserved
1:0	RW	7-Bit Volume Unsigned Ratio EQIn-VOL-LR 00b: 0dB 01b: -6dB 10b: -12dB 11b: -18dB

8.54. Index-12h: EQ Output Volume Control

Default: 0001h

Table 68. Index-12h: EQ Output Volume Control

Bit	Type	Function
15:3	-	Reserved
2:0	RW	7-Bit Volume Unsigned Ratio EQOut-VOL-LR 000b: -3dB 001b: 0dB 010b: 3dB 011b: 6dB 100b: 9dB 101b: 12dB 110b: 15dB 111b: 18dB

8.55. Index-21h: Auto Volume Control Register 1

Default: 0400h

Table 69. Index-21h: Auto Volume Control Register 1

Bit	Type	Function
15	-	Reserved
14:0	RW	The Maximum PCM absolute level after AVC, Thmax (=0~2^15-1)

8.56. Index-22h: Auto Volume Control Register 2

Default: 0390h

Table 70. Index-22h: Auto Volume Control Register 2

Bit	Type	Function
15	-	Reserved
14:0	RW	The Minimum PCM absolute level after AVC, Thmin (=0~2^15-1)

8.57. Index-23h: Auto Volume Control Register 3

Default: 0001h

Table 71. Index-23h: Auto Volume Control Register 3

Bit	Type	Function
15	-	Reserved
14:0	RW	The Non-active PCM absolute level AVC will keep analog unit gain, Thnonact (=0~2^15-1)

Note: Initial Index23=0001'h

8.58. Index-24h: Auto Volume Control Register 4

Default: 01FFh

Table 72. Index-24h: Auto Volume Control Register 4

Bit	Type	Function
15:0	RW	CNTMAXTH1. Controls the Sensitivity to Increased Gain (unit:2^1) This value should be less than CNTMAXTH2 (Max=1111111111111110=2^18-2)

8.59. Index-25h: Auto Volume Control Register 5

Default: 0200h

Table 73. Index-25h: Auto Volume Control Register 5

Bit	Type	Function
15:0	RW	CNTMAXTH2. Controls the Sensitivity to Decreased Gain (unit:2^1) This value should be less than Monitor Window (Optimal: 1/2 Monitor Window) (Max=1111111111111110=2^18-2)

Note: CNTMAXTH1 < CNTMAXTH2

8.60. Index-39h: Digital Internal Register

Default: 9800h

Table 74. Index-39h: Digital Internal Register

Bit	Type	Function
15	RW	Pad Drive Capability 0b: Weak drive 1b: Strong drive
14:13	RW	Reserved
12	RW	Power Gating Enable 0: Disable 1: Enable
11	RW	Vref Power Control Enable 0: Enable 1: Disable
10:0	RW	Reserved

8.61. Reg-7Ch: VENDOR ID 1

Default: 10ECh

Table 75. Reg-7Ch: VENDOR ID 1

Name	Bits	Read/Write	Reset State	Description
vender_id1	15:0	R	10EC'h	Vendor ID=10EC

8.62. Reg-7Eh: VENDOR ID 2

Default: 2303h

Table 76. Reg-7Eh: VENDOR ID 2

Name	Bits	Read/Write	Reset State	Description
vender_id	15:8	R	23'h	Device ID=23
device_id2	7:0	R	03'h	Version ID=03

9. Electrical Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 77. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies					
Digital IO Buffer	DBVDD	-0.3	-	3.63	V
Digital Core	DCVDD	-0.3	-	3.63	V
Analog	AVDD, AVDD2	-0.3	-	3.63	V
Operating Ambient Temperature	Ta	-25	-	+85	°C
Storage Temperature	Ts	-55	-	+125	°C

9.1.2. Recommended Operating Conditions

Table 78. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Digital IO Buffer	DBVDD	1.71*	3.3	3.6	V
Digital Core	DCVDD	1.71	3.3	3.6	V
Analog	AVDD, AVDD2	2.3	3.3	3.6	V

Note: '' indicates a 1μF Capacitor must be connected from AVDD2 to AGND, and should be placed as close as possible to the AVDD2 pin of the ALC5623.*

9.1.3. Static Characteristics

Table 79. Static Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Range	V_{IN}	-0.30	-	DVDD+0.30	V
Low Level Input Voltage	V_{IL}	-	-	0.35DVDD	V
High Level Input Voltage	V_{IH}	0.65DVDD	-	-	V
High Level Output Voltage	V_{OH}	0.9DVDD	-	-	V
Low Level Output Voltage	V_{OL}	-	-	0.1DVDD	V

Note: DVDD=3.3V, $T_{ambient}$=25℃, with 50pF external load.

9.2. Analog Performance Characteristics

Table 80. Analog Performance Characteristics

Parameter	Min	Typ	Max	Units
Full Scale Input Voltage				
Line Inputs	-	1.0	-	Vrms
MIC Inputs (Non-Boost)	-	1.0	-	Vrms
MIC Inputs (Boost 20dB)	-	0.1	-	Vrms
ADC	-	0.7	-	Vrms
Full Scale Output Voltage				
MONO Outputs	-	1.0	-	Vrms
Headphone Amplifiers Outputs	-	1.0	-	Vrms
LINE OUT	-	0.9	-	Vrms
DAC	-	1.0	-	Vrms
S/N Ratio (A-Weighted, HPL/R or MONO with 10KΩ/50pF Load)				
STEREO DAC	-	92	-	dB
STEREO ADC	-	85	-	dB
Total Harmonic Distortion+Noise (HPL/R or MONO with 10KΩ/50pF Load)				
STEREO DAC	-	-85	-	dB
STEREO ADC	-	-80	-	dB
MIC Boost Amplifier				
Gain=20dB	-	20	-	dB
Gain=30dB	-	30	-	dB
Input Impedance (Gain=0dB, ADC mixer=On/Off)				
MIC1N, MIC2N (Differential Mode)	-	16	-	KΩ
MIC1P, MIC2P	-	16	-	KΩ
Input Impedance (Gain=0dB, ADC Mixer=On)				
LINE_IN_L/R, AUXIN_L/R	12.8	16	19.2	KΩ
Input Impedance (Gain=0dB, ADC Mixer=Off)				
LINE_IN_L/R, AUXIN_L/R	25.6	32	38.4	KΩ
MONO_OUT/AUXOUT_L/R Amplifier Quiescent Current (32Ω Load)	-	900	-	μA
MONO_OUT/AUXOUT_L/R Amplifier Efficiency (f_{IN}=1KHz, 32Ω Load)				
Single-Ended Mode (Output Power=25mW)	50	-	-	%
BTL Mode (Output Power=75mW)	50	-	-	%
LINE_OUT/MONO_OUT/AUXOUT_L/R Amplifier THD+N				
Single-Ended Mode (10KΩ Load)				
Output Power=0.1mW	-	-85	-	dB
BTL Mode (10KΩ Load)				
Output Power=0.1mW	-	-85	-	dB
Headphone Amplifier Output Power (32Ω Load)	-	-	31.25	mW
LINE_OUT/MONO_OUT/AUXOUT_L/R Amplifier PSRR (217Hz)	-	50	-	dB

Parameter	Min	Typ	Max	Units
Headphone Amplifier Efficiency (f_{IN}=1KHz, 32Ω Load, Output Power=25mW)	50	-	-	%
Headphone Amplifier THD+N (32Ω Load)				
Output Power=20mW	-	-75	-	dB
Output Power=25mW	-	-74	-	dB
Headphone Amplifier PSRR (217Hz)	-	50	-	dB
Quiescent Playback Current (DAC to HP_OUT with 16Ω Load)				
I_{DDA} (Analog Block)	-	-	4	mA
I_{DDD} (Digital Block)	-	-	5.5	mA
Power Down Current				
I_{DDA} (Analog Block)	-	-	10	µA
I_{DDD} (Digital Block)	-	-	1	µA
MICBIAS Output Voltage				
0.75*AVDD Setting	-	2.475	-	V
0.9*AVDD Setting	-	2.97	-	V
MICBIAS Drive Current	2	-	3	mA

Note: Standard test conditions

$T_{ambient}$=25℃, DBVDD=DCVDD=AVDD=3.3V, AVDD2=5V

1kHz input sine wave; PCM Sampling frequency=48kHz; 0dB=1Vrms, Test bench Characterization BW: 10Hz~22kHz, 0dB attenuation; EQ and 3D disabled.

9.3. Signal Timing

9.3.1. I²C Control Interface

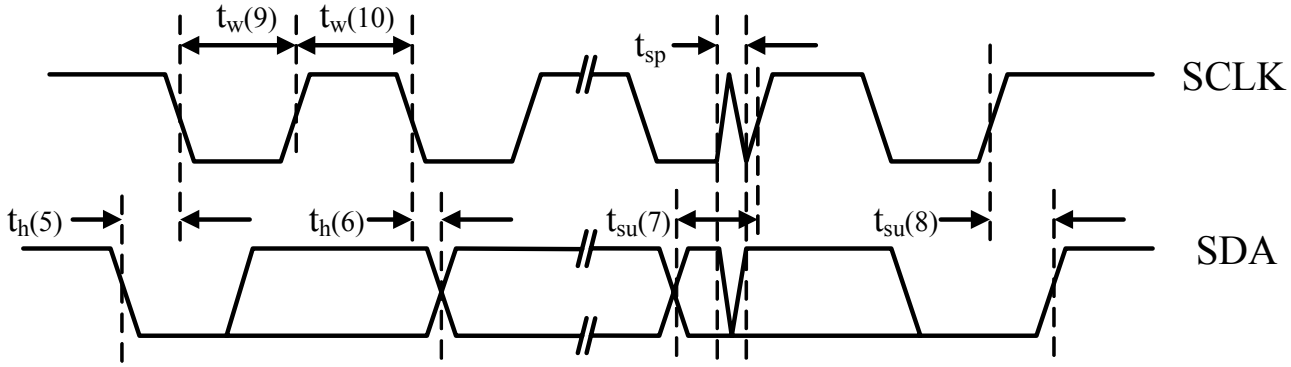


Figure 21. I²C Control Interface

Table 81. I²C Timing

Parameter	Symbol	Min	Typ	Max	Units
Clock Pulse Duration	$t_w(9)$	1.3	-	-	µs
Clock Pulse Duration	$t_w(10)$	600	-	-	ns
Clock Frequency	f	0	-	400K	Hz
Start Hold Time	$t_h(5)$	600	-	-	ns
Data Setup Time	$t_{su}(7)$	100	-	-	ns
Data Hold Time	$t_h(6)$	-	-	900	ns
Rising Time	t_r	-	-	300	ns
Falling Time	t_f	-	-	300	ns
Stop Setup Time	$t_{su}(8)$	600	-	-	ns
Pulse Width of Spikes Suppressed Input Filter	t_{sp}	0	-	50	ns

Note: Condition: MCLK > 8MHz.

9.3.2. I²S/PCM Interface Master Mode

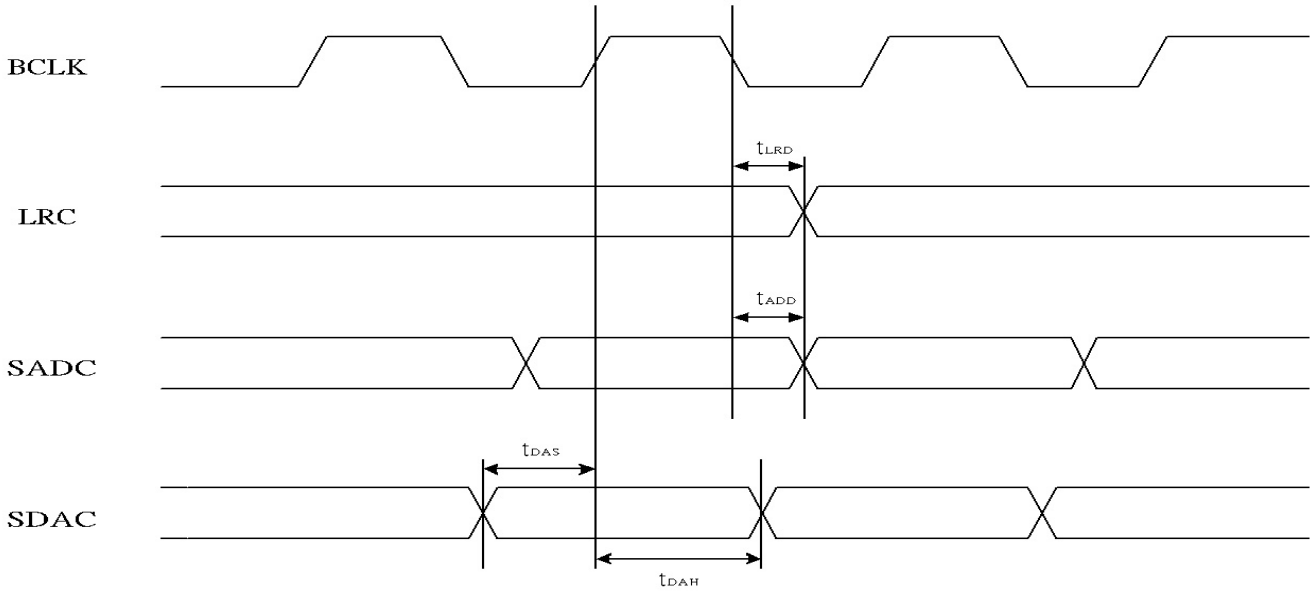


Figure 22. Timing of I²S/PCM Master Mode

Table 82. Timing of I²S/PCM Master Mode

Parameter	Symbol	Min	Typ	Max	Units
LRCK Output to BCLK Delay	t_{LRD}	-	-	30	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

9.3.3. I²S/PCM Interface Slave Mode

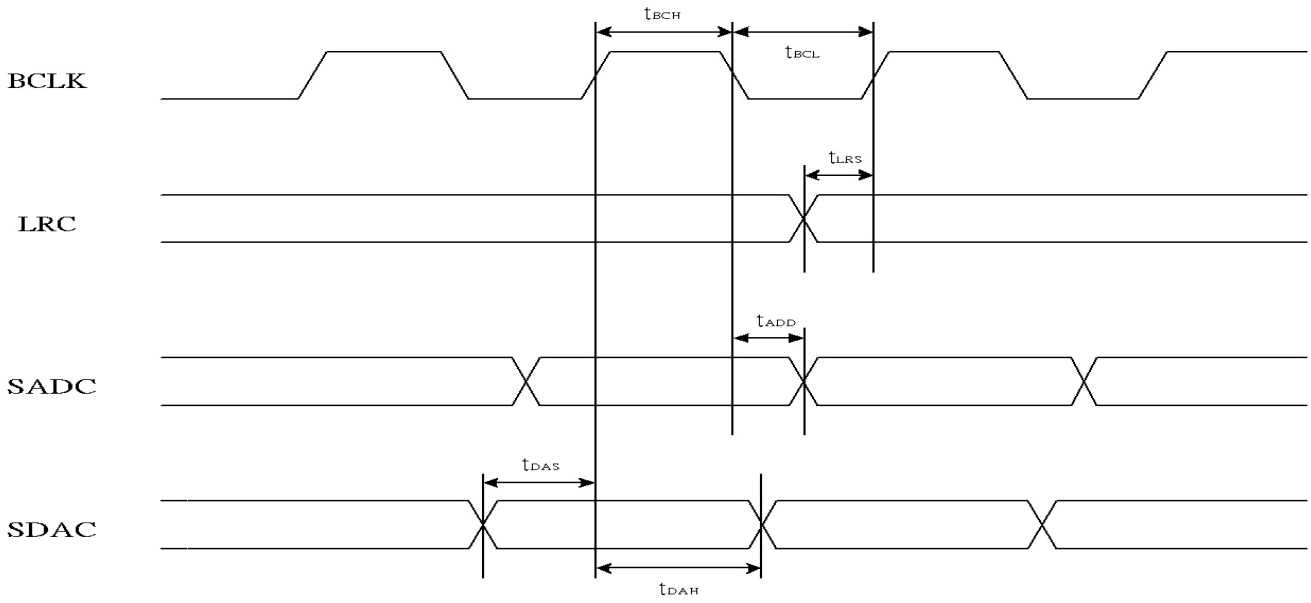


Figure 23. I²S/PCM Slave Mode Timing

Table 83. I²S/PCM Slave Mode Timing

Parameter	Symbol	Min	Typ	Max	Units
BCLK High Pulse Width	t_{BCH}	20	-	-	ns
BCLK Low Pulse Width	t_{BCL}	20	-	-	ns
LRCK Input Setup Time	t_{LRS}	30	-	-	ns
Data Output to BCLK Delay	t_{ADD}	-	-	30	ns
Data Input Setup Time	t_{DAS}	10	-	-	ns
Data Input Hold Time	t_{DAH}	10	-	-	ns

10. Application Circuits

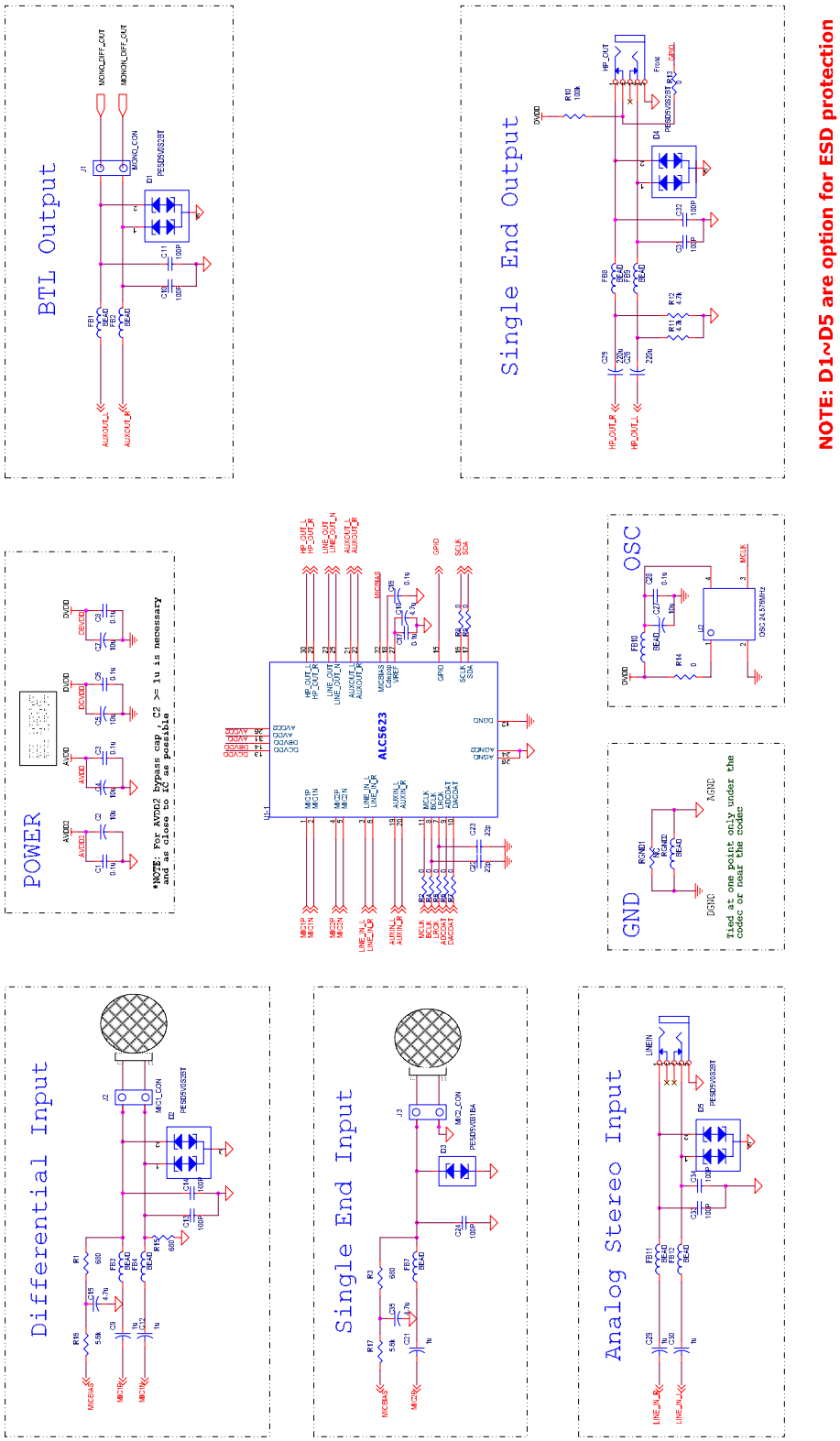
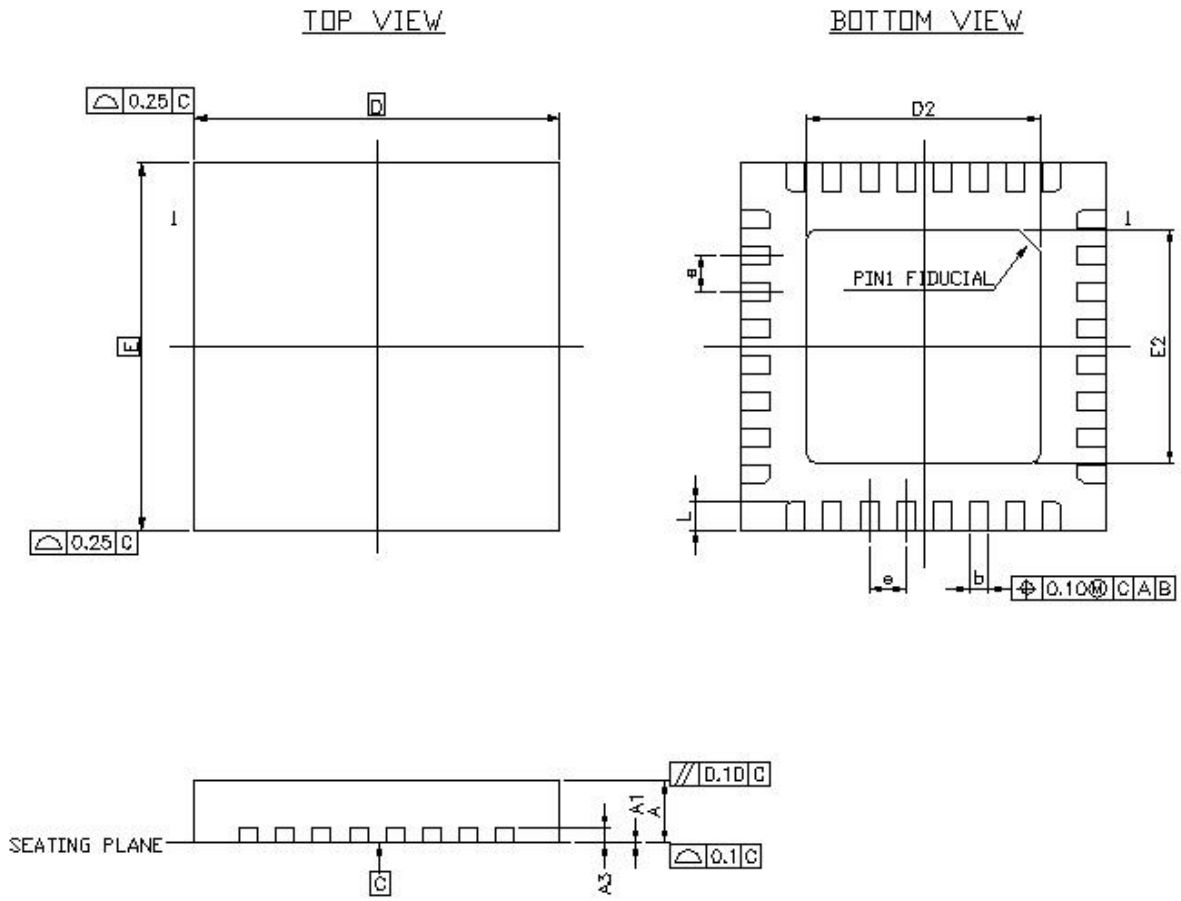


Figure 24. Application Circuits

11. Mechanical Dimensions

Plastic Quad Flat No-Lead Package 32 Leads 5x5mm Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3	0.20REF			0.008REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
c	-	-	0.6	-	-	0.024
D/E	5.00BSC			0.197BSC		
D_2/E_2	3.10	3.35	3.60	0.122	0.132	0.142
e	0.50BSC			0.020BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

12. Appendix A: Stereo I²S Clock Table

MCLK (Hz)	PLL Output (Hz)	Sel_sysclk Reg42[15]	DA/AD Clock Reg36		DAC/ADC Sample Rate LRCK (Hz)
			BCLK=64fs	BCLK=32fs	
24576000	X	0'b	0x386F	0x3C6B	8000
X	24576000	1'b			
16384000	X	0'b	0x366D	0x3A69	
X	16384000	1'b			
24576000	X	0'b	0x366D	0x3A69	12000
X	24576000	1'b			
18432000	X	0'b	0x286F	0x2C6B	
X	18432000	1'b			
24576000	X	0'b	0x286F	0x2C6B	16000
X	24576000	1'b			
16384000	X	0'b	0x266D	0x2A69	
X	16384000	1'b			
24576000	X	0'b	0x266D	0x2A69	24000
X	24576000	1'b			
18432000	X	0'b	0x186F	0x1C6B	
X	18432000	1'b			
24576000	X	0'b	0x186F	0x1C6B	32000
X	24576000	1'b			
16384000	X	0'b	0x166D	0x1A69	
X	16384000	1'b			
24576000	X	0'b	0x166D	0x1A69	48000
X	24576000	1'b			
18432000	X	0'b	0x086F	0x0C6B	
X	18432000	1'b			
22579200	X	0'b	0x366D	0x3A69	11025
X	22579200	1'b			
16934400	X	0'b	0x286F	0x2C6B	
X	16934400	1'b			
22579200	X	0'b	0x266D	0x2A69	22050
X	22579200	1'b			
16934400	X	0'b	0x186F	0x1C6B	
X	16934400	1'b			
22579200	X	0'b	0x166D	0x1A69	44100
X	22579200	1'b			
16934400	X	0'b	0x086F	0x0C6B	
X	16934400	1'b			

13. Ordering Information

Table 84. Ordering Information

Part Number	Package	Status
ALC5623-GR	QFN-32 in 'Green' Package (Tray)	Mass Production
ALC5623-GRT	QFN-32 in 'Green' Package (Tape & Reel)	Mass Production

Note 1: See page 6 for Green package and version identification.
Note 2: Above parts are tested under AVDD=AVDD2=3.3V.

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