Winbond Electronics Corp.

3-IN-1 10/100M FAST ETHERNET CONTROLLER

W89C841F/D

3-IN-1 100BASE-TX/FX &
10BASE-T Ethernet Controller

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Revision A3

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Table of Contents-

1. GENERAL DESCRIPTION 4
2. FEATURES 4
3. PIN CONFIGURATIONS 6
4. PIN DESCRIPTION 9
   - PCI Interface 9
   - Power Management Interface 14
   - BootROM/Flash and EEPROM Interface 15
   - Transceiver Interface 19
   - LED Interface 20
   - Configuration and Test Interface 20
   - Power Pins 20
5. BLOCK DIAGRAM 23
6. SYSTEM DIAGRAM 24
7. FUNCTIONAL DESCRIPTION 25
   - Operation Mode Configuration 25
   - Direct Memory Access Function 25
   - Media Access Control (MAC) Function 26
   - Full Duplex and Half Duplex Function 26
   - Network Media Speed Function 26
   - Flow Control in Full Duplex Mode 26
   - Priority Tagged Frame Supporting QOS 26
   - EEPROM Auto-load and Software Programming Function 27
   - BootROM Read and Flash Programming Function 30
   - MII Management Function 32
   - System Resource Configuring 32
   - Power Management Function 33
8. CONFIGURATION REGISTERS 33
   - Configuration Register Mapping 34
9. FUNCTION REGISTERS 47
   - Cxx Function Registers 47
   - Dxx Function Registers 62
   - MII Management Registers 79
10. ELECTRICAL CHARACTERISTICS 90
   - Absolute Maximum Ratings 90
   - Power Supply 90
   - DC Characteristics 90
   - AC Characteristics 91
11. PACKAGE DIMENSIONS 100
   - W89C841F: 128L QFP (14 x 20 x 2.75 mm footprint 3.2 mm) 100
   - W89C841D: 128L LQFP (14 x 20 x 1.4 mm) 101

1. GENERAL DESCRIPTION

W89C841F is a highly integrated PCI Fast Ethernet MAC controller with embedded Ethernet transceiver for 100BaseTX, 100BaseFX and 10BaseT. It is compliant with IEEE 802.3, 802.3u specification. Auto cross-over function is supported on TP terminal and the network status of W89C841F is indicated by 3 LED pins. W89C841F supports full/half duplex, asymmetrical flow control operation compliant with IEEE 802.3x and VLAN tagged frame compliant with IEEE 802.1p.

According to different applications, W89C841F can be configured into one of 3 modes to operate by setting the pins CONFIG[1:0] and ModeSel[2:0] after power-on reset. The 3 operational modes of W89C841F are listed as below.

1. PCI Ethernet MAC controller with internal Ethernet PHYceiver.
2. Pure PCI Ethernet MAC Controller
3. Pure 10/100M PHYceiver

W89C841F provides a host bus interface complying with the PCI local bus specification R2.2, Mini PCI Specification R1.0 and CardBus. W89C841F plays as a bus master role to improve network performance and reduce the bus utilization. There are built-in 2K bytes TX FIFO and 2K bytes RX FIFO to store data. The DMA controller handles the data transfer between the host memory and the FIFOs. The data received from network are queued into the RX FIFO then directly moved into the host memory through the PCI bus. On the other hand, the transmitted data are fetched from the host memory and directly queued into the transmit FIFO. No extra on-board memory is needed for data buffering during operation.

For PC99/2001, W89C841F implements power management function that are compliant with Advanced Configuration and Power Interface (ACPI) specification R1.0, PCI Power Management Interface specification R1.1 and Network Device Class Power Management Reference specification V1.0a. W89C841F supports $D3_{cold}$ power management state if auxiliary power is detected. 3 types of wakeup events are acceptable like link status change, Magic Packet and 5 sets of wake-up frames.

EEPROM (93C46) is supported by W89C841F to store configuration and Vital Product Data (VPD) information. The length of VPD information is up to 64 bytes. W89C841F can access the CardBus information Structure (CIS) information that is stored at EEPROM (93C56) or BootROM. W89C841F also supports BootROM/Flash interface to read/write BootROM or Flash memory.

2. FEATURES

- Integrated Fast Ethernet MAC controller with10/100M Ethernet transceiver in one chip
- Supports MII interface for programmable single PHYceiver or single MAC controller
- Complies with IEEE 802.3, 802.3u specification
- Supports 10BAST-T, 100BASE-TX and 100BASE-FX
- Supports auto cross-over operation
- Supports half duplex and full duplex for 10/100M operation
- Supports flow control for full duplex mode compliant with IEEE 802.3x

- Complies with IEEE802.3ac, 802.1Q for VLAN-tagged frame
- Supports LED pins for network activity indication
- Configurable to PCI, MiniPCI or CardBus bus interface
- Supports PCI/MiniPCI bus master mode for DMA operation, fully compliant with PCI Local Bus Specification R2.2 and Mini PCI Specification R1.0
- Supports CardBus Information Structure (CIS)
- Supports 25 to 33 MHz PCI clock speed
- Compliant with APCI R1.0, PCI power management R1.1 and Network device Class Power management Reference specification V1.0a
- Supports power management event asserted from $D3_{(cold)}$ device state with auxiliary power existing
- Supports wakeup function for Link status change, Magic Packet and 5 sets of wakeup frames
- Supports Vital Product Data (VPD) data structure up to 64 Bytes
- Supports 2 sets of independent embedded 2K bytes FIFO for transmit and receive
- Flexible multicast address filtering modes
  - 64-bit hash-table
  - All multicast and promiscuous
- Supports 25 MHz crystal or oscillator as internal clock source
- Provides EEPROM (93C46 or 93C56) to store configuration parameters, VPD, and CIS information
- Supports 8KB to 256 KB BootROM interface for both PROM and Flash memory
- 3.3V powered I/Os with 5V tolerant inputs
- Packaged in 128-pin PQFP for W89C841F/ LQFP for W89C841D

3. PIN CONFIGURATIONS

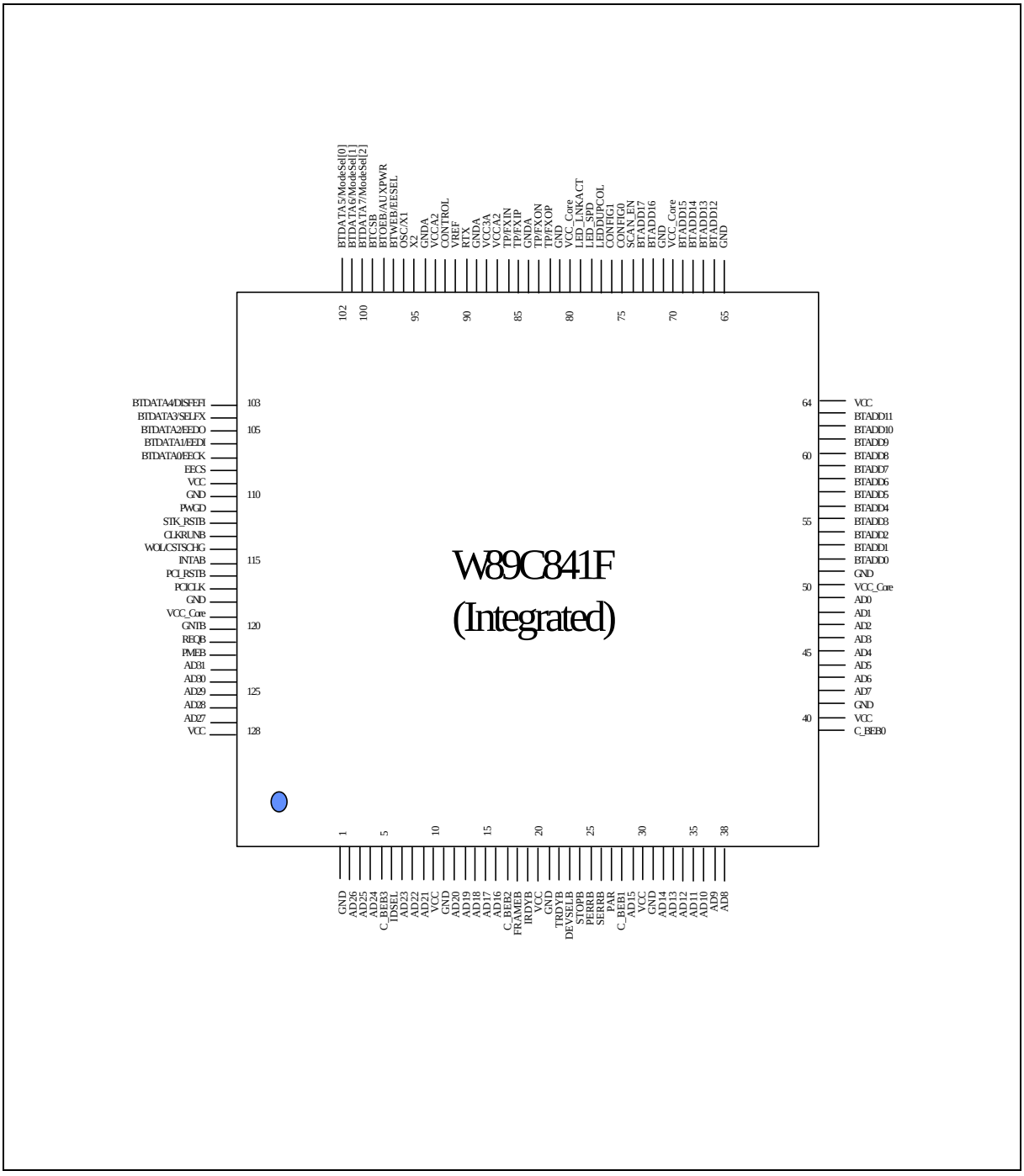


Figure 1. W89C841F Pin Configuration (Integrated)

Pin Configurations, continued

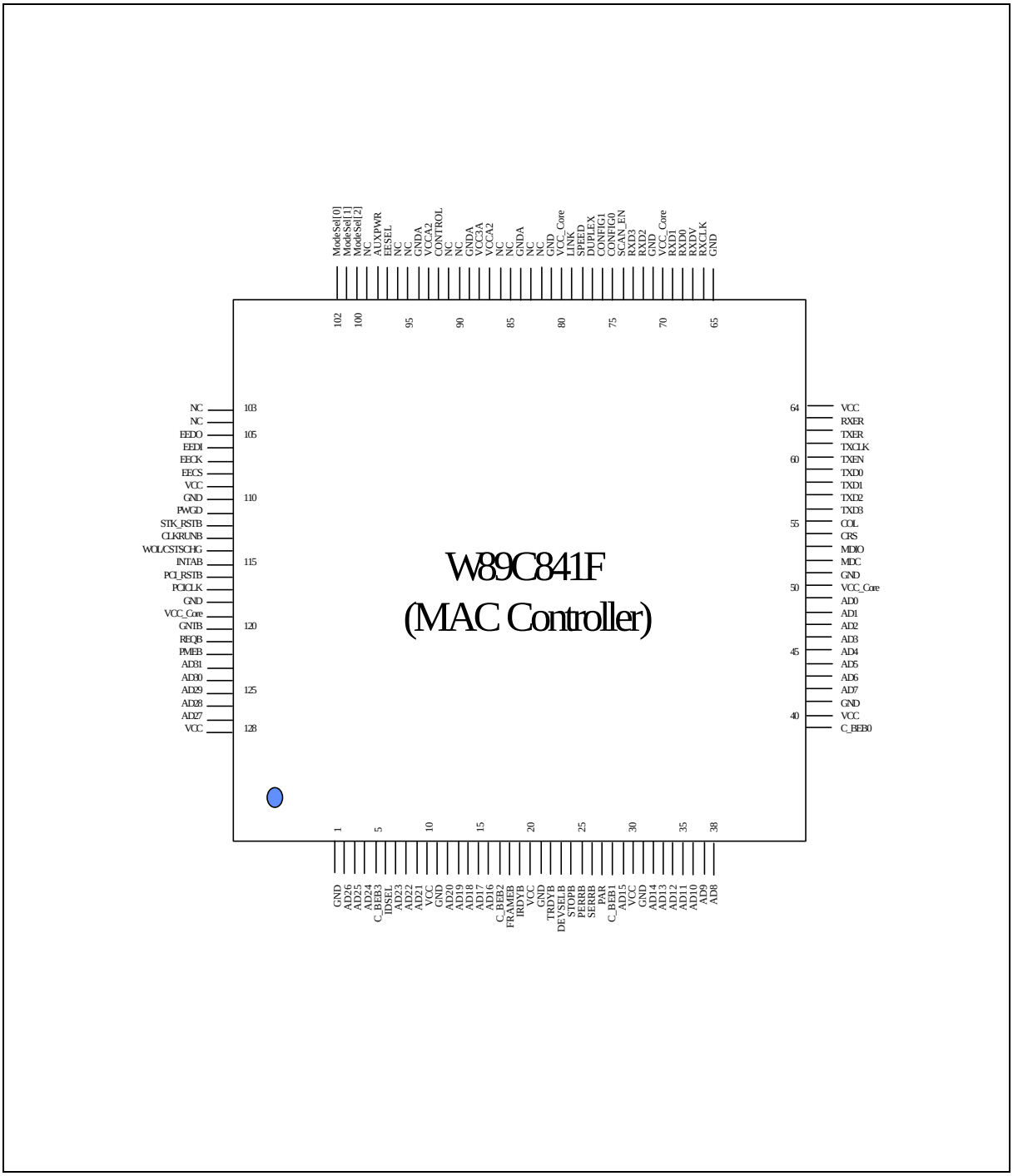
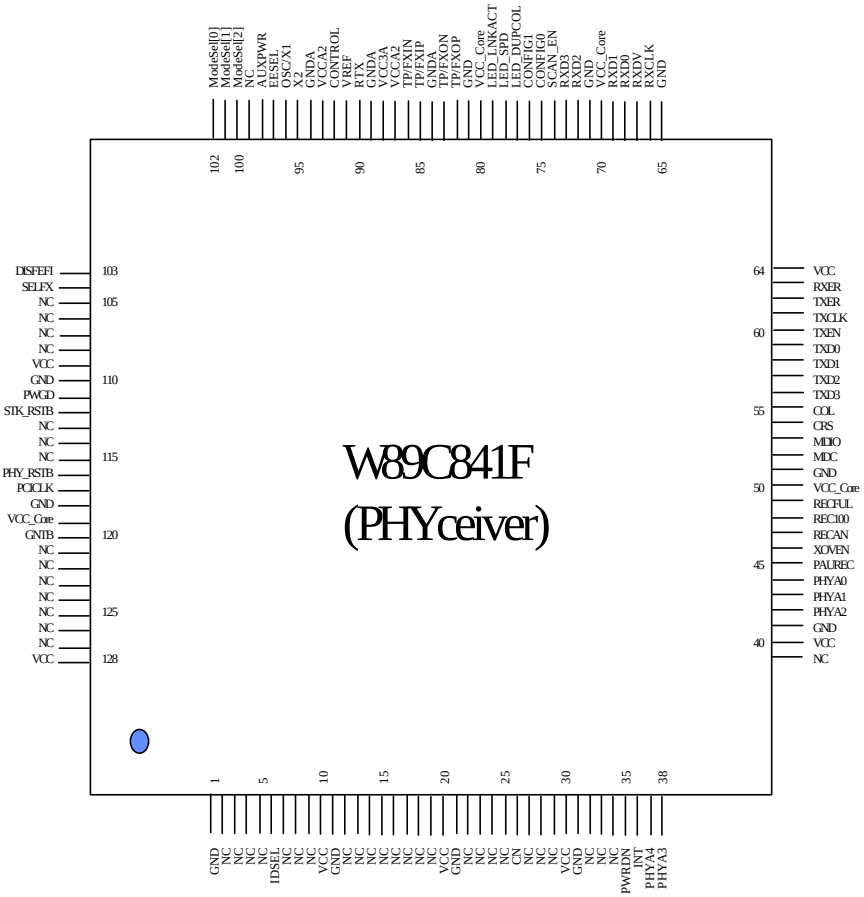


Figure 1. W89C841F Pin Configuration (MAC Controller)

Pin Configurations, continued


W89C841F
(PHYceiver)
ModeSel[0]
ModeSel[1]
ModeSel[2]
NC
LUXPWR
EESEL
OSC/X1
X2
GNDA
VCCA2
CONTROL
VREF
RTX
GNDA
VCC3A
VCCA2
TP/FXIN
TP/FXIP
GNDA
TP/FXON
TP/FXOP
GND
VCC_Core
LED_LNKACT
LED_SPD
LED_DUPCOL
CONFIG1
CONFIG0
SCAN_EN
RXD3
RXD2
GND
VCC_Core
RXD1
RXD0
RXDV
RXCLK
GND
DISFEFI
SELFX
NC
NC
NC
NC
NC
VCC
GND
PWGD
STK_RSTB
NC
NC
NC
PHY_RSTB
PCICLK
GND
VCC_Core
GNTB
NC
NC
NC
NC
NC
NC
NC
VCC
VCC
TXD3
TXD2
TXD1
TXD0
TXEN
TXCLK
RXER
VCC
NC
VCC
GND
PHYA4
PHYA3
INT
PWRDN
NC
NC
NC
GND
VCC
NC
NC
NC
NC
NC
N

4. PIN DESCRIPTION

PCI Interface

SIGNAL NAME	PIN TYP.	PIN NO.	DESCRIPTION
PCICLK	I	117	PCI Clock Input A. Normal and MAC mode W89C841F supports PCI clock rate ranged from 25 MHz to 33 MHz continuously. All PCI signals except PCI_RSTB and INTAB are referenced on the rising edge of this clock. B. PHYceiver mode This pin should be pulled low.
PCI_RSTB/ PHY_RSTB	I	116	PCI Hardware Reset Signal (Normal and MAC mode) When asserted (active low), all PCI output pins of W89C841F will be in high impedance state, and all open drain signals will be floated. The configurations inside W89C841F will be in its initial state. This signal must be asserted for a period of at least 10 PCI clocks to correctly take effect of a reset on hardware. PHYceiver Reset (PHYceiver Mode) This pin is used as to reset PHYceiver.
AD[31:12]	IO/TS	123 – 127, 2 – 4, 7 – 9, 12 – 16, 29, 32 – 34	PCI Multiplexed Address[31:12] and Data Bus[31:12] During the first cycle that FRAMEB asserts, they act as an address bus; on the other cycles, they are switched to be a data bus.
AD[11]/ PWRDN	IO/TS/ I	35	PCI Multiplexed Address[11] and Data Bus[11] (Normal and MAC mode) Power Down Enable (PHYceiver Mode) 1: Power Saving. 0: Normal.
AD[10]/ INT	IO/TS/ O	36	PCI Multiplexed Address[10] and Data Bus[10] (Normal and MAC mode) PHY Interrupt (PHYceiver Mode) Output low that is asserted to indicate an active interrupt event has occurred.

PCI Interface, continued

SIGNAL NAME	PIN TYP.	PIN NO.	DESCRIPTION
AD[9:5]/ PHYA[4:0]	IO/TS/ I	37 – 38, 42 – 44	PCI Multiplexed Address[9:5] and Data Bus[9:5] (Normal and MAC mode) PHY Address (PHYceiver Mode) These pins indicate PHYceiver's address used for MII magement function
AD[4]/ PAUREC	IO/TS/ I	45	PCI Multiplexed Address[4] and Data Bus[4] (Normal and MAC mode) Pause Capability Recommend (PHYceiver Mode) This pin is recommended value for capability at full duplex operation. 1: With pause capability 0: No pause capability
AD[3]/ XOVEN	IO/TS/ I	46	PCI Multiplexed Address[3] and Data Bus[3] (Normal and MAC mode) Auto Cross Over Enable (PHYceiver Mode) In twist pair mode, this pin controls the function of cross over. 1: Enable 0: Disable
AD[2]/ RECAN	IO/TS/ I	47	PCI Multiplexed Address[2] and Data Bus[2] (Normal and MAC mode) Auto Negotiation Enable (PHYceiver Mode) 1: Enable 0: Disable
AD[1]/ REC100	IO/TS/ I	48	PCI Multiplexed Address[1] and Data Bus[1] (Normal and MAC mode) Recommend 100M (PHYceiver Mode) 1: 100M 0: 10M
AD[0]/ RECFUL	IO/TS/ I	49	PCI Multiplexed Address[1] and Data Bus[1] (Normal and MAC mode) Recommend Duplex (PHYceiver Mode) 1: Full Duplex 0: Half Duplex

PCI Interface, continued

SIGNAL NAME	PIN TYP.	PIN NO.	DESCRIPTION
C_BEB[3:0]	IO/TS	5, 17, 28, 39	Multiplexed Command and Byte Enables These signals are driven by current bus master. During address phase, they mean a bus command. On the other phase, they present the byte enable of the transaction.
PAR	IO/TS	27	Parity Signal This PAR represents the even parity across AD[31:0] and C_BEB[3:0]. It has the same timing as AD[31:0] but is delayed by one clock.
FRAMEB	IO/STS	18	PCI Cycle Frame The current bus master asserts FRAMEB to indicate the beginning and duration of a bus access. This signal keeps asserted while the current transaction is ongoing and keeps deasserted to indicate that the next data phase is the final data phase.
IRDYB	IO/STS	19	Initiator Ready The IRDYB is asserted by the current initiator to indicate the ability to complete the data transfer at the current data phase. The initiator asserts IRDYB to indicate the valid write data, or to indicate it is ready to accept the read data. More than or exactly one wait state will be inserted if IRDYB is deasserted during the current transaction. Data is transferred at the clock rising edge when both IRDYB and TRDYB are asserted at the same time.
TRDYB	IO/STS	22	Target Ready Asserted by the current target to indicate ability to complete data transfer at the current data phase. When W89C841F is operating at the bus slave mode, it asserts TRDYB to indicate that the valid read data presents on the bus or to indicate it is ready to accept data. Wait states will be inserted if TRDYB is deasserted. Data is transferred at the rising edge of the PCI clock when IRDYB and TRDYB are both asserted at the same time.
STOPB	IO/STS	24	PCI Stop Asserted by the current target to request PCI bus master to stop the current transaction.

PCI Interface, continued

SIGNAL NAME	PIN TYP.	PIN NO.	DESCRIPTION
IDSEL	I	6	PCI Initialization Device Select A. Normal and MAC mode Asserted by host to signal the configuration access request to W89C841F. B. PHYceiver mode This pin should be pulled to low.
DEVSELB	IO/STS	23	PCI Device Select Asserted by the current target to indicate that it has finished decoding its address as the current access target. When W89C841F is the current master, it checks if the target asserted this signal within 5 PCI clocks after having issued command. If not, W89C841F will abort the access operation, releases PCI bus access right and acts no more bus master. When W89C841F is the target, it asserts DEVSELB in a medium speed, i.e., within 2 clocks.
REQB	O/TS	121	PCI Request Asserted by W89C841F to request bus ownership. REQB will be tri-stated when RSTB asserted.
GNTB	I/TS	120	PCI Grant A. Normal and MAC mode Asserted by host to grant that W89C841F have got the bus ownership. When RSTB asserted, W89C841F will ignore GNTB. B. PHYceiver mode This pin should be pulled to high.
PERRB	IO/STS	25	PCI Parity Error Asserted by the current data receiptor. When W89C841F acts the bus master, if a data parity error is detected and the parity error response bit (F04/FCS[6]) is also set, it will set both bits of F04/FCS[24] and C14/CISR[13] as 1 to terminate the current transaction after the current data phase is finished. When W89C841F acts the target, if a data parity error is detected and the bit F04/FCS[6] is set, it will assert PERRB only.

PCI Interface, continued

SIGNAL NAME	PIN TYP.	PIN NO.	DESCRIPTION
SERRB	O/OD	26	System Error This pin is asserted with one PCI clock width within two PCI clocks after an address parity error is detected, and keeps in high impedance state when idle. The interrupt function caused by this event is gated by the bits in F04/FCS register. W89C841F will assert SERRB and will set a high to the Detect Parity Error bit F04/FCS[31] and the Signal System Erro bit F04/FCS[30] if an address parity error is detected and SERRB enable bit F04/FCS[8] is previously set to 1. The Bus Error Status bit C14/CISR[13] will be set to high if both an address parity error is detected and the parity error response bit F04/FCS[6] is set to high.
INTAB	O/OD	115	Interrupt A INTAB is asserted when any one of unmasked interrupt bits in C14/CISR is set. It keeps asserted until all of the unmasked interrupt bits is cleared.

Power Management Interface

SIGNAL NAME	PIN TYP.	PIN NO.	DESCRIPTION
STK_RSTB	I/PU	112	Sticky Reset Signal A. Normal and MAC mode Sticky_ResetB is a hardware reset signal which is generated from auxiliary power circuit if motherboard supports auxiliary power. So W89C841F can generate PMEB from $D3_{(cold)}$ state to D0 state transition and preserve PME context bits: PME_Status and PME_Enable. B. PHYceiver mode This pin should be floating.
PWGD	I	111	Power Good A. Normal and MAC mode When PWGD = 1, W89C841F is put in normal operation mode. When PWGD = 0, it isolates any PCI input and has all PCI outputs kept in high impedance state. The PCI bus power can be off by operating system. B. PHYceiver mode This pin should be pulled to high.
PMEB	O/OD	122	Power Management Event The PMEB signal indicates that a power management event has occurred, i.e. there is a magic packet received in suspend mode of host.
CLKRUNB	I/OD	113	Clock Run CLKRUNB is used to request starting or speeding up the PCI clock. It also indicates the PCI clock status. W89C841F requests the central resource to start, speed up, or maintain the PCICLK by the assertion of CLKRUNB. For the central resource, CLKRUNB is an S/T/S signal. The central resource is responsible for maintaining CLKRUNB asserted and for driving it high to deasserted state.

Power Management Interface, continued

SIGNAL NAME	PIN TYP.	PIN NO.	DESCRIPTION
WOL/ CSTSCHG	O	114	Wake on LAN Signal The WOL signal indicates that a wake up event (Magic Packet, Link Status change and Wake-up frame) has been received. It is used to inform motherboard to execute wake-up process. The motherboard must support Wake-On-LAN. There are 4 types of output: active high (default), active low, positive pulse, negative pulse. CSTSCHG signal: This signal is used in CardBus application only and is used to inform motherboard to execute wake-up process whenever there is PMEB occurs. It is always an active high signal.

BootROM/Flash and EEPROM Interface

SIGNAL NAME	PIN TYP.	PIN NO.	PIN DESCRIPTION
BtAdd[17:14]/ RXD[3:0]_MAC/ RXD[3:0]_PHY	I/O/ I/ O	73, 72, 69, 68	BootROM Address (Normal Mode) These pins are used as ROM address pins. MII Receive Data (MAC mode) These pins are used to input MII RXD signals. MII Receive Data (PHYceiver mode) These pins are used to output MII RXD signals.
BtAdd[13]/ RXDV_MAC/ RXDV_PHY	I/O/ I/ O	67	BootROM Address (Normal Mode) This pin is used as ROM address pin. MII Receive Data Valid (MAC mode) This pin is used to input MII RXDV signal. MII Receive Data Valid (PHYceiver mode) This pin is used to output MII RXDV signal.
BtAdd[12]/ RXCLK_MAC/ RXCLK_PHY	I/O/ I/ O	66	BootROM Address (Normal Mode) These pins are used as ROM address pin. MII Receive Clock (MAC mode) This pin is used to input MII RXCLK signal. MII Receive Clock (PHYceiver mode) This pin is used to output MII RXCLK signal.

BootROM/Flash and EEPROM Interface, continued

SIGNAL NAME	PIN TYP.	PIN NO.	PIN DESCRIPTION
BtAdd[11]/ RXER_MAC/ RXER_PHY	I/O/ I/ O	63	BootROM Address (Normal Mode) These pins are used as ROM address pin. MII Receive Error (MAC mode) This pin is used to input MII RXER signal. MII Receive Error (PHYceiver mode) This pin is used to output MII RXER signal.
BtAdd[10]/ TXER_MAC/ TXER_PHY	I/O/ O/ I	62	BootROM Address (Normal Mode) These pins are used as ROM address pin. MII Transmit Error (MAC mode) This pin is used to output MII TXER signal. MII Transmit Error (PHYceiver mode) This pin is used to input MII TXER signal.
BtAdd[9]/ TXCLK_MAC/ TXCLK_PHY	I/O/ I/ O	61	BootROM Address (Normal Mode) These pins are used as ROM address pin. MII Transmit Clock (MAC mode) This pin is used to input MII TXCLK signal. MII Transmit Error (PHYceiver mode) This pin is used to output MII TXCLK signal.
BtAdd[8]/ TXEN_MAC/ TXEN_PHY	I/O/ O/ I	60	BootROM Address (Normal Mode) These pins are used as ROM address pin. MII Transmit Enable (MAC mode) This pin is used to output MII TXEN signal. MII Transmit Enable (PHYceiver mode) This pin is used to input MII TXEN signal.
BtAdd[7:4]/ TXD[3:0]_MAC/ TXD[3:0]_PHY	I/O/ O/ I	59, 58, 57, 56	BootROM Address (Normal Mode) These pins are used as ROM address pins. MII Transmit Data (MAC mode) These pins are used to output MII TXD signals. MII Transmit Data (PHYceiver mode) These pins are used to input MII TXD signals.

BootROM/Flash and EEPROM Interface, continued

SIGNAL NAME	PIN TYP.	PIN NO.	PIN DESCRIPTION
BtAdd[3]/ COL_MAC/ COL_PHY	I/O/ I/ O	55	BootROM Address (Normal Mode) This pin is used as ROM address pin. MII Collision (MAC mode) This pin is used to input MII COL signal. MII Collision (PHYceiver mode) This pin is used to output MII COL signal.
BtAdd[2]/ CRS_MAC/ CRS_PHY	I/O/ I/ O	54	BootROM Address (Normal Mode) This pin is used as ROM address pin. MII Carrier Sense (MAC mode) This pin is used to input MII CRS signal. MII Carrier Sense (PHYceiver mode) This pin is used to output MII CRS signal.
BtAdd[1]/ MDIO_MAC/ MDIO_PHY	I/O	53	BootROM Address (Normal Mode) This pin is used as ROM address pin. MII Management Data (MAC mode) This pin is used to input/output MII MDIO signal. MII Management Data (PHYceiver mode) This pin is used to input/output MII MDIO signal.
BtAdd[0]/ MDC_MAC/ MDC_PHY	I/O/ O/ I	52	BootROM Address (Normal Mode) These pins are used as ROM address pin. MII Management Clock (MAC mode) This pin is used to output MII MDC signal. MII Management Clock (PHYceiver mode) This pin is used to input MII MDC signal.
BtData[7:5]/ ModeSel[2:0]	I/O	100 – 102	BootROM Data[7:5] These pins are used as ROM data pins. Mode Selection When power-on, these pins are used as input pins to latch the setting value of ModeSel. Mode / CONFIG / ModeSel Normal / 00 / 000 MAC Controller / 01 / 011 PHYceiver / 10 / 000 Testing / 11 / xxx

BootROM/Flash and EEPROM Interface, continued

SIGNAL NAME	PIN TYP.	PIN NO.	PIN DESCRIPTION
BtData[4]	I/O	103	BootROM Data[4] A. Normal mode This pin is used as ROM data pin. B. PHYceiver mode and MAC mode This pin should be pulled to low.
BtData[3]/ SELFX	I/O/ I	104	BootROM Data[3] This pin is used as ROM data pin FX/TX Selection When power-on, this pin is used as input pin to latch the setting value of SELFX. 1: FX mode 0: TX mode
BtData[2]/ EEDO/ PHY_Duplex	I/O/ O	105	BootROM Data[2]/ EEPROM Data Output (Normal mode and MAC mode) This is pin is used for BootROM data pin or EEPROM data output dependent on the bit EESEL of register Dc4/DEEAR. PHY_DUPLEX (PHYceiver mode) This pin output the PHYceiver duplex status. 1: Half Duplex 0: Full Duplex
BtData[1]/ EEDI	I/O	106	BootROM Data[1]/ EEPROM Data Input This is pin is used for BootROM data signal or EEPROM data input dependent on the bit EESEL of register Dc4/DEEAR.
BtData[0]/ EECK	I/O	107	BootROM Data[0]/ EEPROM Data Clock This is pin is used for BootROM data signal or EEPROM data clock dependent on the bit EESEL of register Dc4/DEEAR.
EECS	O	108	EEPROM Chip Select
BtCSB	O	99	BootROM Chip Select

BootROM/Flash and EEPROM Interface, continued

SIGNAL NAME	PIN TYP.	PIN NO.	PIN DESCRIPTION
BtOEB/ AuxPWR	I/O	98	BootROM Read Enable/ Auxiliary Power Detection A. Normal mode and MAC mode After power on latch, auxiliary power is automatically detected by W89C841F. If auxiliary power is detected to be high, wake-up event generation from D3(cold) to D0 (uninitialized) state is supported. B. PHYceiver mode This pin should be pulled to low.
BtWEB/ EESel	I/O	97	BootROM Write Enable/ EEPROM Type Select A. Normal mode and MAC mode After power on latch, EEPROM type is detected by W89C841F. If it is high, EEPROM (93C56) is used for CardBus application. Otherwise, EEPROM (93C46) is used in PCI/Mini PCI application. B. PHYceiver mode This pin should be pulled to low.

Transceiver Interface

SIGNAL NAME	PIN TYP.	PIN NO.	PIN DESCRIPTION
TP/FXOP	O	82	Twist Pair / Fiber Transmit Output Positive
TP/FXON	O	83	Twist Pair / Fiber Transmit Output Negative
TP/FXIP	I	85	Twist Pair / Fiber Receive input Positive
TP/FXIN	I	86	Twist Pair / Fiber Receive input Negative
OSC/X1	I	96	25 MHz Crystal/OSC clock input
X2	O	95	Crystal Output Left unconnected when oscillator is chosen for X1 input.
VREF	I	91	RC input for Bias.
RTX	I	90	RC input for Transmitter.
CONTROL	O	92	2.5V Regulator Control Output Drive current below 10 mA.

LED Interface

SIGNAL NAME	PIN TYP.	PIN NO.	PIN DESCRIPTION
LED_ LNKACT	I/O	79	LED_LNKACT 0: Link up without activity. 1: Link fail or activity is on (flash 100 mS)
LED_SPD	I/O	78	LED_SPD 0: 100M. 1: 10M.
LED_ DUPCOL	I/O	77	LED_DUPCOL 0: Full duplex or collision in half duplex (flash 100 mS) 1: Half duplex and no collision.

Configuration and Test Interface

SIGNAL NAME	PIN TYP.	PIN NO.	PIN DESCRIPTION
CONFIG[1:0]	I	76, 75	Configuration 00: Normal mode 01: MAC controller mode (Disable internal PHYceiver and disable Boot ROM function) 10: PHYceiver mode (Disable MAC Controller and Boot ROM function) 11: Reserved for testing
Scan_EN	I	74	Scan Enable Reserved for testing. This pin should be pulled to low.

Power Pins

SIGNAL NAME	PIN TYP.	PIN NO.	PIN DESCRIPTION
VCCA2		87, 93	2.5V Analog Power
VCC3A		88	3.3V Analog Power
GNDA		84, 89, 94	Analog Ground
VCC		10, 20, 30, 40, 64, 109, 128	3.3V I/O Digital Power
VCC_Core		50, 70, 80, 119	2.5V Core Digital Power
GND		1, 11, 21, 31, 41, 51, 65, 71, 81, 110, 118	Digital Ground

Pins Mapping Table

W89C841F can be configured into 3 different operational types. In the following table, it lists the pin mapping of different configuration mode.

NORMAL MODE	MAC CONTROLLER MODE	PHYCEIVER MODE
Config = 00 *ModeSel [2:0] = 000*	*Config = 01* *ModeSel [2:0] = 011*	*Config = 10* *ModeSel [2:0] = 000*
LED_LNKACT	LINK (I)	LED_LNKACT (O)
LED_SPD	SPEED (I)	LED_SPD (O)
LED_DUPCOL	DUPLEX (I)	LED_DUPCOL (O)
BTADD17	RXD3 (I)	RXD3 (O)
BTADD16	RXD2 (I)	RXD2 (O)
BTADD15	RDX1 (I)	RDX1 (O)
BTADD14	RDX0 (I)	RDX0 (O)
BTADD13	RXDV (I)	RXDV (O)
BTADD12	RXCLK (I)	RXCLK (O)
BTADD11	RXER (I)	RXER (O)
BTADD10	TXER (O)	TXER (O)
BTADD9	TXCLK (I)	TXCLK (O)
BTADD8	TXEN (O)	TXEN (I)
BTADD7	TXD0 (O)	TXD0 (I)
BTADD6	TXD1 (O)	TXD1 (I)
BTADD5	TXD2 (O)	TXD2 (I)
BTADD4	TXD3 (O)	TXD3 (I)
BTADD3	COL (I)	COL (O)
BTADD2	CRS (I)	CRS (O)
BTADD1	MDIO (I/O)	MDIO (I/O)
BTADD0	MDC (O)	MDC (I)
BTDATA7	ModeSel[2]	ModeSel[2]
BTDATA6	ModeSel[1]	ModeSel[1]
BTDATA5	ModeSel[0]	ModeSel[0]
BTDATA4	NC	NC

Pins Mapping Table, continued

NORMAL MODE	MAC CONTROLLER MODE	PHYCEIVER MODE
Config = 00 *ModeSel [2:0] = 000*	*Config = 01* *ModeSel [2:0] = 011*	*Config = 10* *ModeSel [2:0] = 000*
BTDATA3	NC	SELFX
BTDATA2/ EEDO	EEDO	PHY_DPULEX
BTDATA1/ EEDI	EEDI	NC
BTDATA0/ EECLK	EECLK	NC
BTCSB	NC	NC
BTOEB	NC	NC
BTWEB	NC	NC
AD11	AD11	PWRDN (I)
AD10	AD10	INT (O)
AD9	AD9	PHYA[4] (I)
AD8	AD8	PHYA[3] (I)
AD7	AD7	PHYA[2] (I)
AD6	AD6	PHYA[1] (I)
AD5	AD5	PHYA[0] (I)
AD4	AD4	PAUREC (I)
AD3	AD3	XOVEN (I)
AD2	AD2	RECAN (I)
AD1	AD1	REC100 (I)
AD0	AD0	RECFUL (I)

5. BLOCK DIAGRAM

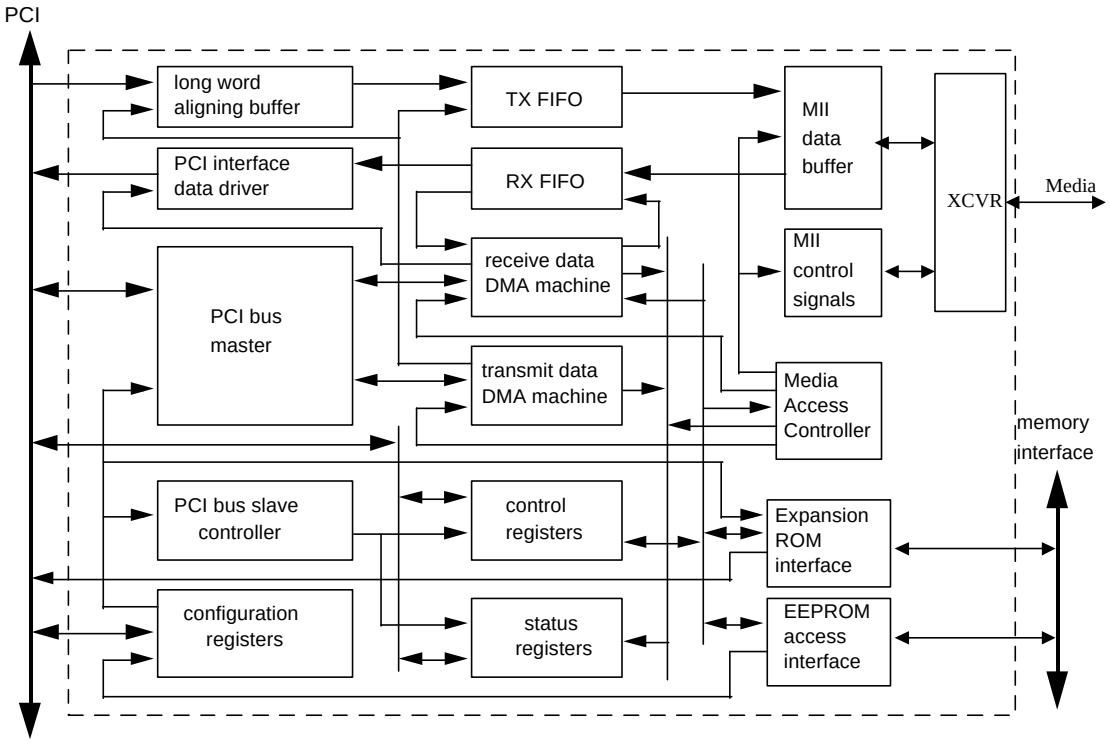


Figure 2. W89C841F Block Diagram

6. SYSTEM DIAGRAM

- NIC product: PCI LAN card, Card bus LAN card, MiniPCI LAN card

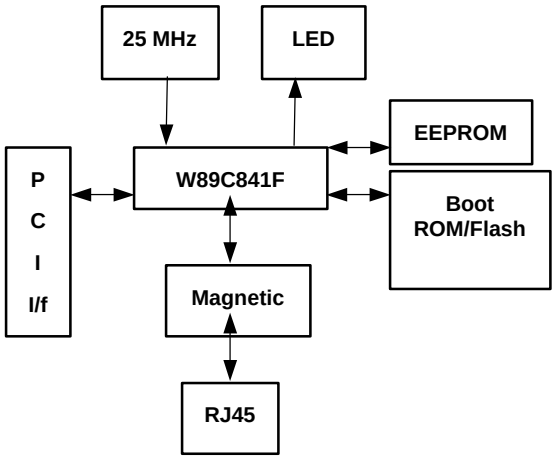


Figure 3. NIC Application

- Home Networking product: HomePNA

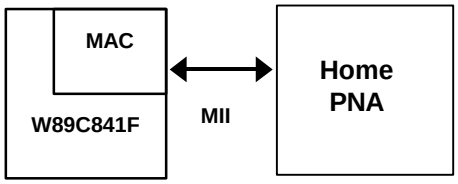


Figure 4. HomePNA Application

- LAN On Mother board: LOM

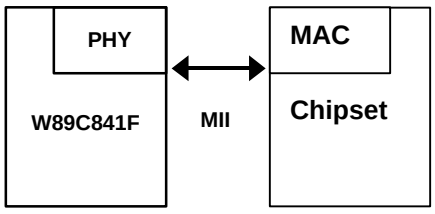


Figure 5. LOM Application

- PCI application: Restore card, Firewall, Education system

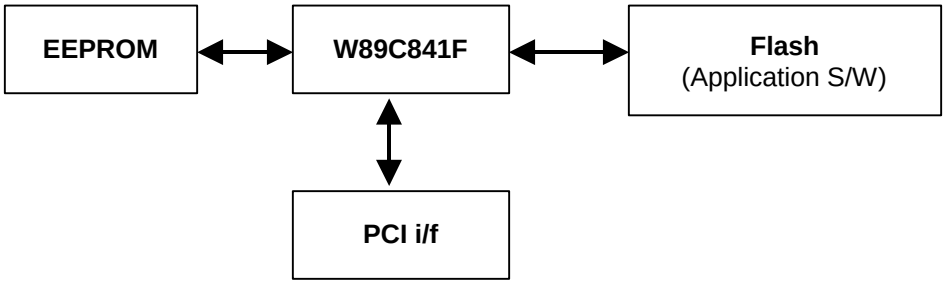


Figure 6. Restore Card Application

7. FUNCTIONAL DESCRIPTION

Operation Mode Configuration

W89C841F can be configured to 3 different operation modes for different applications. In the following table, the assignment of pins CONFIG[1:0] and ModeSel[2:0] is listed.

PIN ASSIGNMENT	NORMAL	MAC CONTROLLER	PHYCEIVER
CONFIG[1:0]	00	01	10
Mode_Sel[2:0]	000	011	000

In the normal mode, W89C841F is used in the NIC application. In the MAC controller mode, W89C841F that is used as a MAC controller plus HomePHY that is used as a transceiver implement a HomePNA card. In the PHYceiver mode, an application like LAN On Motherboard (LOM) is implemented by W89C841F that is used as a single PHYceiver plus PC chipset.

PHYceiver

An internal PHYceiver is embedded in W89C841F. It is compatible with IEEE802.3 10-BAST-T, 100BASE-TX and 100BAST-FX. W89C841F can be configured to twist pair interface or fiber interface. Auto-negotiation and auto-crossover function is supported. W89C841F provides 3 LEDs to indicate Link/Activity, Speed and Duplex/Collision status.

Direct Memory Access Function

On receiving a data packet, the receive DMA function will transfer these data from the internal receive FIFO which has a size of 2k bytes to the host memory with the assistance of the on-chip PCI bus master. During the transaction cycle, the media access controller (MAC) requests the receive DMA state machine to move the data in the receive FIFO onto the PCI bus, and then move it to the host memory.

W89C840F transmit DMA function performs the data transfer from the host memory through on-chip PCI bus master into the internal 2 Kbytes transmit FIFO. The transmit DMA state machine will request the MAC to send out the data in the TX FIFO onto the transmission media.

Media Access Control (MAC) Function

The MAC function of W89C841F fully meets the requirements defined by the IEEE802.3u specification. MAC performs many transmission functions, including the inter-frame spacing function, collision detection, collision enforcement, collision backoff and retransmission. MAC performs the receive functions including the address recognition function, the frame check sequence validation, the frame disassembly, framing and collision filtering.

Full Duplex and Half Duplex Function

In the half duplex mode, the MAC should perform the transmission or reception operation at the different time frame. Simultaneous transmission and reception is not allowed. However, in the time duration from 10 bits time to 16 bits time after the packet is transmitted, the active COL signal is recognized as a SQE test signal but not a collision event. The active signal CRS will be recognized as a loopback carrier sense signal when the MAC is transmitting a packet. The carrier sense lost status is relied on the CRS. Normally, there should not be any carrier sense lost during transmitting if the media and devices are functional. In the full duplex mode, the MAC can perform the transmission and receive operation at the same time. Collision event, SQE lost and carrier sense lost are not defined in the full duplex mode. After auto-negotiation completed, network duplex mode can be decided by internal PHYceiver.

Network Media Speed Function

W89C841F can work at network speed of 100M or 10Mbps. After auto-negotiation completed, network speed can be decided by internal PHYceiver.

Flow Control in Full Duplex Mode

W89C841F supports asymmetrical and symmetrical flow control in full duplex mode compliant with IEEE802.3x. After auto-negotiation completed, W89C841F will decide to operate in which flow control mode (symmetrical, asymmetrical or none).

When the receiving byte counts of RX FIFO is over the high threshold defined at field HTV of register Ddc/DRFCTV[17:9], a pause frame with MAX pause time (FFFFh) is transmitted to prevent the other station keeping on transmitting packets to W89C841F. So W89C841F will not drop packets due to RX FIFO overflow. When the receiving byte count of RX FIFO is below the low threshold defined at field LTV of register Ddc/DRFCTV[8:0], a pause frame with MIN pause time (0000h) is transmitted to let the other station starting to transmit packets to W89C841F.

If W89C841F receives a pause packet with non-zero pause time, the packet transmission ability will be inhibited until the pause time counts down to 0. Pause frame is a flow control packet. It is not a data packet and will be dropped by W89C841F.

Priority Tagged Frame Supporting QOS

A priority tagged frame defined at IEEE 802.1p contains a VLAN tag which indicates the user priority and Null VLAN ID (VID = 0). W89C841F can transmit and receive priority tagged frames to improve the network quality of service if bit VLANEN of register C1c/CNCR is set.

EEPROM Auto-load and Software Programming Function

W89C841F reads configuration parameter from EEPROM and stores these data into the configuration registers and function registers after hardware reset. EEPROM 93C46 or 93C56 will be the choice as the storage device for storing these data according to different application.

In PCI/Mini-PCI application, W89C841F stores configuration parameters and Vital Product Data (VPD) in EEPROM 93C46. Configuration parameters and relative register are listed below:

1) 6 bytes Ethernet address (Register Dcc[31:0] and Dd0[15:0])
2) 1 byte maximum latency (Register F3c[31:24])
3) 1 byte minimum grant (Register F3c[23:16])
4) 2 bytes subsystem ID (Register F2c[31:16])
5) 2 bytes subsystem Vendor ID (Register F2c[15:0])
6) 2 bytes Device ID (Register F00[31:16])
7) 2 bytes Vendor ID (Register F00[15:0])
8) 4 bytes CardBus CIS Pointer (Register F28[31:0])
9) 1 bit Power Management Data Enable
10) 3 bits Auxiliary Current (Register Fdc[24:22])
11) 2 bits Data Scale (Register Fe0[14:13])
12) 6 bytes Power Consumption and Dissipation data for D0, D1 and D3 State (Register Fe0[31:24])
13) 1 bits Power Management Enable (Register D00[6])
14) 1 bit VPD Enable (Register D00[5])
15) 2 bits Bus Type (Register D00[1:0])
16) 1 bit CLKRUN enable (Register D00[11])
17) 1 bit Magic Packet enable (Register D00[10])
18) 3 bits Boot ROM Size (Register Dc0[30:28])
19) 1 byte Base Class Code (Register F08[31:24])
20) 1 byte Subclass code (Register F08[23:16])
21) 1 byte Interface Code (Register F08[15:8]
22) 1 bytes Revision ID (Register F08[7:0]
23) 64 Bytes VPD Data

EEPROM 93C46

ADDRESS	HIGH BYTE (Bit 15 - Bit 8)	LOW BYTE (Bit 7 - Bit 0)
00h	Ethernet Address 1 [15:8]	Ethernet Address 0 [7:0]
01h	Ethernet Address 3 [31:24]	Ethernet Address 2 [23:16]
02h	Ethernet Address 5 [47:40]	Ethernet Address 4 [39:32]
03h	MAXLAT	MINGNT
04h	Subsystem ID (high byte)	Subsystem ID (Low byte)
05h	Subsystem Vendor ID (high byte)	Subsystem Vendor ID (low byte)
06h	Device ID (high byte)	Device ID (low byte)
07h	Vendor ID (high byte)	Vendor ID (low byte)
08h	CardBus CIS pointer (Low Word)	
09h	CardBus CIS pointer (High Word)	
0Ah	PM_Data_En {bit15}	Reserved
0Bh	Aux_Current {bit15 – bit13}	Data_Scale {bit7 – bit6}
0Ch	D0 Power Consumption Data	D0 Power Dissipation Data
0Dh	D1 Power Consumption Data	D1 Power Dissipation Data
0Eh	D3 Power Consumption Data	D3 Power Dissipation Data
0Fh	PM_EN {bit15} VPD_EN {bit14} PCBusType {bit13 – bit12} CKRUN_EN {bit11} MAGP_EN {bit10}	Boot ROM Size {bit7 – bit5}
10h	Base Class Code	Subclass code
11h	Interface Code	Revision ID
12 – 1Fh	Reserved	Reserved
20h – 3Fh	Vital Product Data (VPD)	

In CardBus application, another data structure of CardBus Information Structure (CIS) needs to be stored in the EEPROM 93C56. Totally 128 bytes space addressed from 40h to 7Fh are reserved for CIS use.

EEPROM 93C56

ADDRESS	HIGH BYTE (Bit 15 - Bit 8)	LOW BYTE (Bit 7 - Bit 0)
00h	Ethernet Address 1 [15:8]	Ethernet Address 0 [7:0]
01h	Ethernet Address 3 [31:24]	Ethernet Address 2 [23:16]
02h	Ethernet Address 5 [47:40]	Ethernet Address 4 [39:32]
03h	MAXLAT	MINGNT
04h	Subsystem ID (high byte)	Subsystem ID (Low byte)
05h	Subsystem Vendor ID (high byte)	Subsystem Vendor ID (low byte)
06h	Device ID (high byte)	Device ID (low byte)
07h	Vendor ID (high byte)	Vendor ID (low byte)
08h	CardBus CIS pointer (Low Word)	
09h	CardBus CIS pointer (High Word)	
0Ah	PM_Data_En {bit15}	Reserved
0Bh	Aux_Current {bit15 – bit13}	Data_Scale {bit7–bit6}
0Ch	D0 Power Consumption Data	D0 Power Dissipation Data
0Dh	D1 Power Consumption Data	D1 Power Dissipation Data
0Eh	D3 Power Consumption Data	D3 Power Dissipation Data
0Fh	PM_EN {bit15} VPD_EN {bit14} PCBusType {bit13 – bit12} CLKRUN_EN {bit11} MAGP_EN {bit10}	Boot ROM Size {bit7– bit5}
10h	Base Class Code	Subclass code
11h	Interface Code	Revision ID
12h – 1Fh	Reserved	Reserved
20h – 3Fh	Vital Product Data (VPD)	
40h – 7Fh	CardBus Information Structure	

Dc4/DEEAR register is used as an interface to access the data between the system and EEPROM. The following table lists the reading and writing steps for EEPROM.

COMMAND	STEP
EEPROM Read	Set EEPROM access bit EESEL to 1. Set EEPROM offset address to bits EEOA Set EEPROM Read command to bit EERW Set Start EEPROM Read/write command to bit StartEERW Waiting for read operation completed until bit StartEERW change to 0. Read data from bits EEData.
Disable EEPROM Write Protection	Set EEPROM access bit EESEL to 1. Set EEPROM write protection disable command to bit EERW Set Start EEPROM Read/write command to bit StartEERW Waiting for write protection disable operation completed until bit StartEERW change to 0.
EEPROM Write	1) Set EEPROM access bit EESEL to 1. 2) Set EEPROM offset address to bits EEOA 3) Set EEPROM Data to bits EEData 4) Set EEPROM write command to bit EERW 5) Set Start EEPROM Read/write command to bit StartEERW 6) Waiting for write operation completed until bit StartEERW change to 0.
Enable EEPROM Write Protection	Set EEPROM access bit EESEL to 1. Set EEPROM write protection enable command to bit EERW Set Star EEPROM Read/Write command to bit StartEERW. Waiting for bit StartEERW change to 0.

BootROM Read and Flash Programming Function

W89C841F can address up to 256 Kbytes memory space for the on-board BootROM or Flash memory device. The on-board BootROM device will be mapped into the host memory by the system BIOS. W89C841F will return the mapped memory address depending on the field BootROM size select of register Dc0/DBRAR[30:28]. This field is loaded from EEPROM after power on reset. The relationship between the return value from the register F30/FERBA and the field BootROM size select of register Dc0/DBRAR[30:28] is listed as the following table.

ROM SIZE	DC0/DBRAR[30:28]	F30/FERBA
None	000b	0000_0000h
None	001b	0000_0000h
8 Kbytes	010b	FFFF_E001h
16Kbytes	011b	FFFF_C001h
32Kbytes	100b	FFFF_8001h
64Kbytes	101b	FFFF_0001h
128Kbytes	110b	FFFE_0001h
256Kbytes	111b	FFFC_0001h

The address decoder of W89C841F for accessing the on-board BootROM will be enabled if both the bit 0 of F30/FERBA and the bit 1 of F04/FCS are set to high at the same time. On-board Boot ROM data will be fetched by W89C841F and are loaded into the host memory. On the other hand, the address decoder will be disabled if the bit 0 of F30/FERBA is reset to 0. Under this case, W89C841F will ignore the Dc0/DBRAR, no matter what content it has.

Usually on-board BootROM data can be read by the system BIOS during host system booting or power-on reset. W89C841F also provides an access method by register Dc0/DBRAR and Dc0/DEEAR[31] to read or write Flash memory on Restore Card applications. If BootROM interface is chosen to be accessed, the bit EESEL of register Dc4/DEEAR[31] must be set to 0 at first. The read and write process for BootROM or Flash through register Dc0/DBRAR is listed in the following table.

COMMAND	STEP
Read	1) Set BootROM access bit EESEL (Dc4/DEEAR[31]) to 0. 2) Set the BootROM/Flash offset address to bits BROMA 3) Set BootROM/Flash read control bit BROMRD to 1. 4) Waiting for read operation completed until bit BROMRD change to 0. 5) Read back the data from bits BROMD
Write	1) Set BootROM access bit EESEL (Dc4/DEEAR[31]) to 0. 2) Set the Boot ROM offset address to bits BROMA 3) Write data to bits BROMD 4) Set BootROM write control bit BROMWR to 1. 5) Waiting for write operation completed until bit BROMWR change to 0.

The bit BROMRD (bit 27) and bit BROMWR (bit 26) of the register Dc0/DBRAR should not be set to 1 at the same time. In the case of both of the bit BROMRD and bit BROMWR are 1, it will not properly initialize the read or the write operation for ROM device. The application program can check the contents of the register Dc0/DBRAR to know if the read or write operation is already completed or not. W89C841F will start the read or the write operation when the bit BROMRD or bit BROMWR are set to high and will be reset automatically after the read/write operation is completed. For the write operation, the software driver should not start up the next write data request until the bit BROMWR of Dc0/DBRAR[26] is reset to 0 by W89C841F. For the read operation, the read data will be valid only if the bit BROMRD of the register Dc0/DBRAR[27] is reset to 0 by W89C841F.

MII Management Function

W89C841F supports MII management function through register Dc8/DMMAR to access the MII management registers of the internal PHYceiver (Normal mode) or external PHYceiver (MAC controller mode). The following table lists the read and write access steps for MII management registers.

COMMAND	STEP
Read	Set PHY address to bits PHYADD to default value 01h. Set PHY register address to bits REGADD Set MDIO read command to bit MDIORW Set Start MDIO Read/write command to bit StartMDIORW Waiting for read operation completed until bit StartMDIORW change to 0. Read data from bits PHYData.
Write	Set PHY address to bits PHYADD to default value 01h Set PHY register address to bits REGADD Set PHY data to bits PHYData Set MDIO write command to bit MDIORW Set Start MDIO Read/write command to bit StartMDIORW 6) Waiting for write operation completed until bit StartMDIORW change to 0.

System Resource Configuring

W89C841F will require the I/O space, memory space for function Cxx and Dxx registers and the interrupt line to perform the communication between the network and the host.

In PCI/MiniPCI system, Cxx and Dxx registers can be mapped to either system I/O space or memory space. The following table lists the relative mapping address in double word aligned.

	I/O SPACE ADDRESS	MEMORY SPACE ADDRESS
Cxx Registers	00h – 3Ch	000h – 03Ch
Dxx Registers	00h – FFh	100h – 1FCh

In CardBus system, Cxx and Dxx registers can be mapped to either system I/O space or memory space. But CIS data can be mapped to memory space only. The following table lists the relative mapping address in double word.

	I/O SPACE ADDRESS	MEMORY SPACE ADDRESS
Cxx Register	00h – 3Ch	000h – 03Ch
CIS Data	X	080h – 0FCh
Dxx Register	00h – FFh	100h – 1FCh

W89C841F uses only one interrupt pin INTAB. However, the interrupt line resource assignment is determined by the system BIOS by writing the related data into the bits ILINE of register F3C/FIR[7:0].

Power Management Function

W89C841F supports power management function that is compliant with ACPI R1.0, PCI power management R1.1 and Network Device Class Power management Reference specification V1.0a. Power management state from D0, D1, D3(hot) is provided by W89C841F. But whether the D3(cold) power management state is provided is dependent on the auxiliary power detected or not after power on reset. Power management D2 is not supported by W89C841F.

PME context consists of the bit PME_EN of register Fe0/FPMR1[8] and bit PME_STS of register Fe0/FPMR1[15]. If D3(cold) power management state is supported, PME context will be kept valid. When PMEB is asserted, it must continue to drive the signal low until software explicitly either clears the PME Status bit or clears the PME Enable bit.

Wake-On-LAN Function

If the power management function is enabled, 3 types of wake-up events can be accepted by W89c841F to acknowledge driver that wake-up event has happened. These wake-up events are defined as:

- Link status changed
- Magic Packet
- Wake-up frame

8. CONFIGURATION REGISTERS

The general attributes of the PCI configuration registers implemented in W89C841F are described as the following.

1) Writes to the reserved configuration registers are treated as no-op. The bus access will complete without affecting any data in W89C841F internal registers.
2) Read from the reserved or un-implemented registers will be returned 0 value.
3) SoftReset has no effect on the PCI configuration registers.
4) HardReset will clear the PCI configuration registers.
5) The implemented configuration registers support any byte enable combination access.

6) Burst access to the configuration registers will be terminated after 1st data transfer completed with a disconnect without data.

The following table outlined all the PCI configuration registers inside this chip and summarized its function.

Configuration Register Mapping

CODE	ABBREVIATION	MEANING	SYSTEM I/O OFFSET
F00	FID	Identification	00h
F04	FCS	Command and status	04h
F08	FREV	Revision	08h
F0c	FLT	Latency timer	0ch
F10	FBIOAC	Base I/O address for Cxx registers	10h
F14	FBIOAD	Base I/O address for Dxx registers	14h
F18	FBMA	Base memory address	18h
----	-----	Reserved	1ch – 24h
F28	FCISPR	CardBus CIS pointer	28h
F2c	FSSID	Subsystem ID	2Ch
F30	FERBA	Expansion ROM base address	30h
F34	FCAPR	Capabilities pointer	34h
----	-----	Reserved	38h
F3c	FIR	Interrupt	3Ch
F40	FSR	Signature	40h
Fdc	FPMR0	Power Management Register 0	DCh
Fe0	FPMR1	Power management Register 1	E0h
Fe4	FVPDR0	Vital Product Data Register 0	E4h
Fe8	FVPDR1	Vital Product Data Register 1	E8h

This table lists the initial state of each register in W89C841F after Stk_ResetB, PCI_ResetB, D3toD0_ResetB and software reset.

CODE	ABBR.	STK_RESETB, PCI_RESETB D3TOD0_RESETB	SOFTWARE RESET
F00	FID	0000_0000h	Non affected
F04	FCS	0280_0000h	Non affected
F08	FREV	0200_0000h	Non affected
F0c	FLT	0000_0000h	Non affected
F10	FBIOAC	FFFF_FFC1h	Non affected
F14	FBIOAD	FFFF_FF01h	Non affected
F18	FBMA	FFFF_FE00h	Non affected
F28	FCISPR	0000_0000h	Non affected
F2c	FSSID	0000_0000h	Non affected
F30	FERBA	0000_0000h	Non affected
F34	FCAPR	0000_0000h	Non affected
F3c	FIR	0000_0100h	Non affected
F40	FSR	0000_0044h	Non affected
Fdc	FPMR0	5A02_0001h	Non affected
Fe0	FPMR1	0000_0100h	Non affected
Fe4	FVPDR0	0000_0003h	Non affected
Fe8	FVPDR1	0000_0000h	Non affected

F00/FID Device ID Register

The register specifies the vendor ID and the device ID.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:16	R	DID	Device ID Loaded from EEPROM after hardware reset.
15:0	R	VID	Vendor ID Loaded from EEPROM after hardware reset. FFFFh is an invalid value for vendor ID.

F04/FCS Command and Status Register

The F04/FCS comprises two parts, one is the command register (FCS[15:0]) which provides the control of PCI activity, and another is the status register (FCS[31:16]) which shows the status information of PCI event. Writing 1 to the bits of the status register will clear them; writing 0 has no effect.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31	R/WC	DPE	Detected Parity Error The DPE bit will be set if a parity error is detected by W89C841F even the parity error response bit of register F04/FCS[6] is disabled.
30	R/WC	SSE	Signaled System Error The SSE bit will be set if W89C841F assert SERRB.
29	R/WC	RMA	Received Master Abort The RMA bit will be set if W89C841F master transaction is terminated by a master abort.
28	R/WC	RTA	Received Target Abort The RTA bit will be set if W89C841F master transaction is terminated by a target abort.
27	R/WC	STA	Signaled Target Abort The STA bit will be set if W89C841F slave transaction takes a target abort.
26:25	R	DT	DEVSELB Timing Fixed at 01b. Indicate a medium DEVSEL# assert timing.
24	R/WC	MDPE	Master Data Parity Error The MDPE bit will be set if the following three conditions are met: 1). W89C841F asserts PERRB (on a read) or observes PERRB asserted (on a write). 2). W89C841F acts as a master in the transaction that the error occurs. 3). The parity error response bit of register F04/FCS[6] is set.

F04/FCS Command and Status Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
23	R	FBTBC	Fast Back-to-Back Capable Fixed at 1. Indicates the capability of accepting fast back to back transactions which are not accessing to the same target.
22:21	R	---	Reserved. Fixed at 0.
20	R	CAPS	Capabilities List The value is dependent on the PMEn and VPDEn loaded from EEPROM to decide the W89C841F power management and Vital Product Data capability. While CAPS is equal to 1: indicates that W89C841F supports the PCI Power Management and/or VPD. 0: indicates that W89C841F does not support Power Management and VPD.
19:9	R	---	Reserved. Fixed at 0.
8	R/W	SE	SERRB Enable Set SE bit high to enable W89C841F to assert SERRB if an address parity error is detected. This bit and bit PER must be set 1 to signal SERR event.
7	R	----	Reserved. Fixed at 0.
6	R/W	PER	Parity Error Response Set PER bit to high to enable the W89C841F to respond to parity error. When PER is reset, W89C841F will ignore any parity error and continue the normal operation. W89C841F internal parity checking and generation function will not be disabled even PER is reset.
5:3	R	---	Reserved. Fixed at 0.
2	R/W	BM	Bus Master Set BM bit to high will allow W89C841F acting as a bus master. Reset BM bit to low will disable the W89C841F bus master ability.
1	R/W	MS	Memory Space Set MS bit to high will allow W89C841F to respond to memory space access by the host.
0	R/W	IOS	I/O Space Set IOS bit to high will allow W89C841F to respond to I/O space access by the host.

F08/FREV Device Revision Register

This register which is read-only shows class code, subclass code, interface code and revision ID.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:24	R	BC	Base Class Code Loaded from EEPROM.
23:16	R	SC	Subclass Code Loaded from EEPROM.
15:8	R	IC	Interface Code Loaded from EEPROM.
7:0	R	REV	Revision ID Loaded from EEPROM.

F0C/FLT Latency Timer Register

This register specifies the latency timer of master bus in units of PCI bus clock.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:24	R	---	Reserved, Fixed to 0.
23:16	R	HT	Header Type, Fixed to 0.
15:8	R/W	LT	Latency Timer Specify, in units of PCI clocks, the latency timer value of W89C841F. When W89C841F asserts FRAMEB, its latency timer starts counting up. W89C841F will initiate the transaction termination as soon as its GNTB de-asserted if the timer expired before W89C841F de-asserts FRAMEB.
7:0	R	---	Reserved. Fixed at 0.

F10/FBIOAC Base I/O Address for Cxx Function Registers

This register is written by software after power-on reset to specify W89C841F base I/O address for Cxx function registers access in the system.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31: 6	R/W	BIOA	Base I/O Address Written by power-on software to specify base I/O address for Cxx function registers. W89C841F requires a 64 bytes I/O space.
5:1	R	---	Reserved. Fixed at 0.
0	R	IO	I/O Space Indicator Fixed at 1.

F14/FBIOAD Base I/O Address for Dxx Function Registers

This register is written by software after power-on reset to specify W89C841F base I/O address for Dxx function registers in the system.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31: 8	R/W	BIOA	Base I/O Address Written by power-on software to specify base I/O address for Dxx function registers. W89C841F requires a 256 bytes I/O space.
7:1	R	---	Reserved. Fixed at 0.
0	R	IO	I/O Space Indicator Fixed at 1.

F18/FBMA Base Memory Address Register

This register is written by power-on software to specify W89C841F base memory address in the system.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31: 9	R/W	BMA	Base Memory Address Written by power-on software to specify base memory address for both of Cxx and Dxx function registers. W89C841F requires a 512 bytes memory space.
8:1	R	---	Reserved. Fixed at 0.
0	R	MEM	Memory Space Indicator Fixed at 0.

F28/FCISPR CardBus CIS Pointer Register

This register identifies the location of the Card Information Structure (CIS). In W89C841F, CIS data can be stored in EEPROM or BootROM. CIS pointer value is loaded from EEPROM.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:28	R	RIN	ROM Image Number This field defines the ROM image number (0-Fh) in which the CIS is located. The offset value is added to the start of the ROM image to identify the start of the CIS.
27:3	R	ASO	Address Space Offset This field defines which space the CIS resides within. Memory space: This is the offset into the memory address space governed by Base Address Register F18/FMBA. Adding this value to the value in the Base Address Register gives the location of the start address of the CIS. Bits ASO is fixed to 80h. Expansion ROM space: The offset value is from the start of the ROM image identified by bits RIN.
2:0	R	ASI	Address Space Indicator Specifies the base address within the space indicated. The offset bits ASO is added to this base address to identify the start of the CIS. The address indicators values are: 3 = CIS is in the memory pointed to by the base address register 2. 7 = CIS is in the Boot ROM. Bits RIN identify which Boot ROM image. Other values are reserved.

F2C/FSSID Subsystem ID Register

This register stores the Subsystem ID and Subsystem Vendor ID.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:16	R	SBID	Subsystem ID Loaded from EEPROM.
15:0	R	SBVID	Subsystem Vendor ID Loaded from EEPROM.

F30/FERBA Expansion ROM Base Address Register

This register is written by power-on software to specify the on-board Boot ROM base address in the system.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:13	R/W	EROMB	Expansion ROM Base Address Written by power-on software to specify expansion ROM base address. W89C841F will request up to 256K bytes memory space for the on board Boot ROM according the configuration of bit BROMSEL of register Dc0/DBRAR[30:28].
12:1	R	---	Reserved. Fixed at 0.
0	R/W	ROME	Expansion ROM Enable Set both of this bit and memory space bit of register F04/FCS[1] to 1 to enable expansion ROM access ability.

F34/FCAPPR Capabilities Pointer Register

W89C841F has the capabilities of Power Management and/or Vital Product Data. This register is read-only and is used as the start pointer of capabilities list.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:8	R	---	Reserved. Fixed at 0.
7:0	R	CAPPR	Capabilities Pointer The value is dependent on the PMEn and VPDEn loaded from EEPROM to decide the W89C841F power management and VPD capability. If PMEn = 1, CAPPR is set to DCh. If PMEn = 0 and VPDEn = 1, CAPPR is set to E4h. If PMEn = 0 and VPDEn = 0, CAPPR is set to 00h.

F3C/FIR Interrupt Register

This register stores the MAX Latency Timer and Min Grant Timer. They are loaded from EEPROM.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:24	R	MAXLAT	Max Latency Timer Loaded from EEPROM. Indicates how often, in units of 0.25 µS, W89C841F needs to gain access to PCI bus. Assuming PCI clock rate is 33 MHz.
23:16	R	MINGNT	Min Grant Timer Loaded from EEPROM. Indicates how long a burst period, in units of 0.25 µS, is needed by W89C841F. Assuming PCI clock rate is 33 MHz.
15:8	R	IPIN	Interrupt Pin Fixed at 01h. Indicates INTAB is used.
7:0	R/W	ILINE	Interrupt Line Written by power-on software to specify routing of interrupt line.

F40/FSR Signature Register

The register is designed for identifying the hardware of W89C841F.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:16	R/W	DVAR	Driver Area This field is for driver special use. The driver can write some specific pattern to these bits for bundling the software and hardware of W89C841F together.
15:8	R	---	Reserved. Fixed at 0.
7:0	R	SIG	Signature After the hardware reset, these 8 bits value is toggled as following SIG = 70h at (2N-1)th read 44h at 2Nth read Where N = 1, 2, ...

Fdc/FPMR0 Power Management Register 0

The register provides the power management capabilities of W89C841F.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31: 27	R	PME_SP	PME_Support bit 31 = 1 --- PMEB can be asserted from D3(cold) state. The value is dependent on the auxiliary power source detection from pin BtOEB/AuxPWR after power-on reset. bit 30 = 1 --- PMEB can be asserted from D3 (hot). Fixed to 1. bit 29 = 0 --- PMEB cannot be asserted from D2. Fixed to 0. bit 28 = 1 --- PMEB can be asserted from D1. Fixed to 1. bit 27 = 1 --- PMEB can be asserted from D0. Fixed to 1.
26	R	D2SUP	D2_Support Fixed to 0. W89C841F does not support D2 Power Management State.
25	R	D1SUP	D1_Support Fixed to 1. W89C841F supports D1 Power Management State.
24:22	R	Aux_ Current	3.3V Auxiliary Current This field reports the 3.3Vaux auxiliary current requirements for PCI function. If PM_Data_En is disable and D3 cold is not supported, Aux_Current are fixed to 000b. IF PM_Data_En is disable and D3 cold is supported, Aux_Current bits apply: **Bit** **3.3VAux** 24 23 22 Max. Current Required 1 1 1 375 mA 1 1 0 320 mA 1 0 1 270 mA 1 0 0 220 mA 0 1 1 160 mA 0 1 0 100 mA 0 0 1 55 mA 0 0 0 0 (self powered) If bit PM_Data_En loaded from EEPROM is enabled, PM_Data field of Fe0/FPMR1 Is implemented to report the power consumption and power dissipation of each device state (D0, D1 and D3). So it takes precedence over 3.3Vaux current requirement reporting. Aux_Current bits will be fixed to 000b. Note: The 3.3Vaux Max. auxiliary current of W89C841F is 220 mA which should be loaded from EEPROM.
	R	---	Fixed to 0.

Fdc/FPMR0 Power Management Register 0, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
18:16	R	VERS	Version Fixed at 010b. The W89C841F complies with Revision 1.1 of the PCI Power Management Interface Specification
15:8	R	NXTPR	Next Item Pointer The value is dependent on the VPDEn loaded from EEPROM to decide the W89C841F VPD capability link list pointer. If VPDEn = 1, NXTPR is equal to E4h. If VPDEn = 0, NXTPR is equal to 00h.
7:0	R	CAP_ID	Capability Identifier Fixed to 01h. This linked list item is the PCI Power Management registers.

Fe0/FPMR1 Power Management Register 1

The register provides the power management control, status and power consumption, dissipation data of supported device power states.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:24	R	PM_Data	PM_Data If bit PM_Data_En loaded from EEPROM is enabled, PM_Data is used to report the state dependent data requested by the D_Select field. The value is scaled by the value reported by the D_Scale field. All of the PM_data will be loaded from EEPROM after power on reset.
23:16	R	---	Reserved. Fixed at 0.
15	Sticky bit, R/WC	PME_STS	PME Status This bit is set when the enabled Wake-up Frame detector receives a Wake-up Frame or the enabled Magic Packet detector receives a Magic Packet or the enabled Link Status Change Detector detected a link status change independent of the state of the PME_EN bit. When PME_STS and PME_EN are set, W89C841F asserts PMEB. Writing a 1 to this bit will clear it and cause W89C841F to stop asserting a PMEB (if PME_En is enable). Writing a 0 has no effect. This bit defaults to 0 if PMEB generation from D3cold is not supported If PMEB generation from D3cold is supported, then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded.

Fe0/FPMR1 Power Management Register 1, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
14:13	R	D_Scale	Data Scale Indicates the scaling factor to be used when interpreting the value of the PM_Data field. The value is loaded from EEPROM. 00b = Unknown 01b = 0.1x 10b = 0.01x 11b = 0.001x
12:9	R/W	D_Select	Data Select Used to select which data is to be reported in units Watts through the PM_Data and D_Scale fields. 0 = D0 power Consumed 1 = D1 power Consumed 3 = D3 power Consumed 4 = D0 power Dissipated 5 = D1 power Dissipated 7 = D3 power Dissipated Others = reserved Note: The power consumption and power dissipation of W89C841F at different power state are: 1. D0: 0.59W 2. D1: 0.59W 3. D3: 0.52W
8	Sticky bit, R/W	PME_EN	PME Enable When set to 1, PMEB assertion is enabled. When reset to 0, PMEB assertion is disabled. When PME_STS and PME_EN are set, W89C841F asserts PMEB. This bit defaults to 0 if PMEB generation from D3cold is not supported. If PMEB generation from D3cold is supported, then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded.
7:2	R	---	Reserved. Fixed at 0.
1:0	R/W	PW_STS	Power State 00b --- Indicates W89C841F at D0 power state 01b --- Indicates W89C841F at D1 power state 11b --- Indicates W89C841F at D3 (hot) power state Writing 10b has no effect.

Fe4/FVPDR0 Vital Product Data Register 0

The register provides control and status capability for the data transfer between register Fe8/FVPDR1 and EEPROM.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31	R/W	VPDFlag	VPD Flag A flag used to indicate when the transfer of data between the VPD Data Register (FVPDR1) and EEPROM is completed. A. Read VPD information 1. Reset VPDFlag to 0, and Write VPD Address to VPDADDR. 2. VPDFlag will be set to 1, after 4 bytes data are read from EEPROM to Register FVPDR1 B. Write VPD information 1. Write the data to Register FVPDR1. 2. Set VPDFlag to 1, and write VPD Address to VPDADDR. 3. VPDFlag will be reset to 0, after 4 bytes data are written from Register FVPDR1 to EEPROM.
30:16	R/W	VPDADDR	VPD Address It is used to access VPD data that is stored in EEPROM. The lower 2 bits of VPDADDR must be zero.
15:8	R	NEXTID	Pointer to Next ID Fixed at 00h. There is no next item pointer in the capabilities list.
7:0	R	VPDID	VPD ID Fixed at 03h. It indicates capability structure ID for VPD

Fe8/FVPDR1 Vital Product Data Register 1

The register provides the buffer for VPD from system or EEPROM.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	VPD_Data	VPD Data VPD data are read or written through this register. The least significant byte of this register corresponds to the byte of VPD at the address specified by the bits VPDADDR of register Fe4/FVPDR0.

9. FUNCTION REGISTERS

W89C841F implements two types of function registers: Cxx and Dxx. Cxx function registers are used to perform the function control and status monitor of W89C841F. Dxx function registers are used to control power management parameters, monitor power management status and setup wake-up frames parameters. The general attributes of W89C841F function registers are described as the following:

1) The function registers of W89C841F can be mapped into the host I/O space or memory space.
2) The registers of the W89C841F are double word aligned. Each register consists of 32 bits and may be accessed using any byte-enable combinations with double word aligned address.
3) Burst access to the registers of W89C841F will be terminated after 1st data transfer completed with a Disconnect without Data.
4) SoftReset will have the same effect as done by HardReset on the registers of W89C841F, except for the function registers C34/CMA0, C38/CMA1, D00/DWUPC – D6c/DBWF4BM3, Dcc/DPA0, Dd0/DPA1 and Df0/DFER – Dfc/DFFER and configuration registers
5) Any read on the reserved register will be returned with 0 value.

Cxx Function Registers

The following table outlined all the control/status registers in W89C841F, offset address, and summarized its function.

CODE	ABBR.	MEANING	BASE OFFSET FROM FBIOAC	BASE OFFSET FROM FBMA
C00	CBCR	Bus Control	00h	000h
C04	CTSDR	Transmit Start Demand	04h	004h
C08	CRSDR	Receive Start Demand	08h	008h
C0c	CRDLA	Receive Descriptor List Address	0Ch	00Ch
C10	CTDLA	Transmit Descriptor List Address	10h	010h
C14	CISR	Interrupt Status	14h	014h
C18	CIMR	Interrupt Mask	18h	018h
C1c	CNCR	Network Configuration	1Ch	01Ch
C20	CFDCR	Frame Discarded Counter	20h	020h
C24	CTDAR	Current Transmit Descriptor Address	24h	024h
C28	CTBAR	Current Transmit Buffer Address	28h	028h
C2c	CRDAR	Current Receive Descriptor Address	2ch	02ch
C30	CRBAR	Current Receive Buffer Address	30h	030h
C34	CMA0	Multicast Address 0	34h	034h
C38	CMA1	Multicast Address 1	38h	038h
C3c	CGTR	General Timer Register	3Ch	03Ch

This table lists the initial state of each register in W89C841F after Stk_ResetB, PCI_ResetB, D3toD0_ResetB and software reset.

CODE	ABBR.	STK_RESETB, PCI_RESETB D3TOD0_RESETB	SOFTWARE RESET
C00	CBCR	0001_0010h	0001_0010h
C04	CTSDR	0000_0000h	0000_0000h
C08	CRSDR	0000_0000h	0000_0000h
C0c	CRDLA	0000_0000h	0000_0000h
C10	CTDLA	0000_0000h	0000_0000h
C14	CISR	0000_0000h	0000_0000h
C18	CIMR	0000_0000h	0000_0000h
C1c	CNCR	0000_0130h	0000_0130h
C20	CFDCR	0000_0000h	0000_0000h
C24	CTDAR	0000_0000h	0000_0000h
C28	CTBAR	0000_0000h	0000_0000h
C2c	CRDAR	0000_0000h	0000_0000h
C30	CRBAR	0000_0000h	0000_0000h
C34	CMA0	0000_0000h	not affected
C38	CMA1	0000_0000h	not affected
C3c	CGTR	0000_0000h	0000_0000h

The detail function and operation for each register in W89C841F will be described in the following paragraph.

C00/CBCR PCI Bus Control Register

This register defines the configuration of PCI bus master.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:22	R	----	Reserved. Fixed to 0.
21	R/W	WAIT	Wait State Insertion When WAIT is set, W89C841F as a bus master executes memory read/write with one wait state every data phase. When WAIT is reset, W89C841F as a bus master executes memory read/write with zero wait state every data phase.
20	R/W	DBE	Descriptor Big Endian Mode When set, the descriptors will be handled in big endian mode. When reset, the descriptors will be treated in little endian mode

C00/CBCR PCI Bus Control Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
19:17	R	---	Reserved. Fixed at 0.
16	R/W	PAE	PCI Abort Enable 1: If bus error happened, TXDMA and RXDMA will halt. Driver must reinitialized W89C841F. (default) 0: If bus error happened, TXDMA and RXDMA will not halt. Wrong data will not be written into register of configuration space, Cxx or Dxx.
15:14	R/W	CA	Cache Alignment CA defines the address boundary for the burst access to the data transmission or reception. When the starting address of the data burst access is not aligned, more specifically, the starting address should be a multiple of some number such as 4, 8 etc. W89C841F will have the first burst transfer that causes that the next burst access will has the start address aligned. After the first burst occurred, all other burst operation are aligned with the configuration of CA accordingly. The CA must be initialized with a non-zero value after reset. The alignment configuration is as following: [00] Reserved (default) [01] 8 double word alignment [10] 16 double word alignment [11] 32 double word alignment
13:8	R/W	BL	Burst Length BL defines the maximum number of the double words that can be transferred within one PCI burst transaction. The burst length configuration is as following. 00h Refer to CA 01h 1 double word 02h 2 double word 04h 4 double word 08h 8 double word 10h 16 double word 20h 32 double word other Reserved

C00/CBCR PCI Bus Control Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
7	R/W	BBE	Buffer With Big Endian When set, the data buffers are treated with big endian ordering. When reset, the data buffers are treated with little endian ordering.
6:2	R/W	SKIP	Skip Length Between Descriptors This field specifies the skip length between two descriptors from the start address of the current descriptor to the start address of the next descriptor. The unit of the skip length is double word. The default value after hardware reset is 04h.
1	R/W	ARB	Arbitration Between Tx and Rx Processes When reset, the TX process and RX process will have the right to use the internal bus with the same priority. When set, the RX process will have higher priority than TX process with regarding to the internal bus utilization.
0	R/W	SWR	Software Reset. Set bit SW_Reset to high will reset most internal registers except registers C34/CMA0, C38/CMA1, D00/DWUPC – D6c /DBWF4BM3, Dcc/CPA0, Dd0/CPA1, Df0/DFER – Dfc /DFFER and PCI Configuration Registers.

C04/CTSDR Transmit Start Demand Register

This register is used to request W89C841F to do a transmission process.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	W	TSD	Transmit Start Demand A write to this register will trigger W89C841F transmit DMA to fetch the descriptor for progressing the transmission operation when W89C841F transmit DMA is staying at the suspend state. Otherwise, the write operation will have no effect.

C08/CRSDR Receive Start Demand Register

The register is used to request W89C841F to do a receive process.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	W	RSD	Receive Start Demand A write to this register will trigger W89C841F receive DMA to fetch the descriptor for progressing the receiving operation when W89C841F receive DMA is staying at the suspend state. Otherwise, the write operation will have no effect.

C0c/CRDLA Receive Descriptors List Addresses

The register defines the start address of the receive descriptor list. It should be updated only when the receive DMA state machine is staying at the stop state.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:2	R/W	SRL	Start address of Receive List
1:0	R/W	MBZ	Must be written as 0 for double word alignment.

C10/CTDLA Transmit Descriptors List Addresses

The register defines the start address of the transmit descriptor list. It should be updated only when the transmission DMA state machine is staying at the stop state.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:2	R/W	STL	Start address of Transmit List
1:0	R/W	MBZ	Must be written as 0 for double word alignment.

C14/CISR Interrupt Status Register

Most bits of this register report the interrupt status. The assertion of the interrupt status, reported by bits 0 to bit 14 and the corresponding interrupt mask bits will cause a hardware interrupt to the host. A write with 1 value the status bit will clear them and write 0 will have no effect.

C14/CISR Interrupt Status Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:26	R	---	Reserved. Fixed at 0.
25:23	R	BET	Bus Error Type The field indicates the error type of bus error and is valid only when bit 13, bus error, is set. Assertion of these bits does not generate interrupt. The definition of bus error is as follows. 000 = Parity Error (Master Mode) 001 = Master Abort (Master Mode) 010 = Target Abort (Master Mode) 011 = Signaled System Error (Slave Mode) 100 = Data Parity Error (Slave Mode) 101 – 111 = Reserved The initial state of this field after reset is 0.
22:20	R	TPS	Transmit Process State This field indicates the transmit state. This field does not generate interrupt.
19:17	R	RPS	Receive Process State This field indicates the receive state. This field does not generate interrupt.
16	R	NIR	Normal Interrupt Report The normal interrupt report includes transmit completed interrupt, transmit buffer unavailable interrupt, the receive completed interrupt and the receive pause packet interrupt. The NIR is a logical OR result of the bits 0, 2, 6, 14 of register C14/CISR. Only the bits corresponding to the unmasked bits of C18/CIMR will affect this bit.
15	R	AIR	Abnormal Interrupt Report The abnormal interrupt includes transmit process in idle state interrupt, receive early interrupt, receive error interrupt, transmit FIFO under-flow interrupt, receive buffer unavailable interrupt, receive in idle state interrupt, EEPROM Programming Fail Interrupt, transmit early interrupt, timer expire interrupt, PHY Interrupt and the bus error interrupt. The AIR is a logical OR result of the bits 1, 3, 4, 5, 7, 8, 9, 10, 11, 12, 13 of register C14/CISR. Only these bits corresponding to the unmasked bits of the C18/CIMR will affect this bit.

C14/CISR Interrupt Status Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
14	R/WC	RPP	Receive Pause Packet Interrupt A high indicates a pause packet is received.
13	R/WC	BE	Bus Error Interrupt A high indicates a bus error happened. The error type will be shown by bit 25 – 23.
12	R	PI	PHY Interrupt A high indicates a PHY interrupt happened. PHY interrupt event is stored in Global Interrupt Status Register [address 14h] of MII Management. After reading Global Interrupt Status Register, that register and this bit will be cleared.
11	R/WC	TE	Timer Expired Interrupt A high indicates the general timer of register C3c/CGTR expired.
10	R/WC	TEI	Transmit Early Interrupt W89C841F will has Transmit Early Interrupt status set after the packet to be transmitted is completely transferred into the transmit FIFO if Transmit Early Interrupt On bit of C1c/CNCR[30] is set. The TEI will be cleared automatically after the packet is transmitted out from the transmit FIFO completely.
9	R/WC	EPF	EEPROM Programming Fail Interrupt A high indicates a programming error happened when W89C841F tries to write data into EEPROM that is in write protected state.
8	R/WC	RIDLE	Receive in Idle State Set means the receive DMA state machine is in the idle state.
7	R/WC	RBU	Receive Buffer Unavailable When there is no receive buffer available, this bit is set and the receive process enters the suspend state.
6	R/WC	RINT	Receive Complete Interrupt A high indicates that a frame has been received and the receive status is transferred into the receive descriptors of the current frame.
5	R/WC	TUF	Transmit FIFO Under-flow A high indicates that the transmit FIFO had an under-flow error during the packet transmission.

C14/CISR Interrupt Status Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
4	R/WC	RERR	Receive Error A high indicates that the receive DMA detects a receive error during the packet reception.
3	R/WC	REI	Receive Early Interrupt The REI will be set when the number of the data of the incoming frame, in double word unit, transferred to the data buffer reaches Receive Early Interrupt Threshold specified by the register C1c/CNCR[28:21] if Receive Early Interrupt On in the register C1c/CNCR[31] is set.
2	R/WC	TBU	Transmit Buffer Unavailable A high indicates that there is no available transmit descriptor during or after the packet transmission.
1	R/WC	TIDLE	Transmit Process in Idle State A high indicates the transmit state machine is in the idle state.
0	R/WC	TINT	Transmit Complete Interrupt The TINI will be set when a frame transmission is completed and the FINT (bit 31) of Transmit Descriptor 1 (T01) is set.

C18/CIMR Interrupt Mask Register

The register controls the interrupt enable corresponding to the bits in the register C14/CISR

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:17	R	----	Reserved. Fixed to 0.
16	R/W	NIE	Normal Interrupt Enable The Normal Interrupt will be enabled if the NIE is set to high. The Normal Interrupt is disabled when the NIE is reset to low. The hardware interrupt will be asserted if both the NIE bit of the C18/CIMR[16] and the NIR bit of the C14/CISR[16] are set to high.
15	R/W	AIE	Abnormal Interrupt Enable The Abnormal Interrupt will be enabled if the AIE is set to high. The Abnormal Interrupt is disabled when the AIE is reset to low. The hardware interrupt will be asserted if both the AIE bit of the C18/CIMR[15] and the AIR bit of the C14/CISR[15] are set to high.

C18/CIMR Interrupt Mask Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
14	R/W	RPPE	Receive Pause Packet Interrupt Enable The receive pause packet Interrupt will be enabled if both AIE and BPPE are set to high, otherwise, the receive pause packet Interrupt will be disabled.
13	R/W	BEE	Bus Error Enable The Bus Error Interrupt will be enabled if both AIE and BEE are set to high, otherwise, the Bus Error Interrupt will be disabled.
12	R/W	PIE	PHY Interrupt Enable. The PHY Interrupt will be enabled if both AIE and PIE are set to high, otherwise, the PHY Interrupt will be disabled.
11	R/W	TEE	Timer Expired Enable The Timer Expired Interrupt will be enabled if both AIE and TEE are set to high, otherwise, the Timer Expired Interrupt will be disabled.
10	R/W	TEIE	Transmit Early Interrupt Enable The Transmit Early Interrupt will be enabled if both AIE and TEIE are set to high, otherwise, the Transmit Early Interrupt will be disabled.
9	R/W	EPFE	EEPROM Programming Fail Enable: The EEPROM Programming Fail will be enabled if both AIE and EPFE are set to high, otherwise, the EEPROM Programming Fail will be disabled.
8	R/W	RIE	Receive Idle Enable. The Receive Idle Interrupt will be enabled if both AIE and RIE are set to high, otherwise, the Receive Idle Interrupt will be disabled.
7	R/W	RBUE	Receive Buffer Unavailable Enable. The Receive Buffer Unavailable Interrupt will be enabled if both AIE and RBUE are set to high, otherwise, the Receive Buffer Unavailable Interrupt will be disabled.
6	R/W	RINTE	Receive Complete Interrupt Enable The Receive Interrupt will be enabled if both NIE and RINTE are set to high, otherwise, the Receive Interrupt will be disabled.
5	R/W	TFUE	Transmit FIFO Underflow Enable The Transmit FIFO Underflow Interrupt will be enabled if both AIE and TFUE are set to high, otherwise, the Transmit FIFO Underflow Interrupt will be disabled.

C18/CIMR Interrupt Mask Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
4	R/W	RERRE	Receive Error Enable The Receive Error Interrupt will be enabled if both AIE and RERRE are set to high, otherwise, the Receive Error Interrupt will be disabled.
3	R/W	REIE	Receive Early Interrupt Enable The Receive Early Interrupt will be enabled if both AIE and REIE are set to high, otherwise, the Receive Early Interrupt will be disabled.
2	R/W	TBUE	Transmit Buffer Unavailable Enable The Transmit Buffer Unavailable Interrupt will be enabled if both NIE and TBUE are set to high, otherwise, the Transmit Buffer Unavailable Interrupt will be disabled.
1	R/W	TIE	Transmit Idle Enable The Transmit Idle Interrupt will be enabled if both AIE and TIE are set to high, otherwise, the Transmit Idle Interrupt will be disabled.
0	R/W	TINTE	Transmit Complete Interrupt Enable The Transmit Interrupt will be enabled if both NIE and TINTE are set to high, otherwise, the Transmit Interrupt will be disabled.

C1c/CNCR Network Configuration Register

The register defines the configuration for the data transmission or reception and the interrupt algorithm for interrupt assertion.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31	R/W	REIO	Receive Early Interrupt On The receive early interrupt function will be enabled when the REIO is set to high. Otherwise, receive early interrupt function will be disabled.
30	R/W	TEIO	Transmit Early Interrupt On The transmit early interrupt function will be enabled when the TEIO is set to high. Otherwise, transmit early interrupt function will be disabled.
29	R	ES	Ethernet Speed 1: 100 Mbps 0: 10 Mbps.

C1c/CNCR Network Configuration Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
28:21	R/W	REIT	Receive Early Interrupt Threshold During receiving packet, the W89C841F will assert an interrupt request when the bytes number of the received data, which the receive DMA has moved them into the data buffer, excesses receive early interrupt threshold. To set this field 00H will disable receive early interrupt function. The setting of receive early interrupt threshold is as following. 01h 4 bytes 02h 8 bytes -- -- 0fh 60 bytes 10h 64 bytes -- -- FFh 1020 bytes
20:14	R/W	TTH	Transmit Threshold These bits select the transmit threshold level of the transmit FIFO. The packet Transmission will be started immediately once the data queued into the transmit FIFO has reached the threshold level. The transmission will also be started immediately when the full packet has been transferred into the transmit FIFO even though the frame length is less than the TTH level. To change this bit, the transmit state machine must be in Idle state. The following table shows there is a difference with 16 bytes for each consecutive setting value in this field, except that the first one in the table. 00h full packet 01h 16 bytes 02h 32 bytes -- -- 0Fh 240 bytes 10h 256 bytes -- -- 7Fh 2032 bytes
13	R/W	TXON	**Transmit On** When set, the transmission process will be started. When reset, the transmission state machine will be stopped after the current frame is completed

C1c/CNCR Network Configuration Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
12	R/W	VLANEN	**VLAN Enable** 1: W89C841F can transmit and receive packet with VLAN tagged whose maximum length is equal to 1522 bytes. 0: Only untagged frame are transmitted and received. Packet length up to 1518 bytes is allowed. (default)
11:10	R/W	LBK	**Loopback Mode** The LBK selects the W89C841F loop-back modes: 00 Normal mode (default) 01 Internal Loop-back 10 External Loop-back Reserved
9	R	FD	Full Duplex Mode 1: Full duplex mode. 0: Half duplex mode.
8	R/W	ADP	Accept Directed Packet When set, all incoming packets with a directed address will be accepted.
7	R/W	AEP	Accept Error Packet When set, all incoming CRC error packets passed address filtering will be accepted.
6	R/W	ARP	Accept Runt Packet When set, the incoming packets pass the address filtering with the length less than 64 bytes are accepted.
5	R/W	ABP	Accept Broadcast Packet. When set, all incoming packets with a Broadcast address will be accepted.
4	R/W	AMP	Accept Multicast Packet When set, all incoming packets with a multicast address match the node multicast address table (MAR7 – MAR0) will be accepted.
3	R/W	APP	Accept All Physical Packet When set, all incoming packets with unicast address will be accepted.

C1c/CNCR Network Configuration Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
2	R/W	RXON	Receive On. When set, the receive process will be started. When reset, the receive state machine will be stopped after the current frame is completed.
1	R/W	TFCEN	TX Flow Control Enable 1: W89C841F can transmit Pause packet. 0: W89C841F can not transmit Pause packet. (default)
0	R/W	RFCEN	RX Flow Control Enable 1: W89C841F can parse Pause packet. 0: W89C841F can not parse Pause packet. (default)

C20/CFDCR Frame Discarded Counter Register

The register records the missed packet count and the FIFO overflow count.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31	RC	MRFO	More Receive FIFO Overflow This bit is the overflow bit of the receive FIFO Overflow counter. The actual number of the FIFO overflow must be more than the number shown by the bits RFOC if the MRFO is set to high. This bit will be clear after read.
30:16	RC	RFOC	Receive FIFO Overflow Counter The RFOC indicates the number of the packets that are discarded due to the receive FIFO overflow under the condition of the receive buffer is not available. This counter will be clear after read.
15	RC	MMP	More Missed Packets Overflow bit of Missed Packet Counter. The actual number of the missed packet must be more than the number shown by the bits field MPC if MMP is set tot high. This bit will be clear after read.
14:0	RC	MPC	Missed Packet Counter The MPC indicates the number of packets that are discarded due to the receive FIFO overflow. This counter will be clear after read.

C24/CTDAR Current Transmit Descriptor Address Register

The register shows the start address of the descriptor which W89C841F transmit DMA state machine is used to process the current frame.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R	CTDA	Current Transmit Descriptor Address The CTDA represents the start address of the current receive descriptor which W89C841F transmit DMA state machine is used to process the transmit frame.

C28/CTBAR Current Transmit Buffer Address Register

The register shows the address of the system memory from which W89C841F transmit DMA state machine will fetch the double word data and queue the data into the FIFO for transmission.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R	CTBA	Current Receive Buffer Address The CTBA contains the start address of the host memory from which W89C841F transmit DMA state machine will fetch the double word data and queue it into the FIFO for transmission.

C2c/CRDAR Current Receive Descriptor Address Register

The register shows the start address of the receive descriptor which is used by W89C841F receive DMA state machine to process the current receive frame.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R	CRDA	Current Receive Descriptor Address The CRDA represents the start address of the current receive descriptor which W89C841F receive DMA state machine is used to process the received frame.

C30/CRBAR Current Receive Buffer Address Register

The register shows the start address of the host memory which is used by W89C841F receive DMA state machine to store the current aligned double word data of the current received frame.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R	CRBA	Current Receive Buffer Address The CRBA contains the pointer current address in the on-using buffer of the host memory which will be used by W89C841F receive DMA state machine to store the current aligned double word data of the current received frame.

C34/CMA0 Multicast Address Register 0

The register defines the lower 32 bits of the total 64 bits multicast address hashing table.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:24	R/W	MAR3	Muticast Address 3 The MAR3 defines the bit 31 – 24 of the hashing table.
23:16	R/W	MAR2	Muticast Address 2 The MAR2 defines the bit 23 – 16 of the hashing table.
15:8	R/W	MAR1	Muticast Address 1 The MAR1 defines the bit 15 – 8 of the hashing table.
7:0	R/W	MAR0	Muticast Address 0 The MAR0 defines the bit 7 – 0 of the hashing table.

C38/CMA1 Multicast Address Register 1

The register defines the upper 32 bits of the 64 bits multicast address hashing table.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:24	R/W	MAR7	Muticast Address 7 The MAR7 defines the bit 63 – 56 of the hashing table.
23:16	R/W	MAR6	Muticast Address 6 The MAR2 defines the bit 55 – 48 of the hashing table.
15:8	R/W	MAR5	Muticast Address 5 The MAR1 defines the bit 47 – 40 of the hashing table.
7:0	R/W	MAR4	Muticast Address 4 The MAR4 defines the bit 39 – 32 of the hashing table.

C3c/CGTR General Timer Register

The register shows the real time content of W89C841F internal general timer.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31	R/W	ATLP	Accept Too Long Packet When set, a packet whose length is longer than 1518 (1522) bytes is received. When reset, a packet whose length is longer than 1518 (1522) bytes is not received. Default to 0.
30:17	R	---	Reserved. Fixed at 0.

C3c/CGTR General Timer Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
16	R/W	RECUR	Recursive Mode 1: The value of bits Timer in the register C3c/CGTR[15:0] can be reloaded for internal general timer to count down when the internal general reaches zero. 0: No recursive to the internal general timer. (default)
15:0	R/W	TIMER	General Timer The bits TIMER shows the content of the general timer inside the W89C841F. The internal general timer will count down from the pre-set value, a non zero value, programmed by the driver automatically. The time unit for the internal general timer count_down is approximately 2048 times the cycle duration of the MII TXCLK. For instance, the count down time unit for a 25 MHz MII TXCLK is approximately 82 μS.

Dxx Function Registers

The following table outlined all the Dxx function registers for power management control and status, EEPROM, Boot ROM, PHY's Registers access and CardBus status/event in W89C841F.

CODE	ABBR.	MEANING	BASE OFFSET FROM FBIOAD	BASE OFFSET FROM FBMA
D00	DWUPC	Wake-up Control and Status	00h	100h
D04 – D08	Reserved			
D0c	DWF0CRC	Wake-up Frame B0B1 CRC	0Ch	10Ch
D10	DWF1CRC	Wake-up Frame B2B3 CRC	10h	110h
D14	DWF2CRC	Wake-up Frame B4 CRC	14h	114h
D18 – D1C	Reserved			
D20	DBWF0BM0	Basic Wake-up Frame 0 Byte-Mask 0	20h	120h
D24	DBWF0BM1	Basic Wake-up Frame 0 Byte-Mask 1	24h	124h
D28	DBWF0BM2	Basic Wake-up Frame 0 Byte-Mask 2	28h	128h
D2c	DBWF0BM3	Basic Wake-up Frame 0 Byte-Mask 3	2Ch	12Ch
D30	DBWF1BM0	Basic Wake-up Frame 1 Byte-Mask 0	30h	130h
D34	DBWF1BM1	Basic Wake-up Frame 1 Byte-Mask 1	34h	134h
D38	DBWF1BM2	Basic Wake-up Frame 1 Byte-Mask 2	38h	138h
D3C	DBWF1BM3	Basic Wake-up Frame 1 Byte-Mask 3	3Ch	13Ch

Dxx Function Registers, continued

CODE	ABBR.	MEANING	BASE OFFSET FROM FBIOAD	BASE OFFSET FROM FBMA
D40	DBWF2BM0	Basic Wake-up Frame 2 Byte-Mask 0	40h	140h
D44	DBWF2BM1	Basic Wake-up Frame 2 Byte-Mask 1	44h	144h
D48	DBWF2BM2	Basic Wake-up Frame 2 Byte-Mask 2	48h	148h
D4c	DBWF2BM3	Basic Wake-up Frame 2 Byte-Mask 3	4Ch	14Ch
D50	DBWF3BM0	Basic Wake-up Frame 3 Byte-Mask 0	50h	150h
D54	DBWF3BM1	Basic Wake-up Frame 3 Byte-Mask 1	54h	154h
D58	DBWF3BM2	Basic Wake-up Frame 3 Byte-Mask 2	58h	158h
D5c	DBWF3BM3	Basic Wake-up Frame 3 Byte-Mask 3	5Ch	15Ch
D60	DBWF4BM0	Basic Wake-up Frame 4 Byte-Mask 0	60h	160h
D64	DBWF4BM1	Basic Wake-up Frame 4 Byte-Mask 1	64h	164h
D68	DBWF4BM2	Basic Wake-up Frame 4 Byte-Mask 2	68h	168h
D6c	DBWF4BM3	Basic Wake-up Frame 4 Byte-Mask 3	6Ch	16Ch
D70 – Dbc	---	Reserved		
Dc0	DBRAR	Boot ROM Access	C0h	1C0h
Dc4	DEEAR	EEPROM Access	C4h	1C4h
Dc8	DMMAR	MII Management Access	C8h	1C8h
Dcc	DPA0	Physical Address 0	CCh	1CCh
Dd0	DPA1	Physical Address 1	D0h	1D0h
Dd4	---	Reserved		
Dd8	---	Reserved		
Ddc	DRFCTV	RXDMA Flow Control Threshold Value	DCh	1DCh
Df0	DFER	Function Event Register	F0h	1F0h
Df4	DFEMR	Function Event Mask Register	F4h	1F4h
Df8	DFPSR	Function Present Status Register	F8h	1F8h
Dfc	DFFER	Function Force Event Register	FCh	1FCh

This table lists the initial state of each register in W89C841F after Stk_ResetB, PCI_ResetB, D3toD0_ResetB and software reset.

CODE	ABBR.	STK_RESETB, PCI_RESETB, D3TOD0_RESETB	SOFTWARE RESET
D00	DWUPC	0000_0458h	Non affected
D04 – D08	Reserved		
D0C	DWF0CRC	FFFE_FFFEh	Non affected
D10	DWF1CRC	FFFE_FFFEh	Non affected
D14	DWF2CRC	FFFE_0000h	Non affected
D18 – D1c	Reserved		
D20	DBWF0BM0	0000_0000h	Non affected
D24	DBWF0BM1	0000_0000h	Non affected
D28	DBWF0BM2	0000_0000h	Non affected
D2C	DBWF0BM3	0000_0000h	Non affected
D30	DBWF1BM0	0000_0000h	Non affected
D34	DBWF1BM1	0000_0000h	Non affected
D38	DBWF1BM2	0000_0000h	Non affected
D3C	DBWF1BM3	0000_0000h	Non affected
D40	DBWF2BM0	0000_0000h	Non affected
D44	DBWF2BM1	0000_0000h	Non affected
D48	DBWF2BM2	0000_0000h	Non affected
D4c	DBWF2BM3	0000_0000h	Non affected
D50	DBWF3BM0	0000_0000h	Non affected
D54	DBWF3BM1	0000_0000h	Non affected
D58	DBWF3BM2	0000_0000h	Non affected
D5c	DBWF3BM3	0000_0000h	Non affected
D60	DBWF4BM0	0000_0000h	Non affected
D64	DBWF4BM1	0000_0000h	Non affected
D68	DBWF4BM2	0000_0000h	Non affected
D6c	DBWF4BM3	0000_0000h	Non affected
D70 – Dbc	Reserved		
Dc0	DBRAR	0000_0000h	0000_0000h
Dc4	DEEAR	0000_0000h	0000_0000h
Dc8	DMMAR	4020_0000h	4020_0000h
Dcc	DPA0	0000_0000h	Non affected

Continued

CODE	ABBR.	STK_RESETB, PCI_RESETB, D3TOD0_RESETB	SOFTWARE RESET
Dd0	DPA1	0000_0000h	Non affected
Dd4	Reserved		
Dd8	Reserved		
Ddc	DRFCTV	0003_0100h	0003_0100h
Df0	DFER	0000_0000h	Non affected
Df4	DFEMR	0000_0000h	Non affected
Df8	DFPSR	0000_0000h	Non affected
Dfc	DFFER	0000_0000h	Non affected

D00/DWUPCS Wake-up Control and Status Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31	R/WC	RMGP	Received Magic Packet When set, indicates that a Magic Packet has been received if Magic Packet detector is enabled.
30	R/WC	DLSCD_ L2F	Detected Link Status Change From Link to Fail When set, indicates that a Link Status Change From Link to Fail if Link Status Changes From Link to Fail Detector Enable (LSCDE_L2F = 1).
29	R/WC	DLSCD_ F2L	Detected Link Status Change From Fail to Link When set, indicates that a Link Status Change From Fail to Link if Link Status Changes From Fail to Link Detector Enable (LSCDE_F2L = 1).
28:21	R	---	Reserved. Fixed to 0.
20	R/WC	RWUPF4	Received Wake-up Frame 4 When set, indicates that a Wake-up Frame 4 has been received if Wake-up Frame detector is enabled (WUPFE= 1).
19	R/WC	RWUPF3	Received Wake-up Frame 3 When set, indicates that a Wake-up Frame 3 has been received if Wake-up Frame detector is enabled (WUPFE= 1).
18	R/WC	RWUPF2	Received Wake-up Frame 2 When set, indicates that a Wake-up Frame 2 has been received if Wake-up Frame detector is enabled (WUPFE= 1).

D00/DWUPCS Wake-up Control and Status Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
17	R/WC	RWUPF1	Received Wake-up Frame 1 When set, indicates that a Wake-up Frame 0 has been received if Wake-up Frame detector is enabled (WUPFE = 1).
16	R/WC	RWUPF0	Received Wake-up Frame 0 When set, indicates that a Wake-up Frame 0 has been received if Wake-up Frame detector is enabled (WUPFE = 1).
15:14	R	---	Reserved. Fixed at 0.
13	R/W	PWRDN	PHY Power Down Enable If Bus Type is CardBus which is loaded from EEPROM, bit PWRDN is default to high (active) to force PHY into power down mode after power on reset. If Bus Type is not CardBus, bit PWRDN is default to low to disable power down mode after power on reset. 1: PHY power down enable 0: PHY power down disable
12	R	EETYPE	EEPROM Type After power on reset, EEPROM type will be latched in from pin BtWEB/EESel. 1: 93C56 0: 93C46
11	R/W	CLKRUN_En	CLOCKRUN Enable This bit is loaded from EEPROM to control pin CLKRUNB in MiniPCI or CardBus system. 1: Enable ClockRun function. 0: Disable ClockRun function.
10	R/W	MGPE	Magic Packet Detector Enable Loaded from EEPROM. Setting to 1 and PMEN bit is true enable the operation of Magic Packet Detector.
9	R/W	LSCDE_L2F	Link Status Change From Link to Fail Detector Enable Setting to 1 and PMEN bit is true enable the operation of Link Status Change From Link to Fail Detector.

D00/DWUPCS Wake-up Control and Status Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
8	R/W	LSCDE_F2L	Link Status Change From Fail to Link Detector Enable Setting to 1 and PMEN bit is true enable the operation of Link Status Change From Fail to Link Detector.
7	R/W	WUPFE	Wake-up Frame Detector Enable Setting to 1 and PMEN bit is true enable the operation of Wake-up Frame Detector.
6	R/W	PMEN	Power Management Enable Loaded from EEPROM. 1: PM enable, => Function PMEB and WOL function are enabled. 0: PM disable (default) => Function PMEB and WOL are all disable. Bits MGPE, LSCDE_L2F, LSCDE_F2L and WUPFE are all fixed to 0.
5	R/W	VPDEN	Vital Product Data Enable Loaded from EEPROM. 1: VPD data is stored in EEPROM. 0: VPD data is not stored in EEPROM. (default)
4:3	R/W	WOLTP	Wake ON LAN Signal Type It indicates the signal type of pin WOL/CSTSCHG. 00: Negative Pulse (125ms) 01: Positive Pulse (125ms) 10: Active Low 11: Active High (Default)
2	R	AUXPWR	Aux Power Status This bit is loaded from pin BtOEB/AuxPWR to indicate auxiliary power status. 1: Aux Power is ON. 0: Aux Power is OFF.
1:0	R	BUSTP	PC Bus Type These 2 bits are loaded from EEPROM to configure W89C841F PC Bus type. 00: PCI 01: MiniPCI 10: CardBus 11: reserved.

D0c/DWBF0CRC Wake-up Frame B0B1 CRC Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:16	R/W	WFB0CRC	CRC-16 value for Basic Wake-up Frame 0 match Setting to all 1's except bit[16], after power-on reset.
15:0	R/W	WFB1CRC	CRC-16 value for Basic Wake-up Frame 1 match Setting to all 1's except bit[0], after power-on reset.

D10/DWF1CRC Wake-up Frame B2B3 CRC Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:16	R/W	WFB2CRC	CRC-16 value for Basic Wake-up Frame 2 match Setting to all 1's except bit[16], after power-on reset.
15:0	R/W	WFB3CRC	CRC-16 value for Basic Wake-up Frame 3 match Setting to all 1's except bit[0], after power-on reset.

D14/DWF2CRC Wake-up Frame B4 CRC Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:16	R/W	WFB4CRC	CRC-16 value for Basic Wake-up Frame 4 match Setting to all 1's except bit[16], after power-on reset.
15:0	R	WFB3CRC	Reserved. Fixed to 0.

D20/DBWF0BM0 Basic Wake-up Frame 0 Byte-Mask 0 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF0BM0	Basic Wake-up Frame 0 Byte-Mask 0 The bit 0 is the byte 1 mask of Basic Wake-up Frame 0. --- The bit 31 is the byte 32 mask of Basic Wake-up Frame 0. Setting to 0, after power-on reset.

D24/DBWF0BM1 Basic Wake-up Frame 0 Byte-Mask 1 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF0BM1	Basic Wake-up Frame 0 Byte-Mask 1 The bit 0 is the byte 33 mask of Basic Wake-up Frame 0. --- The bit 31 is the byte 64 mask of Basic Wake-up Frame 0. Setting to 0, after power-on reset.

D28/DBWF0BM2 Basic Wake-up Frame 0 Byte-Mask 2 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF0BM2	Basic Wake-up Frame 0 Byte-Mask 2 The bit 0 is the byte 65 mask of Basic Wake-up Frame 0. --- The bit 31 is the byte 96 mask of Basic Wake-up Frame 0. Setting to 0, after power-on reset.

D2c/DBWF0BM3 Basic Wake-up Frame 0 Byte-Mask 3 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF0BM3	Basic Wake-up Frame 0 Byte-Mask 3 The bit 0 is the byte 97 mask of Basic Wake-up Frame 0. --- The bit 31 is the byte 128 mask of Basic Wake-up Frame 0. Setting to 0, after power-on reset.

D30/DBWF1BM0 Basic Wake-up Frame 1 Byte-Mask 0 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF1BM0	Basic Wake-up Frame 1 Byte-Mask 0 The bit 0 is the byte 1 mask of Basic Wake-up Frame 1. --- The bit 31 is the byte 32 mask of asic Wake-up Frame 1. Setting to 0, after power-on reset.

D34/DBWF1BM1 Basic Wake-up Frame 1 Byte-Mask 1 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF1BM1	Basic Wake-up Frame 1 Byte-Mask 1 The bit 0 is the byte 33 mask of Basic Wake-up Frame 1. --- The bit 31 is the byte 64 mask of Basic Wake-up Frame 1. Setting to 0, after power-on reset.

D38/DBWF1BM2 Basic Wake-up Frame 1 Byte-Mask 2 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF1BM2	Basic Wake-up Frame 1 Byte-Mask 2 The bit 0 is the byte 65 mask of Basic Wake-up Frame 1. --- The bit 31 is the byte 96 mask of Basic Wake-up Frame 1. Setting to 0, after power-on reset.

D3c/DBWF1BM3 Basic Wake-up Frame 1 Byte-Mask 3 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF1BM3	Basic Wake-up Frame 1 Byte-Mask 3 The bit 0 is the byte 97 mask of Basic Wake-up Frame 1. --- The bit 31 is the byte 128 mask of Basic Wake-up Frame 1. Setting to 0, after power-on reset.

D40/DBWF2BM0 Basic Wake-up Frame 2 Byte-Mask 0 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF2BM0	Basic Wake-up Frame 2 Byte-Mask 0 The bit 0 is the byte 1 mask of Basic Wake-up Frame 2. --- The bit 31 is the byte 32 mask of Basic Wake-up Frame 2. Setting to 0, after power-on reset.

D44/DBWF2BM1 Basic Wake-up Frame 2 Byte-Mask 1 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF2BM1	Basic Wake-up Frame 2 Byte-Mask 1 The bit 0 is the byte 33 mask of Basic Wake-up Frame 2. --- The bit 31 is the byte 64 mask of Basic Wake-up Frame 2. Setting to 0, after power-on reset.

D48/DBWF2BM2 Basic Wake-up Frame 2 Byte-Mask 2 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF2BM2	Basic Wake-up Frame 2 Byte-Mask 2 The bit 0 is the byte 65 mask of Basic Wake-up Frame 2. --- The bit 31 is the byte 96 mask of Basic Wake-up Frame 2. Setting to 0, after power-on reset.

D4c/DBWF2BM3 Basic Wake-up Frame 2 Byte-Mask 3 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF2BM3	Basic Wake-up Frame 2 Byte-Mask 3 The bit 0 is the byte 97 mask of Basic Wake-up Frame 2. --- The bit 31 is the byte 128 mask of Basic Wake-up Frame 2. Setting to 0, after power-on reset.

D50/DBWF3BM0 Basic Wake-up Frame 3 Byte-Mask 0 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF3BM0	Basic Wake-up Frame 3 Byte-Mask 0 The bit 0 is the byte 1 mask of Basic Wake-up Frame 3. --- The bit 31 is the byte 32 mask of Basic Wake-up Frame 3. Setting to 0, after power-on reset.

D54/DBWF3BM1 Basic Wake-up Frame 3 Byte-Mask 1 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF3BM1	Basic Wake-up Frame 3 Byte-Mask 1 The bit 0 is the byte 33 mask of Basic Wake-up Frame 3. --- The bit 31 is the byte 64 mask of Basic Wake-up Frame 3. Setting to 0, after power-on reset.

D58/DBWF3BM2 Basic Wake-up Frame 3 Byte-Mask 2 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF3BM2	Basic Wake-up Frame 3 Byte-Mask 2 The bit 0 is the byte 65 mask of Basic Wake-up Frame 3. --- The bit 31 is the byte 96 mask of Basic Wake-up Frame 3. Setting to 0, after power-on reset.

D5c/DBWF3BM3 Basic Wake-up Frame 3 Byte-Mask 3 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF3BM3	Basic Wake-up Frame 3 Byte-Mask 3 The bit 0 is the byte 97 mask of Basic Wake-up Frame 3. --- The bit 31 is the byte 128 mask of Basic Wake-up Frame 3. Setting to 0, after power-on reset.

D60/DBWF4BM0 Basic Wake-up Frame 4 Byte-Mask 0 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF4BM0	Basic Wake-up Frame 4 Byte-Mask 0 The bit 0 is the byte 1 mask of Basic Wake-up Frame 4. --- The bit 31 is the byte 32 mask of Basic Wake-up Frame 4. Setting to 0, after power-on reset.

D64/DBWF4BM1 Basic Wake-up Frame 4 Byte-Mask 1 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF4BM1	Basic Wake-up Frame 4 Byte-Mask 1 The bit 0 is the byte 33 mask of Basic Wake-up Frame 4. --- The bit 31 is the byte 64 mask of Basic Wake-up Frame 4. Setting to 0, after power-on reset.

D68/DBWF4BM2 Basic Wake-up Frame 4 Byte-Mask 2 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF4BM2	Basic Wake-up Frame 4 Byte-Mask 2 The bit 0 is the byte 65 mask of Basic Wake-up Frame 4. --- The bit 31 is the byte 96 mask of Basic Wake-up Frame 4. Setting to 0, after power-on reset.

D6c/DBWF4BM3 Basic Wake-up Frame 4 Byte-Mask 3 Register

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:0	R/W	WF4BM3	Basic Wake-up Frame 4 Byte-Mask 3 The bit 0 is the byte 97 mask of Basic Wake-up Frame 4. --- The bit 31 is the byte 128 mask of Basic Wake-up Frame 4. Setting to 0, after power-on reset.

Dc0/DBRAR Boot ROM Access Register

The register is used to specify the control function and the data message passing for the on board Boot ROM.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31	R	-	Reserved. Fixed to 0.
30:28	R/W	BROMSEL	Boot ROM Size Select BROMSEL bits decides the size of the on board boot ROM device. 00x = No Boot ROM 010 = 8K 011 = 16K 100 = 32K 101 = 64K 110 = 128K 111 = 256K Loaded from EEPROM after Power-on reset.
27	R/W	BROMRD	BootROM Read Control When EESEL bit of register Dc4/DEEAR[31] is reset, setting this bit will perform the on-board boot ROM read operation with the reading address specified by bits BROMA. The bit BROMRD will be cleared automatically after BootROM read operation is completed. Bit BROMRD will not allow to be set high, even writing a logic 1 to BROMRD if the bit EESEL is set.
26	R/W	BROMWR	BootROM Write Control When EESEL bit of register Dc4/DEEAR[31] is reset, setting this bit will perform the on-board boot ROM write operation with the writing address specified by BROMA. This bit BROMWR will be cleared automatically after BootROM write operation is completed. The BROMWR will not allow to be set high, even writing a logic 1 to BROMWR if the bit EESEL is set.
25:8	R/W	BROMA	Boot ROM Offset Address This field contains boot ROM offset address.
7:0	R/W	BROMD	Boot ROM Data BROMD are used to store the read/write data for the on board Boot ROM access when EESEL is reset to low. BROMD is of no meaning if the EESEL is set to high.

Dc4/DEEAR EEPROM Access Register

The register is used to read or write information between system and EEPROM.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31	R/W	EESEL	EEPROM/BootROM Select 1: EEPROM access through Dc4/DEEAR is allowed. (default) 0: BootROM access through Dc0/DBRAR is allowed.
30	R/W	StartEERW	Start EEPROM Read/Write Access Set to 1, to start EEPROM RD/WR access. It will be cleared to 0 automatically, after access is complete.
29:28	R/W	EERW	EEPROM Read/Write Command 00: Read 01: Write 10: Write Protection Disable 11: Write Protection Enable
27:23	R	-------	Reserved. Fixed to 0
22:16	R/W	EEOA	EEPROM Offset Address This field contains EEPROM offset address.
15:0	R/W	EEData	EEPROM Data EEPROM Data is used to store the read/write data for the on board EEPROM access when EESEL is set to high. EEData is of no meaning if the EESEL is set to low.

Dc8/DMMAR MII Management Access Register

The register is used to read or write information between system and MII management registers in transceiver.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31	R/W	StartMDIORW	Start MDIO Read/Write When set to 1, MDIO starts to read/ write PHY data. It will be clear automatically, when access completes.
30:29	R/W	MDIORW	MDIO RD/WR command 01: Write 10: Read (default) 00, 11: reserved

Dc8/DMMAR MII Management Access Register, continued

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
28:26	R	-----	Reserved. Fixed to 0
25:21	R/W	PHYADD	PHY Address The PHY address must be the same as internal transceiver's PHY address setting. Deafult to 01h.
20:16	R/W	REGADD	PHY's Register Address Refer to MII Management Registers to access the dedicated register.
15:0	R/W	REGData	PHY Register Data PHY Register Data is used to store the read/write data for MII management registers in embedded transceiver.

Dcc/DPA0 Physical Address Register 0

The register defines the first 32 bits of the 48 bits MAC address. The DPA0 value is loaded from EEPROM after hardware reset

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:24	R/W	PAR3	Physical Address 3 The PAR3 defines the bit 24 – 31 of the MAC address.
23:16	R/W	PAR2	Physical Address 2 The PAR2 defines the bit 16 – 23 of the MAC address.
15:8	R/W	PAR1	Physical Address 1 The PAR1 defines the bit 8 – 15 of the MAC address.
7:0	R/W	PAR0	Physical Address 0 The PAR0 defines the bit 0 – 7 of the MAC address.

Dd0/DPA1 Physical Address Register 1

The register defines the last 16 bits of the 48 bits MAC address. The DPA1 value is loaded from EEPROM after hardware reset

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:16	R	---	Reserved. Fixed at 0.
15:8	R/W	PAR5	Physical Address 5 The PAR5 defines the 40 – 47 bit of the 48 bit of the MAC address.
7:0	R/W	PAR4	Physical Address 4 The PAR0 defines the 32 – 39 bit of the 48 bit of the MAC address.

Ddc/DRFCTV RXDMA Flow Control Threshold Value

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:18	R	---	Reserved. Fixed to 0.
17:9	R/W	HTV	High Threshold Value When the receive byte count in the RX FIFO is greater than high threshold value, a pause packet with MAX pause time will be transmitted if bit TFCEN of register C1c/CNCR is set. Default value: 9'h180
8:0	R/W	LTV	Low Threshold Value When the receive byte count in the RX FIFO is less than low threshold value, a pause packet with MIN pause time will be transmitted if bit TFCEN of register C1c/CNCR is set. Default value: 9'h100

Df0/DFER Function Event Register

This register is used for reporting of interrupt pending and power-management event detection in a CardBus system. A field in this register is set when the corresponding field in the Function Present State register changes its value. Writing "1" into a field clear the field. Writing "0" has no effect

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:16	R	---	Reserved. Fixed to 0.
15	R/WC	INTR	Interrupt Event It is set when the interrupt is pending or FRS_INTR bit in the register Dfc/DFFER[15] is set, regardless the mask value.
14:5	R	----	Reserved. Fixed to 0.
4	Sticky bit, R/WC	GWAKE	General Wake-up Event It is set when the PRE_GWAKE bit in register Df8/DFPSR[4] changes its state from 0 to 1 or FRS_GWAKE bit in the Dfc/DFFER[4] is set, regardless the mask value. This bit is cleared by write 1 and writing 0 has no effect. This bit is default to 0 if PMEB generation from $D3_{cold}$ is not supported. If PMEB generation from $D3_{cold}$ is supported, then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded. Note: When W89C841F is configured into CardBus system, writing 1 to the field will clear this bit and the PME_Status bit in the register Fe0/FPMR1[15] too. Or writing 1 to the PME_Status bit in the register Fe0/FPMR1[15] will clear PME_Status bit and this GWAKE bit.
3:0	R	---	Reserved. Fixed to 0.

Df4/DFEMR Function Event Mask Register

This register gives software the ability to control what events in the function cause the Status Changed interrupts or the host system Wakeup. This register controls the assertion of the signals INTAB and CSTSCHG in a CardBus system.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:16	R	---	Reserved. Fixed to 0.
15	R/W	INTR_ EN	Interrupt Enable Setting 1 enables the INTR in the function Event register to generate interrupt on the INTAB pin.
14	Sticky bit, R/W	WKUP_ EN	Wake-up Enable Setting 1, enables the GWAKE bit in the register Df0/DFER to generate the Wakeup event on the CSTSCHG line if the GWAKE_En field is set together. When this bit reset to 0, the Wakeup function is disable. This bit defaults to 0 if PMEB generation from $D3_{cold}$ is not supported. If PMEB generation from $D3_{cold}$ is supported, then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded.
13:5	R	---	Reserved. Fixed to 0.
4	Sticky bit, R/W	GWAKE_ EN	General Wake-up Enable Setting 1, enables the GWAKE bit in the register Df0/DFER to generate the Wakeup event on the CSTSCHG line if the WKUP field is also set . When reset to 0, the Wakeup function is disable. This bit defaults to 0 if PMEB generation from $D3_{cold}$ is not supported. If PMEB generation from $D3_{cold}$ is supported, then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded. Note: When W89C841F is configured into CardBus system, setting or clearing PME_En bit in register Fe0/FPMR1[8] will also setting or clearing GWAKE_EN & WKUP_EN bits at the same time. Bits GWAKE_EN & WKUP_EN are allowed to be reset after setting PME_En bit.
3:0	R	---	Reserved. Fixed to 0.

Df8/DFPSR Function Present State Register

This is read-only register reflects the current state of each condition that can cause a status change event.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:16	R	----	Reserved. Fixed to 0.
15	R	PRE_INT	Present Interrupt Status It reflects the current state of interrupt requests regardless of the mask value. It is set when the Ethernet function has a pending interrupt and cleared when the software driver acknowledges all active interrupts from register C14/CISR.
14:5	R	----	Reserved. Fixed to 0.
4	R	PRE_ GWAKE	Present General Wake-up Status: It reflects the current state of the wake-up event. This bit is cleared when either the General Wake-up Event in the function event register is cleared, or when the PME_Status bit in the register Fe0/FPMR1[15] is cleared.
3:0	R	----	Reserved. Fixed to 0.

Dfc/DFFER Function Force Event Register

This register is used to generate interrupt or wake-up event.

BIT	ATTRIBUTE	BIT NAME	DESCRIPTION
31:16	R	---	Reserved. Fixed to 0.
15	W	FRS_INTR	Force Interrupt Event: Writing 1 to this field sets the INTR bit in the register Df0/DFER. PRE_INTR bit in the register Df8/DFPSR[15] is not affected and continues to reflect the current state of the functional interrupt. Writing 0 has no effect.
14:5	R	---	Reserved. Fixed to 0.
4	W	FRS_ GWAKE	Force General Wake-up Event: Writing 1 to this field sets the GWAKE bit in the register Df0/DFER. PRE_GWAKE bit in the register Df8/DFPSR[4] is not affected and continues to reflect the current state of the Wakeup request. Writing 0 has no effect.
3:0	R	---	Reserved. Fixed to 0.

MII Management Registers

W89C841F supports MDC/MDIO interface to access MII management registers located in embedded PHYceiver. The following table list all of the MII Management registers supported by W89C841F.

ADDRESS	REGISTER NAME	DEFAULT
00h	Control Register	3100h
01h	Status Register	7849h
02h	PHY Identifier Register 1	0022h
03h	PHY Identifier Register 2	E011h
04h	Auto Negotiation Advertisement Register	05E1h
05h	Auto Negotiation Link Partner Ability Register	01E1h
06h	Auto Negotiation Expansion Register	0004h
07h	Next Page Transmit Register	2001h
08h	Link Partner Next Page Register	0000h
09h – 0Fh	IEEE Reserved	FFFFh
10h	PHY Specific Control Register	0680h
11h	Port Configuration Register	0026h
12h	PHY Specific Status Register	000Fh
13h	Global Interrupt Enable Register	0000h
14h	Global Interrupt Status Register	0000h
15h	Receive Error Counter	0000h

Control (Register 0h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
0.15	RST	RESET 1 – PHY Reset 0 – Normal operation	R/W SC	0h
0.14	LPBK	Loop Back Enable 1 – Enable loopback mode 0 – Disable Loopback mode	R/W	0h
0.13	SPEED_LSB	Speed Selection LSB 0.13 0 0 10 Mbits/s 0 1 100 Mbits/s 1 0 1000 Mbits/s 1 1 Reserved	R/W	1h
0.12	ANEN	Auto Negotiation Enable 1 – Enable auto negotiation process 0 – Disable Auto negotiation process	R/W	1h
0.11	PDN	Power Down Enable 1 – Power Down 0 – Normal Operation	R/W	0h
0.10	ISO	Isolate AD2105 from Network 1 – Isolate PHY from MII/RMII 0 – Normal Operation	R/W	0h
0.9	ANEN_RST	Restart Auto Negotiation 1 – Restart Auto Negotiation Process 0 – Normal Operation	R/W SC	0h
0.8	DPLX	Duplex Mode 1 – Full Duplex mode 0 – Half Duplex mode	R/W	1h
0.7	COLTST	Collision Test 1 – Enable COL signal test 0 – Disable COL signal test	R/W	0h
0.6	SPEED_MSB	Speed Selection MSB	RO	0h
0.5:0	Reserved	Not Used	RO	00h

Status (Register 1h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
1.15	CAP_T4	100Base-T4 Capable	RO	0h
1.14	CAP_TXF	100Base-X Full Duplex Capable	RO	1h
1.13	CAP_TXH	100Base-X Half Duplex Capable	RO	1h
1.12	CAP_TF	10M Full Duplex Capable	RO	1h
1.11	CAP_TH	10M Half Duplex Capable	RO	1h
1.10	CAP_T2	100Base-T2 Capable	RO	0h
1.9:7	Reserved	Ignored when read	RO	0h
1.6	CAP_SUPR	MF Preamble Suppression Capable	RO	1h
1.5	AN_COMP	Auto Negotiation Complete 1 – Auto Negotiation process completed 0 – Auto Negotiation process not completed	RO	0h
1.4	REM_FLT	Remote Fault Detect 1 – Remote Fault detected 0 – Remote Fault not detected	RO	0h
1.3	CAP_ANEG	Auto Negotiation Ability 1 – Capable of auto negotiation 0 – Not capable of auto negotiation	RO	1h
1.2	LINK	Link Status 1 – Link is up 0 – Link is down	RO, LL	0h
1.1	JAB	Jabber Detect 1 – Jabber condition detected 0 – Jabber condition not detected	RO, LH	0h
1.0	EXTREG	Extended Capability 1 – Extended register set 0 – No extended register set	RO	1h

PHY Identifier Register (Register 2h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
2.15:0	PHY-ID[15:0]	IEEE Address	RO	0022

PHY Identifier Register (Register 3h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
315:0	PHY-ID[15:0]	IEEE Address/Model No./Rev. No.	RO	E011

Advertisement (Register 4h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
4.15	NP	Next Page	RO	0h
4.14	Reserved	Reserved	RO	0h
4.13	RF	Remote Fault 1 – Remote Fault has been detected 0 – No remote fault has been detected	R/W	0h
4.12	IEEE Reserved	Reserved	RO	0h
4.11	ASM_DIR	Asymmetric Pause Direction. Bit[11:10] Capability 00 No Pause 01 Symmetric PAUSE Asymmetric PAUSE toward Link Partner Both Symmetric PAUSE and Asymmetric PAUSE toward local device	R/W	0h
4.10	PAUSE	Pause Operation for Full Duplex	R/W	1h
4.9	T4	Technology Ability for 100Base-T4	RO	0h
4.8	TX_FDX	100Base-TX Full Duplex 1 – Capable of 100M Full duplex operation 0 – Not capable of 100M Full duplex operation	R/W	1h
4.7	TX_HDX	100Base-TX Half Duplex 1 – Capable of 100M operation 0 – Not capable of 100M operation	R/W	1h
4.6	10_FDX	10BASE-T Full Duplex 1 – Capable of 10M Full Duplex operation 0 – Not capable of 10M full duplex operation	R/W	1h
4.5	10_HDX	10Base-T Half Duplex 1 – Capable of 10M operation 0 – Not capable of 10M operation	R/W	1h
4.4:0	Selector Field	These 5 bits are hardwired to 00001b.	RO	01h

Auto Negotiation Link Partner Ability (Register 5h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
5.15	NPAGE	Next Page 1 – Capable of next page function 0 – Not capable of next page function	RO	0h
5.14	ACK	Acknowledge 1 – Link Partner acknowledges reception of the ability data word 0 – Not acknowledged	RO	0h
5.13	RF	Remote Fault 1 – Remote Fault has been detected 0 – No remote fault has been detected	RO	0h
5.12:11	IEEE Reserved	Reserved	RO	0h

Auto Negotiation Link Partner Ability (Register 5h), continued

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
5.11	LP_DIR	Link Partner Asymmetric Pause Direction.	RO	0h
5.10	LP_PAU	Link Partner Pause Capability	RO	0h
5.9	LP_T4	Link Partner Technology Ability for 100Base-T4	RO	0h
5.8	LP_FDX	100Base-TX Full Duplex 1 – Capable of 100M Full duplex operation 0 – Not capable of 100M Full duplex operation	RO	1h
5.7	LP_HDX	100Base-TX Half Duplex 1 – Capable of 100M operation 0 – Not capable of 100M operation	RO	1h
5.6	LP_F10	10BASE-T Full Duplex 1 – Capable of 10M Full Duplex operation 0 – Not capable of 10M full duplex operation	RO	1h
5.5	LP_H10	10Base-T Half Duplex 1 – Capable of 10M operation 0 – Not capable of 10M operation	RO	1h
5.4:0	Selector Field	Encoding Definitions.	RO	1h

Auto Negotiation Expansion Register (Register 6h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
6.15:5	Reserved	Reserved	RO	000h
6.4	PFAULT	Parallel Detection Fault 1 – Fault has been detected 0 – No Fault Detect	RO, LH	0h
6.3	LPNPABLE	Link Partner Next Page Able 1 – Link Partner is next page capable 0 – Link Partner is not next page capable	RO	0h
6.2	NPABLE	Next Page Able Defaults to 1, indicating AD2105 is next page able.	RO	1h
6.1	PGRCV	Page Received 1 – A new page has been received 0 – No new page has been received	RO, LH	0h
6.0	LPANABLE	Link Partner Auto Negotiation Able 1 – Link Partner is auto negotiable 0 – Link Partner is not auto negotiable	RO	0h

Next Page Transmit Register (Register 7h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
7.15	TNPAGE	Transmit Next Page Transmit Code Word Bit 15	R/W	0h
7.14	Reserved	Reserved Transmit Code Word Bit 14	RO	0h
7.13	TMSG	Transmit Message Page Transmit Code Word Bit 13	R/W	1h
7.12	TACK2	Transmit Acknowledge 2 Transmit Code Word Bit 12	R/W	0h
7.11	TTOG	Transmit Toggle Transmit Code Word Bit 11	RO	0h
7.10:0	TFLD[10:0]	Transmit Message Field Transmit Code Word Bit 10...0	R/W	001h

Link Partner Next Page Register (Register 8h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
8.15	PNPAGE	Link Partner Next Page Receive Code Word Bit 15	RO	0h
8.14	PACK	Link Partner Acknowledge Receive Code Word Bit 14	RO	0h
8.13	PMSGP	Link Partner Message Page Receive Code Word Bit 13	RO	0h
8.12	PACK2	Link Partner Acknowledge 2 Receive Code Word Bit 12	RO	0h
8.11	PTOG	Link Partner Toggle Receive Code Word Bit 11	RO	0h
8.10:0	PFLD[10:0]	Link Partner Message Field Receive Code Word Bit 11	RO	000h

Channel and 10M Configuration Register (Register 10h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
16. 15:12	RESERVED	Reserved	RO	0h
16.11	IFSEL	Interface Select. 0: MII 1: RMII	RO	0h
16.10	ENREG8	Enable Register 8 to Store Next Page Information. 1 – Store Next Page in Register 8 0 – Store Next Page in Register 5	R/W	1h
16.9	XOVEN	Cross Over Auto Detect Enable. 0: Disable 1: Enable	R/W	1h
16.8	DISPMG	Disable Power Management Feature. 0: Enable 1: Disable	R/W	0h
16.7	ENRJAB	Enable Receive Jabber Monitor. 0: Disable 1: Enable	R/W	1h
16.6:5	VTHR[1:0]	Medium Detect Voltage Control (Peak to Peak) 00: 50 mV 01: 100 mV 10: 150 mV 11: 200 mV	R/W	0h
16.4	DRV62MA	Reduce 10M Driver to 62mA 1 = 62 mA 0 = Normal	R/W	0h
16.3	APDIS	Auto Polarity Disable 1 = Auto Polarity Function Disabled 0 = Normal	R/W	0h
16.2	DISTJAB	Disable Transmit Jabber 1 – Disable Transmit Jabber Function 0 – Enable Transmit Jabber Function	R/W	0h
16.1	ETH	Enable Extended Distance 1 – Lower 10BASE-T Receive threshold 0 – Normal 10BASE-T Receive threshold	R/W	0h
16.0	FGDLNK	Force 10M Receive Good Link 1 – Force Good Link 0 – Normal Operation	R/W	0h

PHY 100M Module Control Register (Register 11h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
17. 15:8	Reserved	Reserved	RO	0h
17.7	SELFX	Fiber Select 1: Fiber Mode 0: TP Mode	R/W	0h
17.6:5	FXTSEL[1:0]	Fiber Control Signal	R/W	1h
17.4	DISSCR	Disable Scrambler 1 – Disable Scrambler 0 – Enable Scrambler	R/W	0h
17.3	ENFEFI	Enable FEFI 1 – Enable FEFI 0 – Disable FEFI	R/W	pin
17.2:1	BSLIMT[1:0]	Base Line Threshold Adjust	R/W	1h
17.0	ADFS	AD Full Scale Adjust	R/W	0h

PHY Specific Status Register (Register 12h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
18. 15:13	RESERVED	Reserved	RO	0h
18.12	FXEN	Fiber Enable. Only Changed when PHY Reset 0: TX 1: FX mode OR'ed result of PI_SELFX and 17.9 (SELFX)	RO	pin
18.11	XOVER	Cross Over. 0: MDI mode 1: MDIX mode	RO	0h
18.10	JAB	Real Time Jabber Status 1 – Jabber 0 – No Jabber	RO	0h
18.9	POLAR	Polarity. 0: Normal Polarity 1: Polarity Reversed	RO	0h

PHY Specific Status Register (Register 12h), continued

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
18.8	PAUOUT	Pause Out capability. Disabled when Half Duplex. 0: Lack of Pause Out capability 1: Has Pause Out capability	RO	0h
18.7	PAUIN	Pause In capability. Disabled when Half Duplex. 0: Lack of Pause In capability 1: Has Pause In capability	RO	0h
18.6	DUPLEX	Operating Duplex 1 – Full Duplex 0 – Half Duplex	RO	0h
18.5	SPEED	Operating Speed 1 – 100Mb/s 0 – 10Mb/s	RO	0h
18.4	LINK	Real Time Link Status 1 – Link Up 0 – Link Down	RO	0h
18.3	RECPAU	Pause Recommend Value. Only Changed when PHY Reset. This bit is disabled automatically when RECDUP is 0. 0: Pause Disable 1: Pause Enable	RO	1h
18.2	RECDUP	Duplex Recommended Value. Only Changed when PHY Reset 1: Full Duplex 0: Half Duplex	RO	1h
18.1	RECSPD	Speed Recommend Value. Only Changed when PHY Reset 1: 100M 0: 10M	RO	1h
18.0	RECANEN	Recommended Auto Negotiation Value. Only Changed when PHY Reset	RO	1h

Interrupt Enable Register (Register 13h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
19.15	XOVCHG	Cross Over mode Changed Interrupt Enable 1 – Interrupt Enable 0 – Interrupt Disable	R/W	0h
19.14	SPDCHG	Speed Changed Interrupt Enable 1 – Interrupt Enable 0 – Interrupt Disable	R/W	0h
19.13	DUPCHG	Duplex Changed Interrupt Enable 1 – Interrupt Enable 0 – Interrupt Disable	R/W	0h
19.12	PGRCHG	Page Received Interrupt Enable 1 – Interrupt Enable 0 – Interrupt Disable	R/W	0h
19.11	LNKCHG	Link Status Changed Interrupt Enable 1 – Interrupt Enable 0 – Interrupt Disable	R/W	0h
19.10	SYMERR	Symbol Error Interrupt Enable 1 – Interrupt Enable 0 – Interrupt Disable	R/W	0h
19.9	FCAR	False Carrier Interrupt Enable 1 – Interrupt Enable 0 – Interrupt Disable	R/W	0h
19.8	FOURUN	Fifo Over/UnderRun Interrupt Enable 1 – Interrupt Enable 0 – Interrupt Disable	R/W	0h
19.7	JABINT	Jabber Interrupt Enable 1 – Interrupt Enable 0 – Interrupt Disable	R/W	0h
19.6:0	Reserved	Reserved	RO	00h

Interrupt Status Register (Register 14h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
20.15	XOVCHG	Cross Over mode Changed 1 – Cross Over mode Changed 0 – Cross Over mode Not Changed	COR	0h
20.14	SPDCHG	Speed Changed 1 – Speed Changed 0 – Speed Not Changed	COR	0h
20.13	DUPCHG	Duplex Changed 1 – Duplex Changed 0 – Duplex not changed	COR	0h
20.12	PGRCHG	Page Received 1 – Page Received 0 – Page not received	COR	0h
20.11	LNKCHG	Link Status Changed 1 – Link Status Changed 0 – Link Status not Changed	COR	0h
20.10	SYMERR	Symbol Error 1 – Symbol Error 0 – No symbol Error	COR	0h
20.9	FCAR	False Carrier 1 – False Carrier 0 – No false carrier Will be high whenever Link is Failed.	COR	0h
20.8	FOURUN	Fifo Over/UnderRun 1 – FIFO Over/Uner Run 0 – No FIFO Over/Under Run	COR	0h
20.7	JABINT	Jabber 1 – Jabber 0 – No Jabber	COR	0h
20.6:0	Reserved	Reserved	COR	00h

Receive Error Counter Register (Register 15h)

BIT(S)	NAME	DESCRIPTION	R/W	DEFAULT
21.15:0	ERB[15:0]	Error Counter. Includes False Carrier Jabber Symbol Error FIFO Under/Over Run Link Code Word Error Error Start of Stream Error End of Stream	RO	0000h

10. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_S	-55	125	°C
Supply Voltage	V_{CC_core} V_{CC_IO}	2.25 3.0	2.75 3.6	V
Input Voltage	V_{IN}	V_{SS}	5 + 0.5	V
Output Voltage	V_{OUT}	V_{SS}	3.6	V

Power Supply

(T_A = 0° C to 70° C)

PARAMETER	SYMBOL	CONDITION	MAX.	UNIT
Power Supply Current (D0 state)	IDD0	V_{CC_core} = 2.5V V_{CC_IO} = 3.3V	210	mA
Power Supply Current (D1)	IDD1	V_{CC_core} = 2.5V V_{CC_IO} = 3.3V	178	mA
Power Supply Current (D3 hot)	IDD1	V_{CC_core} = 2.5V V_{CC_IO} = 3.3V	178	mA
Power Supply Current (D3 cold)	IDD1	V_{CC_core} = 2.5V V_{CC_IO} = 3.3V	158	mA

DC Characteristics

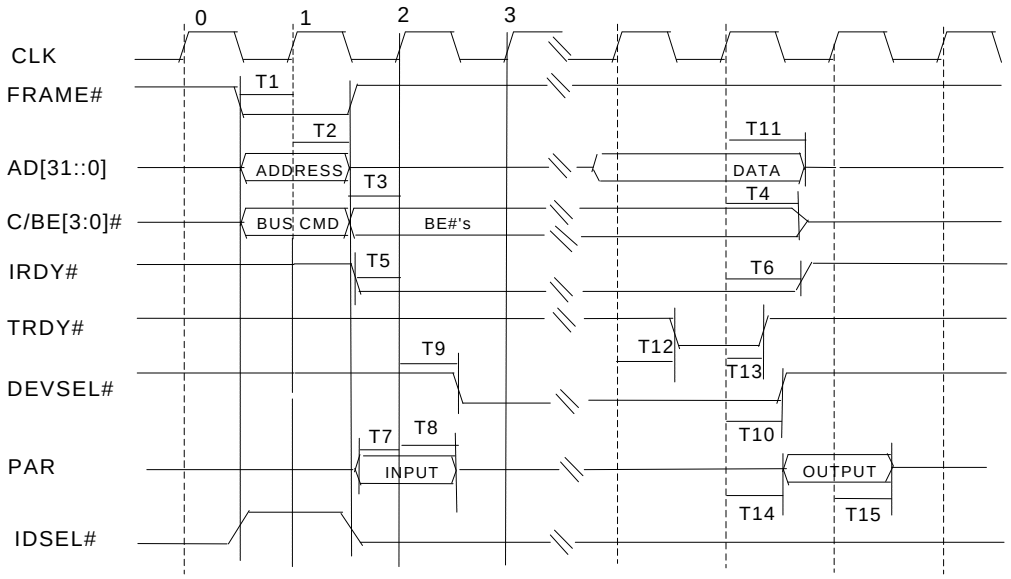
(V_{CC_core} = 2.25V to 2.75V, V_{CC} = 3.0V to 3.6V, V_{SS} = 0V, T_A = 0° C to 70° C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Input Low Voltage	V_{IL}			0.7	V
Input High Voltage	V_{IH}		1.7		V
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA	0	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA	1.85	3.6	V
Input Low Current	I_{IL}	V_{IN} = V_{CC}	-10	10	µA
Input High Current	I_{IH}	V_{IN} = 0V	-10	10	µA

AC Characteristics

(V_{CC_core} = 2.5V, V_{CC_IO} = 3.3V, V_{SS} = 0 V, T_A = 0° C to 70° C)

PCI Slave Read Transaction

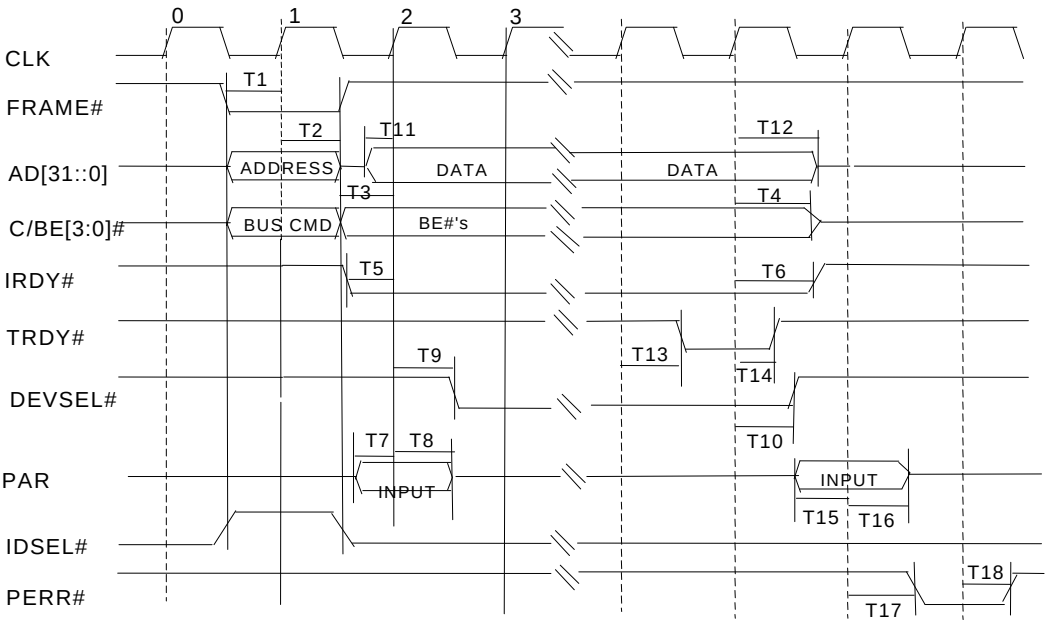


PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNIT
PCI Input Signal Set-up Time*	T1	7			nS
PCI Input Signal Hold Time*	T2	2			nS
BE Byte Enable Set-up Time	T3	7			nS
BE Byte Enable Hold Time	T4	2			nS
IRDY# Set-up Time	T5	7			nS
IRDY# Hold Time	T6	2			nS
PAR Input Set-up Time	T7	7			nS
PAR Input Hold Time	T8	2			nS
DEVSEL# Driven Time	T9	9	10	11	nS
DEVSEL# Hold Time	T10	9	10	11	nS
Output Data Hold Time	T11	9	10	11	nS
TRDY# Driven Time	T12	9	10	11	nS
TRDY# Hold Time	T13	9	10	11	nS
PAR Output Driven Time	T14	9	10	11	nS
PAR Output Hold Time	T15	9	10	11	nS

Note: address, command, and FRAME# for slave access, IDSEL# for configuration read transaction

AC Characteristics, continued

PCI Slave Write Transaction

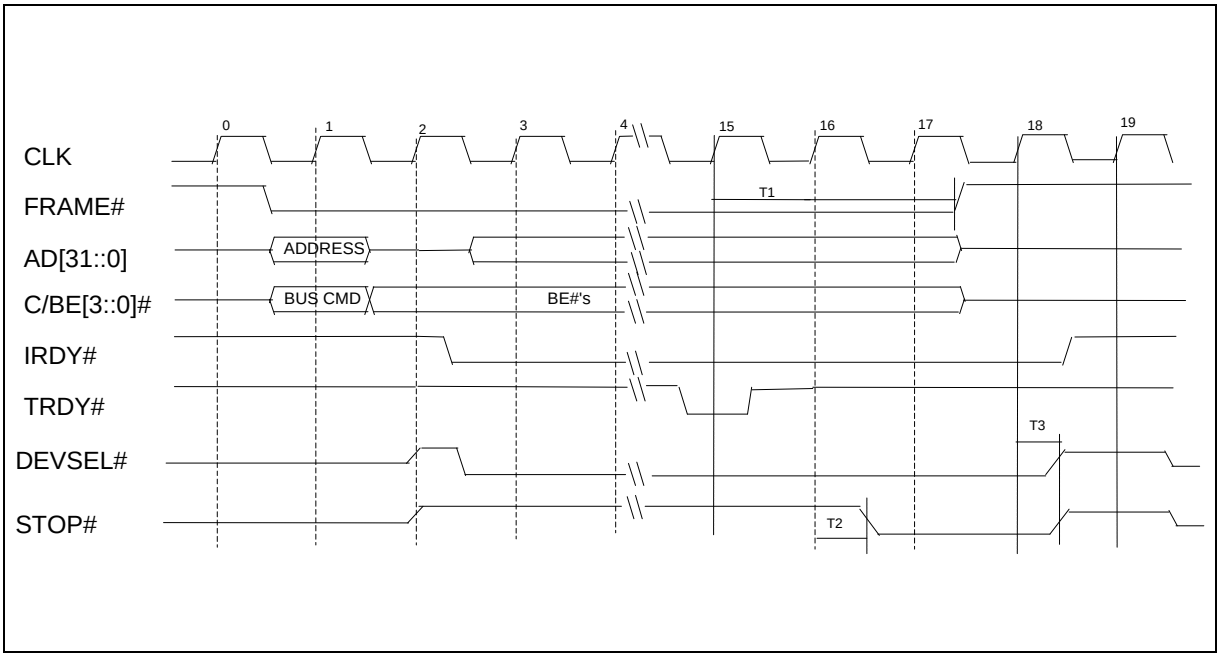


PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNIT
PCI Input Signal Set-up Time*	T1	7			nS
PCI Input Signal Hold Time*	T2	2			nS
BE Byte Enable Set-up Time	T3	7			nS
BE Byte Enable Hold Time	T4	2			nS
IRDY# Set-up Time	T5	7			nS
IRDY# Hold Time	T6	2			nS
PAR Input Set-up Time	T7	7			nS
PAR Input Hold Time	T8	2			nS
DEVSEL# Driven Time	T9	9	10	11	nS
DEVSEL# Hold Time	T10	9	10	11	nS
Input Data Set-up Time	T11	7			nS
Input Data Hold Time	T12	2			nS
TRDY# Driven Time	T13	9	10	11	nS
TRDY# Hold Time	T14	9	10	11	nS
PAR Input Set-up Time	T15	7			nS
PAR Input Hold Time	T16	2			nS
PERR# Driven Time**	T17	9	10	11	nS
PERR# Hold Time**	T18	9	10	11	nS

Note: Address, command, and FRAME# for slave access, IDSEL# for configuration read transaction **PERR# will be asserted if the parity error event occurred.

AC Characteristics, continued

PCI Transaction, Termination Disconnect-C/Retry Type



PARAMETERS	SYMBOL	MIN.	TYPICAL	MAX.	UNIT
FRAME# Deasserted from Clock 15	T1	2			nS
Clock 16 to STOP# Asserted Time	T2	9	10	11	nS
Clock 18 to STOP# and DEVSEL# Hold Time	T3	9	10	11	nS

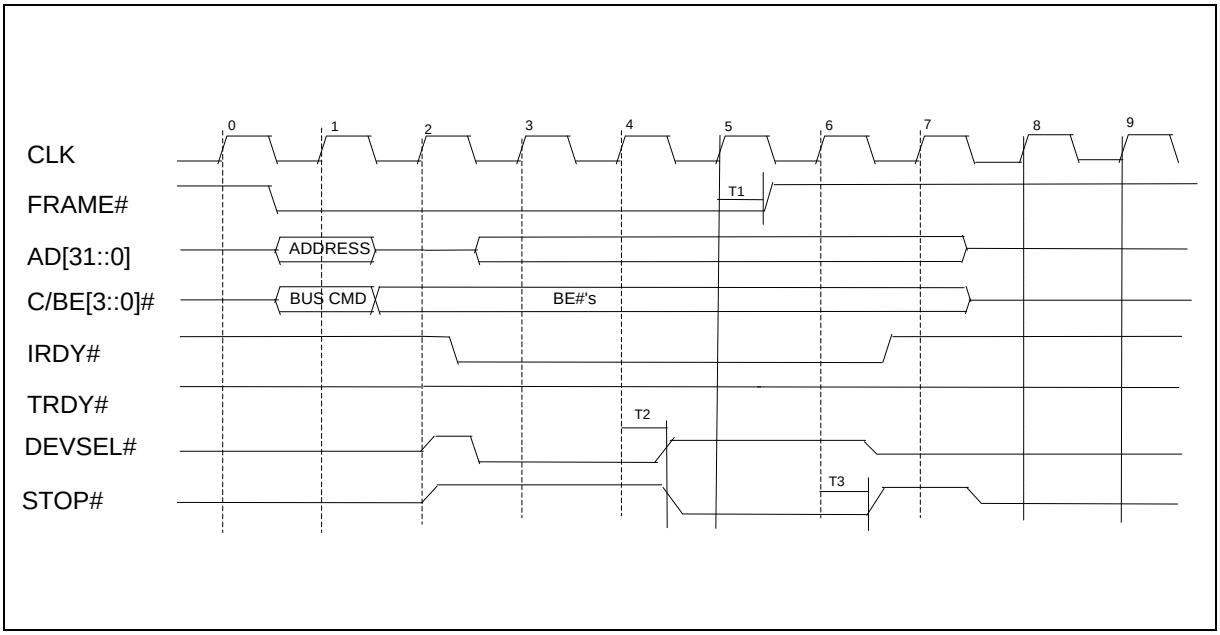
Notes:

1) The other timing requirements for PCI input signal are as the read transaction timing.

2) T1, T2 and T3 are used for the disconnect type C (host try to transfer more than one data phase).

AC Characteristics, continued

Target-Abort Type



PARAMETERS	SYMBOL	MIN.	TYPICAL	MAX.	UNIT
FRAME# Deasserted from Clock 15	T1	2			nS
Clock 4 to DEVSEL# Hold Time	T2	9	10	11	nS
Clock 6 to STOP# Hold Time	T3	9	10	11	nS

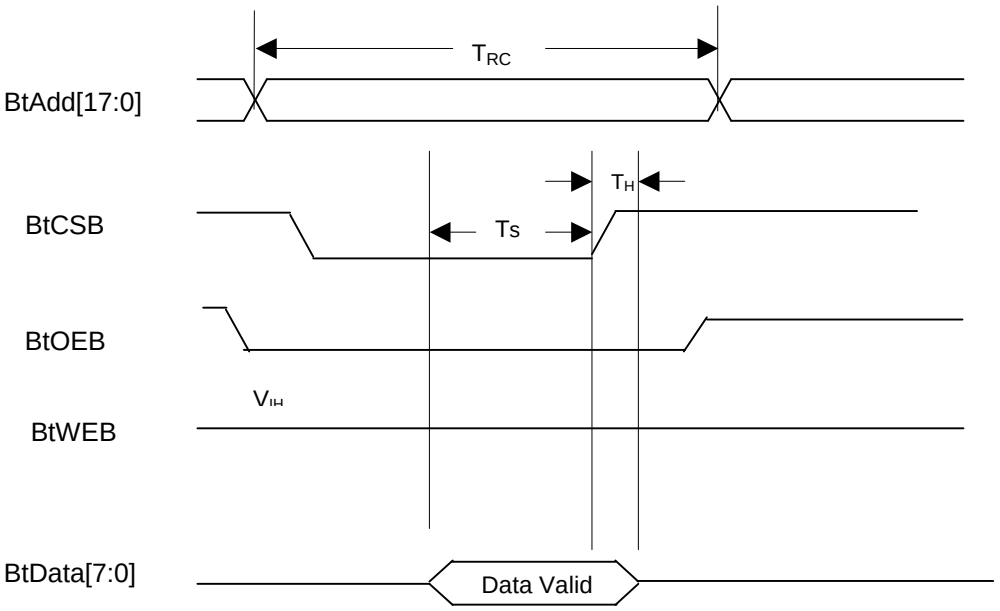
Notes:

1) The other timing requirements for PCI input signal are as the read transaction timing.

2) T2 and T3 are used for the target abort type (host addressing error).

AC Characteristics, continued

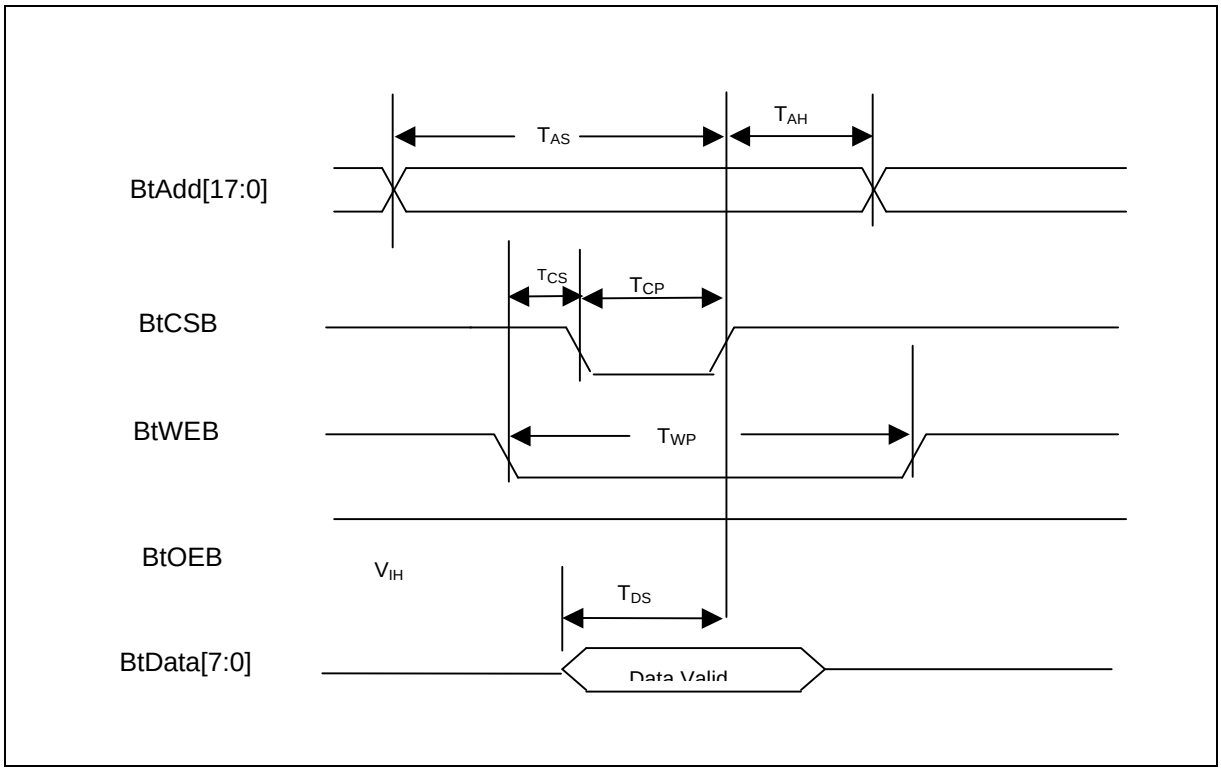
Boot ROM Read Cycle Timing



PARAMETERS	SYMBOL	MIN.	MAX.	UNIT
Read Cycle Time	TRC		330	nS
Data Set-up Time	TS	5	-	nS
Data Hold Time	TH	2	-	nS

AC Characteristics, continued

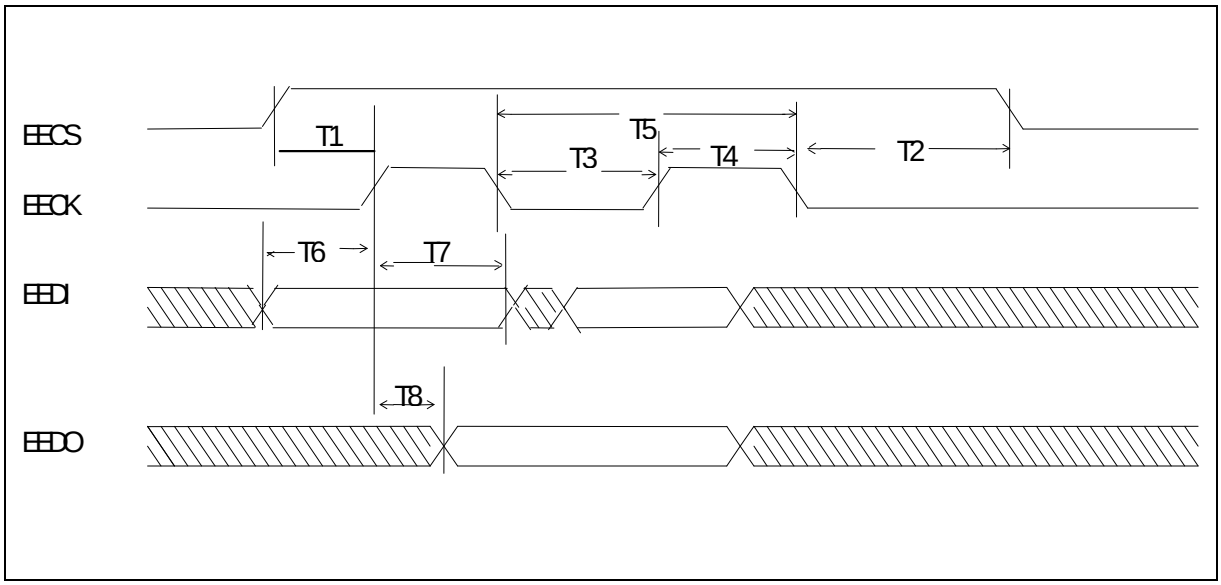
Boot Rom Write Cycle Timing



PARAMETERS	SYMBOL	MIN.	MAX.	UNIT
Address Set-up Time	T_{AS}	-	150	nS
Address Hold Time	T_{AH}	-	60	nS
BtWEB and BtCSB Set-up Time	T_{CS}		88	nS
BtCSB Pulse Width	T_{CP}	-	120	nS
BtWEB Pulse Width	T_{WP}	-	600	nS
Data Set-up Time	T_{DS}	-	120	nS

AC Characteristics, continued

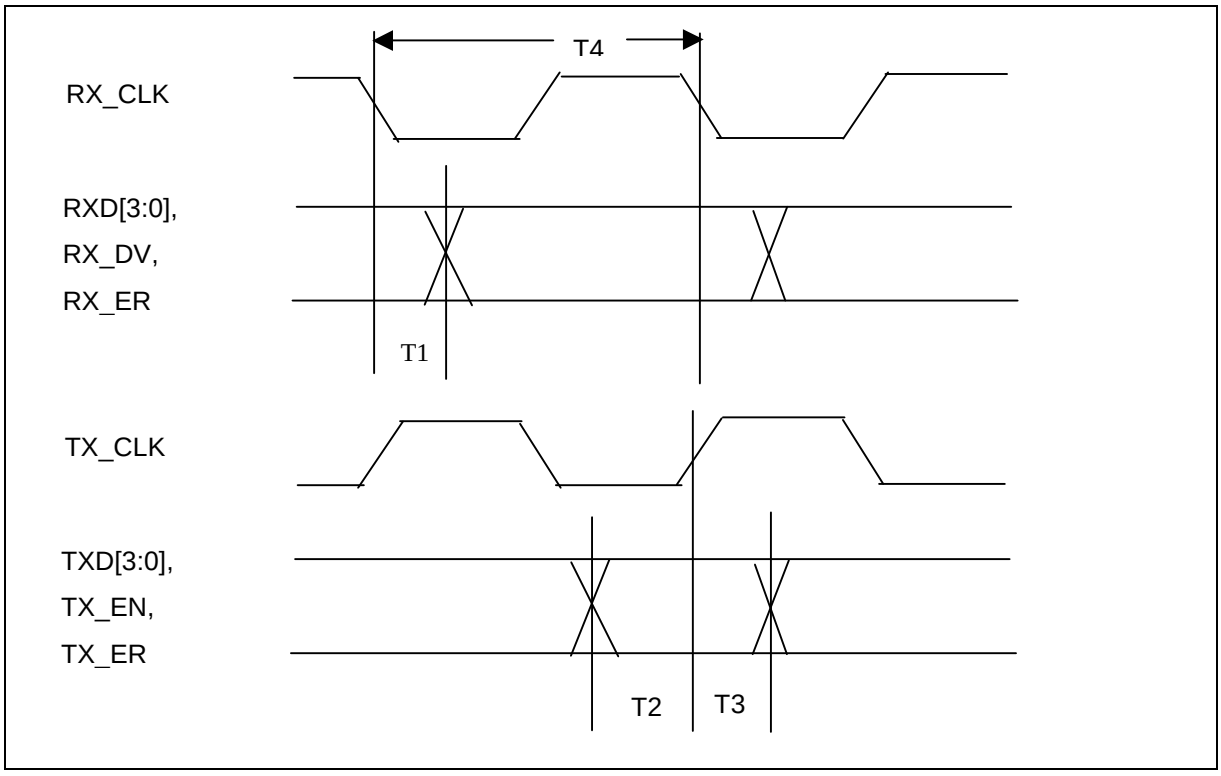
Serial EEPROM Timing



PARAMETERS	SYMBOL	TYP.	UNIT
EECS Asserted to EECK	T1	610	nS
EECS Hold from EECK	T2	3	nS
EECK OFF Time	T3	600	nS
EECK ON Time	T4	600	nS
EECK Clock Period	T5	1.2	uS
EEDI Set-up Time	T6	600	nS
EEDI Hold Time	T7	600	nS
EEDO Output Delay	T8	100	nS

AC Characteristics, continued

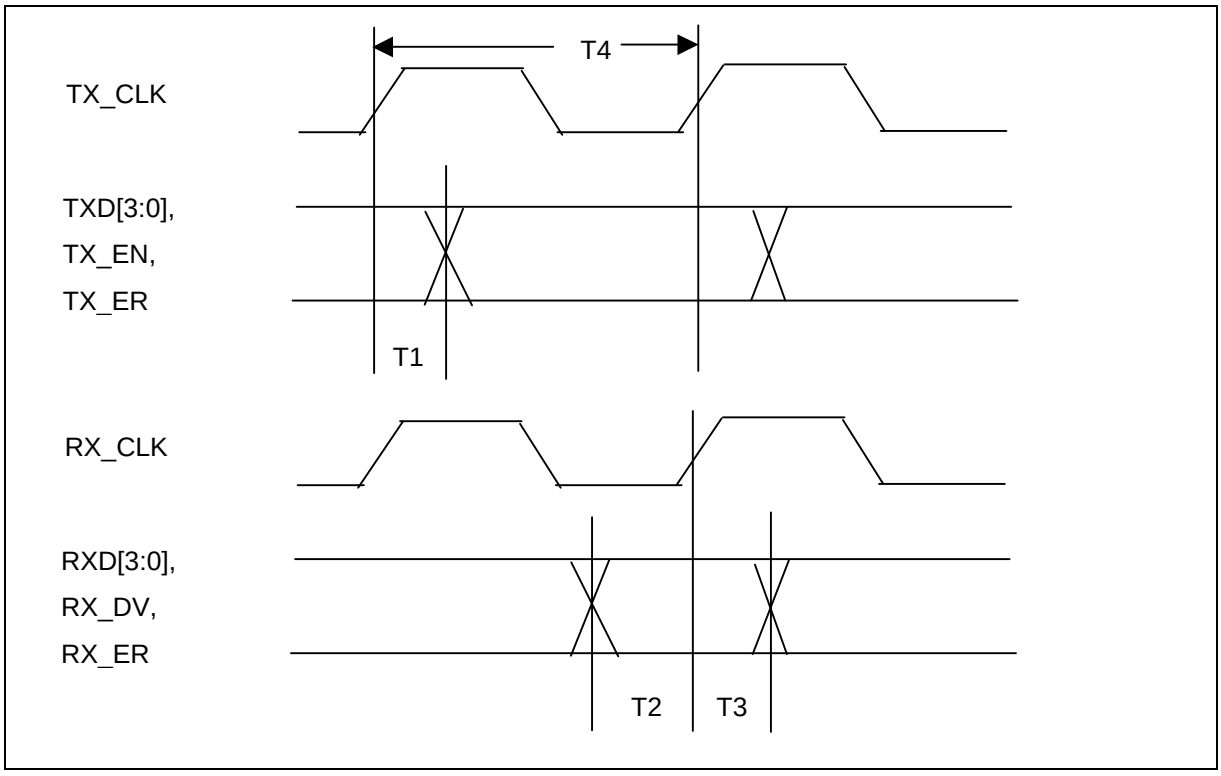
PHYceiver MII Timing



PARAMETERS	SYMBOL	TYP.	UNIT
Output Delay for RXD, RX_DV, RX_ER	T1	5	nS
Set-up Time for TXD, TX_EN, TX_ER	T2	15	nS
Hold Time for TXD, TX_EN, TX_ER	T3	0	nS
Clock Cycle (100M) (10M)	T4	40 400	nS

AC Characteristics, continued

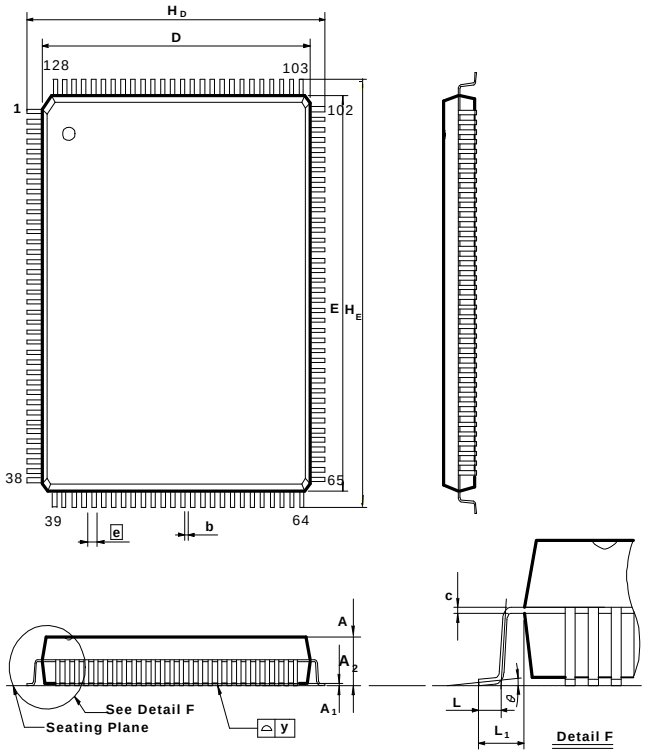
MAC Controller MII Timing



PARAMETERS	SYMBOL	TYP.	UNIT
Output Delay for TXD, TX_EN, TX_ER	T1	7	nS
Setup Time for RXD, RX_DV, RX_ER	T2	10	nS
Hold Time for RXD, RX_DV, RX_ER	T3	10	nS
Clock Cycle (100M) (10M)	T4	40 400	nS

11. PACKAGE DIMENSIONS

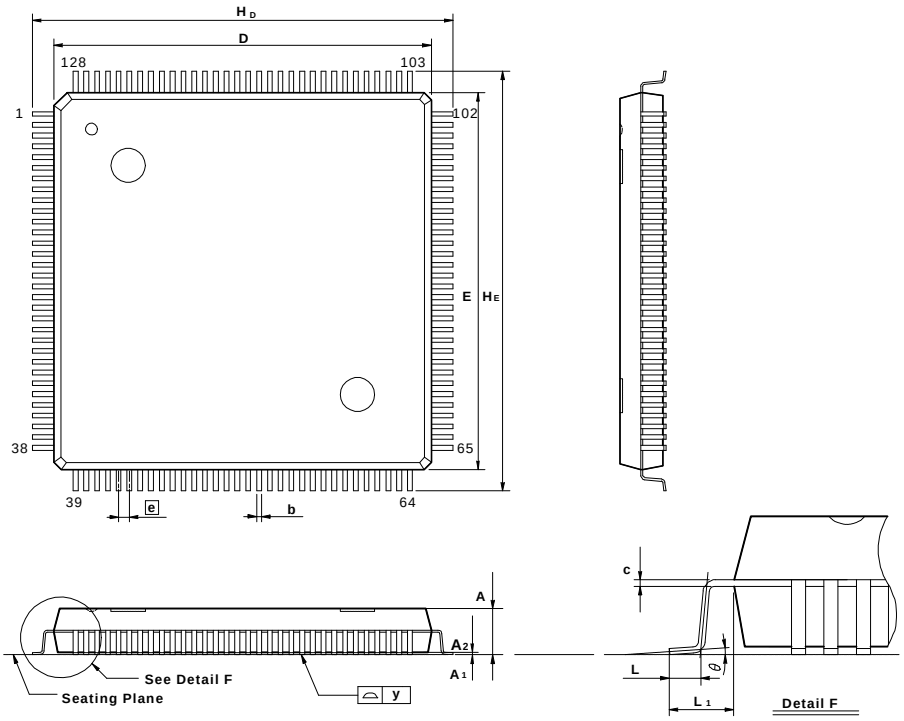
W89C841F: 128L QFP (14 x 20 x 2.75 mm footprint 3.2 mm)



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.134	—	—	3.40
A_1	0.004	—	—	0.10	—	—
A_2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e		0.020			0.50	
H_D	0.669	0.677	0.685	17.00	17.20	17.40
H_E	0.905	0.913	0.921	23.00	23.20	23.40
L	0.023	0.031	0.039	0.60	0.80	1.00
L_1	0.055	0.063	0.071	1.40	1.60	1.80
y	—	—	0.004	—	—	0.10
q	0°	—	12°	0°	—	12°

Package dimensions, continued

W89C841D: 128L LQFP (14 x 20 x 1.4 mm)



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.063	—	—	1.60
A_1	0.002	—	—	0.05	—	—
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.011	0.15	0.20	0.27
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	—	0.020	—	—	0.50	—
H_D	0.626	0.630	0.634	15.90	16.00	16.10
H_E	0.862	0.866	0.870	21.90	22.00	22.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	
y	—	—	0.004	—	—	0.10
q	0°	—	12°	0°	—	12°

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