

Keysight Technologies

M8040A High-Performance BERT 64 GBaud

Preliminary
Data Sheet
Version 0.9



Master your 400G design



Unlocking Measurement Insights

Introduction

The Keysight Technologies Inc. M8040A is a highly integrated BERT for physical layer characterization and compliance testing.

With support for pulse amplitude modulation 4-level (PAM-4) and non-return-to-zero (NRZ) signals, and symbol rates up to 64 GBaud (corresponds to 128 Gbit/s) it covers all flavors of the emerging 400/200 GbE and CEI-56G standards.

The M8040A BERT's true error analysis provides repeatable and accurate results, optimizing the performance margins of your devices.

Key features

- Data rates from 2 to 32 and 64 GBaud
- PAM-4 and NRZ selectable from user interface
- Built-in 4 tap de-emphasis to compensate loss
- Integrated and calibrated jitter injection: RJ, PJ1, PJ2, SJ, BUJ, and clk/2 jitter
- Two pattern generator channels per module to emulate aggressor lane
- Linearity tests with adjustable PAM-4 levels
- Short connections to the DUT with remote heads for the pattern generator
- True PAM-4 error detection in real-time for low BER levels
- Graphical user interface and remote control via M8000 system software
- Scalable and upgradeable with options and modules

Applications

The M8040A is designed for R&D and test engineers who characterize chips, devices, transceiver modules and sub-components, boards and systems with serial I/O ports operating with symbol rates up to 32 GBaud and 64 GBaud in the data center and communications industries.

The M8040A can be used for receiver (input) testing for many popular interconnect standards, such as:

- IEEE 802.3bs 400 and 200 Gigabit Ethernet (200GAUI, 200GBASE, 400GAUI, 400GBASE)
- IEEE 802.3bj 100 Gigabit Ethernet
- 50 Gigabit Ethernet
- OIF CEI - 56G (NRZ and PAM-4 versions)
- 64G/112G Fibre Channel
- Infiniband-HDR
- Proprietary interfaces for chip-to-chip, chip-to-module, backplanes, repeaters, and active optical cables, operating up to 64 GBaud.

M8000 Series of BER Test Solutions

Simplified time-efficient testing is essential when you are developing next-generation computer, consumer, or communication devices

The Keysight M8000 Series is a highly integrated BER test solution for physical layer characterization, validation, and compliance testing.

With support for a wide range of data rates and standards, the M8000 Series provides accurate, reliable results that accelerate your insight into the performance margins of high-speed digital devices.



New: PAM-4 BERT
up to 64 GBaud

Figure 1. The M8000 Series BER test solution is highly integrated and scalable to address the test challenges of the next generation of high-speed digital receiver test.

The M8040A high-performance BERT 64 GBaud extends the M8000 Series for 400G data center interconnect testing

M8040A High-performance BERT 64 GBaud

Simplifies accurate receiver characterization of devices operating up to 32 and 64 GBaud with NRZ and PAM-4 signals

Highest level of integration streamlines receiver test setups

With the M8040A, all critical test capabilities for input/receiver (RX) characterization are built-in. The pattern generator module provides calibrated and integrated jitter sources and de-emphasis to emulate the transmitter (TX) and to compensate for channel loss in the test setup. In addition, the M8040A provides an internal clock synthesizer and a second pattern generator output channel to emulate an aggressor lane.

The analyzer provides true PAM-4 and NRZ error analysis in real time and full sampling to measure down to very low BER and SER.

This high level of integration with the M8040A makes the receiver test set-up connections easier and more robust. Set up and debug time is shortened, calibration is simpler and the frequency of re-adjustments is reduced, resulting in a more efficient use of overall test time.

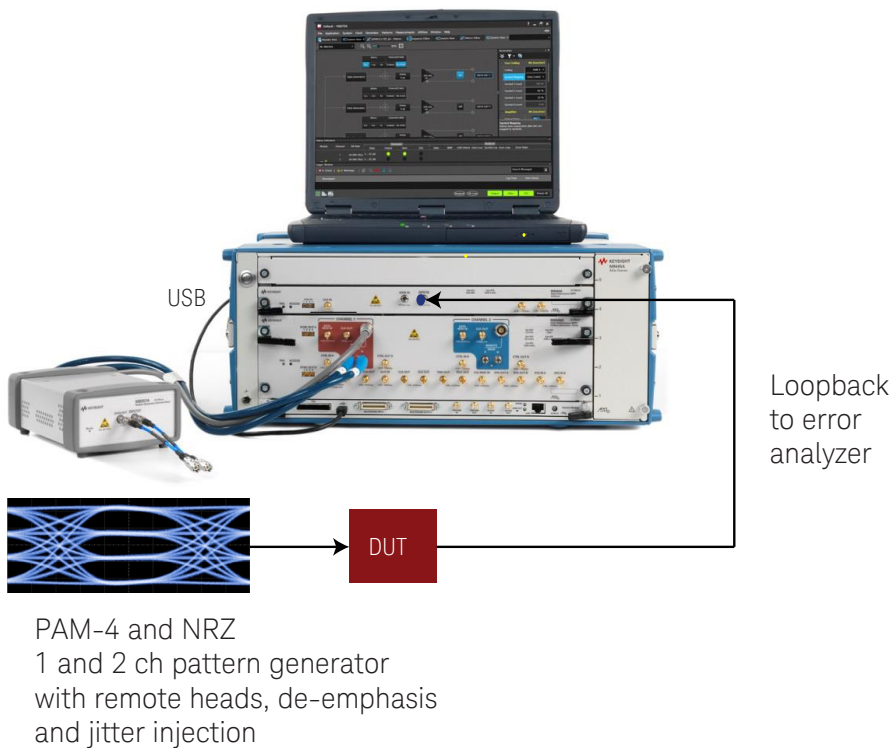


Figure 2. The M8040A streamlines complex receiver test setups. Each of the 1 or 2 pattern generator channels provides built-in de-emphasis, jitter sources, and a remote head to reduce the distance between the generator output and the DUT test board. The full sampling error analyzer can detect errors in real-time for NRZ and PAM-4 signals without the need to split up the PAM-4 signal for multiple error detector channels.

Repeatable and accurate results with M8040A

The M8040A high-performance BERT provides clean NRZ and PAM-4 signals up to 64 GBaud with fast transitions and low intrinsic jitter. The remote head concept of M8040A with the short 1.85 mm cables brings the performance close to the device under test, minimizing signal degradations caused by lossy channels.



Figure 3. The remote head M8057A is required for each channel and is required for NRZ and PAM-4 signals. It contains an adjustable gain amplifier without re-timer. Users can select NRZ or PAM-4 coding and de-emphasis taps settings from the user interface with no need to reconnect cables. The cable between the remote head and the module is 0.85 m long. This allows positioning the remote head closely to the test board for the device under test.

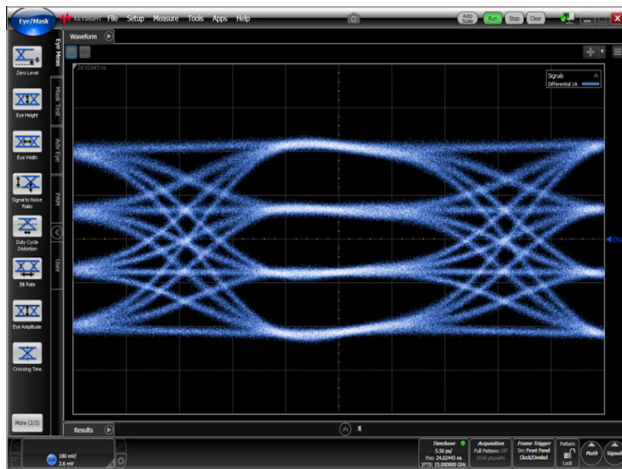


Figure 4. Clean 30 GBaud PAM-4 output signal of pattern generator module M8045A with remote head M8057A using the internal clock source with 600 mV output amplitude and PRBS2¹⁵-1. Measured with Infiniium DCA-X 86100D.

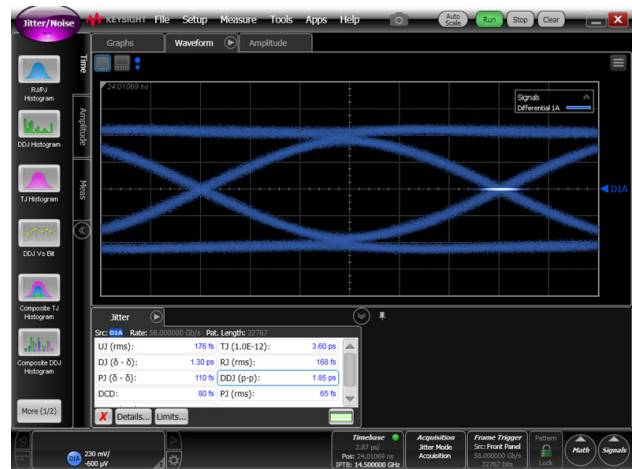


Figure 5. Clean 58 GBaud NRZ output signal of pattern generator module M8045A with remote head M8057A using the internal clock source with 600 mV output amplitude and PRBS2¹⁵-1. Measured with Infiniium DCA-X 86100D.

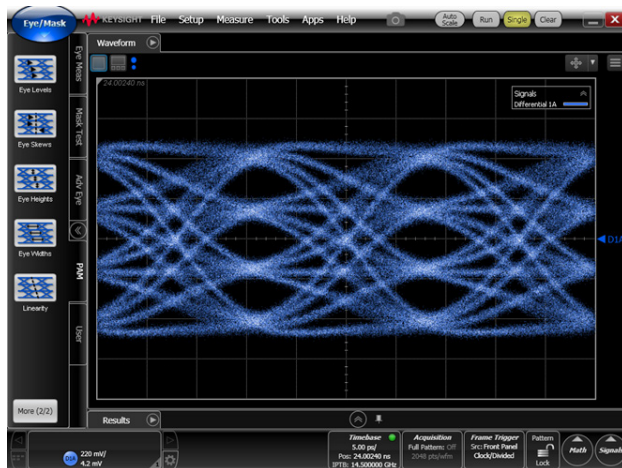
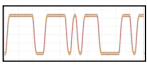
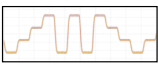


Figure 6. Clean 58 GBaud PAM-4 output signal of pattern generator module M8045A with remote head M8057A using the internal clock source with 600 mV output amplitude and PRBS2¹⁵-1.

Emulate stress conditions for NRZ and PAM-4 input tolerance testing with M8040A

M8040A provides all capabilities required for input tolerance test:

- 1 or 2 channels. Second channel can be used as aggressor lane to emulate crosstalk effects
- Data rates are adjustable from 2 Gb/s NRZ up to 64 GBaud PAM-4, selectable NRZ or PAM-4
- Algorithmic PRBS, QPRBS and memory-based patterns, pattern sequencer with loops, error injection
- Built-in and calibrated jitter sources that can be used simultaneously: RJ, multi-UI low-frequency jitter, multi-tone high-frequency jitter, BUJ, clk/2 jitter, spread-spectrum clocking (SSC)
- De-emphasis for pre- and post-cursor to emulate transmitter de-emphasis and compensate for loss in the test setup
- Automated jitter tolerance testing

	NRZ	PAM-4
		
Effective data rate	Bit rate	Symbol rate
32 Gbit/s	32 Gb/s	16 GBaud
64 Gbit/s	64 Gb/s	32 GBaud
128 Gbit/s	128 Gb/s	64 GBaud

Covered by M8040A

Related IEEE802.3bs 200GBASE/200GAUI proposed symbol rate * # of lanes	Related IEEE802.3bs 400GBASE/400GAUI proposed symbol rate * # of lanes	Related OIF CEI-56G proposed symbol rates
26.5625 Gbit/s NRZ * 8 lanes	26.5625 Gbit/s NRZ * 16 lanes	
26.5625 GBaud PAM-4 * 4 lanes	26.5625 GBaud PAM-4 * 8 lanes	LR-PAM-4: 19.6 to 30 GBaud
	53.125 Gbit/s NRZ * 8 lanes	MR-PAM-4: 18 to 29 GBaud
		MR-NRZ: 39 to 56.2 Gbit/s
		VSR-PAM-4: 19.6 to 29 GBaud
		VSR-NRZ: 39 to 56.2 Gbit/s
		XSR-PAM-4: 19.6 to 29 GBaud
		XSR-NRZ: 39.8 to 58 Gbit/s
		USR-NRZ: 19.6 to 58.0 Gbit/s
	53.125 GBaud PAM-4 * 4 lanes	

Figure 7. M8040A supports data rates up to 32 Gb/s NRZ, 64 Gb/s NRZ, 32 GBaud PAM-4 and 64 GBaud PAM-4. The user interface allows selection of NRZ and PAM-4 without reconnecting the BERT test setup.

Master PAM-4 receiver test challenges with M8040A

Design and test engineers who need to characterize devices that support PAM-4 data formats are facing new test challenges in addition to the signal integrity issues known from 25 Gb/s NRZ device testing.

For PAM-4 input receiver tolerance test, this means impairments that may occur in the real-world should be tolerated by the receiver under test without exceeding the desired BER level. Typical receiver tests include jitter tolerance, interference tolerance test and level sensitivity margins that are applicable for NRZ and PAM-4 devices. In addition PAM-4 receivers require additional margin testing for level non-linearity, cross-talk effects from adjacent lanes and vertical eye closure.

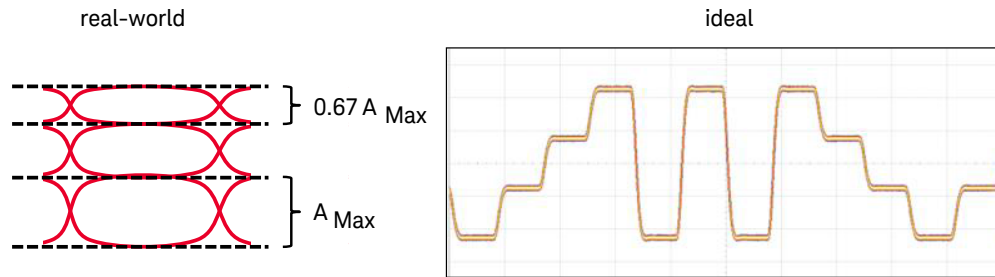


Figure 8. PAM-4 eyes can show a level separation mismatch. Receivers must be able to detect the digital signal content properly within the given mismatch ratio.

Real-time error analysis for PAM-4 and NRZ signals

Receiver verification checks if the receiver under test operates below the specified BER while emulating the worst-case transmitter and channel conditions.

BER measurements are well established for NRZ signals by using a traditional BERT, but what does this mean for PAM-4 signals?

For proper error detection of PAM-4 signals, all thresholds (V_{low} , V_{mid} , and V_{upper}) have to be analyzed simultaneously to ensure a correct symbol error measurement. (See Figure 8.) If a “1” is detected at the V_{mid} threshold, the received pattern can have level 2 or 3. Only if the level detected at V_{upp} is checked simultaneously with V_{mid} , it can be determined if the received inputs have the correct level for a 2 or a 3. If two thresholds are errored within one UI, this case translates just into one symbol error.

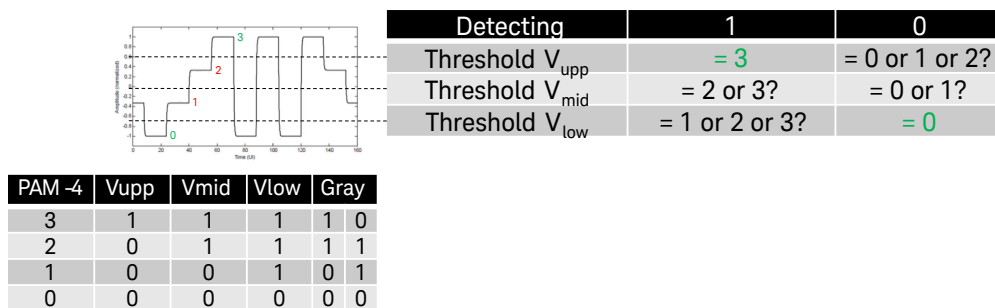


Figure 9. Only a true PAM-4 error analyzer like M8040A, can provide a PAM-4 symbol error rate in real-time without post-processing. Error ratios down to 10^{-15} or error-free can be measured even for long PRBS $2^{31}-1$, QPRBS13-CEI or QPRBS31-CEI patterns. Errored 0,1,2,3 and symbol errors can be counted separately for further debugging.

Specifications for M8045A and M8046A modules and M8057A remote head

M8045A pattern generator module for two data channels, 3-slot AXIe



M8045A Pattern generator module for one data channel, 3-slot AXIe



M8057A remote head with cable connections (0.85 m) front and rear view



M8046A analyzer module, 1-slot AXIe



Figure 10. Front panel views of pattern generator module M8045A (top) as 2 and 1 channel (center) versions, remote head M8057A, and error analyzer module M8046A (bottom). To allow a very short connection to the device under test, the remote head is used. One remote head is needed for each of the pattern generator data outputs of M8045A.

Specifications for pattern generator module M8045A and remote head M8057A

Data output (DATA OUT 1, DATA OUT 2)

The pattern generator supports symbol rates up to 32 GBaud or 64 GBaud, default is one channel and NRZ format.

The remote head M8057A is needed once per channel. Using the P and N outputs of the M8045A without remote head is prohibited.

For the following generator functions a separate module option is required:

- PAM-4 coding up to 32 GBaud (M8045A Option OP3)
- PAM-4 extension to 64 GBaud (M8045A Option OP6)
- Second data channel (M8045A Option OG2)
- Advanced jitter sources (M8045A Option OG3)
- De-emphasis (M8045A Option OG4)

Table 1. Data output characteristics for M8045A with remote head M8057A.

All timing parameters are measured @ 0.5 V into ground at data outputs of remote head M8057A	
Symbol rate	2.025 to 32.4 GBaud for M8045A Option -G32 2.025 to 58.0 GBaud (all specifications are valid up to 58 GBaud with over-programming up to 64.8 GBaud) for M8045A Option -G64
Data format	NRZ (default) PAM-4 (requires M8045A Option -OP3 and for symbol rates above 32 GBaud -OP6 in addition)
Channels per module	1 or 2 (requires M8045A Option -OG2 and second remote head)
Amplitude	
For symbol rates < 32.4 GBaud	50 mV to 0.9 Vpp single ended 100 mV to 1.8 Vpp differential
For symbol rates < 58 GBaud	50 mV to 0.6 Vpp single ended 100 mV to 1.2 Vpp differential
Amplitude accuracy	5 % ± 5 mV typical (AC) ¹
Output voltage window	-1 to +3.0 V
External termination voltage	-1 to +3.0 V. For offset > 1.3 V the termination voltage should be ± 0.5 V of offset
Transition time	9 ps typical (20 to 80%) ²
Intrinsic total jitter	Tbd
Intrinsic Clk/2 jitter	Tbd
Intrinsic random jitter	Tbd fs rms typical for NRZ
Data delay range	0 to 10 ns, resolution 100 fs
Data delay accuracy	± (max. (1.5 ps or 10 mUI whatever is higher) + 1 % of entered value) typical ³
Deskew accuracy	Tbd
SNR	Tbd
Skew between normal and complement output	3 ps maximum at the end of the recommended cable pair. Fixed.
Termination	50 Ω into GND or external termination voltage. Do not operate into open. Unused outputs must be terminated into termination voltage.
Termination modes	Balanced/unbalanced
Coupling	DC/AC selectable coupling of device under test
Connectors	1.85 mm, female

1. At Tbd measured with DCA-X 86108B and clock pattern and in the middle of the eye.

2. Measured with DCA-X 86118A.

3. At constant temperature.

De-emphasis (DATA OUT)

The M8045A provides built-in de-emphasis with positive and negative cursors based on a finite impulse response (FIR) filter see Figure 10. Users can enter the de-emphasis in coefficient values.

Table 2. Specifications for multi-tap de-emphasis (requires Option 0G4).

	NRZ	PAM-4
De-emphasis taps	4, can be adjusted for each channel independently	
Pre-cursor coefficient c0	0.0 to $\pm 0.40^1$	0.0 to $\pm 0.40^1$
Main cursor coefficient c1	0.0 to $\pm 0.40^1$	0.0 to $\pm 0.40^1$
Post-cursor coefficient c2	0.0 to $\pm 1.0^1$	0.0 to 1.0^1
Post-cursor coefficient c3	0.0 to $\pm 0.40^1$	0.0 to $\pm 0.40^1$
Cursor coefficient resolution	0.01	0.01

- Sum of all cursors absolute values may not exceed 1.0 $|c0| + |c1| + |c2| + |c3| \leq 1$. Also $|c0|, |c1|, |c3| < |c2|$.

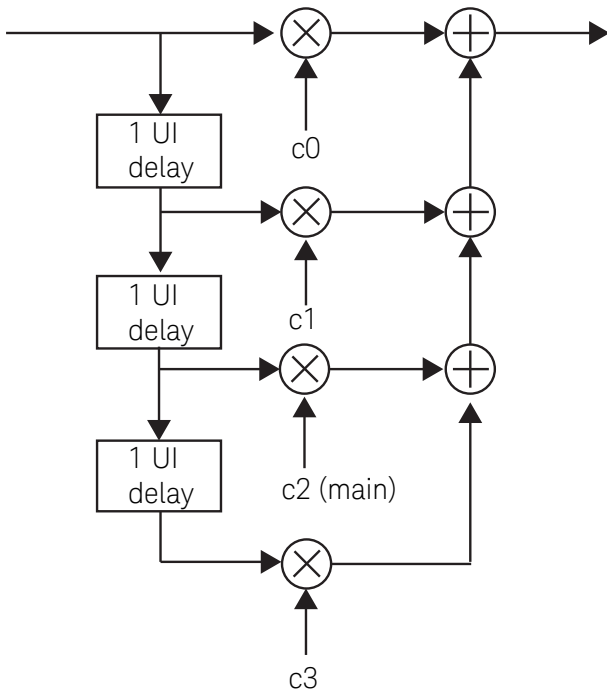


Figure 11. The pattern generator of M8045A provides integrated de-emphasis to emulate TX equalization. The post-cursor c3, main cursor c2 and two pre cursors c0 and c1 can be adjusted.

Clock output 1 and 2 (Channel 1 CLK OUT, Channel 2 CLK OUT)

These clock outputs provide two modes. They can operate with the same jitter as the corresponding data output or operate in a clean mode.

Table 3. Specifications for channel 1 clock output and channel 2 clock output.

Frequency range	1.0125 to 16.2 GHz with M8045A-G32 1.0125 to 32.4 GHz with M8045A-G64	
Frequency divider factors	Symbol rate / clock divider: 2, 4, 8, 16. Divided output frequency must fit into frequency range	
Clean clock mode	On	No jitter injection, no SSC
	Off	Same jitter and SSC as data output of same channel
Amplitude	1 V typical nominal single ended	
Duty cycle	50%, accuracy \pm 15% typical	
Intrinsic random jitter	Tbd rms typical	
Termination	50 Ω into GND or external termination voltage. Do not operate into open.	
Coupling	AC coupled	
Connectors	3.5 mm, female	

Clock output (CLK OUT)

This is a differential clock output with many sub-rate clock dividers. LF SJ and HF jitter can be turned off and on individually. HF jitter has the same setting as HF jitter of data output of channel 1.

Table 4. Clock output specifications.

CLK frequency range	1.0125 to 16.20 GHz	
Clock divider in relation to clock frequency range	n * (1, 2, 4, 8, 10, 16, 20, 24, 30, 32, 40, 50, 64, 66, 80) with n= 1 < 16.2 GHz n= 2 for 16.2 GHz to 32.4 GHz n= 4 > 32.4 GHz For other dividers use TRIG OUT	
Frequency resolution	1 Hz	
Frequency accuracy	± 15 ppm	
Amplitude	Differential	0.2 to 2.0 V, 10 mV steps
	Single ended	0.1 to 1 V, 5 mV steps
Output voltage window	-1 to +3 V ¹	
External termination voltage	-1 to +3 V	
Transition times	20 ps typical (20 to 80%)	
Duty cycle	50%, accuracy ± 15%	
Clock modes	See Table 5	
Intrinsic random jitter	300 fs rms typical at 16.2 GHz and clock divider = 1	
SSB phase noise ²	- 85 dBc/ Hz typical at 10 kHz offset and internal clock and 10/100 MHz as external reference clock - 80 dBc/Hz with 10 kHz offset for reference clock multiplier bandwidth 0.1 MHz	
Termination	50 Ω into GND or external termination voltage. Do not operate into open. Unused outputs must be terminated into termination voltage	
Coupling	DC coupled, differential	
Connectors	3.5 mm, female	

1. If V_{term} is other than 0 V the following applies:
High level voltage range= $2/3 * V_{\text{term}} - 0.95 \text{ V} < \text{HIL} < V_{\text{term}} + 2 \text{ V}$
Low level voltage range= $2/3 * V_{\text{term}} - 1 \text{ V} < \text{LOL} < V_{\text{term}} + 1.95 \text{ V}$
2. For 8.1 to 16.2 GHz clocks.

Table 5. Clock modes.

Clock mode	Clock generation	Input frequency range
Internal	PLL with internal reference	N/A
Reference	PLL with bandwidth below 1 kHz	10/100 MHz
Direct	No PLL	8.1 to 16.2 GHz
Reference clock multiplier bandwidth 100 kHz	m/n PLL with loop bandwidth 100 kHz m, n = 1 to 1620	10 MHz to 16.2 GHz

Supplementary inputs and outputs of M8045A

Reference clock input (REF CLK IN)

This input allows locking the system clock to an external reference clock of 10 or 100 MHz instead of the internal oscillator. It also allows using an external clock, see clock modes as shown in table 5. A SSC tolerant PLL is used to multiply the external reference clock to the system clock.

Table 6. Reference clock input specifications (M8045A only).

Input amplitude	0.2 to 1.4 Vpp
Input frequency	10 MHz to 16.2 GHz, depends on clock mode and max. data rate option
Interface	Single ended. 50 Ω nominal
Connector	SMA, female

Trigger output (TRG OUT)

This output is used to send a trigger signal to another connected device, such as an oscilloscope. Also it can be used to generate a subrate clock.

The trigger output can be used in different modes:

1. Divided clock, dividers:
 - a. For < 16.2 GBaud trigger data rate range 2 to 65532
 - b. For 16.2 to 32.4 GBaud trigger data rate range 4 to 65532 with step resolution of 2
 - c. For > 32.4 GBaud trigger output data rate range 8 to 65532 with step resolution of 4
2. Sequence block trigger with adjustable pulse width and offset
3. PRBS sequence trigger with adjustable pulse width

Table 7. Trigger output specifications.

Amplitude	single-ended	0.1 to 1.0 Vpp
	differential	0.2 to 2.0 Vpp
Output voltage window		-1 to 3 V ¹
External termination voltage		-1 to 3 V
Interface		Differential, 50 Ω
Connector		3.5 mm, female

1. If V_{term} is other than 0 V the following applies:
 High level voltage range = $2/3 * V_{\text{term}} - 0.95 \text{ V} < \text{HIL} < V_{\text{term}} + 2 \text{ V}$
 Low level voltage range = $2/3 * V_{\text{term}} - 1 \text{ V} < \text{LOL} < V_{\text{term}} + 1.95 \text{ V}$

Reference clock output (REF CLK OUT)

Outputs a 10 and 100 MHz clock, 1 Vpp single ended into 50 Ω .

Connector: SMA, female.

Control input A and B (CTRL IN A, CTRL IN B)

Functionality of each input can be selected as: sequence trigger, error add and pattern capture event.

Table 8. Control input specifications.

Input voltage	-1 V to +3 V
Termination voltage	-1 V to +3 V
Threshold voltage	-1 V to +3 V
Delay to data output	Tbd
Connector	3.5 mm, female

Supplementary inputs and outputs of M8045A (continued)

Control output A and B (CTRL OUT A, CTRL OUT B)

Outputs a pulse in case of an error. Generates a pulse or static high/low if used from sequencer.

Table 9. Control output specifications.

Amplitude ¹	0.1 to 2 V
Output voltage ¹	-0.5 to 1.75 V
Delay to data output	$\pm 512 UI \pm \text{jitter amplitude}/2$
Connector	3.5 mm, female

1. When terminated with 50 Ω into GND. Doubles into open.

Synchronization out (SYNC OUT)

The sync output is a clock output to synchronize additional modules to a common clock. Can be used to sync the M8046A with the system internal clock.

System input A/B (SYS IN A/B)

These are control inputs to synchronize events for the pattern sequencer.

Table 10. System input specifications.

Input voltage	-1 V to +3 V
Termination voltage	-1 V to +3 V
Threshold voltage	-1 V to +3 V
Delay to data output	Tbd
Connector	SMA, female

System output A/B (SYS OUT A/B)

Generates a pulse or static high/low controlled by the pattern sequencer. A and B outputs are identical.

Table 11. System output specifications.

Amplitude ¹	0.1 to 2 V
Output voltage ¹	-0.5 to 1.75 V
Delay to data output	$\pm 512 UI \pm \text{jitter amplitude} /2$
Connector	SMA, female

1. When terminated with 50 Ω into GND. Doubles into open.

Auxiliary input (AUX IN)

Not used.

Clock input (CLK IN)

For future use. See reference clock input for direct clock mode.

Jitter specifications

The M8045A has integrated and calibrated jitter sources. To use the jitter injection the M8045A Option -0G3 is required.

Table 12. Specifications for low frequency periodic jitter (requires Option -0G3 advanced jitter sources).

Low frequency periodic jitter (LF PJ)	Amplitude range	0 to 123.5 UI * symbol rate (in GBaud) for modulation frequencies of 100 Hz to 10 kHz, see table below. For modulation frequencies between 10 kHz and 40 MHz the maximum
(generated by IQ modulator)		$LF PJ = \frac{7.792 \text{ UI} * 10^{-3} * \text{symbol rate}}{\text{modulation frequency}^{1,2}}$
	Frequency	100 Hz to 40 MHz, sinusoidal modulation
	Jitter amplitude accuracy	$\pm 2\% \pm 1 \text{ ps}$ typical
	Adjustable	For each data channel independently, same LFPJ for clock and trigger

Low frequency periodic jitter

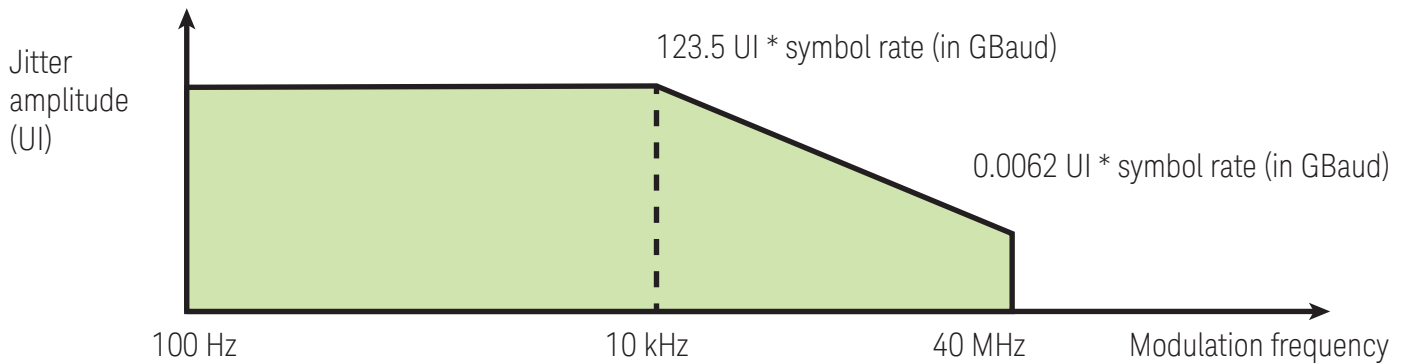


Figure 12. Low frequency periodic jitter maximum depends on data rate and modulation frequency.

Table 13. System output specifications.

Symbol rate	Max UI at modulation frequency 100 Hz to 10 kHz	Max UI at modulation frequency 10 MHz	Max UI at modulation frequency 40 MHz
2.025 to 4.05 GBaud	250 to 500 UI	0.0625 to 0.125 UI	0.012 to 0.024 UI
4.05 to 8.1 GBaud	500 to 1000 UI	0.125 to 0.25 UI	0.024 to 0.048 UI
8.1 to 16.2 GBaud	1000 to 2000 UI	0.25 to 0.5 UI	0.048 to 0.095 UI
16.2 to 32.4 GBaud	2000 to 4000 UI	0.5 to 1 UI	0.095 to 0.19 UI
32.4 to 64.8 GBaud	4000 to 8000 UI	1 to 2 UI	0.19 to 0.38 UI

Table 14. Specifications for high frequency periodic jitter, random jitter, bounded uncorrelated jitter, clock /2 jitter (all require M8045A Option -OG3 advanced jitter sources).

High frequency jitter (generated by delay line)	Range	1 UI for > 32.4 GBaud, for ≤ 32.4 GBaud minimum of: - 1 UI - 1 UI - (PJ frequency - 250 MHz) / 100 MHz * 0.2 UI - 0.5 UI if RJ low pass filter is 1000 MHz - 0.5 UI if external delay modulation is on Note: This is max sum of RJ, HF-PJ1 and HF-PJ, external delay modulation and BUJ.
High frequency periodic jitter (HF PJ1 and HF PJ2)	Range	See HF jitter above ¹
	Frequency	1 kHz to 500 MHz. For symbol rates < 4 GBaud the max modulation frequency is symbol rate / 8. Two tone possible. Sweep.
	Jitter amplitude accuracy	±3 ps ± 10% typical
	Adjustable	For each channel independently
Random jitter (RJ)	Range	0 to 72 mUI rms (1 UI p-p max.) ¹
	Jitter amplitude accuracy	±300 fs ± 10 % typical
	Filters	High-pass: 10 MHz and "off", Low-pass: 100 MHz, Low pass: 500 MHz (for symbol rates ≥ 3.75 GBaud), Low pass: 1 GHz (for symbol rates ≥ 7.5 GBaud)
	Adjustable	For each channel independently
Bounded uncorrelated jitter (BUJ)	Range	See HF jitter above ¹
	PRBS polynomials	2 ⁿ -1, n = 7, 8, 9, 10, 11, 15, 23, 31
	Filters	50/100/200 MHz low pass 3rd order
	Jitter amplitude accuracy	± 5 ps ± 10% typical for settings shown in Table 15
	Adjustable	For each channel independently
	Rate for PRBS generator	625 Mb/s, 1.25 Gb/s, and 2.5 Gb/s
Clock/2 jitter (so called even-odd jitter)	Range	Tbd
	Jitter amplitude accuracy	±3 ps typical
	Adjustable	For each channel independently

1. 1 UI is the maximum sum of RJ, HF-PJ1 and HF-PJ2, external delay modulation and BUJ.

Table 15. BUJ accuracy applies for these BUJ settings.

BUJ calibration settings ¹	Rate for PRBS generator	PRBS polynomial	Low pass filter
CEI 6G	1.25 Gb/s	PRBS 2 ⁹ -1	100 MHz
CEI 11G	2.5 Gb/s	PRBS 2 ¹¹ -1	200 MHz
Gaussian	2.5 Gb/s	PRBS 2 ³¹ -1	100 MHz
CEI 25G	2.5 Gb/s	PRBS 2 ¹¹ -1	200 MHz
CEI 56G	2.5 Gb/s	PRBS 2 ¹¹ -1	200 MHz

1. Other settings are not calibrated and do not necessarily generate the desired jitter histograms for all data rates of the PRBS generator.

Table 16. Specifications for spread spectrum clocking (SSC). Requires M8045A Option -OG3 advanced jitter sources.

SSC (spread spectrum clock)	Range	0 to 10,000 ppm (0 to 1%) peak-peak. Select center-spread, up-spread, and down-spread.
	Frequency	100 Hz to 200 kHz
	Modulation	Triangular and arbitrary modulation
	SSC amplitude accuracy	±0.025% typical
	Outputs	Can be turned on/off together for CLK OUT, DATA OUT 1, DATA OUT 2, TRG OUT, CLK OUT channel 1/2

External jitter modulation

An external modulation source can be used to modulate the delay of the M8045A data outputs, clock output and trigger output.

DATA MOD IN 1, 2

This input can be used for delay modulation by an external source for each data output channel individually.

Table 17. Specifications for external jitter modulation on data outputs.

External jitter - data modulation input 1 and 2	Range	Up to 1 UI ¹ , 0.8 Vpp max
	Frequency	Up to 500 MHz
Gain		1UI/0.725 V ± 5%
Linearity		50 mUI
Connectors		3.5 mm, female

1. See HF jitter specifications for the maximum sum of RJ, HF-PJ1 and HF-PJ2 external delay modulation and BUJ.

CLK MOD IN

This input can be used for delay modulation of TRIG OUT and CLK OUT, the modulation always affects both outputs.

Table 18. Specifications for external jitter modulation for clock and trigger.

External jitter - clock modulation input	Description	Input for the delay modulation for the TRG OUT and CLK OUT. Affects both
	Range	Up to 1 UI ¹ , 0.8 Vpp max
	Frequency	Up to 1 GHz
Gain		1UI/0.725 V ± 5%
Linearity		50 mUI
Connectors		SMA, female

1. See HF jitter specification for the maximum sum of RJ, HF-PJ1 and HF-PJ2, external delay modulation and BUJ.

Pattern and sequencer

Table 19. Specifications for pattern, sequencer.

PRBS ¹	$2^n - 1$, n = 7, 10, 11, 15, 23, 23p, 31, 33, 35, 39, 45, 49, 51, 58
PRBS	2^n , n = 7, 10, 11, 13, 15, 23
QPRBS	OIF-CEI: QPRBS13-CEI, QPRBS31-CEI IEEE 802.3: QPRBS13, PRBS13Q, PRBS31Q, SSPRQ
New patterns in library	PAM-4-linearity, JP03A, JP03B
PAM-4 coding	Gray coding, custom mapping of 00, 01, 10, 11 to symbols 0, 1, 2, 3
Mark density	PRBS 1/8 to 7/8
Zero substitution	Yes
Export/Import	Patterns from M8000 and N4900 series can be imported
Pattern library	Yes
User definable memory	NRZ: 2 Gbit/channel PAM-4: 1 Gsymbol/channel
Vector/sequence granularity	512 bit
Pattern capture	Yes, raw data for PAM-4 Capture data starts on event <ul style="list-style-type: none"> - User defined (minimum) amount of pre-event bits/ symbols and minimum capture bit/symbols - Events: error, CTRL IN A /B, immediate - Max 2 Gbit/ch capture data for NRZ, 1 Gsymbol/ch for PAM-4 Save captured data: <ul style="list-style-type: none"> - With errors - As expected data (ignores error content) - As PG data (ignores error content) - Export via pattern editor windows - Convert bits into all other codings and vice versa - Ability to mask error bits automatically Display of captured data: <ul style="list-style-type: none"> - Display errors with color coding Navigate through error bits/symbols (find next/previous)
Pattern sequencer	3 counted loop levels, 1 infinite loop, # of blocks: 500
Masking	Expected bits and be masked (ignored) during error counting. Bitwise and block-wise masking is possible.

1. Polarity is inverted compared to ParBERT and J-BERT N4903A/B and N49xx series.

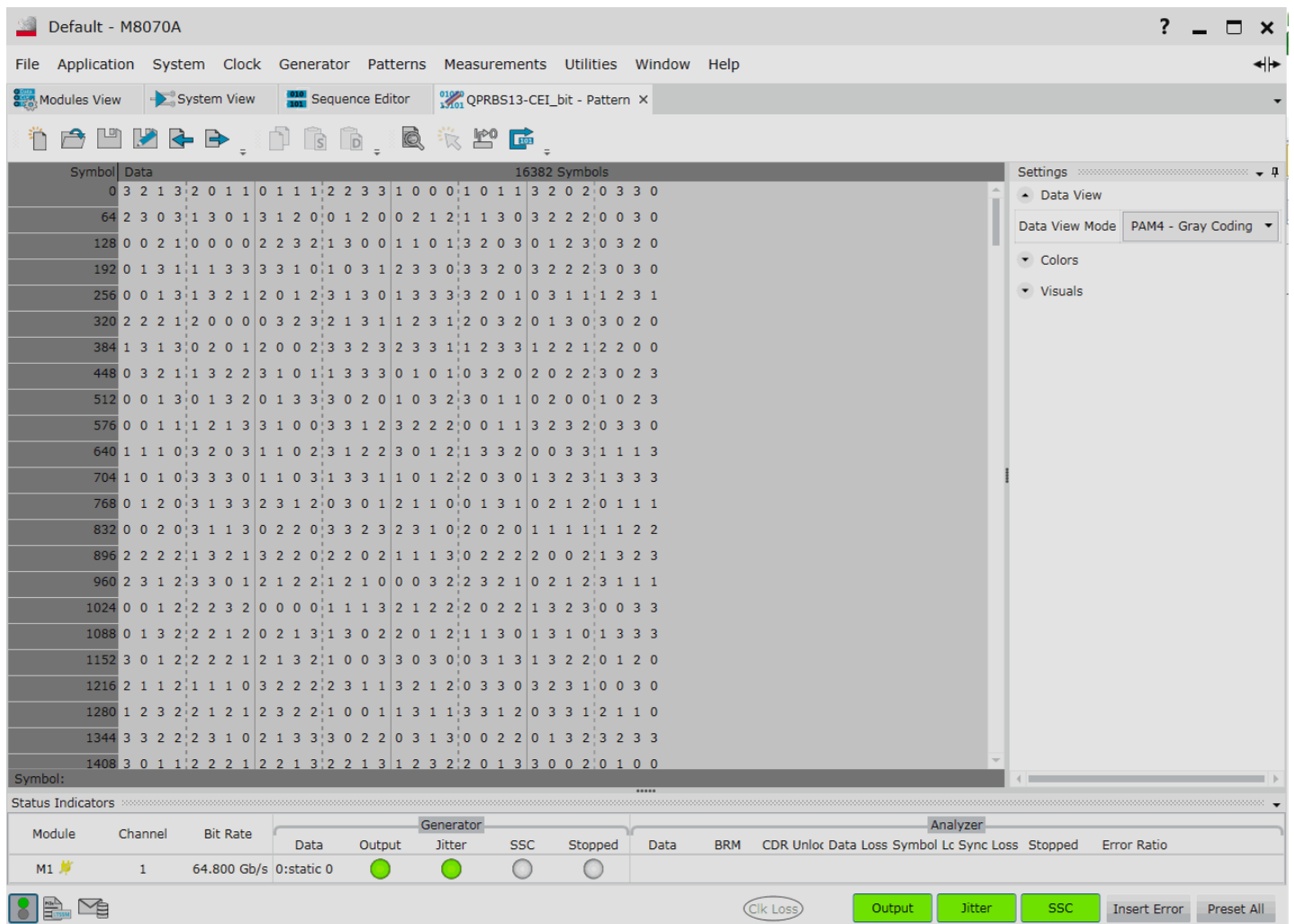


Figure 13. The pattern editor in the M8070A software allows editing NRZ bits and PAM-4 symbols. The PAM-4 symbol to bit mapping can be selected as Gray coded or custom with adjustable PAM-4 levels. Quaternary PRBS, like QPRBS13-CEI or QPRBS31, according to CEI and IEEE standards can be selected as well as SSPRQ and PAM-4 linearity test patterns.

Specifications analyzer module (error detector) M8046A



Figure 14. Front panel of M8046A

The M8046A supports symbol rates up to 32 GBaud, the default is NRZ format.

The analyzer module can be used for error analysis in conjunction with the M8045A pattern generator and the M8195A/M8196A arbitrary waveform generator. For the following functions a separate module option is required:

- PAM-4 decoding up to 32 GBaud (M8046A Option -0P3)

Data input (DATA IN)

Table 20. Specifications for analyzer/error detector.

Symbol rate	2.025 to 32.4 GBaud for M8046A-A32
Channels per module	1
Data format	NRZ (default) PAM-4 (requires M8046A Option -0P3)
Max # of M8046A per M9505A chassis	up to 4 (limited by chassis power)
Input sensitivity ¹	NRZ: 70 mV single ended and differential PAM-4: 70 mV per eye single ended and differential
Max input voltage amplitude	1000 mVpp differential
Input voltage window	-1 V to +3 V
Timing resolution	10 mUI
Input bandwidth	16 GHz typical
Sampling point	Manual and automatic. Finds optimum voltage threshold and delay of the sampling point. Delay accuracy ± 30 mUI. One sampling edge per UI.
Decision threshold range	NRZ: 10 to 90% of full scale input range with Tbd % resolution PAM-4: 10 to 90% of full scale input range with Tbd % resolution
Input equalizer	No
Phase margin	NRZ 1 UI - Tbd ps typical for PRBS $2^{15}-1$ 1 UI - Tbd ps typical for clock pattern
	PAM-4 1 UI - Tbd ps typical for PRBS $2^{15}-1$ 1 UI - Tbd ps typical for clock pattern
Interface	Differential: 100 Ω , Single ended: 50 Ω AC coupled
Connectors	2.4 mm, female

1. Measured with PRBS $2^{31}-1$ at Tbd Gb/s, at BER of 10^{-12} , clean eye

External clock input (CLK IN)

Table 21. Specifications for clock input of analyzer.

Amplitude	Minimum 400 mVpp, maximum 1 Vpp
Frequency range	Symbol rate /2 up to 32.4 GHz or full rate Symbol rate > 32.4 GBaud Rate /4 /2
Divider internal	1, 2
Connector	3.5 mm, female

SYNC input (SYNC IN)

Can be used to clock the analyzer from the pattern generator's M8045A system clock via the sync output A/B (requires cable M8051A-801). Not needed if external clock is used.

Control input A (CTRL IN A)

Functionality can be selected as: sequence trigger, pattern capture event.

Table 22. Specifications for control inputs of analyzer.

Input voltage	-1 to +3 V
Termination voltage	-1 to +3 V
Threshold voltage	-1 to +3 V
Connector	3.5 mm, female

Control output (CTRL OUT A)

Outputs a pulse in case of an error. Generates a pulse or static high/low if used from sequencer.

Table 23. Control output specifications (M8045A and M8055A).

Amplitude	0.1 to 2 V
Output voltage	-0.5 to 1.75 V
Delay from data input	CTRL Out to DATA In Tbd
Delay from sequencer	Tbd
Connector	3.5 mm, female

Measurements

Table 24. Measurement capabilities.

BER, SER	Accumulation and instantaneous
BERT Scan with RJ, DJ separation	No
Jitter tolerance	Yes
Counters	Compared bits, errored bits Counted 0,1,2,3 Errored 0,1,2,3
BER versus parameter automated sweep	Yes ¹
Burst error analysis ¹	Yes ¹

1. Contact factory for availability.

User interface and remote control

The M8070A system software for the M8000 Series of BER test solutions is required to control the M8040A BERT.

The screenshot displays the M8070A software interface. The main window shows a block diagram of the system architecture. On the left, the 'System View' shows the flow from 'DATA MOD IN' and 'CLK MOD IN' through various jitter and delay blocks to the 'Data Generation static 0' and 'Line Coding PAM-4' blocks. The signal then passes through a PLL Synthesizer (Internal 32.400 GHz) and a Divider (+2) to produce 'REF CLK OUT', 'REF CLK IN', and 'CLK OUT 1'. The data path includes 'HF Jitter' and 'LF Jitter Sweep' blocks, followed by a 'Delay 0.0 ps' block and a '300 mV' amplifier to produce 'DATA OUT 1'. A 'TRIG OUT' signal is also generated. The clock path includes a 'Delay 0.0 ps' block and a '100 mV' amplifier to produce 'CLK OUT'. A 'Divisor + 4' block is also present in the clock path.

On the right, the 'Parameters' panel is open for 'M1.DataOut1'. The 'Line Coding' section is expanded, showing the following settings:

- Coding: PAM-4
- Symbol Mapping: Custom
- Custom Symbo...: 00,01,11,10
- Symbol 3 Level: 100 %
- Symbol 2 Level: 67 %
- Symbol 1 Level: 33 %
- Symbol 0 Level: 0 %

Below the parameters, the 'Output State' section shows the On/Off state of the output. The 'Status Indicators' at the bottom of the window show the following status for the 'Generator' and 'Analyzer' sections:

Generator		Analyzer													
Module	Channel	Bit Rate	Data	Output	Jitter	SSC	Stopped	Data	BRM	CDR Unlox	Data Loss	Symbol Lc	Sync Loss	Stopped	Error Ratio
M1	1	64.800 Gb/s	0:static 0	●	●	○	○								

At the bottom of the interface, there are several control buttons: 'Clk Loss', 'Output', 'Jitter', 'SSC', 'Insert Error', and 'Preset All'.

Figure 15. The graphical user interface offers multiple views that can be defined by the user. This example shows the preliminary system view on the left side and the pattern generator data output with the PAM-4 coding and level linearity parameters at the right.

Table 25. User interface and remote control interface.

System software	M8070A
Software licensing	Offline version does not require a license. For controlling the hardware you can choose between a transportable, perpetual license (M8070A-OTP) and a network, perpetual license (M8070A-ONP). The network license is only recommended when using multiple M8040A setups within one company. When ordering M8040A-BU1 the M8070A-OTP license will be pre-installed on the embedded controller.
Controller requirements	Embedded PC: Choose M8040A-BU1 for a pre-installed embedded controller M9536A including pre-installation of M8070A software and module licenses. Otherwise: M9536/7A 1-slot AXIe embedded controller, choose options for Windows 7 or 8, 8 or 16 GB RAM, SSD. External PC: USB connection recommended between external PC and AXIe chassis. Minimum of 8 GB RAM recommended. For PCIe connectivity please refer to list of tested PCs for AXIe Technical Note, pub no. 5990-7632EN
Operating system	Microsoft Windows 7 (64 bit) SP1, Windows 8 (64 bit), Windows 8.1 (64 bit)
Controller connectivity with AXIe chassis	USB 2.0 (Mini-B) recommended, PCIe 2.0/8x (only for highest data throughput and desktop PC)
Programming language	SCPI. Not compatible with N4900 Series and ParBERT 81250A
Remote control interface	Desktop or Laptop PC: LAN M9536A: LAN
Save/Recall	Yes
Export of measurement results	Jitter tolerance results as *.csv file
Display resolution	Minimum requirement 1024 x 768
Scripting interface	The built-in scripting engine is based on IronPython. It enables the control of the device under test as well as other test equipment. Function hooks are available to tailor your measurements, such as read-out of built-in error counters or initializing the device
DUT control interface	Enables access to built-in error counters and status registers of a device under test (BIST) for use with automated measurements like accumulated BER and jitter tolerance. Can also be used to customize the measurements to DUT specific needs. IronPython scripting and .net libraries are supported to interface with the DUT. Requires option M8070A-1TP or -1NP
Software pre-requisites	Microsoft Win 7 SP1 or 8 / 8.1, Keysight IO library rev. 17.2.20605 or above
Software download	See http://www.keysight.com/find/m8070a for latest version Minimum software required to control M8040A is M8070A revision 3.5 or higher

General characteristics and physical dimensions

Modules M8045A and M8046A

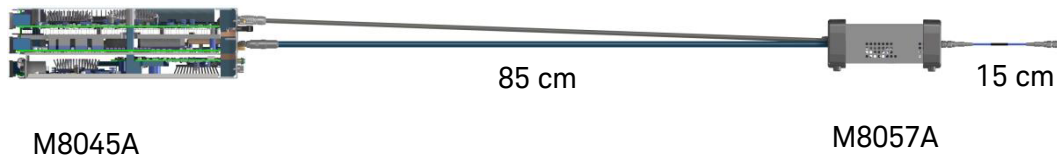
Table 26. General characteristics for M8045A and M8046A modules.

	M8045A	M8046A
Operating temperature	5 to 40 °C (41 to + 104 °F)	
Storage temperature	-40 to +70 °C (modules) (-40 to + 158 °F)	
Operating humidity	15 to 95% relative humidity at 40°C (non-condensing)	
Storage humidity	24 to 90% relative humidity at 65°C (non-condensing)	
Power requirements (module only)	Single channel: 515 W Dual channel: 605 W	238 W
Physical dimensions for modules (W x H x D)	3-slot AXIe module: 351 x 92 x 315 mm\ (13.8 x 3.6 x 12.4 inch)	1-slot AXIe module: 351 x 30 x 309 mm (13.8 x 1.8 x 12.2 inch)
Physical dimensions for M8040A-BU1/-BU2 (W x H x D)	Installed in 5-slot AXIe chassis: 462 x 193 x 446 mm (18.2 x 7.6 x 17.6 inch)	
Weight net	M8045A module: single channel 6.9 kg (15.2 lb) M8045A dual channel: 7.5 kg (16.5 lb) With M8040A-BU1: 25 kg (55 lb) With M8040A-BU2: 21 kg (46.3 lb)	M8046A module: 3.6 kg (8.0 lb) In bundle with M8045A and in a 5-slot chassis: 24.6 kg (54.3 lb)
Weight shipping	M8045A module: With M8040A-BU1: 37 kg (82 lb) With M8040A-BU2: 33 kg (73 lb)	Tbd In bundle with M8045A and in a 5-slot chassis: 37.6 kg (83 lb)
Recommended recalibration period	1 year	
Warranty period	3 years return to Keysight	
Warm-up time	30 minutes	
Cooling requirements	Slot air flow direction is from right to left. When operating the M8045A /46A choose a location that provides at least 50 mm of clearance at each side. See also start-up guide for M9505A chassis.	
EMC	IEC 61326-1	
Safety	IEC 61010-1	
Quality management	ISO 9001, 14001	

Remote head M8057A

Table 27. General characteristics for M8057A remote head.

	M8057A
Operating temperature	5 to 40 °C (41 to + 104 °F)
Storage temperature	-40 to +70 °C (modules) (-40 to + 158 °F)
Operating humidity	15 to 95% relative humidity at 40 °C (non-condensing)
Storage humidity	24 to 90% relative humidity at 65 °C (non-condensing)
Physical dimensions (W x H x D)	Remote head 117 mm x 68 mm x 185 mm, (4.6" x 2.7" x 7.3")
Physical dimensions for remote head with cable	Length of cable connection between M8057A and M8045A module: 85 cm



Weight net	1.7 kg (3.75 lb)
Weight shipping	6.5 kg (14.4 lb)
Recommended recalibration period	1 year
Warranty period	3 years return to Keysight
Warm-up time	30 minutes
EMC	IEC 61326-1

Specification assumptions

The specifications in this document describe the instruments' warranted performance. All specification in this revision of the data sheet are preliminary. Non-warranted values are described as typical. All specifications are valid in the specified operating temperature range after the warm-up time and after auto-adjustment. If not otherwise stated all outputs need to be terminated with 50 Ω to GND. All M8045A specifications if not otherwise stated are valid at the end of the cable M8045A-801.

All M8046A specifications if not otherwise stated are valid using the recommended cable pair N4910A (2.4 mm matched cable pair 24 inches).

Ordering of M8040A High-performance BERT 64 GBaud

The M8040A is scalable and upgradeable. The following table shows all available options. Upgrade options are shown below.

Description	Product #	Option	Comment
High-performance BERT 64 GBaud (systemizing number for factory pre-installation)	M8040A		
Pattern generator and clock module, 32/64 GBaud, 3-slot AXIe	M8045A		
Pattern generator one channel NRZ, data rate up to 32 GBaud (requires remote head, M8057A)	M8045A	G32	One of these is required
Pattern generator one channel NRZ, data rate up to 64 GBaud (requires remote head, M8057A)	M8045A	G64	
Second channel, hardware and license (requires remote head, M8057A)	M8045A	OG2	
Advanced jitter sources for receiver characterization, module-wide license	M8045A	OG3	
De-emphasis, module-wide license	M8045A	OG4	
PAM-4 encoding up to 32GBaud, module-wide license	M8045A	OP3	
Extension to PAM-4 encoding up to 64GBaud, module-wide license	M8045A	OP6	Only with G64
Short cable 1.85 mm (m) to 1.85 mm (m), 0.15 m, absolute matching 699 ps ± 1 ps	M8045A	801	Qty 2 recommended
Remote head for M8045A pattern generator, 1 channel	M8057A		
Analyzer module, 32/64 GBaud, 1-slot AXIe	M8046A		
Analyzer, one channel, data rate up to 32 GBaud, NRZ	M8046A	A32	
PAM-4 decoding up to 32 GBaud, license	M8046A	OP3	
Cable 2.92 mm (m) to 2.92 mm (m), 0.5 m for clock input	M8046A	801	Qty 1 recommended
Software and chassis			
System software for M8000 Series (transportable perpetual or network license)	M8070A	OTP/ONP	
DUT control interface (transportable perpetual or network license)	M8070A	1TP/OTP	
5-slot AXIe chassis with USB option	M8040A	BU2	
5-slot AXIe chassis with USB option and embedded controller M9536A	M8040A	BU1	
Warranty, calibration and productivity services			see next page

Figure 16. Overview of possible M8040A configurations

Description	Product #	Option	Comment
Upgrades for M8040A High-performance BERT 64 GBaud	M8040AU		
Pattern generator and clock module, 32/64 GBaud, 3-slot AXIe	M8045A		
Upgrade to 64 GBaud (requires remote head, M8057A)	M8045A	U64	License
Upgrade to second channel, hardware and license (requires remote head, M8057A)	M8045A	UG2	Requires return-to-factory
Upgrade to advanced jitter sources for receiver characterization, module-wide license	M8045A	UG3	License
Upgrade to de-emphasis, module-wide license	M8045A	UG4	License
Upgrade to PAM-4 encoding up to 32 GBaud, module-wide license	M8045A	UP3	License
Upgrade to extension to PAM-4 encoding up to 64 GBaud, module-wide license	M8045A	UP6	Only with G64/U64
Remote head for M8045A pattern generator, 1 channel	M8057A		
Analyzer module, 32/64 GBaud, 1-slot AXIe	M8046A		
Upgrade to PAM-4 decoding up to 32 GBaud, license	M8046A	UP3	License

Figure 17. All upgrade options for M8040A are orderable under M8040AU. Most options are license options, that can be upgraded on site.

Default accessories included with shipment

M8045A module:

Four 50 Ω resistors, ESD protection kit, certificate of calibration, license entitlement certificate, no signal cables, no blue sync cable

M8046A module:

ESD protection kit, certificate of calibration, license entitlement certificate, no signal cables

M8057A remote head:

includes cable connection to M8045A pattern generator module, one 50 Ω termination (2.4 mm)

M8040A-BU1:

M9505A AXIe chassis with embedded controller, USB cable, getting started guide, AXIe filler panel, power cord

M8040A-BU2:

M9505A AXIe chassis, USB cable, getting started guide, AXIe filler panel, power cord

M8070A:

CD-ROM with M8070A system software

Recommended accessories

Short cable, 1.85 mm (m) to 1.85 mm (m), 0.15 m, 699 ps delay \pm 1 ps (two are recommended for each differential data output of M8057A)	M8045A-801
Matched cable pair 2.4 mm (m) to (m) (recommended for data input of M8046A analyzer)	N4910A
Cable 2.92 mm (m) to 2.92 mm (m), 0.5 m (recommended for clock input of M8046A analyzer)	M8046A-801
M8000 sync cable (when using the system clock of M8045A for M8046A)	M8051A-801
Attenuator, 6 dB, 1.85 mm	8490G-006
DC block 2.4 mm	N9398F
Rack-mount kit for AXIe 5-slot chassis M9505A	Y1226A

Warranty, calibration and productivity services

Extended 5 year warranty Return-to-Keysight	R1280 (R-51B-001-5Z)
Calibration services (3 and 5 years)	R1282 (R50C-001-3/-5)
Productivity assistance	R1380-M8000

Related Keysight literature

Data sheets and configuration guides

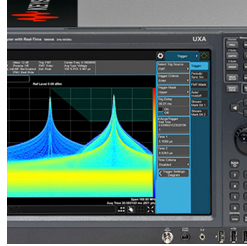
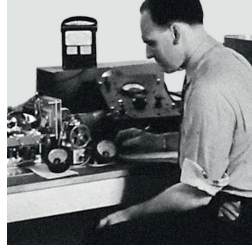
<i>J-BERT M8020A, Data Sheet</i>	5991-3647EN
<i>M8030A Multi-channel BERT, Data Sheet</i>	5992-1287EN
<i>M8062A 32 Gb/s Front-end, Data Sheet</i>	5992-0987EN
<i>N4877A and N1075A CDR/Demux, Data Sheet</i>	5990-9949EN
<i>M9505A AXIe Chassis 5-slot, Data Sheet</i>	5990-6584EN
<i>M8196A 92 GSa/s AWG, Data Sheet</i>	5992-0971EN
<i>N1085A PAM-4 Measurement Application for 86100D DCA-X Series, Data Sheet</i>	5992-1248EN
<i>N1076A/N1077A Clock recovery, Data Sheet</i>	5992-1620EN

Application notes

<i>Characterizing and verifying compliance of 100Gb Ethernet components and systems, Application Note</i>	5992-0019EN
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