

**FEATURES**

- InGaP HBT Technology
- High Efficiency:
  - 37 % @ P<sub>OUT</sub> = +28 dBm
  - 20 % @ P<sub>OUT</sub> = +16 dBm
  - 10 % @ P<sub>OUT</sub> = +10 dBm
- Low Quiescent Current: 4 mA
- Internal Voltage Regulation
- Built-in Directional Coupler
- Common V<sub>MODE</sub> Control Line
- Suitable for SMPS and average power tracking systems with variable supply voltages
- APT can reduce TS.09 average power consumption more than 25%
- Reduced External Component Count
- Thin Package: 0.9 mm
- RoHS Compliant Package, 260 °C MSL-3

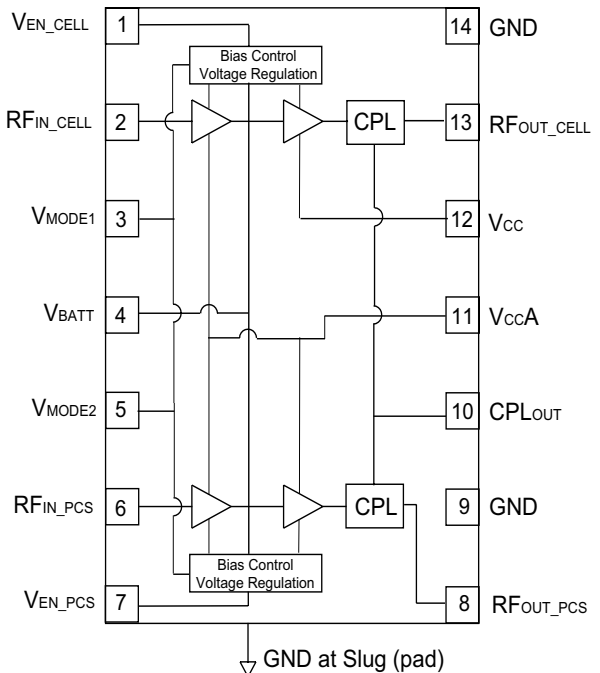
**APPLICATIONS**

- Dual-band Wireless Handsets and Data Devices for CDMA/EVDO networks:
  - Cellular BC 0 and 10
  - PCS BC 1 and 14

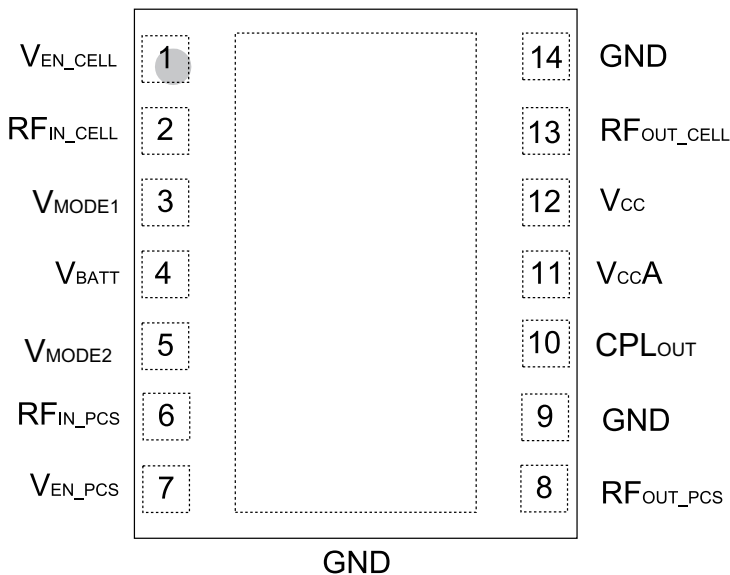
**PRODUCT DESCRIPTION**

AWC6325 addresses the demand for increased integration in dual-band handsets for CDMA networks. The small footprint 3 mm x 5 mm x 0.9 mm surface mount RoHS compliant package contains independent RF PA paths to ensure optimal performance in both frequency bands in less board area than two single band PAs. The package pinout was chosen to enable handset manufacturers to independently provide bias to both power amplifiers and simplify control with common mode pins. The AWC6325 is part of ANADIGICS' 3rd generation of High-Efficiency-at-Low-Power (HELP3E™) family of power amplifiers, which deliver low quiescent currents and significantly greater efficiency through selectable bias modes for high, medium and low power operation. The AWC6325 is designed for use both with and without average power tracking (APT). APT can be used to optimize the V<sub>cc</sub> level for the desired output power level

and linearity, which greatly reduces the total current drawn from the battery. This feature, in conjunction with selectable operating modes, enables significant improvements in overall power added efficiency of the AWC6325 across the entire dynamic range of operating powers. APT requires use of an external variable voltage supply (DC-DC converter), which is used to provide the variable voltage to V<sub>cc</sub> pad of the amplifier. A low-leakage shutdown mode increases standby time. This PA has built-in directional couplers for each band, with a common coupler output port CPL\_OUT. The 3 mm x 5 mm x 0.9 mm surface mount package incorporates matching networks optimized for output power, efficiency and linearity in a 50 Ω system. The device is manufactured on an advanced InGaP HBT MMIC technology offering state-of-the-art reliability, temperature stability, and ruggedness.



**Figure 1: Block Diagram**



**Figure 2: Pinout**

**Table 1: Pin Description**

PIN	NAME	DESCRIPTION
1	$V_{EN\_CELL}$	Enable Voltage for Cell Band
2	$RF_{IN\_CELL}$	RF Input for Cell Band
3	$V_{MODE1}$	Mode Control Voltage 1
4	$V_{BATT}$	Battery Voltage
5	$V_{MODE2}$	Mode Control Voltage 2
6	$RF_{IN\_PCS}$	RF Input for PCS Band
7	$V_{EN\_PCS}$	Enable Voltage for PCS Band
8	$RF_{OUT\_PCS}$	RF Output for PCS Band
9	GND	Ground
10	$CPL_{OUT}$	Coupler Output Port
11	$V_{CCA}$	Supply Voltage A
12	$V_{CC}$	Supply Voltage
13	$RF_{OUT\_CELL}$	RF Output for Cell Band
14	GND	Ground

## ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage ( $V_{BATT}$ , $V_{CC}$ , $V_{CCA}$ )	0	+5	V
Mode Control Voltage ( $V_{MODE1,2}$ , $V_{EN}$ )	0	+3.5	V
RF Input Power ( $P_{IN}$ )	-	+10	dBm
Storage Temperature ( $T_{STG}$ )	-40	+150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
Operating Frequency (f)	814 1850	- -	849 1915	MHz	Cellular BC0 & 10 PCS BC1 & 14
Supply Voltage ( $V_{CC}$ , $V_{CCA}$ )	+0.8	+3.4	+4.35	V	
Battery Voltage ( $V_{BATT}$ )	+3.2	+3.4	+4.35	V	
Enable Voltage ( $V_{EN\_CELL}$ , $V_{EN\_PCS}$ )	+1.35 0	+1.8 0	+3.1 +0.5	V	PA "on" PA "shut down"
Mode Control Voltage ( $V_{MODE1,2}$ )	+1.35 0	+1.8 0	+3.1 +0.5	V	Logic High Logic Low
Cellular RF Output Power CDMA CDMA, HPM CDMA, MPM CDMA, LPM	27.5 <sup>(1)</sup> - -	28.0 16.0 10.0	- - -	dBm	CDMA 2000, RC-1
PCS RF Output Power CDMA CDMA, HPM CDMA, MPM CDMA, LPM	27.5 <sup>(1)</sup> - -	28.0 16.0 10.0	- - -	dBm	CDMA 2000, RC-1
Case Temperature ( $T_C$ )	-30	-	+90	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

## Notes:

(1) For operation at  $V_{CC} = +3.2$  V,  $P_{OUT}$  is derated by 0.5 dB.

**Table 4: Electrical Specifications - Cellular Band (BC 0, 10)**

(T<sub>C</sub> = +25 °C, V<sub>BATT</sub> = V<sub>CC</sub> = +3.4 V, V<sub>EN\_CELL</sub> = +1.8 V, 50 Ω system, CDMA2000 RC-1 waveform)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P <sub>OUT</sub>	V <sub>MODE1</sub>	V <sub>MODE2</sub>
Gain	25 14 7	28 17 12	31 19 14	dB	+28 dBm +16 dBm +10 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Adjacent Channel Power at ± 885 kHz offset <sup>(1)</sup> Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	- - -	-48.5 -52 -53.5	-46.5 -46.5 -46.5	dBc	+28 dBm +16 dBm +10 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Adjacent Channel Power at ± 1.98 MHz offset <sup>(1)</sup> Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	- - -	-58 -59 -68	-56 -56 -56	dBc	+28 dBm +16 dBm +10 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Power-Added Efficiency <sup>(1)</sup>	- - -	37.5 19.5 10	- - -	%	+28 dBm +16 dBm +10 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Quiescent Current (I <sub>q</sub> )	-	4	-	mA	through V <sub>CC</sub> pins, V <sub>MODE1,2</sub> = +1.8 V		
Mode Control Current	-	0.5	-	mA	through V <sub>MODE</sub> pin, V <sub>MODE1,2</sub> = +1.8 V		
BATT Current	-	1.5	-	mA	through V <sub>BATT</sub> pin, V <sub>MODE1,2</sub> = +1.8 V		
Enable Current	-	0.3	-	mA	through V <sub>EN_CELL</sub> pin, V <sub>MODE1,2</sub> = +1.8 V		
Total Decoder Current on V <sub>BATT</sub> (in Shutdown mode)	-	7	-	μA	V <sub>BATT</sub> = +4.35 V, V <sub>CC</sub> = +4.35 V, V <sub>EN_CELL</sub> = 0 V, V <sub>MODE1,2</sub> = 0 V		
HBT Leakage Current (V <sub>CC</sub> ) (Shutdown mode)	-	<1	-	μA	V <sub>BATT</sub> = +4.35 V, V <sub>CC</sub> = +4.35 V, V <sub>EN_CELL</sub> = 0 V, V <sub>MODE1,2</sub> = 0 V		
Noise In Receive Band	-	-133	-	dBm/Hz	869 MHz to 894 MHz		
Harmonics 2f <sub>o</sub> 3f <sub>o</sub> , 4f <sub>o</sub>	- - -	- - -	-35 -35	dBc	P <sub>OUT</sub> ≤ +28 dBm		
Input Impedence	-	2.5:1	-	VSWR			
Coupling Factor	-	22	-	dB			
Spurious Output Level (all spurious outputs)	-	-	-65	dBc	P <sub>OUT</sub> ≤ +28 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range		

Notes:

(1) PAE and ACP measured at 836.5 MHz.

**Table 5: Electrical Specifications - PCS Band (BC 1, 14)**  
 (T<sub>C</sub> = +25 °C, V<sub>BATT</sub> = V<sub>CC</sub> = +3.4 V, V<sub>EN\_PCS</sub> = +1.8 V, 50 Ω system, CDMA2000 RC-1 waveform)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS		
					P <sub>OUT</sub>	V <sub>MODE1</sub>	V <sub>MODE2</sub>
Gain	24 10 7	26.5 13 9	30 16 12	dB	+28 dBm +16 dBm +10 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Adjacent Channel Power at ± 1.25 MHz offset <sup>(1)</sup> Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	- - -	-48 -52.5 -53	-46.5 -46.5 -46.5	dBc	+28 dBm +16 dBm +10 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Adjacent Channel Power at ± 1.98 MHz offset <sup>(1)</sup> Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	- - -	-55 -60 -63	-54 -54 -54	dBc	+28 dBm +16 dBm +10 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Adjacent Channel Power at ± 2.25 MHz offset <sup>(1)</sup> Primary Channel BW = 1.23 MHz Adjacent Channel BW = 30 kHz	- - -	-59.5 -63.5 -67.5	-56.5 -57 -57	dBc	+28 dBm +16 dBm +10 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Power-Added Efficiency <sup>(1)</sup>	- - -	37 20 10	- - -	%	+28 dBm +16 dBm +10 dBm	0 V 1.8 V 1.8 V	0 V 0 V 1.8 V
Quiescent Current (I <sub>cq</sub> )	-	4	-	mA	through V <sub>CC</sub> pins, V <sub>MODE1,2</sub> = +1.8 V		
Mode Control Current	-	0.5	-	mA	through V <sub>MODE</sub> pin, V <sub>MODE1,2</sub> = +1.8 V		
BATT Current	-	1.5	-	mA	through V <sub>BATT</sub> pin, V <sub>MODE1,2</sub> = +1.8V		
Enable Current	-	0.3	-	mA	through V <sub>EN_PCS</sub> pin, V <sub>MODE1,2</sub> = +1.8 V		
Total Decoder Current on V <sub>BATT</sub> (in Shutdown mode)	-	7	-	μA	V <sub>BATT</sub> = +4.35 V, V <sub>CC</sub> = +4.35 V, V <sub>EN_CELL</sub> = 0 V, V <sub>MODE1,2</sub> = 0 V		
HBT Leakage Current on V <sub>CC</sub> (in Shutdown mode)	-	<1	-	μA	V <sub>BATT</sub> = +4.35 V, V <sub>CC</sub> = +4.35 V, V <sub>EN_CELL</sub> = 0 V, V <sub>MODE1,2</sub> = 0 V		
Noise In Receive Band	-	-133	-	dBm/Hz	1930 MHz to 1990 MHz		
Harmonics 2f <sub>o</sub> 3f <sub>o</sub> , 4f <sub>o</sub>	- - -	- - -	-30 -30	dBc	P <sub>OUT</sub> ≤ +28 dBm		
Input Impedence	-	-	2:1	VSWR			
Coupling Factor	-	22	-	dB			
Spurious Output Level (all spurious outputs)	-	-	-65	dBc	P <sub>OUT</sub> ≤ +28 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating conditions		
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range		

Notes:

(1) ACPRs and Efficiency measured at 1880 MHz.

## APPLICATION INFORMATION

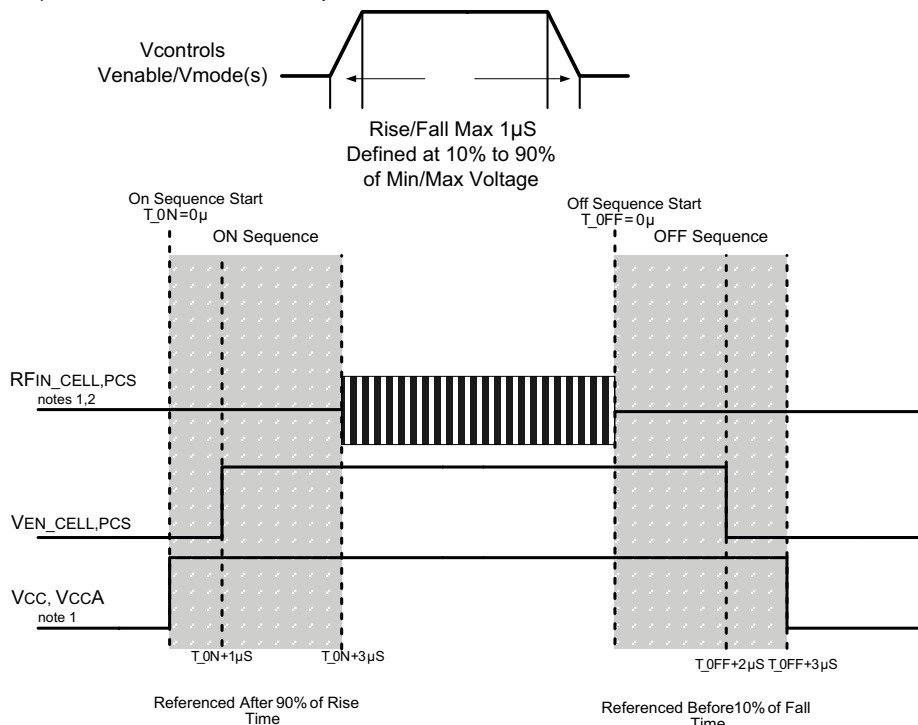
To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site: <http://www.anadigics.com>

### Shutdown Mode

The power amplifier may be placed in a shutdown mode by applying logic low levels (see Operating Ranges table) to the  $V_{ENABLE}$  and  $V_{MODE}$  pads.

### Bias Modes

The power amplifier may be placed in Low, Medium, or High Bias modes by applying the appropriate logic level (see Operating Ranges table) to the  $V_{MODE}$  pin. The Bias Control table lists the recommended modes of operation for various applications.



**Figure 3: Recommended ON/OFF Timing Sequence**

Notes:

- (1) Level might be changed after RF is ON.
- (2) RF OFF defined as  $P_{IN} \leq -30$  dBm.
- (3) Switching simultaneously between  $V_{MODE}$  and  $V_{EN}$  is not recommended.

**Table 6: Bias Control**

APPLICATION	POUT LEVELS	BIAS MODE	$V_{EN\_CELL}$ $V_{EN\_PCS}$	$V_{MODE1}$	$V_{MODE2}$	$V_{CC}$	$V_{BATT}$
Low Bias Mode	< +10 dBm	Low	+1.8 V	+1.8 V	+1.8 V	0.8 - 4.35 V	> 3.2 V
Medium Bias Mode	> +10 dBm < +16 dBm	Medium	+1.8 V	+1.8 V	0 V	0.8 - 4.35 V	> 3.2 V
High Bias Mode	> +16 dBm	High	+1.8 V	0 V	0 V	1.3 - 4.35 V	> 3.2 V
Shutdown	-	Shutdown	0 V	0 V	0 V	3.2 - 4.35 V	>3.2 V

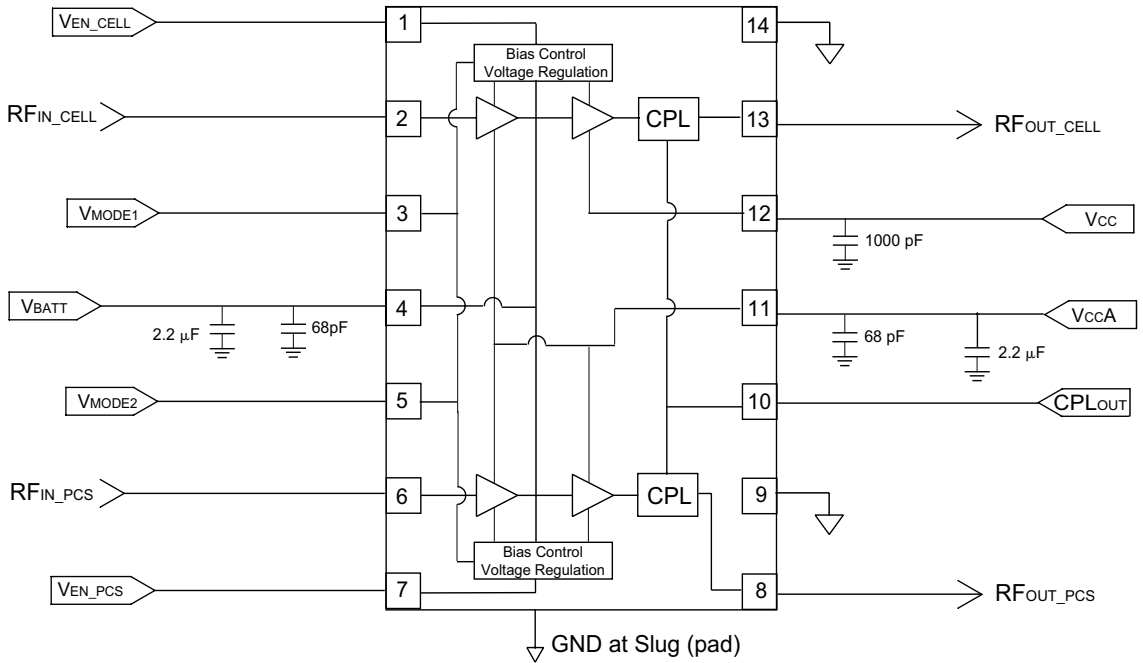
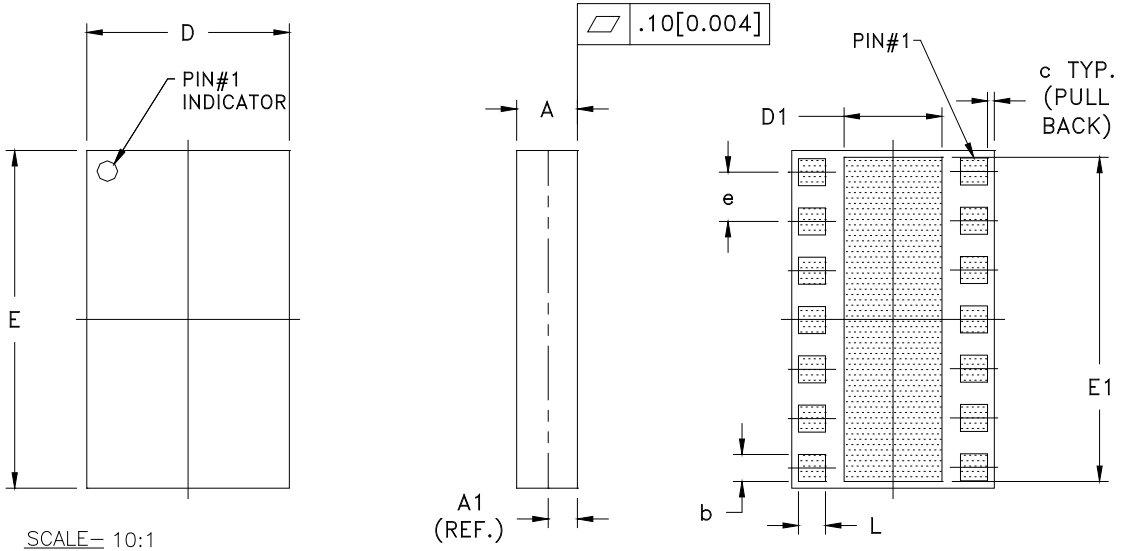


Figure 4: Application Circuit

PACKAGE OUTLINE



SCALE= 10:1

SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.85	0.90	0.95	0.033	0.035	0.037	-
A1	PLEASE REFER TO LAMINATE CONTROL DRAWING						-
b	0.32	0.37	0.41	0.013	0.015	0.016	3
c	-	0.10	-	-	0.004	-	-
D	2.88	3.00	3.12	0.113	0.118	0.123	-
D1	1.45	1.50	1.57	0.057	0.059	0.062	3
E	4.88	5.00	5.12	0.192	0.197	0.202	-
E1	4.70	4.75	4.80	0.185	0.187	0.189	3
e	-	0.73	-	-	0.029	-	4
L	0.32	0.37	0.41	0.013	0.015	0.016	3

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.
4. PITCH MEASUREMENT (e) TAKEN CENTERLINE TO CENTERLINE OF SOLDER MASK OPENINGS.
5. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.

Figure 5: Package Outline - 14 Pin 3 mm x 5 mm x 0.9 mm Surface Mount Module

TOP BRAND

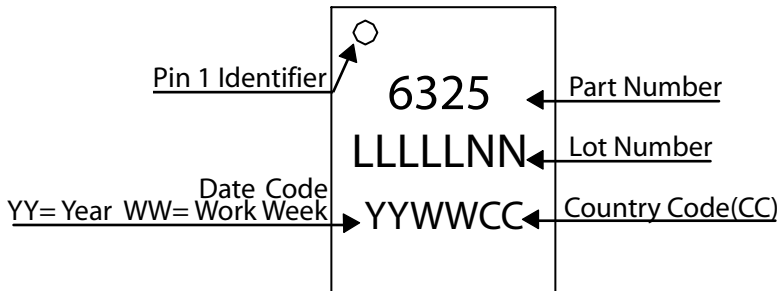


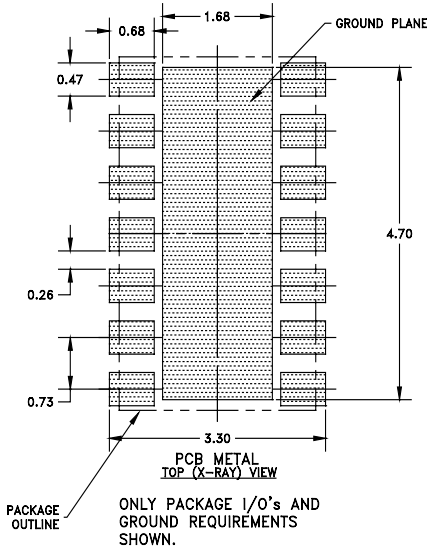
Figure 6: Branding Specification

**PCB BOARD DESIGN GUIDELINES**

Refer to Figure 7 for the recommended PCB metal design, soldermask design, and stencil print patterns when assembling with ANADIGICS modules.

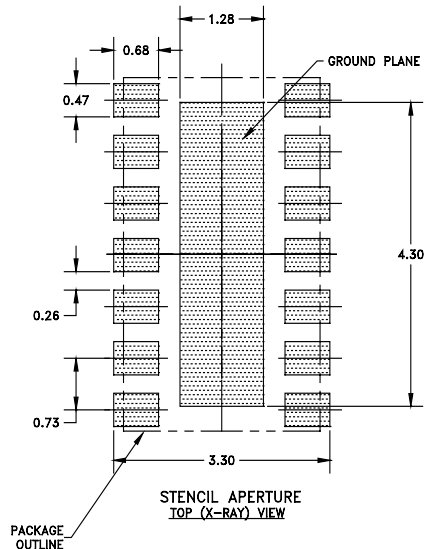
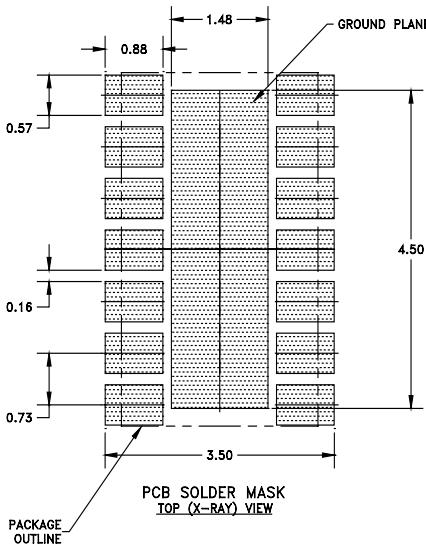
It is important to note that the PCB metal design is dependent upon several factors: the electrical and thermal performance requirements of the product,

and the PCB-to-device interconnect pattern. The PCB metal design recommendations primarily deal with the PCB-to-device interconnection. Specific board-level electrical and thermal performance requirements will be dictated by the physical geometry of the specific application and are the responsibility of the end product manufacturer.



**NOTES:**

- (1) OUTLINE DRAWING REFERENCE: P8002519
- (2) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
- (3) DIMENSIONS IN MILLIMETERS.



**Figure 7: PCB Board Design Guidelines**

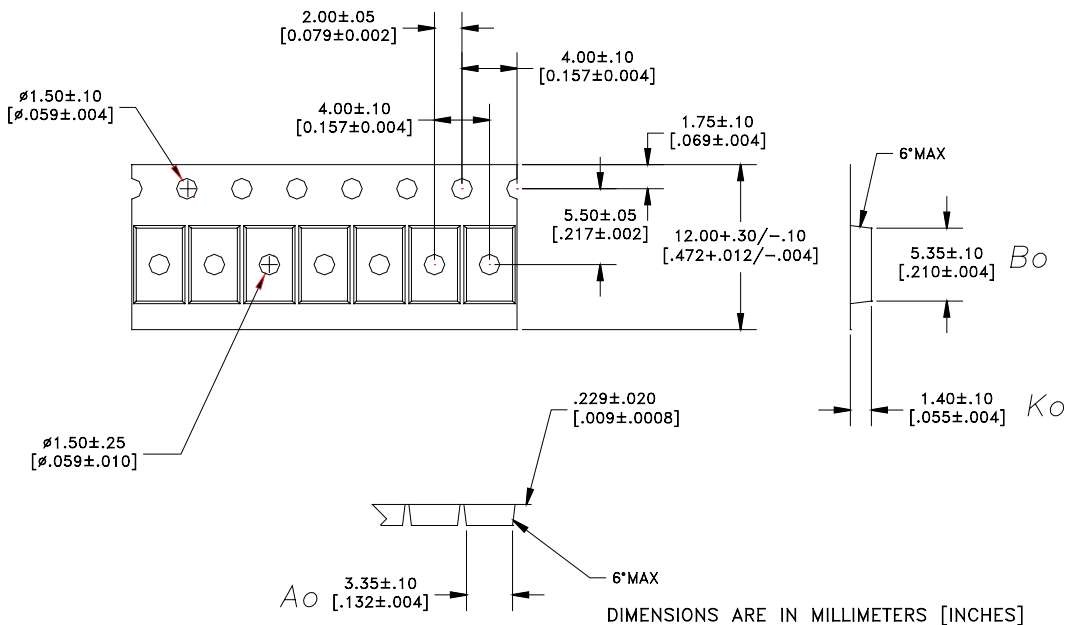
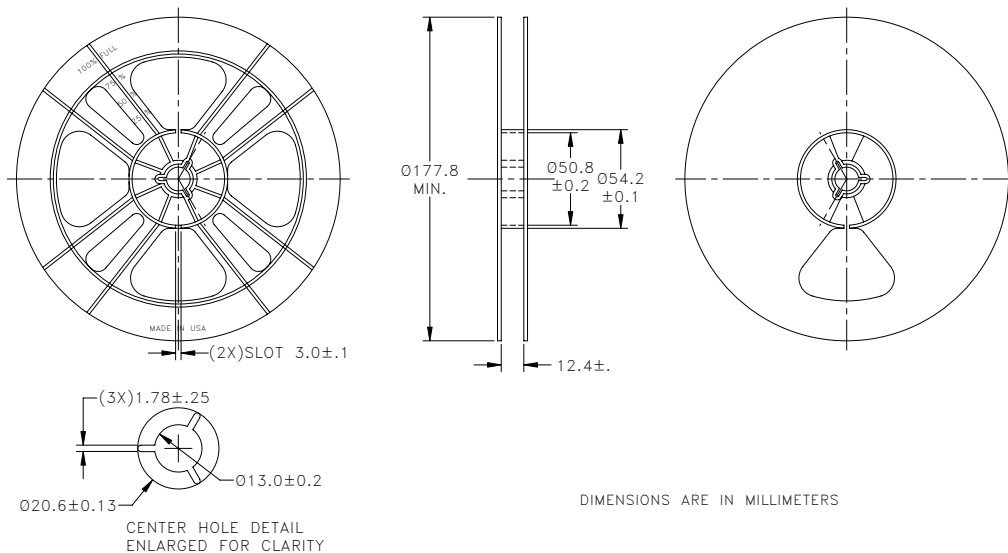


Figure 8: Carrier Tape Drawing



- NOTES:  
 1. MATERIAL: BLACK CARBON POLYSTYRENE  
 SURFACE RESISTIVITY: 1X10<sup>4</sup> TO 1X10<sup>5</sup> ohms/square

DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

Figure 9: Reel Drawing

**ORDERING INFORMATION**

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AWC6325Q7	-30 °C to +90 °C	RoHS Compliant 14 Pin 3 mm x 5 mm x 0.9 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
AWC6325P9	-30 °C to +90 °C	RoHS Compliant 14 Pin 3 mm x 5 mm x 0.9 mm Surface Mount Module	Partial Tape and Reel

**ANADIGICS, Inc.**

141 Mount Bethel Road  
Warren, New Jersey 07059, U.S.A.

Tel: +1 (908) 668-5000

Fax: +1 (908) 668-5132

URL: <http://www.anadigics.com>

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