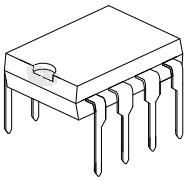
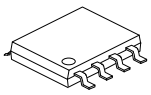
GM1851

LINEAR INTEGRATED CIRCUIT

GROUND FAULT INTERRUPTER



DIP-8



SOP-8

Lead-free: GM1851L
Halogen-free: GM1851G

■ DESCRIPTION

The UTC **GM1851** can specially provide ground fault protection for AC power outlets in consumer and industrial environments. As ground fault currents greater than a presentable threshold value, it will trigger an external SCR-driven circuit breaker to interrupt the AC line and remove the fault condition. Besides of detection of conventional hot wire to ground faults, the neutral fault condition is detected also. In the event that noise pulses introduce unwanted charging currents and a memory circuit that allows firing of even a sluggish breaker on either half-cycle of the line voltage when external full-wave rectification is used, circuitry that rapidly resets the timing capacitor.

■ FEATURES

* Internal power supply shunt regulator
* Externally programmable fault current threshold
* Externally programmable fault current integration time
* Direct interface to SCR
* Operates under line reversal; both load vs line and hot vs neutral
* Detects neutral line faults

■ ORDERING INFORMATION

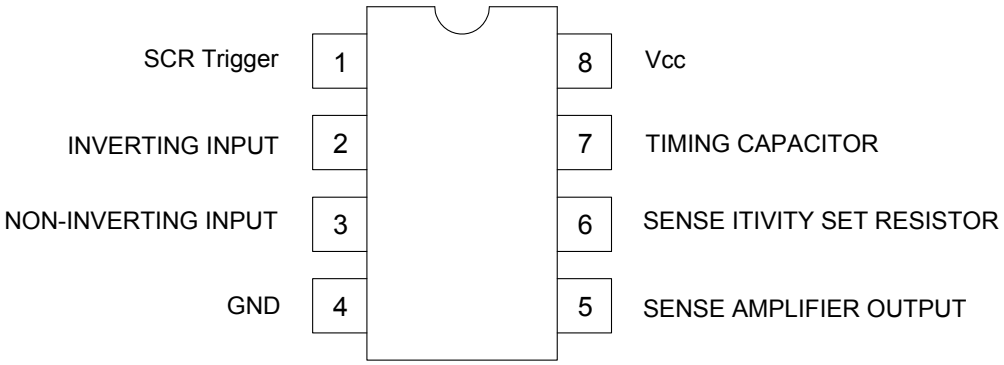
Ordering Number			Package	Packing
Normal	Lead Free	Halogen Free		
GM1851-S08-R	GM1851L-S08-R	GM1851G-S08-R	SOP-8	Tape Reel
GM1851-D08-T	GM1851L-D08-T	GM1851G-D08-T	DIP-8	Tube

GM1851L-S08-R
(1)Packing Type
(2)Package Type
(3)Lead Plating

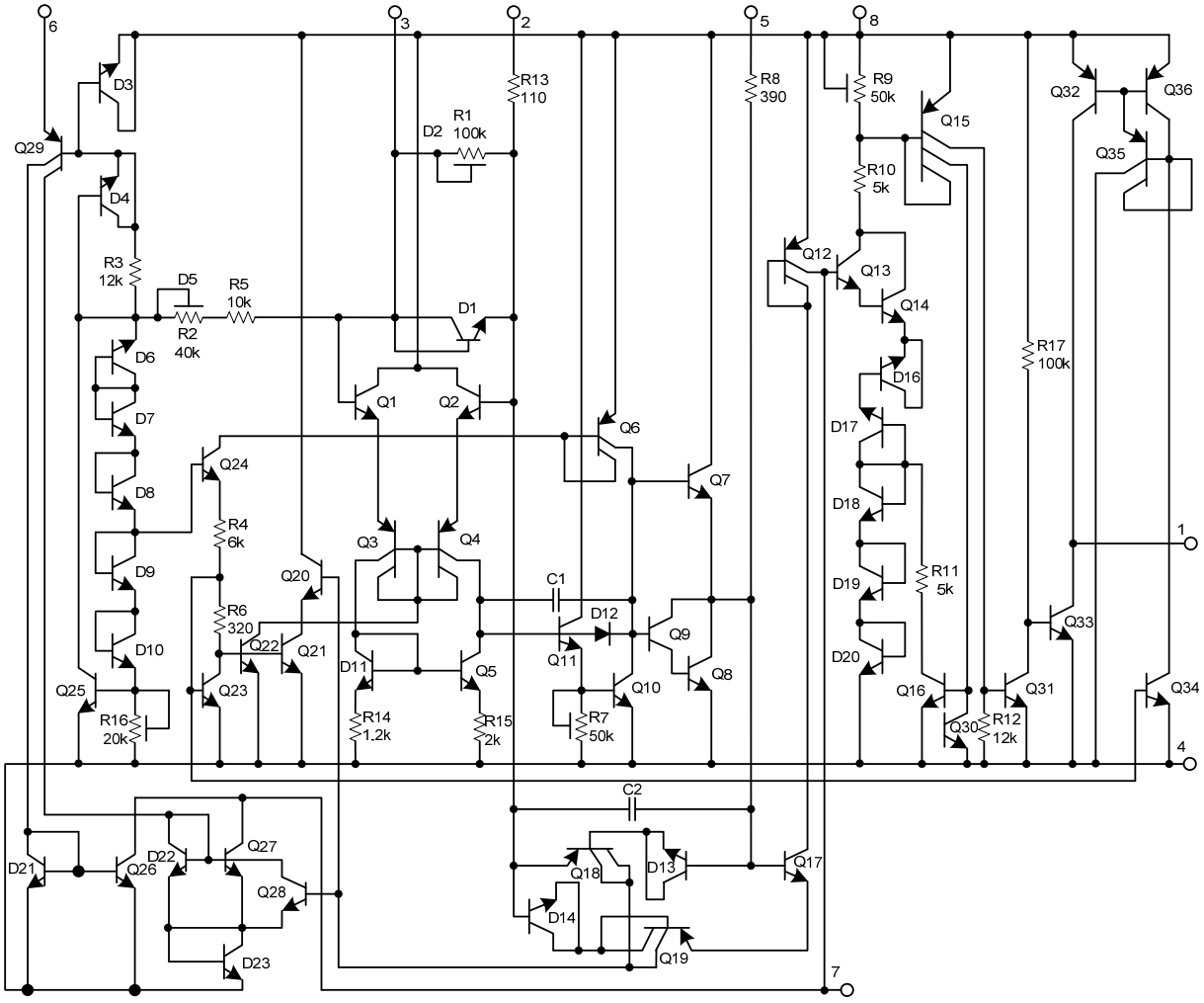
(1) T: Tube, R: Tape Reel
(2) D08: DIP-8, S08: SOP-8
(3) G: Halogen Free, L: Lead Free, Blank: Pb/Sn

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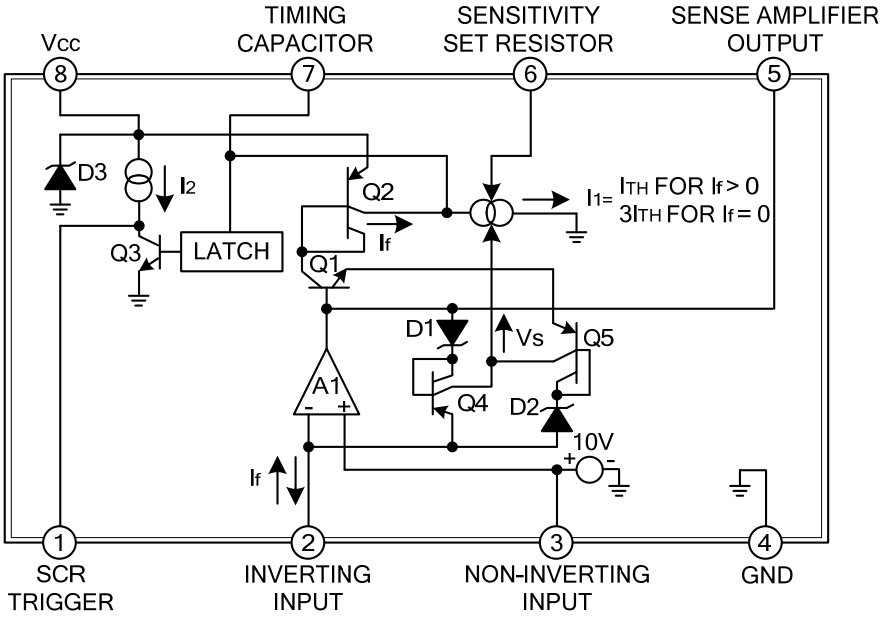
■ PIN CONFIGURATION



■ INTERNAL SCHEMATIC DIAGRAM



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Current	I_{CC}	19	mA
Power Dissipation (Note 1)	P_D	1250	mW
Operating Temperature	T_{OPR}	-40 ~ +70	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (T_a=25°C, I_{SS}=5mA)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS					
Power Supply Shunt Regulator Voltage	Pin 8, Average Value	22	26	30	V
Latch Trigger Voltage	Pin 7	15	17.5	20	V
Sensitivity Set Voltage	Pin 8 to Pin 6	6	7	8.2	V
Output Saturation Voltage	Pin 1, Without Fault		100	240	mV
Output Drive Current	Pin 1, With Fault	0.5	1	2.4	mA
Output External Current Sinking Capability	Pin 1, Without Fault Vpin 1 Held to 0.3V (Note 4)	2.0	5		mA
Output Saturation Resistance	Pin 1, Without Fault		100		Ω
Noise Integration Sink Current Ratio	Pin 7, Ratio of Discharge Currents Between No Fault and Fault Conditions	2.0	2.8	3.6	μA/μA
AC CHARACTERISTICS					
Normal Fault Current Sensitivity	Figure 1 (Note 3)	3	5	7	mA
Normal Fault Trip Time	500Ω Fault, Figure 2 (Note 2)		18		mS
Normal Fault with Grounded Neutral Fault Trip Time	500Ω Normal Fault, 2Ω Neutral, Figure 2 (Note 2)		18		mS

Note: 1. For operation in ambient temperatures above 25℃, the device must be debated based on a 125℃ maximum junction temperature and a thermal resistance of 80℃/W junction to ambient for the DIP and 162/W for the SO Package.
2. Average of 10 trials.
3. Required UL sensitivity tolerance is such that external trimming of UTC GM1851 sensitivity will be necessary.
4. This externally applied current is in addition to the internal "output drive current " source.

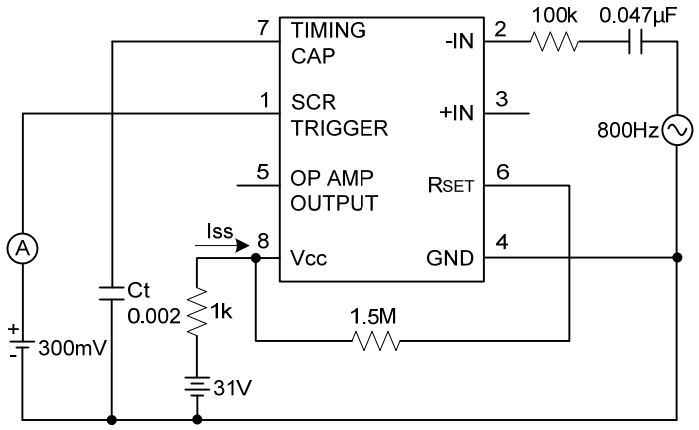


FIGURE 1.Normal Fault Sensitivity Test Circuit

■ CIRCUIT DESCRIPTION (Refer to Block and Connection Diagram)

The UTC **GM1851** operates from 26V as set by an internal shunt regulator, D3. In the absence of a fault (If=0) the feedback path status signal (VS) is correspondingly zero. Under these conditions the capacitor discharge current, I1, sits quiescently at three times its threshold value, ITH, so that noise induced charge on the timing capacitor will be rapidly removed. When a fault current, If, is induced in the secondary of the external sense transformer, the operational amplifier, A1, uses feedback to force a virtual ground at the input as it extracts If. The presence of If during either half-cycle will cause VS to go high, which in turn changes I1 from 3ITH to ITH. Although ITH discharges the timing capacitor during both half-cycles of the line, If only charges the capacitor during the half-cycle in which If exits pin 2. Thus during one half-cycle If-ITH charges the timing capacitor, while during the other half-cycle ITH discharges it. When the capacitor voltage reaches 17.5V, the latch engages and turns off Q3 permitting I2 to drive the gate of an SCR.

■ APPLICATION CIRCUITS

A typical ground fault interrupter circuit is shown in Figure 2. It is designed to operate on 120 VAC line voltage with 5 mA normal fault sensitivity.

A full-wave rectifier bridge and a 15k/2W resistor are used to supply the DC power required by the IC. A 1μF capacitor at pin 8 used to filter the ripple of the supply voltage and is also connected across the SCR to allow firing of the SCR on either half-cycle. When a fault causes the SCR to trigger, the circuit breaker is energized and line voltage is removed from the load. At this time no fault current flows and the IC discharge current increases from ITH to 3ITH (see Circuit Description and Block Diagram). This quickly resets both the timing capacitor and the output latch. At this time the circuit breaker can be reset and the line voltage again supplied to the load, assuming the fault has been removed. A 1000:1 sense transformer is used to detect the normal fault. The fault current, which is basically the difference current between the hot and neutral lines, is stepped down by 1000 and fed into the input pins of the operational amplifier through a 10μF capacitor. The 0.0033μF capacitor between pin 2 and pin 3 and the 200 pF between pins 3 and 4 are added to obtain better noise immunity. The normal fault sensitivity is determined by the timing capacitor discharging current, ITH. ITH can be calculated by:

$$I_{TH}=\frac{7V}{R_{SET}}\div 2 \qquad (1)$$

At the decision point, the average fault current just equals the threshold current, ITH.

$$I_{TH}=\frac{I_{f\,(rms)}}{2}\times 0.91 \qquad (2)$$

Where If(rms) is the rms input fault current to the operational amp and the factor of 2 is due to the fact that If charges the timing capacitor only during one half-cycle, while ITH discharges the capacitor continuously. The factor 0.91 converts the rms value to an average value. Combining equations (1) and (2) we have

$$R_{SET}=\frac{7V}{I_{f\,(rms)}\times 0.91} \qquad (3)$$

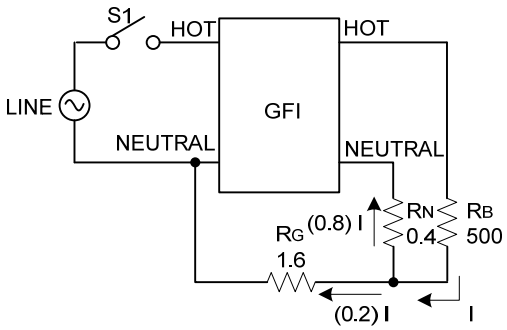
For example, to obtain 5mA (rms) sensitivity for the circuit in Figure 2 we have:

$$R_{SET}=\frac{7V}{\frac{5mA\times 0.91}{1000}}=1.5M\Omega \qquad (4)$$

The correct value for RSET can also be determined from the characteristic curve that plots equation (3). Note that this is an approximate calculation; the exact value of RSET depends on the specific sense transformer used and UTC **GM1851** tolerances. Inasmuch as UL943 specifies a sensitivity " window " of 4mA ~ 6mA, provision should be made to adjust RSET on a per-product basis.

Independent of setting sensitivity, the desired integration time can be obtained through proper selection of the timing capacitor, Ct. Due to the large number of variables involved, proper selection of Ct is best done empirically. The following design example, then should only be used as a guideline.

Assume the goal is to meet UL943 timing requirements. Also assume that worst-case timing occurs during GF1 Start-up (S1 closure) with both a heavy normal fault and a 2Ω grounded neutral fault present. This situation is shown diagrammatically below.



UL943 specifies ≤25 ms average trip time under these conditions. Calculation of C_t based upon charging currents due to normal fault only is as follows:

≤25 ms Specification

-3 ms GFI turn-on time (15k and 1μF)

-8 ms Potential loss of one half-cycle due to fault current sense of half-cycles only

-4 ms Time required to open a sluggish circuit breaker

≤10 ms Maximum integration time that could be allowed

8 ms Value of integration time that accommodates component tolerances and other variables

$$C_t = \frac{1 \times T}{V} \qquad (5)$$

Where T=integration time

V=threshold voltage

I=average fault current into C_t

$$I = \underbrace{\left(\frac{120V_{AC(rms)}}{R_B}\right)}_{\text{heavy fault current generated (swamps } I_{TH})} \times \underbrace{\left(\frac{R_N}{R_G + R_N}\right)}_{\text{portion of fault current shunted around GFI}} \times \underbrace{\left(\frac{1 \text{ turn}}{1000 \text{ turns}}\right)}_{\text{current division of input sense transformer}} \times \underbrace{\left(\frac{1}{2}\right)}_{\text{Ct charging on half-cycles only}} \times \underbrace{\left(0.91\right)}_{\text{rms to average conversion}} \qquad (6)$$

therefore:

$$C_t = \frac{\left[\left(\frac{120}{500}\right) \times \left(\frac{0.4}{1.6+0.4}\right) \times \left(\frac{1}{1000}\right) \times \left(\frac{1}{2}\right) \times \left(0.91\right)\right] \times 0.0008}{17.5} \qquad (7)$$

$$C_t = 0.01\,\mu F$$

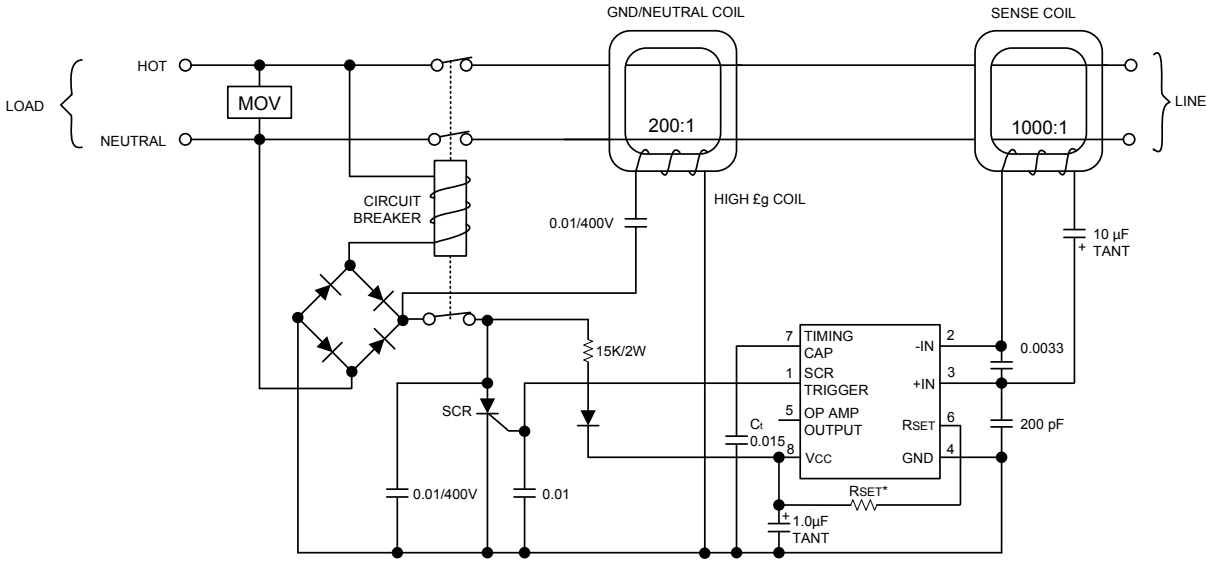
In practice, the actual value of C1 will have to be modified to include the effects of the neutral loop upon the net charging current. The effect of neutral loop induced currents is difficult to quartile, but typically they sum with normal fault currents, thus allowing a larger value of C1.

For UL943 requirements, 0.015μF has been found to be the best compromise between timing and noise.

For those GFI standards not requiring grounded neutral detection, a still larger value capacitor can be used and better noise immunity obtained. The larger capacitor can be accommodated because RN and RG are not present, allowing the full fault current, I, to enter the GFI.

In Figure 2, grounded neutral detection is accomplished by feeding the neutral coil with 120 Hz energy continuously and allowing some of the energy to couple into the sense transformer during conditions of neutral fault.

■ TYPICAL APPLICATION

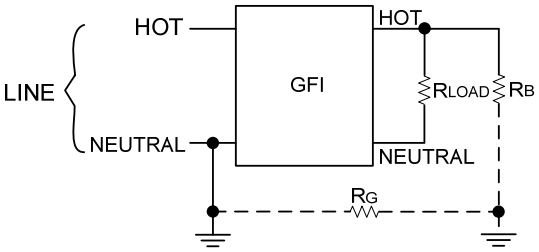


* Adjust R_{SET} for desired sensitivity

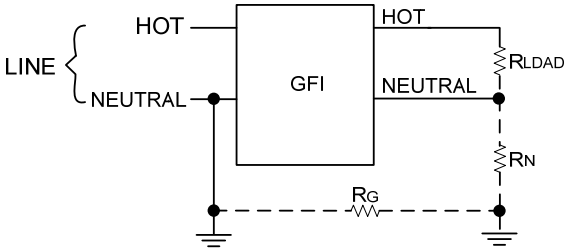
FIGURE 2. 120Hz Neutral Transformer Approach

■ DEFINITION OF TERMS

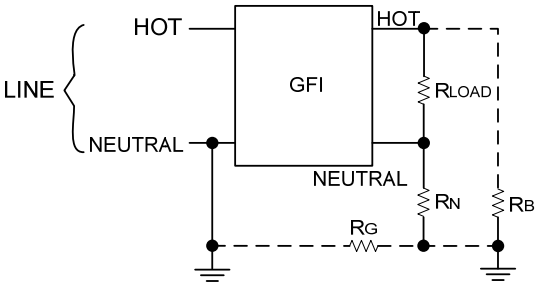
Normal Fault An unintentional electrical path , R_B, between the load terminal of the hot line and the ground, as shown by the dashed lines



Grounded Neutral Fault: An unintentional electrical path between the load terminal of the neutral line and the ground, as shown by the dashed lines.

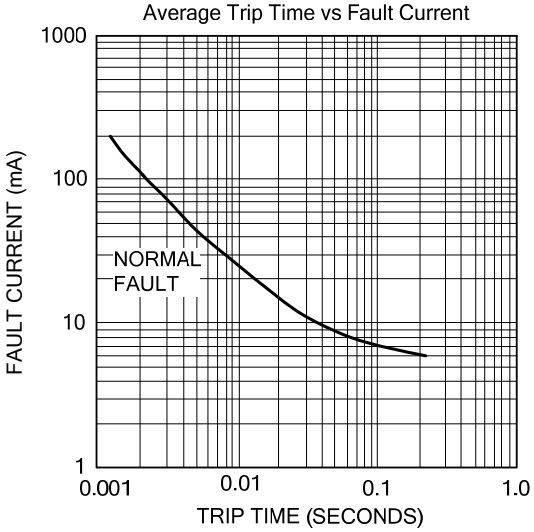


Normal Fault plus Grounded Neutral fault: The combination of the normal fault and the grounded neutral fault, as shown by the dashed lines.

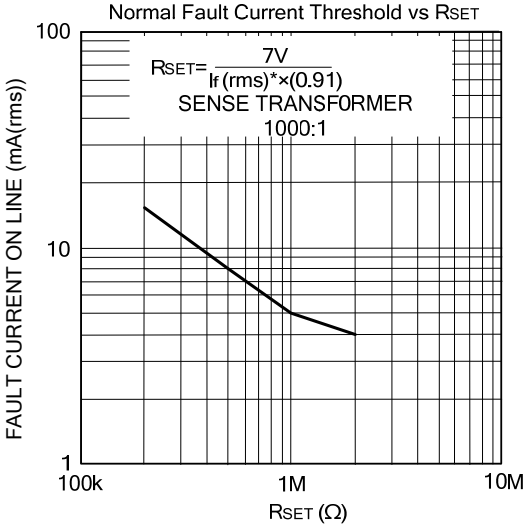


■ TYPICAL PERFORMANCE CHARACTERISTICS

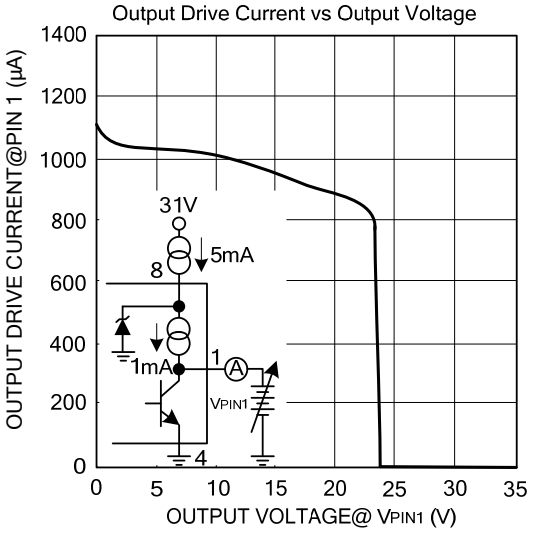
Average Trip Time vs Fault Current



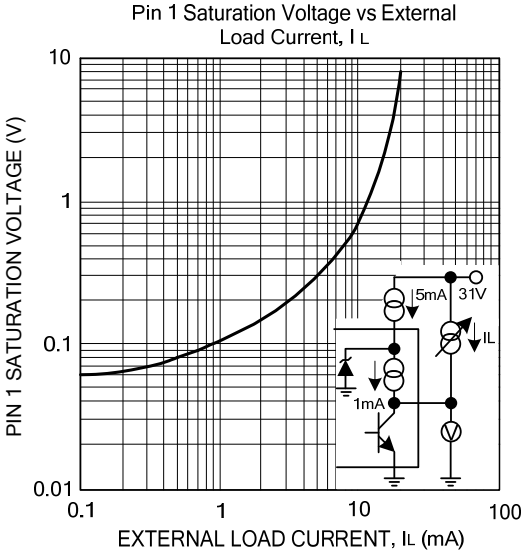
Normal Fault Current Threshold vs RSET



Output Drive Current vs Output Voltage



Pin 1 Saturation Voltage vs External Load Current, I L



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