24-Lane 6-Port Gen2 PCI Express® Switch

89HPES24T6G2
Data Sheet

Device Overview

The 89HPES24T6G2 is a member of IDT's PRECISE™ family of PCI Express® switching solutions. The PES24T6G2 is a 24-lane, 6-port Gen2 peripheral chip that performs PCI Express base switching with a feature set optimized for high performance applications such as servers, storage, and communications systems. It provides connectivity and switching functions between a PCI Express upstream port and up to five downstream ports and supports switching between downstream ports.

Features

- **High Performance PCI Express Switch**
  - *Twenty-four 5 Gbps Gen2 PCI Express lanes supporting 5 Gbps and 2.5 Gbps operation*
  - *Up to six switch ports*
  - *Support for Max Payload Size up to 2048 bytes*
  - *Supports one virtual channel and eight traffic classes*
  - *Fully compliant with PCI Express base specification Revision 2.0*
- **Flexible Architecture with Numerous Configuration Options**
  - *Automatic per port link width negotiation to x8, x4, x2, or x1*
  - *Automatic lane reversal on all ports*
  - *Automatic polarity inversion*
  - *Supports in-band hot-plug presence detect capability*
  - *Supports external signal for hot plug event notification allowing SCI/SMI generation for legacy operating systems*
  - *Dynamic link width reconfiguration for power/performance optimization*
  - *Configurable downstream port PCI-to-PCI bridge device numbering*
  - *Crosslink support*
  - *Supports ARI forwarding defined in the Alternative Routing-ID Interpretation (ARI) ECN for virtualized and non-virtualized environments*
  - *Ability to load device configuration from serial EEPROM*
- **Legacy Support**
  - *PCI compatible INTx emulation*
  - *Supports bus locked transactions, allowing use of PCI Express with legacy software*
- **Highly Integrated Solution**
  - *Requires no external components*
  - *Incorporates on-chip internal memory for packet buffering and queueing*
  - *Integrates twenty-four 5 Gbps / 2.5 Gbps embedded SerDes, 8B/10B encoder/decoder (no separate transceivers needed)*
- **Reliability, Availability, and Serviceability (RAS) Features**
  - *Ability to disable peer-to-peer communications*
  - *Supports ECRC and Advanced Error Reporting*
  - *All internal data and control RAMs are SECDED ECC protected*
  - *Supports PCI Express hot-plug on all downstream ports*
  - *Supports upstream port hot-plug*

Block Diagram

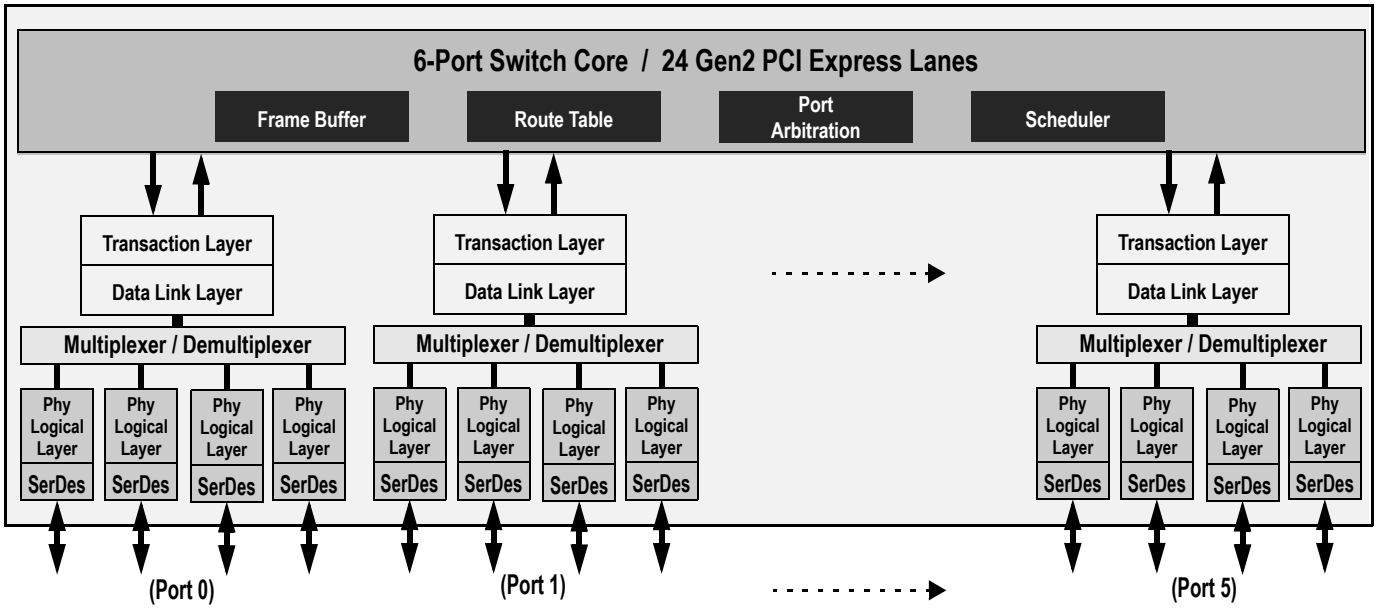


Figure 1 Internal Block Diagram

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- *Hot-swap capable I/O*
- *External Serial EEPROM contents are checksum protected*
- *Supports PCI Express Device Serial Number Capability*
- *Capability to monitor link reliability and autonomously change link speed to prevent link instability*

◆ **Power Management**

- *Utilizes advanced low-power design techniques to achieve low typical power consumption*
- *Support PCI Power Management Interface specification (PCI-PM 1.1)*
  - *Supports device power management states: D0, $D3_{hot}$ and $D3_{cold}$*
- *Support for PCI Express Active State Power Management (ASPM) link state*
  - *Supports link power management states: L0, L0s, L1, L2/L3 Ready and L3*
- *Supports PCI Express Power Budgeting Capability*
- *Configurable SerDes power consumption*
  - *Supports optional PCI-Express SerDes Transmit Low-Swing Voltage Mode*
  - *Supports numerous SerDes Transmit Voltage Margin settings*
- *Unused SerDes are disabled*

◆ **Testability and Debug Features**

- *Per port link up and activity status outputs available on I/O expander outputs*
- *Built in SerDes 8-bit and 10-bit pseudo-random bit stream (PRBS) generators*
- *Numerous SerDes test modes, including a PRBS Master Loopback mode for in-system link testing*
- *Ability to read and write any internal register via SMBus and JTAG interfaces, including SerDes internal controls*
- *Per port statistics and performance counters, as well as proprietary link status registers*

◆ **Eleven General Purpose Input/Output Pins**

- *Each pin may be individually configured as an input or output*
- *Each pin may be individually configured as an interrupt input*
- *Some pins have selectable alternate functions*

◆ **Option A Package: 19mm x 19mm 324-ball Flip Chip BGA with 1mm ball spacing**

◆ **Option B Package: 27mm x 27mm 676-ball Flip Chip BGA with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect, the PES24T6G2 provides the most efficient I/O connectivity solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides connectivity for up to 6 ports across 24 integrated serial lanes. Each lane provides 5 Gbps of bandwidth in both directions and is fully compliant with PCI Express Base Specification, Revision 2.0, including operation in 5 Gbps, 2.5 Gbps, and mixed 5 Gbps / 2.5Gbps modes.

The PES24T6G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 2.0. The PES24T6G2 can operate either as a store and forward or cut-through switch and is designed to switch memory and I/O transactions. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

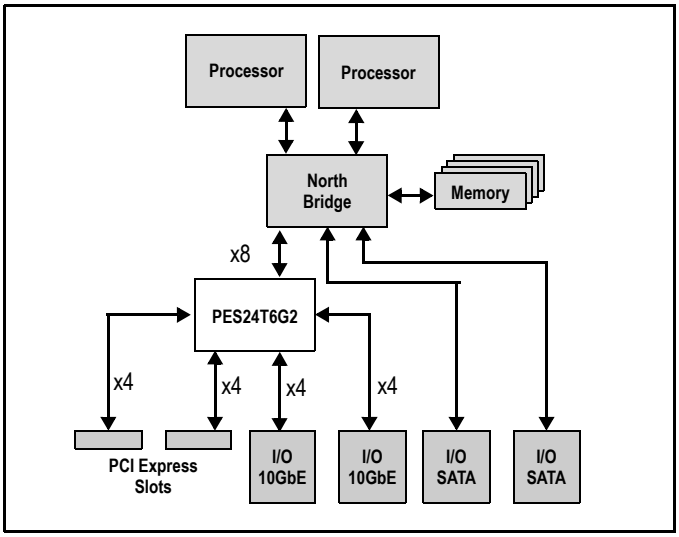


Figure 2 I/O Expansion Application

SMBus Interface

The PES24T6G2 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES24T6G2, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES24T6G2 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Six pins make up each of the two SMBus interfaces. These pins consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins. In the slave interface, these address pins allow the SMBus address to which the device responds to be configured. In the master interface, these address pins allow the SMBus address of the serial configuration EEPROM from which data is loaded to be configured. The SMBus address is set up on negation of PERSTN by sampling the corresponding address pins. When the pins are sampled, the resulting address is assigned as shown in Table 1.

> **Note:** MSMBADDR and SSMBADDR address pins are not available in the 19mm package. The MSMBADDR address is hardwired to 0x50, and the SSMBADDR address is hardwired to 0x77.

Bit	Slave SMBus Address	Master SMBus Address
1	SSMBADDR[1]	MSMBADDR[1]
2	SSMBADDR[2]	MSMBADDR[2]
3	SSMBADDR[3]	MSMBADDR[3]
4	0	MSMBADDR[4]
5	SSMBADDR[5]	1
6	1	0
7	1	1

Table 1 Master and Slave SMBus Address Assignment for 27x27mm Package

As shown in Figure 3, the master and slave SMBuses may be used in a unified or split configuration. In the unified configuration, shown in Figure 3(a), the master and slave SMBuses are tied together and the PES24T6G2 acts both as a SMBus master as well as a SMBus slave on this bus. This requires that the SMBus master or processor that has access to PES24T6G2 registers supports SMBus arbitration. In some systems, this SMBus master interface may be implemented using general purpose I/O pins on a processor or micro controller, and may not support SMBus arbitration. To support these systems, the PES24T6G2 may be configured to operate in a split configuration as shown in Figure 3(b).

In the split configuration, the master and slave SMBuses operate as two independent buses and thus multi-master arbitration is never required. The PES24T6G2 supports reading and writing of the serial EEPROM on the master SMBus via the slave SMBus, allowing in system programming of the serial EEPROM.

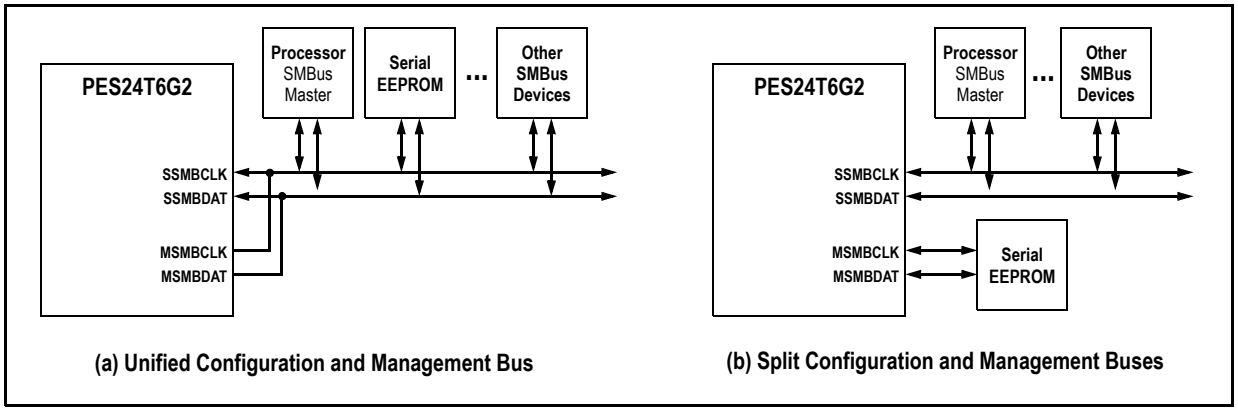


Figure 3 SMBus Interface Configuration Examples

Hot-Plug Interface

The PES24T6G2 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES24T6G2 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES24T6G2 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES24T6G2. In response to an I/O expander interrupt, the PES24T6G2 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES24T6G2 provides General Purpose Input/Output (GPIO) pins (7 pins in the 19mm package and 11 pins in the 27mm package) that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Many GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES24T6G2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
PE0RP[3:0] PE0RN[3:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0. Port 0 is the upstream port.
PE0TP[3:0] PE0TN[3:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0. Port 0 is the upstream port.
PE1RP[3:0] PE1RN[3:0]	I	**PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pairs for port 1.
PE1TP[3:0] PE1TN[3:0]	O	**PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pairs for port 1.
PE2RP[3:0] PE2RN[3:0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE2TP[3:0] PE2TN[3:0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE3RP[3:0] PE3RN[3:0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pairs for port 3.
PE3TP[3:0] PE3TN[3:0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pairs for port 3.
PE4RP[3:0] PE4RN[3:0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pairs for port 4.
PE4TP[3:0] PE4TN[3:0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pairs for port 4.
PE5RP[3:0] PE5RN[3:0]	I	**PCI Express Port 5 Serial Data Receive.** Differential PCI Express receive pairs for port 5.
PE5TP[3:0] PE5TN[3:0]	O	**PCI Express Port 5 Serial Data Transmit.** Differential PCI Express transmit pairs for port 5.
PEREFCLKP PEREFCLKN	I	**PCI Express Reference Clock.** Differential reference clock pair input. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic and on-chip SerDes. The frequency of the differential reference clock is determined by the REFCLKM signal.
REFCLKM[1]	I	**PCI Express Reference Clock Mode Select.** This signal selects the frequency of the reference clock input. 0x0 - 100 MHz 0x1 - 125 MHz This pin should be static and not change following the negation of PERSTN.

Table 2 PCI Express Interface Pins

1. REFCLKM is not available in the 19mm package and frequency is set at 100MHz.

Signal	Type	Name/Description
MSMBADDR[4:1][1]	I	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded.
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus.

Table 3 SMBus Interface Pins (Part 1 of 2)

Signal	Type	Name/Description
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[5,3:1][2]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 3 SMBus Interface Pins (Part 2 of 2)

1. MSMBADDR pins are not available in the 19mm package. Address hardwired to 0x50.
2. SSMBADDR pins are not available in the 19mm package. Address hardwired to 0x77.

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P2RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 2
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P4RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 4
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN0 Alternate function pin type: Input Alternate function: I/O Expander interrupt 0 input
GPIO[3][1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN1 Alternate function pin type: Input Alternate function: I/O Expander interrupt 1 input
GPIO[4][1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN2 Alternate function pin type: Input Alternate function: I/O Expander interrupt 2 input
GPIO[5][1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN3 Alternate function pin type: Input Alternate function: I/O Expander interrupt 3 input
GPIO[6][1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: GPEN Alternate function pin type: Output Alternate function: General Purpose Event (GPE) output

Table 4 General Purpose I/O Pins (Part 1 of 2)

Signal	Type	Name/Description
GPIO[8]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P1RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 1
GPIO[9]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P3RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 3
GPIO[10]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: P5RSTN Alternate function pin type: Output Alternate function: Reset output for downstream port 5

Table 4 General Purpose I/O Pins (Part 2 of 2)

1. GPIO pins 3, 4, 5, 6 are not available in the 19mm package.

Signal	Type	Name/Description
CCLKDS	I	**Common Clock Downstream.** The assertion of this pin indicates that all downstream ports are using the same clock source as that provided to downstream devices.This bit is used as the initial value of the Slot Clock Configuration bit in all of the Link Status Registers for downstream ports. The value may be overridden by modifying the SCLK bit in each downstream port's PCIELSTS register.
CCLKUS	I	**Common Clock Upstream.** The assertion of this pin indicates that the upstream port is using the same clock source as the upstream device. This bit is used as the initial value of the Slot Clock Configuration bit in the Link Status Register for the upstream port. The value may be overridden by modifying the SCLK bit in the P0_PCIELSTS register.
MSMBSMODE[1]	I	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 KHz. This value may not be overridden.
P01MERGEN	I	**Port 0 and 1 Merge.** P01MERGEN is an active low signal. It is pulled high internally via a 92K ohm resistor. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port.
P23MERGEN	I	**Port 2 and 3 Merge.** P23MERGEN is an active low signal. It is pulled high internally via a 92K ohm resistor. When this pin is low, port 2 is merged with port 3 to form a single x8 port. The Serdes lanes associated with port 3 become lanes 4 through 7 of port 2. When this pin is high, port 2 and port 3 are not merged, and each operates as a single x4 port.
P45MERGEN	I	**Port 4 and 5 Merge.** P45MERGEN is an active low signal. It is pulled high internally via a 92K ohm resistor. When this pin is low, port 4 is merged with port 5 to form a single x8 port. The Serdes lanes associated with port 5 become lanes 4 through 7 of port 4. When this pin is high, port 4 and port 5 are not merged, and each operates as a single x4 port.
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside PES24T6G2 and initiates a PCI Express fundamental reset.

Table 5 System Pins (Part 1 of 2)

Signal	Type	Name/Description
RSTHALT[2]	I	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, PES24T6G2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[2:0]	I	**Switch Mode.** These configuration pins determine the PES24T6G2 switch operating mode. 0x0 -Normal switch mode 0x1 -Normal switch mode with Serial EEPROM initialization 0x2 - through 0x7 Reserved These pins should be static and not change following the negation of PERSTN.

Table 5 System Pins (Part 2 of 2)

1. MSMBSMODE is not available in the 19mm package, resulting in the master SMBus operating only at 400 KHz.

2. RSTHALT is not available in the 19mm package.

Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 6 Test Pins

Signal	Type	Name/Description
REFRES0	I/O	**Port 0 External Reference Resistor.** Provides a reference for the Port 0 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES1	I/O	**Port 1 External Reference Resistor.** Provides a reference for the Port 1 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES2	I/O	**Port 2 External Reference Resistor.** Provides a reference for the Port 2 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES3	I/O	**Port 3 External Reference Resistor.** Provides a reference for the Port 3 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES4	I/O	**Port 4 External Reference Resistor.** Provides a reference for the Port 4 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
REFRES5	I/O	**Port 5 External Reference Resistor.** Provides a reference for the Port 5 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground.
V_{DD}CORE	I	**Core V_{DD}.** Power supply for core logic.
V_{DD}I/O	I	**I/O V_{DD}.** LVTTL I/O buffer power supply.
V_{DD}PEA	I	**PCI Express Analog Power.** Serdes analog power supply (1.0V).
V_{DD}PEHA	I	**PCI Express Analog High Power.** Serdes analog power supply (2.5V).
V_{DD}PETA	I	**PCI Express Transmitter Analog Voltage.** Serdes transmitter analog power supply (1.0V).
V_{SS}	I	Ground.

Table 7 Power, Ground, and SerDes Resistor Pins

Pin Characteristics

Note: Some input pads of the PES24T6G2 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE0RN[3:0]	I	PCIe differential[2]	Serial Link		
	PE0RP[3:0]	I				
	PE0TN[3:0]	O				
	PE0TP[3:0]	O				
	PE1RN[3:0]	I				
	PE1RP[3:0]	I				
	PE1TN[3:0]	O				
	PE1TP[3:0]	O				
	PE2RN[3:0]	I				
	PE2RP[3:0]	I				
	PE2TN[3:0]	O				
	PE2TP[3:0]	O				
	PE3RN[3:0]	I				
	PE3RP[3:0]	I				
	PE3TN[3:0]	O				
	PE3TP[3:0]	O				
	PE4RN[3:0]	I				
	PE4RP[3:0]	I				
	PE4TN[3:0]	O				
	PE4TP[3:0]	O				
	PE5RN[3:0]	I				
	PE5RP[3:0]	I				
	PE5TN[3:0]	O				
	PE5TP[3:0]	O				
	PEREFCLKN	I	HCSL	Diff. Clock Input		Refer to Table 9
	PEREFCLKP	I				
	REFCLKM[3]	I	LVTTL	Input	pull-down	
SMBus	MSMBADDR[4:1][4]	I	LVTTL	Input	pull-down	
	MSMBCLK	I/O		STI[5]		pull-up on board
	MSMBDAT	I/O		STI		pull-up on board
	SSMBADDR[5,3:1][4]	I		Input	pull-up	
	SSMBCLK	I/O		STI		pull-up on board
	SSMBDAT	I/O		STI		pull-up on board
General Purpose I/O	GPIO[10:0][6]	I/O	LVTTL	STI, High Drive	pull-up	

Table 8 Pin Characteristics (Part 1 of 2)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
System Pins	CCLKDS	I	LVTTL	Input	pull-up	
	CCLKUS	I		Input	pull-up	
	MSMBSMODE[7]	I		Input	pull-down	
	P01MERGEN	I			pull-up	
	P23MERGEN	I			pull-up	
	P45MERGEN	I			pull-up	
	PERSTN	I		STI		
	RSTHALT[7]	I		Input	pull-down	
	SWMODE[2:0]	I		Input	pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	
SerDes Reference Resistors	REFRES0	I/O	Analog			
	REFRES1	I/O				
	REFRES2	I/O				
	REFRES3	I/O				
	REFRES4	I/O				
	REFRES5	I/O				

Table 8 Pin Characteristics (Part 2 of 2)

1. Internal resistor values under typical operating conditions are 92K Ω for pull-up and 90K Ω for pull-down.
2. All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.
3. REFCLKM is not available in the 19mm package.
4. SMBus address pins are not available in the 19mm package.
5. Schmitt Trigger Input (STI).
6. GPIO pins 3, 4, 5, 6 are not available in the 19mm package.
7. MSMBSMODE and RSTHALT are not available in the 19mm package.

Logic Diagram — PES24T6G2

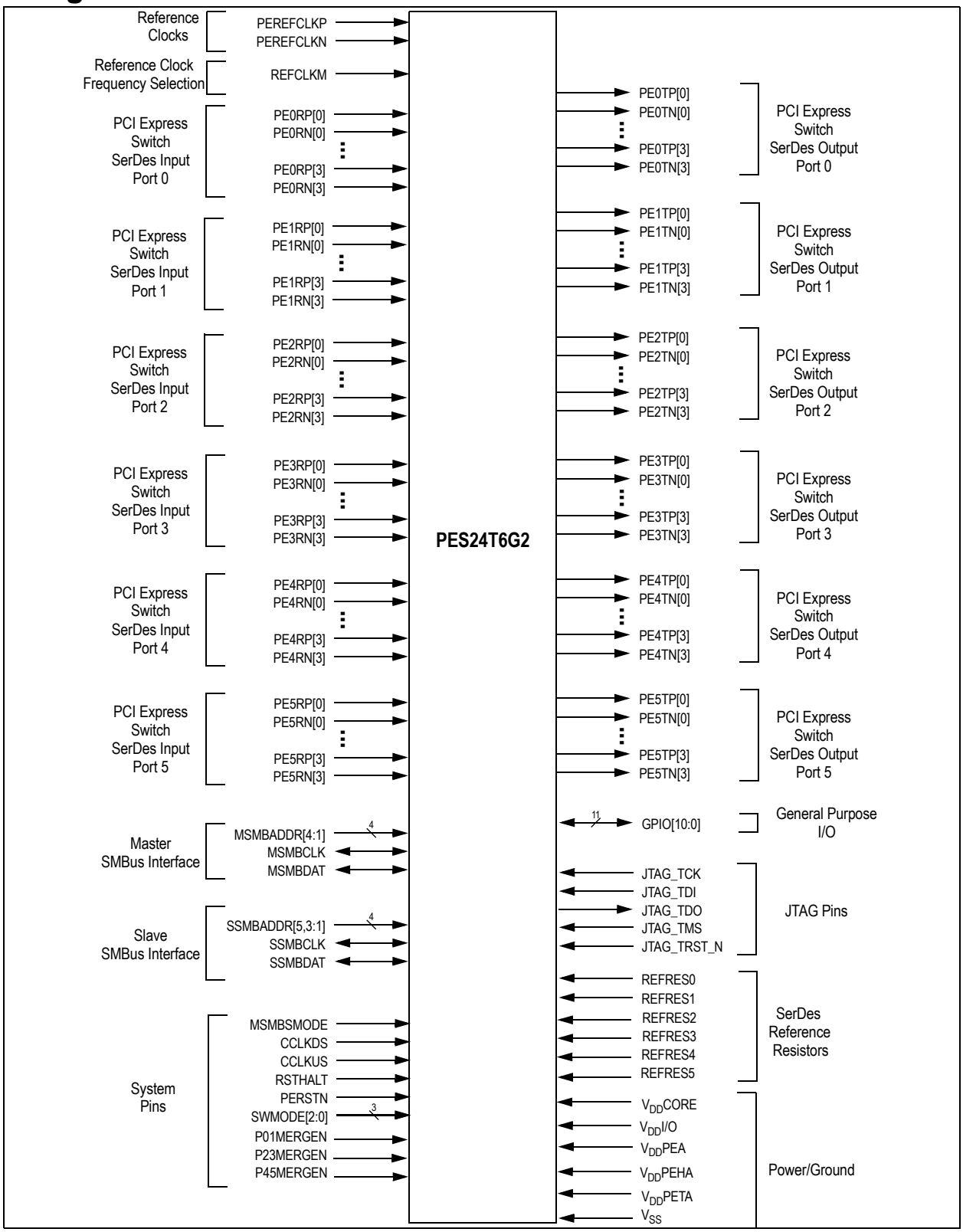


Figure 4 PES24T6G2 Logic Diagram

Note: The following pins are not available in the 19mm package: REFCLKM, MSMBADDR, SSMBADDR, MSMBSMODE, RSTHALT, GPIO[6:3].

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 15.

Parameter	Description	Condition	Min	Typical	Max	Unit
$Refclk_{FREQ}$	Input reference clock frequency range		100		125[1]	MHz
T_{C-RISE}	Rising edge rate	Differential	0.6		4	V/ns
T_{C-FALL}	Falling edge rate	Differential	0.6		4	V/ns
V_{IH}	Differential input high voltage	Differential	+150			mV
V_{IL}	Differential input low voltage	Differential			-150	mV
V_{CROSS}	Absolute single-ended crossing point voltage	Single-ended	+250		+550	mV
$V_{CROSS-DELTA}$	Variation of V_{CROSS} over all rising clock edges	Single-ended			+140	mV
V_{RB}	Ring back voltage margin	Differential	-100		+100	mV
T_{STABLE}	Time before V_{RB} is allowed	Differential	500			ps
$T_{PERIOD-AVG}$	Average clock period accuracy		-300		2800	ppm
$T_{PERIOD-ABS}$	Absolute period, including spread-spectrum and jitter		9.847		10.203	ns
$T_{CC-JITTER}$	Cycle to cycle jitter				150	ps
V_{MAX}	Absolute maximum input voltage				+1.15	V
V_{MIN}	Absolute minimum input voltage		-0.3			V
Duty Cycle	Duty cycle		40		60	%
Rise/Fall Matching	Single ended rising Refclk edge rate versus falling Refclk edge rate			20		%
Z_{C-DC}	Clock source output DC impedance		40		60	Ω

Table 9 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal REFCLKM. Frequency is set at 100 MHz in the 19mm package.

AC Timing Characteristics

Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
PCIe Transmit								
UI	Unit Interval	399.88	400	400.12	199.94	200	200.06	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.75			0.75			UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.125				UI
$T_{TX-RISE}$, $T_{TX-FALL}$	TX Rise/Fall Time: 20% - 80%	0.125			0.15			UI
$T_{TX-IDLE-MIN}$	Minimum time in idle	20			20			UI
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			8			8	ns

Table 10 PCIe AC Timing Characteristics (Part 1 of 2)

Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition from valid idle to diff data			8			8	ns
$T_{TX-SKEW}$	Transmitter data skew between any 2 lanes			1.3			1.3	ns
$T_{MIN-PULSED}$	Minimum Instantaneous Lone Pulse Width	NA			0.9			UI
$T_{TX-HF-DJ-DD}$	Transmitter Deterministic Jitter > 1.5MHz Bandwidth	NA					0.15	UI
$T_{RF-MISMATCH}$	Rise/Fall Time Differential Mismatch	NA					0.1	UI
PCIe Receive								
UI	Unit Interval	399.88	400	400.12	199.94		200.06	ps
$T_{RX-EYE\ (with\ jitter)}$	Minimum Receiver Eye Width (jitter tolerance)	0.4			0.4			UI
$T_{RX-EYE-MEDIUM\ TO\ MAX\ JITTER}$	Max time between jitter median & max deviation			0.3				UI
$T_{RX-SKEW}$	Lane to lane input skew			20			8	ns
$T_{RX-HF-RMS}$	1.5 — 100 MHz RMS jitter (common clock)	NA					3.4	ps
$T_{RX-HF-DJ-DD}$	Maximum tolerable DJ by the receiver (common clock)	NA					88	ps
$T_{RX-LF-RMS}$	10 KHz to 1.5 MHz RMS jitter (common clock)	NA					4.2	ps
$T_{RX-MIN-PULSE}$	Minimum receiver instantaneous eye width	NA			0.6			UI

Table 10 PCIe AC Timing Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[10:0][1]	Tpw[2]	None	50	—	ns	

Table 11 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous. Note that GPIO{6:3} pins are not available in the 19mm package.

2. The values for this symbol were determined by calculation, not by testing.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 5.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 12 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

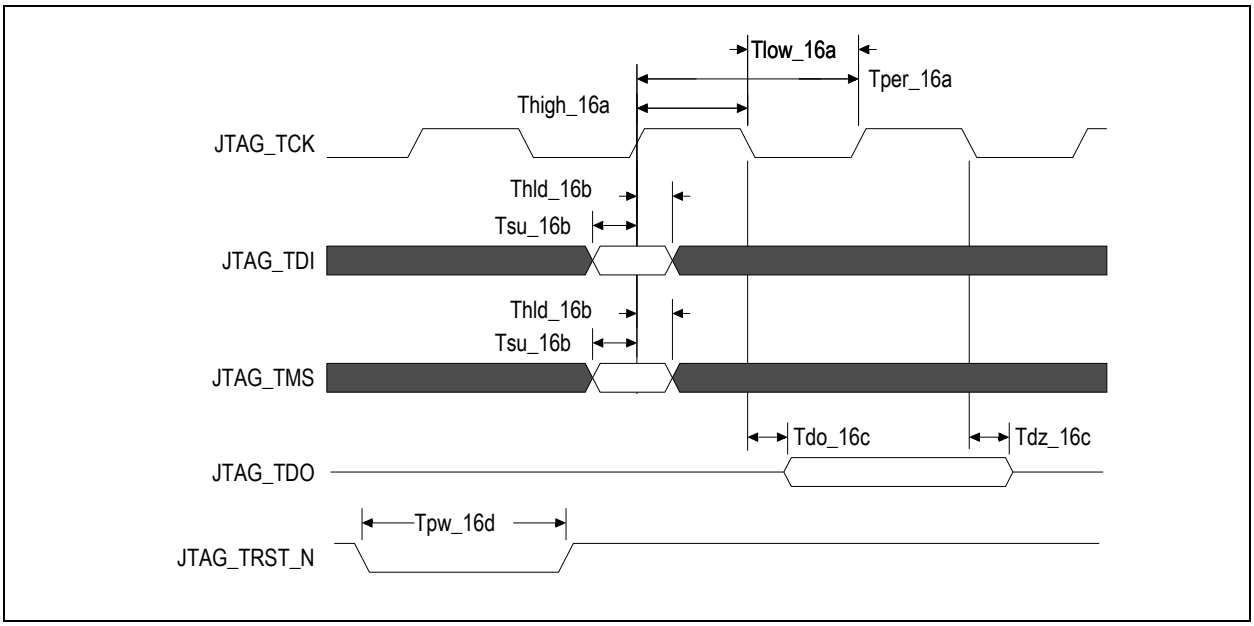


Figure 5 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes LVPECL/CML	3.135	3.3	3.465	V
V_{DD}PEA[1]	PCI Express Analog Power	0.95	1.0	1.1	V
V_{DD}PEHA[2]	PCI Express Analog High Power	2.25	2.5	2.75	V
V_{DD}PETA[1]	PCI Express Transmitter Analog Voltage	0.95	1.0	1.1	V
V_{SS}	Common ground	0	0	0	V

Table 13 PES24T6G2 Operating Voltages

1. V_{DD}PEA and V_{DD}PETA should have no more than 25m$V_{peak\text{-}peak}$ AC power supply noise superimposed on the 1.0V nominal DC value.
2. V_{DD}PEHA should have no more than 50m$V_{peak\text{-}peak}$ AC power supply noise superimposed on the 2.5V nominal DC value.

Absolute Maximum Voltage Rating

Core Supply	PCIe Analog Supply	PCIe Analog High Supply	PCIe Transmitter Supply	I/O Supply
1.5V	1.5V	4.6V	1.5V	4.6V

Table 14 PES24T6G2 Absolute Maximum Voltage Rating

Warning: For proper and reliable operation in adherence with this data sheet, the device should not exceed the recommended operating voltages in Table 13. The absolute maximum operating voltages in Table 14 are offered to provide guidelines for voltage excursions outside the recommended voltage ranges. Device functionality is not guaranteed at these conditions and sustained operation at these values or any exposure to voltages outside the maximum range may adversely affect device functionality and reliability.

Power-Up/Power-Down Sequence

During power supply ramp-up, V_{DD}CORE must remain at least 1.0V below V_{DD}I/O at all times. There are no other power-up sequence requirements for the various operating supply voltages.

The power-down sequence can occur in any order.

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 15 PES24T6G2 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

Number of active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		PCIe Termination Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ 1.0V	Max 1.15V	Typ 3.3V	Max 3.465V	Typ Power	Max Power
8/4/4/4/4 (Full Swing)	mA	1010	1260	1384	1600	161	176	541	600	3	5		
	Watts	1.01	1.39	1.38	1.76	0.40	0.48	0.54	0.66	0.010	0.017	3.35	4.31
8/4/4/4/4 (Half swing)	mA	1010	1260	1190	1376	161	176	281	312	3	5		
	Watts	1.01	1.39	1.19	1.51	0.40	0.48	0.28	0.34	0.010	0.017	2.89	3.74

Table 16 PES24T6G2 Power Consumption

Thermal Considerations — Option A Package

This section describes thermal considerations for the PES24T6G2 (19mm^2 FCBGA324 package). The data in Table 17 below contains information that is relevant to the thermal performance of the PES24T6G2 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	16.8	°C/W	Zero air flow
		10.1	°C/W	1 m/S air flow
		9.2	°C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	4.1	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.3	°C/W	
P	Power Dissipation of the Device	4.31	Watts	Maximum

Table 17 Thermal Specifications for PES24T6G2, 19x19 mm FCBGA324 Package

Thermal Considerations — Option B Package

This section describes thermal considerations for the PES24T6G2 (27mm^2 FCBGA676 package). The data in Table 18 below contains information that is relevant to the thermal performance of the PES24T6G2 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	°C	Maximum
$T_{A(max)}$	Ambient Temperature	70	°C	Maximum

Table 18 Thermal Specifications for PES24T6G2, 27x27 mm FCBGA676 Package

Symbol	Parameter	Value	Units	Conditions
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	14.6	°C/W	Zero air flow
		8.2	°C/W	1 m/S air flow
		7.2	°C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	3.1	°C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.3	°C/W	
P	Power Dissipation of the Device	4.31	Watts	Maximum

Table 18 Thermal Specifications for PES24T6G2, 27x27 mm FCBGA676 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 17. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 17), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). As a general guideline, this device will not need a heat sink if the board has 8 or more layers AND the board size is larger than 4"x12" AND airflow in excess of 0.5 m/s is available. It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Conditions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Serial Link	PCIe Transmit									
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	800		1200	mV	
	$V_{TX-DIFFp-p-LOW}$	Low-Drive Differential Peak to Peak Output Voltage	400		1200	400		1200	mV	
	$V_{TX-DE-RATIO-3.5dB}$	De-emphasized differential output voltage	-3		-4	-3.0	-3.5	-4.0	dB	
	$V_{TX-DE-RATIO-6.0dB}$	De-emphasized differential output voltage	NA			-5.5	-6.0	-6.5	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	0		3.6	0		3.6	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20				mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20			20	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	10					10	dB	0.05 - 1.25GHz
								8	dB	1.25 - 2.5GHz
	RL_{TX-CM}	Transmitter Common Mode Return loss	6					6	dB	
	$Z_{TX-DIFF-DC}$	DC Differential TX impedance	80	100	120			120	Ω	
	VTX-CM-ACpp	Peak-Peak AC Common	NA					100	mV	
	$V_{TX-DC-CM}$	Transmit Driver DC Common Mode Voltage	0		3.6	0		3.6	V	
	$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection			600			600	mV	
	$I_{TX-SHORT}$	Transmitter Short Circuit Current Limit	0		90				90	mA

Table 19 DC Electrical Characteristics (Part 1 of 2)

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Conditions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Serial Link (cont.)	PCIe Receive									
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	120		1200	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	10					10	dB	0.05 - 1.25GHz
								8		1.25 - 2.5GHz
	RL_{RX-CM}	Receiver Common Mode Return Loss	6					6	dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Refer to return loss spec			Ω	
	Z_{RX--DC}	DC common mode impedance	40	50	60	40		60	Ω	
	$Z_{RX-COMM-DC}$	Powered down input common mode impedance (DC)	200k	350k				50k	Ω	
	$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance for V>0 during reset or power down			50k			50k	Ω	
	$Z_{RX-HIGH-IMP-DC-NEG}$	DC input CM input impedance for V<0 during reset or power down			1.0k			1.0k	Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	65		175	mV	
	$V_{RX-CM-ACp}$	Receiver AC common-mode peak voltage			150			150	mV	$V_{RX-CM-ACp}$
PCIe REFCLK										
	C_{IN}	Input Capacitance	1.5	—		1.5	—		pF	
Other I/Os										
LOW Drive Output	I_{OL}		—	2.5	—	—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	2.0	—	V_{DD}I/O + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	2.0	—	V_{DD}I/O + 0.5	V	—
Capacitance	C_{IN}		—	—	8.5	—	—	8.5	pF	—
Leakage	Inputs		—	—	± 10	—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	—	—	± 80	µA	V_{DD}I/O (max)

Table 19 DC Electrical Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0.

PES24T6G2 Package Options

Package Option	Package Size
A	19x19 mm
B	27x27 mm

Table 20 PES24T6G2 Package Options

Option A Package Pinout, 19x19mm 324-BGA Signal Pinout

The following table lists the pin numbers and signal names for the PES24T6G2 device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B17	PE4TN00		D15	V_{DD}CORE		F13	V_{SS}	
A2	V_{DD}I/O		B18	PE4TP00		D16	V_{SS}		F14	PE4RN03	
A3	P01MERGEN		C1	PE3TP02		D17	V_{SS}		F15	PE4RP03	
A4	P23MERGEN		C2	PE3TN02		D18	V_{SS}		F16	V_{SS}	
A5	P45MERGEN		C3	V_{SS}		E1	PE3TP01		F17	PE4TN03	
A6	V_{DD}I/O		C4	PE3RP02		E2	PE3TN01		F18	PE4TP03	
A7	V_{SS}		C5	PE3RN02		E3	V_{SS}		G1	V_{SS}	
A8	JTAG_TDI		C6	V_{SS}		E4	PE3RP01		G2	V_{SS}	
A9	MSMBDAT		C7	JTAG_TCK		E5	PE3RN01		G3	V_{SS}	
A10	V_{DD}I/O		C8	JTAG_TRST_N		E6	V_{DD}CORE		G4	V_{DD}CORE	
A11	V_{SS}		C9	SSMBDAT		E7	V_{DD}CORE		G5	V_{DD}CORE	
A12	GPIO_00	1	C10	CCLKDS		E8	V_{DD}CORE		G6	V_{DD}PEA	
A13	V_{DD}I/O		C11	SWMODE_2		E9	V_{SS}		G7	V_{DD}PEA	
A14	V_{DD}I/O		C12	GPIO_02	1	E10	V_{DD}CORE		G8	V_{DD}CORE	
A15	V_{SS}		C13	GPIO_09	1	E11	V_{DD}CORE		G9	V_{DD}CORE	
A16	V_{SS}		C14	PE4RN01		E12	V_{DD}CORE		G10	V_{DD}CORE	
A17	V_{DD}I/O		C15	PE4RP01		E13	V_{DD}CORE		G11	V_{SS}	
A18	V_{DD}I/O		C16	V_{SS}		E14	PE4RN02		G12	V_{DD}PEA	
B1	PE3TP03		C17	PE4TN01		E15	PE4RP02		G13	V_{DD}PEA	
B2	PE3TN03		C18	PE4TP01		E16	V_{SS}		G14	V_{DD}CORE	
B3	V_{SS}		D1	V_{SS}		E17	PE4TN02		G15	V_{DD}CORE	
B4	PE3RP03		D2	V_{SS}		E18	PE4TP02		G16	V_{SS}	
B5	PE3RN03		D3	V_{SS}		F1	PE3TP00		G17	V_{SS}	
B6	V_{DD}I/O		D4	V_{DD}CORE		F2	PE3TN00		G18	V_{SS}	
B7	V_{DD}I/O		D5	V_{DD}CORE		F3	V_{SS}		H1	PE2TP03	
B8	JTAG_TMS		D6	V_{DD}I/O		F4	PE3RP00		H2	PE2TN03	
B9	SSMBCLK		D7	JTAG_TDO		F5	PE3RN00		H3	V_{SS}	
B10	V_{DD}I/O		D8	MSMBCLK		F6	V_{SS}		H4	PE2RP03	
B11	SWMODE_1		D9	CCLKUS		F7	V_{SS}		H5	PE2RN03	
B12	GPIO_01	1	D10	SWMODE_0		F8	V_{DD}CORE		H6	V_{DD}PEA	
B13	GPIO_10	1	D11	PERSTN		F9	V_{SS}		H7	V_{DD}PEA	
B14	PE4RN00		D12	GPIO_07	1	F10	V_{DD}CORE		H8	V_{DD}CORE	
B15	PE4RP00		D13	GPIO_08		F11	V_{SS}		H9	V_{DD}CORE	
B16	V_{SS}		D14	V_{DD}CORE		F12	V_{SS}		H10	V_{DD}CORE	

Table 21 PES24T6G2 (19x19mm 324-pin) Signal Pin-Out (Part 1 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
H11	V_{SS}		K13	V_{DD}PETA		M15	PE5RP03		P17	V_{DD}CORE	
H12	V_{DD}PEA		K14	V_{DD}CORE		M16	V_{SS}		P18	V_{SS}	
H13	V_{DD}PEA		K15	NC		M17	PE5TN03		R1	V_{SS}	
H14	PE5RN00		K16	V_{SS}		M18	PE5TP03		R2	V_{DD}CORE	
H15	PE5RP00		K17	REFRES5		N1	V_{SS}		R3	V_{DD}CORE	
H16	V_{SS}		K18	REFRES4		N2	V_{SS}		R4	PE1RP03	
H17	PE5TN00		L1	PE2TP01		N3	V_{SS}		R5	PE1RP02	
H18	PE5TP00		L2	PE2TN01		N4	V_{DD}CORE		R6	NC	
J1	PE2TP02		L3	V_{SS}		N5	V_{DD}CORE		R7	PE1RP01	
J2	PE2TN02		L4	PE2RP01		N6	V_{SS}		R8	PE1RP00	
J3	V_{SS}		L5	PE2RN01		N7	V_{SS}		R9	V_{DD}CORE	
J4	PE2RP02		L6	V_{DD}PETA		N8	V_{DD}PEA		R10	PE0RP03	
J5	PE2RN02		L7	V_{DD}PETA		N9	V_{DD}PEHA		R11	PE0RP02	
J6	V_{DD}PEHA		L8	V_{DD}PEA		N10	V_{DD}PETA		R12	V_{DD}CORE	
J7	V_{DD}PEHA		L9	V_{DD}PEHA		N11	V_{DD}PEA		R13	PE0RP01	
J8	V_{DD}CORE		L10	V_{DD}PETA		N12	V_{DD}PEHA		R14	PE0RP00	
J9	V_{SS}		L11	V_{DD}PEA		N13	V_{SS}		R15	V_{DD}CORE	
J10	V_{DD}CORE		L12	V_{DD}PEHA		N14	V_{SS}		R16	V_{DD}CORE	
J11	V_{SS}		L13	V_{DD}PETA		N15	V_{DD}CORE		R17	V_{DD}CORE	
J12	V_{DD}PEHA		L14	PE5RN02		N16	V_{SS}		R18	V_{SS}	
J13	V_{DD}PEHA		L15	PE5RP02		N17	V_{SS}		T1	V_{SS}	
J14	PE5RN01		L16	V_{SS}		N18	V_{SS}		T2	V_{SS}	
J15	PE5RP01		L17	PE5TN02		P1	V_{SS}		T3	V_{SS}	
J16	V_{SS}		L18	PE5TP02		P2	V_{DD}CORE		T4	V_{SS}	
J17	PE5TN01		M1	PE2TP00		P3	V_{DD}CORE		T5	V_{SS}	
J18	PE5TP01		M2	PE2TN00		P4	PE1RN03		T6	V_{SS}	
K1	REFRES2		M3	V_{SS}		P5	PE1RN02		T7	V_{SS}	
K2	REFRES3		M4	PE2RP00		P6	V_{DD}CORE		T8	V_{SS}	
K3	V_{SS}		M5	PE2RN00		P7	PE1RN01		T9	V_{SS}	
K4	V_{DD}CORE		M6	V_{DD}PETA		P8	PE1RN00		T10	V_{SS}	
K5	V_{DD}CORE		M7	V_{DD}PETA		P9	V_{DD}CORE		T11	V_{SS}	
K6	V_{DD}PETA		M8	V_{DD}PEA		P10	PE0RN03		T12	V_{SS}	
K7	V_{DD}PETA		M9	V_{DD}PEHA		P11	PE0RN02		T13	V_{SS}	
K8	V_{DD}CORE		M10	V_{DD}PETA		P12	V_{DD}CORE		T14	V_{SS}	
K9	V_{SS}		M11	V_{DD}PEA		P13	PE0RN01		T15	V_{SS}	
K10	V_{DD}CORE		M12	V_{DD}PEHA		P14	PE0RN00		T16	V_{SS}	
K11	V_{SS}		M13	V_{SS}		P15	V_{DD}CORE		T17	V_{SS}	

Table 21 PES24T6G2 (19x19mm 324-pin) Signal Pin-Out (Part 2 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
K12	V_{DD}PETA		M14	PE5RN03		P16	V_{DD}CORE		T18	V_{SS}	
U1	V_{SS}		U10	PE0TN03		V1	V_{SS}		V10	PE0TP03	
U2	PEREFCLKN		U11	PE0TN02		V2	PEREFCLKP		V11	PE0TP02	
U3	V_{SS}		U12	V_{SS}		V3	V_{SS}		V12	V_{SS}	
U4	PE1TN03		U13	PE0TN01		V4	PE1TP03		V13	PE0TP01	
U5	PE1TN02		U14	PE0TN00		V5	PE1TP02		V14	PE0TP00	
U6	REFRES1		U15	V_{SS}		V6	REFRES0		V15	V_{SS}	
U7	PE1TN01		U16	V_{SS}		V7	PE1TP01		V16	V_{SS}	
U8	PE1TN00		U17	V_{SS}		V8	PE1TP00		V17	V_{SS}	
U9	V_{SS}		U18	V_{SS}		V9	V_{SS}		V18	V_{SS}	

Table 21 PES24T6G2 (19x19mm 324-pin) Signal Pin-Out (Part 3 of 3)

Option A Package — Alternate Signal Functions

Pin	GPIO	Alternate
A12	GPIO_00	P2RSTN
B12	GPIO_01	P4RSTN
C12	GPIO_02	IOEXPINTN0
D12	GPIO_07	GPEN
D13	GPIO_08	P1RSTN
C13	GPIO_09	P3RSTN
B13	GPIO_10	P5RSTN

Table 22 PES24T6G2 (19x19mm 324-Pin) Alternate Signal Functions

Option A Package — Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}I/O	V_{DD}PEA	V_{DD}PEHA	V_{TT}PETA
D4	G9	N15	A2	G6	J6	K6
D5	G10	P2	A6	G7	J7	K7
D14	G14	P3	A10	G12	J12	K12
D15	G15	P6	A13	G13	J13	K13
E6	H8	P9	A14	H6	L9	L6
E7	H9	P12	A17	H7	L12	L7
E8	H10	P15	A18	H12	M9	L10
E10	J8	P16	B6	H13	M12	L13
E11	J10	P17	B7	L8	N9	M6
E12	K4	R2	B10	L11	N12	M7
E13	K5	R3	D6	M8		M10
F8	K8	R9		M11		N10
F10	K10	R12		N8		
G4	K14	R15		N11		
G5	N4	R16				
G8	N5	R17				

Table 23 PES24T6G2 (19x19mm 324-pin) Power Pins

Option A Package — Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	E9	H3	N2	T5	U12
A7	E16	H11	N3	T6	U15
A11	F3	H16	N6	T7	U16
A15	F6	J3	N7	T8	U17
A16	F7	J9	N13	T9	U18
B3	F9	J11	N14	T10	V1
B16	F11	J16	N16	T11	V3
C3	F12	K3	N17	T12	V9
C6	F13	K9	N18	T13	V12
C16	F16	K11	P1	T14	V15
D1	G1	K16	P18	T15	V16
D2	G2	L3	R1	T16	V17
D3	G3	L16	R18	T17	V18
D16	G11	M3	T1	T18	
D17	G16	M13	T2	U1	
D18	G17	M16	T3	U3	
E3	G18	N1	T4	U9	

Table 24 PES24T6G2 (19x19mm 324-pin) Ground Pins

Option A Package — Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	C10	System
CCLKUS	I	D9	
GPIO_00	I/O	A12	General Purpose Input/Output
GPIO_01	I/O	B12	
GPIO_02	I/O	C12	
GPIO_07	I/O	D12	
GPIO_08	I/O	D13	
GPIO_09	I/O	C13	
GPIO_10	I/O	B13	
JTAG_TCK	I	C7	JTAG
JTAG_TDI	I	A8	
JTAG_TDO	O	D7	
JTAG_TMS	I	B8	
JTAG_TRST_N	I	C8	
MSMBCLK	I/O	D8	SMBus
MSMBDAT	I/O	A9	
NO CONNECTION		K15, R6	
P01MERGEN	I	A3	System
P23MERGEN	I	A4	
P45MERGEN	I	A5	
PE0RN00	I	P14	PCI Express
PE0RN01	I	P13	
PE0RN02	I	P11	
PE0RN03	I	P10	
PE0RP00	I	R14	
PE0RP01	I	R13	
PE0RP02	I	R11	
PE0RP03	I	R10	
PE0TN00	O	U14	
PE0TN01	O	U13	
PE0TN02	O	U11	
PE0TN03	O	U10	
PE0TP00	O	V14	
PE0TP01	O	V13	
PE0TP02	O	V11	
PE0TP03	O	V10	

Table 25 PES24T6G2 (19x19mm 324-pin) Alphabetical Signal List (Part 1 of 4)

Signal Name	I/O Type	Location	Signal Category
PE1RN00	I	P8	PCI Express
PE1RN01	I	P7	
PE1RN02	I	P5	
PE1RN03	I	P4	
PE1RP00	I	R8	
PE1RP01	I	R7	
PE1RP02	I	R5	
PE1RP03	I	R4	
PE1TN00	O	U8	
PE1TN01	O	U7	
PE1TN02	O	U5	
PE1TN03	O	U4	
PE1TP00	O	V8	
PE1TP01	O	V7	
PE1TP02	O	V5	
PE1TP03	O	V4	
PE2RN00	I	M5	
PE2RN01	I	L5	
PE2RN02	I	J5	
PE2RN03	I	H5	
PE2RP00	I	M4	
PE2RP01	I	L4	
PE2RP02	I	J4	
PE2RP03	I	H4	
PE2TN00	O	M2	
PE2TN01	O	L2	
PE2TN02	O	J2	
PE2TN03	O	H2	
PE2TP00	O	M1	
PE2TP01	O	L1	
PE2TP02	O	J1	
PE2TP03	O	H1	
PE3RN00	I	F5	
PE3RN01	I	E5	
PE3RN02	I	C5	
PE3RN03	I	B5	PCI Express (cont.)
PE3RP00	I	F4	

Table 25 PES24T6G2 (19x19mm 324-pin) Alphabetical Signal List (Part 2 of 4)

Signal Name	I/O Type	Location	Signal Category
PE3RP01	I	E4	
PE3RP02	I	C4	
PE3RP03	I	B4	
PE3TN00	O	F2	
PE3TN01	O	E2	
PE3TN02	O	C2	
PE3TN03	O	B2	
PE3TP00	O	F1	
PE3TP01	O	E1	
PE3TP02	O	C1	
PE3TP03	O	B1	
PE4RN00	I	B14	
PE4RN01	I	C14	
PE4RN02	I	E14	
PE4RN03	I	F14	
PE4RP00	I	B15	
PE4RP01	I	C15	
PE4RP02	I	E15	
PE4RP03	I	F15	
PE4TN00	O	B17	
PE4TN01	O	C17	
PE4TN02	O	E17	
PE4TN03	O	F17	
PE4TP00	O	B18	
PE4TP01	O	C18	
PE4TP02	O	E18	
PE4TP03	O	F18	
PE5RN00	I	H14	
PE5RN01	I	J14	
PE5RN02	I	L14	
PE5RN03	I	M14	
PE5RP00	I	H15	
PE5RP01	I	J15	
PE5RP02	I	L15	
PE5RP03	I	M15	PCI Express (cont.)
PE5TN00	O	H17	
PE5TN01	O	J17	

Table 25 PES24T6G2 (19x19mm 324-pin) Alphabetical Signal List (Part 3 of 4)

Signal Name	I/O Type	Location	Signal Category
PE5TN02	O	L17	
PE5TN03	O	M17	
PE5TP00	O	H18	
PE5TP01	O	J18	
PE5TP02	O	L18	
PE5TP03	O	M18	
PEREFCLKN	I	U2	
PEREFCLKP	I	V2	
PERSTN	I	D11	System
REFRES0	I/O	V6	SerDes Reference Resistors
REFRES1	I/O	U6	
REFRES2	I/O	K1	
REFRES3	I/O	K2	
REFRES4	I/O	K18	
REFRES5	I/O	K17	
SSMBCLK	I/O	B9	SMBus
SSMBDAT	I/O	C9	
SWMODE_0	I	D10	System
SWMODE_1	I	B11	
SWMODE_2	I	C11	
V_{DD}CORE, V_{DD}I/O, V_{DD}PEA, V_{DD}PEHA, V_{DD}PETA	See Table 28 for a listing of power pins.		
V_{SS}	See Table 24 for a listing of ground pins.		

Table 25 PES24T6G2 (19x19mm 324-pin) Alphabetical Signal List (Part 4 of 4)

Option A Package — Package Trace Length

Signal Name	Conductor Length (microns)
PE0RN00	6476.76
PE0RP00	6852.44
PE0RN01	5193.18
PE0RP01	5556.44
PE0RN02	4122.07
PE0RP02	4488.70
PE0RN03	4026.18
PE0RP03	4426.98
PE0TN00	9779.14
PE0TP00	9830.77
PE0TN01	8725.88
PE0TP01	8836.41
PE0TN02	7608.89
PE0TP02	7657.42
PE0TN03	7295.70
PE0TP03	7361.98
PE1RN00	3844.19
PE1RP00	4219.88
PE1RN01	4261.05
PE1RP01	4636.74
PE1RN02	5263.73
PE1RP02	5639.42
PE1RN03	6331.07
PE1RP03	6726.84
PE1TN00	7518.88
PE1TP00	7605.87
PE1TN01	7393.75
PE1TP01	7528.38
PE1TN02	8469.86
PE1TP02	8583.77
PE1TN03	8516.01
PE1TP03	8650.63
PE2RN00	2227.99
PE2RP00	2600.58
PE2RN01	1881.27

Table 26 Signal Trace Length (Part 1 of 3)

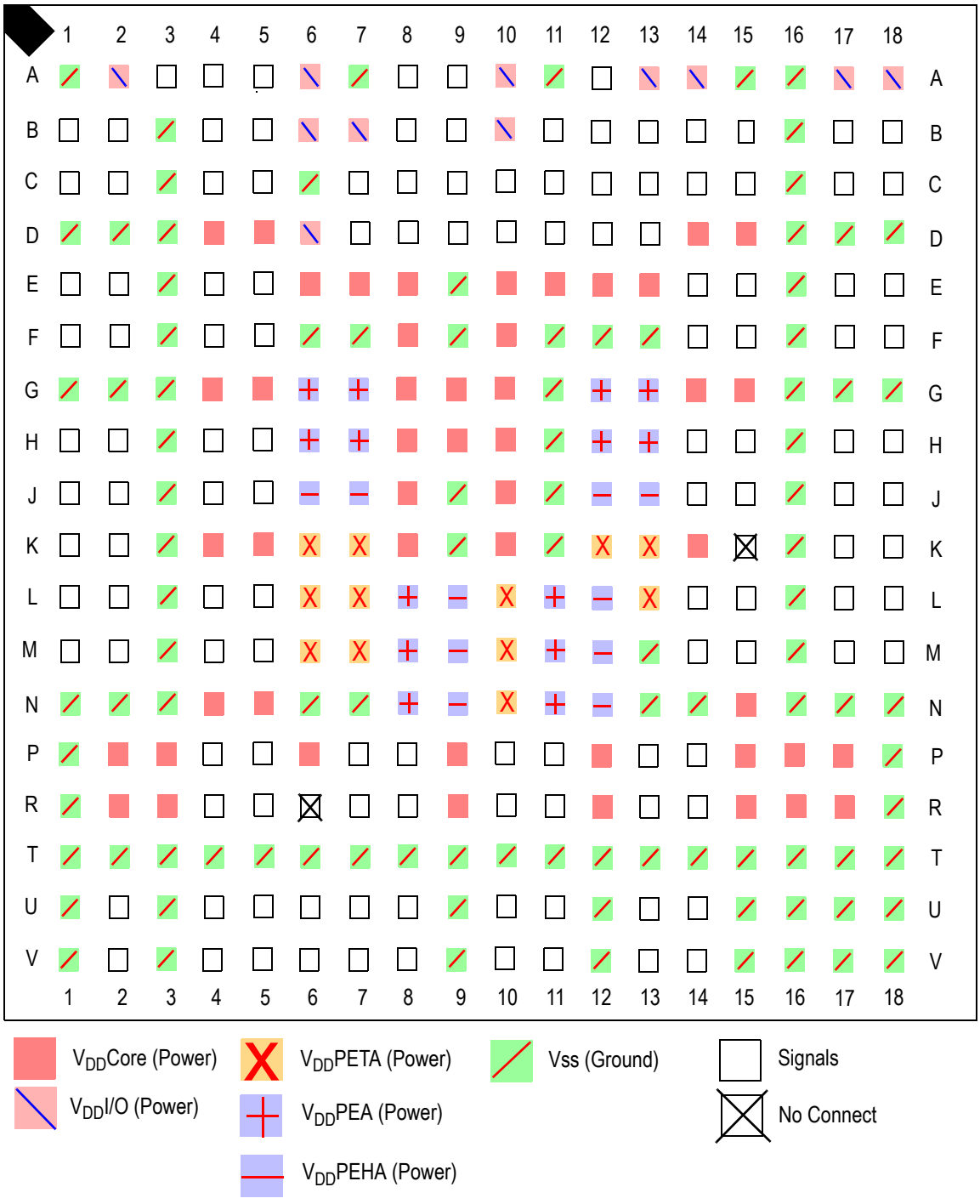
Signal Name	Conductor Length (microns)
PE2RP01	2256.96
PE2RN02	2105.60
PE2RP02	2470.94
PE2RN03	2835.27
PE2RP03	3207.86
PE2TN00	5462.64
PE2TP00	5576.55
PE2TN01	5163.54
PE2TP01	5273.30
PE2TN02	5389.58
PE2TP02	5512.25
PE2TN03	5310.88
PE2TP03	5451.71
PE3RN00	9181.06
PE3RP00	9541.52
PE3RN01	8602.32
PE3RP01	8994.21
PE3RN02	8220.08
PE3RP02	8604.05
PE3RN03	8906.71
PE3RP03	9193.82
PE3TN00	10606.88
PE3TP00	10747.72
PE3TN01	10972.20
PE3TP01	11117.18
PE3TN02	11862.08
PE3TP02	11978.06
PE3TN03	11822.86
PE3TP03	11870.23
PE4RN00	9450.47
PE4RP00	9700.88
PE4RN01	8438.57
PE4RP01	8818.65
PE4RN02	8521.33
PE4RP02	8890.07
PE4RN03	9130.21
PE4RP03	9403.58

Table 26 Signal Trace Length (Part 2 of 3)

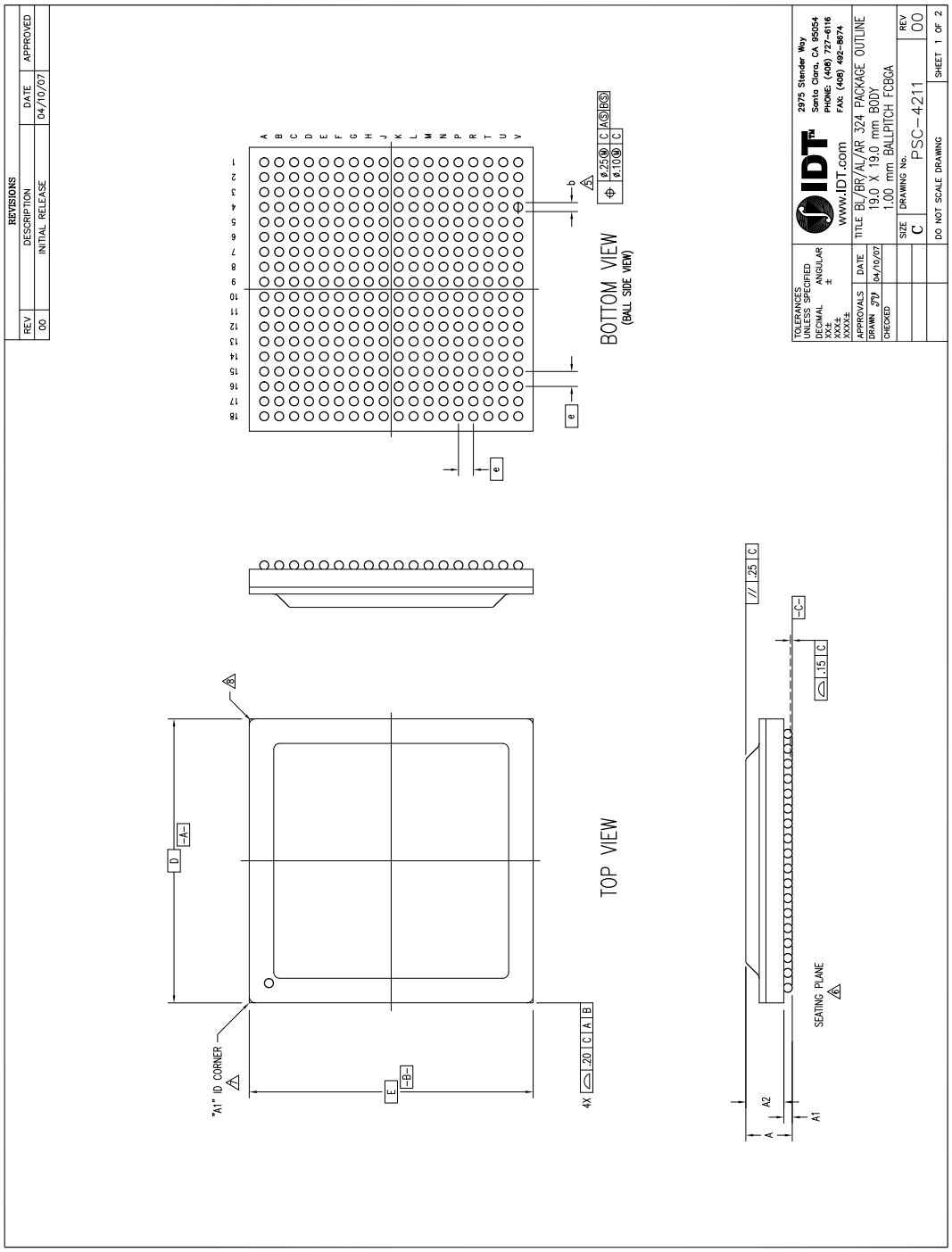
Signal Name	Conductor Length (microns)
PE4TN00	12116.40
PE4TP00	12168.24
PE4TN01	12011.65
PE4TP01	12035.01
PE4TN02	12731.79
PE4TP02	12864.34
PE4TN03	11571.96
PE4TP03	11712.79
PE5RN00	3155.78
PE5RP00	3508.24
PE5RN01	2200.39
PE5RP01	2545.56
PE5RN02	1838.19
PE5RP02	2171.00
PE5RN03	2126.08
PE5RP03	2467.21
PE5TN00	7480.71
PE5TP00	7630.60
PE5TN01	5329.03
PE5TP01	5422.12
PE5TN02	5244.03
PE5TP02	5302.02
PE5TN03	4991.19
PE5TP03	5127.88
PE0REFCLKN	12558.62
PE0REFCLKP	12641.05

Table 26 Signal Trace Length (Part 3 of 3)

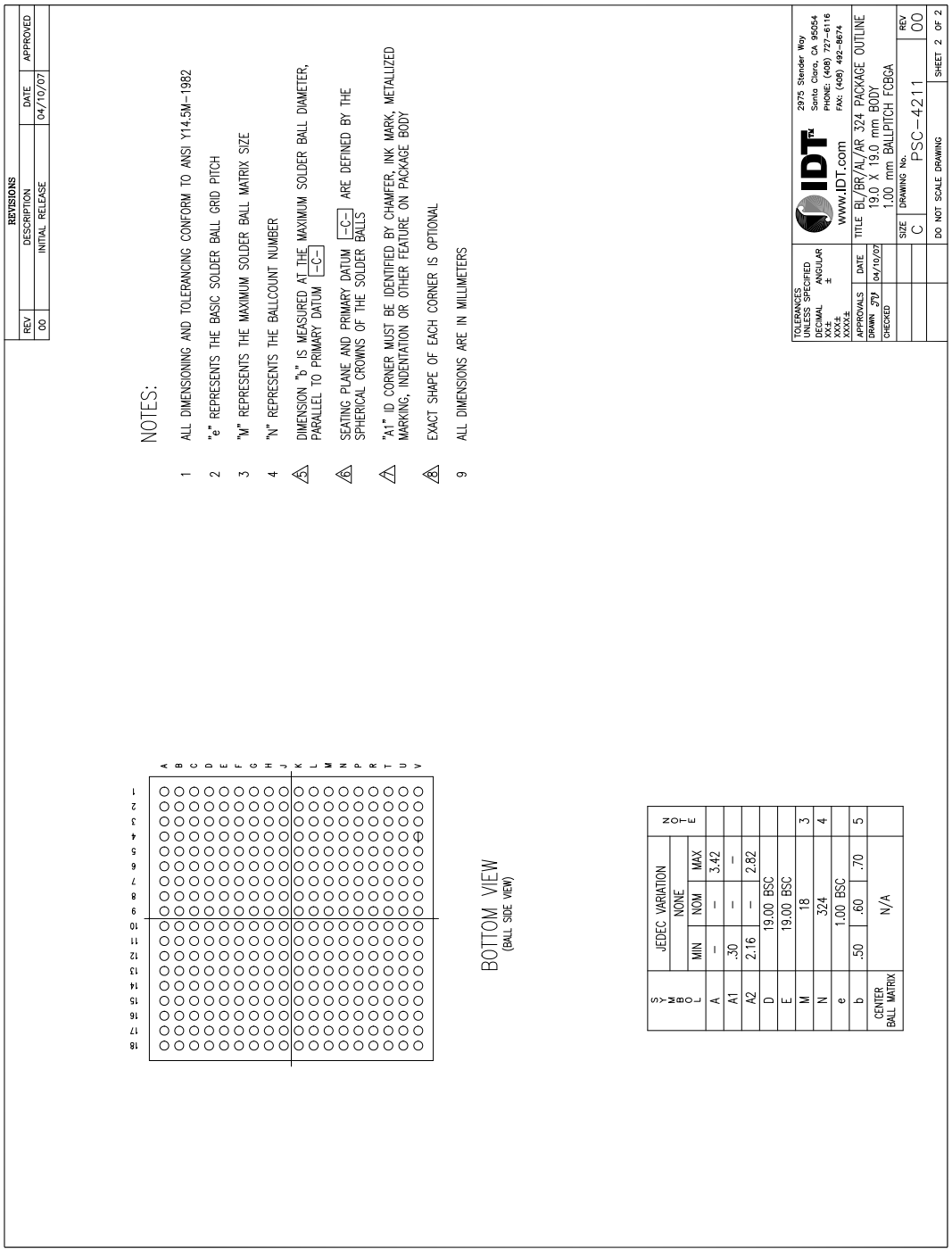
Option A Package Pinout — Top View



Option A Package Drawing — 324-Pin AL324/ALG324



Option A Package Drawing — Page Two



Option B Package Pinout, 27x27mm 676-BGA Signal Pinout

The following table lists the pin numbers and signal names for the PES24T6G2 (27x27mm) device.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	V_{SS}		B9	MSMBDAT		C17	V_{DD}I/O		D25	V_{SS}	
A2	V_{SS}		B10	SSMBADDR_2		C18	V_{SS}		D26	NC	
A3	V_{DD}I/O		B11	SSMBADDR_5		C19	V_{DD}I/O		E1	V_{SS}	
A4	JTAG_TDI		B12	SSMBDAT		C20	V_{SS}		E2	V_{SS}	
A5	JTAG_TMS		B13	V_{SS}		C21	V_{DD}I/O		E3	V_{SS}	
A6	MSMBADDR_1		B14	SWMODE_0		C22	GPIO_10	1	E4	V_{SS}	
A7	MSMBADDR_3		B15	SWMODE_2		C23	V_{DD}I/O		E5	P01MERGEN	
A8	MSMBCLK		B16	V_{SS}		C24	V_{SS}		E6	V_{DD}CORE	
A9	SSMBADDR_1		B17	V_{DD}I/O		C25	V_{SS}		E7	V_{DD}CORE	
A10	SSMBADDR_3		B18	GPIO_00	1	C26	NC		E8	V_{SS}	
A11	SSMBCLK		B19	GPIO_02	1	D1	PEREFCLKP1		E9	V_{DD}CORE	
A12	CCLKUS		B20	GPIO_04	1	D2	V_{SS}		E10	V_{SS}	
A13	CCLKDS		B21	GPIO_06		D3	V_{SS}		E11	V_{DD}CORE	
A14	V_{SS}		B22	MSMBSMODE		D4	P45MERGEN		E12	V_{SS}	
A15	SWMODE_1		B23	REFCLKM		D5	V_{DD}CORE		E13	V_{DD}CORE	
A16	NC		B24	V_{DD}I/O		D6	V_{DD}CORE		E14	V_{SS}	
A17	PERSTN		B25	V_{SS}		D7	V_{SS}		E15	V_{DD}CORE	
A18	RSTHALT		B26	V_{SS}		D8	V_{DD}CORE		E16	V_{SS}	
A19	GPIO_01	1	C1	PEREFCLKN1		D9	V_{SS}		E17	V_{DD}CORE	
A20	GPIO_03	1	C2	V_{SS}		D10	V_{DD}CORE		E18	V_{SS}	
A21	GPIO_05	1	C3	P23MERGEN		D11	V_{SS}		E19	V_{DD}CORE	
A22	GPIO_07	1	C4	V_{DD}CORE		D12	V_{DD}CORE		E20	V_{DD}CORE	
A23	V_{SS}		C5	V_{DD}I/O		D13	V_{DD}CORE		E21	V_{DD}CORE	
A24	GPIO_09	1	C6	V_{SS}		D14	V_{SS}		E22	V_{SS}	
A25	V_{SS}		C7	V_{DD}I/O		D15	V_{DD}CORE		E23	V_{SS}	
A26	V_{SS}		C8	V_{SS}		D16	V_{SS}		E24	V_{SS}	
B1	V_{SS}		C9	V_{DD}I/O		D17	V_{DD}CORE		E25	V_{SS}	
B2	V_{SS}		C10	V_{SS}		D18	V_{DD}CORE		E26	V_{SS}	
B3	V_{DD}I/O		C11	V_{DD}I/O		D19	V_{DD}CORE		F1	V_{DD}CORE	
B4	JTAG_TCK		C12	V_{SS}		D20	V_{SS}		F2	V_{DD}CORE	
B5	JTAG_TDO		C13	V_{DD}I/O		D21	V_{DD}CORE		F3	V_{DD}PEA	
B6	JTAG_TRST_N		C14	V_{DD}CORE		D22	V_{DD}CORE		F4	V_{SS}	
B7	MSMBADDR_2		C15	V_{DD}I/O		D23	GPIO_08	1	F5	V_{SS}	
B8	MSMBADDR_4		C16	V_{DD}CORE		D24	V_{SS}		F6	V_{DD}I/O	

Table 27 PES24T6G2 (27x27mm 676-Pin) Signal Pin-Out (Part 1 of 5)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
F7	V_{SS}		G18	V_{SS}		J3	V_{DD}PETA		K14	V_{SS}	
F8	V_{SS}		G19	V_{SS}		J4	PE3RN02		K15	V_{DD}CORE	
F9	V_{SS}		G20	V_{SS}		J5	PE3RP02		K16	V_{DD}CORE	
F10	V_{SS}		G21	V_{SS}		J6	V_{SS}		K17	V_{SS}	
F11	V_{SS}		G22	PE4RP00		J7	V_{DD}CORE		K18	V_{SS}	
F12	NC		G23	PE4RN00		J8	V_{DD}CORE		K19	V_{DD}CORE	
F13	V_{SS}		G24	V_{DD}PETA		J9	V_{SS}		K20	V_{DD}CORE	
F14	V_{SS}		G25	PE4TP00		J10	V_{SS}		K21	V_{SS}	
F15	V_{SS}		G26	PE4TN00		J11	V_{DD}CORE		K22	V_{DD}PEA	
F16	NC		H1	V_{SS}		J12	V_{DD}CORE		K23	V_{DD}PEA	
F17	V_{SS}		H2	V_{SS}		J13	V_{SS}		K24	V_{DD}PEA	
F18	V_{SS}		H3	V_{DD}PEHA		J14	V_{SS}		K25	V_{SS}	
F19	V_{SS}		H4	V_{DD}PEHA		J15	V_{DD}CORE		K26	REFRES4	
F20	V_{SS}		H5	V_{SS}		J16	V_{DD}CORE		L1	PE3TN01	
F21	V_{SS}		H6	V_{SS}		J17	V_{SS}		L2	PE3TP01	
F22	V_{SS}		H7	V_{DD}CORE		J18	V_{SS}		L3	V_{DD}PETA	
F23	V_{SS}		H8	V_{DD}CORE		J19	V_{DD}CORE		L4	PE3RN01	
F24	V_{DD}PEA		H9	V_{SS}		J20	V_{DD}CORE		L5	PE3RP01	
F25	V_{DD}CORE		H10	V_{SS}		J21	V_{SS}		L6	V_{SS}	
F26	V_{DD}CORE		H11	V_{DD}CORE		J22	PE4RP01		L7	V_{DD}CORE	
G1	PE3TN03		H12	V_{DD}CORE		J23	PE4RN01		L8	V_{DD}CORE	
G2	PE3TP03		H13	V_{SS}		J24	V_{DD}PETA		L9	V_{SS}	
G3	V_{DD}PETA		H14	V_{SS}		J25	PE4TP01		L10	V_{SS}	
G4	PE3RN03		H15	V_{DD}CORE		J26	PE4TN01		L11	V_{DD}CORE	
G5	PE3RP03		H16	V_{DD}CORE		K1	REFRES3		L12	V_{DD}CORE	
G6	V_{SS}		H17	V_{SS}		K2	V_{SS}		L13	V_{SS}	
G7	V_{SS}		H18	V_{SS}		K3	V_{DD}PEA		L14	V_{SS}	
G8	V_{SS}		H19	V_{DD}CORE		K4	V_{DD}PEA		L15	V_{DD}CORE	
G9	V_{SS}		H20	V_{DD}CORE		K5	V_{DD}PEA		L16	V_{DD}CORE	
G10	V_{SS}		H21	V_{SS}		K6	V_{SS}		L17	V_{SS}	
G11	V_{SS}		H22	V_{SS}		K7	V_{DD}CORE		L18	V_{SS}	
G12	V_{SS}		H23	V_{DD}PEHA		K8	V_{DD}CORE		L19	V_{DD}CORE	
G13	V_{SS}		H24	V_{DD}PEHA		K9	V_{SS}		L20	V_{DD}CORE	
G14	V_{SS}		H25	V_{SS}		K10	V_{SS}		L21	V_{SS}	
G15	V_{SS}		H26	V_{SS}		K11	V_{DD}CORE		L22	PE4RP02	
G16	V_{SS}		J1	PE3TN02		K12	V_{DD}CORE		L23	PE4RN02	
G17	V_{SS}		J2	PE3TP02		K13	V_{SS}		L24	V_{DD}PETA	

Table 27 PES24T6G2 (27x27mm 676-Pin) Signal Pin-Out (Part 2 of 5)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
L25	PE4TP02		N10	V_{SS}		P21	V_{SS}		T6	NC	
L26	PE4TN02		N11	V_{DD}CORE		P22	V_{SS}		T7	V_{DD}CORE	
M1	V_{DD}CORE		N12	V_{DD}CORE		P23	V_{DD}PEHA		T8	V_{DD}CORE	
M2	V_{SS}		N13	V_{SS}		P24	V_{DD}PEHA		T9	V_{SS}	
M3	V_{DD}PEHA		N14	V_{SS}		P25	V_{SS}		T10	V_{SS}	
M4	V_{DD}PEHA		N15	V_{DD}CORE		P26	V_{DD}CORE		T11	V_{DD}CORE	
M5	V_{SS}		N16	V_{DD}CORE		R1	PE2TN03		T12	V_{DD}CORE	
M6	NC		N17	V_{SS}		R2	PE2TP03		T13	V_{SS}	
M7	V_{DD}CORE		N18	V_{SS}		R3	V_{DD}PETA		T14	V_{SS}	
M8	V_{DD}CORE		N19	V_{DD}CORE		R4	PE2RN03		T15	V_{DD}CORE	
M9	V_{SS}		N20	V_{DD}CORE		R5	PE2RP03		T16	V_{DD}CORE	
M10	V_{SS}		N21	V_{SS}		R6	V_{SS}		T17	V_{SS}	
M11	V_{DD}CORE		N22	PE4RP03		R7	V_{DD}CORE		T18	V_{SS}	
M12	V_{DD}CORE		N23	PE4RN03		R8	V_{DD}CORE		T19	V_{DD}CORE	
M13	V_{SS}		N24	V_{DD}PETA		R9	V_{SS}		T20	V_{DD}CORE	
M14	V_{SS}		N25	PE4TP03		R10	V_{SS}		T21	NC	
M15	V_{DD}CORE		N26	PE4TN03		R11	V_{DD}CORE		T22	V_{SS}	
M16	V_{DD}CORE		P1	V_{DD}CORE		R12	V_{DD}CORE		T23	V_{DD}PEA	
M17	V_{SS}		P2	V_{SS}		R13	V_{SS}		T24	V_{DD}PEA	
M18	V_{SS}		P3	V_{DD}PEHA		R14	V_{SS}		T25	V_{SS}	
M19	V_{DD}CORE		P4	V_{DD}PEHA		R15	V_{DD}CORE		T26	V_{DD}CORE	
M20	V_{DD}CORE		P5	V_{SS}		R16	V_{DD}CORE		U1	PE2TN02	
M21	NC		P6	V_{SS}		R17	V_{SS}		U2	PE2TP02	
M22	V_{SS}		P7	V_{DD}CORE		R18	V_{SS}		U3	V_{DD}PETA	
M23	V_{DD}PEHA		P8	V_{DD}CORE		R19	V_{DD}CORE		U4	PE2RN02	
M24	V_{DD}PEHA		P9	V_{SS}		R20	V_{DD}CORE		U5	PE2RP02	
M25	V_{SS}		P10	V_{SS}		R21	V_{SS}		U6	V_{SS}	
M26	V_{DD}CORE		P11	V_{DD}CORE		R22	PE5RP00		U7	V_{DD}CORE	
N1	PE3TN00		P12	V_{DD}CORE		R23	PE5RN00		U8	V_{DD}CORE	
N2	PE3TP00		P13	V_{SS}		R24	V_{DD}PETA		U9	V_{SS}	
N3	V_{DD}PETA		P14	V_{SS}		R25	PE5TP00		U10	V_{SS}	
N4	PE3RN00		P15	V_{DD}CORE		R26	PE5TN00		U11	V_{DD}CORE	
N5	PE3RP00		P16	V_{DD}CORE		T1	V_{DD}CORE		U12	V_{DD}CORE	
N6	V_{SS}		P17	V_{SS}		T2	V_{SS}		U13	V_{SS}	
N7	V_{DD}CORE		P18	V_{SS}		T3	V_{DD}PEA		U14	V_{SS}	
N8	V_{DD}CORE		P19	V_{DD}CORE		T4	V_{DD}PEA		U15	V_{DD}CORE	
N9	V_{SS}		P20	V_{DD}CORE		T5	V_{SS}		U16	V_{DD}CORE	

Table 27 PES24T6G2 (27x27mm 676-Pin) Signal Pin-Out (Part 3 of 5)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
U17	V_{SS}		W2	PE2TP01		Y13	V_{SS}		AA24	V_{DD}PETA	
U18	V_{SS}		W3	V_{DD}PETA		Y14	V_{SS}		AA25	PE5TP03	
U19	V_{DD}CORE		W4	PE2RN01		Y15	V_{DD}CORE		AA26	PE5TN03	
U20	V_{DD}CORE		W5	PE2RP01		Y16	V_{DD}CORE		AB1	V_{SS}	
U21	V_{SS}		W6	V_{SS}		Y17	V_{SS}		AB2	V_{SS}	
U22	PE5RP01		W7	V_{DD}CORE		Y18	V_{SS}		AB3	V_{DD}CORE	
U23	PE5RN01		W8	V_{DD}CORE		Y19	V_{DD}CORE		AB4	V_{DD}CORE	
U24	V_{DD}PETA		W9	V_{SS}		Y20	V_{DD}CORE		AB5	V_{DD}CORE	
U25	PE5TP01		W10	V_{SS}		Y21	V_{SS}		AB6	V_{SS}	
U26	PE5TN01		W11	V_{DD}CORE		Y22	V_{SS}		AB7	PE1RP03	
V1	V_{DD}CORE		W12	V_{DD}CORE		Y23	V_{DD}PEHA		AB8	V_{SS}	
V2	V_{SS}		W13	V_{SS}		Y24	V_{DD}PEHA		AB9	PE1RP02	
V3	V_{DD}PEA		W14	V_{SS}		Y25	V_{SS}		AB10	V_{DD}PEA	
V4	V_{DD}PEA		W15	V_{DD}CORE		Y26	REFRES5		AB11	PE1RP01	
V5	V_{DD}PEA		W16	V_{DD}CORE		AA1	PE2TN00		AB12	V_{SS}	
V6	V_{SS}		W17	V_{SS}		AA2	PE2TP00		AB13	PE1RP00	
V7	V_{DD}CORE		W18	V_{SS}		AA3	V_{DD}PETA		AB14	V_{DD}PEA	
V8	V_{DD}CORE		W19	V_{DD}CORE		AA4	PE2RN00		AB15	PE0RP03	
V9	V_{SS}		W20	V_{DD}CORE		AA5	PE2RP00		AB16	V_{SS}	
V10	V_{SS}		W21	V_{SS}		AA6	V_{SS}		AB17	PE0RP02	
V11	V_{DD}CORE		W22	PE5RP02		AA7	V_{SS}		AB18	V_{DD}PEA	
V12	V_{DD}CORE		W23	PE5RN02		AA8	V_{SS}		AB19	PE0RP01	
V13	V_{SS}		W24	V_{DD}PETA		AA9	V_{SS}		AB20	V_{SS}	
V14	V_{SS}		W25	PE5TP02		AA10	V_{SS}		AB21	PE0RP00	
V15	V_{DD}CORE		W26	PE5TN02		AA11	V_{SS}		AB22	V_{SS}	
V16	V_{DD}CORE		Y1	REFRES2		AA12	NC		AB23	V_{DD}CORE	
V17	V_{SS}		Y2	V_{SS}		AA13	V_{SS}		AB24	V_{DD}CORE	
V18	V_{SS}		Y3	V_{DD}PEHA		AA14	V_{SS}		AB25	V_{SS}	
V19	V_{DD}CORE		Y4	V_{DD}PEHA		AA15	V_{SS}		AB26	V_{SS}	
V20	V_{DD}CORE		Y5	V_{SS}		AA16	NC		AC1	V_{SS}	
V21	V_{SS}		Y6	V_{SS}		AA17	V_{SS}		AC2	V_{SS}	
V22	V_{DD}PEA		Y7	V_{DD}CORE		AA18	V_{SS}		AC3	V_{DD}CORE	
V23	V_{DD}PEA		Y8	V_{DD}CORE		AA19	V_{SS}		AC4	V_{DD}CORE	
V24	V_{DD}PEA		Y9	V_{SS}		AA20	V_{SS}		AC5	V_{DD}CORE	
V25	V_{SS}		Y10	V_{SS}		AA21	V_{SS}		AC6	V_{DD}PEHA	
V26	V_{DD}CORE		Y11	V_{DD}CORE		AA22	PE5RP03		AC7	PE1RN03	
W1	PE2TN01		Y12	V_{DD}CORE		AA23	PE5RN03		AC8	V_{DD}PEA	

Table 27 PES24T6G2 (27x27mm 676-Pin) Signal Pin-Out (Part 4 of 5)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
AC9	PE1RN02		AD7	V_{SS}		AE5	V_{SS}		AF3	V_{DD}CORE	
AC10	V_{DD}PEA		AD8	V_{DD}PETA		AE6	V_{SS}		AF4	V_{DD}CORE	
AC11	PE1RN01		AD9	V_{SS}		AE7	PE1TP03		AF5	V_{DD}CORE	
AC12	V_{DD}PEHA		AD10	V_{DD}PETA		AE8	V_{SS}		AF6	V_{SS}	
AC13	PE1RN00		AD11	V_{DD}PETA		AE9	PE1TP02		AF7	PE1TN03	
AC14	V_{DD}PEHA		AD12	V_{DD}PEHA		AE10	V_{SS}		AF8	REFRES1	
AC15	PE0RN03		AD13	V_{DD}PETA		AE11	PE1TP01		AF9	PE1TN02	
AC16	V_{DD}PEA		AD14	V_{DD}PEHA		AE12	V_{SS}		AF10	V_{DD}CORE	
AC17	PE0RN02		AD15	V_{DD}PETA		AE13	PE1TP00		AF11	PE1TN01	
AC18	V_{DD}PEA		AD16	V_{DD}PEA		AE14	V_{SS}		AF12	V_{DD}CORE	
AC19	PE0RN01		AD17	V_{SS}		AE15	PE0TP03		AF13	PE1TN00	
AC20	V_{DD}PEHA		AD18	V_{DD}PETA		AE16	V_{SS}		AF14	V_{DD}CORE	
AC21	PE0RN00		AD19	V_{DD}PETA		AE17	PE0TP02		AF15	PE0TN03	
AC22	V_{SS}		AD20	V_{DD}PEHA		AE18	V_{SS}		AF16	V_{DD}CORE	
AC23	V_{DD}CORE		AD21	V_{DD}PETA		AE19	PE0TP01		AF17	PE0TN02	
AC24	V_{DD}CORE		AD22	V_{SS}		AE20	V_{SS}		AF18	REFRES0	
AC25	V_{SS}		AD23	V_{DD}CORE		AE21	PE0TP00		AF19	PE0TN01	
AC26	V_{SS}		AD24	V_{DD}CORE		AE22	V_{SS}		AF20	V_{SS}	
AD1	V_{SS}		AD25	V_{SS}		AE23	V_{DD}CORE		AF21	PE0TN00	
AD2	V_{SS}		AD26	V_{SS}		AE24	V_{DD}CORE		AF22	V_{SS}	
AD3	V_{DD}CORE		AE1	V_{SS}		AE25	V_{SS}		AF23	V_{DD}CORE	
AD4	V_{DD}CORE		AE2	V_{SS}		AE26	V_{SS}		AF24	V_{DD}CORE	
AD5	V_{DD}CORE		AE3	V_{DD}CORE		AF1	V_{SS}		AF25	V_{SS}	
AD6	V_{DD}PEHA		AE4	V_{DD}CORE		AF2	V_{SS}		AF26	V_{SS}	

Table 27 PES24T6G2 (27x27mm 676-Pin) Signal Pin-Out (Part 5 of 5)

Option B Package — Core Power Pins

V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}Core	V_{DD}Core
C4	H16	M19	T15	Y12
C14	H19	M20	T16	Y15
C16	H20	M26	T19	Y16
D5	J7	N7	T20	Y19
D6	J8	N8	T26	Y20
D8	J11	N11	U7	AB3
D10	J12	N12	U8	AB4
D12	J15	N15	U11	AB5
D13	J16	N16	U12	AB23
D15	J19	N19	U15	AB24
D17	J20	N20	U16	AC3
D18	K7	P1	U19	AC4
D19	K8	P7	U20	AC5
D21	K11	P8	V1	AC23
D22	K12	P11	V7	AC24
E6	K15	P12	V8	AD3
E7	K16	P15	V11	AD4
E9	K19	P16	V12	AD5
E11	K20	P19	V15	AD23
E13	L7	P29	V16	AD24
E15	L8	P26	V19	AE3
E17	L11	R7	V20	AE4
E19	L12	R8	V26	AE23
E20	L15	R11	W7	AE24
E21	L16	R12	W8	AF3
F1	L19	R15	W11	AF4
F2	L20	R16	W12	AF5
F25	M1	R19	W15	AF10
F26	M7	R20	W16	AF12
H7	M8	T1	W19	AF14
H8	M11	T7	W20	AF16
H11	M12	T8	Y7	AF23
H12	M15	T11	Y8	AF24
H15	M16	T12	Y11	

Table 28 PES24T6G2 (27x27mm 676-Pin) Core Power Pins

Option B Package — I/O, PCIe, and Transmitter Power Pins

$V_{DD}I/O$	$V_{DD}PEA$	$V_{DD}PEHA$	$V_{DD}PETA$
A3	F3	H3	G3
B3	F24	H4	G24
B17	K3	H23	J3
B24	K4	H24	J24
C5	K5	M3	L3
C7	K22	M4	L24
C9	K23	M23	N3
C11	K24	M24	N24
C13	T3	P3	R3
C15	T4	P4	R24
C17	T23	P23	U3
C19	T24	P24	U24
C21	V3	Y3	W3
C23	V4	Y4	W24
F6	V5	Y23	AA3
	V22	Y24	AA24
	V23	AC6	AD8
	V24	AC12	AD10
	AB10	AC14	AD11
	AB14	AC20	AD13
	AB18	AD6	AD15
	AC8	AD12	AD18
	AC10	AD14	AD19
	AC16	AD20	AD21
	AC18		1.
	AD16		

Table 29 PES24T6G2 (27x27mm 676-Pin) I/O, PCIe, and Transmitter Power Pins

Option B Package — Ground Pins

V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
A1	E3	G9	J18	N13	T22	Y13	AC22
A2	E4	G10	J21	N14	T25	Y14	AC25
A14	E8	G11	K2	N17	U6	Y17	AC26
A23	E10	G12	K6	N18	U9	Y18	AD1
A25	E12	G13	K9	N21	U10	Y21	AD2
A26	E14	G14	K10	P2	U13	Y22	AD7
B1	E16	G15	K13	P5	U14	Y25	AD9
B2	E18	G16	K14	P6	U17	AA6	AD17
B13	E22	G17	K17	P9	U18	AA7	AD22
B16	E23	G18	K18	P10	U21	AA8	AD25
B25	E24	G19	K21	P13	V2	AA9	AD26
B26	E25	G20	K25	P14	V6	AA10	AE1
C2	E26	G21	L6	P17	V9	AA11	AE2
C6	F4	H1	L9	P18	V10	AA13	AE5
C8	F5	H2	L10	P21	V13	AA14	AE6
C10	F7	H5	L13	P22	V14	AA15	AE8
C12	F8	H6	L14	P25	V17	AA17	AE10
C18	F9	H9	L17	R6	V18	AA18	AE12
C20	F10	H10	L18	R9	V21	AA19	AE14
C24	F11	H13	L21	R10	V25	AA20	AE16
C25	F13	H14	M2	R13	W6	AA21	AE18
D2	F14	H17	M5	R14	W9	AB1	AE20
D3	F15	H18	M9	R17	W10	AB2	AE22
D7	F17	H21	M10	R18	W13	AB6	AE25
D9	F18	H22	M13	R21	W14	AB8	AE26
D11	F19	H25	M14	T2	W17	AB12	AF1
D14	F20	H26	M17	T5	W18	AB16	AF2
D16	F21	J6	M18	T9	W21	AB20	AF6
D20	F22	J9	M22	T10	Y2	AB22	AF20
D24	F23	J10	M25	T13	Y5	AB25	AF22
D25	G6	J13	N6	T14	Y6	AB26	AF25
E1	G7	J14	N9	T17	Y9	AC1	AF26
E2	G8	J17	N10	T18	Y10	AC2	

Table 30 PES24T6G2 (27x27mm 676-Pin) Ground Pins

Option B Package — Alternate Signal Functions

Pin	GPIO	Alternate
B18	GPIO[0]	P2RSTN
A19	GPIO[1]	P4RSTN
B19	GPIO[2]	IOEXPINTN0
A20	GPIO[3]	IOEXPINTN1
B20	GPIO[4]	IOEXPINTN2
A21	GPIO[5]	IOEXPINTN3
A22	GPIO[7]	GPEN
D23	GPIO[8]	P1RSTN
A24	GPIO[9]	P3RSTN
C22	GPIO[10]	P5RSTN

Table 31 PES24T6G2 (27x27mm 676-Pin) Alternate Signal Functions

Option B Package — No Connection Pins

NC Pins
A16
C26
D26
F12
F16
M6
M21
T6
T21
AA12
AA16

Table 32 PES24T6G2 (27x27mm 676-Pin) No Connection Pins

Option B Package — Signals Listed Alphabetically

Signal Name	I/O Type	Location	Signal Category
CCLKDS	I	A13	System
CCLKUS	I	A12	
GPIO_00	I/O	B18	General Purpose Input/Output
GPIO_01	I/O	A19	
GPIO_02	I/O	B19	
GPIO_03	I/O	A20	
GPIO_04	I/O	B20	
GPIO_05	I/O	A21	
GPIO_06	I/O	B21	
GPIO_07	I/O	A22	
GPIO_08	I/O	D23	
GPIO_09	I/O	A24	
GPIO_10	I/O	C22	
JTAG_TCK	I	B4	JTAG
JTAG_TDI	I	A4	
JTAG_TDO	O	B5	
JTAG_TMS	I	A5	
JTAG_TRST_N	I	B6	
MSMBADDR_1	I	A6	SMBus
MSMBADDR_2	I	B7	
MSMBADDR_3	I	A7	
MSMBADDR_4	I	B8	
MSMBCLK	I/O	A8	
MSMBDAT	I/O	B9	
MSMBSMODE	I	B22	System
NO CONNECTION	See Table 32 for a list of No Connect pins.		
P01MERGEN	I	E5	System
P23MERGEN	I	C3	
P45MERGEN	I	D4	

Table 33 PES24T6G2 (27x27mm 676-Pin) Alphabetical Signal List (Part 1 of 5)

Signal Name	I/O Type	Location	Signal Category
PE0RN00	I	AC21	PCI Express
PE0RN01	I	AC19	
PE0RN02	I	AC17	
PE0RN03	I	AC15	
PE0RP00	I	AB21	
PE0RP01	I	AB19	
PE0RP02	I	AB17	
PE0RP03	I	AB15	
PE0TN00	O	AF21	
PE0TN01	O	AF19	
PE0TN02	O	AF17	
PE0TN03	O	AF15	
PE0TP00	O	AE21	
PE0TP01	O	AE19	
PE0TP02	O	AE17	
PE0TP03	O	AE15	
PE1RN00	I	AC13	
PE1RN01	I	AC11	
PE1RN02	I	AC9	
PE1RN03	I	AC7	
PE1RP00	I	AB13	
PE1RP01	I	AB11	
PE1RP02	I	AB9	
PE1RP03	I	AB7	
PE1TN00	O	AF13	
PE1TN01	O	AF11	
PE1TN02	O	AF9	
PE1TN03	O	AF7	
PE1TP00	O	AE13	
PE1TP01	O	AE11	
PE1TP02	O	AE9	
PE1TP03	O	AE7	
PE2RN00	I	AA4	
PE2RN01	I	W4	
PE2RN02	I	U4	
PE2RN03	I	R4	

Table 33 PES24T6G2 (27x27mm 676-Pin) Alphabetical Signal List (Part 2 of 5)

Signal Name	I/O Type	Location	Signal Category
PE2RP00	I	AA5	PCI Express (cont.)
PE2RP01	I	W5	
PE2RP02	I	U5	
PE2RP03	I	R5	
PE2TN00	O	AA1	
PE2TN01	O	W1	
PE2TN02	O	U1	
PE2TN03	O	R1	
PE2TP00	O	AA2	
PE2TP01	O	W2	
PE2TP02	O	U2	
PE2TP03	O	R2	
PE3RN00	I	N4	
PE3RN01	I	L4	
PE3RN02	I	J4	
PE3RN03	I	G4	
PE3RP00	I	N5	
PE3RP01	I	L5	
PE3RP02	I	J5	
PE3RP03	I	G5	
PE3TN00	O	N1	
PE3TN01	O	L1	
PE3TN02	O	J1	
PE3TN03	O	G1	
PE3TP00	O	N2	
PE3TP01	O	L2	
PE3TP02	O	J2	
PE3TP03	O	G2	
PE4RN00	I	G23	
PE4RN01	I	J23	
PE4RN02	I	L23	
PE4RN03	I	N23	
PE4RP00	I	G22	
PE4RP01	I	J22	
PE4RP02	I	L22	
PE4RP03	I	N22	

Table 33 PES24T6G2 (27x27mm 676-Pin) Alphabetical Signal List (Part 3 of 5)

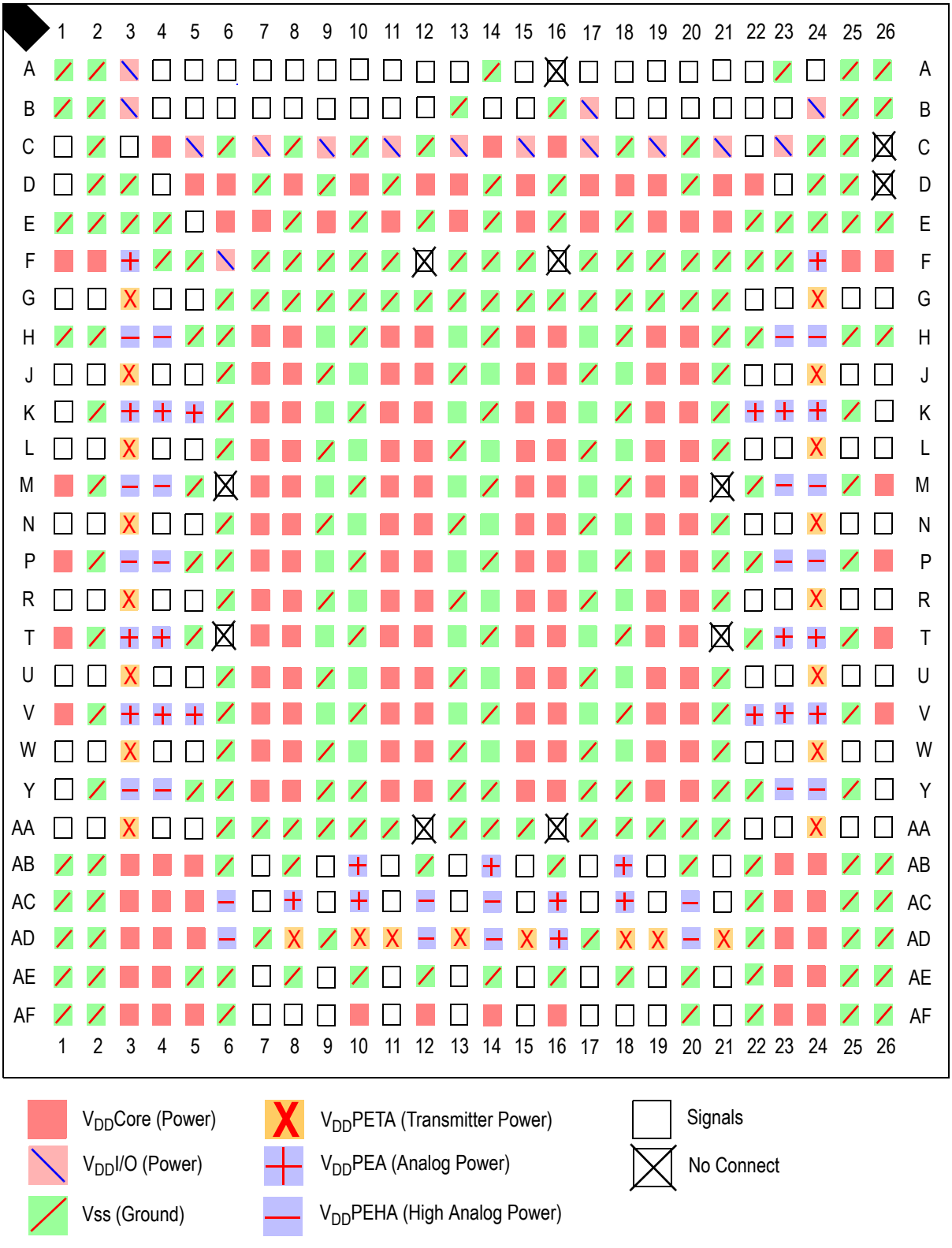
Signal Name	I/O Type	Location	Signal Category
PE4TN00	O	G26	PCI Express (cont.)
PE4TN01	O	J26	
PE4TN02	O	L26	
PE4TN03	O	N26	
PE4TP00	O	G25	
PE4TP01	O	J25	
PE4TP02	O	L25	
PE4TP03	O	N25	
PE5RN00	I	R23	
PE5RN01	I	U23	
PE5RN02	I	W23	
PE5RN03	I	AA23	
PE5RP00	I	R22	
PE5RP01	I	U22	
PE5RP02	I	W22	
PE5RP03	I	AA22	
PE5TN00	O	R26	
PE5TN01	O	U26	
PE5TN02	O	W26	
PE5TN03	O	AA26	
PE5TP00	O	R25	
PE5TP01	O	U25	
PE5TP02	O	W25	
PE5TP03	O	AA25	
PEREFCLKN	I	C1	
PEREFCLKP	I	D1	
PERSTN	I	A17	System
REFCLKM	I	B23	PCI Express
REFRES0	I/O	AF18	SerDes Reference Resistors
REFRES1	I/O	AF8	
REFRES2	I/O	Y1	
REFRES3	I/O	K1	
REFRES4	I/O	K26	
REFRES5	I/O	Y26	
RSTHALT	I	A18	System

Table 33 PES24T6G2 (27x27mm 676-Pin) Alphabetical Signal List (Part 4 of 5)

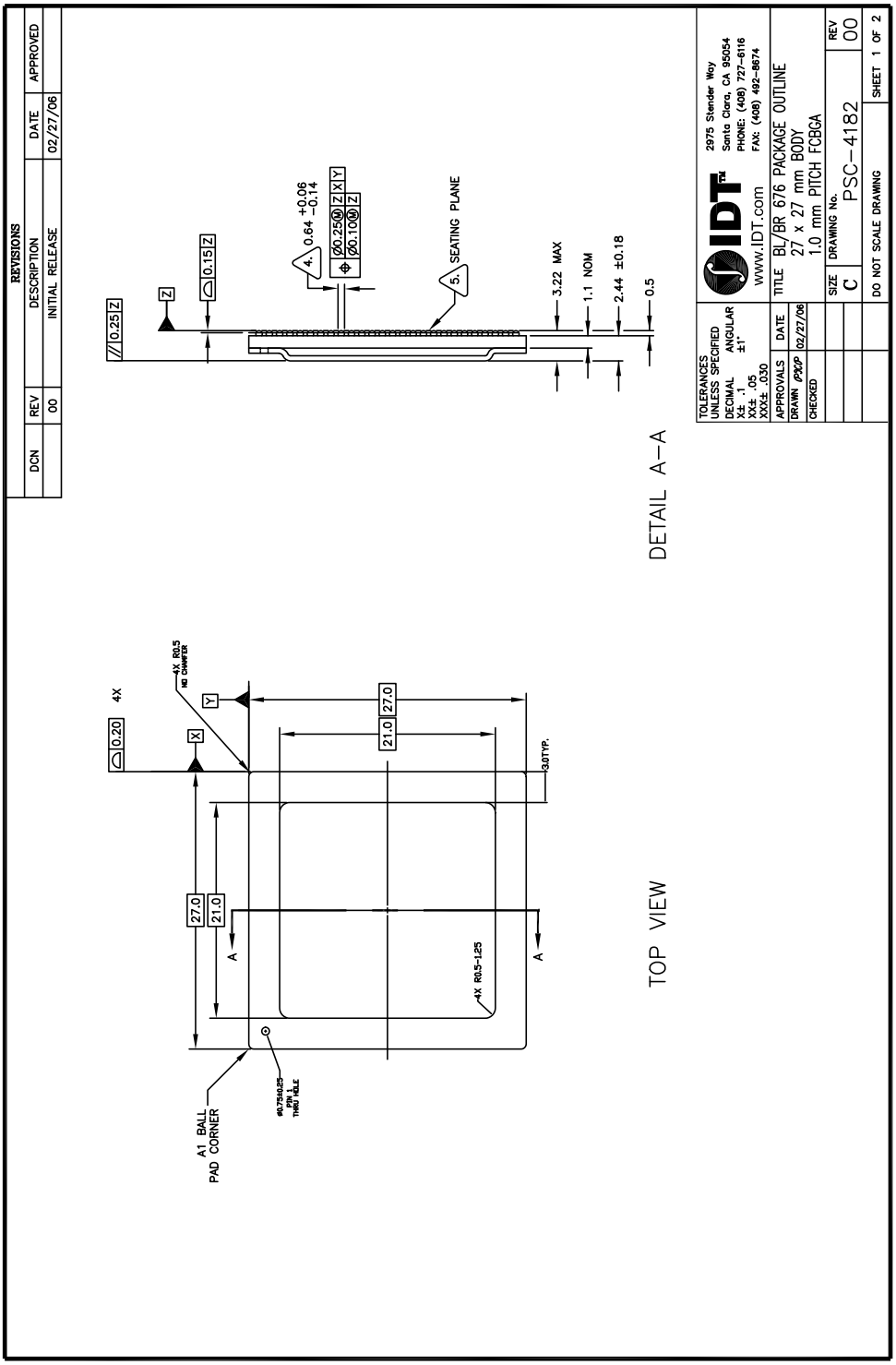
Signal Name	I/O Type	Location	Signal Category
SSMBADDR_1	I	A9	SMBus
SSMBADDR_2	I	B10	
SSMBADDR_3	I	A10	
SSMBADDR_5	I	B11	
SSMBCLK	I/O	A11	
SSMBDAT	I/O	B12	
SWMODE_0	I	B14	System
SWMODE_1	I	A15	
SWMODE_2	I	B15	
V_{DD}CORE, V_{DD}I/O, V_{DD}PEA, V_{DD}PEHA, V_{DD}PETA	See Tables 28 and 29 for a listing of power pins.		
V_{SS}	See Table 30 for a listing of ground pins.		

Table 33 PES24T6G2 (27x27mm 676-Pin) Alphabetical Signal List (Part 5 of 5)

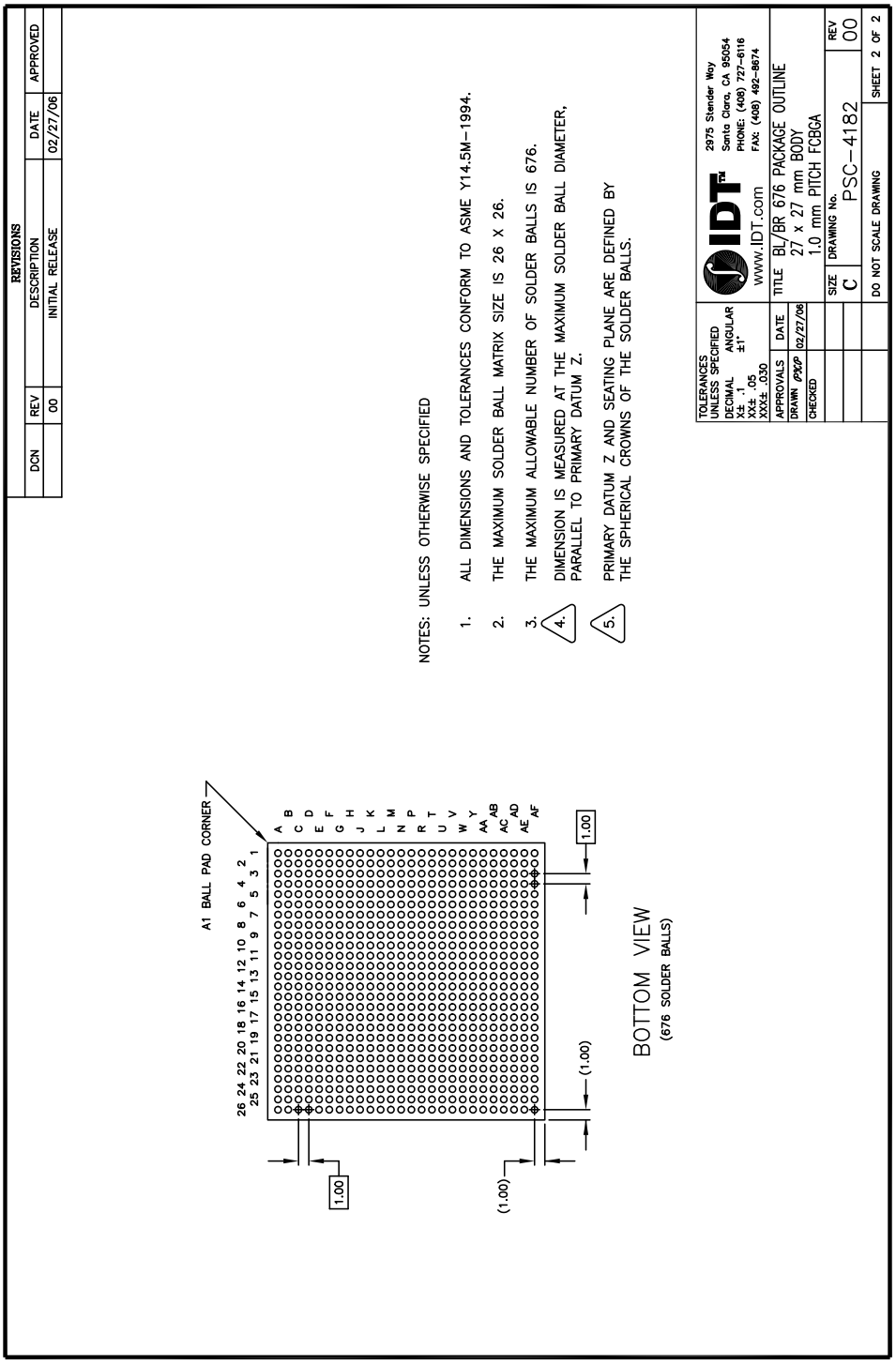
Option B Package Pinout — Top View



Option B Package Drawing — 676-Pin BL676/BLG676



Option B Package Drawing — Page Two



Revision History

January 15, 2009: Publication of final data sheet.

February 11, 2009: Revised AC Timing Characteristics table and DC Electrical Characteristics table to correct typos.

March 6, 2009: Added industrial temperature.

April 7, 2009: In Valid Combinations, changed ZB to ZC silicon for commercial temperature.

February 2, 2010: Added new section Absolute Maximum Voltage Rating with table.

September 13, 2010: In Table 8, changed Buffer type for PCI Express from CML to PCIe differential and changed reference clocks to HCSL.

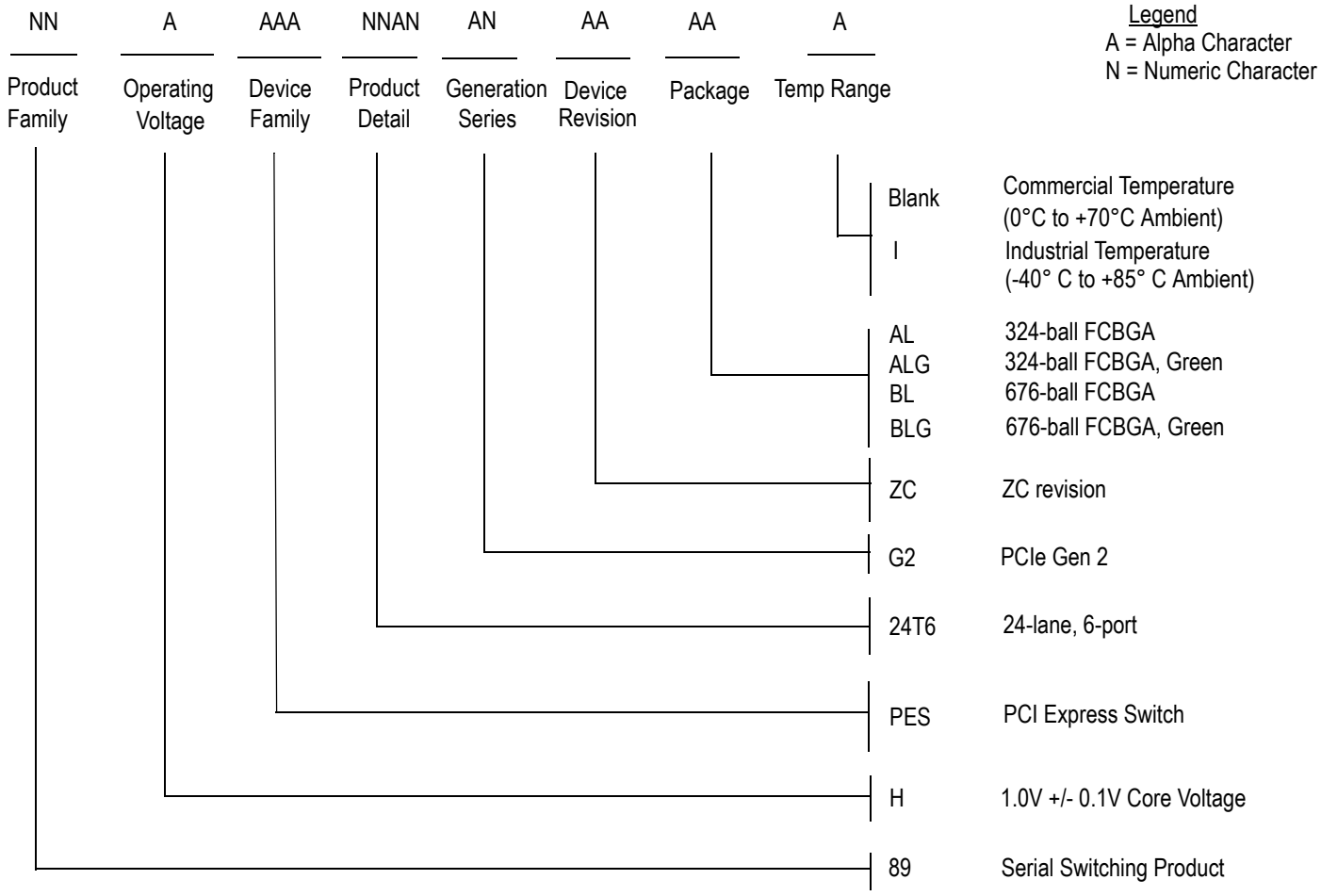
January 20, 2011: Added new Table 26, Package Trace Length for 19x19mm FCBGA package.

March 30, 2011: In Table 13, added VddPETA to footnote #1.

February 13, 2013: In Table 8, changed P01MERGEN, P23MERGEN, and P45MERGEN pins from pull-down to pull-up.

April 30, 2013: In Table 5, changed description for PxxMERGEN pins to pull-up via 92K ohm resistor.

Ordering Information



Valid Combinations

Option A (19x19mm)

89HPES24T6G2ZCAL	324-ball FCBGA package, Commercial Temperature
89HPES24T6G2ZCALG	324-ball Green FCBGA package, Commercial Temperature
89HPES24T6G2ZCALI	324-ball FCBGA package, Industrial Temperature
89HPES24T6G2ZCALGI	324-ball Green FCBGA package, Industrial Temperature

Option B (27x27mm)

89HPES24T6G2ZCBL	676-ball FCBGA package, Commercial Temperature
89HPES24T6G2ZCBLG	676-ball Green FCBGA package, Commercial Temperature
89HPES24T6G2ZCBLI	676-ball FCBGA package, Industrial Temperature
89HPES24T6G2ZCBLGI	676-ball Green FCBGA package, Industrial Temperature

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