19-1924; Rev 1; 10/01

Complete Dual-Band Quadrature Transmitter

General Description

The MAX2369 is a dual-band, triple-mode complete transmitter for cellular phones. The device takes a differential I/Q baseband input and mixes it up to IF through a quadrature modulator and IF variable-gain amplifier (VGA). The signal is then routed to an external bandpass filter and upconverted to RF through an SSB mixer and RF VGA. The signal is further amplified with an on-board PA driver.

The MAX2369 is designed for dual-band operation and supports TDMA for the PCS band as well as TDMA and AMPS for the cellular band. The desired mode of operation is selected by loading data on the SPI™/MICROWIRE™-compatible 3-wire serial bus. The MAX2369 then routes the signals to the appropriate ports depending on which band is selected. The MAX2369 includes two RF LO input ports and two PA driver ports, eliminating the need for external switching circuitry.

The MAX2369 takes advantage of the serial bus to set modes such as charge-pump current, high or low sideband injection, and IF/RF gain balancing. It is packaged in a small (7mm × 7mm) 48-pin QFN package with exposed paddle.

Applications

Dual-Band TDMA/Amps Handsets

GAIT Handsets

Triple-Mode, Dual-Mode, or Single-Mode Mobile Phones

Satellite Phones

Wireless Data Links (WAN/LAN)

Wireless Local Area Networks (LANs)

High-Speed Data Modems

High-Speed Digital Cordless Phones

Wireless Local Loop (WLL)

Pin Configuration appears at end of data sheet.

Selector Guide appears at end of data sheet.

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MICROWIRE is a trademark of National Semiconductor Corp.

Features

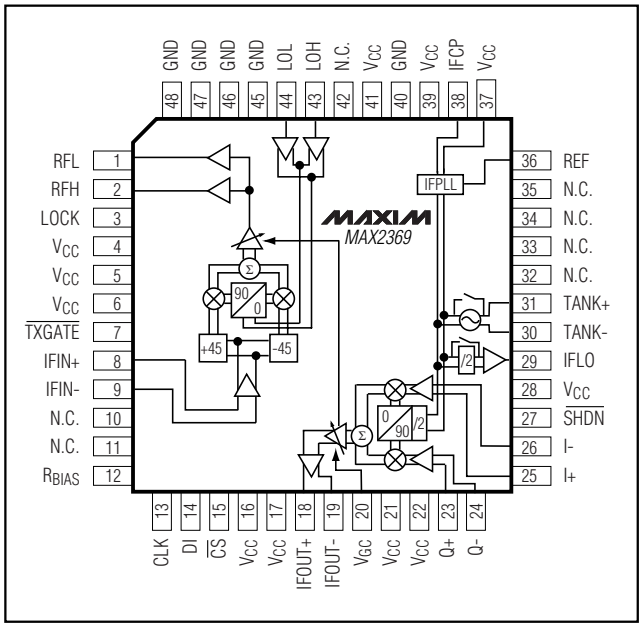
- **Dual-Band, Triple-Mode Operation**
- **+7dBm Output Power with -34dBc ACPR (NADC Modulation)**
- **100dB Power Control Range**
- **Supply Current Drops as Output Power Is Reduced**
- **On-Chip IF VCO and IF PLL**
- **QSPI/SPI/MICROWIRE-Compatible 3-Wire Bus**
- **Digitally Controlled Operational Modes**
- **+2.7V to +5.5V Operation**
- **Single Sideband Upconverter Eliminates SAW Filters**
- **Power Control Distributed at IF and RF for Optimum Dynamic Range**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2369EGM	-40°C to +85°C	48 QFN-EP*

**Exposed paddle*

Functional Diagram



Complete Dual-Band Quadrature Transmitter

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +3.6V
RFL, RFH.....+5.5V
DI, CLK, $\overline{CS}$, VGC, $\overline{SHDN}$, $\overline{TXGATE}$, LOCK.....-0.3V to (V_{CC} + 0.3V)
AC Input Pins (IFIN, Q, I, TANK, REF, LOL, LOH).....1.0V peak
Digital Input Current ($\overline{SHDN}$, $\overline{TXGATE}$, CLK, DI, $\overline{CS}$) .....±10mA

Continuous Power Dissipation (T_A = +70°C)
48-Pin QFN-EP (derate 27mW/°C above +70°C) 2.5W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(**MAX2369 Test Fixture:** V_{CC} = V_{BATT} = +2.75V, $\overline{SHDN}$ = $\overline{TXGATE}$ = +2.0V, VGC = +2.5V, R_{BIAS} = 16kΩ, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, and operating modes are defined in Table 6.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Supply Voltage				2.7		3.0	V
Operating Supply Current	(Note 1)	PCS mode	VGC = 0.5V		80	106	mA
			VGC = 2.0V		85	112	
			VGC = 2.5V		120	150	
		Cellular digital mode	VGC = 0.5V		82	107	
			VGC = 2.0V		87	113	
			VGC = 2.5V		123	155	
		FM mode	VGC = 0.5V		77	101	
			VGC = 2.0V		80	105	
			VGC = 2.5V		105	133	
		Addition for IFLO buffer			6.5	11	
	$\overline{TXGATE}$ = 0.6V				16	25	
	$\overline{SHDN}$ = 0.6V, sleep mode				0.5	20	µA
Logic High				2.0			V
Logic Low						0.6	V
Logic Input Current				-5		+5	µA
VGC Input Current				-12		+12	µA
VGC Input Resistance During Shutdown	$\overline{SHDN}$ = 0.6V			200	280		kΩ
Lock Indicator High	50kΩ pullup load			V_{CC} - 0.4			V
Lock Indicator Low	50kΩ pullup load					0.4	V

AC ELECTRICAL CHARACTERISTICS

(**MAX2369 Evaluation Kit:** 50Ω system, operating modes as defined in Table 6, input voltage at I and Q = 200mV$_{RMS}$ differential, common mode = V_{CC}/2, 300kHz quadrature CW tones, IF synthesizer locked with passive lead-lag second-order loop filter, REF = 200mVp-p at 19.44MHz, V_{CC} = $\overline{SHDN}$ = $\overline{CS}$ = $\overline{TXGATE}$ = +2.75V, V_{BAT} = +2.75V, IF output load = 400Ω, LOH, LOL input power = -7dBm, f_{LOL} = 1017.26MHz, f_{LOH} = 2061.26MHz, IFIN = 125mV$_{RMS}$ at 181.26MHz, IS-136 TDMA modulation, f_{RFH} = 1880MHz, f_{RFL} = 836MHz, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MODULATOR, QUADRATURE MODES (Digital Cellular, Digital PCS, FM IQ)					
IF Frequency Range			120–235		MHz
I/Q Common-Mode Input Voltage	V_{CC} = 2.7V to 3.0V (Notes 2, 3, 4)	1.35	V_{CC} / 2	V_{CC} – 1.25	V
IF Gain Control Range	VGC = 0.5V to 2.5V, IFG = 100		85		dB
IF Output Power, Digital Mode	VGC = 2.5V, IFG = 100		-10		dBm
Gain Variation Over Temperature	Relative to +25°C, T_A = -40°C to +85°C (Note 4)		±0.8		dB
RX Band Noise Power	VGC = 2.5V, IFG = 100, F_{IF} = 181.26MHz, noise measured at F_{IF} ± 20MHz		-145		dBm/Hz
Carrier Suppression	VGC = 2.5V, IFG = 100	30	49		dB
Sideband Suppression	VGC = 2.5V, IFG = 100	30	38		dB
MODULATOR, FM MODE					
IF Gain Control Range	VGC = 0.5V to 2.5V, IFG = 100		85		dB
Output Power	VGC = 2.5V, IFG = 111, I/Q modulation		-8.5		dBm
	VGC = 2.5V, IFG = 111, direct VCO modulation		-5.5		
UPCONVERTER AND PREDRIVER					
IF Frequency Range			120–235		MHz
Low-Band Frequency Range	RFL port		800–1000		MHz
High-Band Frequency Range	RFH port		1700–2000		MHz
LOL Frequency Range			800–1150		MHz
LOH Frequency Range			1400–2300		MHz
Output Power, RFL (Note 4)	VGC = 2.5V, NADC modulation, ACPR < -32dBc/ -55dBc at +30kHz/+60kHz offset	5.8	7		dBm
	VGC = 2.5V, FM mode	9	12		
Output Power, RFH (Note 4)	VGC = 2.6V, NADC modulation, ACPR = -32dB/ -55dBc at +30kHz/+60kHz offset	4	6.6		dBm
Power-Control Range	VGC = 0.5V to 2.5V		30		dB
Gain Variation Over Temperature	Relative to +25°C, T_A = -40°C to +85°C (Note 4)			±3	dB
RF Image Rejection (Note 4)	RFL	-25			dBc
	RFH	-24			
LO Leakage (Note 4)	RFL, VGC = 2.5V			-22	dBm
	RFH, VGC = 2.6V			-24	
RX Band Noise Power	RFL, VGC = 2.5V		-133		dBm/ Hz
	RFH, VGC = 2.6V		-134		

AC ELECTRICAL CHARACTERISTICS (continued)

(**MAX2369 Evaluation Kit:** 50Ω system, operating modes as defined in Table 6, input voltage at I and Q = 200mV$_{RMS}$ differential, common mode = V_{CC}/2, 300kHz quadrature CW tones, IF synthesizer locked with passive lead-lag second-order loop filter, REF = 200mVp-p at 19.44MHz, V_{CC} = $\overline{SHDN}$ = $\overline{CS}$ = $\overline{TXGATE}$ = +2.75V, V_{BAT} = +2.75V, IF output load = 400Ω, LOH, LOL input power = -7dBm, f_{LOL} = 1017.26MHz, f_{LOH} = 2061.26MHz, IFIN = 125mV$_{RMS}$ at 181.26MHz, IS-136 TDMA modulation, f_{RFH} = 1880MHz, f_{RFL} = 836MHz, T_A = +25°C, unless otherwise noted.)

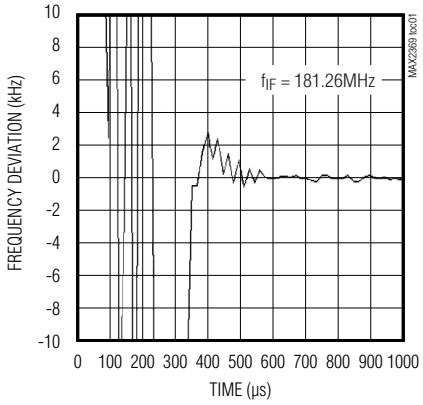
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IF_PLL					
Reference Frequency		5		30	MHz
Frequency Reference Signal Level		0.1		0.6	Vp-p
IF Main Divide Ratio		256		16384	
IF Reference Signal Ratio		2		2048	
VCO Operating Range			240–470		MHz
IF LO Output Power	BUF_EN = 1		-6		dBm
Charge-Pump Source/Sink Current	ICP = 00	148	200	260	µA
	ICP = 01	185	260	345	
	ICP = 10	295	400	515	
	ICP = 11	385	530	700	
Turbolock Boost Current	(Note 5)	385	530	700	µA
Charge-Pump Source/Sink Matching	Locked, all values of ICP, over specified compliance range (Note 6)		5		%
Charge-Pump High-Z Leakage	Over specified compliance range (Note 6)			10	nA

Note 1: See Table 6 for register settings.
Note 2: ACPR is met over the specified V_{CM} range.
Note 3: V_{CM} must be supplied by the I/Q baseband source with ±6µA capability.
Note 4: Guaranteed by design and characterization.
Note 5: When enabled, turbolock is active during acquisition and injects boost current in addition to the normal charge-pump current.
Note 6: Charge Pump Compliance range is 0.5V to V_{CC} - 0.5V.

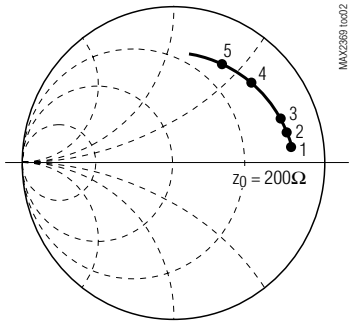
Typical Operating Characteristics

(MAX2369EVKIT, V_{CC} = +2.8V, V_{BAT} = 3.0V, T_A = +25°C, unless otherwise noted.)

IF P_{LL} SETTLING TIME

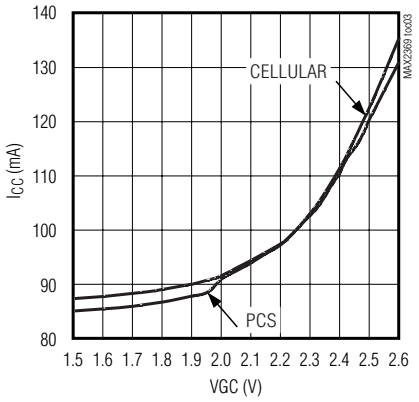


TANK 1/S11 vs. FREQUENCY

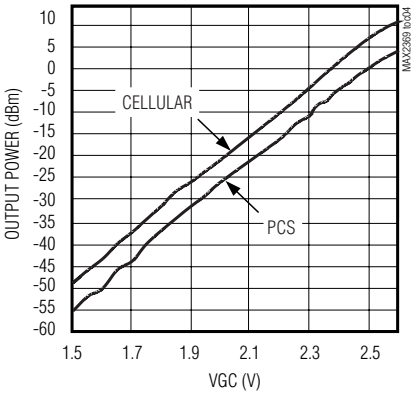


EQUIVALENT PARALLEL R-C
1: 200MHz, 1.76kΩ, 0.26pF
2: 260MHz, 1.66kΩ, 0.31pF
3: 330MHz, 1.58kΩ, 0.34pF
4: 780MHz, 1.21kΩ, 0.43pF
5: 1GHz, 0.94kΩ, 0.47pF

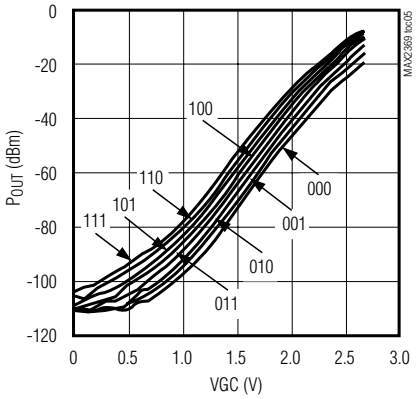
I_{CC} vs. VGC INPUT



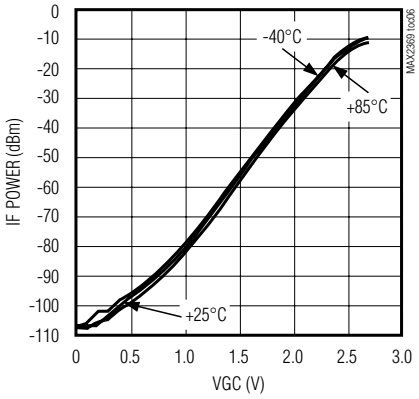
OUTPUT POWER vs. VGC INPUT



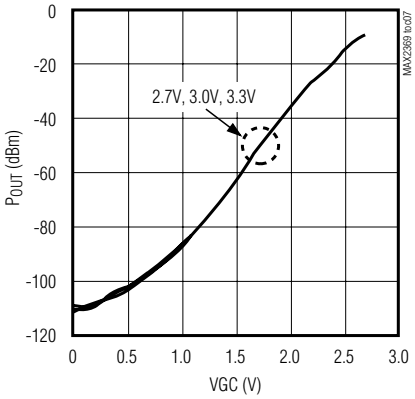
IF OUTPUT POWER vs. VGC INPUT AND IF DAC SETTING



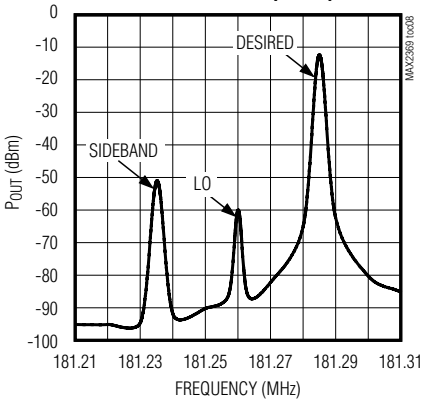
IF OUTPUT POWER vs. VGC INPUT



IF OUTPUT POWER vs. VGC INPUT



SIDEBAND SUPPRESSION AND LO FEEDTHROUGH (IFOUT)

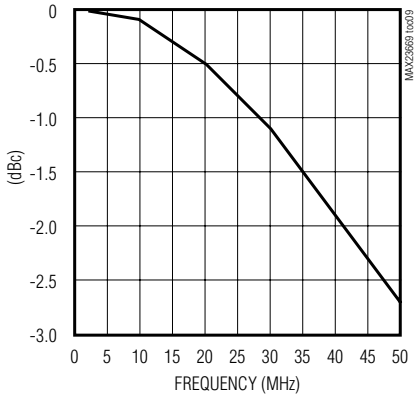


Complete Dual-Band Quadrature Transmitter

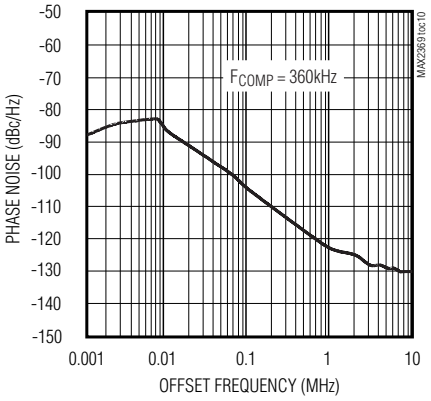
Typical Operating Characteristics (continued)

(MAX2369EVKIT, V_{CC} = +2.8V, V_{BAT} = 3.0V, T_A = +25°C, unless otherwise noted.)

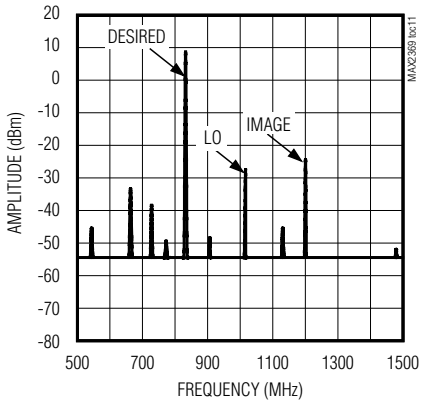
I/Q BASEBAND FREQUENCY RESPONSE



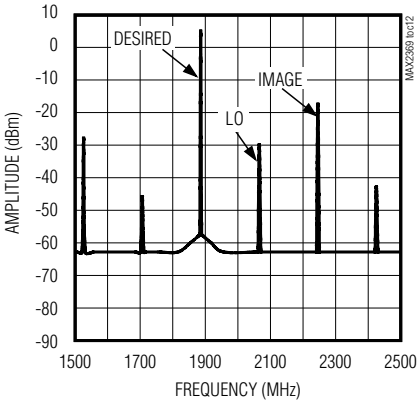
PHASE NOISE LOW-BAND OSCILLATOR vs. FREQUENCY OFFSET (181.26MHz)



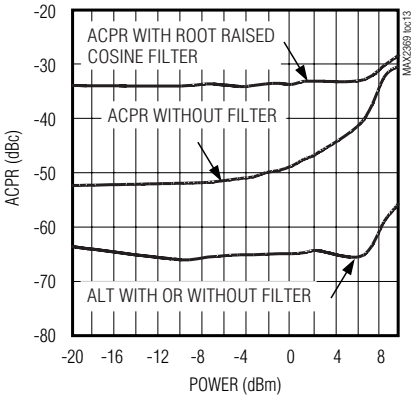
RFL OUTPUT SPECTRUM



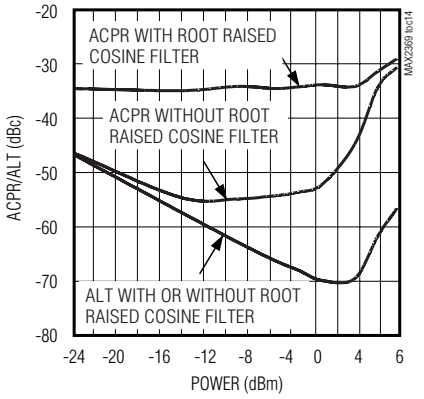
RFH OUTPUT SPECTRUM



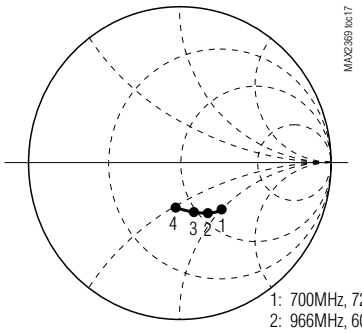
CASCADED ACPR/ALT vs. POWER (RFL)



CASCADED ACPR/ALT vs. POWER (RFH)

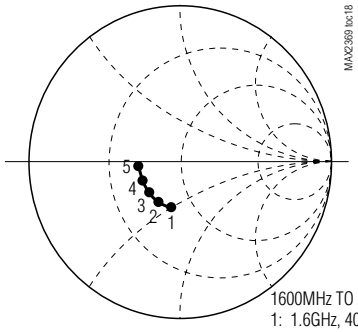


LOL PORT S11



1: 700MHz, 72Ω –j51Ω
2: 966MHz, 60Ω –j46Ω
3: 1.22MHz, 52Ω –j38Ω
4: 1.5GHz, 40Ω –j25Ω

LOH PORT S11



1600MHz TO 2500MHz
1: 1.6GHz, 40Ω –j25Ω
2: 1.75GHz, 36Ω –j22Ω
3: 1.88GHz, 34Ω –j18Ω
4: 2.01GHz, 32Ω –j15Ω
5: 2.5GHz, 29Ω –j0Ω

Pin Description

PIN	NAME	FUNCTION
1	RFL	Transmitter RF Output for Cellular Band (800MHz to 1000MHz)—for both FM and digital modes. This open-collector output requires a pullup inductor to the supply voltage, which is part of the output matching network and may be connected directly to the battery.
2	RFH	Transmitter RF Output for PCS Band (1700MHz to 2000MHz). This open collector output requires a pullup inductor to the supply voltage. The pullup inductor is part of the output matching network and may be connected directly to the battery.
3	LOCK	Open-Collector Output Indicating Lock Status of the IF PLL. Requires a pullup resistor. Control using configuration register bit LD_MODE.
4	V_{CC}	Power Supply. Supply pin for the driver stage. V_{CC} must be bypassed to system ground as close to the pin as possible. The ground vias for the bypass capacitor should not be shared by any other branch. Bypass to ground with 100pF and 100nF capacitors.
5	V_{CC}	Power Supply. Connect to pin 4 for normal operation.
6	V_{CC}	Supply Pin for the Upconverter Stage. V_{CC} must be bypassed to system ground as close to the pin as possible. The ground vias for the bypass capacitor should not be shared by any other branch.
7	$\overline{TXGATE}$	Digital Input. A logic low on $\overline{TXGATE}$ shuts down everything except the IF PLL, IF VCO, and serial bus and registers. This mode is used for IF PLL settling before the transmit time slot.
8, 9	IFIN+, IFIN-	Differential Inputs to the RF Upconverter. These pins are internally biased to +1.5V. The input impedance for these ports is nominally 400Ω differential. The IF filter should be AC-coupled to these ports. Keep the differential lines as short as possible to minimize stray pickup and shunt capacitance.
10, 11	N.C.	No Connection. Leave these pins floating.
12	R_{BIAS}	Bias Resistor Pin. RBIAS is internally biased to a bandgap voltage of +1.18V. An external resistor or current source must be connected to this pin to set the bias current for the upconverters and PA driver stages. The nominal resistor value is 16kΩ. This value can be altered to optimize the linearity of the driver stage.
13, 14, 15	CLK, DI, $\overline{CS}$	Input Pins from the 3-Wire Serial Bus (SPI/QSPI/MICROWIRE compatible). An R-C filter on each of these pins may be used to reduce noise.
16, 17	V_{CC}	Power supply. Bypass to ground with a 1000pF capacitor.
18, 19	IFOUT+, IFOUT-	Differential IF Outputs. These pins must be inductively pulled up to V_{CC}. A differential IF bandpass filter is connected between this port and IFIN+ and IFIN-. The pullup inductors can be part of the filter structure. The differential output impedance of this port is nominally 600Ω. The transmission lines from these pins should be short to minimize the pickup of spurious signals and noise.
20	VGC	RF and IF Variable-Gain Control Analog Input. VGC floats to +1.5V. Apply +0.5V to +2.6V to control the gain of the RF and IF stages. An RC filter on this pin may be used to reduce DAC noise or PDM clock spurs from this line.
21	V_{CC}	Supply Pin for the IF VGA. Bypass with a capacitor as close to the pin as possible. The bypass capacitor must not share its ground vias with any other branches.

Complete Dual-Band Quadrature Transmitter

Pin Description (continued)

PIN	NAME	FUNCTION
22	V_{CC}	Supply for the I/Q Modulator. Bypass with capacitor as close to the pin as possible. The bypass capacitor must not share its ground vias with any other branches.
23, 24	Q+, Q-	Differential Q-Channel Baseband Inputs to the Modulator. These pins go directly to the bases of a differential pair and require an external common-mode bias voltage.
25, 26	I+, I-	Differential I-Channel Baseband Inputs to the Modulator. These pins go directly to the bases of a differential pair and require an external common-mode bias voltage.
27	$\overline{SHDN}$	Shutdown Input. A logic low on $\overline{SHDN}$ shuts down the entire IC. An R-C lowpass filter may be used to reduce digital noise.
28	V_{CC}	Supply Pin to the VCO Section. Bypass as close to the pin as possible. The bypass capacitor should not share its vias with any other branches.
29	IFLO	Buffered LO Output. Control the output buffer using register bit BUF_EN and the divide ratio using the register bit BUF_DIV.
30, 31	TANK-, TANK+	Differential Tank Pins for the IF VCO. These pins are internally biased to +1.6V.
32, 33, 34, 35, 42	N.C.	No Connection. Leave these pins floating.
36	REF	Reference Frequency Input. REF is internally biased to V_{CC} - 0.7V and must be AC-coupled to the reference source. This is a high-impedance port (25kΩ || 3pF).
37	V_{CC}	Supply for the IF Charge Pump. This supply can differ from the system V_{CC}. Bypass as close to the pin as possible. The bypass capacitor must not share its vias with any other branches.
38	IFCP	High-Impedance Output of the IF Charge Pump. Connect to the tune input of the IF VCOs through the IF PLL loop filter. Keep the line from IFCP to the tune input as short as possible to prevent spurious pickup, and connect the loop filter as close to the tune input as possible.
39	V_{CC}	Supply Pin for Digital Circuitry. Bypass as close to the pin as possible. The bypass capacitor must not share its vias with any other branch.
40, 45, 46, 47, 48	GND	Ground. Connect to PC board ground plane.
41	V_{CC}	Supply Pin. Bypass as close to the pin as possible. The bypass capacitor may share with supply pin for digital circuitry, pin 39.
43	LOH	High-band RF LO Input Port. AC-couple to this port.
44	LOL	Low-band RF LO Input Port. AC-couple to this port.
Exposed paddle	GND	DC and AC GND Return for the IC. Connect to PC board ground plane using multiple vias.

Detailed Description

The MAX2369 complete quadrature transmitter accepts differential I/Q baseband inputs with external common-mode bias. A modulator upconverts this to IF frequency in the 120MHz to 235MHz range. A gain control voltage pin (VGC) controls the gain of both the IF and RF VGAs simultaneously to achieve best noise and linearity performance. The IF signal is brought off-chip for filtering, then fed to a single sideband upconverter followed by the RF VGA and PA driver. The RF upconverter requires an external VCO for operation. The IF PLL and operating mode can be programmed by an SPI/QSPI/MICROWIRE-compatible 3-wire interface.

The following sections describe each block in the MAX2369 *Functional Diagram.*

I/Q Modulator

Differential in-phase (I) and quadrature-phase (Q) input pins are designed to be DC-coupled and biased with the baseband output from a digital-to-analog converter (DAC). I and Q inputs need a DC bias of $V_{CC}/2$ and a current-drive capability of 6µA. Common-mode voltage will work within a 1.35V to (V_{CC} - 1.25V) range. Typically, I and Q will be driven differentially with a $200mV_{RMS}$ baseband signal. Optionally, I and Q may be programmed for $100mV_{RMS}$ operation with the IQ_LEVEL bit in the configuration register. The IF VCO output is fed into a divide-by-two/quadrature generator block to derive quadrature components to drive the IQ modulator. The output of the modulator is fed into the VGA.

IF VCO

The VCO oscillates at twice the desired IF frequency. Oscillation frequency is determined by external tank components (see *Applications Information*). Typical phase-noise performance for the tank is shown in *Typical Operating Characteristics.*

IFLO Output Buffer

IFLO provides a buffered LO output when BUF_EN is 1. The IFLO output frequency is equal to the VCO frequency when BUF_DIV is 0, and half the VCO frequency when BUF_DIV is 1. The output power is -6dBm. This output is used in test mode.

IF PLL

The IF PLL uses a charge-pump output to drive a loop filter. The loop filter will typically be a passive second-order lead lag filter. Outside the filter's bandwidth, phase noise will be determined by the tank components. The two components that contribute most significantly to phase noise are the inductor and varactor. Use high-Q inductors and varactors to maximize equivalent parallel resistance. The ICP_MAX bit in the OPCTRL register can be set to 1 to increase the charge pump current.

IF VGA

The IF VGA allows varying an IF output level that is controlled by the VGC voltage. The voltage range on VGC of +0.5V to +2.6V provides a gain-control range of 85dB. The IF output ports from the VGA are optimized for IF frequency from 120MHz to 235MHz. IFOUT ports support direct VCO FM modulation. The differential IF output port has an output impedance of 600Ω when pulled up to V_{CC} through a choke.

Single Sideband Mixer

The RF transmit mixer uses a single sideband architecture to eliminate an off-chip RF filter. The mixer is followed by the RF VGA. The RF VGA is controlled by the same VGC pin as the IF VGA to provide optimum linearity and noise performance. The total power control range is >100dB.

PA Driver

The MAX2369 includes two power-amplifier (PA) drivers. Each is optimized for the desired operating frequency. RFL is optimized for cellular-band operation. RFH is optimized for PCS operation. The PA drivers have open-collector outputs and require pullup inductors. The pullup inductors can act as the shunt element in a shunt series match.

Programmable Registers

The MAX2369 includes five programmable registers consisting of two divide registers, a configuration register, an operational control register, and a test register. Each register consists of 24 bits. The 4 least significant bits (LSBs) are the register's address. The 20 most significant bits (MSBs) are used for register data. All registers contain some "don't care" bits. These can be either a zero or a 1 and do not affect operation (Figure 1). Data is shifted in MSB first, followed by the 4-bit address. When $\overline{CS}$ is low, the clock is active and data is shifted with the rising edge of the clock. When $\overline{CS}$ transitions to high, the shift register is latched into the register selected by the contents of the address bits. Power-up defaults for the five registers are shown in Table 1. The registers should be initialized according to Table 2. The dividers and control registers are programmed from the SPI/QSPI/MICROWIRE-compatible serial port.

Complete Dual-Band Quadrature Transmitter

The IFM register sets the main frequency divide ratio for the IF PLL. The IFR register sets the reference frequency divide ratio. The IF VCO frequency can be determined by the following:

$$\text{IF VCO frequency} = f_{REF} \times (\text{IFM} / \text{IFR})$$

where f_{REF} is the external reference frequency.

The operational control register (OPCTRL) controls the state of the MAX2369. See Table 3 for the function of each bit.

The configuration register (CONFIG) sets the configuration for the IF PLL and the baseband I/Q input levels See Table 4 for a description of each bit.

The test register is not needed for normal use.

Power Management

Bias control is distributed among several functional sections and can be controlled to accommodate many different power-down modes as shown in Table 5.

The shutdown control bit is of particular interest since it differs from the $\overline{SHDN}$ pin. When the shutdown control bit is active (SHDN_BIT = 0), the serial interface is left active so that the part can be turned on with the serial bus while all other functions remain shut off. In contrast,

MSB												24 BIT REGISTER											LSB
DATA 20 BITS																				ADDRESS 4 BITS			
B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	A3	A2	A1	A0
						IFM DIVIDE RATIO REGISTER (14 BITS)														ADDRESS			
X	X	X	X	X	X	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	1	0
									IFR DIVIDE RATIO REGISTER (11 BITS)											ADDRESS			
X	X	X	X	X	X	X	X	X	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	1	1
				CONTROL REGISTER (16 BITS)																ADDRESS			
X	X	X	X	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	1	0	0
				CONFIGURATION REGISTER (16 BITS)																ADDRESS			
X	X	X	X	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	1	0	1
												TEST REGISTER (8 BITS)								ADDRESS			
X	X	X	X	X	X	X	X	X	X	X	X	B7	B6	B5	B4	B3	B2	B1	B0	0	1	1	1

X = DON'T CARE

Figure 1. Register Configuration

Table 1. Register Power-Up Default States

REGISTER	DEFAULT	ADDRESS	FUNCTION
IFM	6519 dec	0010_b	IF M divider count
IFR	0492 dec	0011_b	IF R divider count
OPCTRL	892F hex	0100_b	Operational control settings
CONFIG	D03F hex	0101_b	Configuration and setup control
TEST	0000 hex	0111_b	Test-mode control

Table 2. Register Initialization for F_{REF} = 19.44MHz, F_{IF} = 181.26MHz, F_{COMP} = 360kHz

REGISTER	DEFAULT	ADDRESS	FUNCTION
IFM	1007 dec	0010_b	IF M divider count
IFR	0054 dec	0011_b	IF R divider count
OPCTRL	890F hex	0100_b	Operational control settings
CONFIG	903D hex	0101_b	Configuration and setup control
TEST	0000 hex	0111_b	Test-mode control

when the $\overline{SHDN}$ pin is low it shuts down everything. In either case, PLL programming and register information is lost. To retain the register information, use standby mode ($\overline{STBY}$ = 0).

Signal Flow Control

Table 6 shows an example of key registers for triple-mode operation.

Applications Information

The MAX2369 is designed for use in dual-band, triple-mode systems. It is recommended for triple-mode handsets. A typical application circuit is shown in Figure 2.

3-Wire Interface

Figure 3 shows the 3-wire interface timing diagram. The 3-wire bus is SPI/QSPI/MICROWIRE compatible.

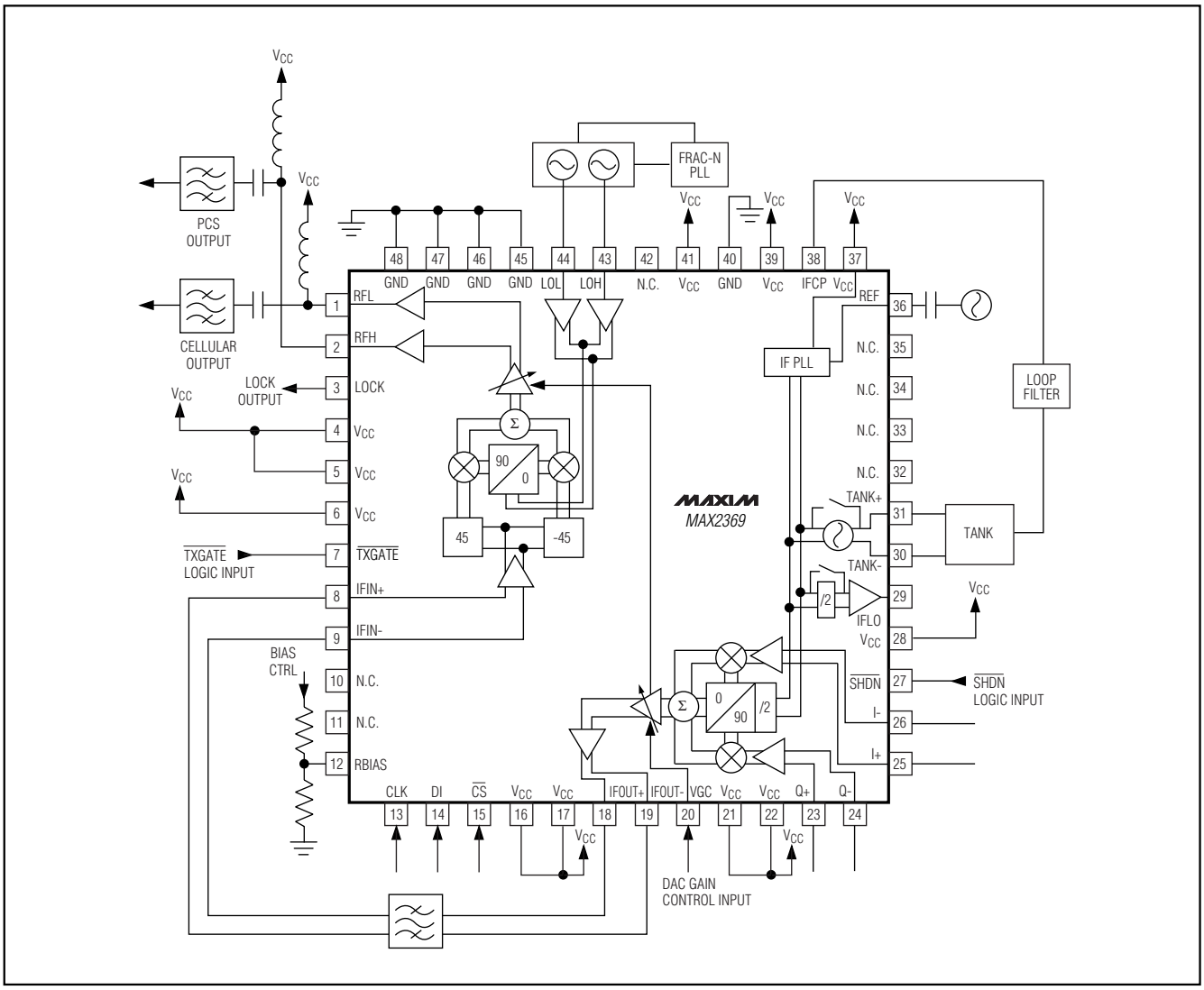


Figure 2. MAX2369 Typical Application Circuit

Table 3. Operation Control Register (OPCTRL)

BIT NAME	POWER-UP STATE	BIT LOCATION (0 = LSB)	FUNCTION
LO_SEL	1	15	1 selects LOL input port; 0 selects LOH port.
UNUSED	0	14	Set to 0 for normal operation.
ICP_MAX	0	13	1 keeps IF turbo-mode current active even when frequency acquisition is achieved. This mode is used when high operating IF charge-pump current is needed.
MODE	01	12, 11	Sets operating mode according to the following: 00 = FM mode 01 = Cellular digital mode; RFL is selected 10 = Not used 11 = PCS mode; RFH is selected
UNUSED	0	10	Set to 0 for normal operation.
UNUSED	0	9	Set to 0 for normal operation.
IFG	100	8, 7, 6	3-bit IF gain control. Alters IF gain by approximately 2dB per LSB (0 to 14dB). Provides a means for adjusting balance between RF and IF gain for optimized linearity.
SIDE_BAND	1	5	When this register is 1, the upper sideband is selected (LO below RF). When this register is 0, the lower sideband is selected (LO above RF).
BUF_EN	0	4	0 turns IFLO buffer off; 1 turns IFLO buffer on.
MOD_TYPE	1	3	0 selects direct VCO modulation. (IF VCO is externally modulated and the I/Q modulator is bypassed); 1 selects quadrature modulation.
$\overline{\text{STBY}}$	1	2	0 shuts down everything except registers and serial interface.
$\overline{\text{TXSTBY}}$	1	1	0 shuts down modulator and upconverter, leaving PLL locked and registers active. This is the programmable equivalent to the $\overline{\text{TXGATE}}$ pin.
SHDN_BIT	1	0	0 shuts down everything except serial interface, and also resets all registers to power-up state.

Table 4. Configuration Register (CONFIG)

BIT NAME	POWER-UP STATE	BIT LOCATION (0 = LSB)	FUNCTION
IF_PLL_SHDN	1	15	0 shuts down the IF PLL. This mode is used with an external IF VCO and IF PLL.
UNUSED	1	14	Set to 0 for normal operation.
UNUSED	0	13	Set to 0 for normal operation.
IQ_LEVEL	1	12	1 selects 200mV$_{RMS}$ input mode; 0 selects 100mV$_{RMS}$ input mode.
BUF_DIV	0	11	1 selects ÷2 on IFLO port; 0 bypasses the divider.
VCO_BYPASS	0	10	1 bypasses IF VCO and enables a buffered input for external VCO use.
ICP	00	9, 8	A 2-bit register sets the IF charge-pump current as follows: 00 = 200µA 01 = 260µA 10 = 400µA 11 = 530µA
UNUSED	00	7, 6	Not used. Leave in the power-up/initialized state.
IF_PD_POL	1	5	IF phase-detector polarity; 1 selects positive polarity (increasing tuning voltage on the VCO produces increasing frequency); 0 selects negative polarity (increasing tuning voltage on the VCO produces decreasing frequency).
UNUSED	111	4, 3 ,2	Not used. Leave in the power-up/initialized state.
UNUSED	1	1	Set to 0 for normal operation.
LD_MODE	1	0	Determines output mode for LOCK detector pin as follows: 0 = test mode, LD_MODE cannot be 0 for normal operation 1 = IF PLL lock detector

Electromagnetic Compliance Considerations

Two major concepts should be employed to produce a noise-free and EMC-compliant transmitter: minimize circular current-loop area to reduce H-field radiation and minimize voltage drops to reduce E-field radiation. To minimize the circular current-loop area, bypass as close to the part as possible and use the distributed capacitance of a ground plane. To minimize voltage drops, make V_{CC} traces short and wide, and make RF traces short.

The “don't care” bits in the registers should be zero in order to minimize electromagnetic radiation due to unnecessary bit banging. RC filtering can also be used to slow the clock edges on the 3-wire interface, reducing high-frequency spectral content. RC filtering also provides for transient protection against IEC802 testing by shunting high frequencies to ground, while the series resistance attenuates the transients for error-free operation. The same applies to the override pins ($\overline{SHDN}$, $\overline{TXGATE}$).

When floating the override pins, bypass to ground with the capacitors as close to the part as possible.

High-frequency bypass capacitors are required close to the pins with a dedicated via to ground. The 48-pin QFN-EP package provides minimal inductance ground by using an exposed paddle under the part. Provide at least five low-inductance vias under the paddle to ground to minimize ground inductance. Use a solid ground plane wherever possible. Any cutout in the ground plane may act as slot radiator and reduce its shield effectiveness.

Keep the RF LO traces as short as possible to reduce LO radiation and susceptibility to interference.

Table 5. Power-Down Modes

POWER-DOWN MODES	COMMENTS	OFF								
		UPCONVERTER	MODULATOR	SERIAL BUS	OPCTRL REG	IF LO BUFFER	IF VCO	IF PLL	IF PLL REGS	CONFIG REG
$\overline{SHDN}$ pin	Ultra-low shutdown current	X	X	X	X	X	X	X	X	X
$\overline{TXGATE}$ pin	For punctured TX mode	X	X							
IF PLL SHDN	For external IF PLL use							X	X	
TX STBY	TX is off, but IF LO stays locked	X	X							
REG STBY	Shuts down, but preserves registers	X	X			X	X	X		
REG SHDN	Serial bus is still active	X	X		X	X	X	X	X	X

Table 6. Register and Control Pin States for Key Operating Modes

MODE	DESCRIPTION	OPCTRL REGISTER						IF_PLL_SHDN	CONTROL PINS	
		LO_SEL	MODE	MOD_TYPE	$\overline{STBY}$	$\overline{TXSTBY}$	SHDN_BIT		$\overline{TXGATE}$	$\overline{SHDN}$
PCS Digital	RFH selected	0	11	1	1	1	1	1	H	H
Cellular Digital	RFL selected	1	01	1	1	1	1	1	H	H
FM	Direct VCO modulation, RFL selected	1	00	0	1	1	1	1	H	H
FM_IQ	FM with IQ modulation, RFL selected	1	00	1	1	1	1	1	H	H
PCS TXGATE	Gated transmission, PCS	0	11	1	1	X	1	1	L	H
Cellular TXGATE	Gated transmission, cellular digital	1	01	1	1	X	1	1	L	H
Sleep	Everything off	X	XX	X	X	X	X	X	X	L

X = Don't care

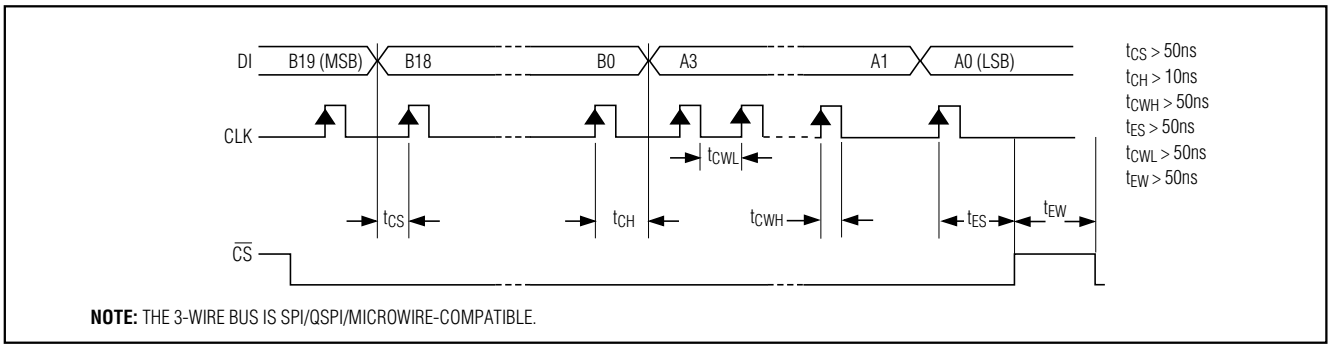


Figure 3. 3-Wire Interface Diagram

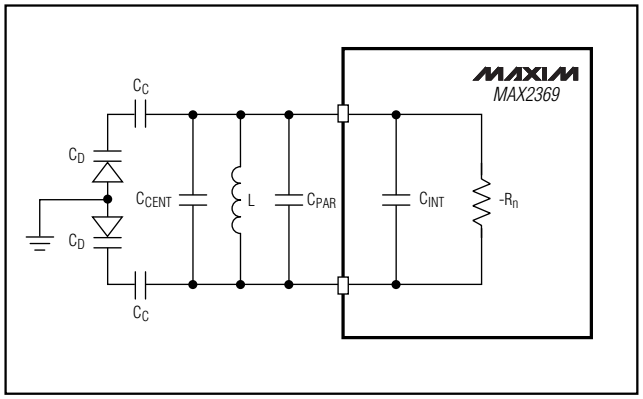


Figure 4. Tank Port Oscillator

IF Tank Design

The IF VCO tank (TANK+, TANK-) is fully differential. The external tank components are shown in Figure 4. The frequency of oscillation is determined by the following equation:

$$f_{OSC} = \frac{1}{2\pi \sqrt{(C_{INT} + C_{CENT} + C_{VAR} + C_{PAR})\ L}}$$

$$C_{VAR} = \frac{C_D \times C_C}{2\ (C_D + C_C)}$$

C_{INT} = Internal capacitance of TANK port

C_D = Capacitance of varactor

C_{VAR} = Equivalent variable tuning capacitance

C_{PAR} = Parasitic capacitance due to PC board pads and traces

C_{CENT} = External capacitor for centering oscillation frequency

C_C = External coupling capacitor to the varactor

Internal to the IC, the charge pump will have a leakage of less than 10nA. This is equivalent to a 300MΩ shunt resistor. The charge-pump output must see an extremely high DC resistance of greater than 300MΩ. This will minimize charge-pump spurs at the comparison frequency. Make sure there is no solder flux under the varactor or loop filter.

Layout Issues

The MAX2369 EV kit can be used as a starting point for layout. For best performance, take into consideration power-supply issues, as well as the RF, LO, and IF layout.

Power-Supply Layout

To minimize coupling between different sections of the IC, the ideal power-supply layout is a star configuration, which has a large decoupling capacitor at a central V_{CC} node. The V_{CC} traces branch out from this node, each going to a separate V_{CC} node in the MAX2369 circuit. At the end of each trace is a bypass capacitor with impedance to ground less than 1Ω at the frequency of interest. This arrangement provides local decoupling at each V_{CC} pin. Use at least one via per bypass capacitor for a low-inductance ground connection.

Matching Network Layout

The layout of a matching network can be very sensitive to parasitic circuit elements. To minimize parasitic inductance, keep all traces short and place components as close to the IC as possible. To minimize parasitic capacitance, a cutout in the ground plane (and any other planes) below the matching network components can be used.

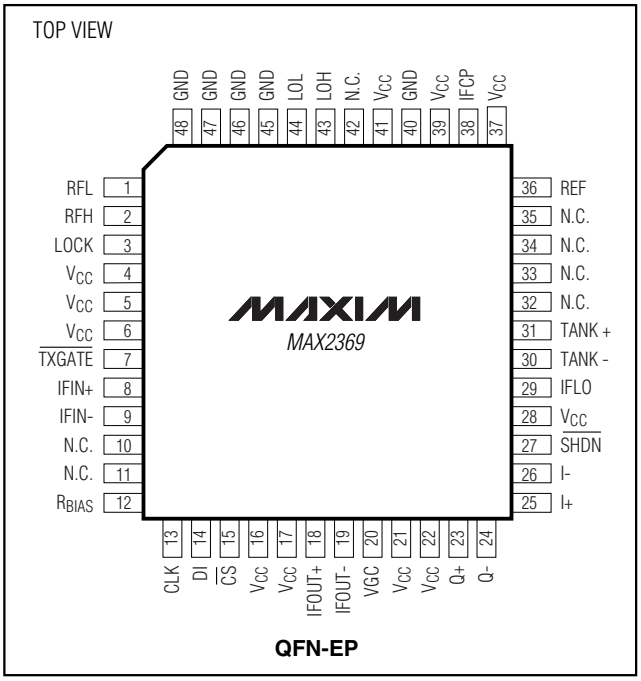
On the high-impedance ports (e.g., IF inputs and outputs), keep traces short to minimize shunt capacitance.

Complete Dual-Band Quadrature Transmitter

Tank Layout

Keep the traces coming out of the tank short to reduce series inductance and shunt capacitance. Keep the inductor pads and coupling capacitor pads small to minimize stray shunt capacitance.

Pin Configuration



QFN-EP

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.