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SHENZHEN TOPWAY TECHNOLOGY CO., LTD.

LM24080BCW-4

LCD Module User Manual

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Date: 2012-04-07	Date:	Date:

Rev.	Descriptions	Release Date
0.1	New release	2010-04-30
0.2	Update Interfacing Setting	2012-04-07

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1. Basic Specifications

1.1 Display Specifications

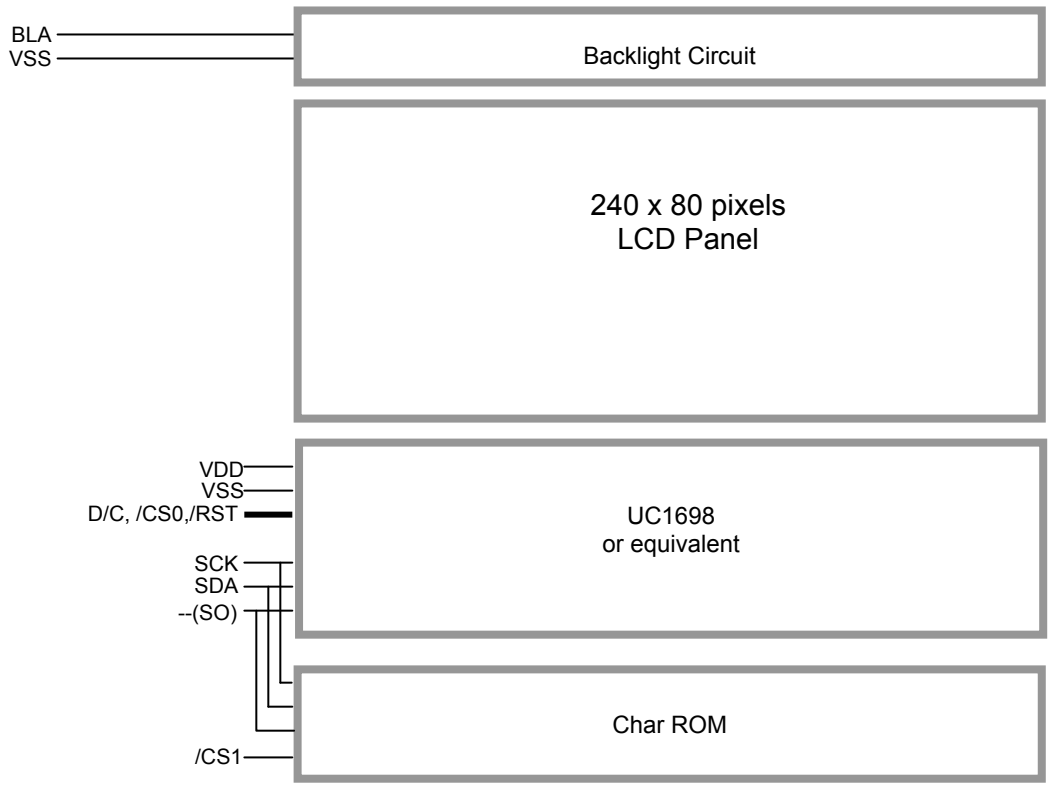
1) LCD Display Mode : FSTN, Positive, Transflective
2) Display Color : Display Data = “1” : Dark Gray (*1)
: Display Data = “0” : Light Gray (*2)
3) Viewing Angle : 6H
4) Driving Method : 1/80 duty, 1/10 bias
5) Backlight : White LED backlight

Note:
*1. Color tone may slightly change by Temperature and Driving Condition.
*2. The Color is defined as the inactive / background color

1.2 Mechanical Specifications

1) Outline Dimension : 130.0 x 65.0 x 11.5 MAX.
see attached Outline Drawing for details

1.3 Block Diagram



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1.4 Terminal Functions

Pin No.	Pin Name	I/O	Descriptions				
			Display				Char Rom
			8-bit parallel 68mode	8-bit parallel 80mode	Serial		
					4wire	3wire	
1	VSS	Power	0V Power Supply, GND				-
2	VDD	Power	Positive Power Supply				-
3	NC	-					-
4	D/C	Input	Register Select D/C=HIGH: data on DB0 to DB7 is display data D/C=LOW: data on DB0 to DB7 is command data			pull down	-
5	NC	Input	In read mode R/W = H; Data read form LCD module, data appears at DB0 – DB7 and can be read by the host while, E = H and the device is being selected In write mode R/W = L; Data write to the LCD module, data appears at DB0 – DB7 will be written into the LCD module at E = H→L and device is being selected	Write enable input, active LOW	No connection, leave open		-
6	VSS	Input		Read enable input, active LOW	pull down		
7	SCK(SI)	IO	8-bit bi-directional data bus(DB0~DB7)		Serial clock input		serial data input
8	SDA(SCLK)				Serial data input		serial clock input
9	VSS	IO			pull down		-
10	--(SO)	IO			pull up or pull down		serial data output
11	VSS	IO			pull down		-
12	VSS						
13	VSS						
14	VSS						
15	/CS0	Input	Chip Select Signal /CS=L: Data IO is enabled				/CS0=H, controller not selected
16	/RST	Input	Reset Signal: /RST = L, Reset the LCD Module /RST = H, Normal Running				-
17	/CS1	Input	Chip Select Signal /CS1=H,Char Rom not selected				/CS1=L, Char Rom selected
18	NC	-	No connection,leave open				-
19	NC	-	No connection,leave open				-
20	BLA	Power	Positive Power Supply for LED backlight				-

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2. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	-0.3	+3.6	V	V_{SS} = 0V
Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	V_{SS} = 0V
Operating Temperature	T_{OP}	-20	+70	°C	No Condensation
Storage Temperature	T_{ST}	-30	+80	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

3. Electrical Characteristics

3.1 DC Characteristics

V_{SS}=0V, V_{DD}=3.0V, T_{OP}=25°C

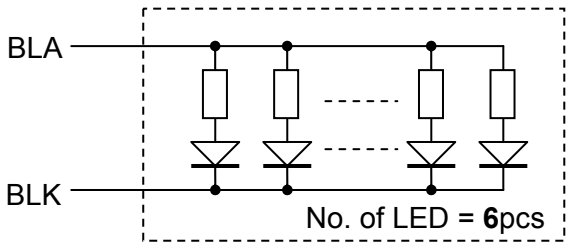
Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Operating Voltage	V_{DD}	2.7	3.0	3.3	V	VDD
Input High Voltage	V_{IN}	0.7xVDD	-	VDD	V	SCK,SDA,/CS0,/CS1,D/C, /RST,--(SO)
Input Low Voltage	V_{IN}	VSS	-	0.2xVDD	V	SCK,SDA,/CS0,/CS1,D/C, /RST,--(SO)
Operating Current	I_{DD}	-	0.8	3.0	mA	VDD

3.2 LED Backlight Circuit Characteristic

BLK=0V, If_{BLA}=102mA, T_{OP} =25°C

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Forward Voltage	Vf_{BLA}	-	3.0	-	V	BLA
Forward Current	If_{BLA}	-	102	132	mA	BLA

Cautions:
Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.



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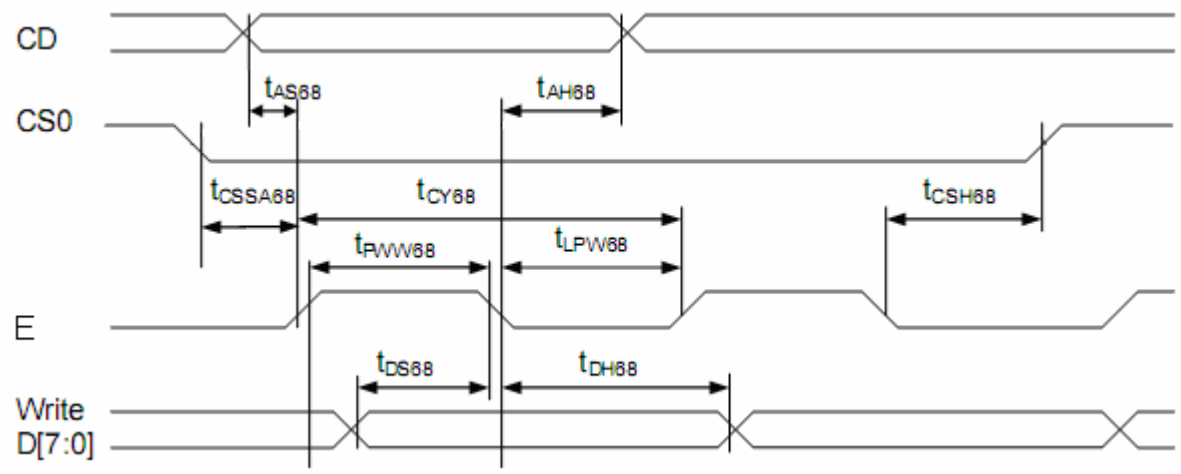
3.3 AC Characteristics

3.3.1 68 Mode

V_{SS}=0V, V_{DD}=3.0V, T_{OP}=25°C

Item	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time	tAS68	0	-	-	ns
Address hold time	tAH68	0	-	-	ns
System cycle time	tCY68	80	-	-	ns
Pulse width	tPWW68	50	-	-	ns
Low pulse width	tLPW68	40	-	-	ns
Data setup time	tDS68	30	-	-	ns
Data hold time	tDH68	0	-	-	ns
Chip select setup time	tCSSA68	5	-	-	ns
	tCSH68	5	-	-	ns

Note: *1. Input signal rise/fall time should be less than 20ns
For details, please refer to UC1698U datasheet.



Bus Timing Diagram

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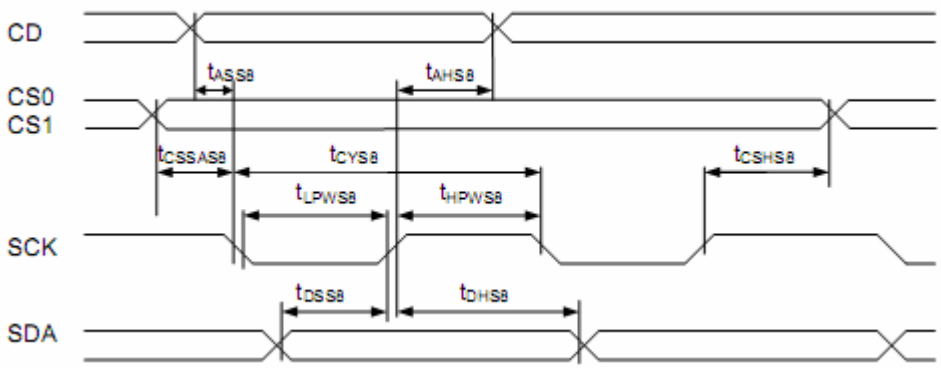
3.3.2 Serial Bus Timing (for S8/S8uc)

($2.5V \leq V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		40	–	nS
t_{LPWS8}		Low pulse width		20	–	nS
t_{HPWS8}		High pulse width		20	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		15 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		5 5		nS

($1.65V \leq V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		75	–	nS
t_{LPWS8}		Low pulse width		37	–	nS
t_{HPWS8}		High pulse width		38	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time		10 10		nS



Serial Bus Timing Characteristics(for S8/S8uc)

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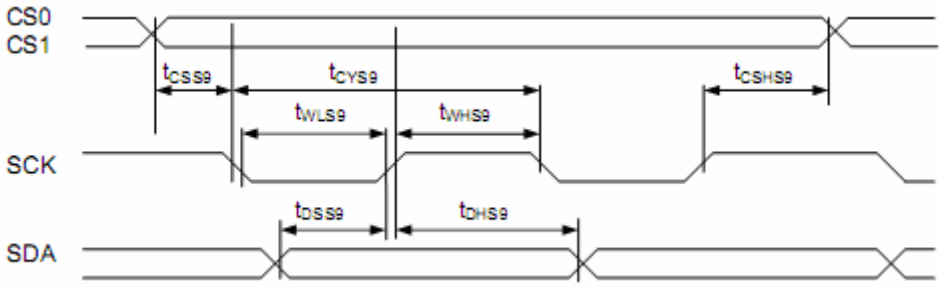
3.3.3 Serial Bus Timing (S9)

(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		40	–	nS
t_{LPWS9}		Low pulse width		20	–	nS
t_{HPWS9}		High pulse width		20	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		15 0	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		5 5		nS

(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		75	–	nS
t_{LPWS9}		Low pulse width		38	–	nS
t_{HPWS9}		High pulse width		38	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 0	–	nS
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10		nS

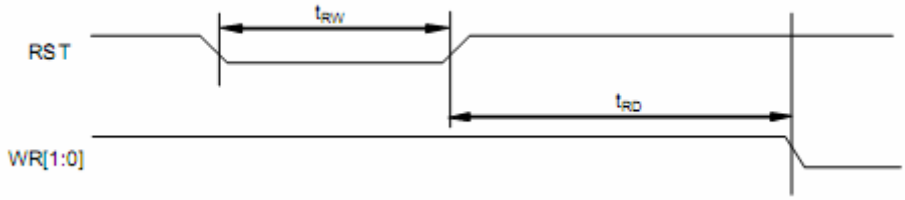


Serial Bus Timing Characteristics(S9)

3.4 Reset Timing

(1.65V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	–	μS
t_{RD}	RST, WR	Reset to WR pulse delay		10	–	mS



Reset Timing Diagram

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4. Function Specifications

4.1 Resetting the LCD module

The LCD module should be initialized by hardware reset, using /RST terminal.
While turning on the VDD and VSS power supply, maintain /RST terminal at LOW level. After the power supply stabilized, release the reset terminal (/RST=HIGH)

4.2 Interfacing Setting

Jumpers could been used to change bus interfacing family

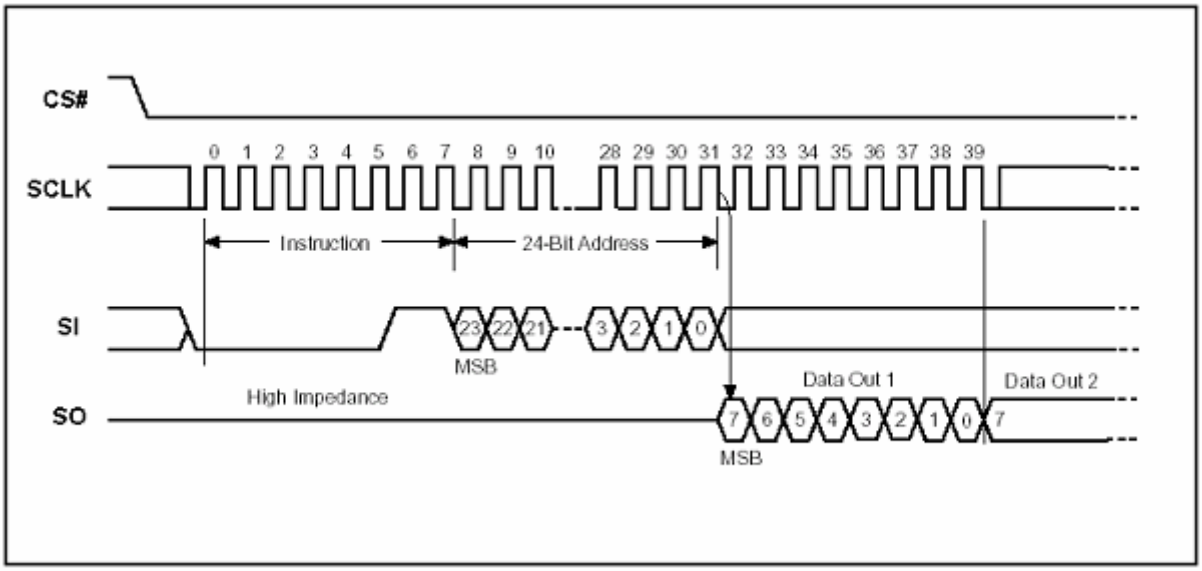
Jumper						Function Discription
JP1	JP2	JP3	JP4	JP5	JP6	
open	close	close	open	close	open	68 mode 8 bit selected
open	close	open	close	close	open	80 mode 8 bit selected
close	open	open	close	open	close	4wire serial *1 <default>

NOTE1:In serial mode, the pin E must been pull down,and other unused control pins and data bus pins been connected to VDD or VSS

4.3 Character ROM

4.3.1 Accessing Character ROM

First, /CS1=L,1byte command(03 or 0B,common speed or fast speed) and 3bytes adress through SI at every SCLK= L→H bit by bit
Second, the data in the adress send out through SO at erery SCLK= H→L bit by bit
Third, only /CS1=H,reading data is finished,otherwise the data in the next adress will be read out



Read Data Bytes Instruction Sequence and Data-out Sequence

NOTE: For details, please refer to GT21L16S2W datasheet.

4.3.2 Instruction Set of using Charactor ROM

Instruction	Description	Instruction Code(One-Byte)		Address Bytes	Dummy Bytes	Data Bytes
READ	Read Data Bytes	0000 0011	03 h	3	—	1 to ∞
FAST_READ	Read Data Bytes at Higher Speed	0000 1011	0B h	3	1	1 to ∞

4.4 Display Pixel Map(example)

1,1	2,1	3,1	4,1	5,1	- - -	- - -	236,1	237,1	238,1	239,1	240,1

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1,2	2,2	3,2	4,2	5,2	- - -	- - -	236,2	237,2	238,2	239,2	240, 2
1,3	2,3	3,3	4,3	5,3	- - -	- - -	236,3	237,3	238,3	239,3	240, 3
: : :	: : :	: : :	: : :	: : :	: : :	: : :	: : :	: : :	: : :	: : :	: : :
1, 78	2, 78	3, 78	4, 78	5, 78	- - -	- - -	236,238	237, 78	238, 78	239, 78	240,78
1, 79	2, 79	3, 79	4, 79	5, 79	- - -	- - -	236, 79	237, 79	238, 79	239, 79	240,79
1, 80	2, 80	3, 80	4, 80	5, 80	- - -	- - -	236, 80	237, 80	238, 80	239, 80	240,80

Pixel mapping (Top View)

Note:

*1. Based on the top view of the LCD module,
the 1, 1 (x, y) pixel is the upper-left pixel;
the 240, 80 (x, y) pixel is the lower-right pixel.

*2. The registet LC[7:6] is set to 01b.

*3

1,1	2,1	3,1	4,1	5,1	6,1
1st byte		2nd byte		3rd byte	

Pixel[1,1]=1st byte D7~D4,Pixel[2,1]=1st byte D3~D0,Pixel[3,1]=2nd byte D7~D4, Pixel[4,1]=2nd byte D3~D0.

*4. For the details of memory mapping please refer to UC1698 datasheet.

4.5 Command Summary

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	Command	D/C	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Product Code, PID, MID}	N/A
				Ver	PMO[6:0]								
				Product Code (8h)				PID[1:0]		MID[1:0]			
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	0	#	#	#	Set CA[6:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Power Control	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7	Set Adv. Program Control	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0 or 1	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
8	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0
9	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0
	Set Row Address MSB	0	0	0	1	1	1	#	#	#	#	Set RA[7:4]	0
10	Set V_{BIAS} Potentiometer	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	40H
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
11	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[8]	0
12	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
13	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set {FLT, FLB}	0
		0	0	#	#	#	#	#	#	#	#		
14	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
15	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
16	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
17	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
18	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0
19	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[4:0]	1DH
				-	-	-	#	#	#	#	#		
20	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)
21	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
22	Set COM Scan Function	0	0	1	1	0	1	1	#	#	#	Set CSF[2:0]	000b
23	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
24	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
25	Set Test Control	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
26	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 12
27	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	159
		0	0	-	#	#	#	#	#	#	#		
28	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
29	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	159
		0	0	-	#	#	#	#	#	#	#		
30	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Shared with MTP commands	Set WPC0	0
		0	0	-	#	#	#	#	#	#	#		
31	Set Window Program Starting Row Address	0	0	1	1	1	1	0	1	0	1		Set WPP0	0
		0	0	#	#	#	#	#	#	#	#		
32	Set Window Program Ending Column Address	0	0	1	1	1	1	0	1	1	0		Set WPC1	127
		0	0	-	#	#	#	#	#	#	#		
33	Set Window Program Ending Row Address	0	0	1	1	1	1	0	1	1	1		Set WPP1	159
		0	0	#	#	#	#	#	#	#	#		
34	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]		0: Inside
35	Set MTP Operation control	0	0	1	0	1	1	1	0	0	0	Set MTPC[4:0]		10H
		0	0	-	-	-	#	#	#	#	#			

Note: *1.For the details, please refer to UC1698 Data sheet.
*2. C/D: 0:Control, 1:Data; W/R: 0: Write Cycle, 1:Read Cycle(Read available in 68 mode); #: Useful Data bIts; - Don't Care

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5. Design and Handling Precaution

1. The LCD panel is made by glass. Any mechanical shock (eg. dropping form high place) will damage the LCD module.
2. Do not add excessive force on the surface of the display, which may cause the Display color change abnormally.
3. The polarizer on the LCD is easily get scratched. If possible, do not remove the LCD protective film until the last step of installation.
4. Never attempt to disassemble or rework the LCD module.
5. Only Clean the LCD with Isopropyl Alcohol or Ethyl Alcohol. Other solvents (eg. water) may damage the LCD.
6. When mounting the LCD module, make sure that it is free form twisting, warping and distortion.
7. Ensure to provide enough space (with cushion) between case and LCD panel to prevent external force adding on it, or it may cause damage to the LCD or degrade the display result.
8. Only hold the LCD module by its side. Never hold LCD module by add force on the heat seal or TAB.
9. Never add force to component of the LCD module. It may cause invisible damage or degrade of the reliability.
10. LCD module could be easily damaged by static electricity. Be careful to maintain an optimum anti-static work environment to protect the LCD module.
11. When peeling off the protective film from LCD, static charge may cause abnormal display pattern. It is normal and will resume to normal in a short while.
12. Take care and prevent get hurt by the LCD panel sharp edge.
13. Never operate the LCD module exceed the absolute maximum ratings.
14. Keep the signal line as short as possible to prevent noisy signal applying to LCD module.
15. Never apply signal to the LCD module without power supply.
16. IC chip (eg. TAB or COG) is sensitive to the light. Strong lighting environment could possibly cause malfunction. Light sealing structure casing is recommend.
17. LCD module reliability may be reduced by temperature shock.
18. When storing the LCD module, avoid exposure to the direct sunlight, high humidity, high temperature or low temperature. They may damage or degrade the LCD module

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