2.4W Stereo Fully Differential Audio Power Amplifier With Stereo Class AB Cap-free Headphone Driver and LDO

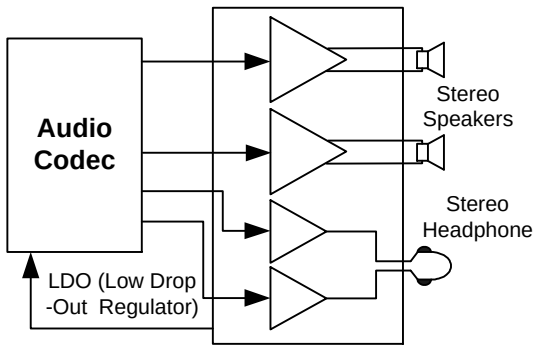
Features

- **Meeting VISTA™ Requirement**
- **Fully Differential Power Amplifier with Excellent RF Rectification Immunity**
- **No Output Capacitor Required for Head Phone Driver**
- **Integrated LDO (Low Dropout Regulator) for Audio Codec (3.3V)**
- **Adjustable Gain Setting for Power Amplifier**
- **A_V=-1.5V/V Fixed Gain Setting for Headphone Driver**
- **Fast Start-up Time**
- **Integrated De-Pop Circuitry**
- **High PSRR (Power Supply Rejection Ratio)**
- **Thermal and Over-Current Protections**
- **Less External Components Required**
- **Space Saving Package**
  – TQFN5x5-32A
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **LCD Monitor**
- **Notebook**
- **Portable DVD**

Simplified Application Circuit



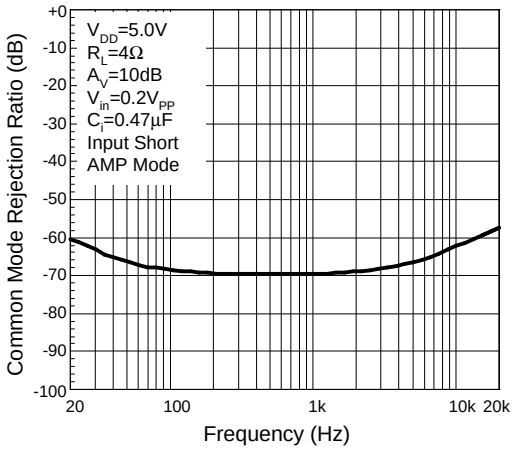
General Description

The APA2061 is a stereo fully differential audio power amplifier with stereo Class-AB cap-free headphone driver and LDO available in a TQFN5X5-32A pins package.

The built-in gain setting at power amplifier can minimize the external component counts. For the flexible application, the gain can be set to 4-steps, 10, 12, 15.6, and 21.6dB by gain control pins (GAIN0 and GAIN1). The power amplifier's fully differential architecture provides high PSRR, increased immunity to noise and RF rectification.

The APA2061 power amplifiers are capable of driving 2.4W at V_{DD}=5V into 4Ω speaker, the cap-free headphone drivers can provide 180mW at HV_{DD}=3.3V into16Ω headphones, and the LDO has a maximum 120mA (3.3V) driver current for audio codec. The APA2061 provides thermal and over-current protections.

The cap-free headphone driver eliminates the DC blocking capacitors at outputs and saves the PCB space. The integration of fully differential power amplifier, cap-free headphone driver, and LDO is a best solution for VISTA™ requirement and it can lower the total BOM costs.



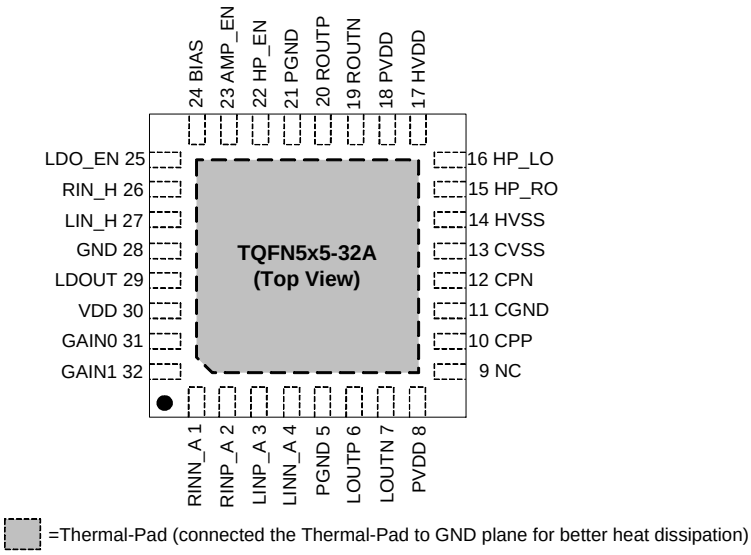
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APA2061 □□□-□□ □ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN5x5-32A Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APA2061 QB : 	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



=Thermal-Pad (connected the Thermal-Pad to GND plane for better heat dissipation)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage (VDD to GND, PVDD to PGND)	-0.3 to 6	V
HV_{DD}	Supply Voltage (HVDD to GND)	-0.3 to 6	
V_{SS}	Supply Voltage (HVSS, CVSS to GND)	-6 to +0.3	
	Input Voltage (RINN_A, RINP_A, LINN_A, LINP_A to GND)	-0.3 to V_{DD}+0.3	
	Input Voltage (RIN_H, LIN_H to GND)	V_{SS}-0.3 to HV_{DD}+0.3	
	Input Voltage (GAIN0, GAIN1, LDO_EN, AMP_EN, HP_EN to GND)	-0.3 to V_{DD}+0.3	
	Input Voltage (PGND, CGND to GND)	-0.3 to +0.3	

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Absolute Maximum Ratings (Cont.) (Note 1)

Symbol	Parameter	Rating	Unit
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	
P_D	Power Dissipation	Internally Limited	W

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient (Note 2) TQFN5X5-32A	40	°C/W
θ_{JC}	Thermal Resistance -Junction to Case (Note 3) TQFN5X5-32A	8	

Note 2: Please refer to " Layout Recommendation", the Thermal-Pad on the bottom of the IC should soldered directly to the PCB's Thermal-Pad area that with several thermal vias connect to the ground plan, and the PCB is a 2-layer, 5-inch square area with 2oz copper thickness**.**

Note 3: The case temperature is measured at the center of the Thermal-Pad on the underside of the TQFN5X5-32A package.

Recommended Operating Conditions

Symbol	Parameter		Range	Unit
V_{DD}	Supply Voltage		4.5 ~ 5.5	V
HV_{DD}	Supply Voltage		3.0 ~ 5.5	
V_{IH}	High Level Input Voltage	GAIN0, GAIN1, LDO_EN, AMP_EN, HP_EN	2 ~ V_{DD}	
V_{IL}	Low Level Input Voltage	GAIN0, GAIN1, LDO_EN, AMP_EN, HP_EN	0 ~ 0.5	
V_{IC}	Common Mode Input Voltage	For Power Amplifier	0.5 ~ V_{DD}-0.5	
		For Headphone Amplifier	HV_{SS} ~ HV_{DD}	
I_{LDOUT}	Output Current (LDOUT)		0 ~ 200	mA
T_A	Ambient Temperature Range		-40 ~ 85	°C
T_J	Junction Temperature Range		-40 ~ 125	
C_{OUT}	LDO Output Capacitor (MLCC type)		1 ~ 100	µF
R_L	Speaker Resistance		4 ~	Ω
R_L	Headphone Resistance		16 ~	

Electrical Characteristics

Refer to the typical application circuits. V_{DD}=5V, HV_{DD}=3.3V, GND=0V, T_A=25°C (unless otherwise noted).

Symbol	Parameter	Test Conditions		APA2061			Unit
				Min.	Typ.	Max.	
$I_{DD(HVDD)}$	Supply Current	V_{AMP_EN}=V_{HP_EN}=V_{LDO_EN}=5V	HV_{DD}	-	2.5	5	mA
$I_{DD(VDD)}$			V_{DD}	-	9	18	

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Electrical Characteristics (Cont.)

Refer to the typical application circuits. V_{DD}=5V, HV_{DD}=3.3V, GND=0V, T_A=25°C (unless otherwise noted).

Symbol	Parameter	Test Conditions		APA2061 Min.	APA2061 Typ.	APA2061 Max.	Unit
$I_{AMP(HVDD)}$	Power Amplifier Supply Current	V_{AMP_EN}=5V, V_{HP_EN}=V_{LDO_EN}=0V	HV_{DD}	-	0.1	0.2	mA
$I_{AMP(VDD)}$			V_{DD}	-	4.5	11	
$I_{HP(HVDD)}$	Headphone Driver Supply Current	V_{HP_EN}=5, V_{AMP_EN}=V_{LDO_EN}=0V	HV_{DD}	-	2.5	5	
$I_{HP(VDD)}$			V_{DD}	-	6	12	
$I_{LDO(HVDD)}$	LDO Supply Current	V_{LDO_EN}=5V, V_{AMP_EN} =V_{HP_EN}=0V	HV_{DD}	-	0.1	0.2	
$I_{LDO(VDD)}$			V_{DD}	-	0.4	0.65	
$I_{SD(HVDD)}$	Shutdown Current	V_{AMP_EN} =V_{HP_EN}=V_{LDO_EN}=0V	HV_{DD}	-	-	2	µA
$I_{SD(VDD)}$			V_{DD}	-	-	5	
I_I	Input Current	GAIN0, GAIN1, LDO_EN, AMP_EN, HP_EN		-	-	1	
SPEAKER MODE, A_V=10dB							
$T_{START-UP}$	Start-Up Time from Shutdown	C_B=0.47µF		-	25	-	ms
R_i	Input Resistor	A_V=10dB		-	76	-	kΩ
		A_V=12dB		-	60	-	
		A_V=15.6dB		-	40	-	
		A_V=21.6dB		17	20	-	
A_V	Closed-Loop Gain	V_{GAIN0}=V_{GAIN1}=0V		9.5	10	10.5	dB
		V_{GAIN0}=0V, V_{GAIN1}=V_{DD}		11.5	12	12.5	
		V_{GAIN0}=V_{DD}, V_{GAIN1}=0V		15.1	15.6	16.1	
		V_{GAIN0}=V_{GAIN1}=V_{DD}		21.1	21.6	22.1	
V_{OS}	Output Offset Voltage	R_L=8Ω		-	5	20	mV
P_O	Output Power	THD+N=1%, f_{in}=1kHz R_L=4Ω R_L=8Ω		1	1.9 1.3	-	W
		THD+N=10%, f_{in}=1kHz R_L=4Ω R_L=8Ω		-	2.4 1.5	-	
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz R_L=4Ω, P_O=1.4W R_L=8Ω, P_O=0.9W		-	0.07 0.05	-	%
Crosstalk	Channel Separation	f_{in}=1kHz R_L=4Ω, Po=200mW R_L=8Ω, Po=130mW		-	-110 -110	-	dB
PSRR	Power Supply Rejection Ratio	f_{in}=217Hz, V_{rr}=0.2V_{rms},R_L=8Ω		-	-75	-	
CMRR	Common Mode Rejection Ratio	f_{in}=1kHz, V_{in}=0.2$V_{rms.}$,R_L=8Ω		-	-65	-	
S/N	Signal-to-Noise Ratio	f_{in}=20~20kHz, With A-weighting Filter R_L=4Ω, P_O=1.4W R_L=8Ω, P_O=0.9W		-	100 100	-	
V_n	Noise Output Voltage	f_{in}=20~20kHz, With A-weighting Filter R_L=8Ω		-	22	-	µVrms

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Electrical Characteristics (Cont.)

Refer to the typical application circuits. V_{DD}=5V, HV_{DD}=3.3V, GND=0V, T_A=25°C (unless otherwise noted).

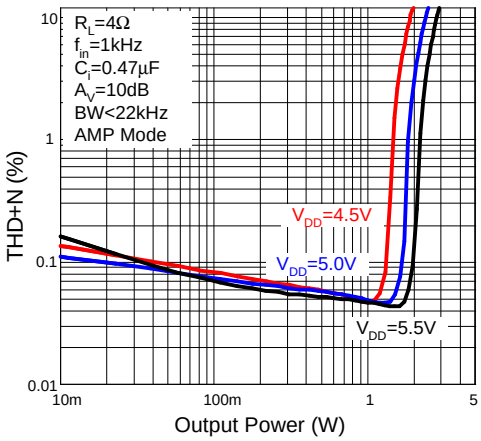
Symbol	Parameter	Test Conditions	APA2061			Unit
			Min.	Typ.	Max.	
HEADPHONE MODE, A_V = -1.5V/V, C_{PF}=C_{PO}=1㎌F(X5R TYPE)						
$T_{START-UP}$	Start-Up Time from Shutdown	C_B=0.47μF	-	10	-	ms
R_i	Input Resistor		17	20	-	kΩ
A_V	Closed-Loop Gain		-1.45	-1.5	-1.55	V/V
V_{OS}	Output Offset Voltage	R_L=32Ω	-	1	5	mV
P_O	Output Power	THD+N=1%, f_{in}=1kHz R_L=16Ω R_L=32Ω	 100	 140 120	 -	mW
		THD+N=10%, f_{in}=1kHz R_L=16Ω R_L=32Ω	 150	 180 160	 -	
V_O	Output Swing Voltage	THD+N=1%, f_{in}=1kHz R_L=320Ω R_L=10kΩ	 1.8	 2.0 2.1	 -	V
		THD+N=10%, f_{in}=1kHz R_L=320Ω R_L=10kΩ	 -	 2.45 2.6	 -	
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz R_L=16Ω, P_O=125mW R_L=32Ω, P_O=88mW R_L=320Ω, V_O=1.5V R_L=10kΩ, V_O=1.6V	 -	 0. 03 0. 02 0. 005 0. 004	 -	%
Crosstalk	Channel Separation	f_{in}=1kHz R_L=16Ω, P_O=16mW R_L=32Ω, P_O=12mW R_L=320Ω, V_O=0.22V R_L=10kΩ, V_O=0.22V	 -	 -82 -82 -77 -77	 -	dB
PSRR	Power Supply Rejection Ratio	f_{in}=217Hz,V_{rr}=0.2V_{rms} R_L=32Ω	-	-80	-	
S/N	Signal-to-Noise Ratio	f_{in}=20~20kHz, With A-weighting Filter R_L=16Ω, P_O=125mW R_L=32Ω, P_O=88mW R_L=320Ω, V_O=1.5V R_L= 10kΩ, V_O=1.6V	 -	 99 100 100 100	 -	
V_n	Noise Output Voltage	f_{in}=20~20kHz, With A-weighting Filter R_L=32Ω	-	15	-	μVrms
LDO (LOW DROP-OUT REGULATOR)						
I_O	Output Current		-	-	120	mA
V_O	Output Voltage	I_O=1mA	3.2	3.3	3.4	V
	Line Regulation	I_O=1mA, V_{DD}=4.5V to 5.5V	-	1.5	5	mV
	Load Regulation	I_O=1mA to 200mA	-	0.03	0.1	mV/mA
PSRR	Power Supply Rejection Ratio	I_O=1mA, f_{in}=120Hz, V_{rr}=0.2V_{rms}	-	-50	-	dB
R_{DIS}	Discharge Resistor		-	50	-	kΩ
CHARGE PUMP, C_{PF}=C_{PO}=1㎌F(X5R TYPE)						
F_{OSC}	Oscillator Frequency		-	450	-	kHz
R_{EQ}	Equivalent Resistance		-	10	-	Ω
CV_{ss}	Negative Output Voltage	No load	-5.1	-5	-4.9	V
R_{DIS}	Discharge Resistor		-	5	-	kΩ

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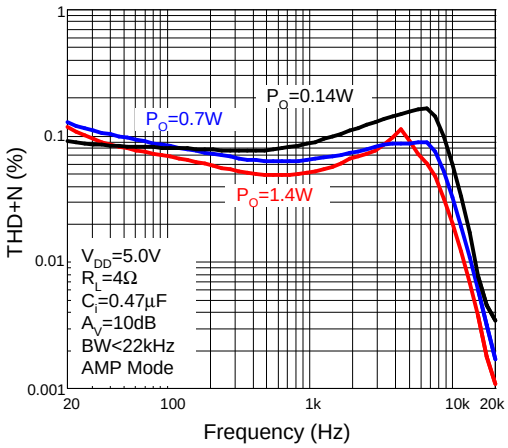
Typical Operating Characteristics

(T_A=+25°C, unless otherwise noted.)

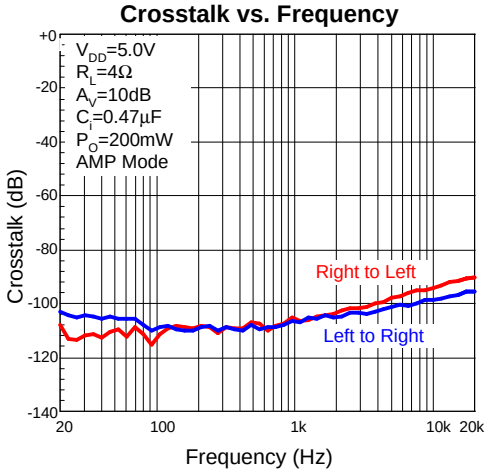
THD+N vs. Output Power



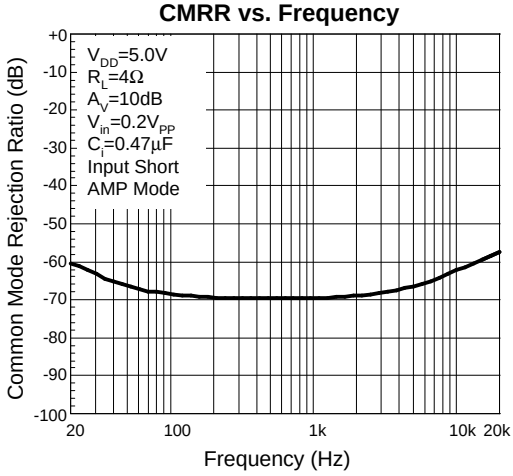
THD+N vs. Frequency



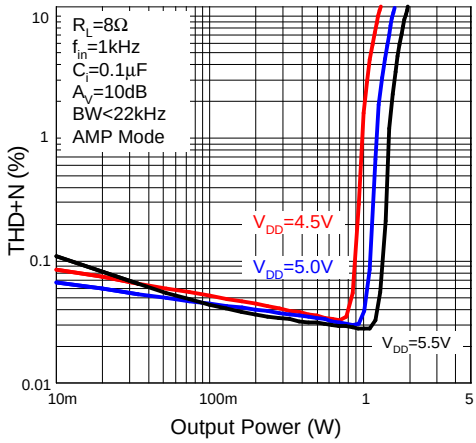
Crosstalk vs. Frequency



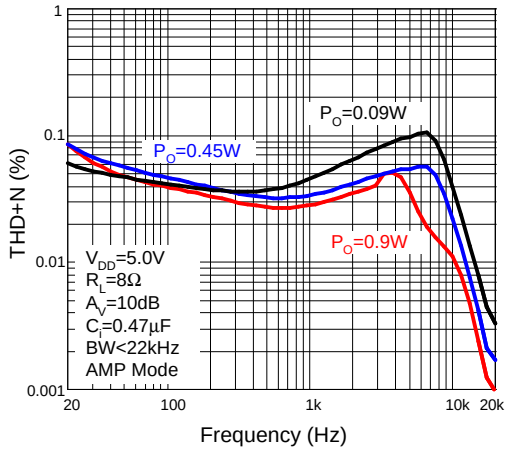
CMRR vs. Frequency



THD+N vs. Output Power



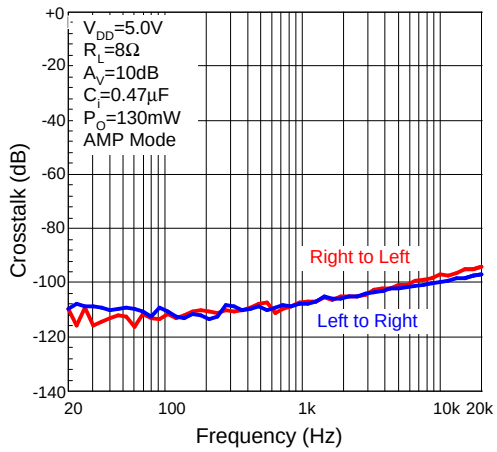
THD+N vs. Frequency



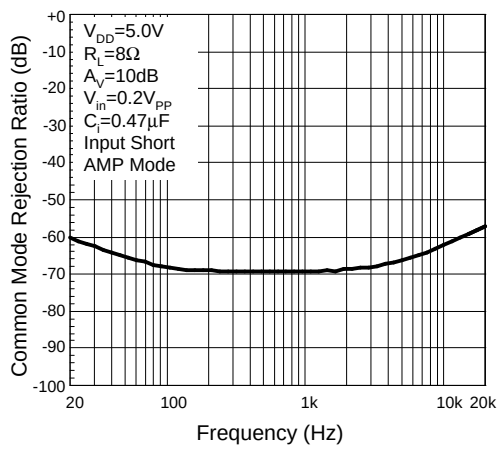
Typical Operating Characteristics (Cont.)

(T_A=+25°C, unless otherwise noted.)

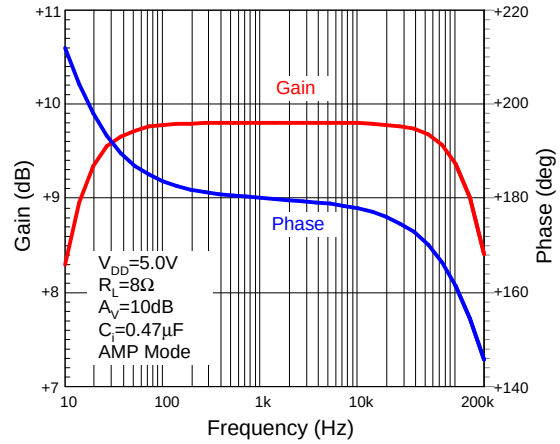
Crosstalk vs. Frequency



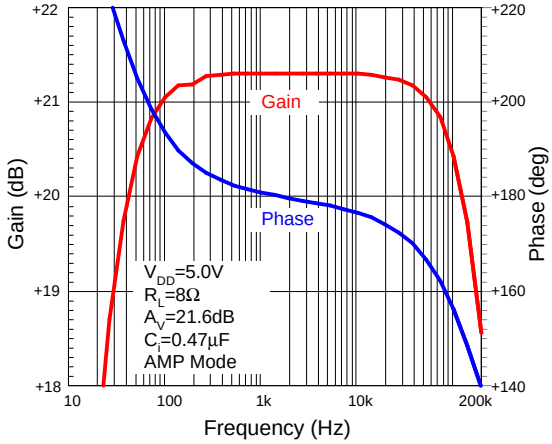
CMRR vs. Frequency



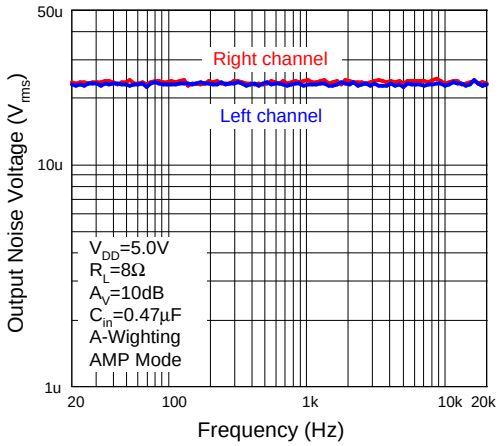
Frequency Response



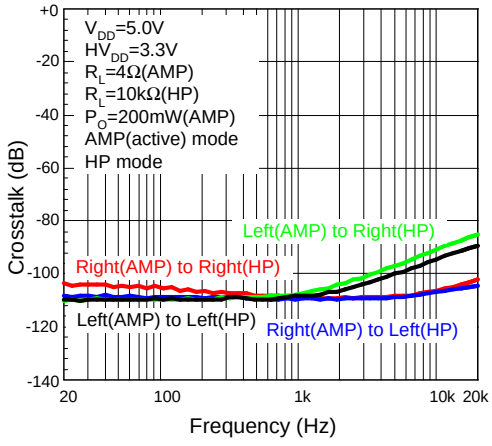
Frequency Response



Output Noise Voltage vs. Frequency



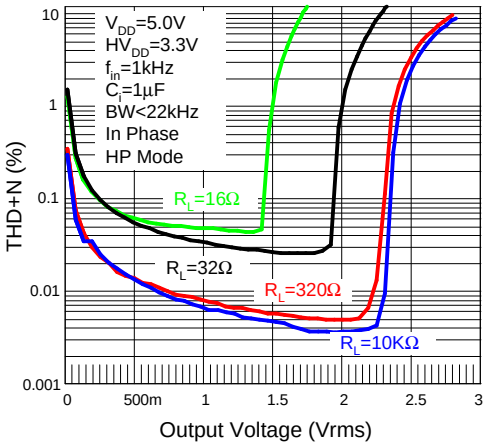
Crosstalk vs. Frequency



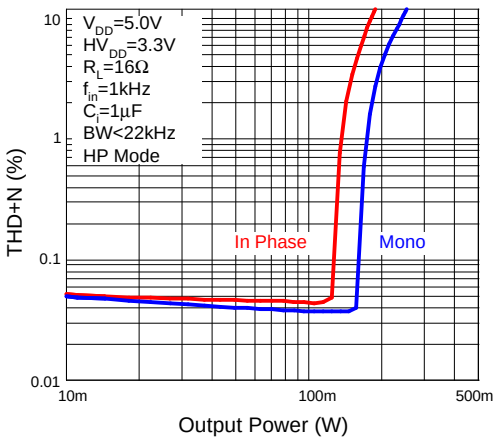
Typical Operating Characteristics (Cont.)

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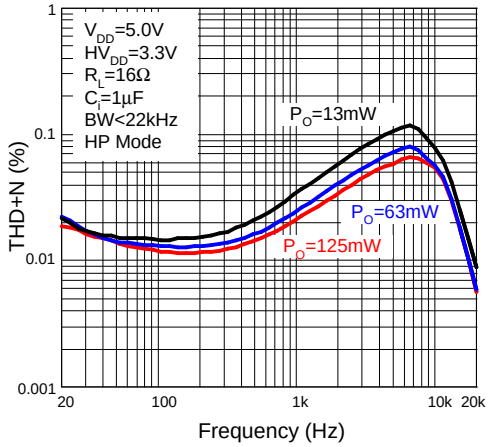
THD+N vs. Output Voltage



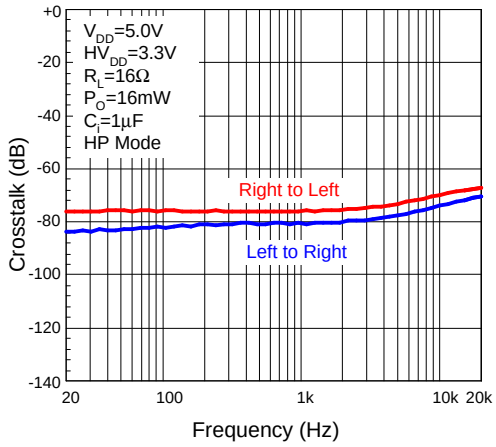
THD+N vs. Output Power



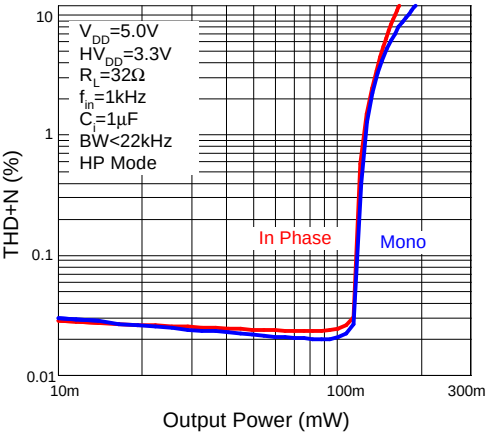
THD+N vs. Frequency



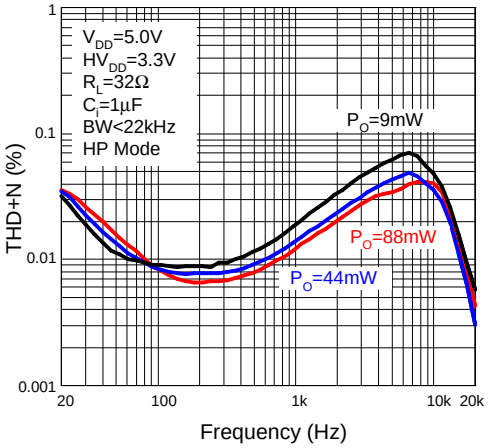
Crosstalk vs. Frequency



THD+N vs. Output Power



THD+N vs. Frequency

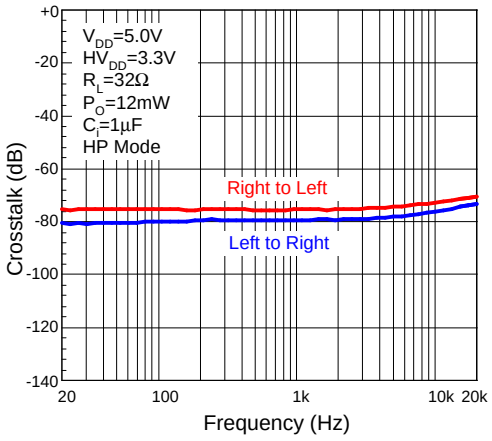


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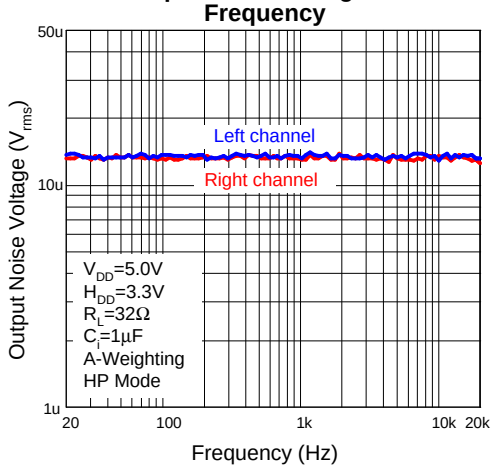
Typical Operating Characteristics (Cont.)

(T_A = +25°C, unless otherwise noted.)

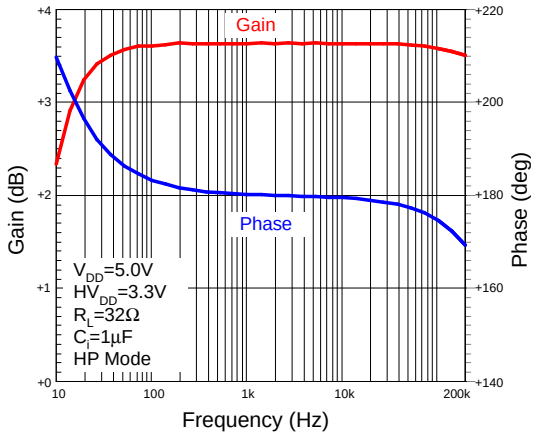
Crosstalk vs. Frequency



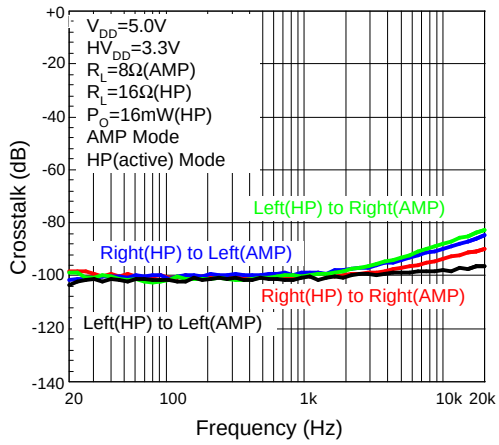
Output Noise Voltage vs. Frequency



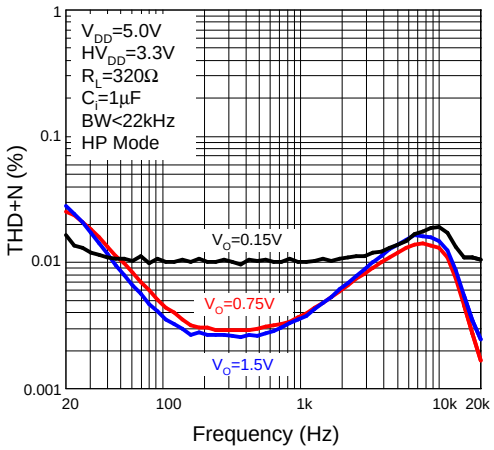
Frequency Response



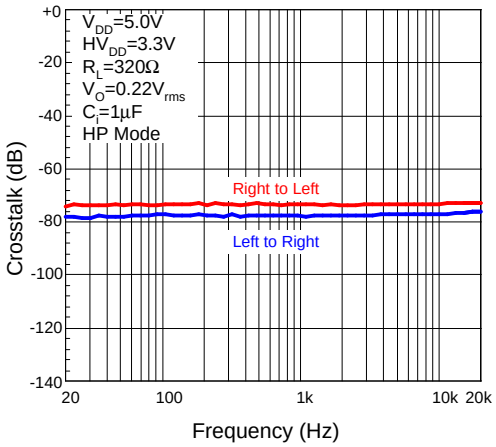
Crosstalk vs. Frequency



THD+N vs. Frequency



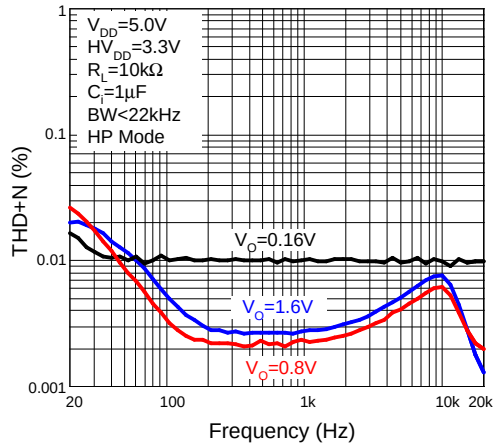
Crosstalk vs. Frequency



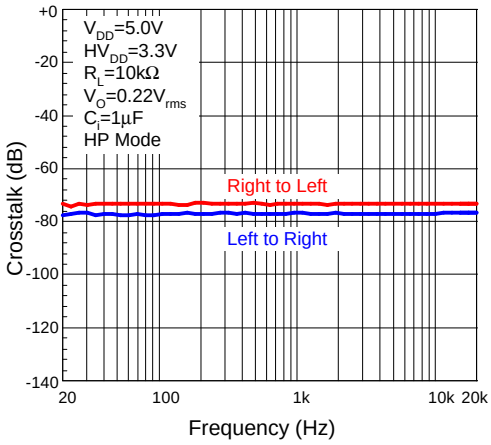
Typical Operating Characteristics (Cont.)

(T_A = +25°C, unless otherwise noted.)

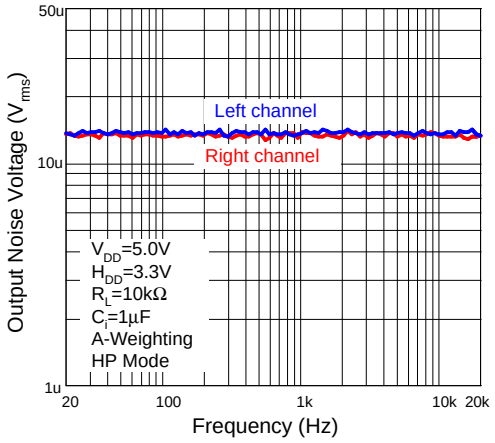
THD+N vs. Frequency



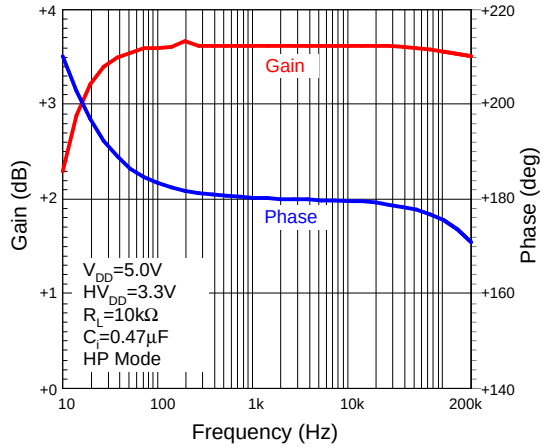
Crosstalk vs. Frequency



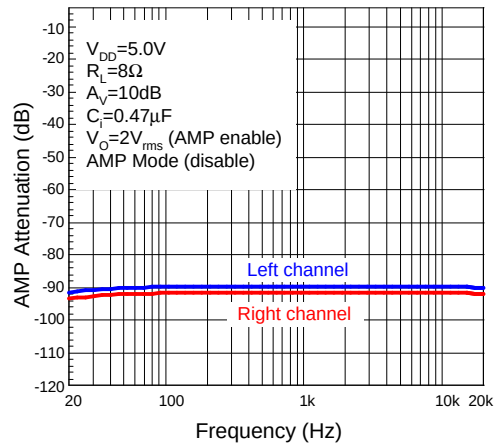
Output Noise Voltage vs. Frequency



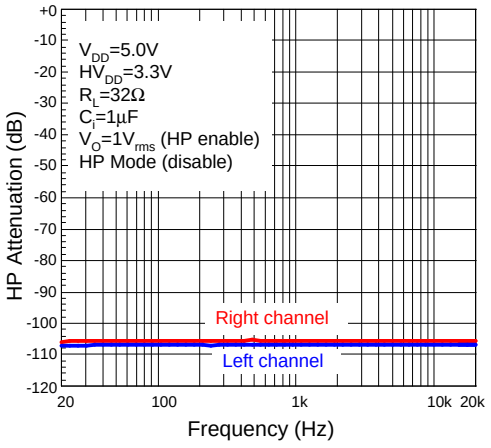
Frequency Response



AMP Attenuation vs. Frequency



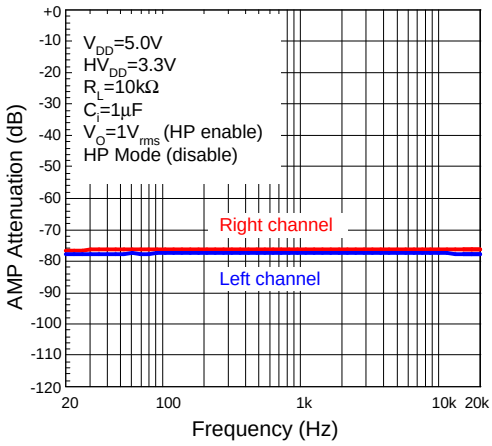
HP Attenuation vs. Frequency



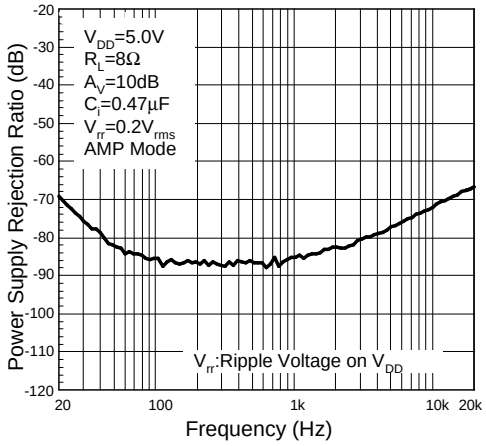
Typical Operating Characteristics (Cont.)

(T_A = +25°C, unless otherwise noted.)

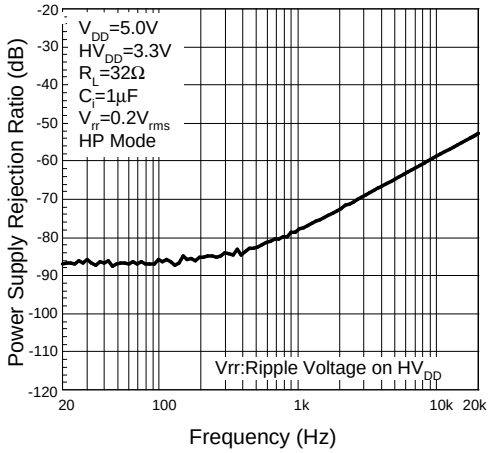
HP Attenuation vs. Frequency



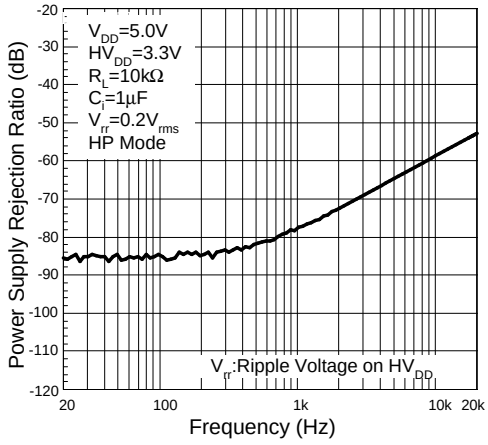
PSRR vs. Frequency



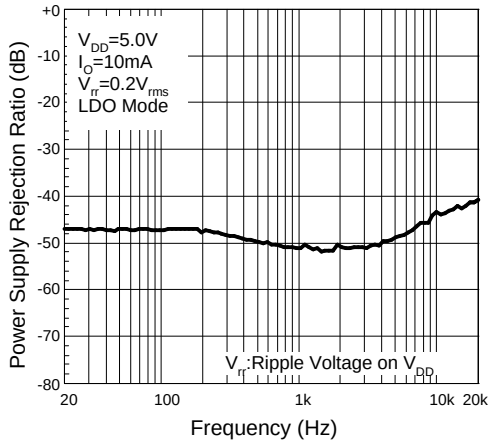
PSRR vs. Frequency



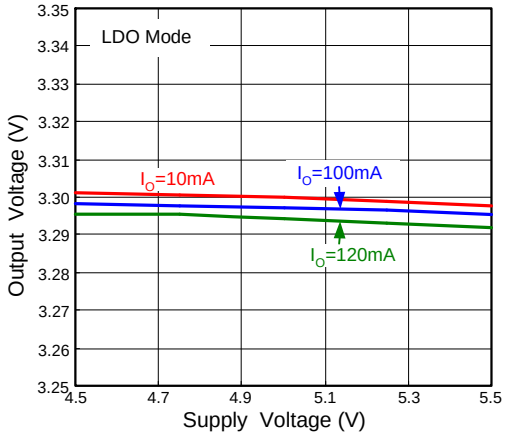
PSRR vs. Frequency



PSRR vs. Frequency



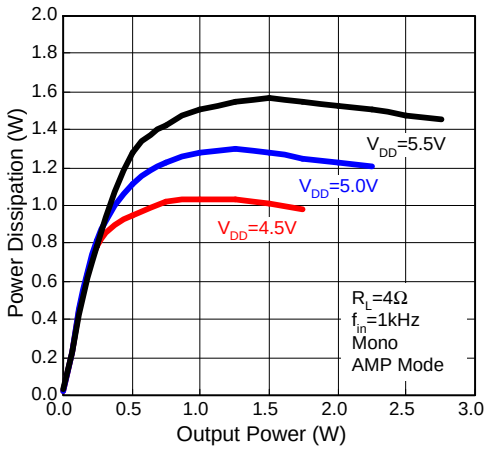
LDO Output Voltage vs. Supply Voltage



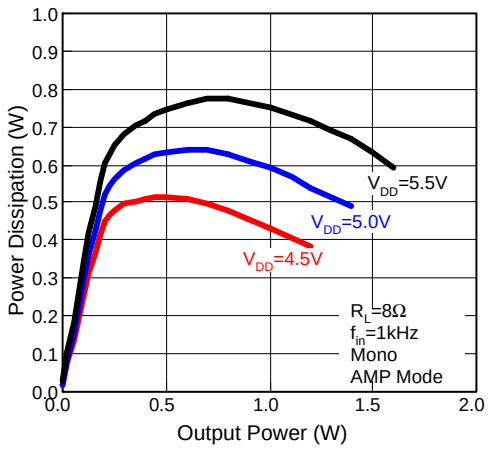
Typical Operating Characteristics (Cont.)

(T_A = +25°C, unless otherwise noted.)

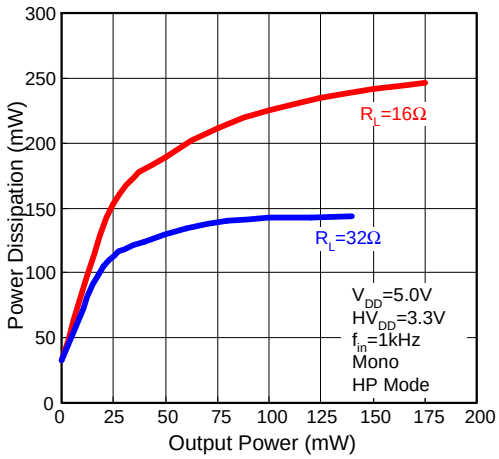
Power Dissipation vs. Output Power



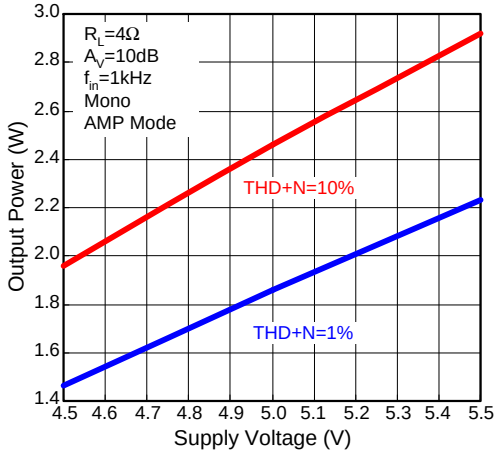
Power Dissipation vs. Output Power



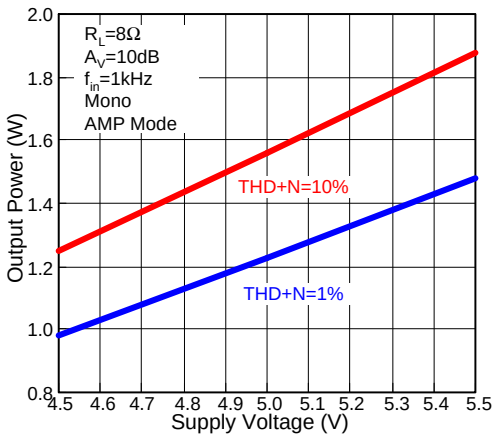
Power Dissipation vs. Output Power



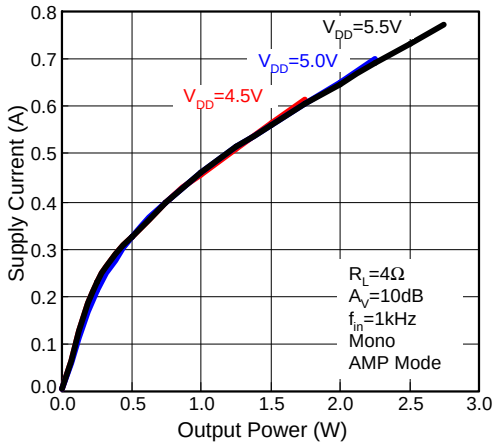
Output Power vs. Supply Voltage



Output Power vs. Supply Voltage



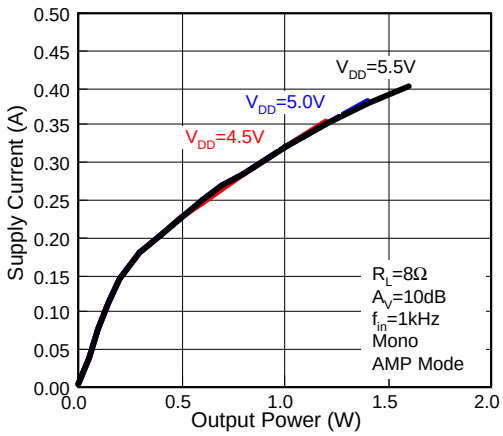
Supply Current vs. Output Power



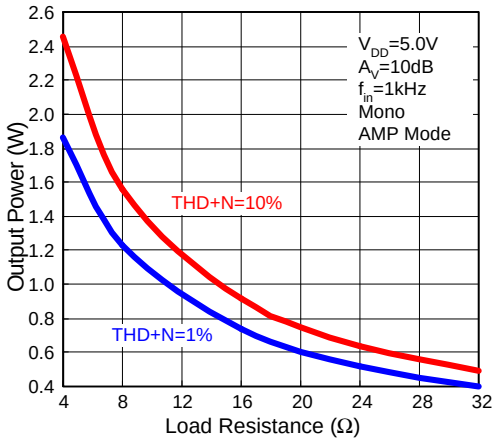
Typical Operating Characteristics (Cont.)

(T_A = +25°C, unless otherwise noted.)

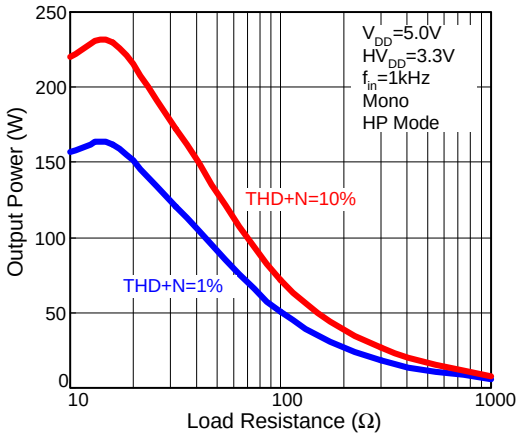
Supply Current vs. Output Power



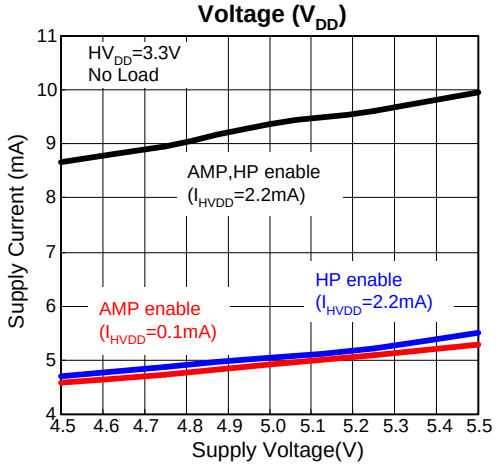
Output Power vs. Load Resistance



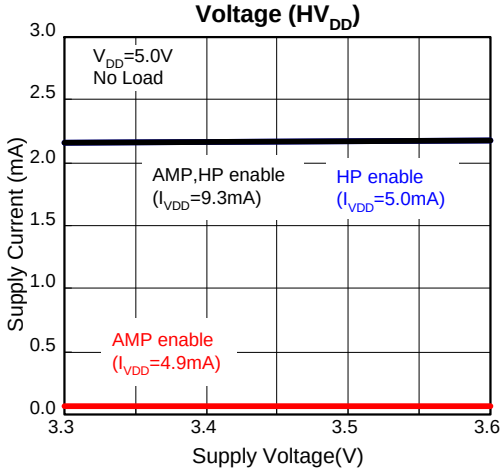
Output Power vs. Load Resistance



Supply Current (I_{VDD}) vs. Supply Voltage (V_{DD})

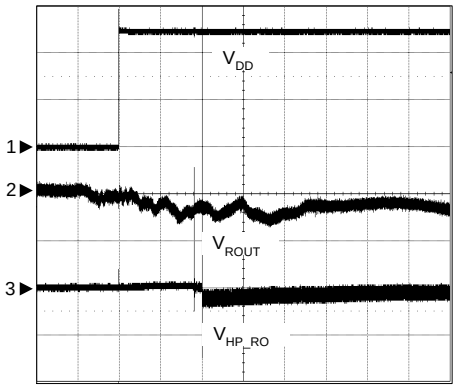


Supply Current (I_{HVDD}) vs. Supply Voltage (HV_{DD})



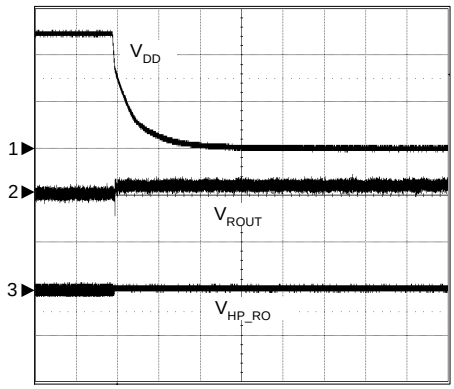
Operating Waveforms

Power On



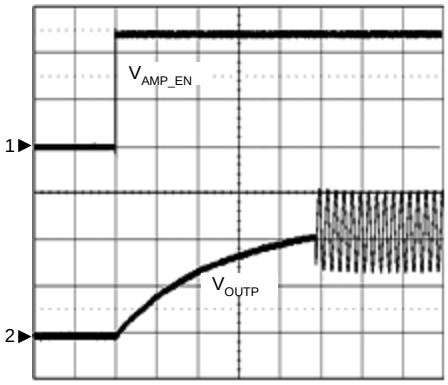
CH1: V_{DD}, 2V/Div, DC
CH2: V_{ROUT}, 20mV/Div, DC
CH3: V_{HP_RO}, 20mV/Div, DC
TIME: 5ms/Div

Power Off



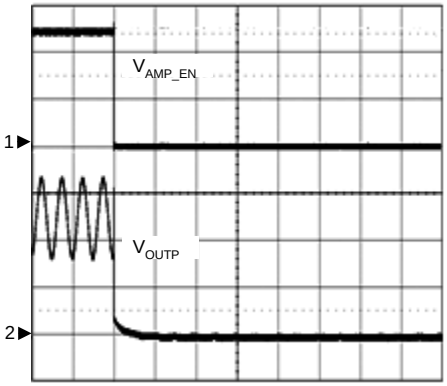
CH1: V_{DD}, 2V/Div, DC
CH2: V_{ROUT}, 20mV/Div, DC
CH3: V_{HP_RO}, 20mV/Div, DC
TIME: 20ms/Div

Speaker Enable



CH1: V_{AMP_EN}, 2V/Div, DC
CH2: V_{OUTP}, 1V/Div, AC
TIME: 5ms/Div

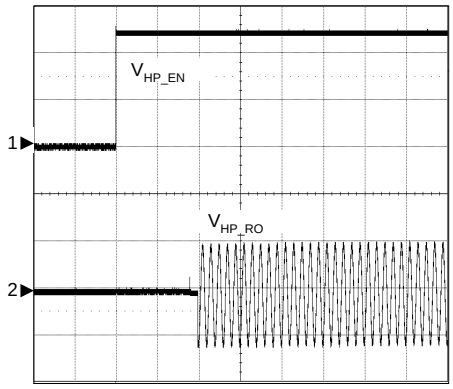
Speaker Disable



CH1: V_{AMP_EN}, 2V/Div, DC
CH2: V_{OUTP}, 1V/Div, AC
TIME: 1ms/Div

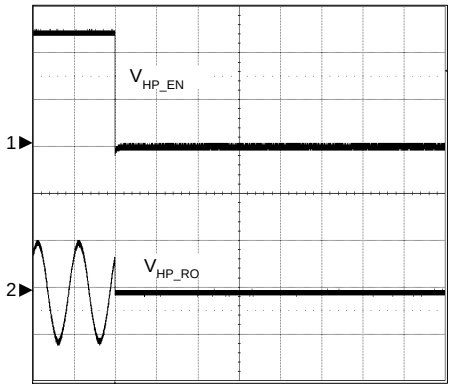
Operating Waveforms (Cont.)

Headphone Enable



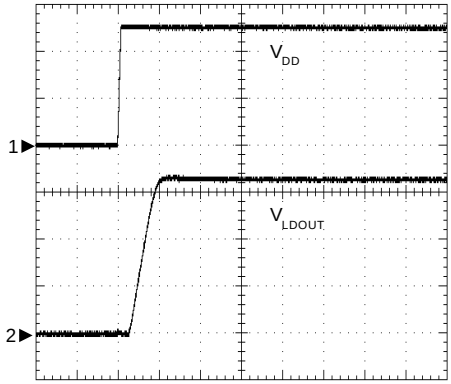
CH1: V_{HP_EN}, 2V/Div, DC
CH2: V_{HP_LO}, 1V/Div, AC
TIME: 5ms/Div

Headphone Disable



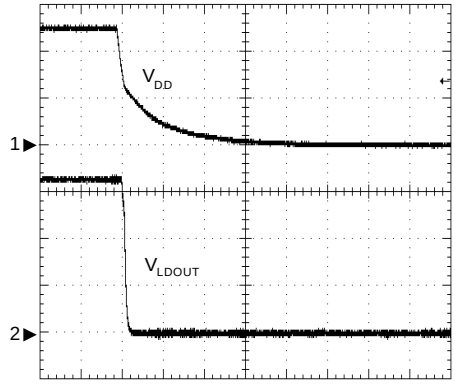
CH1: V_{HP_EN}, 2V/Div, DC
CH2: V_{HP_LO}, 1V/Div, AC
TIME: 1ms/Div

LDO Power On



I_O=120mA
CH1: V_{DD}, 2V/Div, DC
CH2: V_{LDOUT}, 1V/Div, DC
TIME: 100µs/Div

LDO Power Off

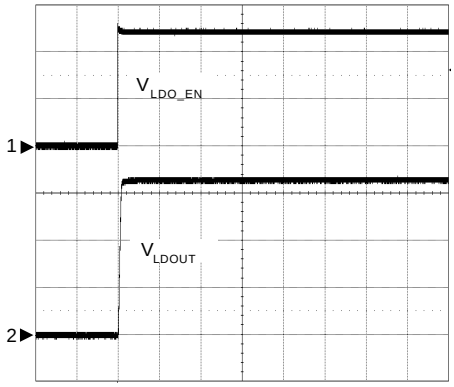


I_O=120mA
CH1: V_{DD}, 2V/Div, DC
CH2: V_{LDOUT}, 1V/Div, DC
TIME: 20ms/Div

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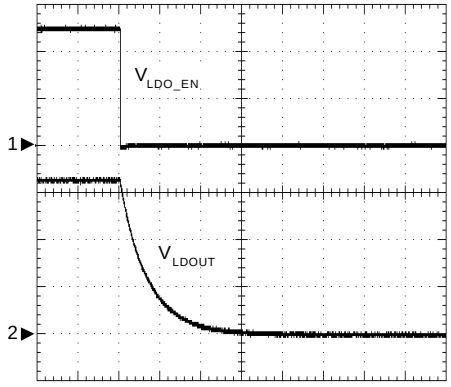
Operating Waveforms (Cont.)

LDO Enable



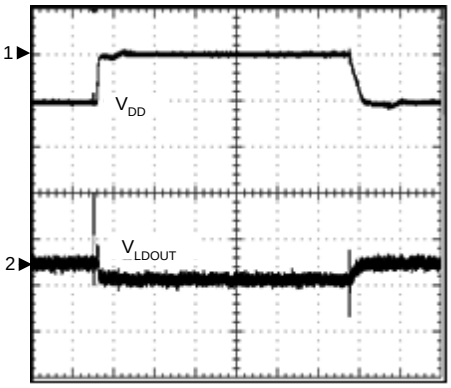
I_O=120mA
CH1: V_{LDO_EN}, 2V/Div, DC
CH2: V_{LDOUT}, 1V/Div, DC
TIME: 1ms/Div

LDO Disable



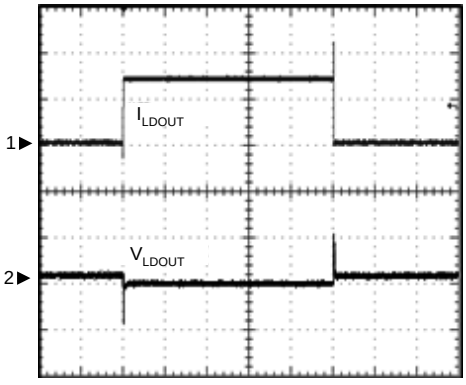
I_O=120mA
CH1: V_{LDO_EN}, 2V/Div, DC
CH2: V_{LDOUT}, 1V/Div, DC
TIME: 1ms/Div

LDO Line Transient



CH1: V_{DD}, 1V/Div, DC
V_{DD} Offset = 5.5V
CH2: V_{LDOUT}, 10mV/Div, DC
V_{LDOUT} Offset = 3.3V
TIME: 200µs/Div

LDO Load Transient

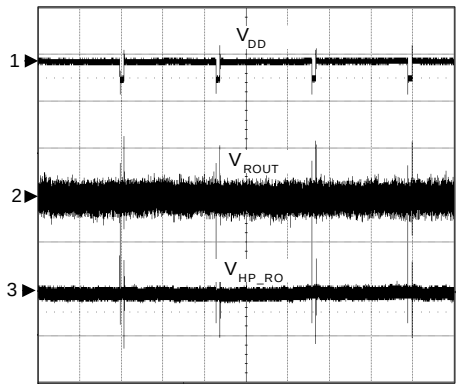


CH1: I_{LDOUT}, 200mA/Div, DC
CH2: V_{LDOUT}, 5mV/Div, DC
V_{LDOUT} Offset = 3.3V
TIME: 200µs/Div

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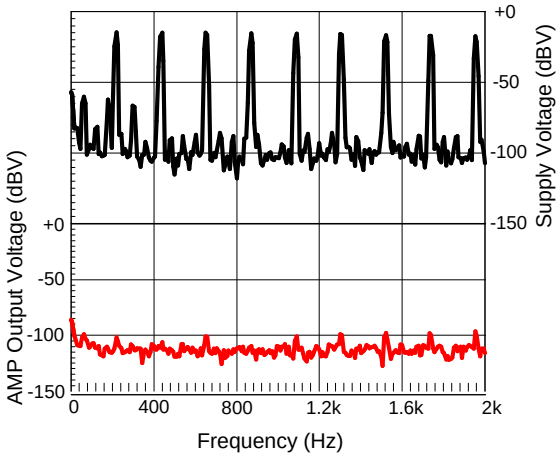
Operating Waveforms (Cont.)

GSM Power Supply Rejection vs. Time

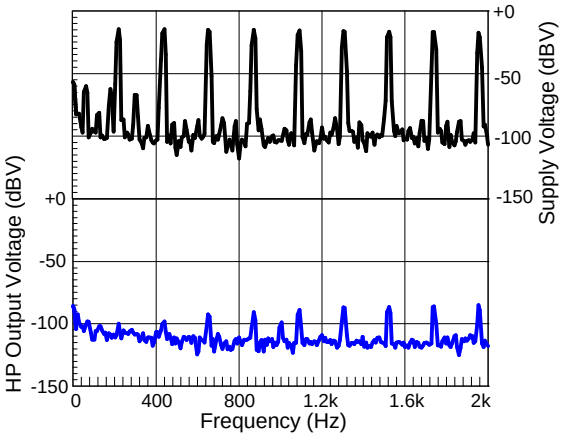


CH1: V_{DD}, 500mV/Div, DC
V_{DD} Offset = 5.0V
CH2: V_{ROUT} , 20mV / Div, DC
CH3: V_{HP_RO} , 20mV / Div, DC
TIME: 2ms/Div

GSM Power Supply Rejection vs. Frequency



GSM Power Supply Rejection vs. Frequency

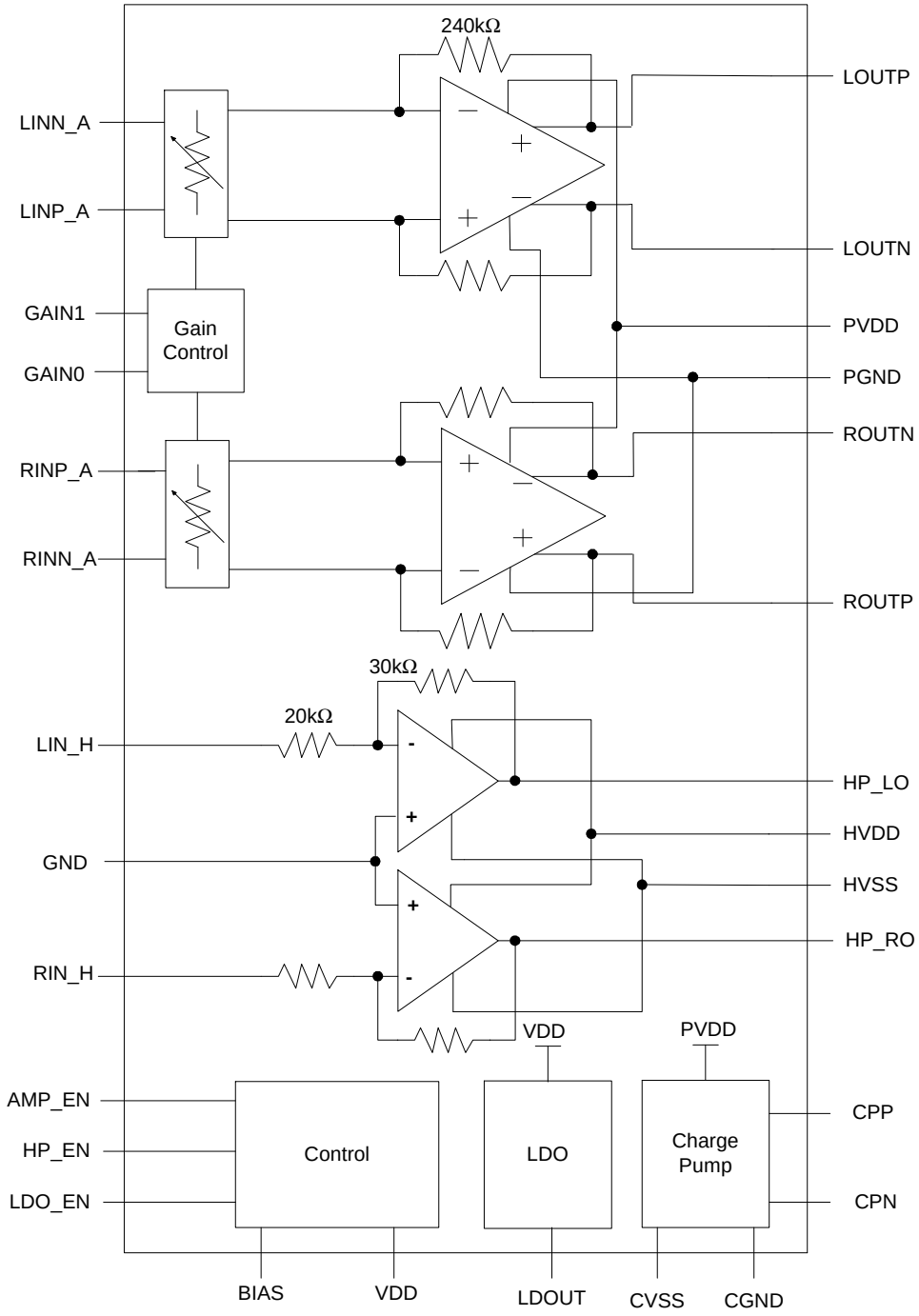


Pin Description

PIN		I/O/P	FUNCTION
NO.	NAME		
1	RINN_A	I	The inverting input pin of right channel power amplifier.
2	RINP_A	I	The non-inverting input pin of right channel power amplifier.
3	LINP_A	I	The non-inverting input pin of left channel power amplifier.
4	LINN_A	I	The inverting input pin of left channel power amplifier.
5,21	PGND	P	Power amplifier's ground
6	LOUTP	O	The positive output pin of left channel power amplifier.
7	LOUTN	O	The negative output pin of left channel power amplifier.
8,18	PVDD	P	Power amplifier's supply voltage pin, connect this pin to VDD.
9	NC	-	No Connection.
10	CPP	I/O	Charge pump flying capacitor positive connection.
11	CGND	P	Charge pump's ground.
12	CPN	I/O	Charge pump flying capacitor negative connection.
13	CVSS	O	Charge pump output pin, connect this pin to the HVSS.
14	HVSS	P	Headphone driver's negative supply voltage pin, connect this pin to CVSS.
15	HP_RO	O	The output pin of right channel headphone driver.
16	HP_LO	O	The output pin of left channel headphone driver.
17	HVDD	P	Headphone driver's positive supply voltage pin.
19	ROUTN	O	The negative output pin of right channel power amplifier.
20	ROUTP	O	The positive output pin of right channel power amplifier.
22	HP_EN	I	Headphone drivers enable input pin; High=Enable.
23	AMP_EN	I	Power amplifiers enable input pin; High=Enable.
24	BIAS	P	Bias voltage for power amplifiers.
25	LDO_EN	I	LDO (Low Drop-Out Regulator) enables input pin; High=Enable.
26	RIN_H	I	The input pin of right channel headphone driver.
27	LIN_H	I	The input pin of left channel headphone driver.
28	GND	P	Control block's ground, connect this pin to CGND and PGND.
29	LDOUT	O	LDO (Low Drop-Out Regulator)'s output pin.
30	VDD	P	Control block and LDO supply voltage pin, connect this pin to PVDD.
31	GAIN0	I	Control pin for internal gain setting, MSB, Bit 1.
32	GAIN1	I	Control pin for internal gain setting, LSB, Bit 0.

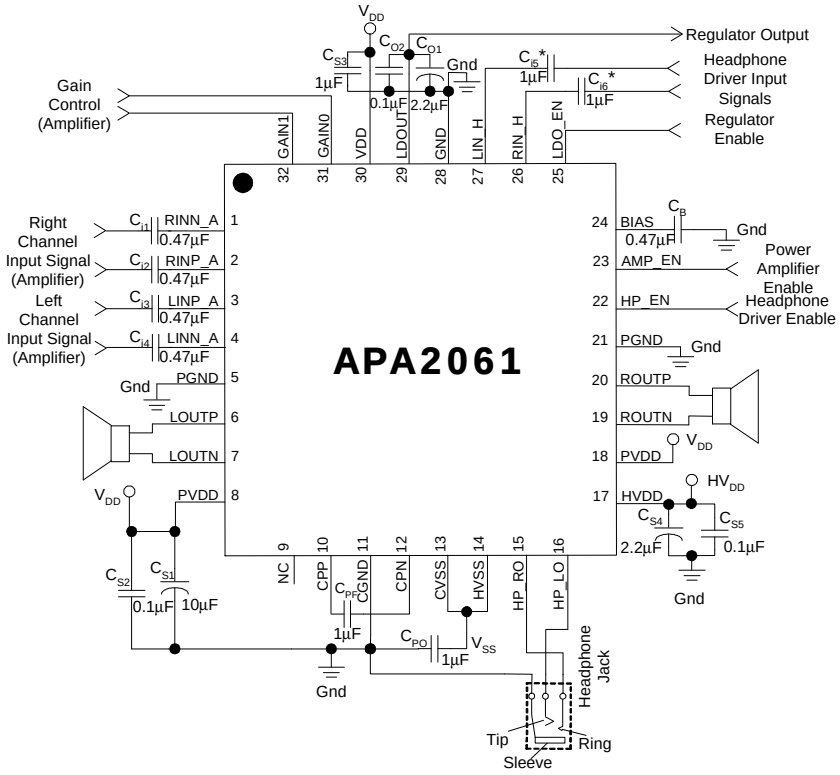
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Block Diagram

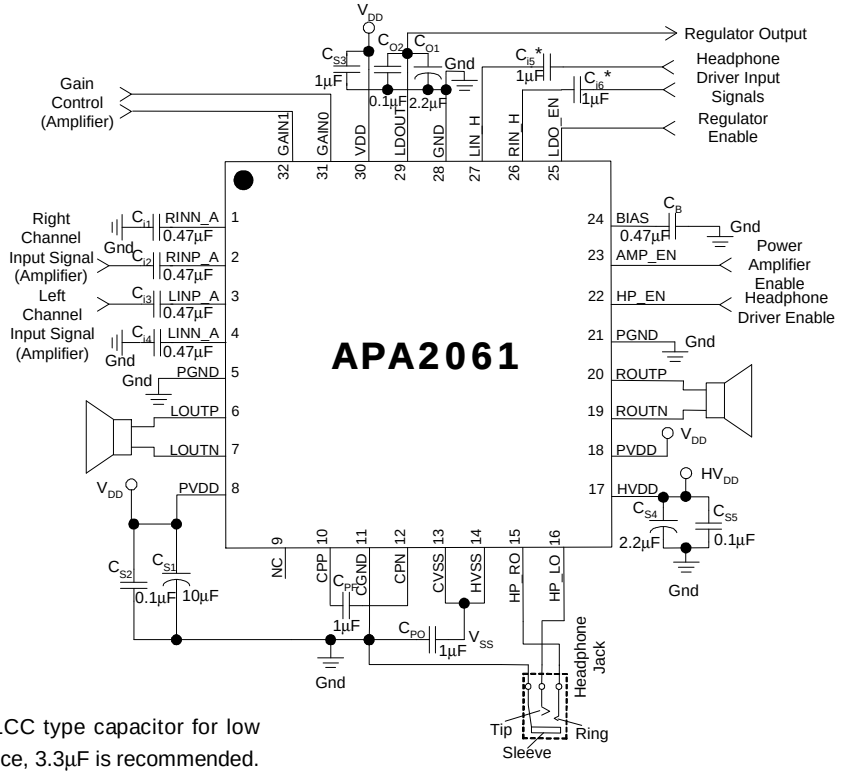


Typical Application Circuit

Differential input mode



Single-ended input mode



Note * : If using MLCC type capacitor for low frequency performance, 3.3µF is recommended.

Function Description

Fully Differential Amplifier

The APA2061's power amplifier is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier has some advantages versus traditional amplifier. Firstly, don't need the input coupling capacitors because the common-mode feedback will compensate the input bias. The inputs can be biased from 0.5V to V_{DD}-0.5V, and the outputs are still biased at mid-supply voltage of the power amplifier. If the inputs are biased out of the input range, the coupling capacitors are required. Secondly, the fully differential amplifier has outstanding immunity against supply voltage ripple (217Hz) caused by GSM RF transmitters' signal, which is better than the typical audio amplifier.

Gain Setting Function

For the convenient uses, the APA2061's power amplifiers provide four gain setting options by GAIN0 and GAIN1 pins.

GAIN0	GAIN1	A_V(dB)	R_i(kΩ)	R_f(kΩ)
0	0	10	60	240
0	1	12	76	240
1	0	15.6	40	240
1	1	21.6	20	240

Headphone Mode Operation

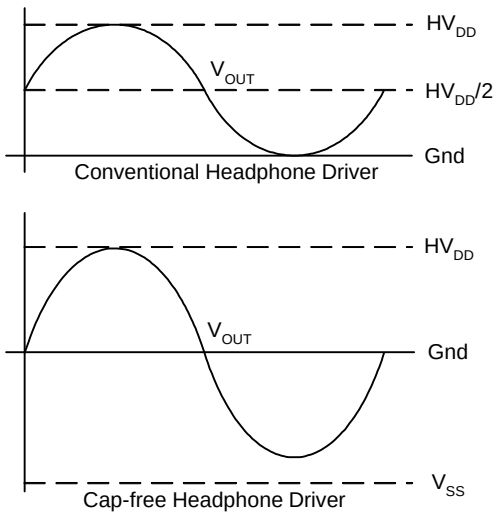


Figure 1: The Cap-Free Headphone Driver's Operation

The Cap-free headphone drivers use a charge pump to invert the positive power supply (V_{DD}) to the negative power supply (V_{SS}) (see Figure 1). The headphone amplifiers operate at this bipolar power supply, and the outputs reference refers to the ground. This feature eliminates the output capacitor that using in conventional single-ended headphone amplifiers. In addition, the power supply rail for Cap-free headphone drivers has almost 1.5X compare to the single power supply rail headphone drivers.

Thermal Protection

The thermal protection circuit limits the junction temperature of the APA2061. When the junction temperature exceeds T_J = +150°C, a thermal sensor turns off the amplifier, allowing the devices to cool. The thermal sensor allows the amplifier to start-up after the junction temperature down about 125 °C. The thermal protection is designed with a 25 °C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the ICs.

Over-Current Protection (OCP)

- The power amplifier monitors the output buffers' current. When the over-current occurs, the output buffers' current will be reduced and limited to a fold-back current level. The power amplifier will go back to normal operation until the over-current current situation has been removed. In addition, if the over-current period is long enough and the IC's junction temperature reaches the thermal protection threshold, the IC enters thermal protection mode.
- The LDO regulator provides a current-limit circuitry, which monitors and controls P-channel MOS's gate voltage, limiting the output current to 0.4A. For reliable operation, the device should not be operated in current-limit for extended period time. When the output voltage drops below 0.6V, which is caused by the over load or short circuit, the internal short circuit current-limit circuitry limits the output current down to 250mA. The short circuit current-limit is used to reduce the power dissipation during short circuit condition. The short circuit current-limit has a blanking time feature after the under-voltage lockout threshold is reached, therefore, it will avoid the output causing short circuit current-limit protection during start-up; the blanking time is about 600μs.

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Function Description (Cont.)

Over-Current Protection (OCP) (Cont.)

- The charge pump monitors the output voltage (V_{SS}). In addition, it has an over-voltage protection to avoid over-current occuring on headphone driver's output. When the output voltage (V_{SS}) is greater than –2V, the charge pump will turn off the charge pump's output. The charge pump's output will turn on again if the situation has been removed. Typical under voltage protection threshold is -2V with 0.5V hysteresis.

Low Drop-Out (LDO) Regulator

The LDO regulator's output provides maximum 120mA drive capacity for external audio codec. A 2.2µF decoupling capacitor with 0.1µf capacitor (filtering the high frequency noise) is recommended at LDO regulator's output. The LDO regulator has built-in under-voltage lockout circuits to keep the output shutting off until internal circuitry is operating properly. The under-voltage lockout function initiates a soft-start process after input voltage exceeds its rising under-voltage lockout threshold during power on. The internal soft-start circuit controls the rise rate of the output voltage and limits the current surge during start-up. Approximate 20µs delay time after the VDD is over the under-voltage lockout threshold; the LDO regulator's output voltage starts the soft-start. The typical soft-start interval is about 130µs and the under-voltage lockout threshold is 2.5V with 0.15V hysteresis.

Enable Mode

The APA2061 provides the independent enable control functions and allows user disable any main circuit blocks when not in using, and these can save the power consumption. In addition, if either the power amplifier or the headphone driver is disabled, the released time will happen immediately when enable the power amplifier or the headphone driver. However, if both the power amplifier and the headphone driver are disabled at the same time, the released time will be the $T_{START-UP}$ Time when enable one of them. Disable all blocks (V_{AMP_EN}=V_{HP_EN}= V_{LDO_EN}=0V), The APA2061 enters the shutdown mode, and only consumption 5µA(Max.) at V_{DD} supply current and 2µA(Max.) at HV_{DD} supply current.

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Application Information

Windows Vista™ Premium Mobile Requirement

Device Type	Requirement	Value	APA2061 typical performance
Analog Line Output Jack (R_L=10kΩ)	Full Scale Output voltage	≥0.707V_{rms}	2.3V_{rms}
	THD+N	≤-65dBFS 20Hz~20kHz	-70dB 20Hz~20kHz
	Line output cross-talk	≤-50dB, 20Hz~15kHz	-70dB 20Hz~20kHz
	Noise level during system activity	≤-80dBFS A-weighting	-100dBFS A-weighting
Analog Headphone Output Jack (R_L=320Ω)	Full Scale Output voltage	≥0.707V_{rms}	2.3V_{rms}
	THD+N	≤-65dBFS 100Hz~20kHz	-78dB 100Hz~20kHz
	Headphone output cross-talk	≤-50 dB 100Hz~15kHz	-75 dB 100Hz~15kHz
	Noise level during system activity	≤-80dBFS A-weighting	-100dBFS A-weighting
Analog Headphone Output Jack (R_L=32Ω)	Full Scale Output voltage	≥0.3V_{rms}	2.0V_{rms}
	THD+N	≤-45dBFS 100Hz~20kHz	-68dB 100Hz~20kHz
	Headphone output cross-talk	≤-50dB 100Hz~15kHz	-70 dB 100Hz~15kHz
	Noise level during system activity	≤-80dBFS A-weighting	-100dBFS A-weighting

Input Capacitor (C_i)

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the minimum input impedance R_i form a high-pass filter with the corner frequency is determined in the following equation:

$$f_{C(highpass)} = \frac{1}{2\pi R_i C_i} \quad (1)$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. Consider the example where R_i is 20kΩ and the specification calls for a flat bass response down to 40Hz. The equation is reconfigured as below :

$$C_i = \frac{1}{2\pi R_i f_c} \quad (2)$$

When input resistance varation is considered, the value of C_i is 0.2µF. Therefore, a value in the range from 0.22µF to 1.0µF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i + R_f, C_i) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitors should face the amplifiers' inputs in most applications because the DC level of the amplifiers' inputs are held at V_{DD}/2. Please note that it is important to confirm the capacitor polarity in the application.

Power Supply Decoupling Capacitor, C_s

The APA2061 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) to be as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, (0.1µF typically) placed as close as possible to the device VDD lead works best.

For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

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Application Information (Cont.)

Charge Pump Flying Capacitor (C_{PF})

The flying capacitor affects the load transient of the charge pump. If the capacitor's value is too small, it will degrade the charge pump's current driver capability and the performance of headphone amplifier. Increasing the flying capacitor's value will improve the load transient of charge pump. Recommend using the low ESR ceramic capacitors (X5R type is recommended) above 1µf.

Charge Pump Output Capacitor (C_{PO})

The output capacitor's value affects the power ripple directly at V_{SS}. Increasing the value of output capacitor will reduce the power ripple. The ESR of output capacitor affects the load transient of V_{SS}. Low ESR and greater than 1µf ceramic capacitor (X5R type is recommended) is recommendation.

Layout Recommendation

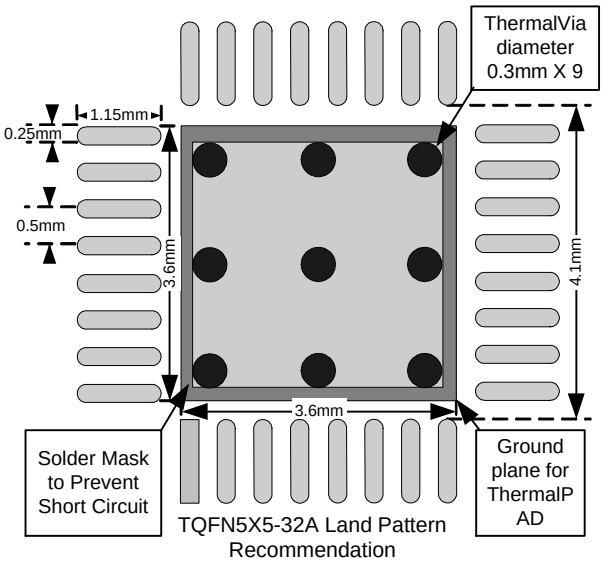


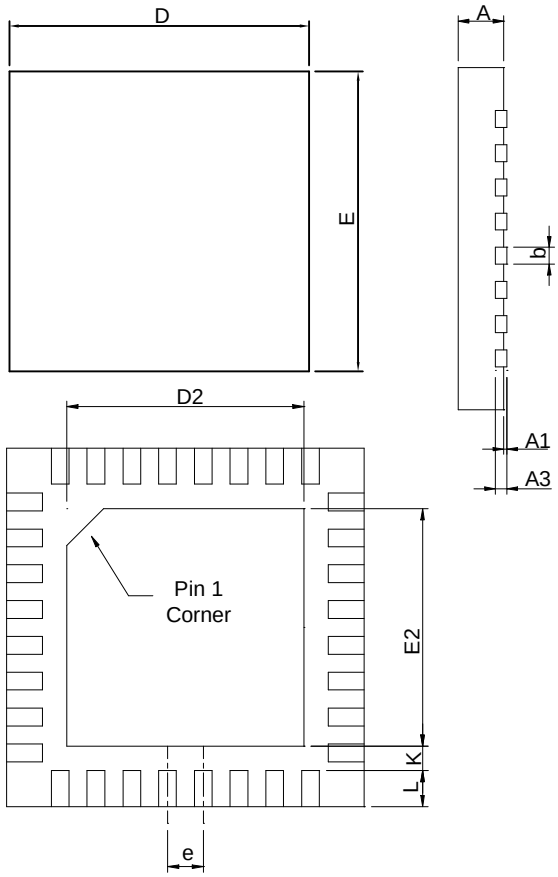
Figure 5. TQFN5X5-32A Land Pattern Recommendation

1. All components should be placed close to the APA2061. For example, the input capacitor (C_I) should be close to APA2061's input pins to avoid causing noise coupling to APA2061's high impedance inputs; the decoupling capacitor (C_S) should be placed by the APA2061's power pin to decouple the power rail noise.
2. The output traces should be short, wide (>50mil), and symmetric.
3. The input trace should be short and symmetric.
4. The power trace width should greater than 50 mil.
5. The TQFN5x5-32A thermal pad should be soldered on PCB, and the ground plane needs solded mask (to avoid short circuit) except the thermal pad area.

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Package Information

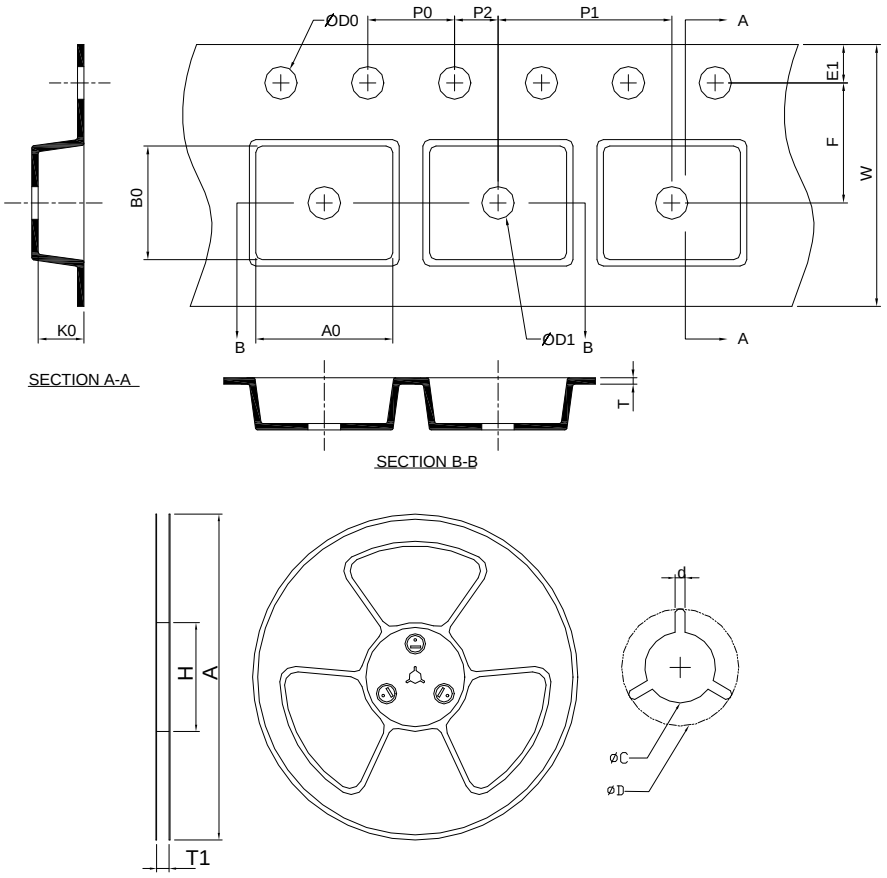
TQFN5x5-32A



SYMBOL	TQFN5x5-32A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	4.90	5.10	0.193	0.201
D2	3.10	3.50	0.122	0.138
E	4.90	5.10	0.193	0.201
E2	3.10	3.50	0.122	0.138
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	

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Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN5x5-32A	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.30±0.20	5.30±0.20	1.30±0.20

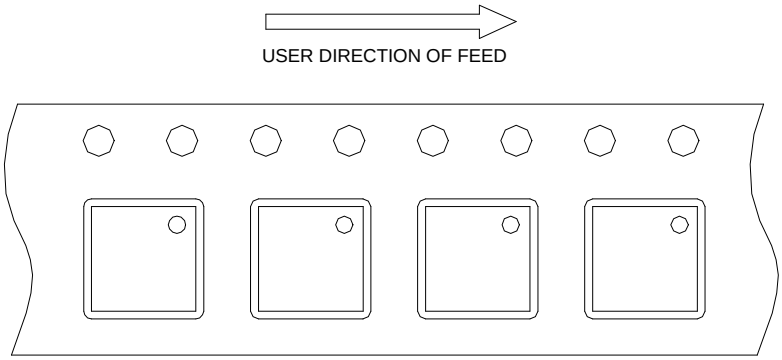
(mm)

Devices Per Unit

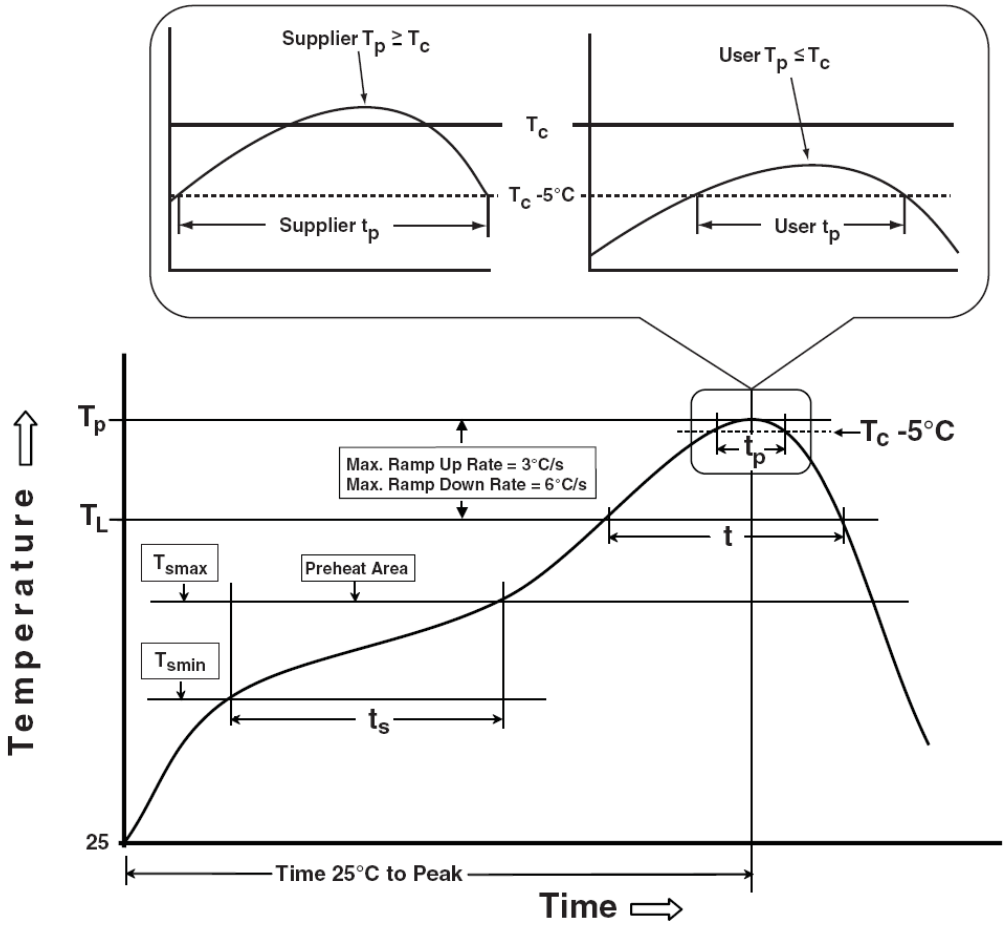
Package Type	Unit	Quantity
TQFN5x5-32A	Tape & Reel	2500

Taping Direction Information

TQFN5x5-32A



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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