PI6LC48P04

4-Output LVPECL Networking Clock Generator

Features

- Four differential LVPECL output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended clock input
- Supports the following output frequencies: 212.5MHz, 159.375MHz, 106.25MHz, 53.125MHz, 156.25MHz, 187.5MHz
- RMS phase jitter @ 212.5MHz, using a 26.5625MHz crystal (12kHz – 20MHz): 0.3ps (typical)
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free package: 24-TSSOP

Description

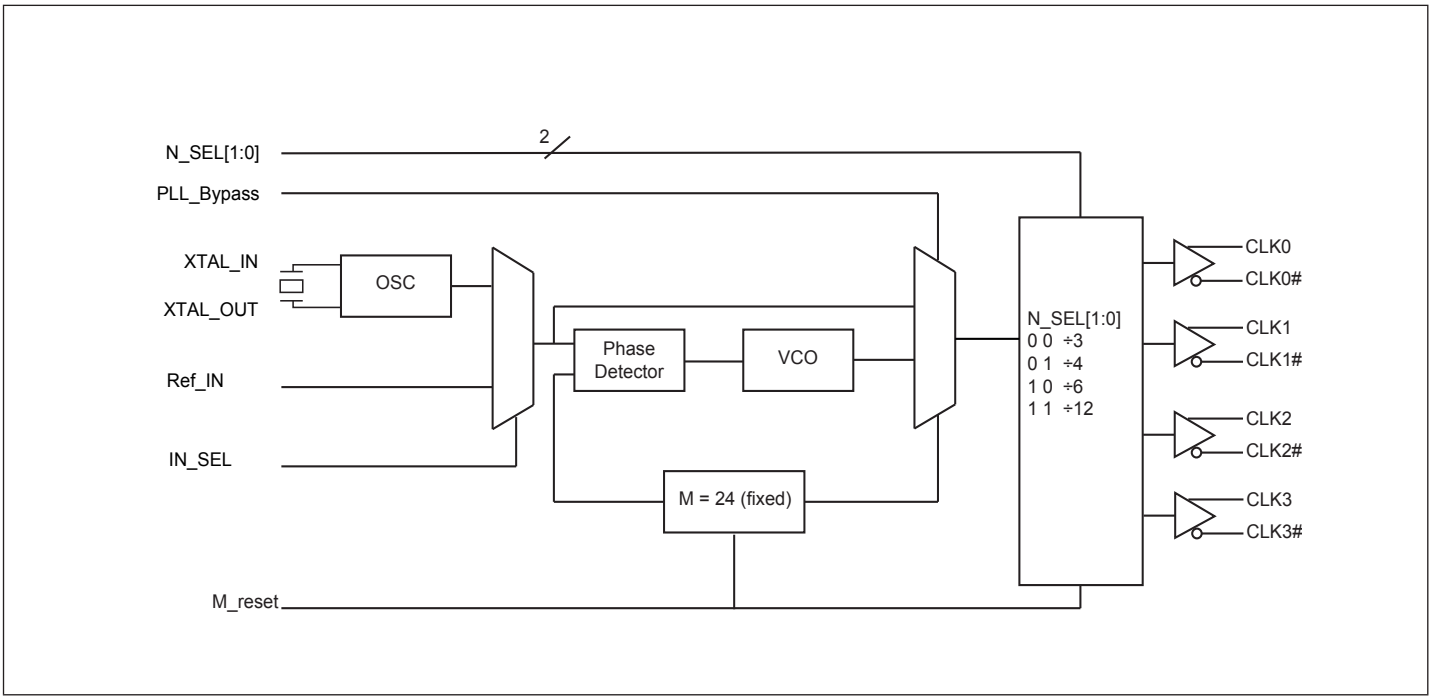
The PI6LC48P04 is a 4-output LVPECL synthesizer optimized to generate Ethernet and Fibre Channel reference clock frequencies and is a member of Pericom's HiFlex family of high performance clock solutions. Using a 26.5625MHz or a 26.04166MHz crystal, the following frequencies can be generated based on the settings of 2 frequency select pins (N_SEL[1:0]): 212.5MHz, 159.375MHz, 106.25MHz, 53.125MHz, and 156.25MHz.

The PI6LC48P04 uses Pericom's proprietary low phase noise VCO technology and can achieve less than 1ps typical rms phase jitter, so it is ideal for Ethernet interface in all kind of systems.

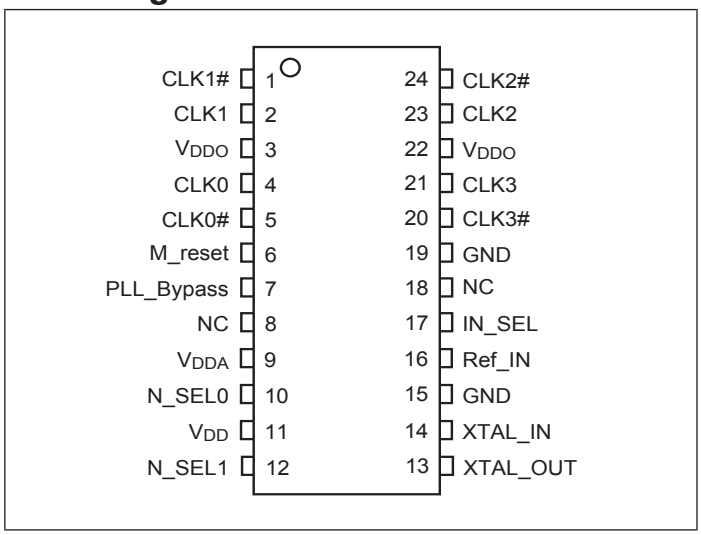
Applications

- Networking systems

Block Diagram



Pin Configuration



Pinout Table

Pin No.	Pin Name	I/O Type		Description
1, 2	CLK1#, CLK1	Output		LVPECL Output Clock 1
3, 22	V_{DDO}	Power		Output supply pins
4, 5	CLK0, CLK0#	Output		LVPECL Output Clock 0
6	M_reset	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and outputs are enabled.
7	PLL_Bypass	Input	Pulldown	Selects either the PLL or the active input reference to be routed to the output dividers. When LOW, selects PLL (PLL enable). When HIGH, selects the reference clock (PLL bypass).
8, 18	NC			Not connected
9	V_{DDA}	Power		Analog power supply
10, 12	N_SEL0, N_SEL1	Input	Pulldown	Frequency select pins
11	V_{DD}	Power		Core power supply
13, 14	XTAL_OUT, XTAL_IN	Output / Input		Parallel resonant crystal interface. XTAL_OUT is the output, and XTAL_IN is the input.
15, 19	GND	Power		Ground
16	Ref_IN	Input	Pulldown	CMOS reference clock input
17	IN_SEL	Input	Pulldown	Selects between the single-ended Ref_IN or crystal interface as the PLL reference source. When HIGH, selects Ref_IN. When LOW selects XTAL inputs.
20, 21	CLK3#, CLK3	Output		LVPECL Output Clock 3
23, 24	CLK2, CLK2#	Output		LVPECL Output Clock 2

Frequency Select Function Table

Inputs						Output Frequency (MHz)
Input Frequency (MHz)	N_SEL1	N_SEL0	M Div. Value	N Div. Value	M/N Div. Value	
26.5625	0	0	24	3	8	212.5
26.5625	0	1	24	4	6	159.375
26.5625	1	0	24	6	4	106.25
26.5625	1	1	24	12	2	53.125
26.04166	0	1	24	4	6	156.25
23.4375	0	0	24	3	8	187.5

Typical Crystal Requirement

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			26.5625		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

Recommended Crystal Specification

Pericom recommends:

a) FL2650003, SMD 3.2x2.5(4P), 26.5625MHz, CL=18pF, +/-25ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

b) FY2650002, SMD 5x3.2(4P), 26.5625MHz, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

Maximum Ratings (Over operating free-air temperature range)

Storage Temperature..... -65°C to+155°C
Ambient Temperature with Power Applied.....-40°C to+85°C
3.3V Analog Supply Voltage.....-0.5 to +3.6V
ESD Protection (HBM) 2000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Specifications

Power Supply DC Characterisitcs, (T_A = -40 to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{GND}	Power Supply Current				130	mA
I_{DDA}	Analog Supply Current	Included in I_{GND}			30	mA

Power Supply DC Characterisitcs, (T_A = -40 to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{GND}	Power Supply Current				125	mA
I_{DDA}	Analog Supply Current	Included in I_{GND}			30	mA

LVCMOS/LVTTL DC Characterisitcs, (T_A = -40 to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage	V_{DD} = 3.3V ± 5%	2		V_{DD} + 0.3	V
		V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	V_{DD} = 3.3V ± 5%	-0.3		0.8	V
		V_{DD} = 2.5V ± 5%	-0.3		0.7	V
I_{IH}	Input High Current	Ref_IN, M_reset, N_SEL[0:1], PLL_Bypass, IN_SEL, V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	Ref_IN, M_reset, N_SEL[0:1], PLL_Bypass, IN_SEL, V_{DD} = V_{IN} = 0V	-5			µA
C_{IN}	Input Capacitance			4		pF
$R_{PULL-DOWN}$	Input Pulldown Resistor			51		kΩ

LVPECL DC Characterisitcs, ($V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40 to 85°C)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output High Voltage(1)	V_{DD} = 3.3V	1.9		2.4	V
		V_{DD} = 2.5V	1.1		1.6	
V_{OL}	Output Low Voltage(1)	V_{DD} = 3.3V	1.2		1.6	V
		V_{DD} = 2.5V	0.4		0.8	

Note: 1. LVPECL Termination: Source 150ohm to GND and 100ohm across CLK and CLK#.

AC Electrical Characteristics

LVPECL Termination: Source 150ohm to GND and using 0.01uF ac-coupled to 50ohm to GND

AC Characterisitcs, ($V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40 to 85°C)

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
f_{OUT}	Output Frequency Range	N_SEL[1:0] = 00	186		226	MHz
		N_SEL[1:0] = 01	140		170	MHz
		N_SEL[1:0] = 10	93		113	MHz
		N_SEL[1:0] = 11	46		57	MHz
$t_{sk(o)}$	Output Skew(1, 2)				70	ps
$t_{jit(Ø)}$	RMS Phase Jitter, (Random)(3)	212.5MHz, (12kHz - 20MHz)		0.3		ps
		159.375MHz, (12kHz - 20MHz)		0.3		ps
		156.25MHz, (12kMHz - 20MHz)		0.3		ps
		106.25MHz, (12kHz - 20MHz)		0.33		ps
		106.25MHz, (637kHz - 50MHz)		0.3		ps
		53.125MHz, (12kHz - 20MHz)		0.4		ps
		53.125MHz, (637kHz - 50MHz)		0.5		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%			400	ps
odc	Output Duty Cycle		48		52	%

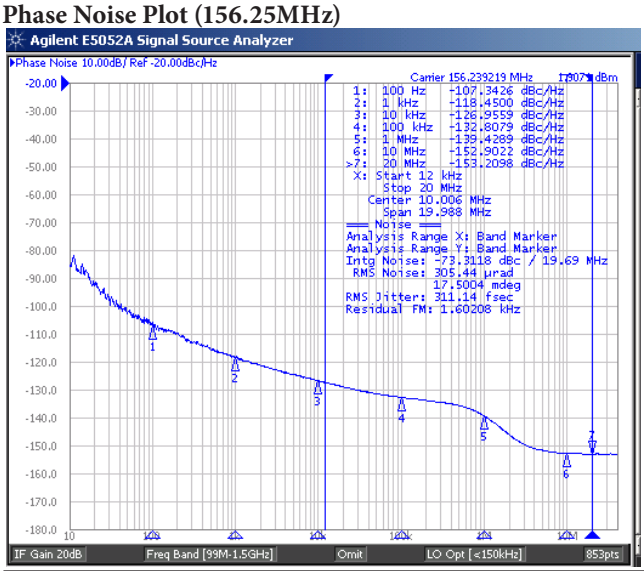
Note: Electrical parameters are quaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
Note1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
Note2: This parameter is defined in accordance with JEDEC Standard 65.
Note3: Please refer to the Phase Noise Plots.

AC Characterisitcs, ($V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40 to 85°C)

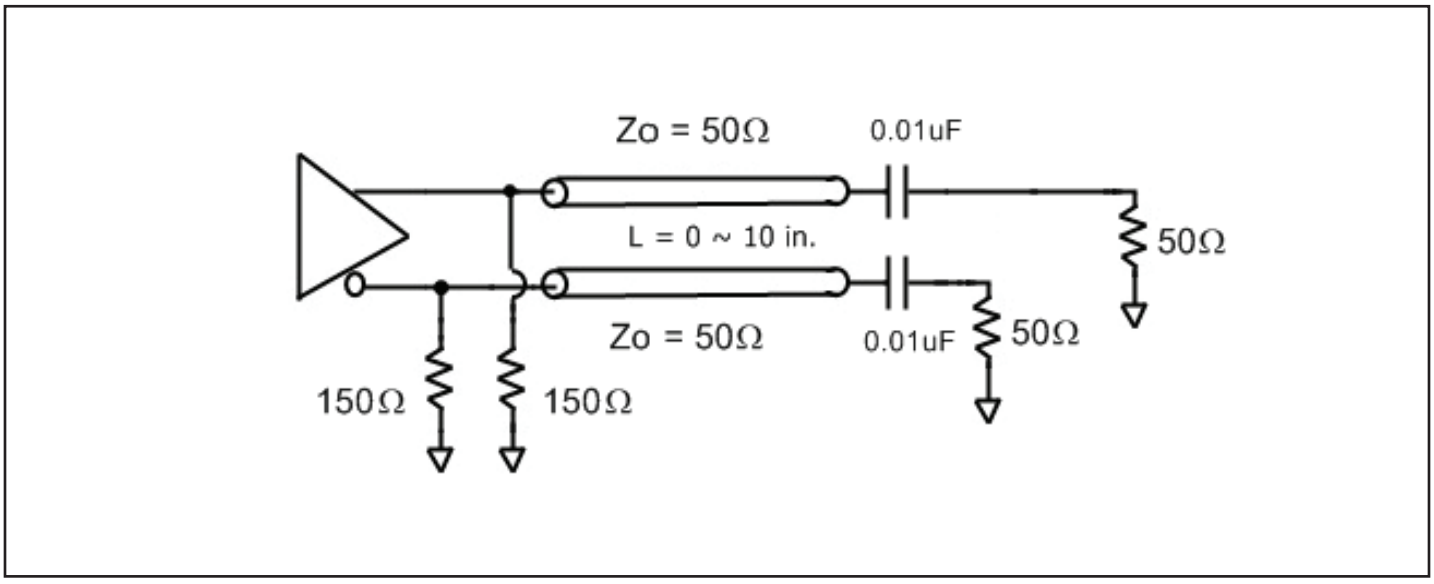
Symbol	Parameter	Condition	Min.	Typ.	Max	Units
f_{OUT}	Output Frequency Range	N_SEL[1:0] = 00	186		226	MHz
		N_SEL[1:0] = 01	140		170	MHz
		N_SEL[1:0] = 10	93		113	MHz
		N_SEL[1:0] = 11	46		57	MHz
$t_{sk(o)}$	Output Skew(1, 2)				70	ps
$t_{jit(Ø)}$	RMS Phase Jitter, (Random)(3)	212.5MHz, (12kHz - 20MHz)		0.3		ps
		159.375MHz, (12kHz - 20MHz)		0.3		ps
		156.25MHz, (12kMHz - 20MHz)		0.3		ps
		106.25MHz, (12kHz - 20MHz)		0.3		ps
		106.25MHz, (637kHz - 50MHz)		0.3		ps
		53.125MHz, (12kHz - 20MHz)		0.4		ps
		53.125MHz, (637kHz - 50MHz)		0.5		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%			400	ps
odc	Output Duty Cycle		48		52	%

Note: Electrical parameters are quaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
Note1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
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Note3: Please refer to the Phase Noise Plots.

Phase Noise Plot (156.25MHz)

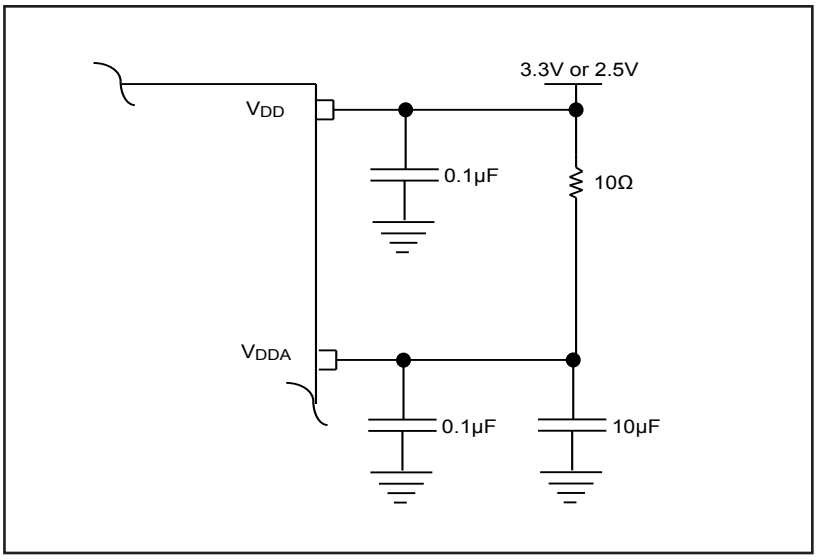


LVPECL Test Circuit



Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The PI6LC48P04 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.1µF bypass capacitors should be used for each pin. Figure below illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.



Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. A 1kΩ resistor can be tied from XTAL_IN to ground for additional protection.

Ref_IN Input:

For applications not requiring the use of the clock, it can be left floating. A 1kΩ resistor tied from the Ref_IN to ground can provide additional protection.

LVCMOS Control Pins:

All control pins have internal pulldowns; A 1kΩ resistor tied from each control pin to ground can provide additional protection.

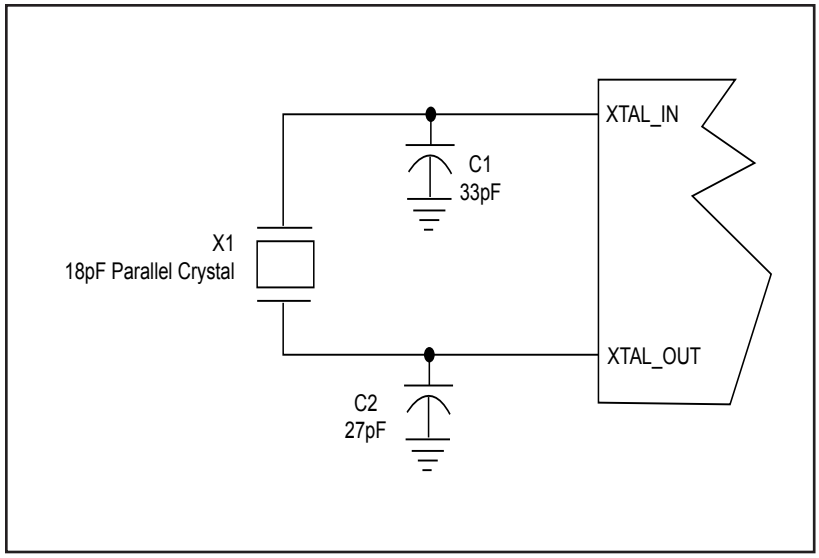
Outputs:

LVPECL Outputs:

All unused LVPECL outputs can be left floating.

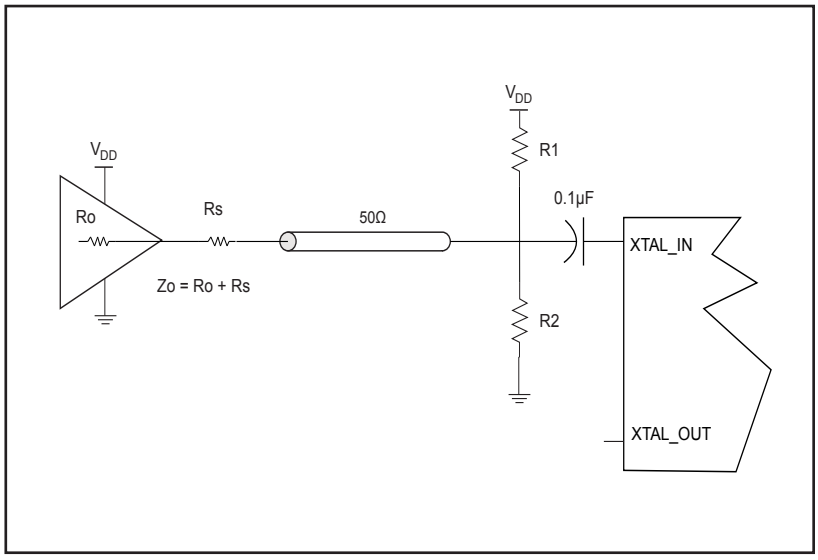
Crystal Input Interface

The clock generator has been characterized with 18pF parallel resonant crystals. The capacitor values shown in the figure below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

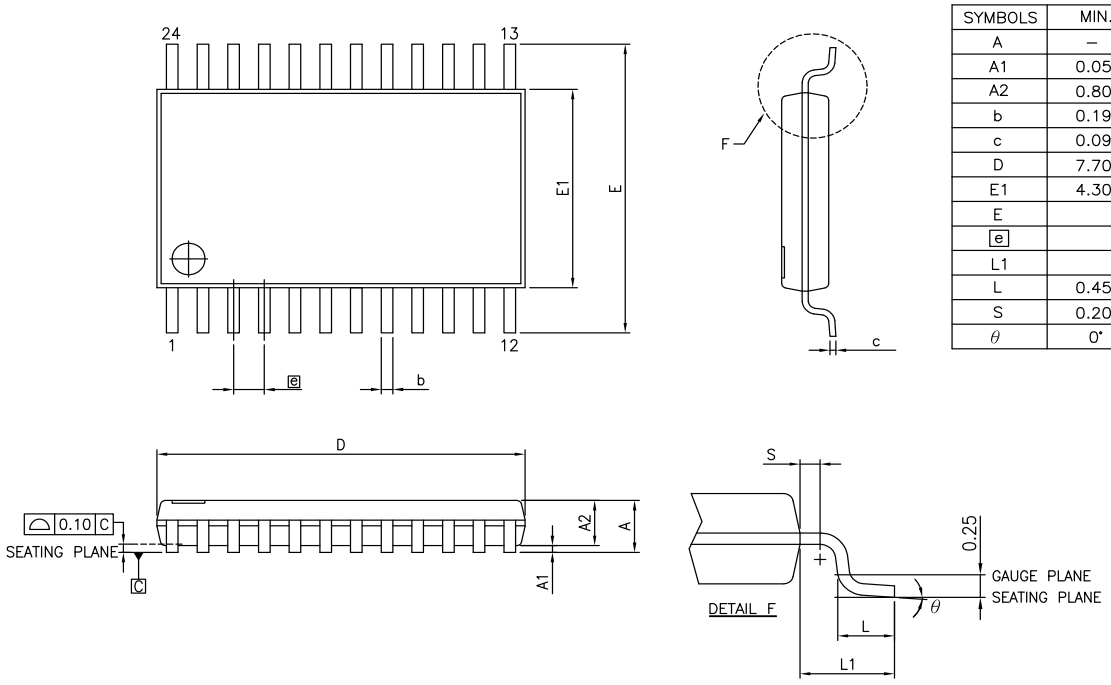


LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in the figure below. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of the two ways. First, R1 and R2 in parallel should equal the transmission line empedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is quaranteed by using a quartz crystal.



Packaging Mechanical: 24-Contact TSSOP (L)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Notes:
1. Refer JEDEC: MO-153F/AD
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

PERICOM Enabling Serial Connectivity

DATE: 05/03/12

DESCRIPTION: 24-pin, 173mil Wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1312 **REVISION: F**

12-0374

Ordering Information

Ordering Code	Packaging Type	Package Description	Operating Temperature
PI6LC48P04LIE	L	Pb-free & Green, 24-pin TSSOP	Industrial
PI6LC48P04LIEX	L	Pb-free & Green, 24-pin TSSOP, Tape & Reel	Industrial

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging