(MARCOM) DC2570 DOCUMENT CONTROL MASTER

ZILOG

PRELIMINARY PRODUCT SPECIFICATION

Z86128

L21C™ LINE 21 CLOSED-CAPTION CONTROLLER

Q4/92

Z86128

L21C™ LINE 21 CLOSED-CAPTION CONTROLLER

FEATURES

- Complete stand-alone Line 21 Closed-Caption Controller which conforms to FCC Line 21 Closed-Caption Specifications of April 12, 1991
- Simple system interface
- Optional serial interface for mode
- Requires only two inputs to operate
  - Composite video
  - Any horizontal timing pulse
- On-board Analog Sync and Data Slicer
  - No external analog required
- CMOS VLSI design for low power and low cost
- On-board Display RAM
- Odd or even Field Selectable in serial control mode
- On-board character font ROM - 12x18 character in 16x26 cell
- Visual Attributes
  - Color
  - Underline
  - Italic
  - Blink
- Smooth scrolling
- Valid Line 21 input detection
- Automatic screen blanking after 1.5 seconds with no valid input (auto blanking)
- Automatic caption display RAM erase after 16 seconds with no valid input
- 18-pin DIP package
- Automatic erase on channel change

GENERAL DESCRIPTION

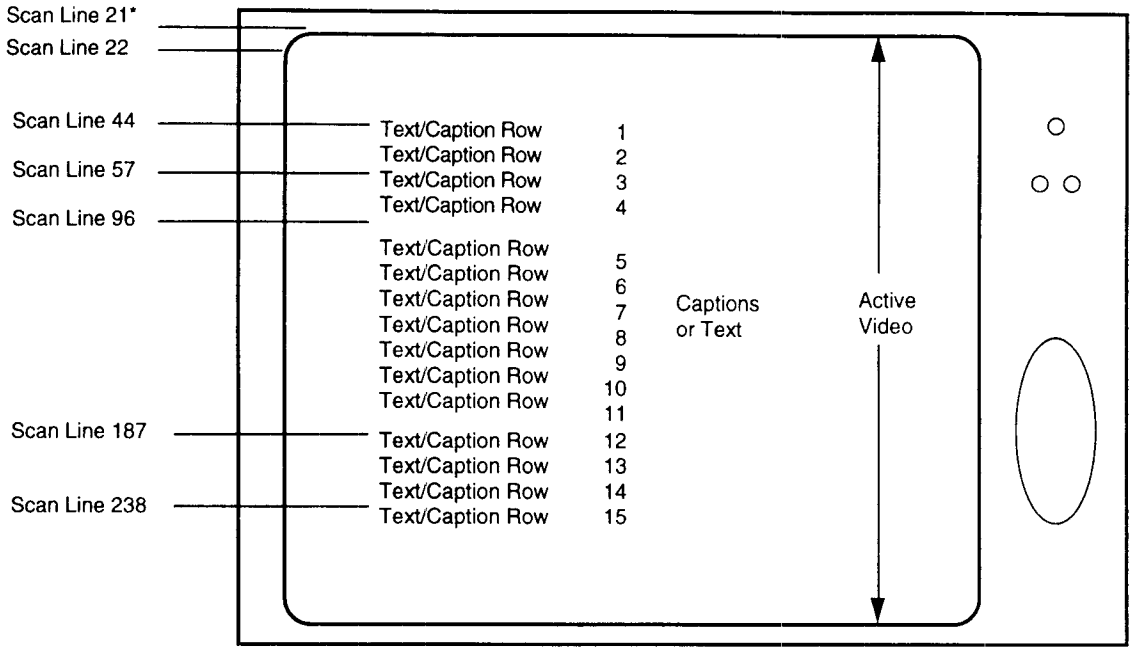
The Z86128 (Line 21 Closed-Caption Controller) is a single I.C. designed to provide the functional performance of a L21C Decoder module (Figure 1). This Superintegration™ VLSI device is completely self contained and only requires composite video signal, a horizontal SYNC signal as input and an "external keyer", i.e., video signal switch between TV video and Closed-Caption video (Figure 5) to produce captioned video. The Z86128 uses a wired logic approach to perform the functions selected through its input control signals. It is fabricated using standard CMOS technology and designed to achieve the lowest possible cost.

The Z86128 is intended for use in a set-top decoder or in any television receiver conforming to the NTSC standard. It is capable of processing and displaying all standard L21C format transmissions including the codes specified by the FCC "Report and Order" on GEN Docket No. 91-1, dated April 12, 1991. If and when PAL and SECAM TV standards define a protocol using the Line 21 format, this design will be readily convertible to that standard.

The Line 21 Closed Captioning System

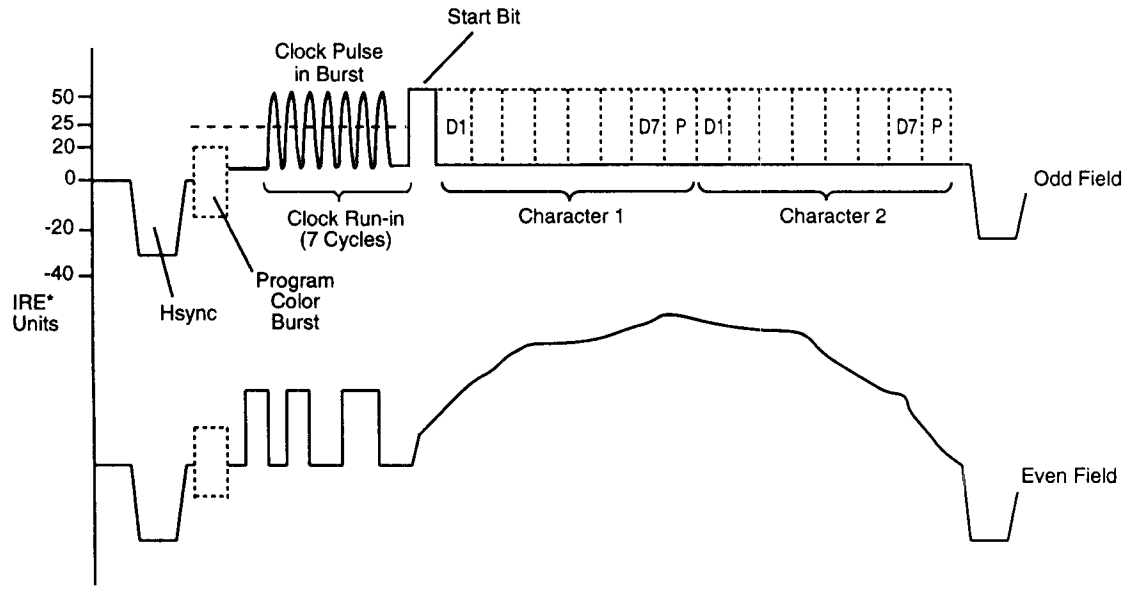
The L21C system provides for the transmission of CAPTION information and other TEXT material as an encoded composite data signal. This is during the unblanked portion of Line 21, field 1, of the standard NTSC video signal. In addition, a framing code is transmitted during the first half of Line 21, field 2. The encoded composite video signal for Line 21, field 1 and 2, is shown in Figure 2. The video signal conforms to the Standard Synchronizing Waveform for Color Transmission given in Sub-part E, Part 73 of the FCC Rules and Regulations.

GENERAL DESCRIPTION (Continued)



*Scan Line 21 is the last scan line of the vertical retrace blank interval

Figure 1. Closed-Caption TV Display Format



Notes:
*Iv PP = 140 IRE
1. Line 21 must be in its proper relative position to the leading edge of the Vsync pulse.
2. Measured from the mid-point of the leading edge of Hsync to the midpoint on the rising edge of the first "clock run-in cycle."

Figure 2. Encoded Composite Video Signal

PIN DESCRIPTION

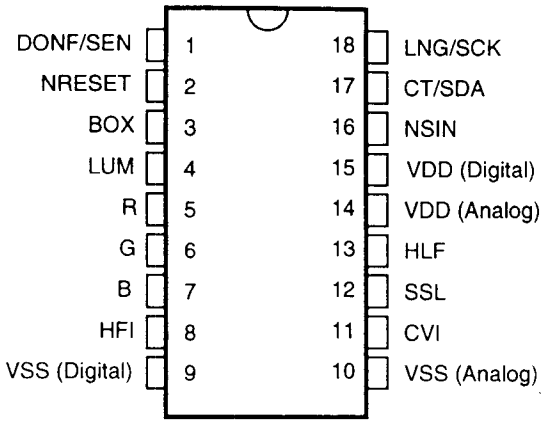


Figure 3. 18-Pin DIP Pin Assignments

Pin No.	Signal Description
11	Composite Video Input (CVI) Composite NTSC video, nominally 1.0V p-p,. band limited to 600 kHz. Circuit operates with signal variations between 0.7-1.4V p-p. It is recommended that this signal pin be driven by an emitter follower through a 0.1 µF capacitor.
12	Sync Slice Level (SSL) Capacitor (0.1 µF) to store sync slice level voltage.
8	H Flyback Input (HFI) Horizontal sync input at CMOS levels, polarity independent. Typically derived from the H Flyback pulse or any other horizontal timing signal.
13	H Loop Filter (HLF) Value to be specified
9	V_{SS} Digital. Digital Ground Connect to system ground
1	DONF/SEN Input (control)
	In Parallel Mode this input controls the Decoder On/Off function CMOS input with High = On, Low = Off. In Serial Mode this input is the Enable for serial data input.

Pin No.	Signal Description
17	CT/SDA I/O (control) In Parallel Mode this input, along with the LAG/SCK input, selects the Data Channel to be processed. CMOS input with High=CAPTIONS, Low =TEXT. In Serial mode this pin first outputs the status bit, then becomes the input for serial control data and is in high impedance state when the L21C is in a power-down state.
2	NRESET Master reset for the I.C. and must be used in the Parallel Control Mode. It may be tied High in the Serial Mode if reset is to be performed through the serial data stream.
18	LAG/SCK Input (control) In Parallel Mode this input selects the Data Channel to be processed (along with CT/SDA). CMOS input High = LANGUAGE I, Low= LANGUAGE II. In Serial Mode this input is Serial Clock In and will be in the high impedance state when the L21C is in a power-down state.
3	Box Output (Box) Active High, CMOS level "black box" keying signal for Caption/Text display area.
4	Luminance Output (LUM) Active High, CMOS level signal. Character video luminance signal.
5, 6, 7	Color signals, RGB Outputs Active High, CMOS level color character video for color receiver use.
15	V_{DD} Digital Power pin. Connect to +5V source. Decouple to Gnd with a .1 µF capacitor.
14	V_{DD} Analog Decouple to Gnd with a .1 µF capacitor.
10	V_{SS} Analog. Analog Ground Connect to system ground.
16	(NSIN) Input (Control) Selects the mode to be used in interpreting the signals on the three Control pins: High = Parallel Mode, Low = Serial Mode.

FUNCTIONAL DESCRIPTION

Data Transmission Format

The composite data signal contained within the active portion of Line 21 consists of a seven cycle sine-wave clock run-in burst, a start bit and 16 bits of data. These 16 bits consist of two 8-bit alphanumeric characters formulated according to the USA Standard Code for Information Interchange (USASCII; x 3.4-1967) with odd parity. The clock rate is 0.5035 MHz which is 32 fH. The clock burst and data packet are 50 IRE units peak-to-peak and are filtered to a "2T" response. Data is sent with the least significant bit (bit D1) being sent first and the most significant bit (bit D8, the parity bit) sent last.

Multiplexed Data Channels

The Line 21 closed-captioned system defines four different data channels which can be time multiplexed within the Line 21 data stream. They are Captions - LANGUAGE I (C1), Captions - LANGUAGE II (C2), Text - LANGUAGE I (T1) and Text - LANGUAGE II (T2). Both languages can be English in either case.

TEXT (optional) is defined as non-video related information therefore its display can fill the screen. In a full screen, TEXT mode displays a black box 15 rows high by 34 columns wide which covers the screen. Text appears starting at the top with a maximum of 32 characters per row. When all 15 rows have been used, the display scrolls up as additional information is received.

Captions are video related information so they are not permitted to overwrite the screen. Captions may be displayed in any four rows in any combination. Four rows may be displayed at one time. All the rows in each caption appear at once in Pop-on Captions mode.

A secondary Caption display mode, called Rollup Captions, is also provided. In this mode, caption information is displayed in any consecutive combination; two, three or four rows. Data appears in the base row and scrolls up as new information is received. The data scrolls off the top row selected as in the TEXT mode. This mode is usually used for captioning unscripted and fast turnaround programming such as talk shows and news.

Data Format

The four data channels are transmitted in Line 21 as a time multiplexed data stream. The start of a particular channel's data stream is identified by the occurrence of one of its unique command codes. Once a unique command code is received, all subsequent data is considered to belong to that data channel until a unique command code is received for another data channel. The Alarm On and Alarm Off codes are an exception to this rule. Alarm codes are ignored by everything except the Alarm output control circuits.

The 7-bit ASCII table defines two types of information, printing and non-printing. Printable data are data bytes having values between x0100000 (20H) and x1111111 (7FH), where x represents the parity bit. Data bytes having values between x0000000 (00H) and x0011111 (1FH) are called non-printing characters since they have no displayable font character in the standard ASCII table.

Displayable Character Set

The specifications* define a modified ASCII table character set where eight of the alphanumeric characters have been changed to provide some foreign characters. In addition, 15 additional characters are defined by special character commands. The changes from the standard ASCII table characters are shown in Table 1.

* The information presented here essentially conforms to the 1985 NCI specifications with the exception of the changes made in the FCC document.

Table 1. Different ASCII Characters

Hex Code	ASCII Value	Line 21 Value
2A	*	á
5C	\	é
5E	^	í
5F	-	ó
60	'	ú
7B	{	ç
7D	}	Ñ
7E	~	ñ

Fifteen additional displayable characters are sent by transmitting a two-byte code. The sixteenth code provides a transparent space. The byte pair has a non-printing character followed by a printing character, where the non-printing character is 11H for LANGUAGE I and 19H for LANGUAGE II. The printing character determines the special font character that will be displayed according to Table 2.

Table 2. Print Character Font Determination

Print	Character
30	®
31	°
32	1/2
33	¿
34	™
35	¢
36	£
37	♪
38	à
39	(transparent mark)
3A	è
3B	â
3C	ê
3D	î
3E	ô
3F	û

Commands and Special Information

Data channel commands and special information are transmitted as ***two byte pairs*** consisting of a non-printing character followed by a printing character. The two bytes of the pair must be transmitted in the same field and the pair is transmitted twice in successive frames. This redundancy provides some immunity for errors due to noise for control information.

Throughout the Line 21 system, bit 4 of the non-printing character identifies the Language. Bit D4=0 signifies LANGUAGE I commands and D4 = 1 signifies LANGUAGE II. The non-printing characters used in the Line 21 system are 10H-17H for LANGUAGE I and 18H-1FH for LANGUAGE II.

Data Channel Commands. All the data channel command codes use the non-printing character 14H for LANGUAGE I and 1CH for LANGUAGE II. The printing character determines the particular command function. The commands are shown in Table 3. The printing character's value is given in Hex.

Table 3. Data Channel Commands

Data Channel = Captions (C1 or C2) Hex

Print	Function
20	Resume Caption Loading (off screen)
25	Resume 2 Line Roll-up
26	Resume 3 Line Roll-up
27	Resume 4 Line Roll-up
29	Resume Direct Loading (on screen)
2C	Erase Displayed Memory
2E	Erase Non-displayed Memory
2F	Show Caption (flip memories)

Data Channel = Text (T1 or T2)

Print	Function
2A	Start Text
2B	Resume Text

The following commands are shared by all of the data channels:

Print	Function
21	Backspace
28	Flash On/Off
2D	New Line (carriage return)

The Alarm circuit command codes are:

Print	Function
22	Alarm Off
23	Alarm On

The commands specified in the April 12, 1991 FCC document are:

Print	Function
14+24	Delete to end of row
17+21	Tab Offset 1 column
17+22	Tab Offset 2 column
17+23	Tab Offset 3 column

The "delete to end of row" command will erase the memory contents from the current column position to the end of the current line. The Tab offset column commands will move the current column position plus 1, 2, or 3 character positions from the current column position.

Data Location and Attribute Codes. Additional codes are used for positioning the data on the screen and for controlling the character attributes. There are two location attributes, row and column (tab or indent) position and three character attributes, color, italics and underline. All attribute information is contained in the Preamble Codes (Precodes) and Mid-row Codes (Midcodes).

The Precodes identify the display row and character attributes for the caption data that follows it. These attributes hold for the entire line unless changed by a Midcode or Indent code. All the non-printing characters, 10H-17H for LANGUAGE I and 18H-1FH for LANGUAGE II are used. The code pair assignments for the location and character attributes are given in Table 4.

Table 4. Two Byte Pairs for Location and Character Attributes

Non-print Caption Row	11 1	11 2	12 3	12 4	15 5	15 6	16 7	16 8	17 9	17 10	10 11	13 12	13 13	14 14	14 15
ATTRIBUTE															
Monochrome	40	60	40	60	40	60	40	60	40	60	40	40	60	40	60
Mono Underline	41	61	41	61	41	61	41	61	41	61	41	41	61	41	61
Green	42	62	42	62	42	62	42	62	42	62	42	42	62	42	62
Green Underline	43	63	43	63	43	63	43	63	43	63	43	43	63	43	63
Blue	44	64	44	64	44	64	44	64	44	64	44	44	64	44	64
Blue Underline	45	65	45	65	45	65	45	65	45	65	45	45	65	45	65
Cyan	46	66	46	66	46	66	46	66	46	66	46	46	66	46	66
Cyan Underline	47	67	47	67	47	67	47	67	47	67	47	47	67	47	67
Red	48	68	48	68	48	68	48	68	48	68	48	48	68	48	68
Red Underline	49	69	49	69	49	69	49	69	49	69	49	49	69	49	69
Yellow	4A	6A	4A	6A	4A	6A	4A	6A	4A	6A	4A	4A	6A	4A	6A
Yellow Underline	4B	6B	4B	6B	4B	6B	4B	6B	4B	6B	4B	4B	6B	6B	6B
Magenta	4C	6C	4C	6C	4C	6C	4C	6C	4C	6C	4C	4C	6C	6C	6C
Magenta Underline	4D	6D	4D	6D	4D	6D	4D	6D	4D	6D	4D	4D	6D	6D	6D
Italics (mono)	4E	6E	4E	6E	4E	6E	4E	6E	4E	6E	4E	4E	6E	6E	6E
Italics Underline	4F	6F	4F	6F	4F	6F	4F	6F	4F	6F	4F	4F	6F	6F	6F
Indent 0 (mono)	50	70	50	70	50	70	50	70	50	70	50	50	70	50	70
Indent 0 Underline	51	71	51	71	51	71	51	71	51	71	51	51	71	51	71
Indent 4	52	72	52	72	52	72	52	72	52	72	52	52	72	52	72
Indent 4 Underline	53	73	53	73	53	73	53	73	53	73	53	53	73	53	73
Indent 8	54	74	54	74	54	74	54	74	54	74	54	54	74	54	74
Indent 8 Underline	55	75	55	75	55	75	55	75	55	75	55	55	75	55	75
Indent 12	56	76	56	76	56	76	56	76	56	76	56	56	76	56	76
Indent 12 Underline	57	77	57	77	57	77	57	77	57	77	57	57	77	57	77
Indent 16	58	78	58	78	58	78	58	78	58	78	58	58	78	58	78
Indent 16 Underline	59	79	59	79	59	79	59	79	59	79	59	59	79	59	79
Indent 20	5A	7A	5A	7A	5A	7A	5A	7A	5A	7A	5A	5A	7A	5A	7A
Indent 20 Underline	5B	7B	5B	7B	5B	7B	5B	7B	5B	7B	5B	5B	7B	5B	7B
Indent 24	5C	7C	5C	7C	5C	7C	5C	7C	5C	7C	5C	5C	7C	5C	7C
Indent 24 Underline	5D	7D	5D	7D	5D	7D	5D	7D	5D	7D	5D	5D	7D	5D	7D
Indent 28	5E	7E	5E	7E	5E	7E	5E	7E	5E	7E	5E	5E	7E	5E	7E
Indent 28 Underline	5F	7F	5F	7F	5F	7F	5F	7F	5F	7F	5F	5F	7F	5F	7F

The Midcodes are used to change the character attributes in the middle of a caption row. The Midcodes occupy a space on the display screen. The characters following the Midcode are displayed with the attributes assigned by the Midcode. These hold until the end of the row unless changed by another Midcode. The Indent codes listed in Table 4 actually perform in the same manner as a Midcode.

The Midcodes use the non-printing characters 11H and 19H, respectively, for the two languages. The printing character of the two byte pair contains the character attributes as shown in Table 5.

Table 5. Print Character Attributes

Print	Character Attribute	Print	Character Attribute
20	Monochrome	28	Red
21	Monochrome Underline	29	Red Underlined
22	Green	2A	Yellow
23	Green Underlined	2B	Yellow Underlined
24	Blue	2C	Magenta
25	Blue Underlined	2D	Magenta Underlined
26	Cyan	2E	Italics
27	Cyan Underlined	2F	Italics Underlined

DECODER OPERATION

The Z86128 provides full function Line 21 performance. Control inputs are included to enable the decoder to process and display any of the four data channels (C1, C2, T1 or T2) transmitted in Line 21 of the incoming video. The Decoder On/Off input (DONF/SEN), controls the display. When switched to the Decoder Off (TV) state, incoming data in the selected channel is still processed but not displayed. Provisions have been made to select Field 1 or Field 2 operation.

Display Format

Characters are displayed as white or colored, dot matrix character on a black background. The characters are described by a 6x9 dot pattern within a character cell which is 8 dots wide by 13 dots high. This leaves a one dot border of black around each character and provision for one scanline for underline, offset by one scanline of black, between the character and the bottom edge of the cell. Character luminance is 90 IRE units and the black box surround, 10 IRE units.

The character ROM consists of a 12x18 dot matrix pattern per character. Alternate rows and columns are read out of each field to produce an interleaved and rounded character.

A display row contains a maximum of 32 characters plus a leading and trailing blank box, each a character cell in width, making the overall width of a display row 34 x 8 = 272 dots. Successive display rows are joined together so that the total display occupies 195 dots high. The black box is 34 character cells wide by 195 dots high resulting in a box size of 45.018 µsec in width by 195 TV scan lines in height. When centered in the video display, this box will start 13.2 µsec after the leading edge of H in-scan line 43 and extend-to-scan line 237. This places the display within the safe title area for NTSC receivers. Character width is 42.37 µsec, also centered on the screen, resulting in a leading and trailing 1.32 µsec black border (See Figure 6).

Text Mode Display
When TEXT mode, in either language, has been selected (and valid Line 21 code has been detected in the incoming video) the 15-row by 34-character black box appears. Received TEXT characters are displayed as they are received starting in row 5. Successive carriage returns (new line command) moves the display down successive rows until 7 or 8 display rows have been used. Thereafter, the text scrolls up as new characters are added to the bottom row.

If the data for the selected channel is interrupted by a command for another channel, data processing stops but the display remains. When a Resume Text command is received, data processing will resume and the new characters are added starting at the position that the display row/cclumn pointer was prior to the interruption of data processing. If a Start Text command is received, the display is cleared and new characters are displayed starting in row 5, column 1 (left side).

When scrolling, the display will shift one scan line per frame until a complete row has been scrolled. If a carriage return is received before scrolling is complete, the display immediately completes the "scroll" by jumping up the remaining scan lines and starts displaying the new text.

There will never be any transparent boxes in the TEXT display.

Caption Mode Display
When Caption mode, in either language, has been selected, the screen is transparent (display box disappears). Caption data can appear in any of the 15 display rows but a single caption may consist of no more than 4 rows. The form of the caption display depends on the caption mode indicated by the transmitted caption command, *Pop-on*, *Paint-on* or *Roll-up*.

Pop-on captions work with two caption memories. One of them is always being displayed while the other is being used to accumulate new caption data. A new caption is popped-on by swapping the two memories (the show caption command). When the on-screen memory is erased, the screen is blank (transparent) and the memory defaults to the row/column pointer at row 1, column 1 and monochrome non-underlined.

When caption mode is selected, the decoder processes any data following the Resume Caption Loading (RCL) command (or the Show Caption command). Normally, this command is followed by a Precode to indicate the row, column and character attributes to be used with the following data. If no Precode is received the data is added to the location last indicated by the row/column pointer prior to the receipt of the RCL command and with the character attributes previously assigned.

Paint-on caption mode is essentially equivalent to the Pop-on mode except that the data received after the Resume Direct Loading (RDL) command is written to the on-screen memory rather than the off-screen memory. All the rules for Precodes, Midcodes, etc., are otherwise the same.

Roll-up caption mode presents a "text" like display that is limited to 2, 3 or 4 rows depending on the Resume Roll-up (RRn) command used. The precode following the RRn command will be used to indicate the base row for the roll-up display. The base row will be the "bottom row" for the roll-up display. In this case, a black box does not appear until characters are being displayed and the box is only wide enough to provide a leading and trailing box in each line. The new data appears in the "bottom row" and as each carriage return is received, the row scrolls up and the new data added to the bottom. When the number of rows indicated by the Resume command has been reached, the data in the top row scrolls off as new data is added to the bottom.

The TAB (indent) precode permits placing captions starting at four character boundaries. The TAB offset command provides the means for adjusting the starting position for a caption at any column position. The TAB offset command must immediately follow the TAB command or it will be ignored.

Display Erase and Autoblanking

The display is erased in the TEXT mode by the Start Text command (but box is maintained) and in the Caption mode by the Erase Displayed Memory command. The non-displayed memory can be erased by the Erase Non-displayed Memory command.

Three other events can also cause the display to be erased. First, changing the data channel for processing by switching between CAPTIONs and TEXT, or between LANGUAGEs I and II, clears the memory and hence the display. Second, if the autoblanking circuit is activated by the loss of valid code, then the display is turned off and the memory cleared. Last, in the Caption mode, if no valid caption command in the selected language is received for a 16 second period, the on-screen memory is erased.

The autoblanking circuit maintains the status of the presence of valid data. The decoder is held in the Decoder off (TV) state until data is continuously detected for a period of 0.5 seconds. Once the valid data decision has been made, and assuming that the user has selected the Decoder on state, the normal display for the data channel selected is presented.

The autoblanking circuit will not be activated again until valid data has been lost for 1.5 seconds. Any valid data received during the 1.5 second period resets the counter so that the autoblanking will only be activated on continuous loss of data for 1.5 seconds.

Decoder Control Interface

The L21C can operate in either of two control modes, Parallel Mode or Serial Mode. Parallel Control Mode permits the control of the decoder functions by means of simple switch selections on the three control inputs DONF, CT, and LNG. In the Serial Mode these three inputs are changed into Serial Enable (EN), Serial Data (SDA) and Serial Clock (SCK), respectively. The control of the decoder functions are controlled by clocking in a data word via this serial bus system.

BLOCK DIAGRAM DESCRIPTION

The Z86128 is designed to provide the functional performance of a L21C decoder with only two input signals being required, Composite Video and H Flyback or any other Horizontal timing pulse. The Decoder performs two basic functions, namely extracting the Line 21 code from the incoming video and converting the recovered code for the channel selected, into displayable information. Figure 4 shows the Z86128's block diagram.

The Z86128 generates its own H and V sync signals so that all internal processing is performed with noise immune signals. The decoder design has been formulated to achieve the best performance at the lowest possible cost.

Input Signals

The Composite Video input should be a signal which is nominally 1 V p-p with sync tips negative and band limited to 600 kHz. The Z86128 will operate with in an input level variation of ±3 dB.

H Flyback is a CMOS level input signal which provides horizontal sync information for the Phase/Frequency detector. It maintains a coarse lock of the VCO whether composite video is present or not. This signal can also be used in future applications to provide horizontal timing information in the absence of video. It can be positive or negative polarity.

Video Input Signal Processing

Comp Video input is AC coupled to the I.C. and the sync tip is internally clamped to a fixed reference voltage. Initially, the signal is clamped using a simple clamp, but improved impulse noise performance is achieved once the internal sync circuits lock to the incoming signal. Noise rejection is obtained by making the clamp operative only during the sync tip. The clamped composite video signal is fed to both the Data Slicer and Sync Slicer blocks.

The Data Slicer generates a clean CMOS level data signal by slicing the signal at its midpoint. The slice level is established on an adaptive basis during Line 21 of the odd field. The resultant value is stored until the next odd field Line 21 begins. A high level of noise immunity is achieved by using this process.

The Data Clock Recovery circuit produces a 32H clock signal (DCLK) that is locked in phase to the sliced clock run-in burst obtained from the Data Slicer. The Dot Clock is locked in phase with H sync but the DCLK phase is not determined until occurrence of Line 21 data. When Line 21 code appears, DCLK phase lock is achieved during the clock run-in burst and used to reclock the sliced data. Once phase lock is established it is maintained until a change in video signal occurs.

The Sync Slicer processes the clamped Comp Video signal to extract Comp Sync, which is then used to lock the internally generated sync to the incoming video. Sync slicing is performed in two steps. Initially, the sync is sliced at a fixed offset level from the sync tip. When the internal vertical counter locks, the slice level reference switches from a fixed to an adaptive basis. An external capacitor stores the slice level.

Timing and Synchronizing Circuits

All internal timing and synchronizing signals are derived from the on-board 12 MHz VCO. Its output is the DOT CLK signal used to drive the Horizontal and Vertical counter chains and for display timing. No external components are required to bring it within the pull-in range of the Phase/ Frequency detector.

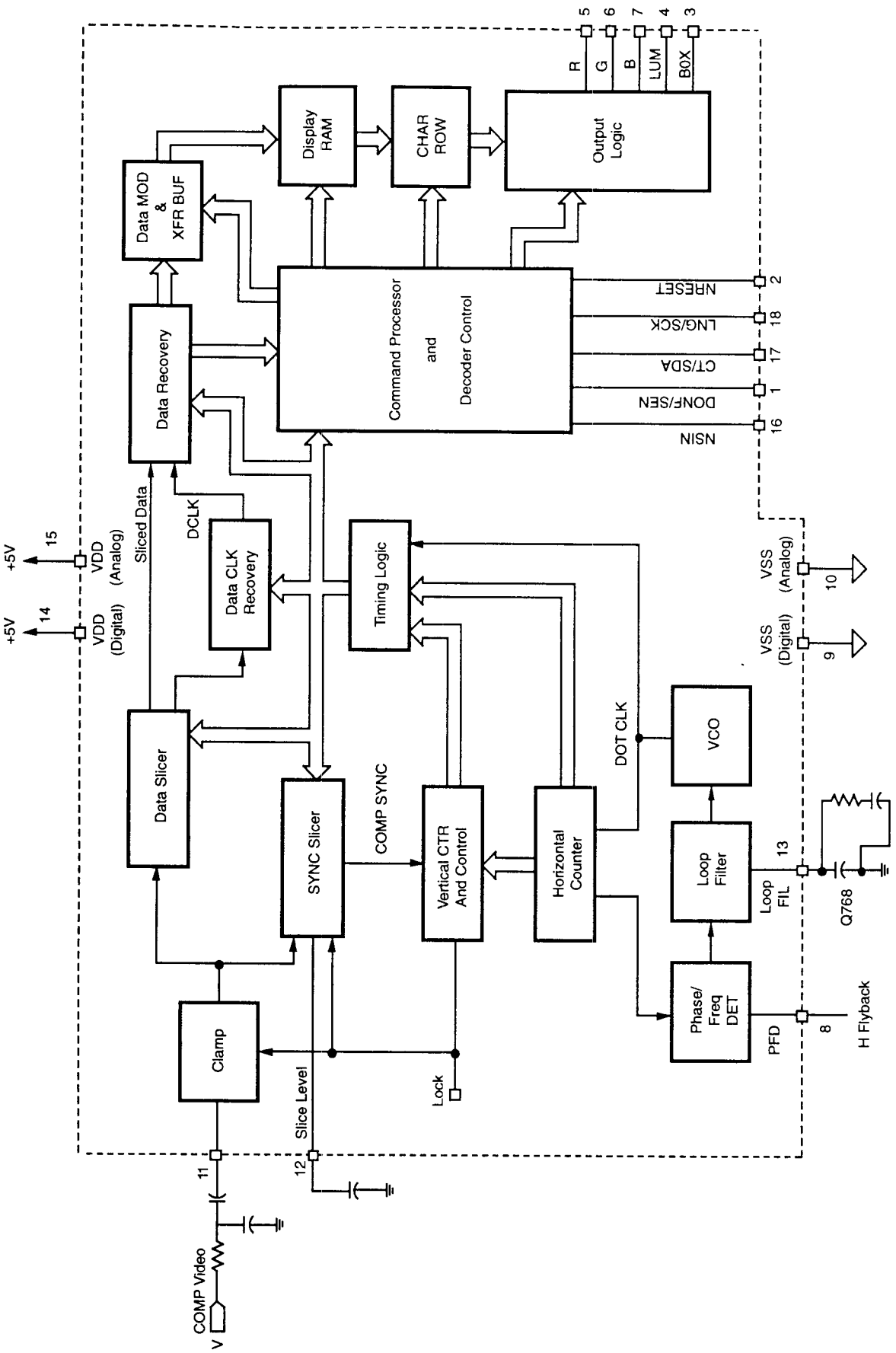


Figure 4. Z86128 Block Diagram

BLOCK DIAGRAM DESCRIPTION (Continued)

The Horizontal Counter is a divide-by-768 circuit with intermediate outputs needed to generate the timing logic signals used in data recovery and data output (display). It produces pulse signals at 1H, 2H, 32H and 48H rates as well as the horizontal square wave, Q768, that is used to phase-lock the VCO.

The Vertical Counter and Control circuits produce a noise free vertical pulse by dividing the horizontal signal in a 525 counter. The internal synchronizing signals are phased up with the incoming video by comparing the internally generated vertical pulse to an input vertical pulse derived from the Comp Sync signal provided by the Sync Slicer. When proper phasing has been established, this circuit outputs the LOCK signal which is used to provide additional noise immunity to the slicing circuits.

The locked state is established only after several successive fields have occurred in which these two vertical pulses remain in sync. Once locked, the internal timing will flywheel until such time as the two vertical pulses lose coincidence for a number of consecutive fields. Until LOCK is established, the decoder operates on a pulse for pulse basis.

Data Recovery

The Data Recovery circuits perform the initial processing of the data in Line 21. The sliced data is relocked using DCLK and the relocked data stream is checked for the presence of valid data. When data is present the two bytes are clocked into the Serial/Parallel register and output in parallel form.

This block checks the bytes for valid (odd) parity. It also determines whether the recovered byte pair is a repeat of the previously received byte pair. That information is used with the redundancy flag in the Command Processor to determine whether the command should be executed or not.

Command Processor

The Command Processor circuits control the manipulation of the data for storage and display. It decodes the control inputs (Decoder On/Off, Captions/Text, LANGUAGE I/II) to determine the display status desired and the data channel selected. This information is then used to perform its most important function, the control of the loading, addressing and clearing of the Display RAM.

During data recovery time (TV lines 21-42), the Command Processor transfers only the data received for the data channel selected, to the RAM for storage and display. In those cases such as special characters, midcodes, parity errors, etc., where the data stored or action to be taken is different than the specific bytes received, the Command Processor converts the input data to the appropriate form.

During the display time (line 43-237), the Command Processor controls the operations of the Display RAM, Character ROM and output Logic circuits.

Memory and Display Circuits

These circuits operate together to generate the output color signals R, G, B and the monochrome signals Luminance and Box. The character ROM contains the dot pattern for all the characters but not the underline characteristic. The output logic provides the hardware underline control circuits and the italics slant generator. The smooth scroll display control is also performed in the output logic block.

Decoder Control Circuit

The Decoder Control Circuit block converts the signals provided to the three controls into the internal control signals required to establish the operating mode of the decoder. The control pin NSIN switches the inputs from parallel input control to serial input control. This block performs the serial-to-parallel conversion or the parallel-to-parallel conversion as the case may be (Figure 5).

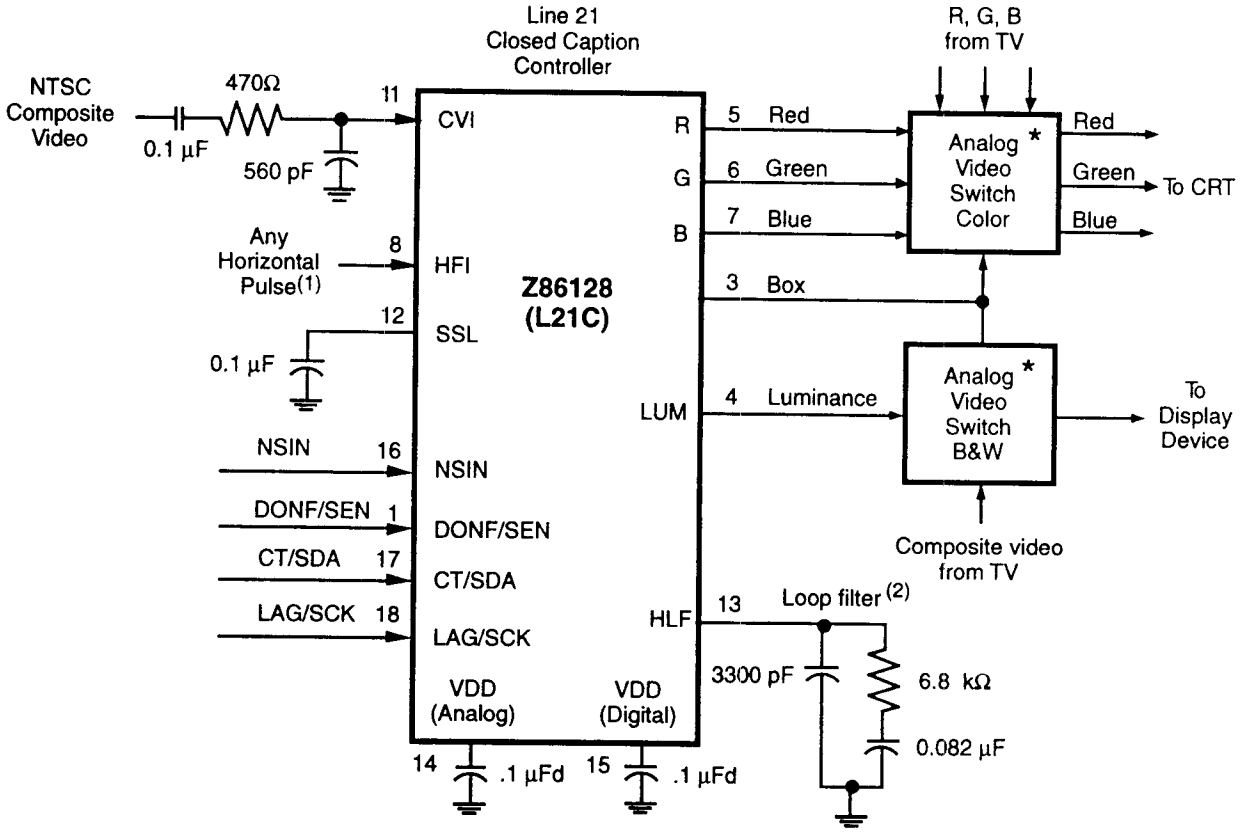


Figure 5. L21C Application Block Diagram

Notes:

* External Keyer

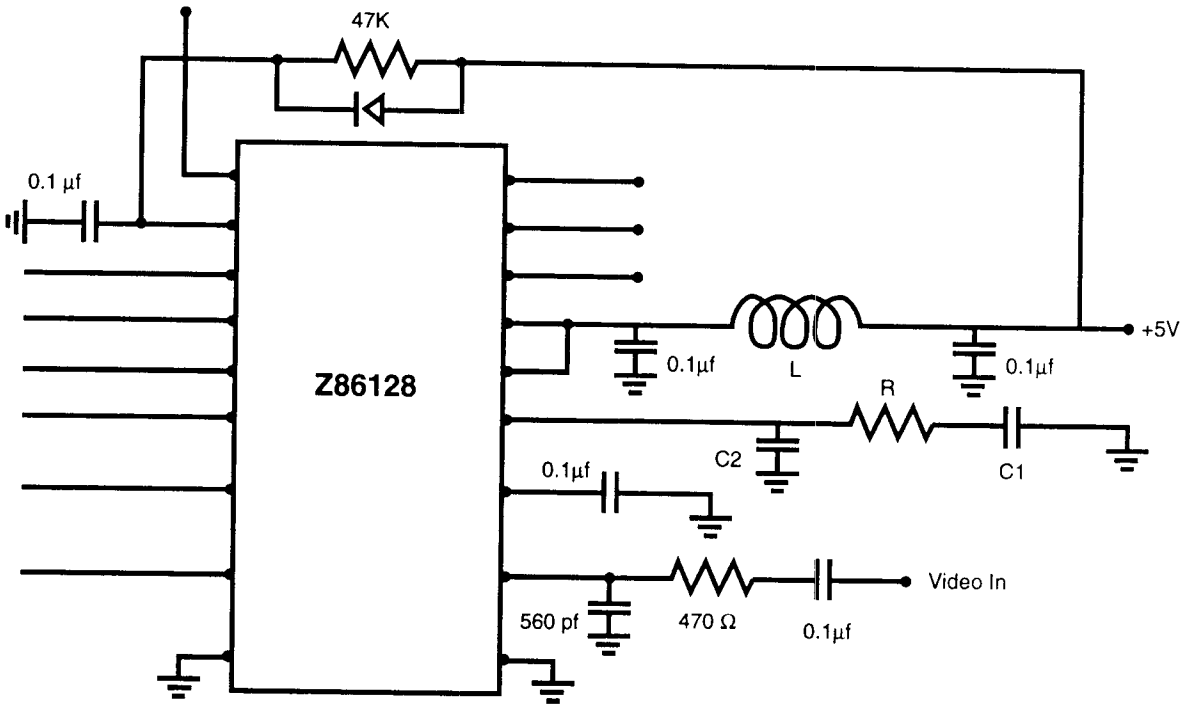
(1) For VCR or other applications where a horizontal pulse is not available, simply generate a signal which pulses at a 15.73 kHz rate. The HFI input is edge trigger, therefore any polarity and duty cycle will be adequate. A 555 timer with the proper compensation is all that is needed to maintain ±3% variability to 15.73 kHz.

(2) The Loop filter capacitors should be good quality film capacitors at 10% tolerance and the resistors at 5% tolerance.

(3) Check with local sales office for loop filter recommended values.

EMI REDUCTION

The following recommendations are made to enable the user to minimize EMI radiation from the chip which tend to ocur at 193 MHz (Channel 10). The circuit diagram, component layout, and single sided pattern needed to achieve the desired effect are shown below. There is also a ground plane shield pattern for those users who prefer to use a double sided printed circuit board. It should be noted that the pattern using line widths greater than those shown for the signal lead ***must*** be followed as shown.



C = 0.1 µf Ceramic Disk

L = Four turns of #30 wire on ferron cube bead #56 590 65/3B

C1, C2, R = Loop Filter

Figure 6. Printed Circuit Layout of Critical Parts to Reduce RF Interference

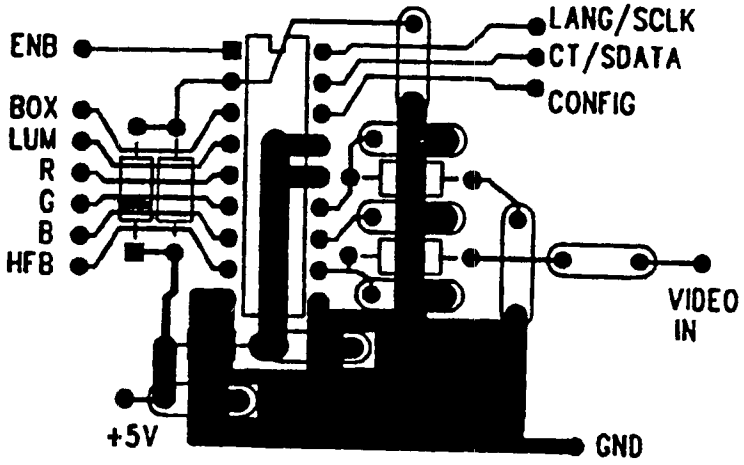


Figure 7. Circuit Layout

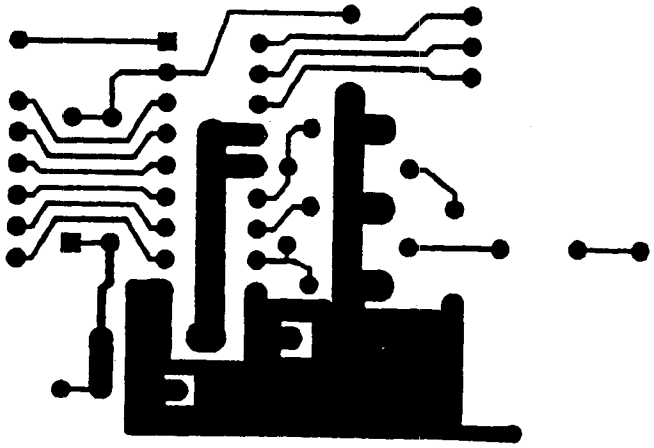


Figure 8. Layout Viewed from Component Side

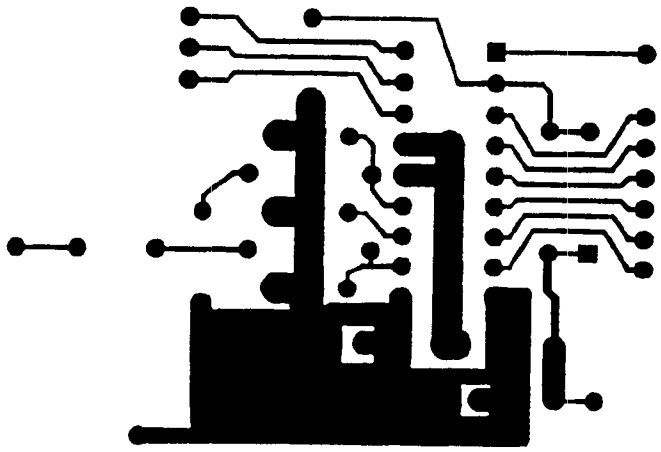


Figure 9. Layout Viewed from Circuit Side

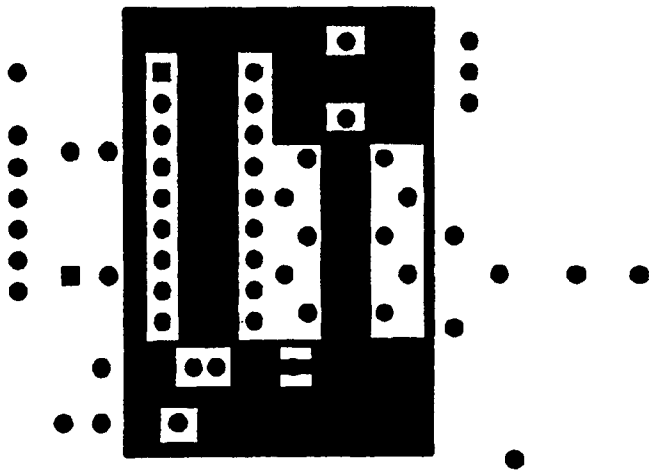


Figure 10. Layout of Ground Plan Viewed from Component Side

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{DD} = +4.75V to +5.25V

Sym	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Voltage Low	0	$0.2V_{DD}$	V	
V_{IH}	Input Voltage High	$0.7V_{DD}$	V_{DD}	V	
V_{OL}	Output Voltage Low		0.4	V	I_{OL} = 1.00 mA
V_{OH}	Output Voltage High	V_{DD}-0.4		V	I_{OH} = 0.75 mA
I_{IL}	Input Leakage	-3.0	3.0	µA	0V, V_{DD}
I_{CC}	Supply Current		20	mA	Estimated

ABSOLUTE MAXIMUM RATINGS

Sym	Description	Min	Max	Units
V_{DD}	Supply Voltage*	-0.3	+7.0	V
T_{STG}	Storage Temp	-65°	+150°	C
T_A	Oper Ambient Temp	0°	+70°	C

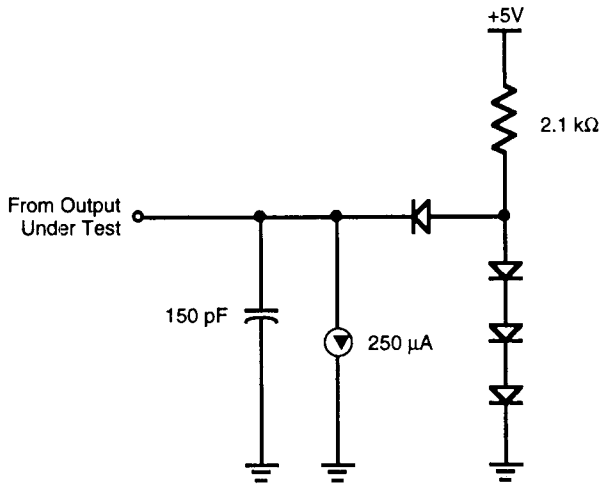
Notes:

* Voltages on all pins with respect to GND.

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Standard Test Load).



Standard Test Load

AC AND TIMING CHARACTERISTICS
(Reference Figure 11)

Composite Video Input

Amplitude: 1.0 V p-p, ±3 dB
Polarity: Sync tips negative
Bandwidth: 600 kHz

Horizontal Signal Input (preferably H Flyback)

Amplitude: CMOS level signal, Low ≤ $0.2V_{DD}$, High ≥ $0.7V_{DD}$
Polarity: Any
Frequency: 15,734.263 Hz, ±3%

Line 21[1] Input Parameters (at 1.0 V p-p) (see Figure 11)

Code Level: 50 IRE ± 10 IRE
Clock Run-in Start[2]: 10.5 µs, ±0.5 µs

Input Signal-to-Random Noise Performance

Unit will function down to a 25 dB ratio (CCIR weighted) with one error per row or better at that level.

Internal Sync Circuits

The internal sync circuits will lock to all 525 line signals having a vertical sync pulse that meets the following conditions:

- It is at least 2.5H long.
- It starts at the proper 2H boundary for its field.
- If equalizing pulse serrations are present they must be less than 0.125H in width.

Timing Signals

Dot Clock: 768 x FH = 12.0839 MHz
Dot Period: 82.75 nsec
Character Cell Width: 1.324 µsec
Width of Row (Box): 45.018 µsec
Width of Row (Char): 42.370 µsec

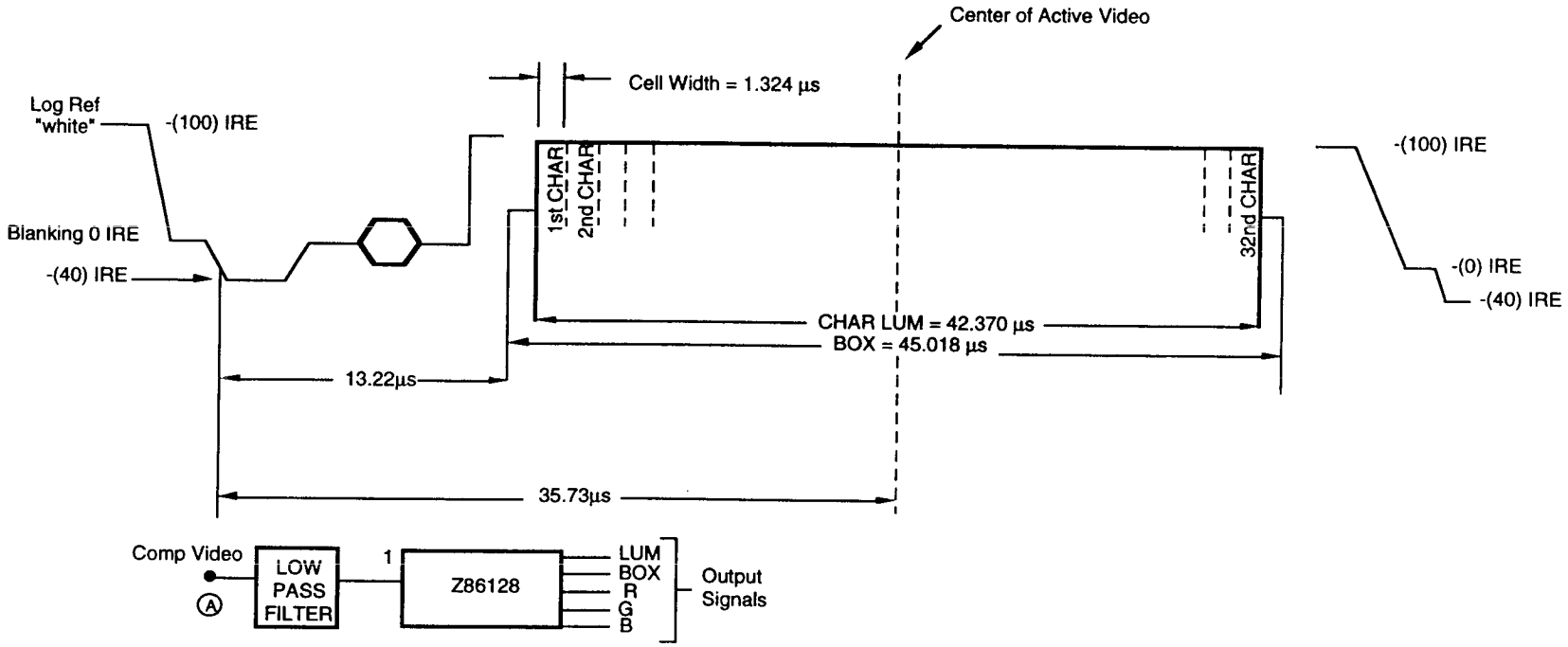


Figure 11. Line 21 AC/DC Timing

The serial input shift register is loaded via the SDA, SCK and SEN pins as indicated by the timing (Figure 12). When the SEN pin is Low the serial interface is disabled and the SDA pin will be an input. On the Low to High transition of SEN, the state of the Serial Status (SS) bit will be ***output*** on the SDA pin. The SEN pin should remain High for the duration of the data transfer. On the first High to Low transition of SCK the SDA pin will be restored to the input mode state. Serial input data may then be driven into the SDA pin which will be clocked in on the positive transitions of the SCK signal. The serial data stream consists of eight data: bits (B0-B7) and one address bit (A0). The bit assignments are given in Table 6.

The A0 bit determines if the eight Serial Data bits will be loaded into the Hardware Control Register or if the Serial Status bit will be set. If A0 is Low, the contents of the Input Shift Register will be loaded into the Hardware Control Register when the SEN pin is brought Low. If A0 is High, the Serial Status bit will be set when the SEN pin is brought Low. This indicates to the Command Processor that the Input Shift Register should be serviced. The Command Processor will clear the Serial Status bit.

The Hardware Register is used to turn the Decoder On or OFF and to Reset the IC. To do this the A0 bit and all reserved bits must be set to zero (0).

To Reset the part clock in the data with bits B6 and B7 set to a one (1). Then clock in data with those bits returned to 0.

To turn the Decoder On, clock in data with bit B1 set to 1 and all other bits set to 0. To turn the Decoder Off, clock in data with all bits set to 0.

The Input Shift Register is used to control the Data Channel to be processed by the Decoder. To set the desired operation, data must be clocked in with the Z0 bit set to 1. The B1 and B2 bits are then used to control the LANGuage I or II and the Captions or Text selections. All other B bits much be set to 0. Bit B1 = 1 sets the LANG to language 1 and B1 = 0 sets it to language 2. Bit B2 = 1 sets the Decoder to recover Captions and B2 = 0 sets Text recovery.

In writing to both the Hardware and Input Shift Registers, it is recommended that the serial port be rewritten by the system at some convenient rate. Please refer to the Serial Mode Timing Diagram (Figure 12) for the details of how to input the serial data.

Use of the Status Bit

The Status Bit is used to inform the sender that the serial data previously clocked into the Control Port Software Register has been processed and that new data can now be clocked in. If only occasional data is being input or if the Hardware Register is loaded before the Input Shift Register, then monitoring the STATUS BIT is unnecessary. However, if repeated data is clocked into the Input Shift Register or if the Hardware Register is loaded immediately after the Input Shift Register, then the STATUS BIT output should be checked or the data in the Register may be overwritten. It takes no more than one TV frame time (33 msec) to read in the data from the Input Shift Register.

The STATUS BIT is output when SEN is switched High. If the bit is a 1, then the Command Processor has not yet read the previously supplied serial data. The SEN signal should then be switched Low and no clocks should be provided. If the STATUS BIT is a 0, then normal serial data clocking should proceed.

Table 6. Control and Shift Register Bits

Bit No.	Hardware Control Register	Input Shift Register
B0	Reserved	Reserved
B1	Decoder On/Off, HI=ON, LO=OFF	LANG Select, HI=I, LO=II
B2	Reserved	C/T Select, HI=F1, LO
B3	Reserved	Field Select (1=F2, 0=F1)
B4	Reserved	Reserved
B5	Reserved	Reserved
B6	Command Processor Reset	Reserved
B7	Chip Reset	Reserved
A0	0	1

Note:
Reserved bits must be = 0, Low

Serial Control Mode

The three control pins, DONEN (Pin 1), CTDA (Pin 17) and LNGCK (Pin 18), control the operating modes of the Line 21 ASIC. They can be operated in either the Parallel Control mode or the Serial Control mode. The control mode is selected by setting the state of NSIN (Pin 16). When NSIN is Low, the Serial Control mode is selected.

The Serial Control mode controls the operating modes of the Line 21 ASIC by using a three wire serial bus. (This bus can coexist with an IIC bus since the DATA pin (Pin 17) and CLK pin (Pin 18) are high-impedance when the ENA (Pin 1) pin is Low).

The Serial Control Port has two 8-bit internal registers, the Hardware Control Register (HCR) and the Software Control Register (SCR). Data is clocked into the appropriate register under the control of a steering bit, A0. When A0 is Low, the serial data is clocked into the HCR, and when A0 is High, it is clocked into the SCR.

The readiness of the Serial Control Port to accept data is indicated by a Serial Status (SS) bit. The SS bit is output on the DATA pin when the ENA pin is first brought High. The status of the SS bit should be read and if it is High, then the Serial Control Port can not be loaded and ENA should be brought Low.

The port can be polled until SS is Low, at which time a Serial Control byte can be entered. The loading sequence is continued by first generating a High to Low transition on the CLK pin, which changes the DATA pin from output mode to input mode. (CLK may be in either the High or Low state when ENA is first brought High). The control byte is then clocked in on the rising edge of CLK, least significant bit (LSB) first. Once the 8 bits have been clocked in, the steering bit A0 is read in by bringing the ENA pin Low again. This ends the load sequence. Each control byte must be entered using this sequence.

The Serial Control Port can perform the functions available in the Parallel Control mode, namely selecting the data channel to be displayed and the Decoder On/Off state. It can also be used to Reset the part, to Reset the Command Processor only and to switch decoder operation from Field 1 decoding to Field 2 decoding. The control bytes needed to perform these selections are listed below in Table 1.

In order to initiate operation when power is first applied, the required procedure is to load HCR with Reset (C0) first. Then, load SCR with the appropriate data channel control byte, for example C1, F1 (06). Followed this by loading HCR with Decoder ON (02). Subsequent changes in operating conditions should be made without resetting the part.

The timing diagram for the control signals is shown in Figure 12.

Table 6. Serial Control Bytes

Function	Bits 0	1	2	3	4	5	6	7	Byte (Hex)
HCR Control Bytes (A0 = 0)									
Reset	0	0	0	0	0	0	1	1	C0
Decoder ON	0	1	0	0	0	0	0	0	02
Decoder OFF	0	0	0	0	0	0	0	0	00
SCR Control Bytes (A0=1)									
C1, F1	0	1	1	0	0	0	0	0	06
C2, F1	0	0	1	0	0	0	0	0	04
T1, F1	0	1	0	0	0	0	0	0	02
T2, F1	0	0	0	0	0	0	0	0	00
C1, F2	0	1	1	1	0	0	0	0	0E
C2, F2	0	0	1	1	0	0	0	0	0C
T1, F2	0	1	0	1	0	0	0	0	0A
T2, F2	0	0	0	1	0	0	0	0	08

Control Port Descriptions

Port Control	
Parallel Mode (NSIN = High)	Serial Mode (NSIN = Low)
Pin 1 = Decoder On/Off, CMOS input, High = On, Low = Off	Pin 1 = Serial Enable (SEN)
Pin 17 = Captions/Text, CMOS input, High = Captions, Low = Text	Pin 17 = Serial Data (SDA)
Pin 18 = LANG I/II, CMOS input, High = LANG I, Low = LANG II	Pin 18 = Serial Clock (SCK)

Horizontal Timing

The timing of the output signals; Box, Luminance, and RGB is set so that the start of the leading box preceding the first displayable character cell will occur at 13.22 µs. This is after the midpoint of the leading edge of the horizontal sync pulse of the composite video signal is fed to the 600 kHz low pass filter at the input to the Z86128. It is assumed that the delay through the filter will be 220 ns (refererence Figure 11).

There are two ways to execute a FULL RESET of the Z86128:

1. Hold NRESET Low for 100 ns. This stops all internal circuits. The part is static and 100 ns is the worst case time for the NRESET signal to propagate through the various gates.
2. Send NRESET command through the serial interface. The result is the same as in number 1.

FULL RESET is useful during power-up. A FULL RESET of the part during normal operation is not necessary.

A partial reset may also be executed through the serial interface only. This is the COMMAND PROCESSOR RESET. Basically, all internal timing circuits continue to operate, but the caption display is removed from the screen and the Z86128 waits for new line 21 data. This is useful for situations such as channel change.

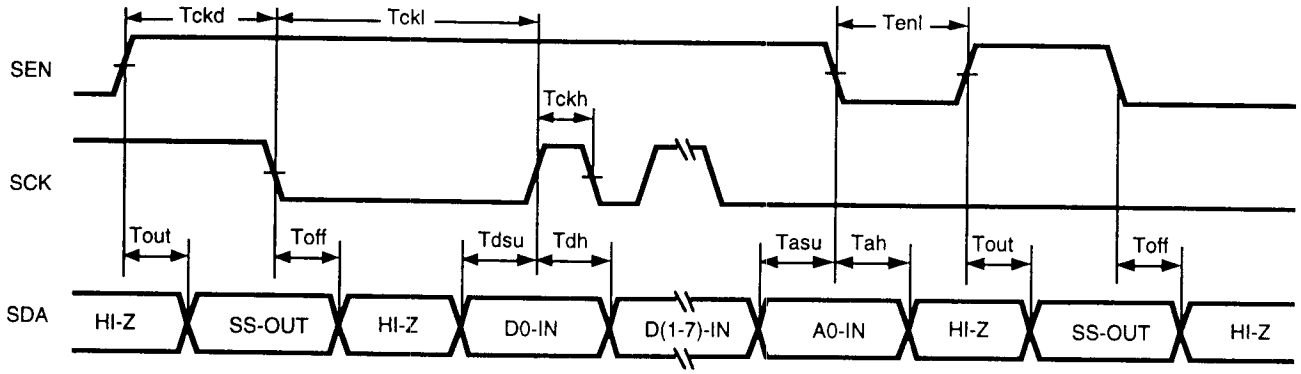
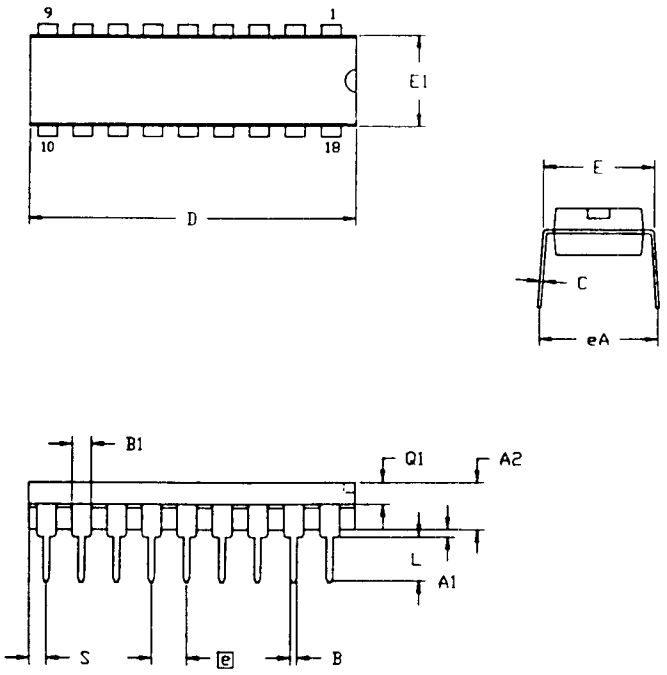


Figure 12. Serial Mode Timing Diagram

Symbol	Description	Min.	Max.	Units
T_{OUT}	Output enable time, ENA rising edge to Data Out		200	ns
T_{OFF}	Output disable time, CLK or ENA falling edge to Data Hi-Z		100	ns
T_{CKD}	Data read time, ENA rising edge to CLK low	200		ns
T_{CKL}	CLK low time	200		ns
T_{CKH}	CLK high time	200		ns
T_{DSU}	Data set up time	100		ns
T_{DH}	Data hold time	100		ms
T_{ENI}	ENA low time	200		ns
T_{ASU}	A0 set up time	100		ns
T_{AH}	A0 hold time	100		ns

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

18-Pin DIP Package Diagram

ORDERING INFORMATION

Z86128

12 MHz
18-Pin DIP
Z8612812PSC

For fast results, contact your Zilog sales office for assistance in ordering the part desired.

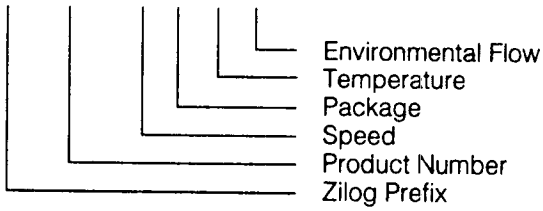
Package
P = Plastic DIP

Temperature
S = 0°C to +70°C

Speed
12 = 12 MHz

Environmental
C= Plastic Standard

Example:
Z 86128 12 P S C is an 86128, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



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Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
Telex 910-338-7621
FAX 408 370-8056