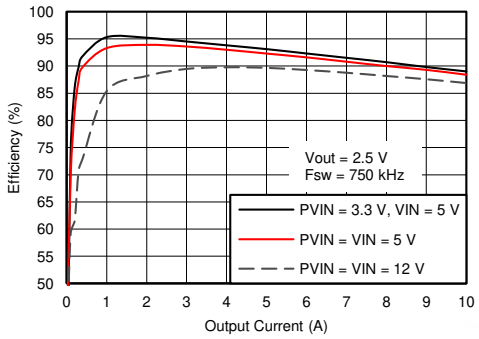
TPS84A20 2.95V 至 17V 输入、10A 同步降压集成式电源解决方案

1 特性

- 完整的集成式电源解决方案可实现小尺寸和扁平设计
- 10mm × 10mm × 4.3mm 封装
- 效率最高可达 95%
- Eco-mode™/轻负载效率 (LLE)
- 宽输出电压调节范围为 0.6V 至 5.5V，基准精度为 1%
- 支持针对更高电流的并行运行
- 可选分离电源轨可实现低至 2.95V 的输入电压
- 可调节的开关频率范围（200kHz 至 1.2MHz）
- 与外部时钟同步
- 提供 180° 异相位时钟信号
- 可调慢速启动
- 输出电压排序/跟踪
- 电源正常输出
- 可编程欠压锁定 (UVLO)
- 过流和过热保护
- 预偏置输出启动
- 工作温度范围：–40°C 至 +85°C
- 增强的散热性能：13.3°C/W
- 符合 EN55022 B 类辐射标准

2 应用

- 宽带和通信基础设施
- 自动测试和医疗设备
- 紧凑型 PCI/PCI 快速接口/PXI 快速接口
- DSP 和 FPGA 负载点 应用

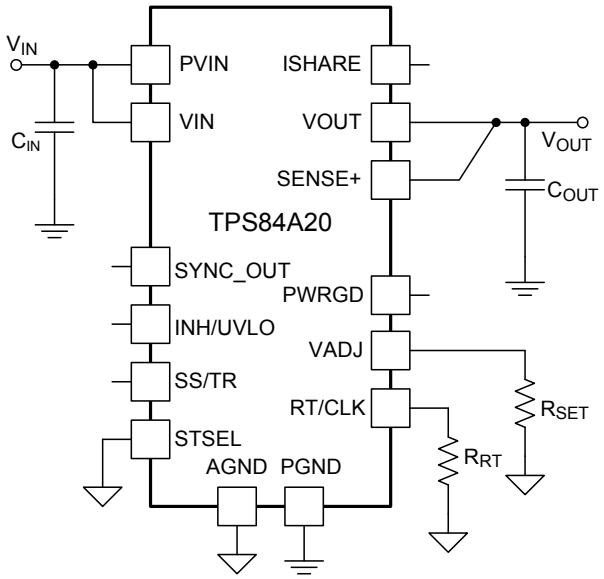


3 说明

TPS84A20 是一个简单易用的集成式电源解决方案，它在一个小外形尺寸的 QFN 封装内整合了一个带有功率 MOSFET 的 10A 直流/直流转换器、一个电感器以及无源器件。此整体电源解决方案仅需三个外部组件，并省去了环路补偿和磁性元件选择过程。

此器件采用 10mm × 10mm × 4.3mm QFN 封装，可轻松焊接到印刷电路板上，并可实现紧凑的负载点设计。可实现超过 95% 的效率，具有热阻为 13.3°C/W 的出色功率耗散能力。TPS84A20 提供离散负载点设计的灵活性和特性集，并且非常适合为广泛的集成电路 (IC) 和系统供电。先进的封装技术可提供一个与标准 QFN 贴装和测试技术兼容的稳健耐用且可靠的电源解决方案。

简化应用



4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (April 2018) to Revision C **Page**

- Added V_{OUT} Range values under different I_{OUT} conditions in Table 9 24

Changes from Revision A (June 2017) to Revision B **Page**

- 已添加 TI 参考设计顶部导航图标 1
- Increased the peak reflow temperature and maximum number of reflows to JEDEC specification for improved manufacturability 3
- 添加*机械、封装和可订购信息* 部分 30

Changes from Original (MARCH 2013) to Revision A **Page**

- Added peak reflow and maximum number of reflows information 3
- Added Parallel Operation section 19

Table 1. Ordering Information

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating temperature range (unless otherwise noted)		MIN	MAX	UNIT
Input Voltage	VIN, PVIN	–0.3	20	V
	INH/UVLO, PWRGD, RT/CLK, SENSE+	–0.3	6	V
	ILIM, VADJ, SS/TR, STSEL, SYNC_OUT, ISHARE, OCP_SEL	–0.3	3	V
Output Voltage	PH	–1.0	20	V
	PH 10ns Transient	–3.0	20	V
	VOUT	–0.3	6	V
Source Current	RT/CLK, INH/UVLO		±100	µA
	PH		current limit	A
Sink Current	PH		current limit	A
	PVIN		current limit	A
	PWRGD	–0.1	2	mA
Operating Junction Temperature		–40	125(2)	°C
Storage Temperature		–65	150	°C
Peak Reflow Case Temperature(3)(4)			245	°C
Maximum Number of Reflows Allowed(3)(4)			3	
Mechanical Shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		1500	G
Mechanical Vibration	Mil-STD-883D, Method 2007.2, 20-2000Hz		20	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See the temperature derating curves in the Typical Characteristics section for thermal information.
(3) For soldering specifications, refer to the *Soldering Requirements for BQFN Packages* application note.
(4) Devices with a date code prior to week 14 2018 (1814) have a peak reflow case temperature of 240°C with a maximum of one reflow.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)		MIN	NOM	MAX	UNIT
PV_{IN}	Input Switching Voltage	2.95		17	V
V_{IN}	Input Bias Voltage	4.5		17	V
V_{OUT}	Output Voltage	0.6		5.5	V
f_{SW}	Switching Frequency	200		1200	kHz

5.3 Package Specifications

TPS84A20		UNIT
Weight		1.45 grams
Flammability	Meets UL 94 V-O	
MTBF Calculated reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	37.4 MHrs

5.4 Electrical Characteristics

Over –40°C to 85°C free-air temperature, PV_{IN} = V_{IN} = 12 V, V_{OUT} = 1.8 V, I_{OUT} = 10 A, C_{IN} = 0.1 µF + 2 x 22 µF ceramic + 100 µF bulk, C_{OUT} = 4 x 47 µF ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OUT}	Output current	T_A = 85°C, natural convection		0 (1)		10	A
V_{IN}	Input bias voltage range	Over output current range		4.5		17	V
PV_{IN}	Input switching voltage range	Over output current range		2.95 (2)		17 (3)	V
UVLO	V_{IN} Undervoltage lockout	V_{IN} Increasing			4.0	4.5	V
		V_{IN} Decreasing		3.5	3.85		
$V_{OUT(adj)}$	Output voltage adjust range	Over output current range		0.6		5.5	V
V_{OUT}	Set-point voltage tolerance	T_A = 25°C, I_{OUT} = 0 A				±1% (4)	
	Temperature variation	–40°C ≤ T_A ≤ +85°C, I_{OUT} = 0 A			±0.2%		
	Line regulation	Over input voltage range			±0.1%		
	Load regulation	Over output current range			±0.2%		
	Total output voltage variation	Includes set-point, line, load, and temperature variation				±1.5% (4)	
η	Efficiency	P_{VIN} = V_{IN} = 12 V, I_O = 5 A	V_{OUT} = 5.0 V, f_{SW} = 1 MHz		93 %		
			V_{OUT} = 3.3 V, f_{SW} = 750 kHz		92 %		
			V_{OUT} = 2.5 V, f_{SW} = 750 kHz		90 %		
			V_{OUT} = 1.8 V, f_{SW} = 500 kHz		89 %		
			V_{OUT} = 1.2 V, f_{SW} = 300 kHz		86 %		
			V_{OUT} = 0.9 V, f_{SW} = 250 kHz		84 %		
			V_{OUT} = 0.6 V, f_{SW} = 200 kHz		81 %		
		P_{VIN} = V_{IN} = 5 V, I_O = 5 A	V_{OUT} = 3.3 V, f_{SW} = 750 kHz		94 %		
			V_{OUT} = 2.5 V, f_{SW} = 750 kHz		93 %		
			V_{OUT} = 1.8 V, f_{SW} = 500 kHz		92 %		
			V_{OUT} = 1.2 V, f_{SW} = 300 kHz		89 %		
			V_{OUT} = 0.9 V, f_{SW} = 250 kHz		87 %		
			V_{OUT} = 0.6 V, f_{SW} = 200 kHz		83 %		
	Output voltage ripple	20 MHz bandwidth			14		mV_{P-P}
I_{LIM}	Current limit threshold	ILIM pin open			15		A
		ILIM pin to AGND			12		A
	Transient response	1.0 A/µs load step from 25 to 75% $I_{OUT(max)}$	Recovery time		100		µs
			VOUT over/undershoot		80		mV
V_{INH}	Inhibit threshold voltage	Inhibit High Voltage		1.3		open (5)	V
		Inhibit Low Voltage		-0.3		1.1	
I_{INH}	INH Input current	V_{INH} < 1.1 V			-1.15		µA
	INH Hysteresis current	V_{INH} > 1.3 V			-3.3		µA
$I_{I(stby)}$	Input standby current	INH pin to AGND			2	10	µA
Power Good	PWRGD Thresholds	V_{OUT} rising	Good		95%		
			Fault		108%		
		V_{OUT} falling	Fault		91%		
			Good		104%		
	PWRGD Low Voltage	I(PWRGD) = 0.5 mA				0.3	V
f_{SW}	Switching frequency	R_{RT} = 169 kΩ		400	500	600	kHz
f_{CLK}	Synchronization frequency	CLK Control		200		1200	kHz
V_{CLK-H}	CLK High-Level			2.0		5.5	V
V_{CLK-L}	CLK Low-Level					0.5	V
D_{CLK}	CLK Duty Cycle			20	50	80	%

(1) See Light Load Efficiency (LLE) section for more information for output voltages < 1.5 V.
(2) The minimum P_{VIN} is 2.95 V or (V_{OUT} + 0.7 V), whichever is greater. See Table 9 for more details.
(3) The maximum PV_{IN} voltage is 17 V or (22 x V_{OUT}), whichever is less. See Table 9 for more details.
(4) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external R_{SET} resistor.
(5) Value when no voltage divider is present at the INH/UVLO pin. This pin has an internal pull-up. If it is left open, the device operates when input power is applied. A small, low-leakage MOSFET is recommended for control. Do not tie this pin to VIN.

Electrical Characteristics (continued)

Over –40°C to 85°C free-air temperature, PV_{IN} = V_{IN} = 12 V, V_{OUT} = 1.8 V, I_{OUT} = 10 A,
C_{IN} = 0.1 µF + 2 x 22 µF ceramic + 100 µF bulk, C_{OUT} = 4 x 47 µF ceramic (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal Shutdown		Thermal shutdown		175		°C
		Thermal shutdown hysteresis		10		°C
C_{IN}	External input capacitance	Ceramic	44 (6)			µF
		Non-ceramic		100 (6)		
C_{OUT}	External output capacitance	Ceramic	47 (7)	200	1500	µF
		Non-ceramic		220 (7)	5000 (8)	
		Equivalent series resistance (ESR)			35	mΩ

(6) A minimum of 44 µF of external ceramic capacitance is required across the input (VIN and PVIN connected) for proper operation. An additional 100 µF of bulk capacitance is recommended. It is also recommended to place a 0.1-µF ceramic capacitor directly across the PVIN and PGND pins of the device. Locate the input capacitance close to the device. When operating with split VIN and PVIN rails, place 4.7µF of ceramic capacitance directly at the VIN pin. See Table 6 for more details.
(7) The amount of required output capacitance varies depending on the output voltage (see Table 5). The amount of required capacitance must include at least 1x 47 µF ceramic capacitor. Locate the capacitance close to the device. Adding additional capacitance close to the load improves the response of the regulator to load transients. See Table 5 and Table 6 more details.
(8) The maximum output capacitance of 5000 µF includes the combination of both ceramic and non-ceramic capacitors.

5.5 Thermal Information

THERMAL METRIC (1)		TPS84A20 RVQ42 42 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance (2)	13.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter (3)	1.6	
ψ_{JB}	Junction-to-board characterization parameter (4)	5.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics Application Report*.
(2) The junction-to-ambient thermal resistance, θ_{JA}, applies to devices soldered directly to a 100-mm x 100-mm double-sided PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces θ_{JA}.
(3) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JT} * Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} * Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

6 Device Information

Functional Block Diagram

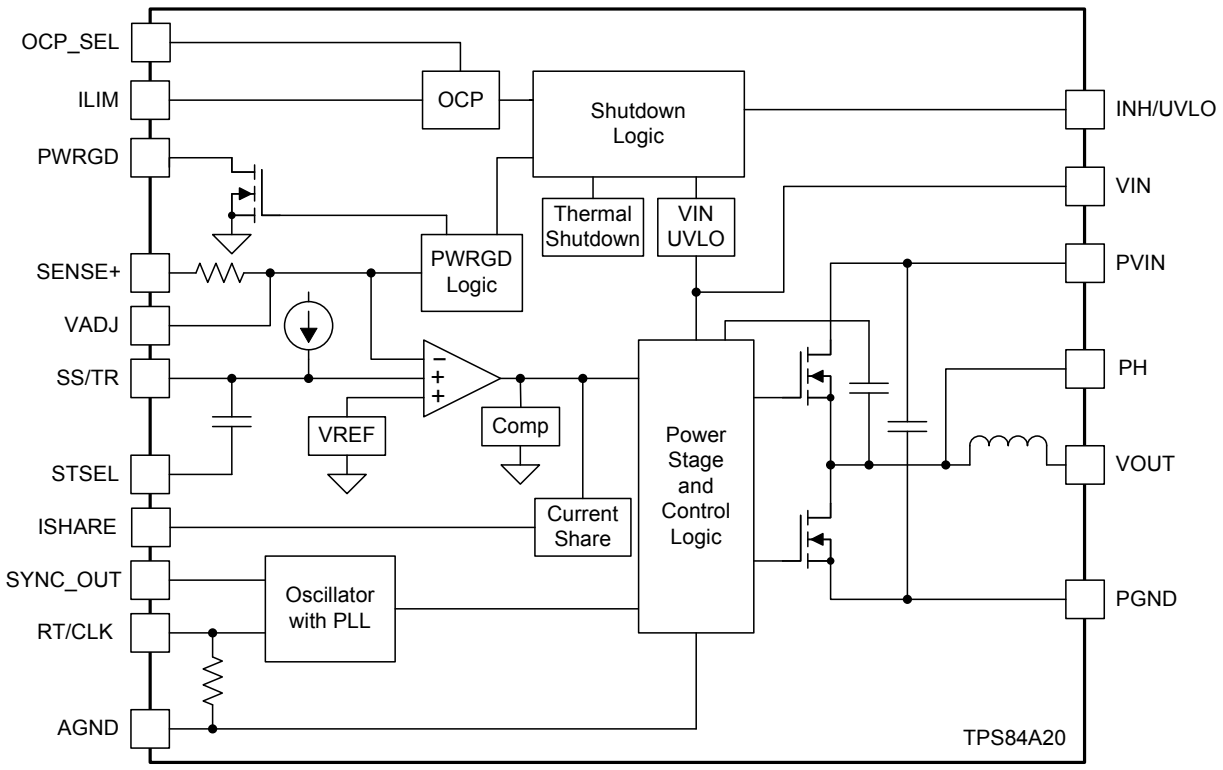


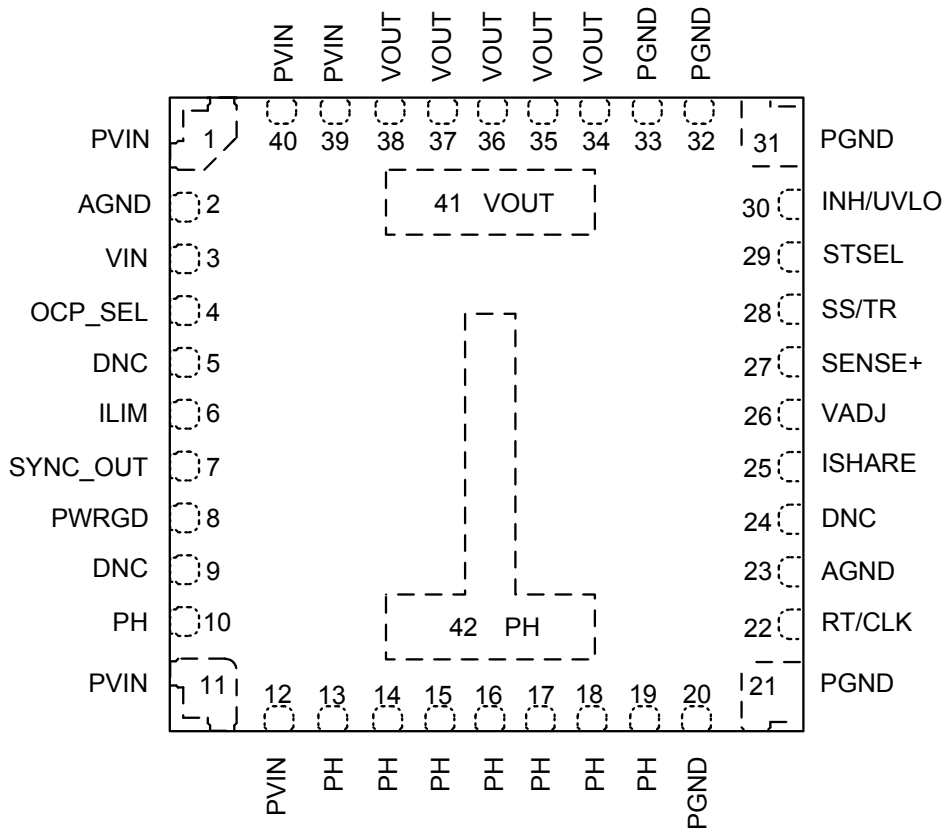
Table 2. Pin Descriptions

TERMINAL		DESCRIPTION
NAME	NO.	
AGND	2	Zero volt reference for the analog control circuit. These pins are not connected together internal to the device and must be connected to one another using an AGND plane of the PCB. These pins are associated with the internal analog ground (AGND) of the device. See *Layout Considerations*.
	23	
PGND	20	This is the return current path for the power stage of the device. Connect these pins to the load and to the bypass capacitors associated with PVIN and VOUT.
	21	
	31	
	32	
	33	
VIN	3	Input bias voltage pin. Supplies the control circuitry of the power converter. Connect this pin to the input bias supply. Connect bypass capacitors between this pin and PGND.
PVIN	1	Input switching voltage. Supplies voltage to the power switches of the converter. Connect these pins to the input supply. Connect bypass capacitors between these pins and PGND.
	11	
	12	
	39	
	40	
VOUT	34	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external bypass capacitors between these pins and PGND.
	35	
	36	
	37	
	38	
	41	
PH	10	Phase switch node. These pins must be connected to one another using a small copper island under the device for thermal relief. Do not place any external component on these pins or tie them to a pin of another function.
	13	
	14	
	15	
	16	
	17	
	18	
	19	
	42	
DNC	5	Do not connect. Do not connect these pins to AGND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
	9	
	24	
ISHARE	25	Current share pin. Connect this pin to other TPS84A20 devices ISHARE pin when paralleling multiple TPS84A20 devices. When unused, treat this pin as a Do Not Connect (DNC) and leave it isolated from all other signals or ground.
OCP_SEL	4	Over current protection select pin. Leave this pin open for hiccup mode operation. Connect this pin to AGND for cycle-by-cycle operation. See *Overcurrent Protection* for more details.
ILIM	6	Current limit pin. Leave this pin open for full current limit threshold. Connect this pin to AGND to reduce the current limit threshold by approximately 20%.
SYNC_OUT	7	Synchronization output pin. Provides a 180° out-of-phase clock signal.
PWRGD	8	Power Good flag pin. This open drain output asserts low if the output voltage is more than approximately ±6% out of regulation. A pullup resistor is required.
RT/CLK	22	This pin is connected to an internal frequency setting resistor which sets the default switching frequency. An external resistor can be connected from this pin to AGND to increase the frequency. This pin can also be used to synchronize to an external clock.
VADJ	26	Connecting a resistor between this pin and AGND sets the output voltage.
SENSE+	27	Remote sense connection. This pin must be connected to VOUT at the load or at the device pins. Connect this pin to VOUT at the load for improved regulation.

Table 2. Pin Descriptions (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
SS/TR	28	Slow-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage rise time. A voltage applied to this pin allows for tracking and sequencing control.
STSEL	29	Slow-start or track feature select. Connect this pin to AGND to enable the internal SS capacitor. Leave this pin open to enable the TR feature.
INH/UVLO	30	Inhibit and UVLO adjust pin. Use an open drain or open collector logic device to ground this pin to control the INH function. A resistor divider between this pin, AGND, and PVIN/VIN sets the UVLO voltage.

RVQ PACKAGE
(TOP VIEW)



7 Typical Characteristics (PVIN = VIN = 12 V)

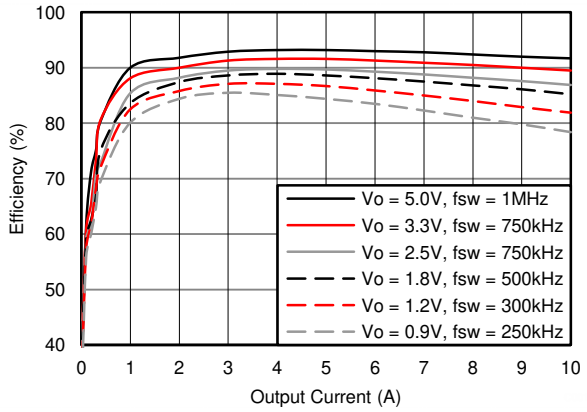


Figure 1. Efficiency versus Output Current

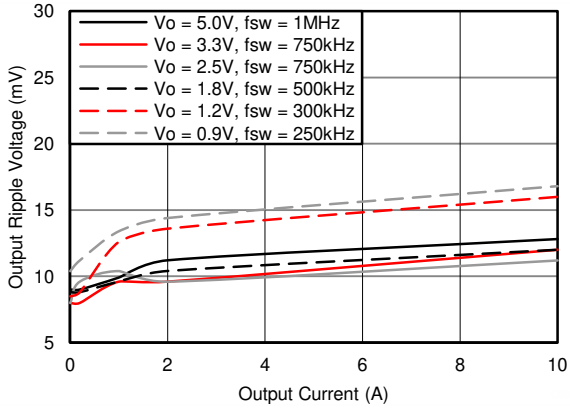


Figure 2. Voltage Ripple versus Output Current

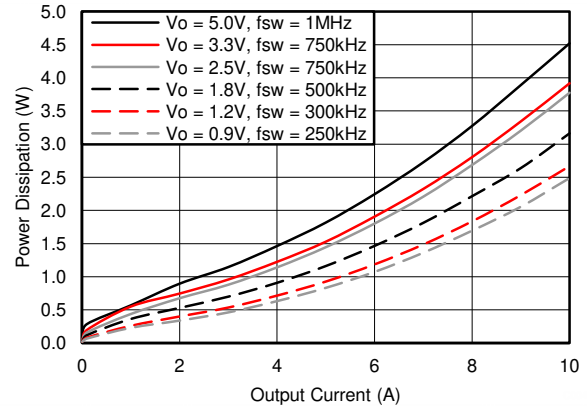


Figure 3. Power Dissipation versus Output Current

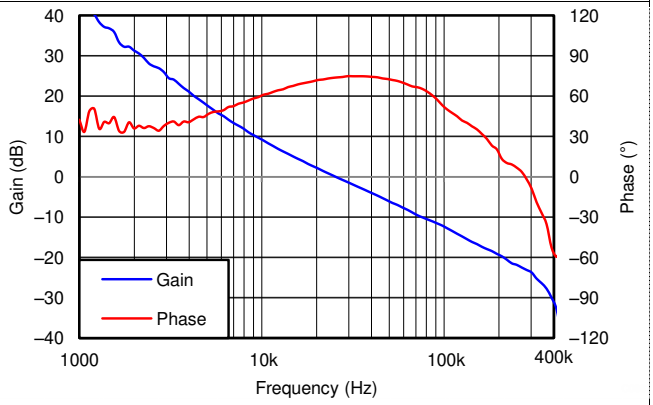


Figure 4. V_{OUT} = 1.8 V, I_{OUT} = 10 A, C_{OUT1} = 200 µF Ceramic, f_{SW} = 500 kHz

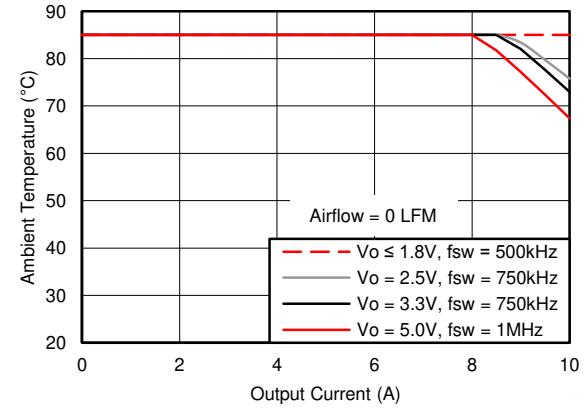


Figure 5. Safe Operating Area

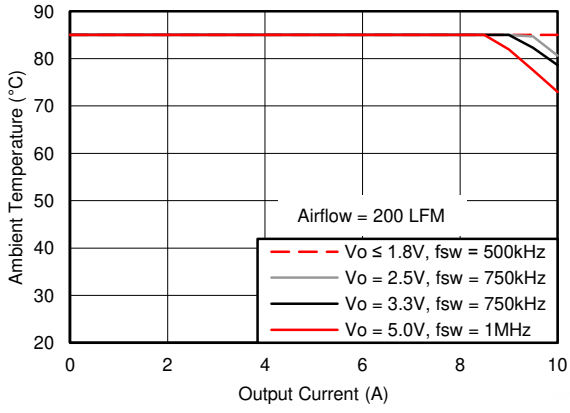


Figure 6. Safe Operating Area

The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100-mm × 100-mm double-sided PCB with 2-oz. copper. Applies to Figure 5 and Figure 6.

8 Typical Characteristics (PVIN = VIN = 5 V)

The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 7, Figure 8, and Figure 9.

The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100-mm × 100-mm double-sided PCB with 2-oz. copper. Applies to Figure 11.

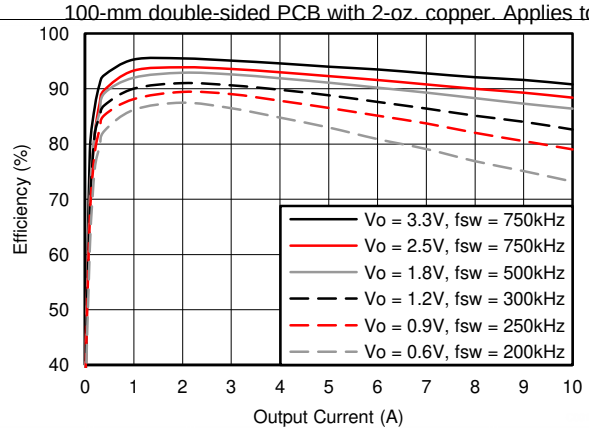


Figure 7. Efficiency versus Output Current

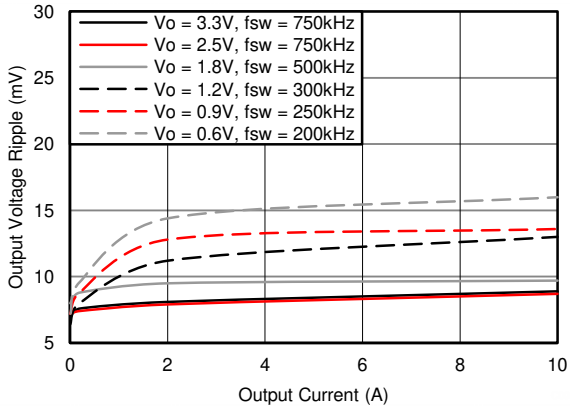


Figure 8. Voltage Ripple versus Output Current

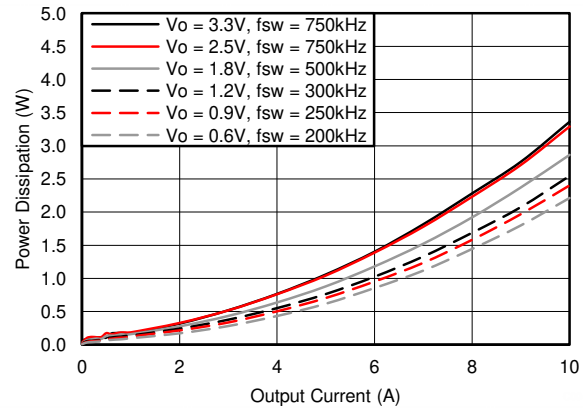


Figure 9. Power Dissipation versus Output Current

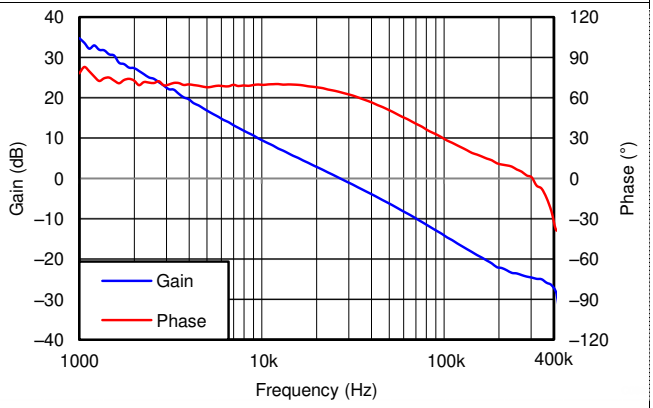


Figure 10. V_{OUT} = 1.8 V, I_{OUT} = 10 A, C_{OUT1} = 200 µF Ceramic, f_{SW} = 500 kHz

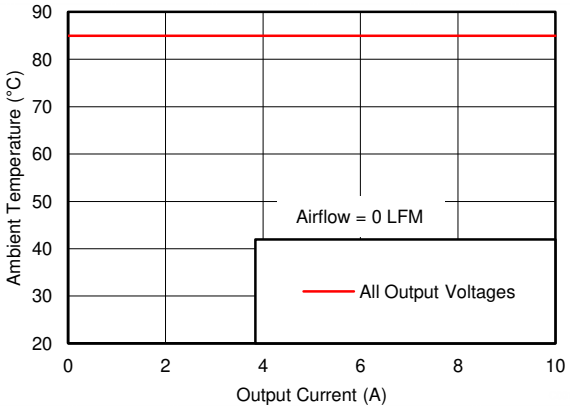


Figure 11. Safe Operating Area

9 Typical Characteristics (PVIN = 3.3 V, VIN = 5 V)

The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 12, Figure 13, and Figure 14.

The temperature derating curves represent the conditions at which internal components are at or below the

Typical Characteristics (PVIN = 3.3 V, VIN = 5 V) (continued)

manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm double-sided PCB with 2 oz. copper. Applies to Figure 16.

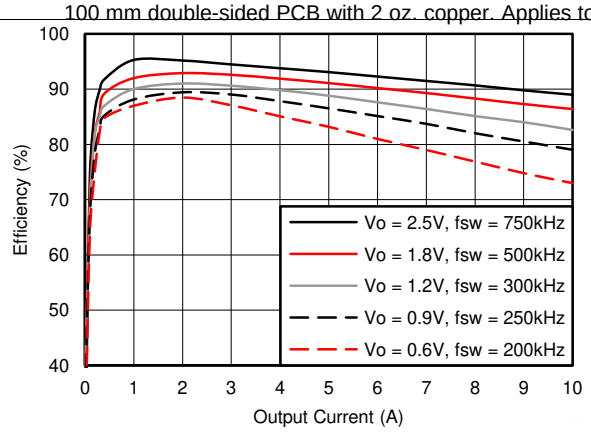


Figure 12. Efficiency versus Output Current

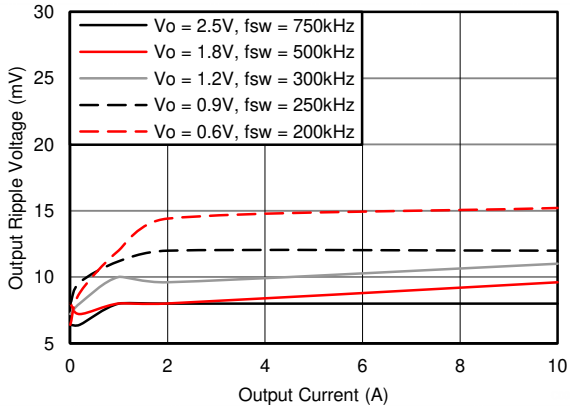


Figure 13. Voltage Ripple versus Output Current

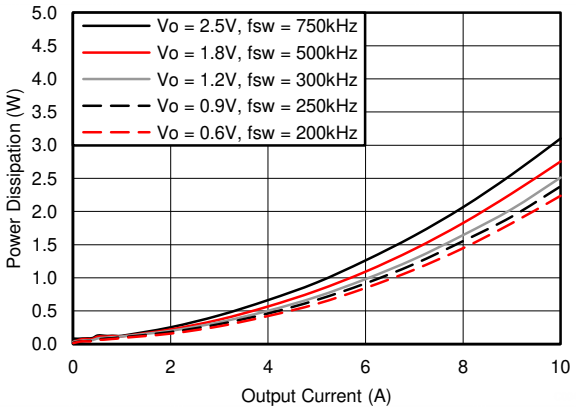


Figure 14. Power Dissipation versus Output Current

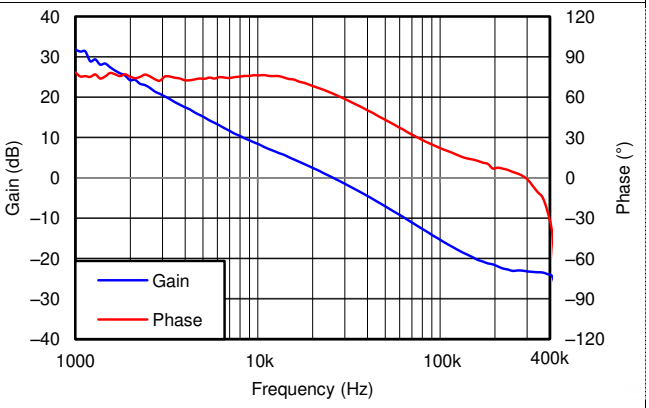


Figure 15. V_{OUT} = 1.8 V, I_{OUT} = 10 A, C_{OUT1} = 200 µF Ceramic, f_{SW} = 500 kHz

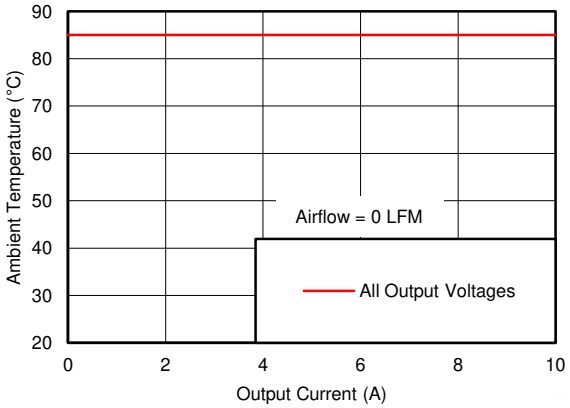


Figure 16. Safe Operating Area

10 Application Information

10.1 Adjusting the Output Voltage

The VADJ control sets the output voltage of the TPS84A20. The output voltage adjustment range is from 0.6 V to 5.5 V. The adjustment method requires the addition of R_{SET}, which sets the output voltage, the connection of SENSE+ to VOUT, and in some cases R_{RT} which sets the switching frequency. The R_{SET} resistor must be connected directly between the VADJ (pin 26) and AGND (pin 23). The SENSE+ pin (pin 27) must be connected to VOUT either at the load for improved regulation or at VOUT of the device. The R_{RT} resistor must be connected directly between the RT/CLK (pin 22) and AGND (pin 23). Table 3 gives the standard external R_{SET} resistor for a number of common bus voltages, along with the recommended R_{RT} resistor for that output voltage.

Table 3. Standard R_{SET} Resistor Values for Common Output Voltages

RESISTORS	OUTPUT VOLTAGE V_{OUT} (V)						
	0.9	1.0	1.2	1.8	2.5	3.3	5.0
R_{SET} (kΩ)	2.87	2.15	1.43	0.715	0.453	0.316	0.196
R_{RT} (kΩ)	1000	1000	487	169	90.9	90.9	63.4

For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 4.

$$R_{SET} = \frac{1.43}{\left(\left(\frac{V_{OUT}}{0.6}\right) - 1\right)} \ (k\Omega) \quad (1)$$

Table 4. Standard R_{SET} Resistor Values

V_{OUT} (V)	R_{SET} (kΩ)	R_{RT}(kΩ)	f_{SW}(kHz)	V_{OUT} (V)	R_{SET} (kΩ)	R_{RT}(kΩ)	f_{SW}(kHz)
0.6	open	OPEN	200	3.1	0.348	90.9	750
0.7	8.66	OPEN	200	3.2	0.332	90.9	750
0.8	4.32	OPEN	200	3.3	0.316	90.9	750
0.9	2.87	1000	250	3.4	0.309	90.9	750
1.0	2.15	1000	250	3.5	0.294	90.9	750
1.1	1.74	1000	250	3.6	0.287	90.9	750
1.2	1.43	487	300	3.7	0.280	90.9	750
1.3	1.24	487	300	3.8	0.267	90.9	750
1.4	1.07	487	300	3.9	0.261	90.9	750
1.5	0.953	487	300	4.0	0.255	90.9	750
1.6	0.866	487	300	4.1	0.243	63.4	1000
1.7	0.787	487	300	4.2	0.237	63.4	1000
1.8	0.715	169	500	4.3	0.232	63.4	1000
1.9	0.665	169	500	4.4	0.226	63.4	1000
2.0	0.619	169	500	4.5	0.221	63.4	1000
2.1	0.576	169	500	4.6	0.215	63.4	1000
2.2	0.536	169	500	4.7	0.210	63.4	1000
2.3	0.511	169	500	4.8	0.205	63.4	1000
2.4	0.475	169	500	4.9	0.200	63.4	1000
2.5	0.453	90.9	750	5.0	0.196	63.4	1000
2.6	0.432	90.9	750	5.1	0.191	63.4	1000
2.7	0.412	90.9	750	5.2	0.187	63.4	1000
2.8	0.392	90.9	750	5.3	0.182	63.4	1000
2.9	0.374	90.9	750	5.4	0.178	63.4	1000
3.0	0.357	90.9	750	5.5	0.174	63.4	1000

10.2 Capacitor Recommendations for the TPS84A20 Power Supply

10.2.1 Capacitor Technologies

10.2.1.1 Electrolytic, Polymer-Electrolytic Capacitors

When using electrolytic capacitors, high-quality, computer-grade electrolytic capacitors are recommended. Polymer-electrolytic type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo OS-CON capacitor series is suggested due to the lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range of 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0°C.

10.2.1.2 Ceramic Capacitors

The performance of aluminum electrolytic capacitors is less effective than ceramic capacitors above 150 kHz. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

10.2.1.3 Tantalum, Polymer-Tantalum Capacitors

Polymer-tantalum type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo POSCAP series and Kemet T530 capacitor series are recommended rather than many other tantalum types due to their lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

10.2.2 Input Capacitor

The TPS84A20 requires a minimum input capacitance of 44 µF of ceramic type. An additional 100 µF of non-ceramic capacitance is recommended for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage. At worst case, when operating at 50% duty cycle and maximum load, the combined ripple current rating of the input capacitors must be at least 5 Arms. Table 6 includes a preferred list of capacitors by vendor. It is also recommended to place a 0.1-µF ceramic capacitor directly across the PVIN and PGND pins of the device. When operating with split VIN and PVIN rails, place 4.7 µF of ceramic capacitance directly at the VIN pin.

10.2.3 Output Capacitor

The required output capacitance is determined by the output voltage of the TPS84A20. See Table 5 for the amount of required capacitance. The effects of temperature and capacitor voltage rating must be considered when selecting capacitors to meet the minimum required capacitance. The required output capacitance can be comprised of all ceramic capacitors, or a combination of ceramic and bulk capacitors. The required capacitance must include at least one 47 µF ceramic. When adding additional non-ceramic bulk capacitors, low-ESR devices like the ones recommended in Table 6 are required. The required capacitance above the minimum is determined by actual transient deviation requirements. See Table 7 for typical transient response values for several output voltage, input voltage and capacitance combinations. Table 6 includes a preferred list of capacitors by vendor.

Table 5. Required Output Capacitance

V_{OUT} RANGE (V)		MINIMUM REQUIRED C_{OUT} (µF)
MIN	MAX	
0.6	< 0.8	500 µF (1)
0.8	< 1.2	300 µF (1)
1.2	< 3.0	200 µF (1)
3.0	< 4.0	100 µF (1)
4.0	5.5	47 µF ceramic

(1) Minimum required must include at least one 47-µF ceramic capacitor.

Table 6. Recommended Input/Output Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (µF)	ESR (2) (mΩ)
Murata	X5R	GRM32ER61E226K	25	22	2
TDK	X5R	C3225X5R0J107M	6.3	100	2
TDK	X5R	C3225X5R0J476K	6.3	47	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
Murata	X5R	GRM32ER60J476M	6.3	47	2
Panasonic	EEH-ZA	EEH-ZA1E101XP	25	100	30
Sanyo	POSCAP	16TQC68M	16	68	50
Kemet	T520	T520V107M010ASE025	10	100	25
Sanyo	POSCAP	10TPE220ML	10	220	25
Sanyo	POSCAP	6TPE100MI	6.3	100	25
Sanyo	POSCAP	2R5TPE220M7	2.5	220	7
Kemet	T530	T530D227M006ATE006	6.3	220	6
Kemet	T530	T530D337M006ATE010	6.3	330	10
Sanyo	POSCAP	2TPF330M6	2.0	330	6
Sanyo	POSCAP	6TPE330MFL	6.3	330	15

(1) **Capacitor Supplier Verification, RoHS, Lead-free, and Material Details**
Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Maximum ESR at 100 kHz, 25°C.

10.3 Transient Response

Table 7. Output Voltage Transient Response

C_{IN1} = 3x 47 µF CERAMIC, C_{IN2} = 100 µF POLYMER-TANTALUM						
V_{OUT} (V)	V_{IN} (V)	C_{OUT1} CERAMIC	C_{OUT2} BULK	VOLTAGE DEVIATION (mV)		RECOVERY TIME (µs)
				2.5 A LOAD STEP, (1 A/µs)	5 A LOAD STEP, (1 A/µs)	
0.6	5	500 µF	220 µF	25	60	100
	12	500 µF	220 µF	30	65	100
0.9	5	300 µF	220 µF	40	85	100
		300 µF	470 µF	35	70	110
	12	300 µF	220 µF	45	90	100
		300 µF	470 µF	35	75	110
1.2	5	200 µF	220 µF	55	110	110
		200 µF	470 µF	45	90	110
	12	200 µF	220 µF	55	110	110
		200 µF	470 µF	45	90	110
1.8	5	200 µF	220 µF	70	140	130
		200 µF	470 µF	60	120	140
	12	200 µF	220 µF	70	145	140
		200 µF	470 µF	55	120	150
3.3	5	100 µF	220 µF	115	230	200
	12	100 µF	220 µF	120	240	200

10.4 Transient Waveforms

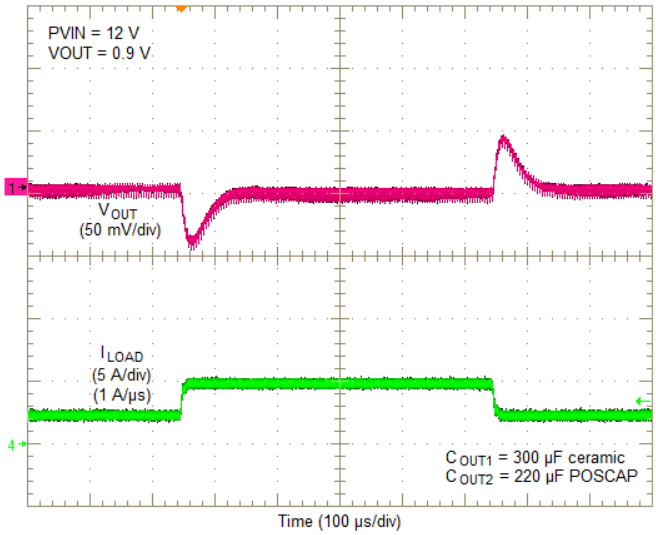


Figure 17. PVIN = 12 V, VOUT = 0.9 V, 2.5 A Load Step

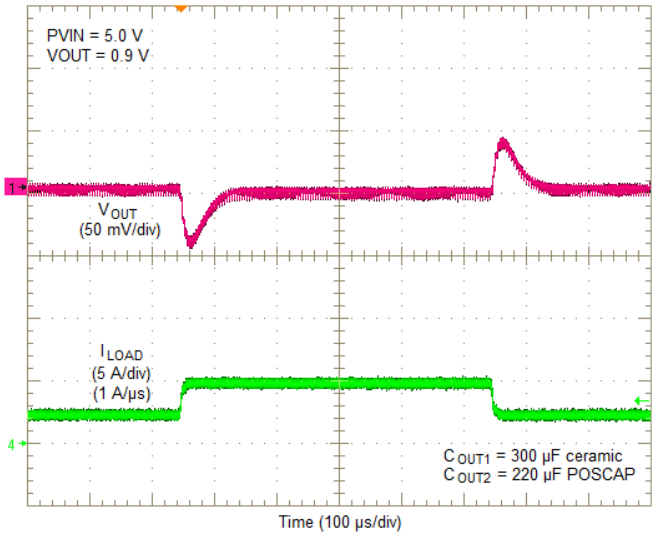


Figure 18. PVIN = 5 V, VOUT = 0.9 V, 2.5 A Load Step

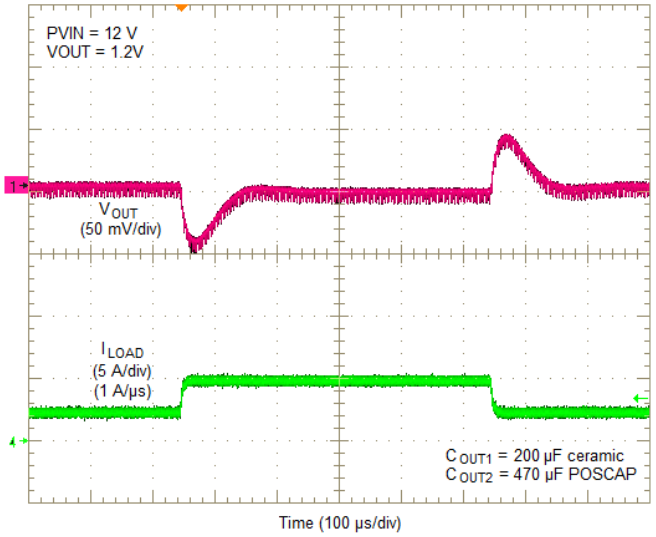


Figure 19. PVIN = 12 V, VOUT = 1.2 V, 2.5 A Load Step

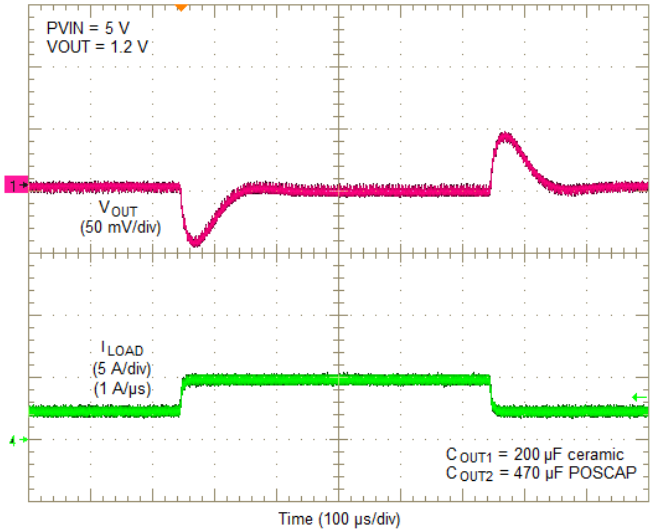


Figure 20. PVIN = 5 V, VOUT = 1.2 V, 2.5 A Load Step

Transient Waveforms (continued)

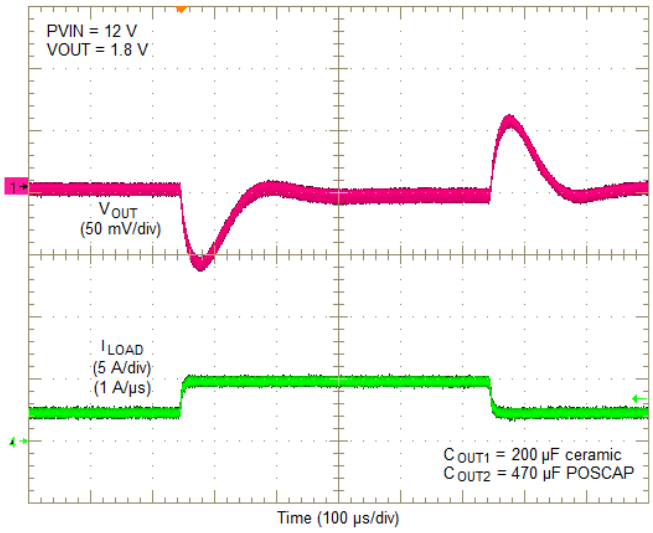


Figure 21. PVIN = 12 V, VOUT = 1.8 V, 2.5 A Load Step

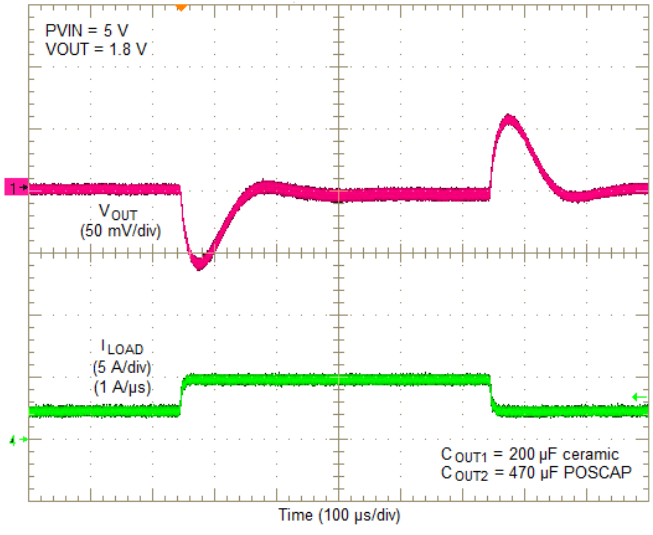


Figure 22. PVIN = 5 V, VOUT = 1.8 V, 2.5 A Load Step

10.5 Application Schematics

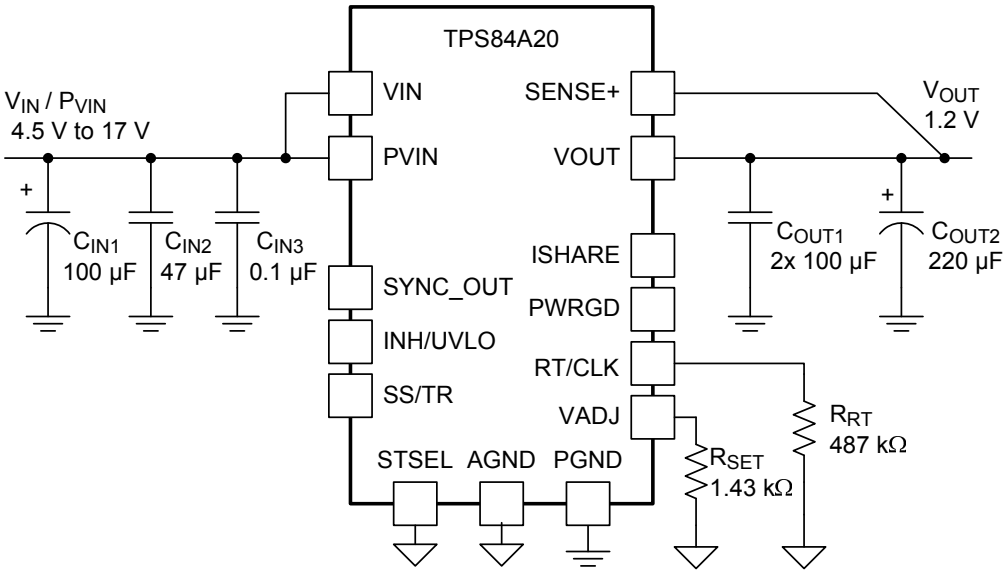


Figure 23. Typical Schematic
PVIN = VIN = 4.5 V to 17 V, VOUT = 1.2 V

Application Schematics (continued)

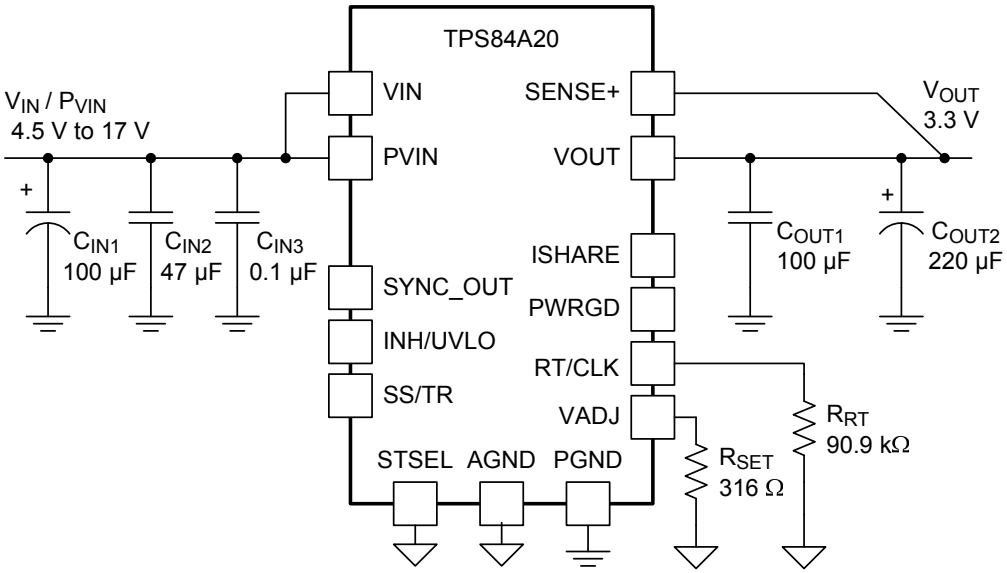


Figure 24. Typical Schematic
PVIN = VIN = 4.5 V to 17 V, VOUT = 3.3 V

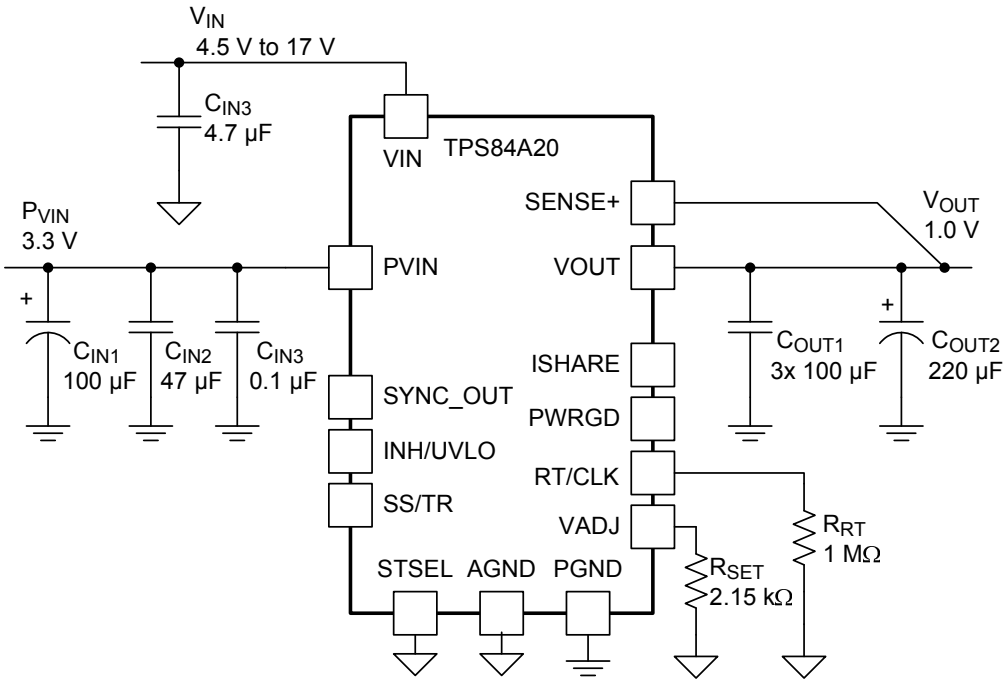


Figure 25. Typical Schematic
PVIN = 3.3 V, VIN = 4.5 V to 17 V, VOUT = 1.0 V

10.6 VIN and PVIN Input Voltage

The TPS84A20 allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN voltage supplies the internal control circuits of the device. The PVIN voltage provides the input voltage to the power converter system.

If tied together, the input voltage for the VIN pin and the PVIN pin can range from 4.5 V to 17 V. If you are using the VIN pin separately from the PVIN pin, the VIN pin must be greater than 4.5 V, and the PVIN pin can range from as low as 2.95 V to 17 V. When operating from a split rail, it is recommended to supply VIN from 5 V to 12 V, for best performance. A voltage divider connected to the INH/UVLO pin can adjust either input voltage UVLO appropriately. See the *Programmable Undervoltage Lockout (UVLO)* section for more information.

10.7 3.3 V PVIN Operation

Applications operating from a PVIN of 3.3 V must provide at least 4.5 V for VIN. It is recommended to supply VIN from 5 V to 12 V, for best performance. See the *Powering TPS84k Devices from 3.3 V Application Note* for help creating 5 V from 3.3 V using a small, simple charge pump device.

10.8 Power Good (PWRGD)

The PWRGD pin is an open-drain output. Once the voltage on the SENSE+ pin is between 95% and 104% of the set voltage, the PWRGD pin pulldown is released and the pin floats. The recommended pullup resistor value is between 10 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD pin is in a defined state once VIN is greater than 1.0 V, but with reduced current sinking capability. The PWRGD pin achieves full current sinking capability once the VIN pin is above 4.5 V. The PWRGD pin is pulled low when the voltage on SENSE+ is lower than 91% or greater than 108% of the nominal set voltage. Also, the PWRGD pin is pulled low if the input UVLO or thermal shutdown is asserted, the INH pin is pulled low, or the SS/TR pin is below 1.4 V.

10.9 Light Load Efficiency (LLE)

The TPS84A20 operates in pulse skip mode at light load currents to improve efficiency and decrease power dissipation by reducing switching and gate drive losses.

These pulses can cause the output voltage to rise when there is no load to discharge the energy. For output voltages < 1.5 V, a minimum load is required. The amount of required load can be determined by Equation 2. In most cases, the minimum current drawn by the load circuit will be enough to satisfy this load. Applications requiring a load resistor to meet the minimum load, the added power dissipation will be ≤ 3.6 mW. A single 0402 size resistor across VOUT and PGND can be used.

$$I_{MIN} = 600\ \mu A - \left(\frac{V_{OUT}}{1.43k + R_{SET}} \right) (A) \quad (2)$$

When V_{OUT} = 0.6 V and R_{SET} = OPEN, the minimum load current is 600 µA.

10.10 SYNC_OUT

The TPS84A20 provides a 180° out-of-phase clock signal for applications requiring synchronization. The SYNC_OUT pin produces a 50% duty cycle clock signal that is the same frequency as the switching frequency of the device, but is 180° out of phase. Operating two devices 180° out of phase reduces input and output voltage ripple. The SYNC_OUT clock signal is compatible with other TPS84K devices that have a CLK input.

10.11 Parallel Operation

Up to six TPS84A20 devices can be paralleled for increased output current. Multiple connections must be made between the paralleled devices and the component selection is slightly different than for a stand-alone TPS84A20 device. Figure 26 shows a typical TPS84A20 parallel schematic. Refer to the *TPS84A20 Parallel Operation Application Note* for information and design help when paralleling multiple TPS84A20 devices.

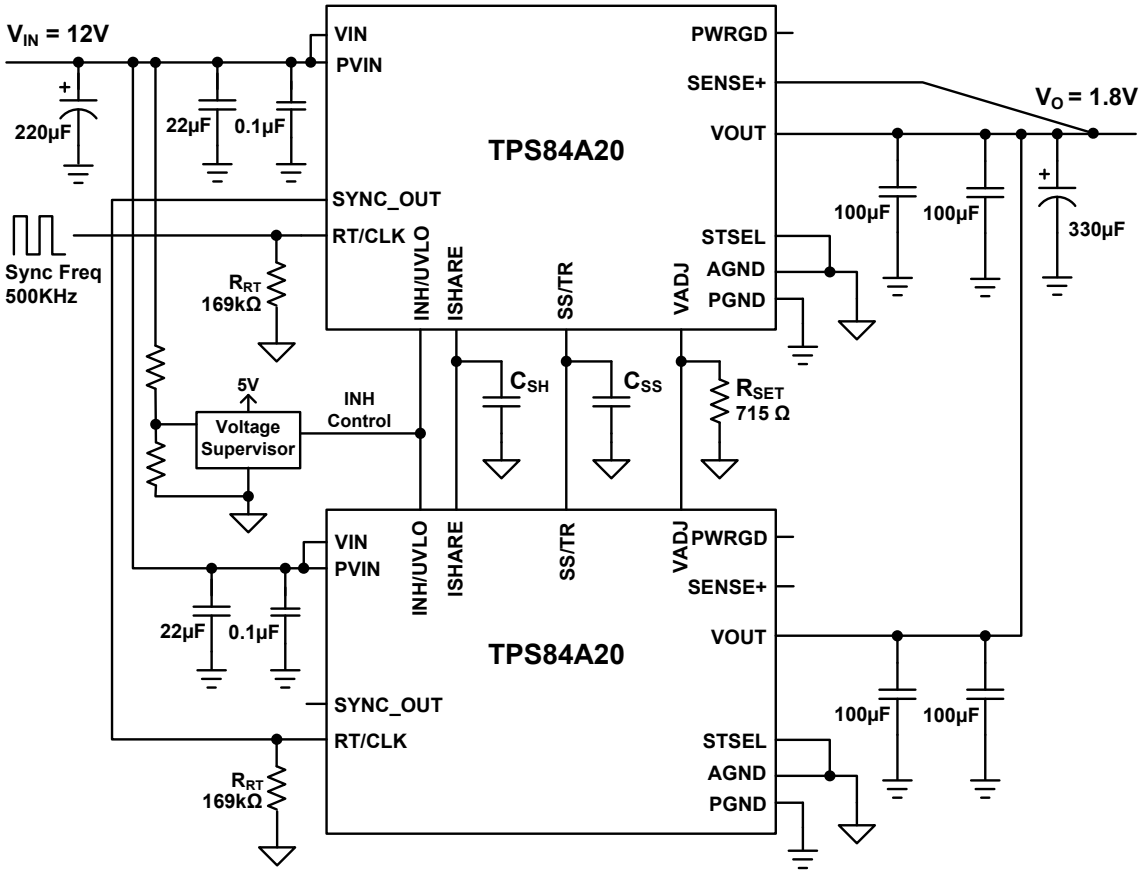


Figure 26. Typical TPS84A20 Parallel Schematic

10.12 Power-Up Characteristics

When configured as shown in the front page schematic, the TPS84A20 produces a regulated output voltage following the application of a valid input voltage. During the power-up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. Figure 27 shows the start-up waveforms for a TPS84A20, operating from a 5-V input (PVIN = VIN) and with the output voltage adjusted to 1.8 V. Figure 28 shows the start-up waveforms for a TPS84A20 starting up into a pre-biased output voltage. The waveforms were measured with a 5-A constant current load.

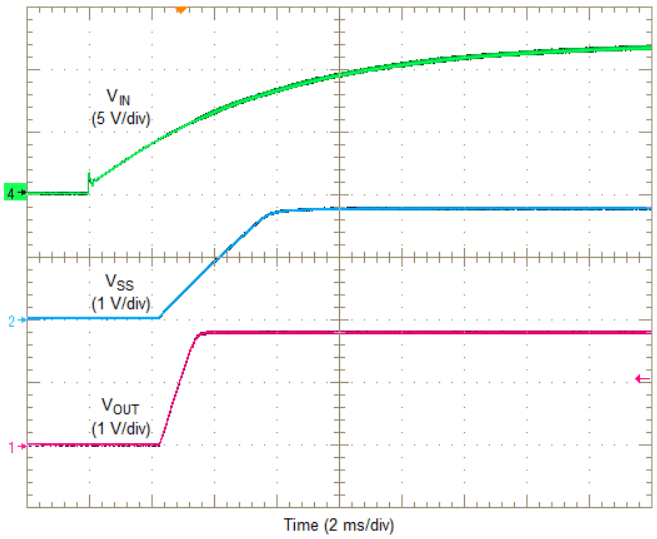


Figure 27. Start-Up Waveforms

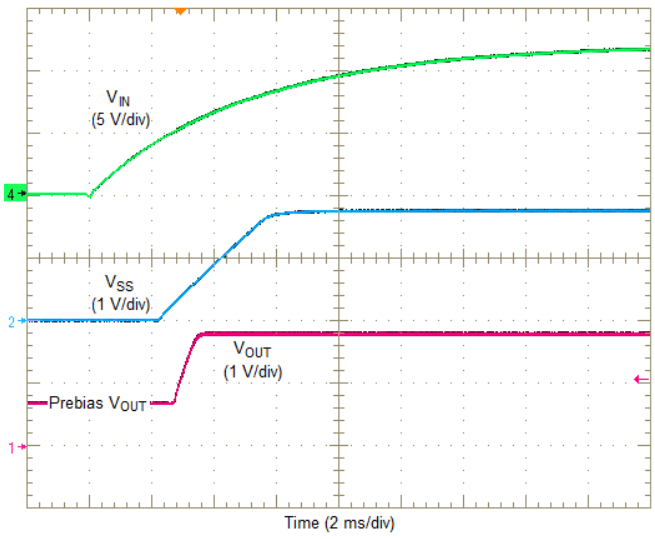


Figure 28. Start-up into Pre-bias

10.13 Pre-Biased Start-Up

The TPS84A20 has been designed to prevent the low-side MOSFET from discharging a pre-biased output. During pre-biased startup, the low-side MOSFET does not turn on until the high-side MOSFET has started switching. The high-side MOSFET does not start switching until the slow start voltage exceeds the voltage on the VADJ pin. Refer to Figure 28.

10.14 Remote Sense

The SENSE+ pin must be connected to V_{OUT} at the load, or at the device pins.

Connecting the SENSE+ pin to V_{OUT} at the load improves the load regulation performance of the device by allowing it to compensate for any I-R voltage drop between its output pins and the load. An I-R drop is caused by the high output current flowing through the small amount of pin and trace resistance. This should be limited to a maximum of 300 mV.

NOTE

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that can be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the SENSE+ connection, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

10.15 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 165°C typically.

10.16 Output On/Off Inhibit (INH)

The INH pin provides electrical on/off control of the device. Once the INH pin voltage exceeds the threshold voltage, the device starts operation. If the INH pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The INH pin has an internal pullup current source, allowing the user to float the INH pin for enabling the device. If an application requires controlling the INH pin, use an open drain/collector device, or a suitable logic gate to interface with the pin.

Figure 29 shows the typical application of the inhibit function. The Inhibit control has its own internal pullup to VIN potential. An open-collector or open-drain device is recommended to control this input.

Turning Q1 on applies a low voltage to the inhibit control (INH) pin and disables the output of the supply, shown in Figure 30. If Q1 is turned off, the supply executes a soft-start power-up sequence, as shown in Figure 31. A regulated output voltage is produced within 2 ms. The waveforms were measured with a 5-A constant current load.

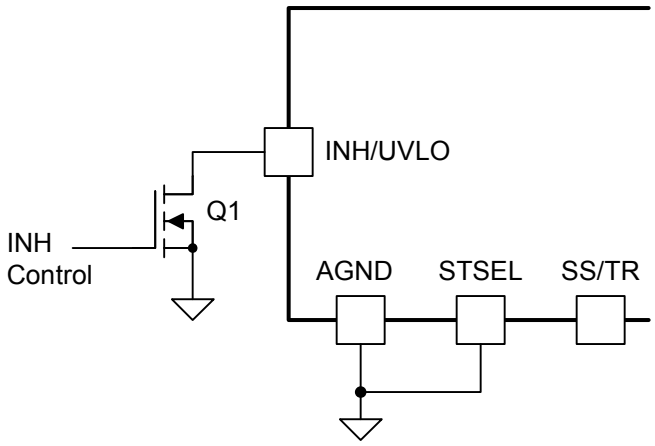


Figure 29. Typical Inhibit Control

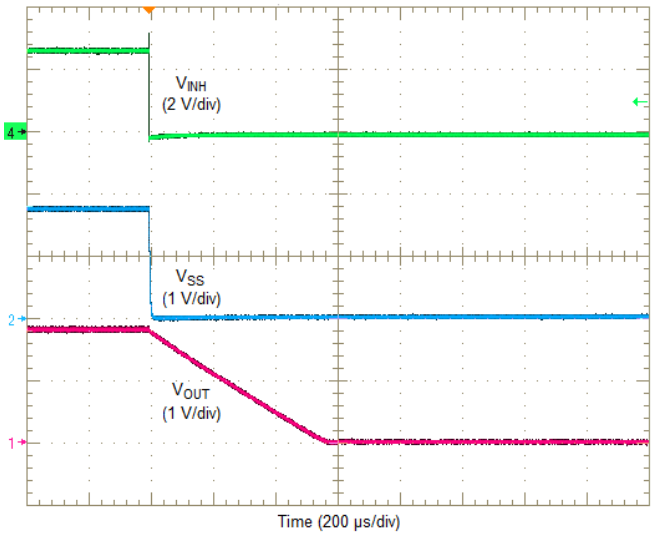


Figure 30. Inhibit Turn-Off

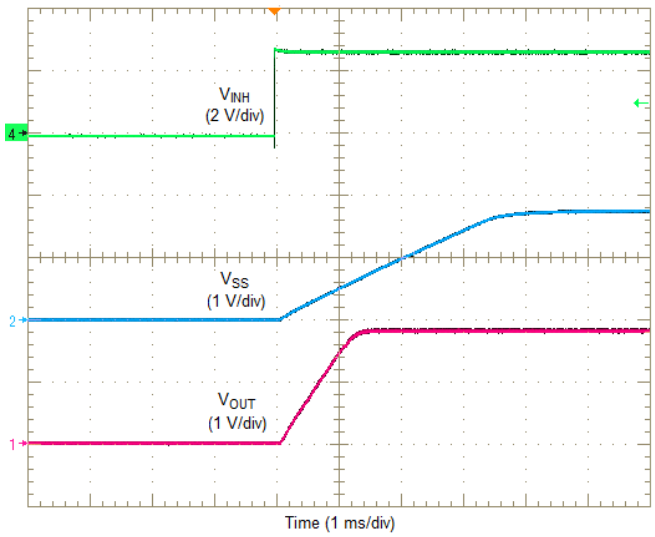


Figure 31. Inhibit Turn-On

10.17 Slow Start (SS/TR)

Connecting the STSEL pin to AGND and leaving SS/TR pin open enables the internal SS capacitor with a slow start interval of approximately 1.2 ms. Adding additional capacitance between the SS pin and AGND increases the slow start time. Increasing the slow start time reduces inrush current. Table 8 shows an additional SS capacitor connected to the SS/TR pin and the STSEL pin connected to AGND. See Table 8 for SS capacitor values and timing interval.

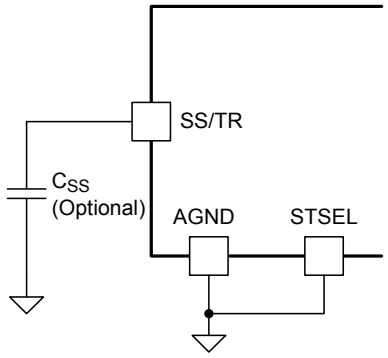


Figure 32. Slow-Start Capacitor (C_{SS}) and STSEL Connection

Table 8. Slow-Start Capacitor Values and Slow-Start Time

C_{SS} (nF)	OPEN	3.3	4.7	10	15	22	33
SS Time (msec)	1.2	2.1	2.5	3.8	5.1	7.0	9.8

10.18 Overcurrent Protection

For protection against load faults, the TPS84A20 incorporates output overcurrent protection. The overcurrent protection mode can be selected using the OCP_SEL pin. Leaving the OCP_SEL pin open selects hiccup mode and connecting it to AGND selects cycle-by-cycle mode. In hiccup mode, applying a load that exceeds the overcurrent threshold of the regulator causes the regulated output to shut down. Following shutdown, the module periodically attempts to recover by initiating a soft-start power-up as shown in Figure 33. This is described as a hiccup mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced which reduces power dissipation. Once the fault is removed, the module automatically recovers and returns to normal operation as shown in Figure 34.

In cycle-by-cycle mode, applying a load that exceeds the overcurrent threshold of the regulator limits the output current and reduces the output voltage as shown in Figure 35. During this period, the current flowing into the fault remains high causing the power dissipation to stay high as well. Once the overcurrent condition is removed, the output voltage returns to the set-point voltage as shown in Figure 36.

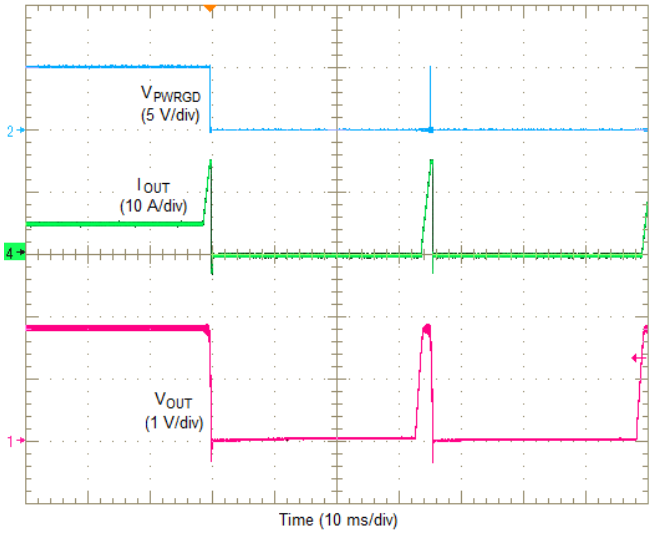


Figure 33. Overcurrent Limiting (Hiccup)

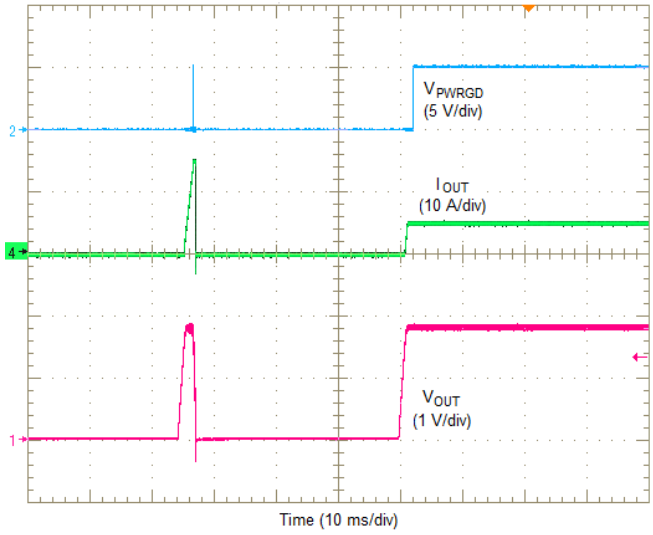


Figure 34. Removal of Overcurrent (Hiccup)

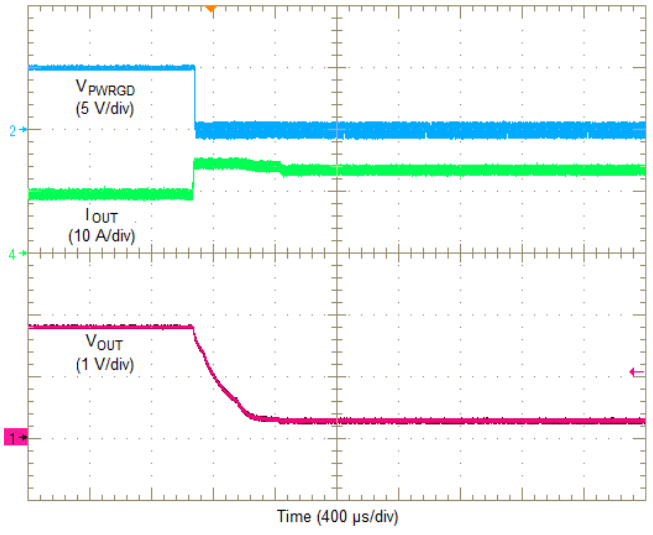


Figure 35. Overcurrent Limiting (Cycle-by-Cycle)

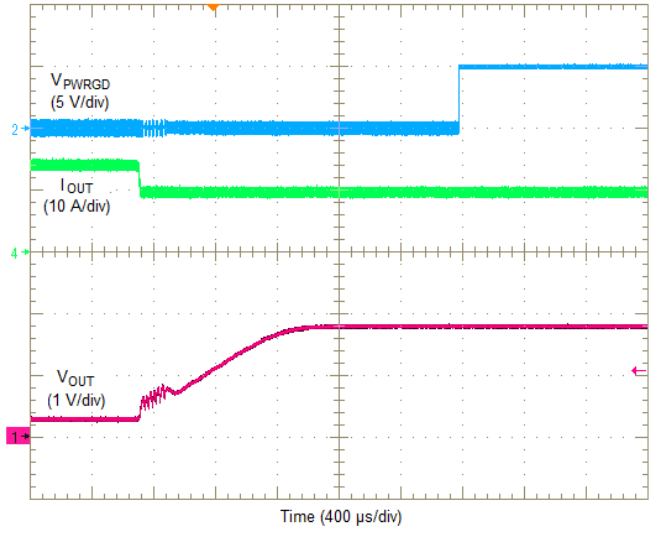


Figure 36. Removal of Overcurrent (Cycle-by-Cycle)

10.19 Synchronization (CLK)

An internal phase locked loop (PLL) has been implemented to allow synchronization between 200 kHz and 1200 kHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle between 20% to 80%. The clock signal amplitude must transition lower than 0.5 V and higher than 2.0 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. In applications where both RT mode and CLK mode are needed, the device can be configured as shown in Figure 37.

Before the external clock is present, the device works in RT mode and the switching frequency is set by RT resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the CLK pin is pulled above the RT/CLK high threshold (2.0 V), the device switches from RT mode to CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from CLK mode back to RT mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by the RT resistor (R_{RT}).

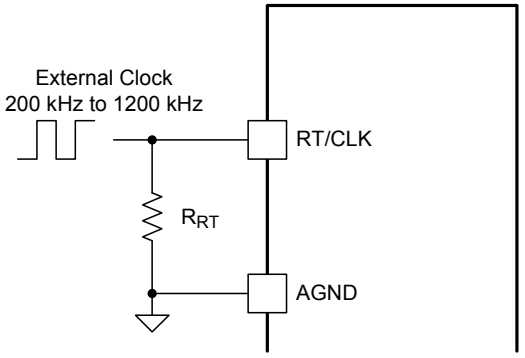


Figure 37. RT/CLK Configuration

The switching frequency must be selected based on the output voltages of the devices being synchronized. Table 9 shows the allowable frequencies for a given range of output voltages. The allowable switching frequency changes based on the maximum output current (I_{OUT}) of an application. The table shows the V_{OUT} range when I_{OUT} ≤ 10 A, 9 A, and 8 A. For the most efficient solution, always synchronize to the lowest allowable frequency. For example, an application requires synchronizing three TPS84A20 devices with output voltages of 1.0 V, 1.2 V and 1.8 V, all powered from PVIN = 12 V. Table 9 shows that all three output voltages should be synchronized to 300 kHz.

Table 9. Allowable Switching Frequency versus Output Voltage

SWITCHING FREQUENCY (kHz)	PVIN = 12 V			PVIN = 5 V		
	V_{OUT} RANGE (V)			V_{OUT} RANGE (V)		
	I_{OUT} ≤ 10 A	I_{OUT} ≤ 9 A	I_{OUT} ≤ 8 A	I_{OUT} ≤ 10 A	I_{OUT} ≤ 9 A	I_{OUT} ≤ 8 A
200	0.6 - 1.2	0.6 - 1.6	0.6 - 2.0	0.6 - 1.5	0.6 - 2.5	0.6 - 4.3
300	0.8 - 1.9	0.8 - 2.6	0.8 - 3.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
400	1.0 - 2.7	1.0 - 4.0	1.0 - 5.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
500	1.3 - 3.8	1.3 - 5.5	1.3 - 5.5	0.6 - 4.3	0.6 - 4.3	0.6 - 4.3
600	1.5 - 5.5	1.5 - 5.5	1.5 - 5.5	0.7 - 4.3	0.7 - 4.3	0.7 - 4.3
700	1.8 - 5.5	1.8 - 5.5	1.8 - 5.5	0.8 - 4.3	0.8 - 4.3	0.8 - 4.3
800	2.0 - 5.5	2.0 - 5.5	2.0 - 5.5	0.9 - 4.3	0.9 - 4.3	0.9 - 4.3
900	2.2 - 5.5	2.2 - 5.5	2.2 - 5.5	1.0 - 4.3	1.0 - 4.3	1.0 - 4.3
1000	2.5 - 5.5	2.5 - 5.5	2.5 - 5.5	1.1 - 4.3	1.1 - 4.3	1.1 - 4.3
1100	2.7 - 5.5	2.7 - 5.5	2.7 - 5.5	1.3 - 4.3	1.2 - 4.3	1.2 - 4.3
1200	3.0 - 5.5	3.0 - 5.5	3.0 - 5.5	1.4 - 4.3	1.3 - 4.3	1.3 - 4.3

10.20 Sequencing (SS/TR)

Many of the common power supply sequencing methods can be implemented using the SS/TR, INH and PWRGD pins. The sequential method is illustrated in Figure 38 using two TPS84A20 devices. The PWRGD pin of the first device is coupled to the INH pin of the second device which enables the second power supply once the primary supply reaches regulation. Figure 39 shows sequential turnon waveforms of two TPS84A20 devices.

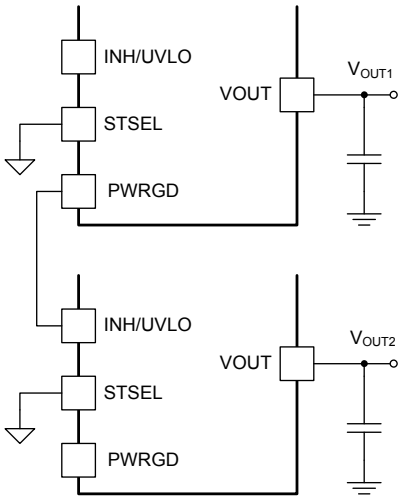


Figure 38. Sequencing Schematic

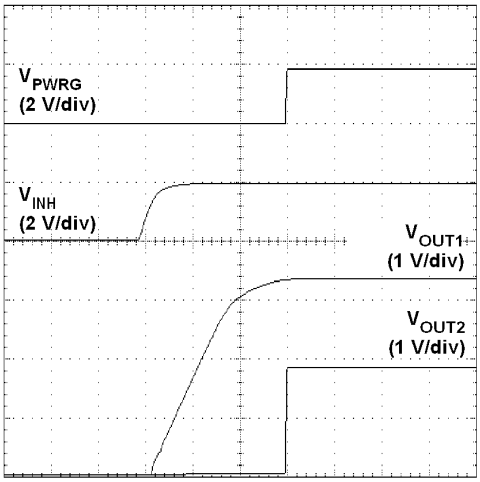


Figure 39. Sequencing Waveforms

Simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 40 to the output of the power supply that needs to be tracked or to another voltage reference source. The tracking voltage must exceed 750 mV before V_{OUT2} reaches its set-point voltage.Figure 41 shows simultaneous turnon waveforms of two TPS84A20 devices. Use Equation 3 and Equation 4 to calculate the values of R1 and R2.

$$R1 = \frac{(V_{OUT2} \times 12.6)}{0.6} \ (k\Omega) \quad (3)$$

$$R2 = \frac{0.6 \times R1}{(V_{OUT2} - 0.6)} \ (k\Omega) \quad (4)$$

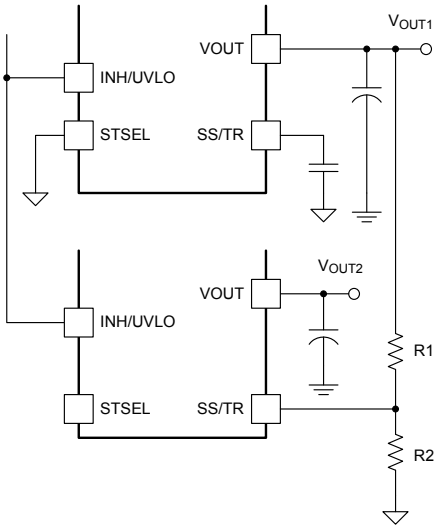


Figure 40. Simultaneous Tracking Schematic

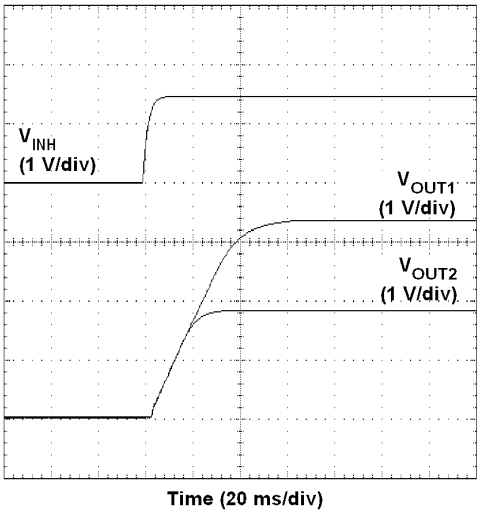


Figure 41. Simultaneous Tracking Waveforms

10.21 Programmable Undervoltage Lockout (UVLO)

The TPS84A20 implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 4.5 V(max) with a typical hysteresis of 150 mV.

If an application requires either a higher UVLO threshold on the VIN pin or a higher UVLO threshold for a combined VIN and PVIN, then the UVLO pin can be configured as shown in Figure 42 or Figure 43. Table 10 lists standard values for R_{UVLO1} and R_{UVLO2} to adjust the VIN UVLO voltage up.

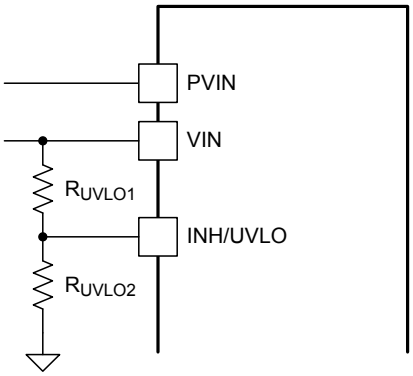


Figure 42. Adjustable VIN UVLO

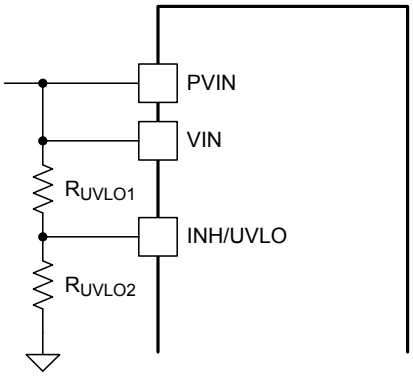


Figure 43. Adjustable VIN and PVIN Undervoltage Lockout

Table 10. Standard Resistor values for Adjusting VIN UVLO

VIN UVLO (V)	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10.0
R_{UVLO1} (kΩ)	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1	68.1
R_{UVLO2} (kΩ)	21.5	18.7	16.9	15.4	14.0	13.0	12.1	11.3	10.5	9.76	9.31
Hysteresis (mV)	400	415	430	450	465	480	500	515	530	550	565

For a split rail application, if a secondary UVLO on PVIN is required, VIN must be ≥ 4.5 V. Figure 44 shows the PVIN UVLO configuration. Use Table 11 to select R_{UVLO1} and R_{UVLO2} for PVIN. If PVIN UVLO is set for less than 3.0 V, a 5.1-V zener diode should be added to clamp the voltage on the UVLO pin below 6 V.

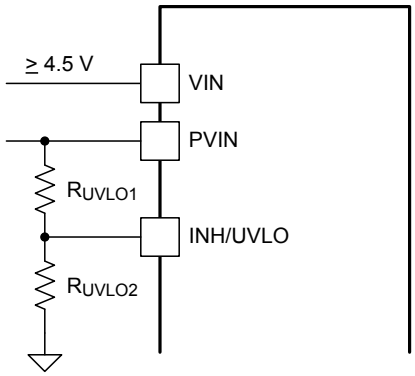


Figure 44. Adjustable PVIN Undervoltage Lockout, (VIN ≥4.5 V)

Table 11. Standard Resistor Values for Adjusting PVIN UVLO, (VIN ≥4.5 V)

PVIN UVLO (V)	2.9	3.0	3.5	4.0	4.5	
R_{UVLO1} (kΩ)	68.1	68.1	68.1	68.1	68.1	For higher PVIN UVLO voltages, see Table 10 for resistor values.
R_{UVLO2} (kΩ)	47.5	44.2	34.8	28.7	24.3	
Hysteresis (mV)	330	335	350	365	385	

10.22 Layout Considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 45 through Figure 48, shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (PVIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Keep AGND and PGND separate from one another.
- Place R_{SET}, R_{RT}, and C_{SS} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

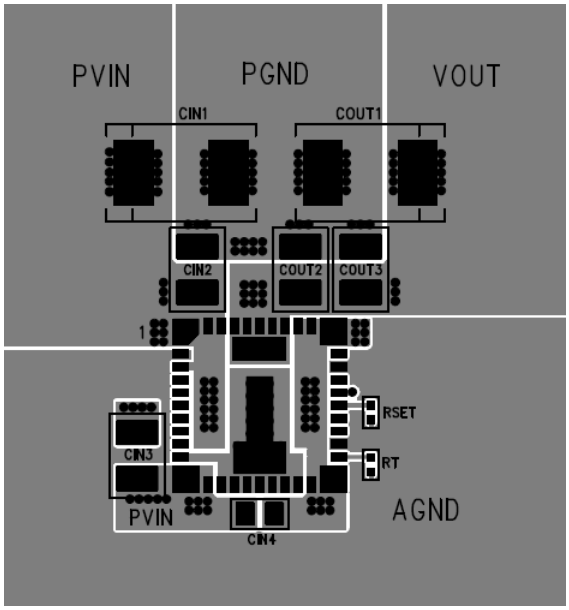


Figure 45. Typical Top-Layer Layout

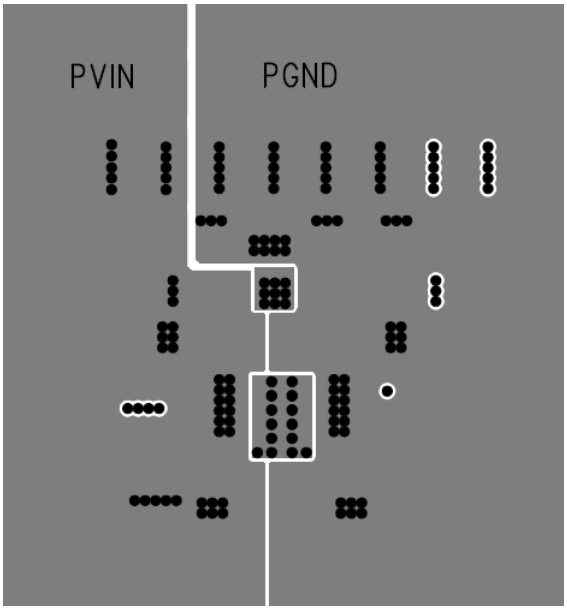


Figure 46. Typical Layer-2 Layout

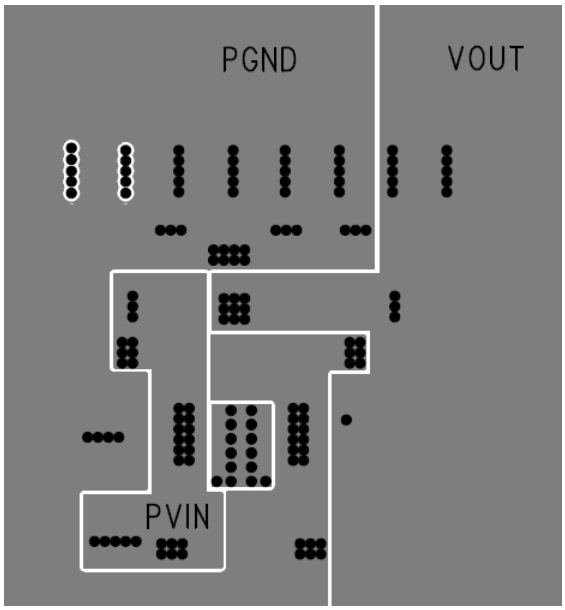


Figure 47. Typical Layer 3 Layout

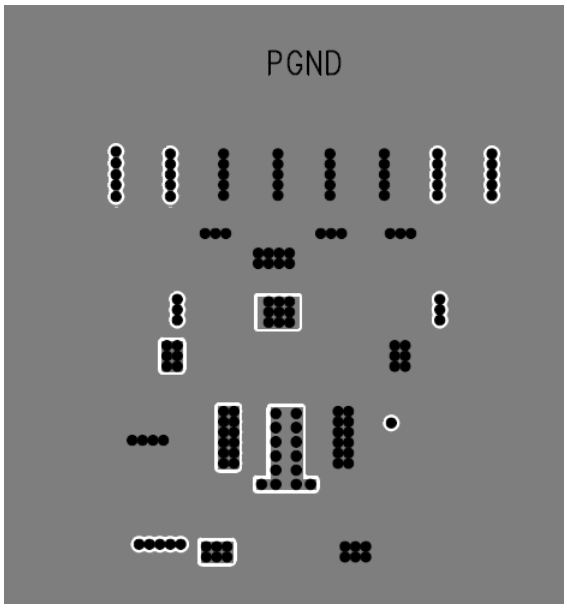


Figure 48. Typical Bottom-Layer Layout

10.23 EMI

The TPS84A20 is compliant with EN55022 Class B radiated emissions. Figure 49 and Figure 50 show typical examples of radiated emissions plots for the TPS84A20 operating from 5V and 12V respectively. Both graphs include the plots of the antenna in the horizontal and vertical positions.

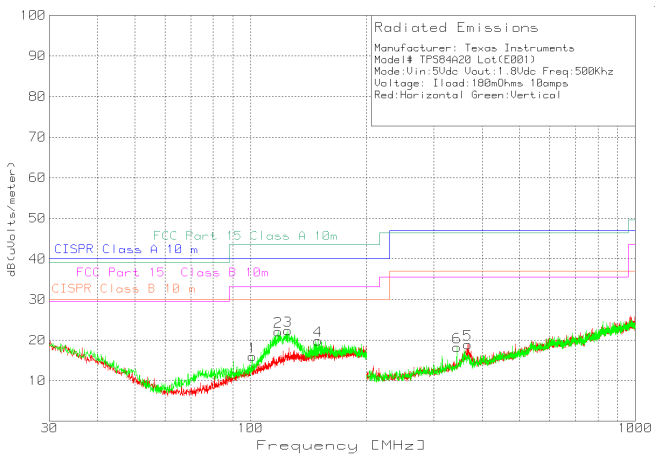


Figure 49. Radiated Emissions 5-V Input, 1.8-V Output, 10-A Load (EN55022 Class B)

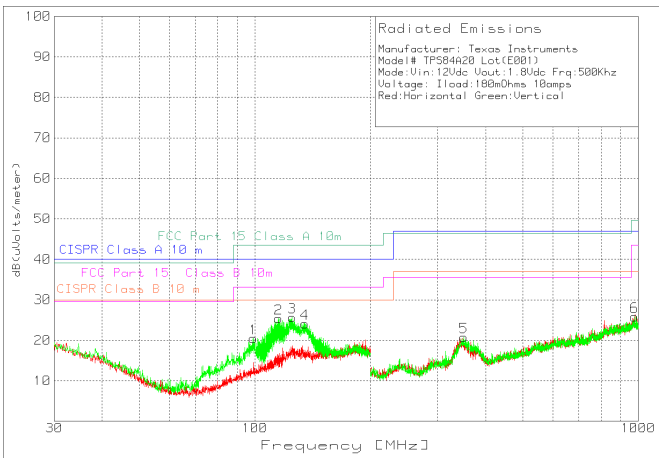


Figure 50. Radiated Emissions 12-V Input, 1.8-V Output, 10-A Load (EN55022 Class B)

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 商标

Eco-mode, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

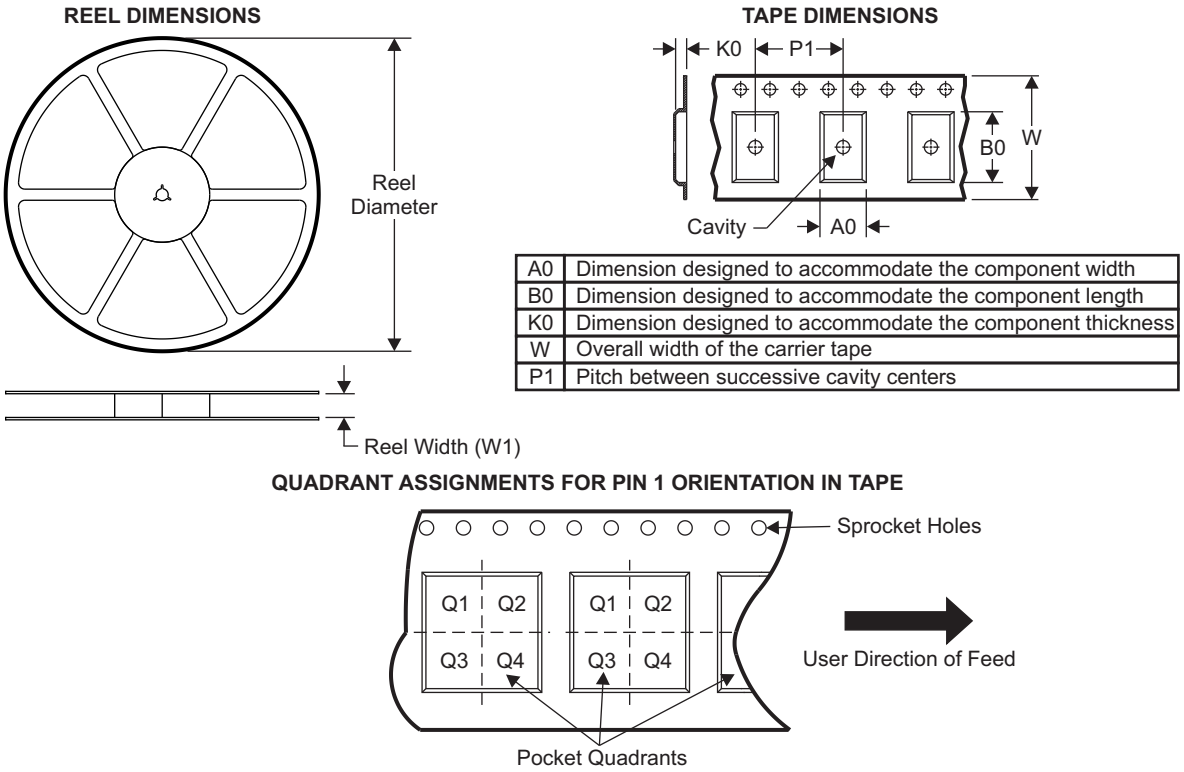
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

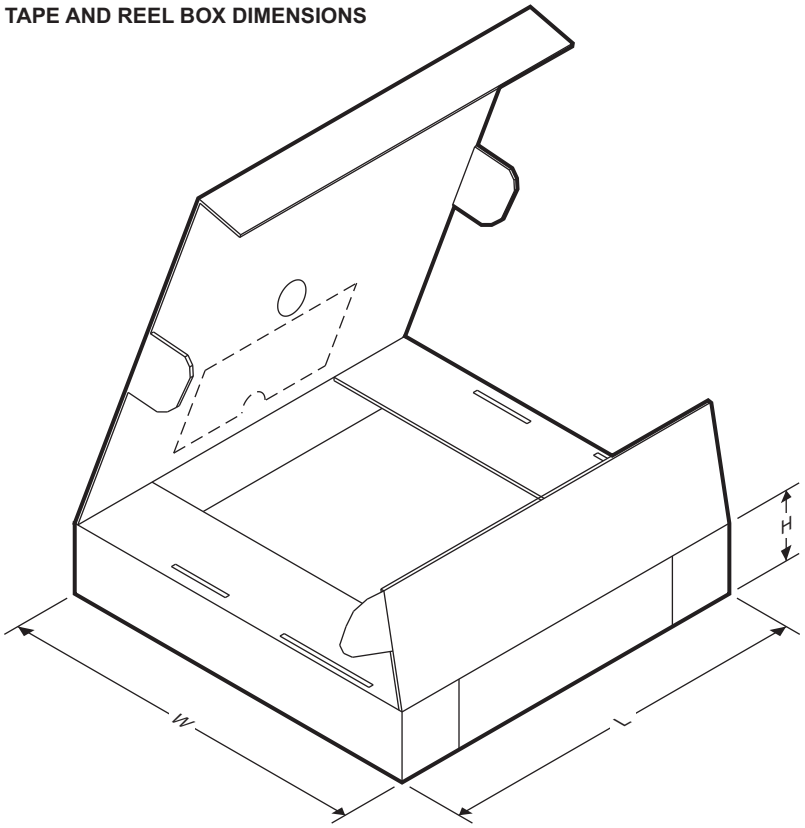
12.1 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS84A20RVQR	B3QFN	RVQ	42	500	330.0	24.4	10.35	10.35	4.6	16.0	24.0	Q2
TPS84A20RVQT	B3QFN	RVQ	42	250	330.0	24.4	10.35	10.35	4.6	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS84A20RVQR	B3QFN	RVQ	42	500	383.0	353.0	58.0
TPS84A20RVQT	B3QFN	RVQ	42	250	383.0	353.0	58.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS84A20RVQR	ACTIVE	B3QFN	RVQ	42	500	RoHS Exempt & Green	NIPDAU	Level-3-245C-168 HR	-40 to 85	(54020, TPS84A20)	Samples
TPS84A20RVQT	ACTIVE	B3QFN	RVQ	42	250	RoHS Exempt & Green	NIPDAU	Level-3-245C-168 HR	-40 to 85	(54020, TPS84A20)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

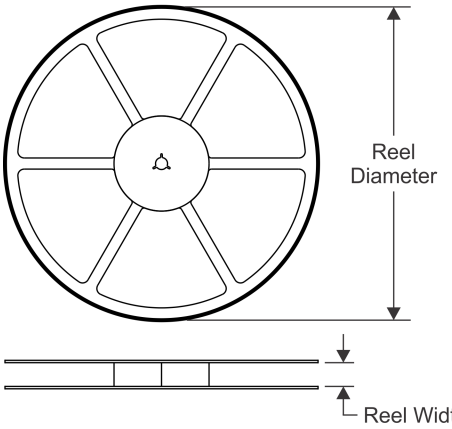
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

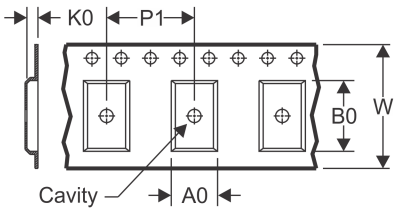
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

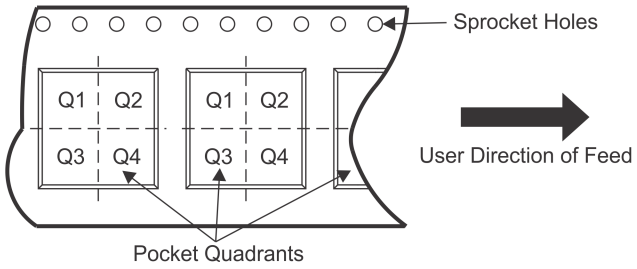


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

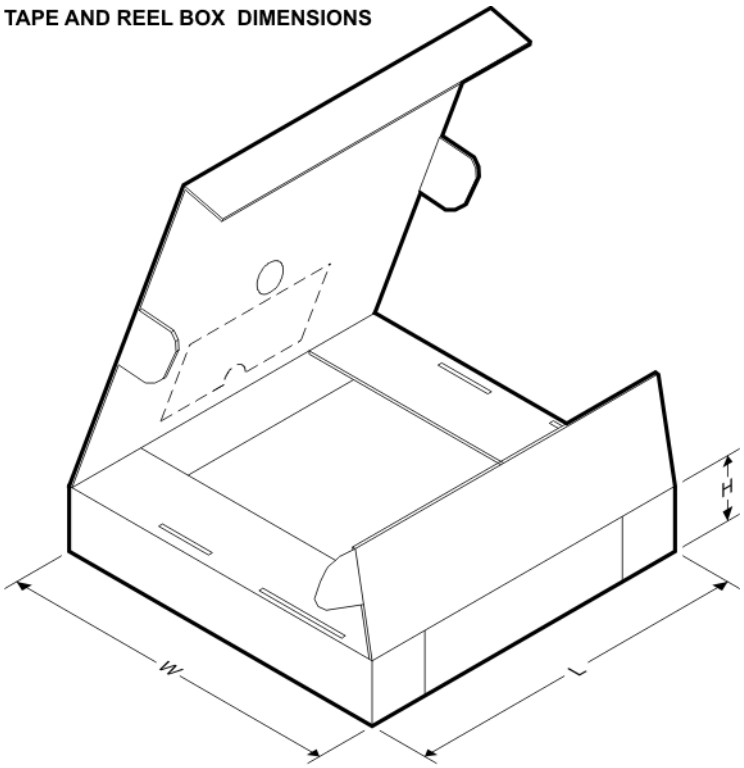
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS84A20RVQR	B3QFN	RVQ	42	500	330.0	24.4	10.35	10.35	4.6	16.0	24.0	Q2
TPS84A20RVQT	B3QFN	RVQ	42	250	330.0	24.4	10.35	10.35	4.6	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

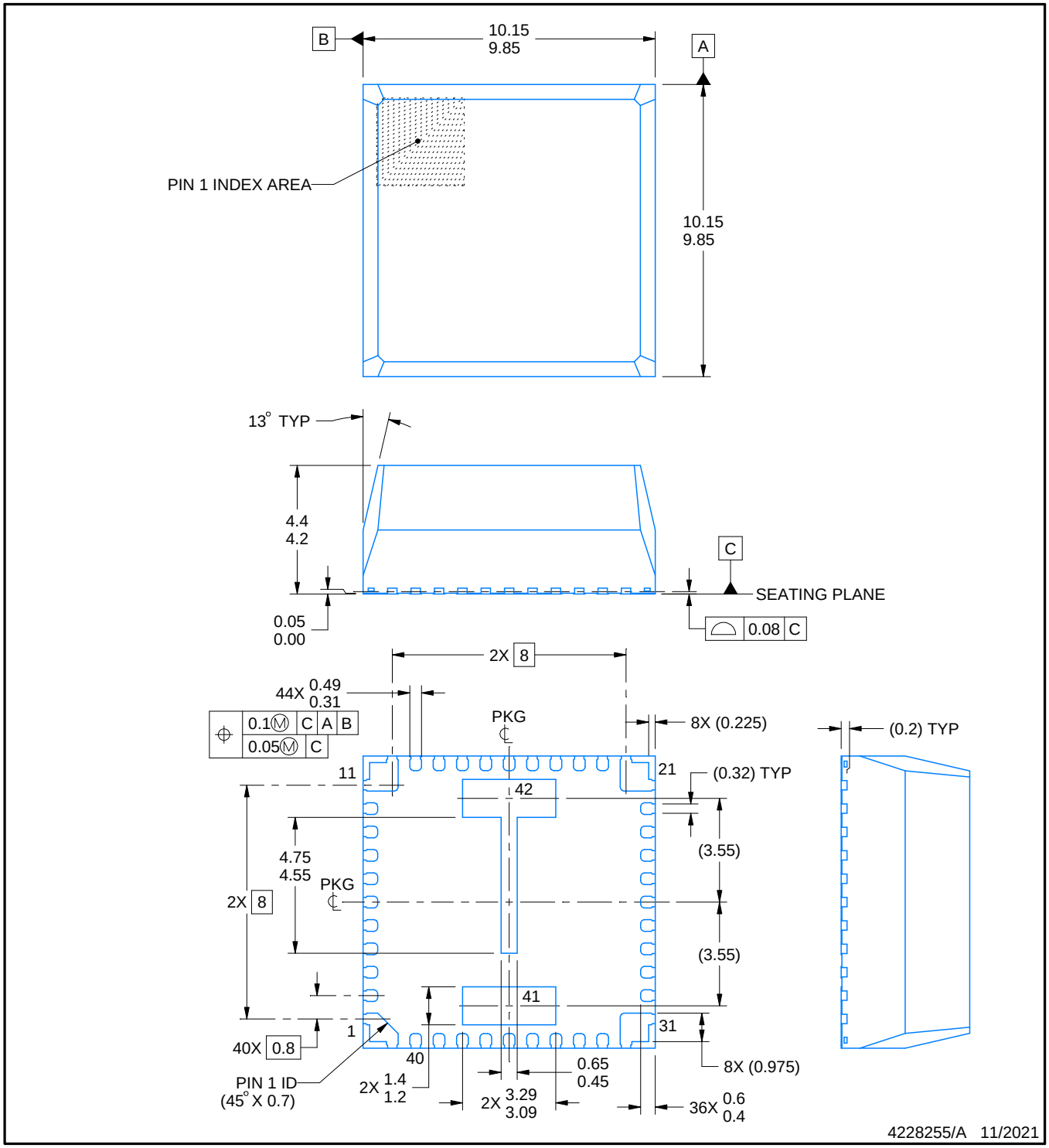
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS84A20RVQR	B3QFN	RVQ	42	500	383.0	353.0	58.0
TPS84A20RVQT	B3QFN	RVQ	42	250	383.0	353.0	58.0

PACKAGE OUTLINE

RVQ0042A

B3QFN - 4.4 mm max height

SUPER THICK QUAD FLATPACK - NO LEAD



NOTES:

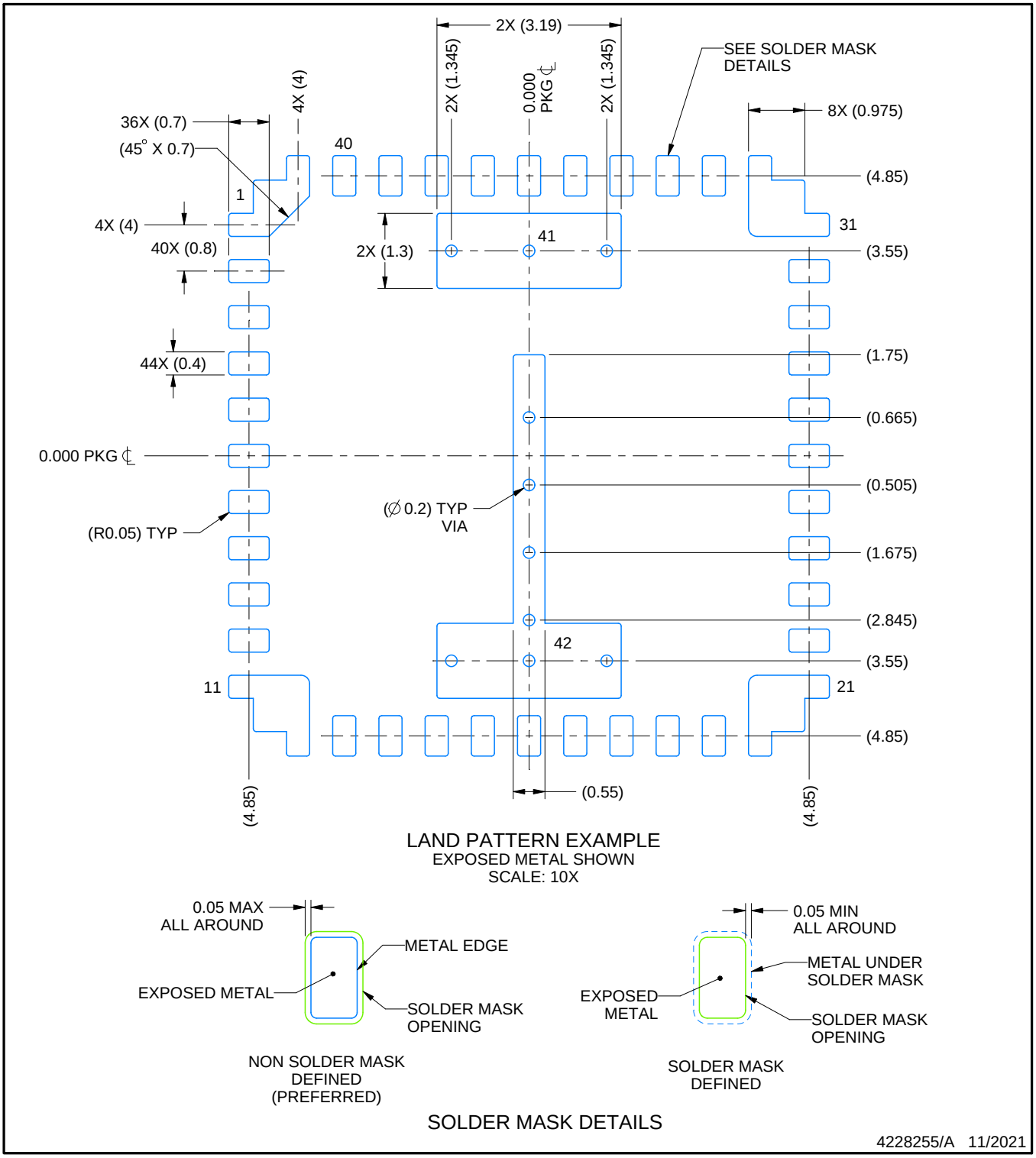
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RVQ0042A

B3QFN - 4.4 mm max height

SUPER THICK QUAD FLATPACK - NO LEAD



NOTES: (continued)

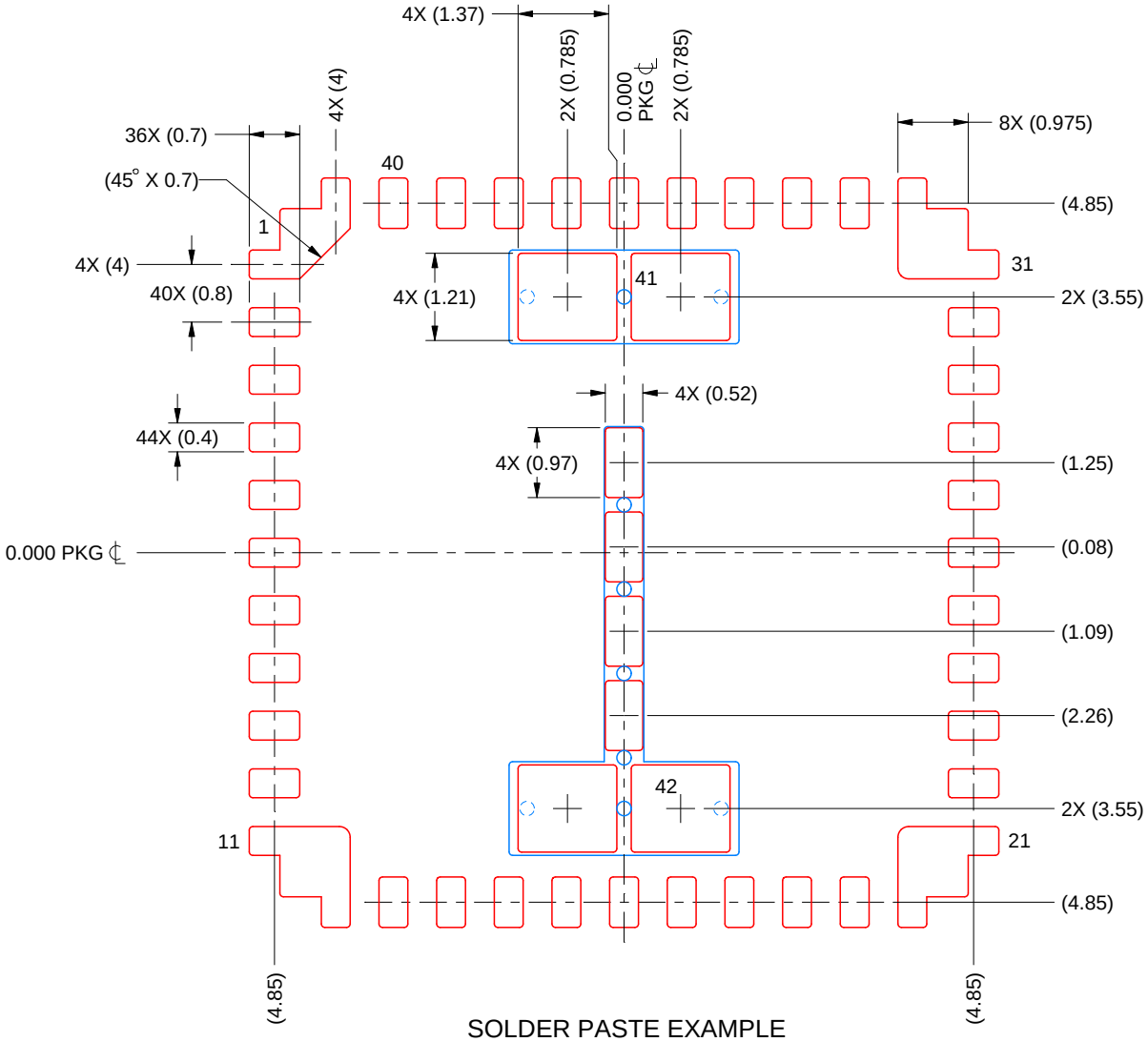
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RVQ0042A

B3QFN - 4.4 mm max height

SUPER THICK QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm STENCIL THICKNESS
SCALE: 10X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 41: 81%
PAD 42: 80%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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