Simultaneous Sampling Dual 175 kSPS 14-Bit ADC

AD7863

FEATURES

Two fast 14-bit ADCs
Four input channels
Simultaneous sampling and conversion
5.2 µs conversion time
Single supply operation
Selection of input ranges
- **±10 V for AD7863-10**
- **±2.5 V for AD7863-3**
- **0 V to 2.5 V for AD7863-2**

High speed parallel interface
Low power, 70 mW typical
Power saving mode, 105 µW maximum
Overvoltage protection on analog inputs
14-bit lead compatible upgrade to AD7862

GENERAL DESCRIPTION

The AD7863 is a high speed, low power, dual 14-bit analog-to-digital converter that operates from a single 5 V supply.

The part contains two 5.2 µs successive approximation ADCs, two track/hold amplifiers, an internal 2.5 V reference and a high speed parallel interface. Four analog inputs are grouped into two channels (A and B) selected by the A0 input. Each channel has two inputs (V_{A1} and V_{A2} or V_{B1} and V_{B2}) that can be sampled and converted simultaneously, thus preserving the relative phase information of the signals on both analog inputs. The part accepts an analog input range of ±10 V (AD7863-10), ±2.5 V (AD7863-3), and 0 V to 2.5 V (AD7863-2). Overvoltage protection on the analog inputs for the part allows the input voltage to go to ±17 V, ±7 V, or +7 V respectively, without causing damage.

A single conversion start signal ($\overline{CONVST}$) simultaneously places both track/holds into hold and initiates conversion on both channels. The BUSY signal indicates the end of conversion and at this time the conversion results for both channels are available to be read. The first read after a conversion accesses the result from V_{A1} or V_{B1}, and the second read accesses the result from V_{A2} or V_{B2}, depending on whether the multiplexer select (A0) is low or high, respectively. Data is read from the part via a 14-bit parallel data bus with standard $\overline{CS}$ and $\overline{RD}$ signals. In addition to the traditional dc accuracy specifications such as linearity, gain, and offset errors, the part is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7863 is fabricated in the Analog Devices, Inc. linear compatible CMOS (LC^{2}MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. It is available in 28-lead SOIC_W and SSOP.

FUNCTIONAL BLOCK DIAGRAM

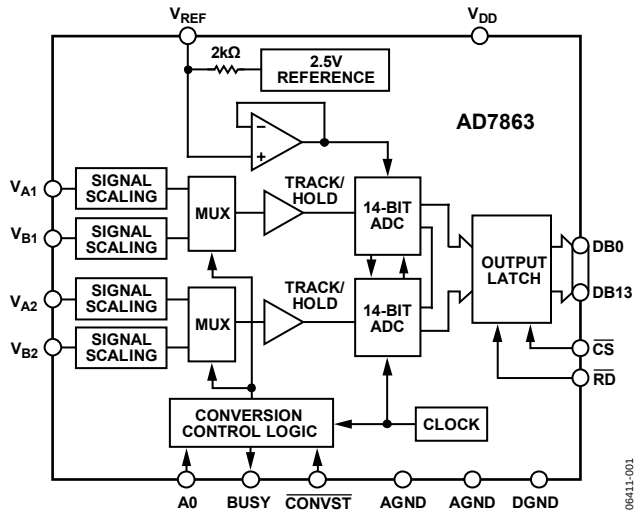

Figure 1.

PRODUCT HIGHLIGHTS

1. The AD7863 features two complete ADC functions allowing simultaneous sampling and conversion of two channels. Each ADC has a two-channel input mux. The conversion result for both channels is available 5.2 µs after initiating conversion.
2. The AD7863 operates from a single 5 V supply and consumes 70 mW typical. The automatic power-down mode, where the part goes into power-down once conversion is complete and wakes up before the next conversion cycle, makes the AD7863 ideal for battery-powered or portable applications.
3. The part offers a high speed parallel interface for easy connection to microprocessors, microcontrollers, and digital signal processors.
4. The part is offered in three versions with different analog input ranges. The AD7863-10 offers the standard industrial input range of ±10 V; the AD7863-3 offers the common signal processing input range of ±2.5 V, while the AD7863-2 can be used in unipolar 0 V to 2.5 V applications.
5. The part features very tight aperture delay matching between the two input sample and hold amplifiers.

Rev. B
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REVISION HISTORY

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SPECIFICATIONS

V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, REF = Internal. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	A Version[1]	B Version[1]	Unit	Test Conditions/Comments
SAMPLE AND HOLD				
−3 dB Small Signal Bandwidth	7	7	MHz typ	
Aperture Delay[2]	35	35	ns max	
Aperture Jitter[2]	50	50	ps typ	
Aperture Delay Matching[2]	350	350	ps max	
DYNAMIC PERFORMANCE[3]				f_{IN} = 80.0 kHz, f_S = 175 kSPS
Signal-to-(Noise + Distortion) Ratio[4]				
@ 25°C	78	78	dB min	
T_{MIN} to T_{MAX}	77	77	dB min	
Total Harmonic Distortion[4]	−82	−82	dB max	−87 dB typ
Peak Harmonic or Spurious Noise[4]	−82	−82	dB max	−90 dB typ
Intermodulation Distortion[4]				fa = 49 kHz, fb = 50 kHz
Second Order Terms	−93	−93	dB typ	
Third Order Terms	−89	−89	dB typ	
Channel-to-Channel Isolation[4]	−86	−86	dB typ	f_{IN} = 50 kHz sine wave
DC ACCURACY				Any channel
Resolution	14	14	Bits	
Minimum Resolution for Which No Missing Codes are Guaranteed	14	14	Bits	
Relative Accuracy[4]	±2.5	±2	LSB max	
Differential Nonlinearity[4]	+2 to −1	+2 to −1	LSB max	
AD7863-10, AD7863-3				
Positive Gain Error[4]	±10	±8	LSB max	
Positive Gain Error Match[4]	10	10	LSB max	
Negative Gain Error[4]	±10	±8	LSB max	
Negative Gain Error Match[4]	10	10	LSB max	
Bipolar Zero Error	±10	±8	LSB max	
Bipolar Zero Error Match	8	6	LSB max	
AD7863-2				
Positive Gain Error[4]	±14		LSB max	
Positive Gain Error Match[4]	16		LSB max	
Unipolar Offset Error	±14		LSB max	
Unipolar Offset Error Match	10		LSB max	
ANALOG INPUTS				
AD7863-10				
Input Voltage Range	±10	±10	V	
Input Resistance	9	9	kΩ typ	
AD7863-3				
Input Voltage Range	±2.5	±2.5	V	
Input Resistance	3	3	kΩ typ	
AD7863-2				
Input Voltage Range	2.5	2.5	V	
Input Current	100	100	nA max	

Parameter	A Version[1]	B Version[1]	Unit	Test Conditions/Comments
REFERENCE INPUT/OUTPUT				
REF IN Input Voltage Range	2.375 to 2.625	2.375 to 2.625	V	2.5 V ± 5%
REF IN Input Current	±100	±100	µA max	
REF OUT Output Voltage	2.5	2.5	V nom	
REF OUT Error @ 25°C	±10	±10	mV max	
REF OUT Error T_{MIN} to T_{MAX}	±20	±20	mV max	
REF OUT Temperature Coefficient	25	25	ppm/°C typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	
Input Capacitance, C_{IN}[5]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	4.0	4.0	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11 to DB0				
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Capacitance[5]	10	10	pF max	
Output Coding				
AD7863-10, AD7863-3				Twos complement
AD7863-2				Straight (natural) binary
CONVERSION RATE				
Conversion Time				
Mode 1 Operation	5.2	5.2	µs max	For both channels
Mode 2 Operation[6]	10.0	10.0	µs max	For both channels
Track/Hold Acquisition Time[4, 7]	0.5	0.5	µs max	
POWER REQUIREMENTS				
V_{DD}	5	5	V nom	±5% for specified performance
I_{DD}				
Normal Mode (Mode 1)				
AD7863-10	18	18	mA max	
AD7863-3	16	16	mA max	
AD7863-2	11	11	mA max	
Power-Down Mode (Mode 2)				
I_{DD} @ 25°C[8]	20	20	µA max	40 nA typ. Logic inputs = 0 V or V_{DD}
Power Dissipation				
Normal Mode (Mode 1)				
AD7863-10	94.50	94.50	mW max	V_{DD} = 5.25 V, 70 mW typ
AD7863-3	84	84	mW max	V_{DD} = 5.25 V, 70 mW typ
AD7863-2	57.75	57.75	mW max	V_{DD} = 5.25 V, 45 mW typ
Power-Down Mode @ 25°C	105	105	µW max	210 nW typ, V_{DD} = 5.25 V

[1] Temperature ranges are as follows: A Version and B Version, –40°C to +85°C.
[2] Sample tested during initial release.
[3] Applies to Mode 1 operation. See Operating Modes section.
[4] See Terminology section.
[5] Sample tested @ 25°C to ensure compliance.
[6] This 10 µs includes the wake-up time from standby. This wake-up time is timed from the rising edge of $\overline{CONVST}$, whereas conversion is timed from the falling edge of $\overline{CONVST}$, for a narrow $\overline{CONVST}$ pulse width the conversion time is effectively the wake-up time plus conversion time, 10 µs. This can be seen from Figure 6. Note that if the $\overline{CONVST}$ pulse width is greater than 5.2 µs, the effective conversion time increases beyond 10 µs.
[7] Performance measured through full channel (multiplexer, SHA, and ADC).
[8] For best dynamic performance of the AD7863, ATE device testing has to be performed with power supply decoupling in place. In the AD7863 power-down mode of operation, the leakage current associated with these decoupling capacitors is greater than that of the AD7863 supply current. Therefore, the 40 nA typical figure shown is characterized and guaranteed by design figure, which reflects the supply current of the AD7863 without decoupling in place. The maximum figure shown in the Conditions/Comments column reflects the AD7863 with supply decoupling in place—0.1 µF in parallel with 10 µF disc ceramic capacitors on the V_{DD} pin and 2 × 0.1 µF disc ceramic capacitors on the V_{REF} pin, in both cases to the AGND plane.

TIMING CHARACTERISTICS

V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, REF = Internal. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1, 2]	A, B Versions	Unit	Test Conditions/Comments
t_{CONV}	5.2	µs max	Conversion time
t_{ACQ}	0.5	µs max	Acquisition time
Parallel Interface			
t_1	0	ns min	$\overline{CS}$ to $\overline{RD}$ setup time
t_2	0	ns min	$\overline{CS}$ to $\overline{RD}$ hold time
t_3	35	ns min	$\overline{CONVST}$ pulse width
t_4	45	ns min	$\overline{RD}$ pulse width
t_5[3]	30	ns min	Data access time after falling edge of $\overline{RD}$
t_6[4]	5	ns min	Bus relinquish time after rising edge of $\overline{RD}$
	30	ns max	
t_7	10	ns min	Time between consecutive reads
t_8	400	ns min	Quiet time

[1] Sample tested at 25°C to ensure compliance. All input signals are measured with tr = tf = 1 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2] See Figure 2.
[3] Measured with the load circuit of Figure 3 and defined as the time required for an output to cross 0.8 V or 2.0 V.
[4] These times are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

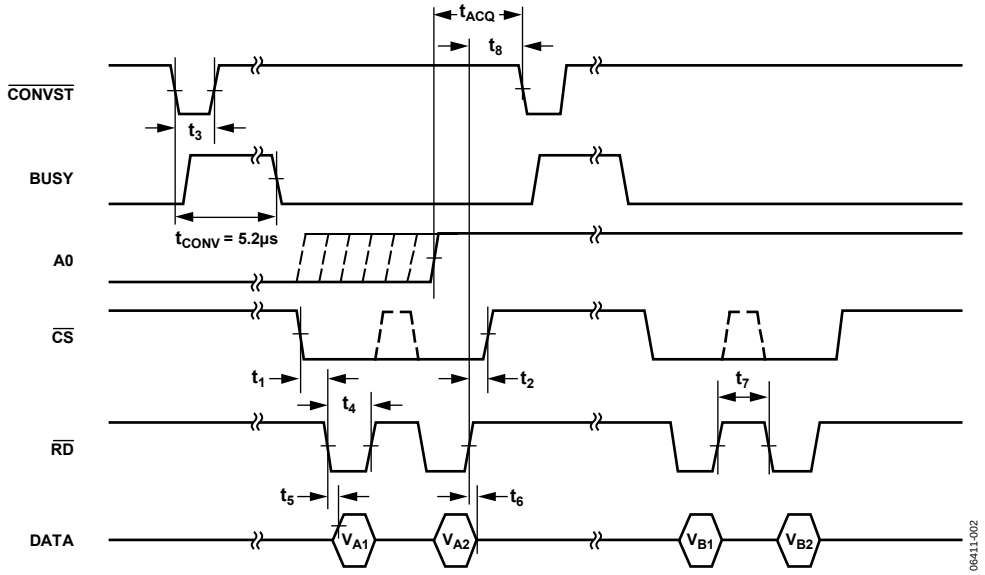


Figure 2. Timing Diagram

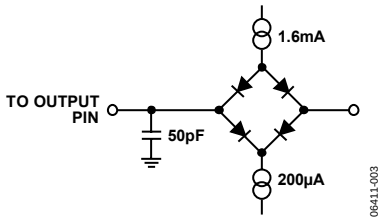


Figure 3. Load Circuit for Access Time and Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Ratings
V_{DD} to AGND	−0.3 V to +7 V
V_{DD} to DGND	−0.3 V to +7 V
Analog Input Voltage to AGND	
AD7863-10	±17 V
AD7863-3	±7 V
AD7863-2	7 V
Reference Input Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Commercial (A Version and B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SOIC Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	71.40°C/W
θ_{JC} Thermal Impedance	23.0°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
SSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	109°C/W
θ_{JC} Thermal Impedance	39.0°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

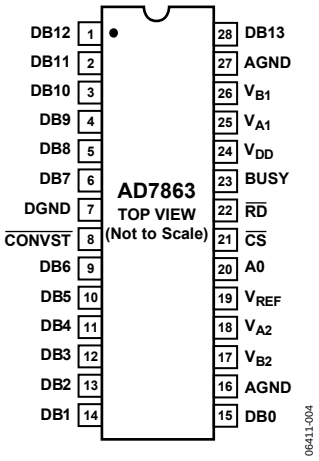


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 6	DB12 to DB7	Data Bit 12 to Data Bit 7. Three-state TTL outputs.
7	DGND	Digital Ground. Ground reference for digital circuitry.
8	$\overline{\text{CONVST}}$	Convert Start Input. Logic input. A high-to-low transition on this input puts both track/holds into their hold mode and starts conversion on both channels.
9 to 15	DB6 to DB0	Data Bit 6 to Data Bit 0. Three-state TTL outputs.
16	AGND	Analog Ground. Ground reference for mux, track/hold, reference, and DAC circuitry.
17	V_{B2}	Input Number 2 of Channel B. Analog input voltage ranges of ±10 V (AD7863-10), ±2.5 V (AD7863-3), and 0 V to 2.5 V (AD7863-2).
18	V_{A2}	Input Number 2 of Channel A. Analog input voltage ranges of ±10 V (AD7863-10), ±2.5 V (AD7863-3), and 0 V to 2.5 V (AD7863-2).
19	V_{REF}	Reference Input/Output. This pin is connected to the internal reference through a series resistor and is the output reference source for the analog-to-digital converter. The nominal reference voltage is 2.5 V, and this appears at the pin.
20	A0	Multiplexer Select. This input is used in conjunction with $\overline{\text{CONVST}}$ to determine on which pair of channels the conversion is to be performed. If A0 is low when the conversion is initiated, then channels V_{A1} and V_{A2} are selected. If A0 is high when the conversion is initiated, channels V_{B1} and V_{B2} are selected.
21	$\overline{\text{CS}}$	Chip Select Input. Active low logic input. The device is selected when this input is active.
22	$\overline{\text{RD}}$	Read Input. Active low logic input. This input is used in conjunction with $\overline{\text{CS}}$ low to enable the data outputs and read a conversion result from the AD7863.
23	BUSY	Busy Output. The busy output is triggered high by the falling edge of $\overline{\text{CONVST}}$ and remains high until conversion is completed.
24	V_{DD}	Analog and Digital Positive Supply Voltage, 5.0 V ± 5%.
25	V_{A1}	Input Number 1 of Channel A. Analog input voltage ranges of ±10 V (AD7863-10), ±2.5 V (AD7863-3), and 0 V to 2.5 V (AD7863-2).
26	V_{B1}	Input Number 1 of Channel B. Analog input voltage ranges of ±10 V (AD7863-10), ±2.5 V (AD7863-3), and 0 V to 2.5 V (AD7863-2).
27	AGND	Analog Ground. Ground reference for mux, track/hold, reference, and DAC circuitry.
28	DB13	Data Bit 13 (MSB). Three-state TTL output. Output coding is twos complement for the AD7863-10 and AD7863-3. Output coding is straight (natural) binary for the AD7863-2.

TERMINOLOGY

Signal-to-(Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the analog-to-digital converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all non-fundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

Signal to (Noise + Distortion) = (6.02*N* + 1.76) dB

For a 14-bit converter, this is 86.04 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7863 it is defined as

$$THD\,(dB) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}$$

where:

V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, and V_5 are the rms amplitudes of the second through the fifth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3. Intermodulation terms are those for which neither m nor n is equal to zero. For example, the second order terms include (fa + fb) and (fa − fb), and the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7863 is tested using two input frequencies. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, and the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental, expressed in decibels (dB).

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 50 kHz sine wave signal to all nonselected channels and determining how much that signal is attenuated in the selected channel. The figure given is the worst case across all channels.

Relative Accuracy
Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Positive Gain Error (AD7863-10, ±10 V, AD7863-3, ±2.5 V)
This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal 4 × V_{REF} − 1 LSB (AD7863-10, ±10 V range) or V_{REF} − 1 LSB (AD7863-3, ±2.5 V range), after the bipolar offset error has been adjusted out.

Positive Gain Error (AD7863-2, 0 V to 2.5 V)
This is the deviation of the last code transition (11 . . . 110 to 11 . . . 111) from the ideal V_{REF} − 1 LSB, after the unipolar offset error has been adjusted out.

Bipolar Zero Error (AD7863-10, ±10 V, AD7863-3, ±2.5 V)
This is the deviation of the midscale transition (all 0s to all 1s) from the ideal 0 V (AGND).

Unipolar Offset Error (AD7863-2, 0 V to 2.5 V)
This is the deviation of the first code transition (00 . . . 000 to 00 . . . 001) from the ideal AGND + 1 LSB.

Negative Gain Error (AD7863-10, ±10 V, AD7863-3, ±2.5 V)
This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal −4 × V_{REF} + 1 LSB (AD7863-10, ±10 V range) or −V_{REF} + 1 LSB (AD7863-3, ±2.5 V range), after bipolar zero error has been adjusted out.

Track-and-Hold Acquisition Time
Track-and-hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, with ±½ LSB, after the end of conversion (the point at which the track-and-hold returns to track mode). It also applies to situations where a change in the selected input channel takes place or where there is a step input change on the input voltage applied to the selected $V_{AX/BX}$ input of the AD7863. It means that the user must wait for the duration of the track-and-hold acquisition time after the end of conversion or after a channel change/step input change to $V_{AX/BX}$ before starting another conversion, to ensure that the part operates to specification.

CONVERTER DETAILS

The AD7863 is a high speed, low power, dual 14-bit analog-to-digital converter that operates from a single 5 V supply. The part contains two 5.2 µs successive approximation ADCs, two track-and-hold amplifiers, an internal 2.5 V reference, and a high speed parallel interface. Four analog inputs are grouped into two channels (A and B) selected by the A0 input. Each channel has two inputs (V_{A1} and V_{A2} or V_{B1} and V_{B2}) that can be sampled and converted simultaneously, thus preserving the relative phase information of the signals on both analog inputs. The part accepts an analog input range of ±10 V (AD7863-10), ±2.5 V (AD7863-3), and 0 V to 2.5 V (AD7863-2). Overvoltage protection on the analog inputs for the part allows the input voltage to go to ±17 V, ±7 V, or +7 V, respectively, without causing damage. The AD7863 has two operating modes, the high sampling mode and the auto sleep mode, where the part automatically goes into sleep after the end of conversion. These modes are discussed in more detail in the Timing and Control section.

Conversion is initiated on the AD7863 by pulsing the $\overline{\text{CONVST}}$ input. On the falling edge of $\overline{\text{CONVST}}$, both on-chip track-and-holds are simultaneously placed into hold and the conversion sequence is started on both channels. The conversion clock for the part is generated internally using a laser-trimmed clock oscillator circuit. The BUSY signal indicates the end of conversion and at this time the conversion results for both channels are available to be read. The first read after a conversion accesses the result from V_{A1} or V_{B1}, and the second read accesses the result from V_{A2} or V_{B2}, depending on whether the multiplexer select A0 is low or high, respectively, before the conversion is initiated. Data is read from the part via a 14-bit parallel data bus with standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals.

Conversion time for the AD7863 is 5.2 µs in the high sampling mode (10 µs for the auto sleep mode), and the track/hold acquisition time is 0.5 µs. To obtain optimum performance from the part, the read operation should not occur during the conversion or during the 400 ns prior to the next conversion. This allows the part to operate at throughput rates up to 175 kHz and achieve data sheet specifications.

TRACK-AND-HOLD SECTION

The track-and-hold amplifiers on the AD7863 allow the ADCs to accurately convert an input sine wave of full-scale amplitude to 14-bit accuracy. The input bandwidth of the track-and-hold is greater than the Nyquist rate of the ADC, even when the ADC is operated at its maximum throughput rate of 175 kHz (that is, the track-and hold can handle input frequencies in excess of 87.5 kHz).

The track-and-hold amplifiers acquire input signals to 14-bit accuracy in less than 500 ns. The operation of the track-and-holds is essentially transparent to the user. The two track-and-hold amplifiers sample their respective input channels simultaneously, on the falling edge of $\overline{\text{CONVST}}$. The aperture time for the track-and-holds (that is, the delay time between the external $\overline{\text{CONVST}}$ signal and the track-and-hold actually going into hold) is well-matched across the two track-and-holds on one device and also well-matched from device to device. This allows the relative phase information between different input channels to be accurately preserved. It also allows multiple AD7863s to simultaneously sample more than two channels. At the end of conversion, the part returns to its tracking mode. The acquisition time of the track-and-hold amplifiers begins at this point.

REFERENCE SECTION

The AD7863 contains a single reference pin, labeled V_{REF}, that provides access to the part's own 2.5 V reference. Alternatively, an external 2.5 V reference can be connected to this pin, thus providing the reference source for the part. The part is specified with a 2.5 V reference voltage. Errors in the reference source result in gain errors in the AD7863 transfer function and add to the specified full-scale errors on the part. On the AD7863-10 and AD7863-3, it also results in an offset error injected in the attenuator stage.

The AD7863 contains an on-chip 2.5 V reference. To use this reference as the reference source for the AD7863, connect two 0.1 µF disc ceramic capacitors from the V_{REF} pin to AGND. The voltage that appears at this pin is internally buffered before being applied to the ADC. If this reference is required for use external to the AD7863, it should be buffered because the part has a FET switch in series with the reference output resulting in a source impedance for this output of 5.5 kΩ nominal. The tolerance on the internal reference is ±10 mV at 25°C with a typical temperature coefficient of 25 ppm/°C and a maximum error over temperature of ±25 mV.

If the application requires a reference with a tighter tolerance or the AD7863 needs to be used with a system reference, the user has the option of connecting an external reference to this V_{REF} pin. The external reference effectively overdrives the internal reference and thus provides the reference source for the ADC. The reference input is buffered before being applied to the ADC with a maximum input current of ±100 µA. A suitable reference source for the AD7863 is the AD780 precision 2.5 V reference.

CIRCUIT DESCRIPTION

ANALOG INPUT SECTION

The AD7863 is offered as three part types: the AD7863-10, which handles a ±10 V input voltage range, the AD7863-3, which handles input voltage range ±2.5 V and the AD7863-2, which handles a 0 V to 2.5 V input voltage range.

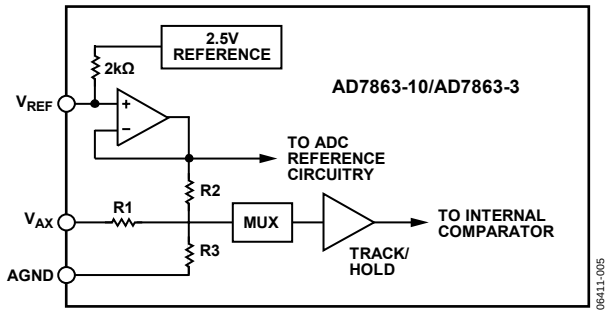


Figure 5. AD7863-10/AD7863-3 Analog Input Structure

Figure 5 shows the analog input section for the AD7863-10 and AD7863-3. The analog input range of the AD7863-10 is ±10 V into an input resistance of typically 9 kΩ. The analog input range of the AD7863-3 is ±2.5 V into an input resistance of typically 3 kΩ. This input is benign, with no dynamic charging currents because the resistor stage is followed by a high input impedance stage of the track-and-hold amplifier. For the AD7863-10, R1 = 8 kΩ, R2 = 2 kΩ and R3 = 2 kΩ. For the AD7863-3, R1 = R2 = 2 kΩ and R3 is open circuit.

For the AD7863-10 and AD7863-3, the designed code transitions occur on successive integer LSB values (that is, 1 LSB, 2 LSBs, 3 LSBs . . .). Output coding is twos complement binary with 1 LSB = FS/16,384. The ideal input/output transfer function for the AD7863-10 and AD7863-3 is shown in Table 5.

Table 5. Ideal Input/Output Code (AD7863-10/AD7863-3)

Analog Input[1]	Digital Output Code Transition
+FSR/2 – 1 LSB[2]	011 . . . 110 to 011 . . . 111
+FSR/2 – 2 LSBs	011 . . . 101 to 011 . . . 110
+FSR/2 – 3 LSBs	011 . . . 100 to 011 . . . 101
GND + 1 LSB	000 . . . 000 to 000 . . . 001
GND	111 . . . 111 to 000 . . . 000
GND – 1 LSB	111 . . . 110 to 111 . . . 111
–FSR/2 + 3 LSBs	100 . . . 010 to 100 . . . 011
–FSR/2 + 2 LSBs	100 . . . 001 to 100 . . . 010
–FSR/2 + 1 LSB	100 . . . 000 to 100 . . . 001

[1]FSR is full-scale range = 20 V (AD7863-10) and = 5 V (AD7863-3) with V_{REF} = 2.5 V.
[2]1 LSB = FSR/16,384 = 1.22 mV (AD7863-10) and 0.3 mV (AD7863-3) with V_{REF} = 2.5 V.

The analog input section for the AD7863-2 contains no biasing resistors and the $V_{AX/BX}$ pin drives the input directly to the multiplexer and track-and-hold amplifier circuitry. The analog input range is 0 V to 2.5 V into a high impedance stage with an input current of less than 100 nA. This input is benign, with no dynamic charging currents. Once again, the designed code transitions occur on successive integer LSB values. Output coding is straight (natural) binary with 1 LSB = FS/16,384 = 2.5 V/16,384 = 0.15 mV. Table 6 shows the ideal input/output transfer function for the AD7863-2.

Table 6. Ideal Input/Output Code (AD7863-2)

Analog Input[1]	Digital Output Code Transition
+FSR – 1 LSB[2]	111 . . . 110 to 111 . . . 111
+FSR – 2 LSB	111 . . . 101 to 111 . . . 110
+FSR – 3 LSB	111 . . . 100 to 111 . . . 101
GND + 3 LSB	000 . . . 010 to 000 . . . 011
GND + 2 LSB	000 . . . 001 to 000 . . . 010
GND + 1 LSB	000 . . . 000 to 000 . . . 001

[1]FSR is full-scale range = 2.5 V for AD7863-2 with V_{REF} = 2.5 V.
[2]1 LSB = FSR/16,384 = 0.15 mV for AD7863-2 with V_{REF} = 2.5 V.

OFFSET AND FULL-SCALE ADJUSTMENT

In most digital signal processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Invariably, some applications require that the input signal span the full analog input dynamic range. In such applications, offset and full-scale error have to be adjusted to zero.

Figure 6 shows a typical circuit that can be used to adjust the offset and full-scale errors on the AD7863 (V_{A1} on the AD7863-10 version is shown for example purposes only). Where adjustment is required, offset error must be adjusted before full-scale error. This is achieved by trimming the offset of the op amp driving the analog input of the AD7863 while the input voltage is ½ LSB below analog ground. The trim procedure is as follows: apply a voltage of –0.61 mV (–½ LSB) at V_1 in Figure 6 and adjust the op amp offset voltage until the ADC output code flickers between 11 1111 1111 1111 and 00 0000 0000 0000.

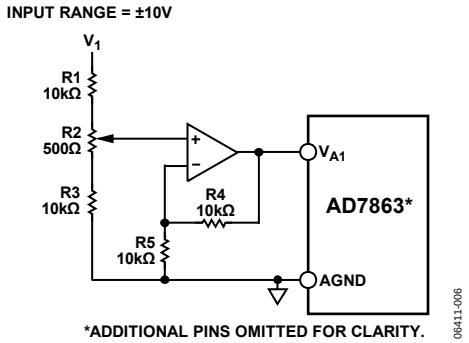


Figure 6. Full-Scale Adjust Circuit

Gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows:

Positive Full-Scale Adjust (−10 Version)

Apply a voltage of 9.9927 V (FS/2 – 1 LSBs) at V_1. Adjust R2 until the ADC output code flickers between 01 1111 1111 1110 and 01 1111 1111 1111.

Negative Full-Scale Adjust (−10 Version)

Apply a voltage of −9.9976 V (−FS + 1 LSB) at V_1. Adjust R2 until the ADC output code flickers between 10 0000 0000 0000 and 10 0000 0000 0001.

An alternative scheme for adjusting full-scale error in systems that use an external reference is to adjust the voltage at the V_{REF} pin until the full-scale error for any of the channels is adjusted out. The good full-scale matching of the channels ensures small full-scale errors on the other channels.

TIMING AND CONTROL

Figure 7 shows the timing and control sequence required to obtain optimum performance (Mode 1) from the AD7863. In the sequence shown, a conversion is initiated on the falling edge of $\overline{\text{CONVST}}$. This places both track-and-holds into hold simultaneously and new data from this conversion is available in the output register of the AD7863 5.2 µs later. The BUSY signal indicates the end of conversion and at this time the conversion results for both channels are available to be read. A second conversion is then initiated. If the multiplexer select (A0) is low, the first and second read pulses after the first conversion accesses the result from Channel A (V_{A1} and V_{A2}, respectively). The third and fourth read pulses, after the second conversion and A0 high, accesses the result from Channel B (V_{B1} and V_{B2}, respectively). The state of A0 can be changed any time after the $\overline{\text{CONVST}}$ goes high, that is, track-and-holds into hold and 500 ns prior to the next falling edge of $\overline{\text{CONVST}}$. Note that A0 should not be changed during conversion if the nonselected channels have negative voltages applied to them, which are outside the input range of the AD7863, because this affects the conversion in progress. Data is read from the part via a 14-bit parallel data bus with standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signal, that is, the read operation consists of a negative going pulse on the $\overline{\text{CS}}$ pin combined with two negative going pulses on the $\overline{\text{RD}}$ pin (while the $\overline{\text{CS}}$ is low), accessing the two 14-bit results. Once the read operation has taken place, a further 400 ns should be allowed before the next falling edge of $\overline{\text{CONVST}}$ to optimize the settling of the track-and-hold amplifier before the next conversion is initiated. The achievable throughput rate for the part is 5.2 µs (conversion time) plus 100 ns (read time) plus 0.4 µs (quiet time). This results in a minimum throughput time of 5.7 µs (equivalent to a throughput rate of 175 kHz).

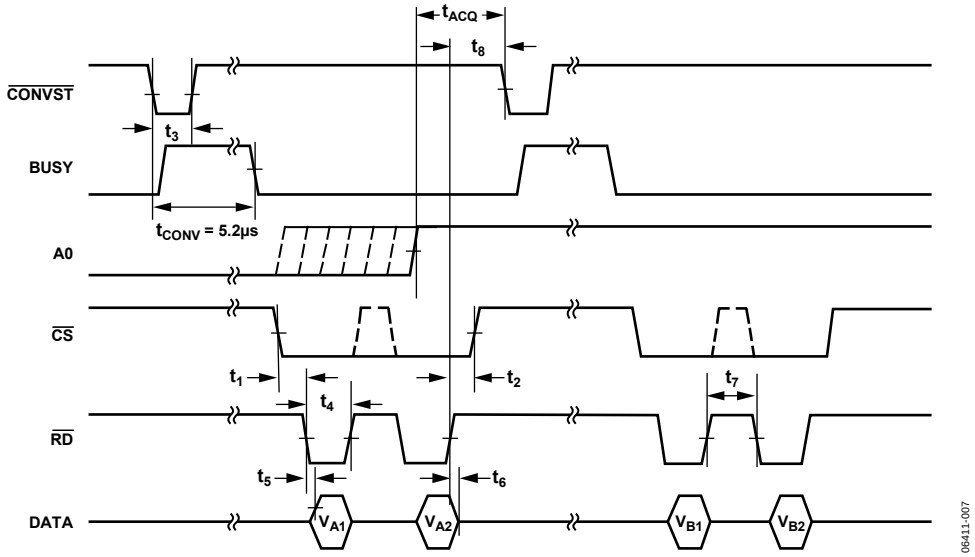


Figure 7. Mode 1 Timing Operation Diagram for High Sampling Performance

Read Options

Apart from the read operation previously described and displayed in Figure 7, other $\overline{CS}$ and $\overline{RD}$ combinations can result in different channels/inputs being read in different combinations. Suitable combinations are shown in Figure 8, Figure 9, and Figure 10.

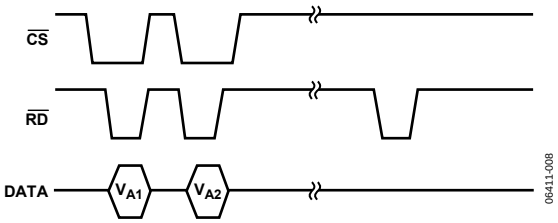


Figure 8. Read Option A (A0 is Low)

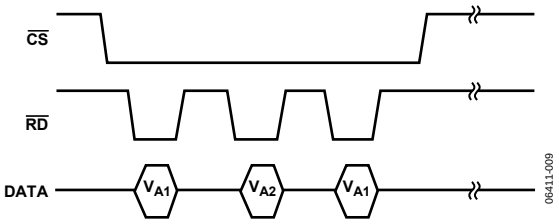


Figure 9. Read Option B (A0 is Low)

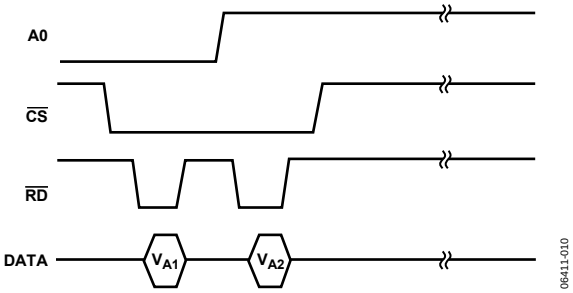


Figure 10. Read Option C

OPERATING MODES

MODE 1 OPERATION

Normal Power, High Sampling Performance

The timing diagram in Figure 7 is for optimum performance in operating Mode 1 where the falling edge of $\overline{\text{CONVST}}$ starts conversion and puts the track-and-hold amplifiers into their hold mode. This falling edge of $\overline{\text{CONVST}}$ also causes the BUSY signal to go high to indicate that a conversion is taking place. The BUSY signal goes low when the conversion is complete, which is 5.2 µs max after the falling edge of $\overline{\text{CONVST}}$ and new data from this conversion is available in the output latch of the AD7863. A read operation accesses this data. If the multiplexer select A0 is low, the first and second read pulses after the first conversion accesses the result from Channel A (V_{A1} and V_{A2}, respectively). The third and fourth read pulses, after the second conversion and A0 high, access the result from Channel B (V_{B1} and V_{B2}, respectively). Data is read from the part via a 14-bit parallel data bus with standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals. This data read operation consists of a negative going pulse on the $\overline{\text{CS}}$ pin combined with two negative going pulses on the $\overline{\text{RD}}$ pin (while the $\overline{\text{CS}}$ is low), accessing the two 14-bit results. For the fastest throughput rate the read operation takes 100 ns. The read operation must be complete at least 400 ns before the falling edge of the next $\overline{\text{CONVST}}$ and this gives a total time of 5.7 µs for the full throughput time (equivalent to 175 kHz). This mode of operation should be used for high sampling applications.

MODE 2 OPERATION

Power-Down, Auto-Sleep After Conversion

The timing diagram in Figure 11 is for optimum performance in operating Mode 2 where the part automatically goes into sleep mode once BUSY goes low after conversion and wakes up before the next conversion takes place. This is achieved by keeping $\overline{\text{CONVST}}$ low at the end of the second conversion, whereas it was high at the end of the second conversion for Mode 1 operation.

The operation shown in Figure 11 shows how to access data from both Channel A and Channel B, followed by the auto sleep mode. One can also set up the timing to access data from Channel A only or Channel B only (see the Read Options section) and then go into auto sleep mode. The rising edge of $\overline{\text{CONVST}}$ wakes up the part. This wake-up time is 4.8 µs when using an external reference and 5 ms when using the internal reference, at which point the track-and-hold amplifiers go into their hold mode, provided the $\overline{\text{CONVST}}$ has gone low. The conversion takes 5.2 µs after this giving a total of 10 µs (external reference, 5.005 ms for internal reference) from the rising edge of $\overline{\text{CONVST}}$ to the conversion being complete, which is indicated by the BUSY going low.

Note that because the wake-up time from the rising edge of $\overline{\text{CONVST}}$ is 4.8 µs, if the $\overline{\text{CONVST}}$ pulse width is greater than 5.2 µs the conversion takes more than the 10 µs (4.8 µs wake-up time + 5.2 µs conversion time) shown in Figure 11 from the rising edge of $\overline{\text{CONVST}}$. This is because the track-and-hold amplifiers go into their hold mode on the falling edge of $\overline{\text{CONVST}}$ and the conversion does not complete for a further 5.2 µs. In this case, the BUSY is the best indicator of when the conversion is complete. Even though the part is in sleep mode, data can still be read from the part.

The read operation is identical to that in Mode 1 operation and must also be complete at least 400 ns before the falling edge of the next $\overline{\text{CONVST}}$ to allow the track-and-hold amplifiers to have enough time to settle. This mode is very useful when the part is converting at a slow rate because the power consumption is significantly reduced from that of Mode 1 operation.

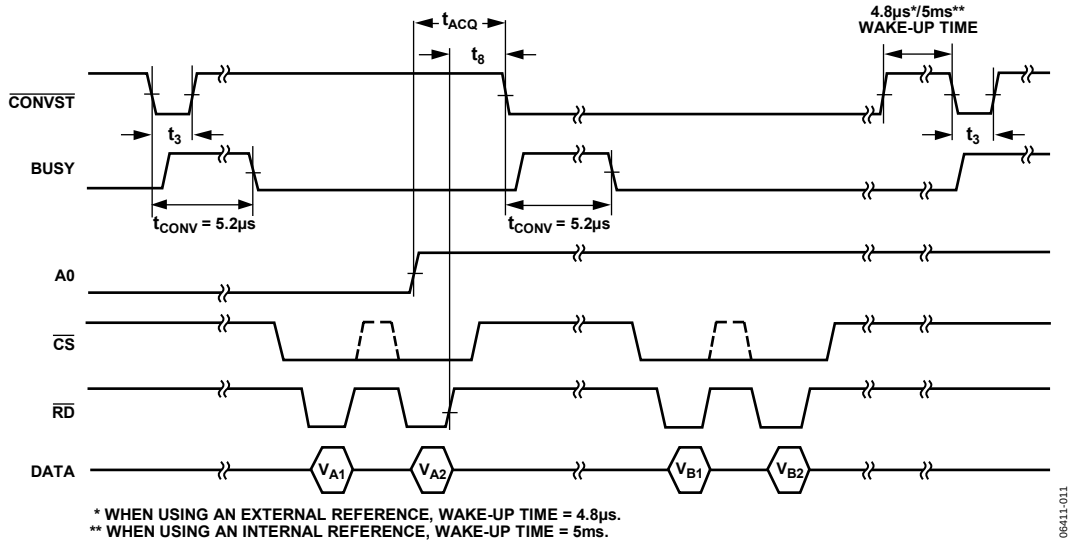


Figure 11. Mode 2 Timing Diagram Where Automatic Sleep Function Is Initiated

AD7863 DYNAMIC SPECIFICATIONS

The AD7863 is specified and tested for dynamic performance as well as traditional dc specifications such as integral and differential nonlinearity. These ac specifications are required for the signal processing applications such as phased array sonar, adaptive filters, and spectrum analysis. These applications require information on the ADC's effect on the spectral content of the input signal. Hence, the parameters for which the AD7863 is specified include SNR, harmonic distortion, intermodulation distortion, and peak harmonics. These terms are discussed in more detail in the following sections.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc; SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)\ \text{dB} \quad (1)$$

where N is the number of bits.

Thus for an ideal 14-bit converter, SNR = 86.04 dB.

Figure 12 shows a histogram plot for 8192 conversions of a dc input using the AD7863 with 5 V supply. The analog input was set at the center of a code transition. It can be seen that the codes appear mainly in the one output bin, indicating very good noise performance from the ADC.

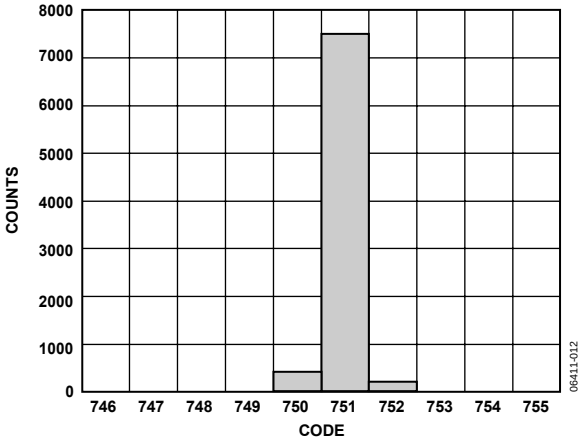


Figure 12. Histogram of 8192 Conversions of a DC Input

The output spectrum from the ADC is evaluated by applying a sine wave signal of very low distortion to the $V_{AX/BX}$ input, which is sampled at a 175 kHz sampling rate. A fast fourier transform (FFT) plot is generated from which the SNR data can be obtained. Figure 13 shows a typical 8192 point FFT plot of the AD7863 with an input signal of 10 kHz and a sampling frequency of 175 kHz. The SNR obtained from this graph is −80.72 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

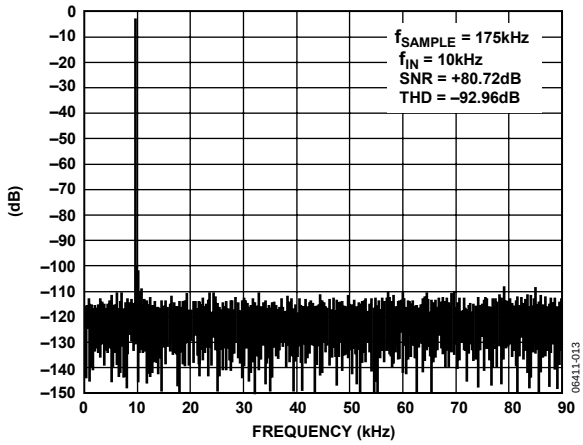


Figure 13. AD7863 FFT Plot

EFFECTIVE NUMBER OF BITS

The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to obtain a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Figure 14 shows a typical plot of effective numbers of bits vs. frequency for an AD7863-2 with a sampling frequency of 175 kHz. The effective number of bits typically falls between 13.11 and 11.05 corresponding to SNR figures of 80.68 dB and 68.28 dB.

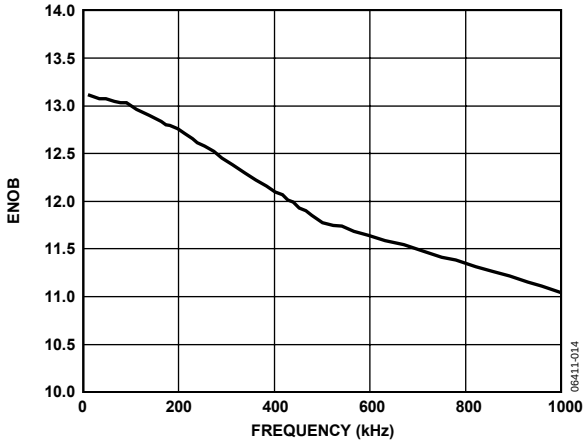


Figure 14. Effective Numbers of Bits vs. Frequency

TOTAL HARMONIC DISTORTION (THD)

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD7863, THD is defined as

$$THD\left(dB\right) = 20\log\frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2}}}{V_1} \qquad (3)$$

where:

V_1 is the rms amplitude of the fundamental.

V_2, V_3, V_4, and V_5 are the rms amplitudes of the second through the fifth harmonic.

THD is also derived from the FFT plot of the ADC output spectrum.

INTERMODULATION DISTORTION

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which neither m nor n is equal to zero. For example, the second order terms include (fa + fb) and (fa – fb) and the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa – 2fb).

In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two equal amplitude, low distortion sine waves. Figure 15 shows a typical IMD plot for the AD7863.

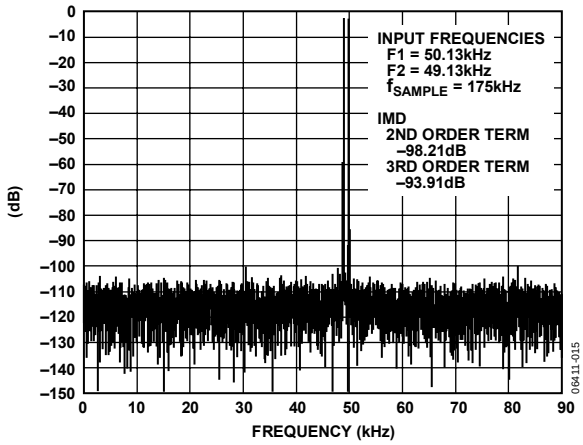


Figure 15. IMD Plot

PEAK HARMONIC OR SPURIOUS NOISE

Harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, the peak is a noise peak.

DC LINEARITY PLOT

Figure 16 and Figure 17 show typical DNL and INL plots for the AD7863.

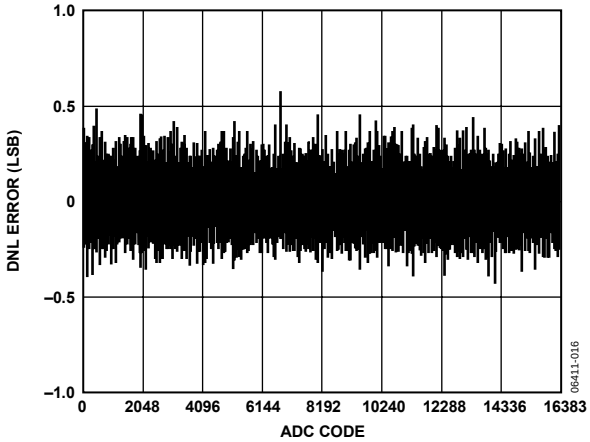


Figure 16. DC DNL Plot

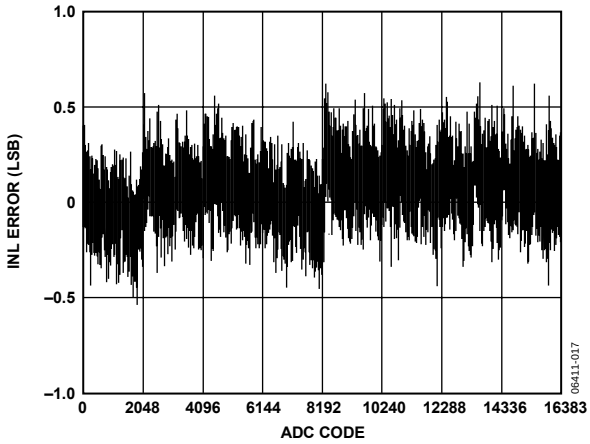


Figure 17. DC INL Plot

POWER CONSIDERATIONS

In the automatic power-down mode the part can be operated at a sample rate that is considerably less than 175 kHz. In this case, the power consumption is reduced and depends on the sample rate. Figure 18 shows a graph of the power consumption vs. sampling rates from 1 Hz to 100 kHz in the automatic power-down mode. The conditions are 5 V supply at 25°C.

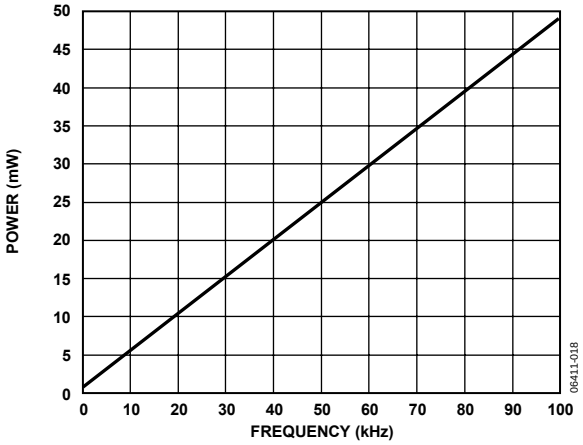


Figure 18. Power vs. Sample Rate in Auto Power-Down

MICROPROCESSOR INTERFACING

The AD7863 high speed bus timing allows direct interfacing to DSP processors as well as modern 16-bit microprocessors. Suitable microprocessor interfaces are shown in Figure 19 through Figure 23.

AD7863 TO ADSP-2100 INTERFACE

Figure 19 shows an interface between the AD7863 and the ADSP-2100. The CONVST signal can be supplied from the ADSP-2100 or from an external source. The AD7863 BUSY line provides an interrupt to the ADSP-2100 when conversion is completed on both channels. The two conversion results can then be read from the AD7863 using two successive reads to the same memory address. The following instruction reads one of the two results:

MR0 = DM (ADC)

where:

MR0 is the ADSP-2100 MR0 register.
ADC is the AD7863 address.

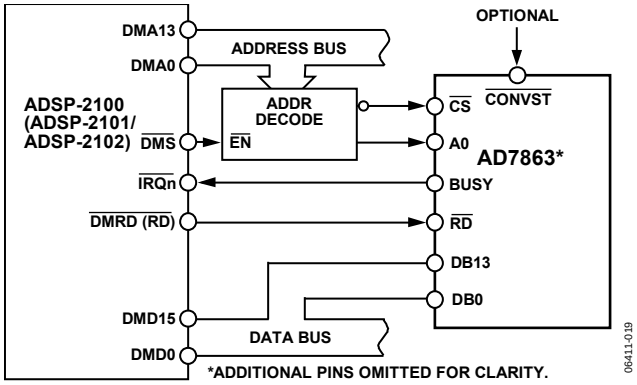


Figure 19. AD7863 to ADSP-2100 Interface

AD7863 TO ADSP-2101/ADSP-2102 INTERFACE

The interface outlined in Figure 19 also forms the basis for an interface between the AD7863 and the ADSP-2101/ADSP-2102. The READ line of the ADSP-2101/ADSP-2102 is labeled RD. In this interface, the RD pulse width of the processor can be programmed using the data memory wait state control register. The instruction used to read one of the two results is as outlined for the ADSP-2100.

AD7863 TO TMS32010 INTERFACE

An interface between the AD7863 and the TMS32010 is shown in Figure 20. Once again the CONVST signal can be supplied from the TMS32010 or from an external source, and the TMS32010 is interrupted when both conversions have been completed. The following instruction is used to read the conversion results from the AD7863:

IN D, ADC

where:

D is data memory address.
ADC is the AD7863 address.

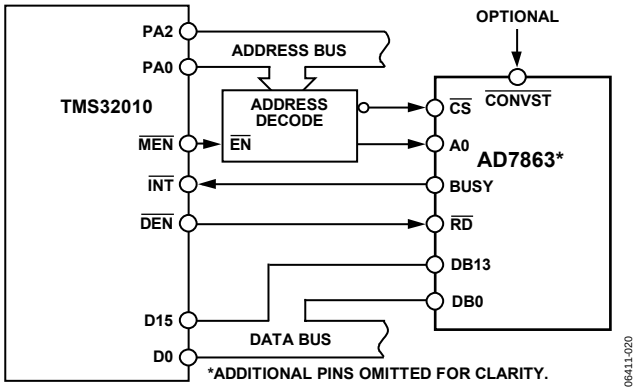


Figure 20. AD7863 to TMS32010 Interface

AD7863 TO TMS320C25 INTERFACE

Figure 21 shows an interface between the AD7863 and the TMS320C25. As with the two previous interfaces, conversion can be initiated from the TMS320C25 or from an external source, and the processor is interrupted when the conversion sequence is completed. The TMS320C25 does not have a separate RD output to drive the AD7863 RD input directly. This has to be generated from the processor STRB and R/W outputs with the addition of some logic gates. The RD signal is OR gated with the MSC signal to provide the one WAIT state required in the read cycle for correct interface timing. Conversion results are read from the AD7863 using the following instruction:

IN D, ADC

where:

D is data memory address.
ADC is the AD7863 address.

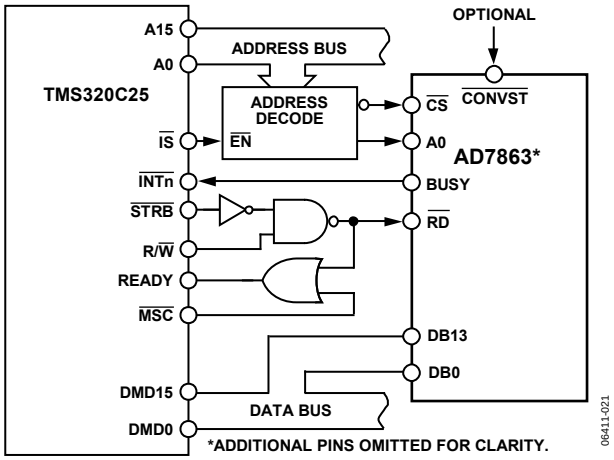


Figure 21. AD7863 to TMS320C25 Interface

Some applications may require that the conversion be initiated by the microprocessor rather than an external timer. One option is to decode the AD7863 $\overline{\text{CONVST}}$ from the address bus so that a write operation starts a conversion. Data is read at the end of the conversion sequence as before. Figure 23 shows an example of initiating conversion using this method. Note that for all interfaces, it is preferred that a read operation not be attempted during conversion.

AD7863 TO MC68000 INTERFACE

An interface between the AD7863 and the MC68000 is shown in Figure 22. As before, conversion can be supplied from the MC68000 or from an external source. The AD7863 BUSY line can be used to interrupt the processor or, alternatively, software delays can ensure that conversion has been completed before a read to the AD7863 is attempted. Because of the nature of its interrupts, the MC68000 requires additional logic (not shown in Figure 23) to allow it to be interrupted correctly. For further information on MC68000 interrupts, consult the MC68000 users manual.

The MC68000 $\overline{\text{AS}}$ and R/$\overline{\text{W}}$ outputs are used to generate a separate $\overline{\text{RD}}$ input signal for the AD7863. $\overline{\text{CS}}$ is used to drive the MC68000 $\overline{\text{DTACK}}$ input to allow the processor to execute a normal read operation to the AD7863. The conversion results are read using the following MC68000 instruction:

MOVE.W ADC, D0

where:

D0 is the 68000 *D*0 register.
ADC is the AD7863 address.

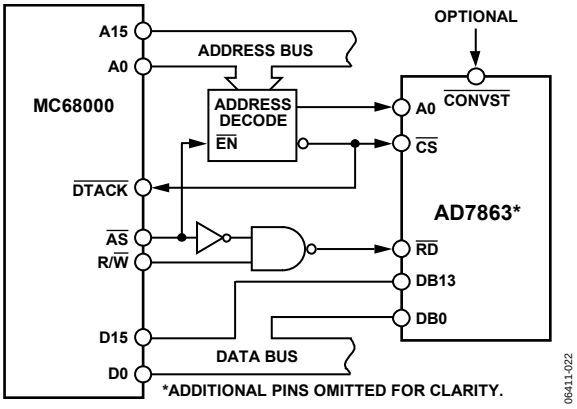


Figure 22. AD7863 to MC68000 Interface

AD7863 TO 80C196 INTERFACE

Figure 23 shows an interface between the AD7863 and the 80C196 microprocessor. Here, the microprocessor initiates conversion. This is achieved by gating the 80C196 $\overline{\text{WR}}$ signal with a decoded address output (different from the AD7863 $\overline{\text{CS}}$ address). The AD7863 BUSY line is used to interrupt the microprocessor when the conversion sequence is completed.

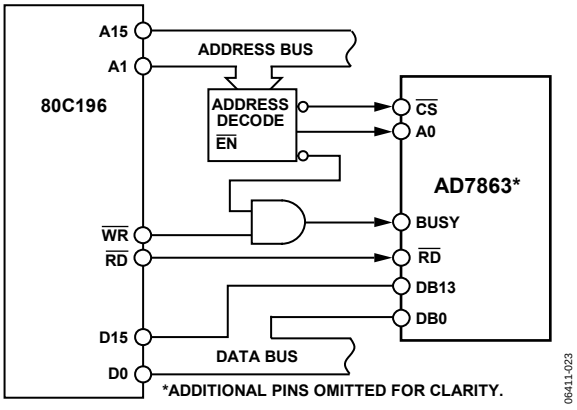


Figure 23. AD7863–80C196 Interface

VECTOR MOTOR CONTROL

The current drawn by a motor can be split into two components: one produces torque and the other produces magnetic flux. For optimal performance of the motor, these two components should be controlled independently. In conventional methods of controlling a three-phase motor, the current (or voltage) supplied to the motor and the frequency of the drive are the basic control variables. However, both the torque and flux are functions of current (or voltage) and frequency. This coupling effect can reduce the performance of the motor because, for example, if the torque is increased by increasing the frequency, the flux tends to decrease.

Vector control of an ac motor involves controlling the phase in addition to drive and current frequency. Controlling the phase of the motor requires feedback information on the position of the rotor relative to the rotating magnetic field in the motor. Using this information, a vector controller mathematically transforms the three phase drive currents into separate torque and flux components. The AD7863 is ideally suited for use in vector motor control applications.

A block diagram of a vector motor control application using the AD7863 is shown in Figure 24. The position of the field is derived by determining the current in each phase of the motor. Only two phase currents need to be measured because the third can be calculated if two phases are known. V_{A1} and V_{A2} of the AD7863 are used to digitize this information.

Simultaneous sampling is critical to maintaining the relative phase information between the two channels. A current sensing isolation amplifier, transformer, or Hall effect sensor is used between the motor and the AD7863. Rotor information is obtained by measuring the voltage from two of the inputs to the motor. V_{B1} and V_{B2} of the AD7863 are used to obtain this information. Once again the relative phase of the two channels is important. A DSP microprocessor is used to perform the mathematical transformations and control loop calculations on the information fed back by the AD7863.

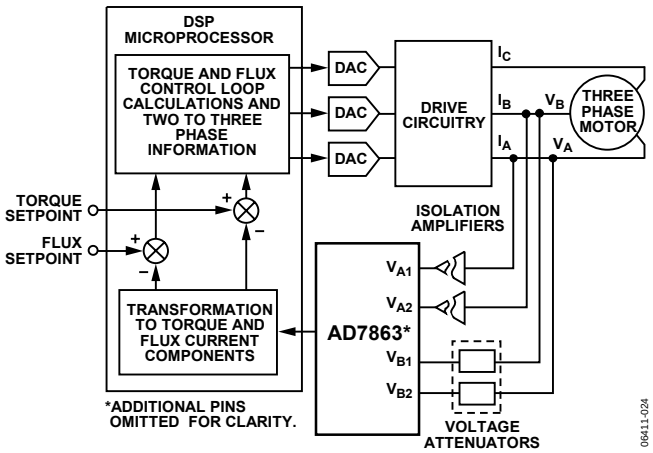


Figure 24. Vector Motor Control Using the AD7863

MULTIPLE AD7863S

Figure 25 shows a system where a number of AD7863s can be configured to handle multiple input channels. This type of configuration is common in applications such as sonar and radar. The AD7863 is specified with typical limits on aperture delay. This means that the user knows the difference in the sampling instant between all channels. This allows the user to maintain relative phase information between the different channels.

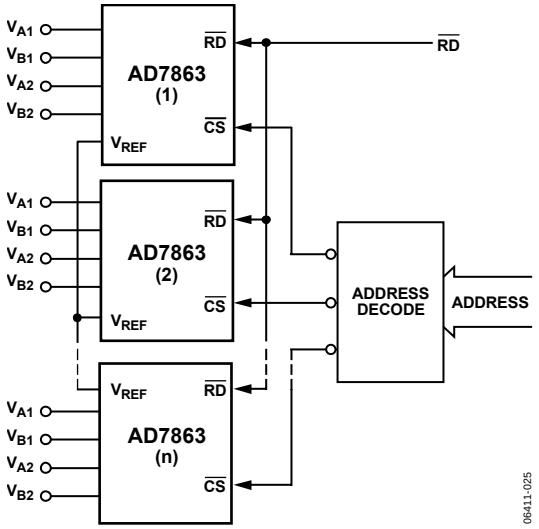


Figure 25. Multiple AD7863s in Multichannel System

A common read signal from the microprocessor drives the $\overline{RD}$ input of all AD7863s. Each AD7863 is designated a unique address selected by the address decoder. The reference output of AD7863 Number 1 is used to drive the reference input of all other AD7863s in the circuit shown in Figure 25. One V_{REF} can be used to provide the reference to several other AD7863s. Alternatively, an external or system reference can be used to drive all V_{REF} inputs. A common reference ensures good full-scale tracking between all channels.

APPLICATIONS HINTS

PC BOARD LAYOUT CONSIDERATIONS

The AD7863 is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the AD7863 it is imperative that great care be given to the PC board layout. Figure 26 shows a recommended connection diagram for the AD7863.

GROUND PLANES

The AD7863 and associated analog circuitry should have a separate ground plane, referred to as the analog ground plane (AGND). This analog ground plane should encompass all AD7863 ground pins (including the DGND pin), voltage reference circuitry, power supply bypass circuitry, the analog input traces, and any associated input/buffer amplifiers.

The regular PCB ground plane (referred to as the DGND for this discussion) area should encompass all digital signal traces, excluding the ground pins, leading up to the AD7863.

POWER PLANES

The PC board layout should have two distinct power planes, one for analog circuitry and one for digital circuitry. The analog power plane should encompass the AD7863 (V_{DD}) and all associated analog circuitry. This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point, if necessary through a ferrite bead, as illustrated in Figure 26. This bead (part numbers for reference: Fair-Rite 274300111 or Murata BL01/02/03) should be located within three inches of the AD7863.

The PCB power plane (V_{CC}) should provide power to all digital logic on the PC board, and the analog power plane (V_{DD}) should provide power to all AD7863 power pins, voltage reference circuitry and any input amplifiers, if needed. A suitable low noise amplifier for the AD7863 is the AD797, one for each input. Ensure that the $+V_S$ and the $-V_S$ supplies to each amplifier are individually decoupled to AGND.

The PCB power (V_{CC}) and ground (DGND) should not overlay portions of the analog power plane (V_{DD}). Keeping the V_{CC} power and the DGND planes from overlaying the V_{DD} contributes to a reduction in plane-to-plane noise coupling.

SUPPLY DECOUPLING

Noise on the analog power plane (V_{DD}) can be further reduced by use of multiple decoupling capacitors (Figure 26).

Optimum performance is achieved by the use of disc ceramic capacitors. The V_{DD} and reference pins (whether using an external or an internal reference) should be individually decoupled to the analog ground plane (AGND). This should be done by placing the capacitors as close as possible to the AD7863 pins with the capacitor leads as short as possible, thus minimizing lead inductance.

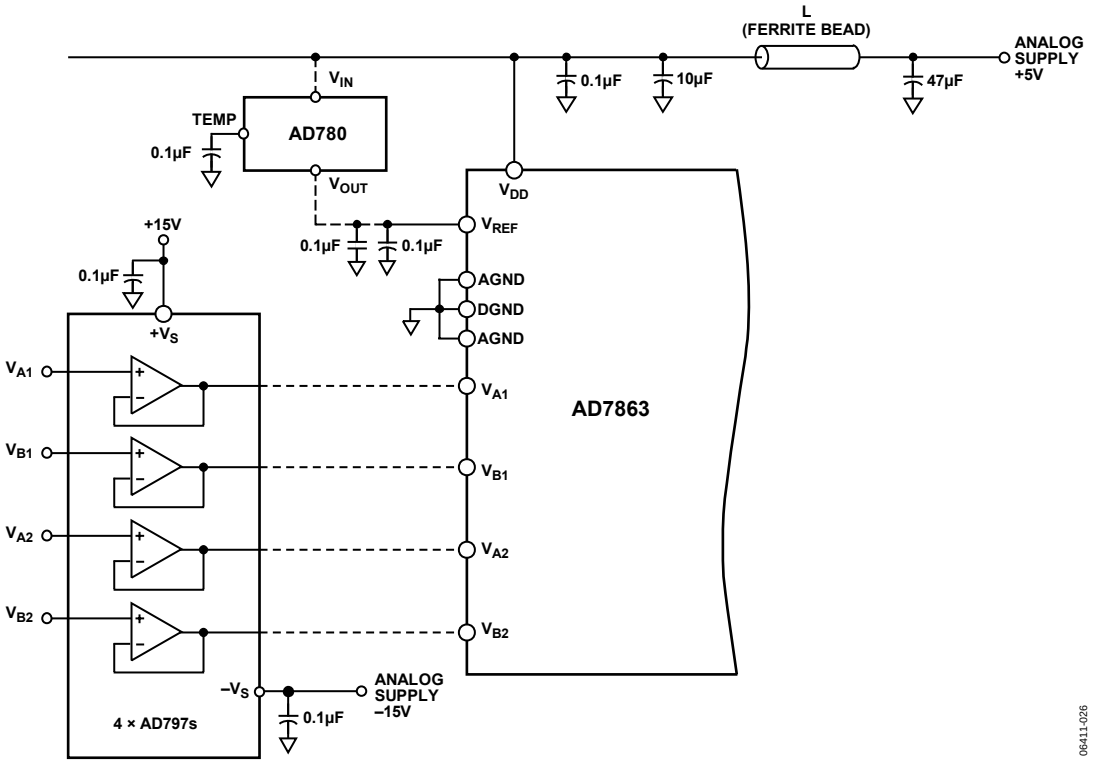
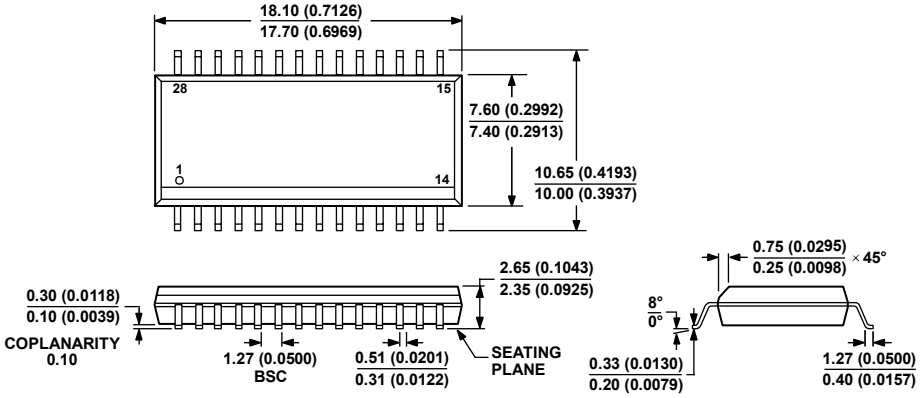


Figure 26. Typical Connections Diagram Including the Relevant Decoupling

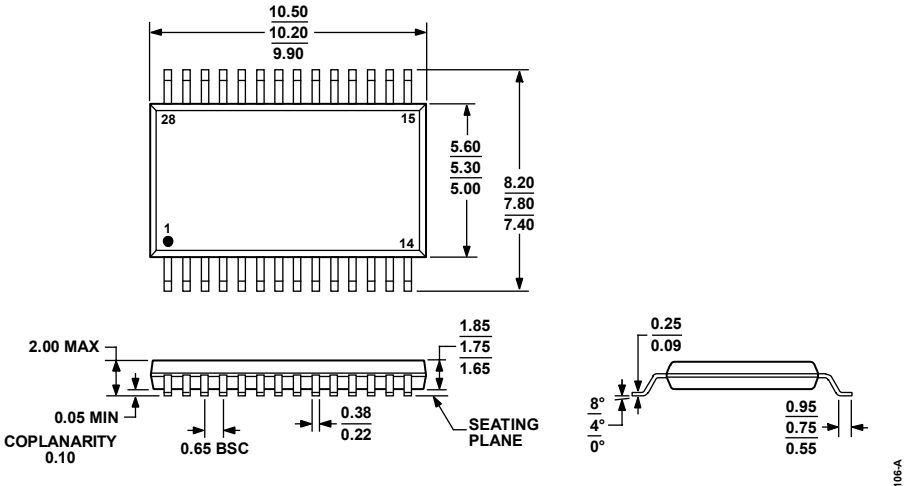
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060706-A

Figure 27. 28-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-28)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-150-AH

060106-A

Figure 28. 28-Lead Shrink Small Outline Package [SSOP]
(RS-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Input Range	Relative Accuracy	Temperature Range	Package Description	Package Option
AD7863AR-10	±10 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863AR-10REEL	±10 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863AR-10REEL7	±10 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863ARZ-10[1]	±10 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863ARZ-10REEL[1]	±10 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863ARZ-10REEL7[1]	±10 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863ARS-10	±10 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARS-10REEL	±10 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARS-10REEL7	±10 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARSZ-10[1]	±10 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARSZ-10REEL[1]	±10 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARSZ-10REEL7[1]	±10 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863BR-10	±10 V	±2.0 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863BR-10REEL	±10 V	±2.0 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863BR-10REEL7	±10 V	±2.0 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863BRZ-10[1]	±10 V	±2.0 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863AR-3	±2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863AR-3REEL	±2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863AR-3REEL7	±2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863ARZ-3[1]	±2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863ARS-3	±2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARS-3REEL	±2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARS-3REEL7	±2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARSZ-3[1]	±2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARSZ-3REEL[1]	±2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARSZ-3REEL7[1]	±2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863BR-3	±2.5 V	±2.0 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863BR-3REEL	±2.5 V	±2.0 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863BR-3REEL7	±2.5 V	±2.0 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863BRZ-3[1]	±2.5 V	±2.0 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863AR-2	0 V to 2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863AR-2REEL	0 V to 2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863AR-2REEL7	0 V to 2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863ARZ-2[1]	0 V to 2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863ARZ-2REEL[1]	0 V to 2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863ARZ-2REEL7[1]	0 V to 2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SOIC_W	RW-28
AD7863ARS-2	0 V to 2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARS-2REEL	0 V to 2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARS-2REEL7	0 V to 2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARSZ-2[1]	0 V to 2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARSZ-2REEL[1]	0 V to 2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
AD7863ARSZ-2REEL7[1]	0 V to 2.5 V	±2.5 LSB	–40°C to +85°C	28-Lead SSOP	RS-28
EVAL-AD7863CB				Evaluation Board	

[1] Z = Pb-free part.

NOTES

NOTES

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