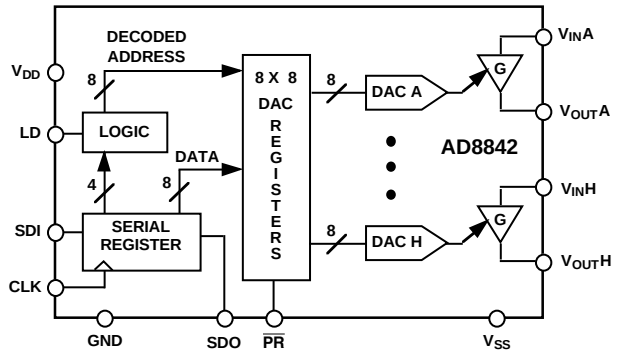
8-Bit Octal, 4-Quadrant Multiplying, CMOS TrimDAC

AD8842

FEATURES
Low Cost
Replaces 8 Potentiometers
50 kHz 4-Quadrant Multiplying Bandwidth
Low Zero Output Error
Eight Individual Channels
3-Wire Serial Input
500 kHz Update Data Loading Rate
±3 V Output Swing
Midscale Preset, Zero Volts Out

APPLICATIONS
Automatic Adjustment
Trimmer Replacement
Vertical Deflection Amplitude Adjustment
Waveform Generation and Modulation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8842 provides eight general purpose digitally controlled voltage adjustment devices. The TrimDAC® capability allows replacement of the mechanical trimmer function in new designs. The AD8842 is ideal for ac or dc gain control of up to 50 kHz bandwidth signals. The four-quadrant multiplying capability is useful for signal inversion and modulation often found in video vertical deflection circuitry.

Internally the AD8842 contains eight voltage output digital-to-analog converters, each with separate voltage inputs. A new current conveyor amplifier design performs the four-quadrant multiplying function with a single amplifier at the output of the current steering digital-to-analog converter. This approach offers an improved constant input resistance performance versus previous voltage switched DACs used in TrimDAC circuits, eliminating the need for additional input buffer amplifiers.

Each DAC has its own DAC register that holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register that is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded where the first 4 bits determine the address of the DAC register to be loaded with the last 8 bits of data. A serial data output pin at the opposite end of the serial register allows simple daisy chaining in multiple DAC applications without additional external decoding logic.

TrimDAC is a registered trademark of Analog Devices, Inc.
The current conveyor amplifier is a patented circuit belonging to Analog Devices, Inc.

The AD8842 consumes only 95 mW from ±5 V power supplies. For single 5 V supply applications consult the DAC-8841. The AD8842 is pin compatible with the 1 MHz multiplying bandwidth DAC8840. The AD8842 is available in 24-pin plastic DIP and surface mount SOL-24 packages.

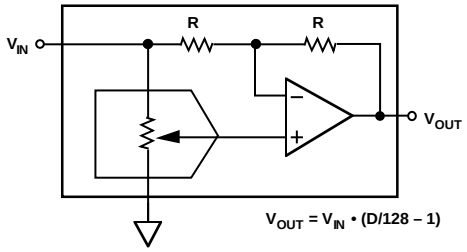


Figure 1. Functional Circuit of One 4-Quadrant Multiplying Channel

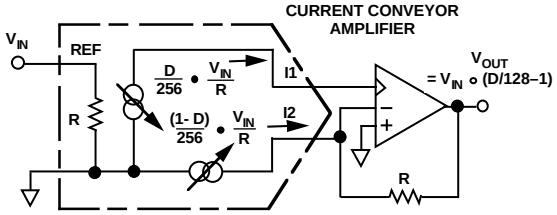


Figure 2. Actual Current Conveyor Implementation of Multiplying DAC Channel

REV. A

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AD8842–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{DD} = +5 V, V_{SS} = –5 V, All $V_{IN}x$ = +3 V, T_A = –40°C to +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY—All Specifications Apply for DACs A, B, C, D, E, F, G, H						
Resolution	N		8			Bits
Integral Nonlinearity Error	INL			±0.2	±1	LSB
Differential Nonlinearity	DNL	All Devices Monotonic		±0.4	±1	LSB
Full-Scale Gain Error	G_{FSE}			2		LSB
Output Offset	V_{BZE}	$\overline{PR}$ = 0, Sets D = 80_H		5	25	mV
Output Offset Drift	TCV_{BZ}	$\overline{PR}$ = 0, Sets D = 80_H		5		µV/°C
VOLTAGE INPUTS—Applies to All Inputs $V_{IN}x$						
Input Voltage Range[1]	IVR		±3	±4		V
Input Resistance	R_{IN}		12	19		kΩ
Input Capacitance	C_{IN}			9		pF
DAC OUTPUTS—Applies to All Outputs $V_{OUT}x$						
Voltage Range[1]	OVR	R_L = 10 kΩ	±3	±4		V
Output Current	I_{OUT}	ΔV_{OUT} < 1.5 LSB	±3			mA
Capacitive Load	C_L	No Oscillation		500		pF
DYNAMIC PERFORMANCE—Applies to All DACs						
Full Power Gain Bandwidth[1]	GBW	$V_{IN}x$ = ±3 V_P, R_L = 2 kΩ, C_L = 10 pF	10	50		kHz
Slew Rate		Measured 10% to 90%				
Positive	SR+	$\Delta V_{OUT}x$ = +5.5 V	0.5	1.0		V/µs
Negative	SR–	$\Delta V_{OUT}x$ = –5.5 V	1.0	1.8		V/µs
Total Harmonic Distortion	THD	$V_{IN}x$ = 4 V p-p, D = FF_H, f = 1 kHz, f_{LPF} = 80 kHz, R_L = 1 kΩ		0.01		%
Spot Noise Voltage	e_N	f = 1kHz, V_{IN} = 0 V		78		nV/√Hz
Output Settling Time	t_S	±1 LSB Error Band, D = 00_H to FF_H		2.9		µs
		D = FF_H to 00_H		5.4		µs
Channel-to-Channel Crosstalk	C_T	Measured Between Adjacent Channels, f = 100 kHz		72		dB
Digital Feedthrough	Q	$V_{IN}x$ = 0 V, D = 0 to 255_{10}		5		nV-s
POWER SUPPLIES						
Positive Supply Current	I_{DD}	$\overline{PR}$ = 0 V		10	14	mA
Negative Supply Current	I_{SS}	$\overline{PR}$ = 0 V		9	13	mA
Power Dissipation[2]	P_{DISS}			95	135	mW
Power Supply Rejection	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%		0.0001	0.01	%/%
Power Supply Range	PSR	V_{DD}, $\lvert V_{SS} \rvert$	4.75	5.00	5.25	V
DIGITAL INPUTS						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	V
Input Current	I_L				±10	µA
Input Capacitance	C_{IL}			7		pF
Input Coding				Offset Binary		
DIGITAL OUTPUT						
Logic High	V_{OH}	I_{OH} = –0.4 mA	3.5			V
Logic Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
TIMING SPECIFICATIONS[1]						
Input Clock Pulse Width	t_{CH}, t_{CL}		60			ns
Data Setup Time	t_{DS}		40			ns
Data Hold Time	t_{DH}		20			ns
CLK to SDO Propagation Delay	t_{PD}				80	ns
DAC Register Load Pulse Width	t_{LD}		70			ns
Preset Pulse Width	t_{PR}		50			ns
Clock Edge to Load Time	t_{CKLD}		30			ns
Load Edge to Next Clock Edge	t_{LDCK}		60			ns

NOTES
[1]Guaranteed by design, not subject to production test.
[2]Calculated limit = 5 V × (I_{DD} + I_{SS}).
Specifications subject to change without notice.

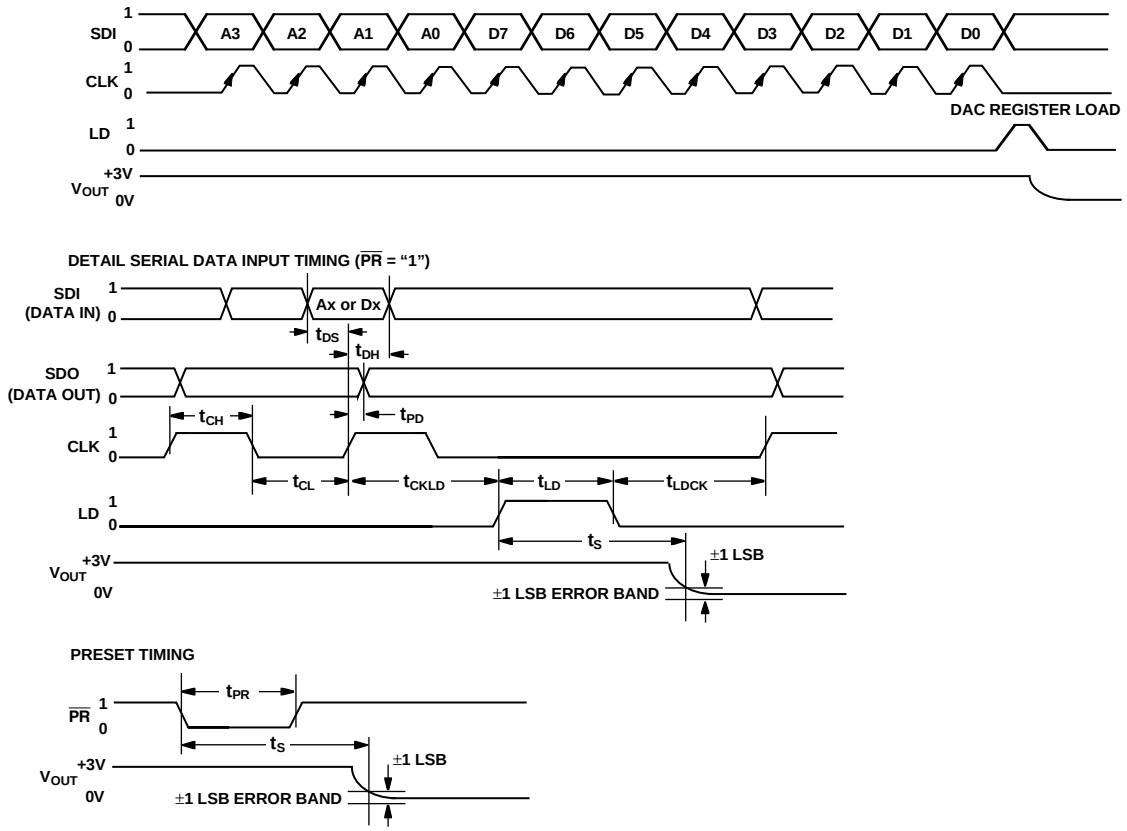


Figure 3. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . –0.3 V, +7 V
V_{SS} to GND . . . . . +0.3 V, –7 V
V_{IN}x to GND . . . . . V_{DD}, V_{SS}
V_{OUT}x to GND . . . . . V_{DD}, V_{SS}
Short Circuit I_{OUT}x to GND . . . . . Continuous
Digital Input & Output Voltage to GND . . . . . V_{DD}, 0 V
Operating Temperature Range . . . . . –40°C to +85°C
Maximum Junction Temperature (T_J Max) . . . . . +150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Package Power Dissipation . . . . . $(T_J Max–T_A)/\theta_{JA}$
Thermal Resistance θ_{JA},
SOIC (SOL-24) . . . . . 70°C/W
P-DIP (N-24) . . . . . 57°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8842 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN DESCRIPTION

Pin	Mnemonic	Description
1	$V_{OUT}C$	DAC C Output
2	$V_{OUT}B$	DAC B Output
3	$V_{OUT}A$	DAC A Output
4	$V_{IN}B$	DAC B Reference Input
5	$V_{IN}A$	DAC A Reference Input
6	GND	Ground
7	$\overline{PR}$	Preset Input, active low, all DAC registers = 80_H
8	$V_{IN}E$	DAC E Reference Input
9	$V_{IN}F$	DAC F Reference Input
10	$V_{OUT}E$	DAC E Output
11	$V_{OUT}F$	DAC F Output
12	$V_{OUT}G$	DAC G Output
13	$V_{OUT}H$	DAC H Output
14	$V_{IN}G$	DAC G Reference Input
15	$V_{IN}H$	DAC H Reference Input
16	LD	Load DAC Register Strobe, active-high input that transfers the data bits from the serial-input register into the decoded DAC register. SDI and CLK inputs are disabled when LD is high. See Tables I and II
17	CLK	Serial Clock Input, positive edge triggered
18	SDO	Serial Data Output, active totem pole output
19	V_{SS}	Negative 5 V Power Supply
20	SDI	Serial Data Input
21	V_{DD}	Positive 5 V Power Supply
22	$V_{IN}D$	DAC D Reference Input
23	$V_{IN}C$	DAC C Reference Input
24	$V_{OUT}D$	DAC D Output

PIN CONFIGURATION

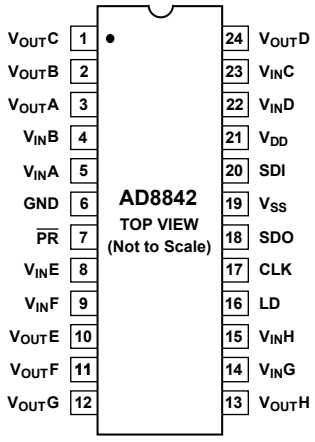


Table I. Serial Input Decode Table

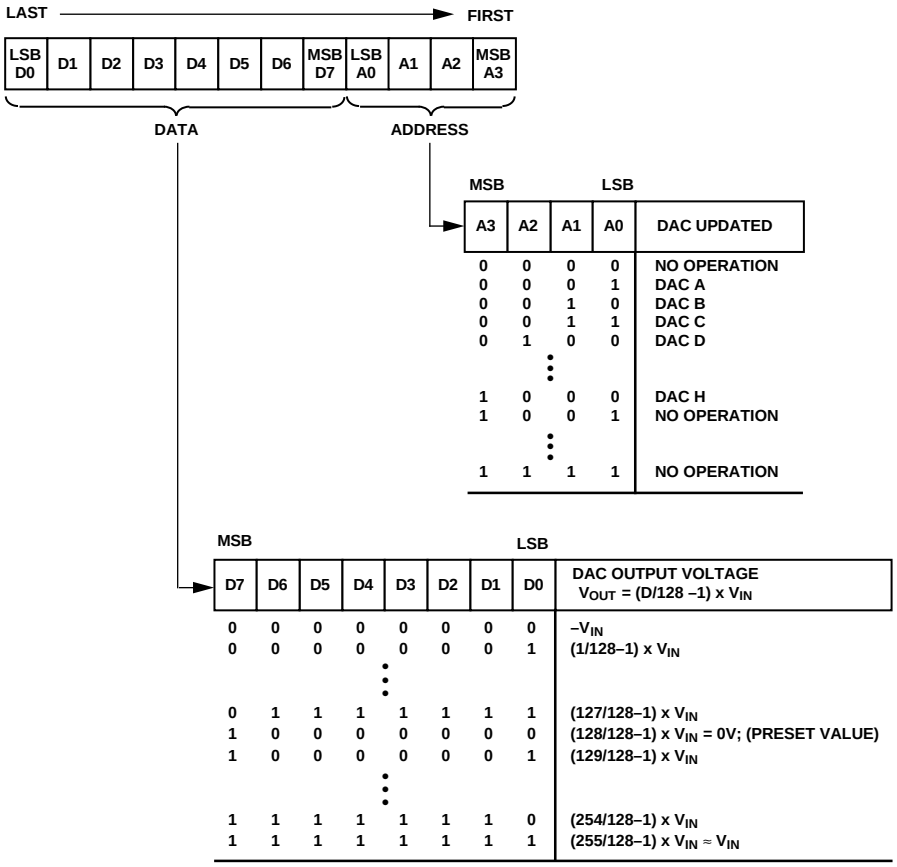


Table II. Input Logic Control Truth Table

CLK	LD	$\overline{PR}$	Input Shift Register Operation
L	L	H	No Operation
↑	L	H	Shift One Bit in from SDI (Pin 20), Shift One Bit* Out from SDO (Pin 18)
X	L	L	All DAC Registers = 80_H
X	H	H	Load Serial Register Data into DAC(X) Register
X	H	X	Serial Data Input Register Loading Disabled

*Data shifted into the SDI pin appears twelve clocks later at the SDO pin.

AD8842–Typical Performance Characteristics

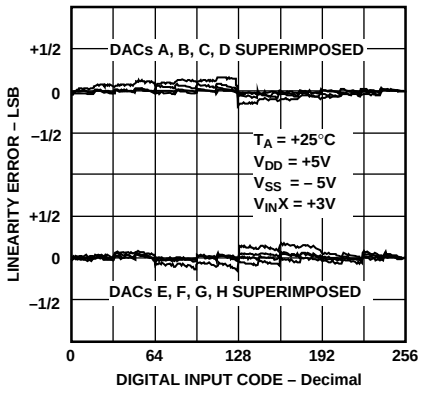


Figure 4. Linearity Error vs. Digital Code

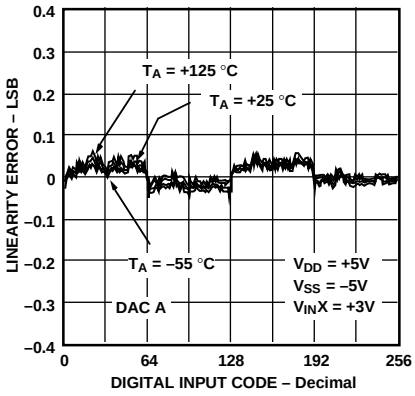


Figure 5. Linearity Error vs. Digital Code vs. Temperature

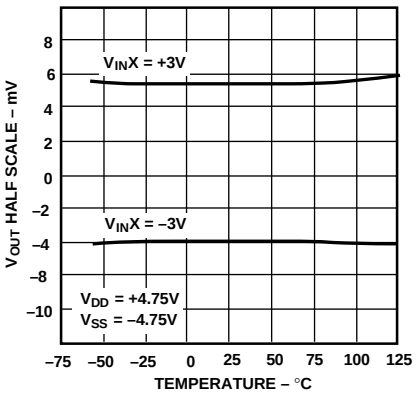


Figure 6. V_{OUT} Half Scale (80_H) vs. Temperature

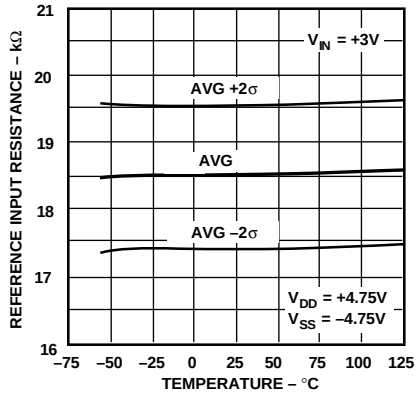


Figure 7. Input Resistance (V_{IN}) vs. Temperature

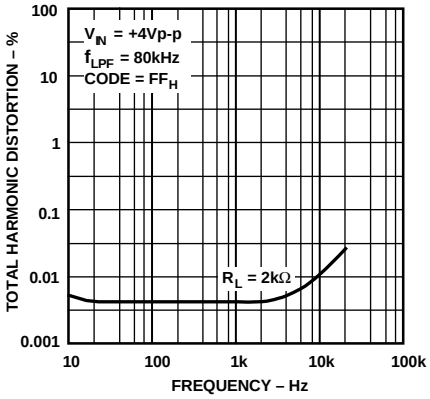


Figure 8. Total Harmonic Distortion vs. Frequency

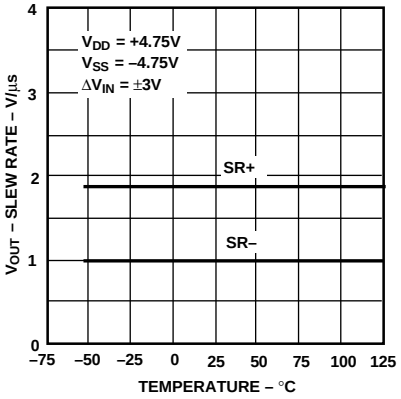


Figure 9. V_{OUT} Slew Rate vs. Temperature

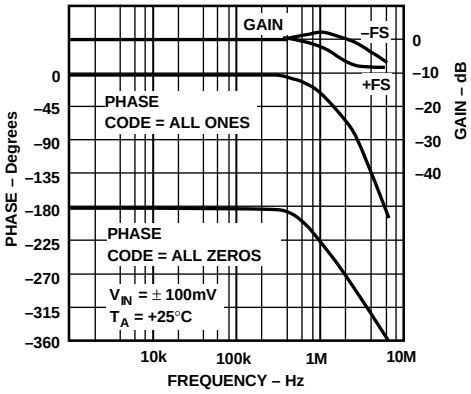


Figure 10. Gain and Phase vs. Frequency (Code = 00_H or FF_H)

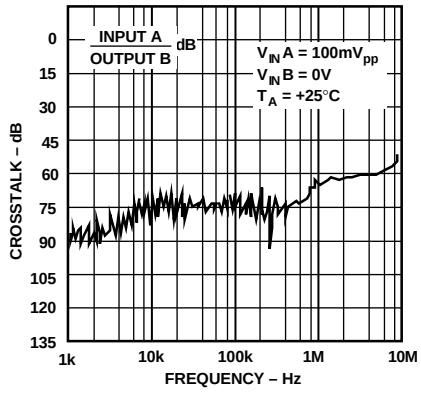


Figure 11. DAC Crosstalk vs. Frequency

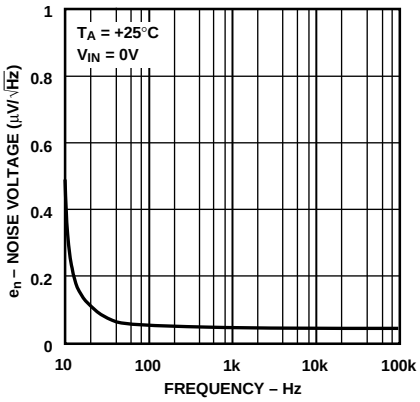


Figure 12. Voltage Noise Density vs. Frequency

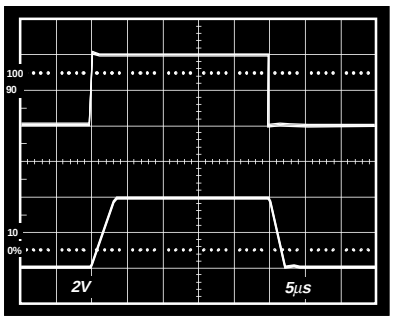


Figure 13. Pulse Response—Upper Trace V_{IN} @ 2 V/Div Lower Trace V_{OUT} @2 V/Div

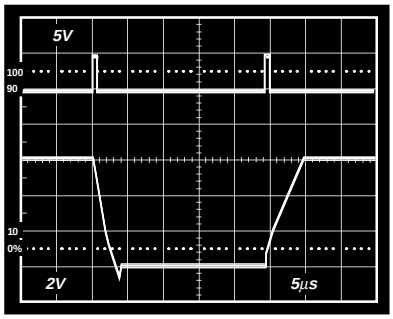


Figure 16. Settling Time—Upper Trace LD @ 5 V/Div, Lower Trace V_{OUT} @ 2 V/Div

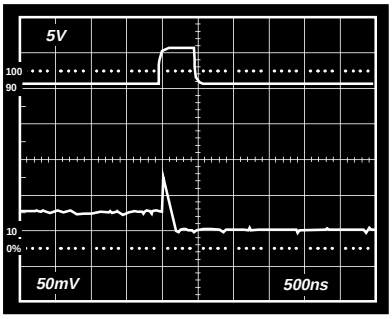


Figure 14. Worst Case 1 LSB Step Change Code 80_H to $7F_H$, Upper Trace LD @ 5 V/Div, Lower Trace V_{OUT} @ 50 mV/Div

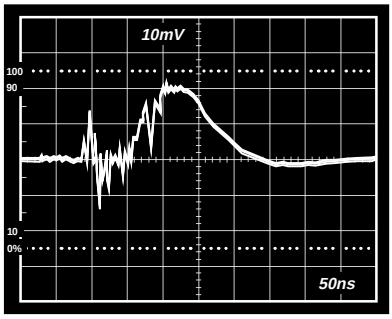


Figure 17. Digital Feedthrough—V_{OUT} @ 10 mV/Div, V_{IN} = 0 V; Code $7F_H$ to 80_H

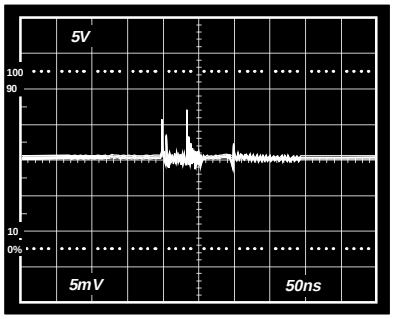


Figure 15. Crosstalk—V_{OUT} @ 5 mV/Div

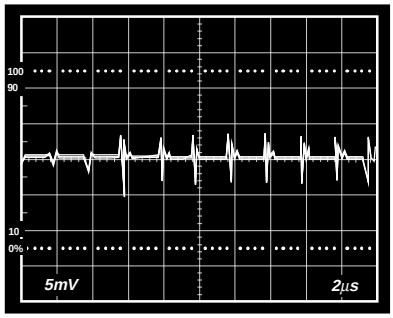


Figure 18. Clock Feedthrough—V_{OUT} @ 5 mV/Div

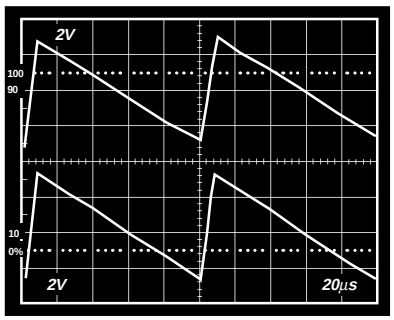


Figure 19. 10 kHz Sawtooth Waveform, Upper Trace V_{IN}, Lower Trace V_{OUT}

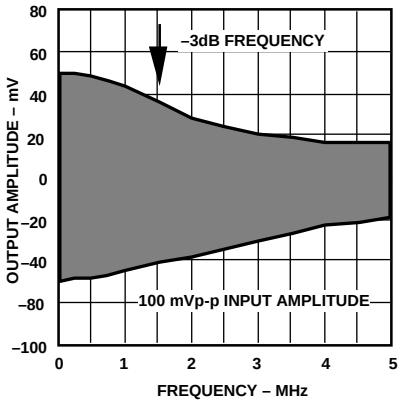


Figure 20. AC Sweep Frequency 100 mV p-p Amplitude Response

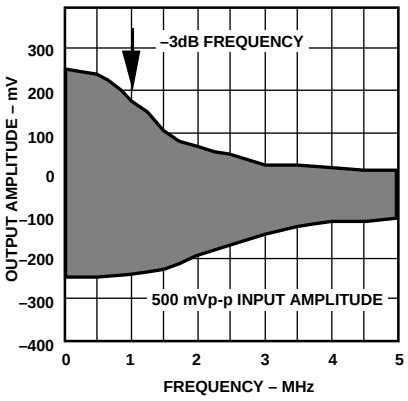


Figure 21. AC Sweep Frequency 500 mV p-p Amplitude Response

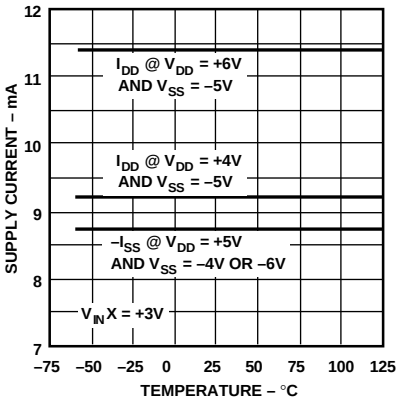


Figure 22. Supply Current vs. Voltage and Temperature

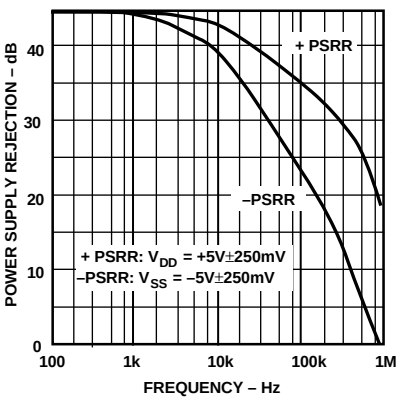


Figure 23. PSRR vs. Frequency

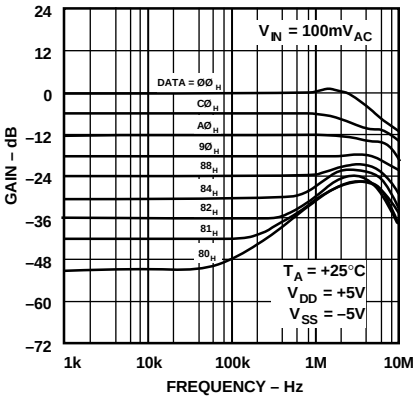


Figure 24. Gain (V_{OUT}/V_{IN}) and Feedthrough vs. Frequency

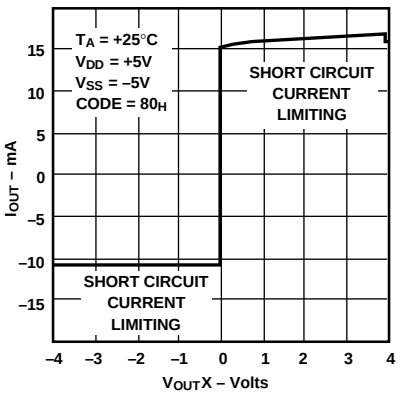


Figure 25. Short Circuit Limit Output Current vs. Voltage

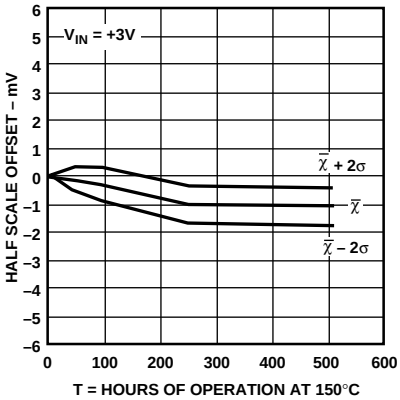
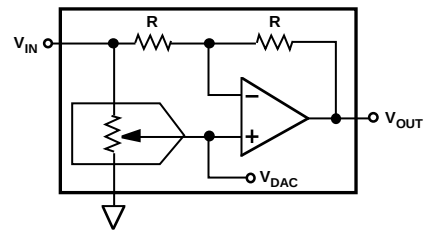


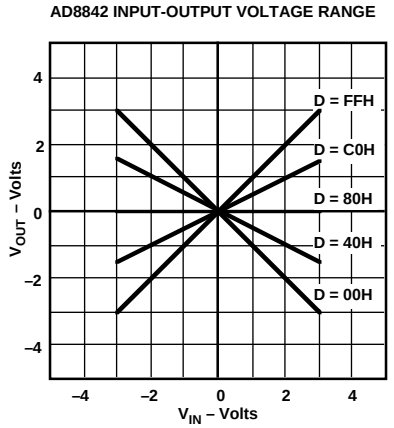
Figure 26. Output Voltage Drift Accelerated by Burn-In

CIRCUIT OPERATION

The AD8842 is a general purpose 8-channel ac or dc signal-level adjustment device designed to replace potentiometers used in the three-terminal connection mode. Eight independent channels of programmable signal level control are available in this 24-pin package device. The outputs are completely buffered providing up to 3 mA of output drive-current to drive external loads. The functional equivalent DAC and amplifier combination shown in Figure 27 produces four-quadrant multiplication of the signal inputs applied to V_{IN} times the digital input control word. In addition the AD8842 provides a 50 kHz full power bandwidth in each four-quadrant multiplying channel. Operating from plus and minus 5 V power supplies, analog inputs and outputs of ±3 V are easily accommodated.



$V_{DAC} = D/256 \times V_{IN}$
$V_{OUT} = 2 \times V_{DAC} - V_{IN}$
$= 2\ (D/256) \times V_{IN} - V_{IN}$
$= (D/128 - 1) \times V_{IN}$



$V_{OUT} = V_{IN}\ (D/128 - 1)$, WHERE D = 0 TO 255

Figure 27. Functional Equivalent Circuit to the AD8842 Results in a 4-Quadrant Multiplying Channel

In order to simplify use with a controlling microprocessor a PCB space saving three-wire serial data interface was chosen. This interface can be easily adapted to almost all microcomputer and microprocessor systems. A clock (CLK), serial data input (SDI) and a load (LD) strobe pins make up the three-wire interface. The 12-bit input data word used to change the value of the internal DAC registers contains a 4-bit address and 8-bits of data. Using this word combination any DAC register can be changed at a given time without disturbing the other channels. A serial data output SDO pin simplifies cascading multiple AD8842s without adding address decoder chips to the system.

During system power up a logic low on the preset $\overline{PR}$ pin forces all DAC registers to 80_H which in turn forces all the buffer amplifier outputs to zero volts. This asynchronous input pin $\overline{PR}$ can be activated at any time to force the DAC registers to the half-scale code 80_H. This is generally the most convenient place to start general purpose adjustment procedures.

Achieving 4-Quadrant Multiplying with a Current Conveyor Amplifier

The traditional current output CMOS digital-to-analog converter requires two amplifiers to perform the current-to-voltage translation and the half-scale offset to achieve four-quadrant multiplying capability. The circuit shown in Figure 28 shows one such traditional connection.

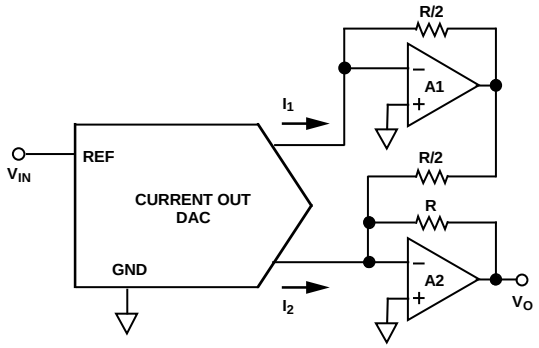


Figure 28. One Traditional Technique to Achieve Four-Quadrant Multiplying with a Complementary Current Output DAC

A single new current conveyor amplifier design emulates amplifiers A1 and A2 shown in Figure 28. Figure 29 shows the connection and equations that define this new circuit that achieves four-quadrant multiplication with only one amplifier.

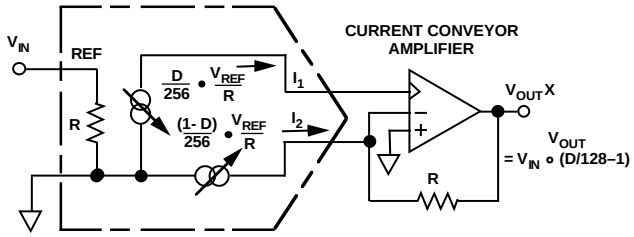


Figure 29. Current Conveyor Amplifier

Using the equations given in Figure 29 one can calculate the final output equation as follows:

$$V_O = -\left[\left(1 - \frac{D}{256}\right) \times \frac{V_{IN}}{R}\right] \times R - \left[\frac{-D}{256} \times \frac{V_{IN}}{R}\right] \times R$$

$$\left(\frac{D}{256} - 1\right) V_{IN} + \frac{D}{256} \times V_{IN}$$

$$= \left(\frac{2D}{256} - 1\right) V_{IN}$$

$$= \left(\frac{D}{128} - 1\right) V_{IN}$$

ADJUSTING AC OR DC SIGNAL LEVELS

The four-quadrant multiplication operation of the AD8842 is shown in Figure 27. For dc operation the equation describing the relationship between V_{IN}, digital inputs and V_{OUT} is:

$$V_{OUT}(D) = (D/128\text{-}1) \times V_{IN} \quad (1)$$

where D is a decimal number between 0 and 255

The actual output voltages generated with a fixed 3 V dc input applied to V_{IN} are summarized in this table.

Table III.

Decimal Input (D)	V_{OUT}(D)	Comments (V_{IN} = 3 V)
0	–3.00 V	Inverted FS
1	–2.98	
127	–0.02	
128	0.00	Zero Output
129	0.02	
254	2.95	
255	2.98	Full Scale (FS)

Notice that the output polarity is the same as the input polarity when the DAC register is loaded with 255 (in binary = all ones). Also note that the output does not exactly equal the input voltage. This is a result of the R-2R ladder DAC architecture chosen. When the DAC register is loaded with 0, the output polarity is inverted and exactly equals the magnitude of the input voltage V_{IN}. The actual voltage measured when setting up a DAC in this example will vary within the ±1 LSB linearity error specification of the AD8842. The calculated voltage error would be ±0.023 V (= ±3 V/128).

If V_{IN} is an ac signal such as a sine wave, then we can use Equation 2 to describe circuit performance.

$$V_{OUT}(t, D) = (D/128\text{-}1) \times A \sin(\omega t) \quad (2)$$

where $\omega = 2\pi f$, A = sine wave amplitude, and D = decimal input code.

This transfer characteristic Equation 2 lends itself to amplitude and phase control of the incoming signal V_{IN}. When the DAC is loaded with all zeros, the output sine wave is shifted by 180° with respect to the input sine wave. This powerful multiplying capability can be used for a wide variety of modulation, waveform adjustment and amplitude control.

SIGNAL INPUTS (V_{IN}A, B, C, D, E, F, G, H)

The eight independent V_{IN} inputs have a constant input-resistance nominal value of 19 kΩ as specified in the electrical characteristics table. These signal-inputs are designed to receive not only dc, but ac input voltages. The signal-input voltage range can operate to within one volt of either supply. That is, the operating input-voltage-range is:

$$V_{SS} + 1\ V < V_{IN}x < (V_{DD} - 1\ V) \quad (3)$$

DAC OUTPUTS (V_{OUT}A, B, C, D, E, F, G, H)

The eight D/A converter outputs are fully buffered by the AD8842's internal amplifier. This amplifier is designed to drive up to 1 kΩ loads in parallel with 100 pF. However, in order to minimize internal device power consumption, it is recommended whenever possible to use larger values of load resistance. The amplifier output stage can handle shorts to GND; however, care should be taken to avoid continuous short circuit operation.

The low output impedance of the buffers minimizes crosstalk between analog input channels. A graph (Figure 11) of analog crosstalk between channels is provided in the typical performance characteristics section. At 100 kHz 70 dB of channel-to-channel isolation exists. It is recommended to use good circuit layout practice such as guard traces between analog channels and power supply bypass capacitors. A 0.01 µF ceramic in parallel with a 1 µF–10 µF tantalum capacitor provides a good power supply bypass for most frequencies encountered.

DIGITAL INTERFACING

The four digital input pins (CLK, SDI, LD, PR) of the AD8842 were designed for TTL and 5 V CMOS logic compatibility. The SDO output pin offers good fanout in CMOS logic applications and can easily drive several AD8842s.

The Logic Contro Input Truth Table II describes how to shift data into the internal 12-bit serial input register. Note that the CLK is a positive-edge sensitive input. If mechanical switches are used for breadboard evaluation, they should be debounced by a flipflop or other suitable means. The basic three-wire serial data interface setup is shown in Figure 30.

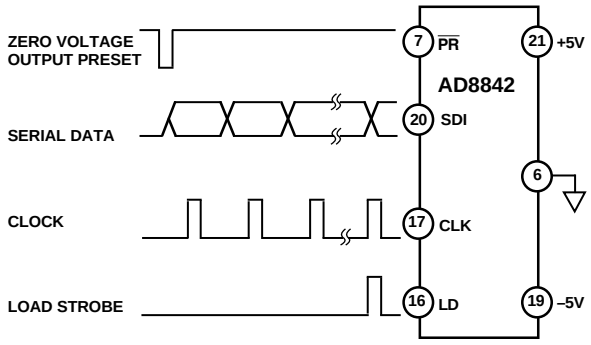


Figure 30. Basic Three-Wire Serial Interface

The required address plus data input format is defined in the serial input decode Table I. Note there are 8 address states that result in no operation (NOP) or activity in the AD8842 when the positive edge triggered load-strobe (LD) is activated. This NOP can be used in cascaded applications where only one DAC out of several packages needs updating. The packages not requiring data changes would receive the NOP address, that is, all zeros. It takes 12 clocks on the CLK pin to fully load the serial-input shift-register. Data on the SDI input pin is subject to the timing diagram (Figure 3) data setup and data hold time requirements. After the twelfth clock pulse the processor needs to activate the LD strobe to have the AD8842 decode the serial-register contents and update the target DAC register with the 8-bit data word. This needs to be done before the thirteenth positive clock edge. The timing requirements are provided in the electrical characteristic table and in the Figure 3 timing diagram. After twelve clock edges, data initially loaded into the shift register at SDI appears at the shift register output SDO. A multiple package interface circuit is shown in Figure 31. In this topology all the devices are clocked with the new data; however, only the decoded package address signal updates the target package LD strobe which is being used as a chip select.

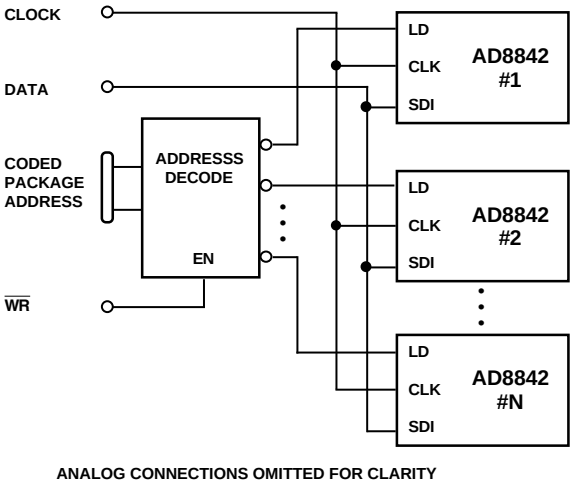


Figure 31. Addressing Multiple AD8842 Packages

There is some digital feedthrough from the digital input pins. Operating the clock only when the DAC registers require updating minimizes the effect of the digital feedthrough on the analog signal channels. Measurements of DAC switch feedthrough shown in the electrical characteristics table were accomplished by grounding the $V_{IN}x$ inputs and cycling the data codes between all zeros and all ones. Under this condition 5 nV-s of feedthrough was measured on the output of the switched DAC channel. An adjacent channel measured less than 1 nV-s of digital crosstalk. The digital feedthrough and crosstalk photographs shown in the typical performance characteristics section display these characteristics (Figures 15 and 17).

Figure 32 shows a three-wire interface for a single AD8842 that easily cascades for multiple packages. This circuit topology often called daisy chaining requires preformating all the serial data for each package in the chain. In the case of the 3 packages shown a 36 bit data word must be completely clocked into all the AD8842 serial data input registers then the LD strobe would transfer the data bits into the DAC registers updating one DAC in each package.

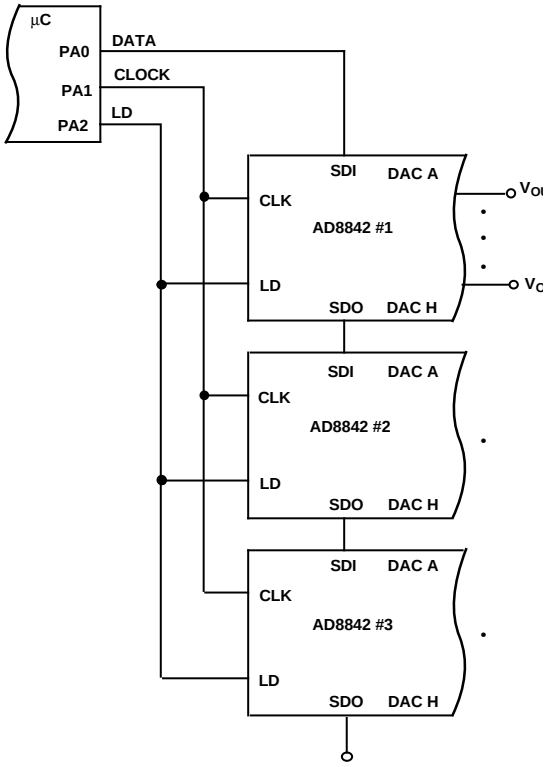
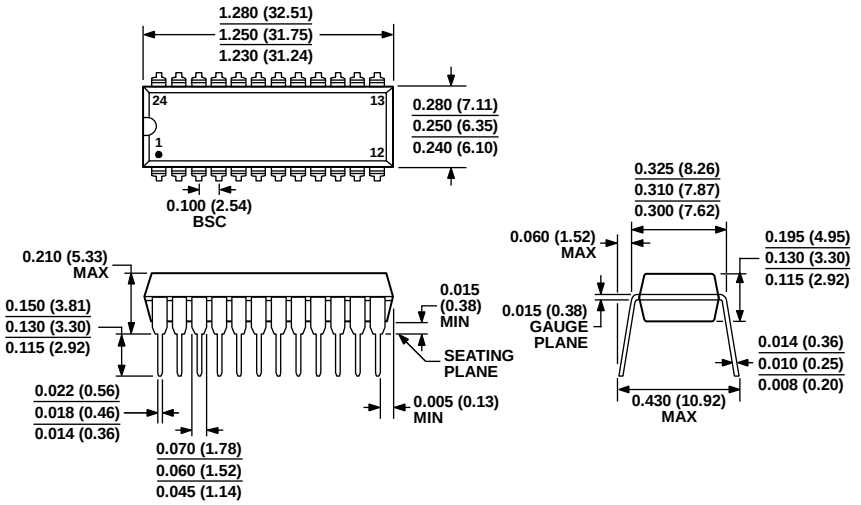


Figure 32. Three-Wire Interface Updates Multiple AD8842s

OUTLINE DIMENSIONS

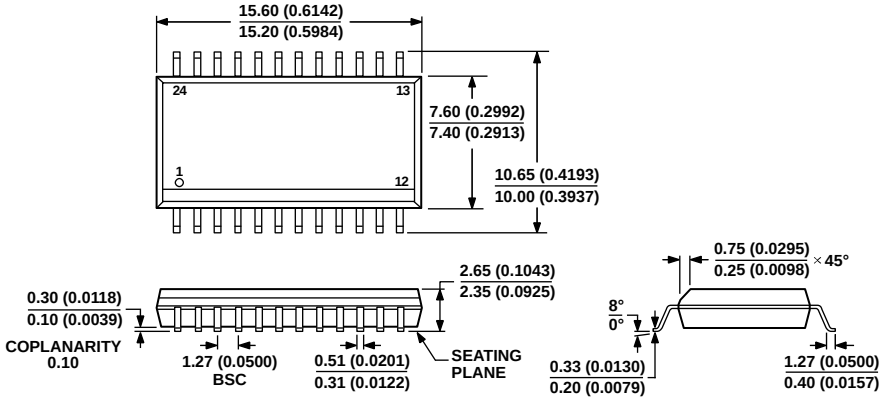


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071006-A

Figure 33. 24-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-24-1)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013-AD

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12-09-2010-A

Figure 34. 24-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-24)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8842AN	−40°C to +85°C	24-Lead PDIP	N-24-1
AD8842ANZ	−40°C to +85°C	24-Lead PDIP	N-24-1
AD8842AR	−40°C to +85°C	24-Lead SOIC_W	RW-24
AD8842AR-REEL	−40°C to +85°C	24-Lead SOIC_W	RW-24
AD8842ARZ	−40°C to +85°C	24-Lead SOIC_W	RW-24
AD8842ARZ-REEL	−40°C to +85°C	24-Lead SOIC_W	RW-24

[1] Z = RoHS Compliant Part.

REVISION HISTORY

10/11—Rev. 0 to Rev. A

Changes to Pin 13 Mnemonic 4
Updated Outline Dimensions 12
Changes to Ordering Guide 13

4/94—Revision 0: Initial Version

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