GENERAL DESCRIPTION

The XR16V794[1] (794), is a 2.25V to 3.6V octal Universal Asynchronous Receiver and Transmitter (UART) with 5V tolerant serial (modem) inputs. The highly integrated device is designed for high bandwidth requirement in communication systems. The global interrupt source register provides a complete interrupt status indication for all 4 channels to speed up interrupt parsing. Each UART has its own 16C550 compatible set of configuration registers, TX and RX FIFOs of 64 bytes, fully programmable transmit and receive FIFO trigger levels, TX and RX FIFO level counters, automatic RTS/CTS or DTR/DSR hardware flow control with programmable hysteresis, autoamtic software (Xon/Xoff) flow control, RS-485 half-duplex direction control with programmable turn-around delay, Intel or Motorola bus interface and sleep mode with a wake-up indicator.

NOTE: *Covered by US patents #5,649,122 and #5,949,787*

APPLICATIONS

- Remote Access Servers
- Ethernet Network to Serial Ports
- Network Management
- Factory Automation and Process Control
- Point-of-Sale Systems
- Multi-port RS-232/RS-422/RS-485 Cards

FEATURES

- 2.25V to 3.6V with 5V Tolerant Serial Inputs
- Single Interrupt output for all 4 UARTs
- A Global Interrupt Source Register for all 4 UARTs
- 5G “Flat” UART Registers for easier programming
- Simultaneous Initialization of all UART channels
- **A General Purpose Command-driven 16-bit Timer/counter**
- Sleep Mode with Wake-up Indication
- Highly Integrated Device for Space Saving
- Each UART is independently controlled with:
  - 16C550 Compatible 5G Register Set
  - 64-byte Transmit and Receive FIFOs
  - **Fractional Baud Rate Generator**
  - Transmit and Receive FIFO Level Counters
  - Programmable TX and RX FIFO Trigger Level
  - Automatic RTS/CTS or DTR/DSR Flow Control
  - Automatic Xon/Xoff Software Flow Control
  - RS485 Half-Duplex Control Output with Selectable Turn-around Delay
  - Infrared (IrDA 1.0) Data Encoder/Decoder
  - Programmable Data Rate with Prescaler
- Up to 8 Mbps Serial Data Rate
- Pin compatible to XR16L784. Same 64-pin LQFP Package (10x10x1.4 mm)

FIGURE 1. BLOCK DIAGRAM

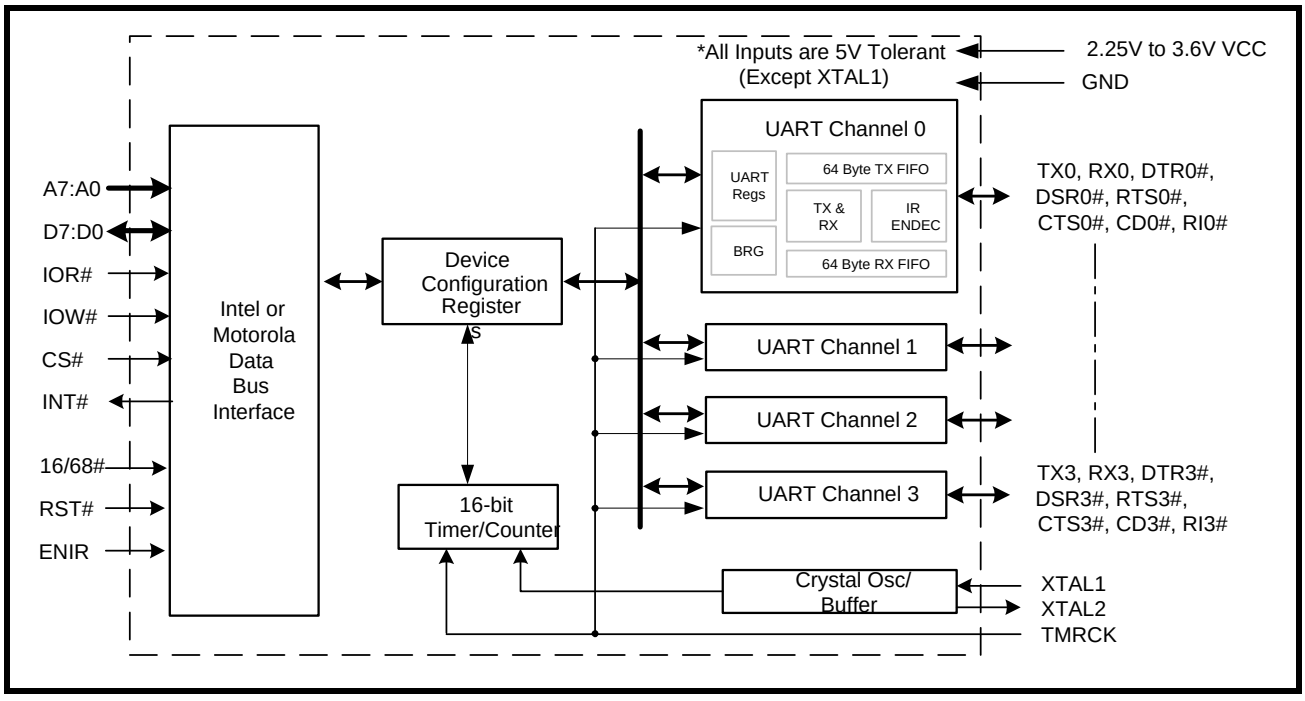
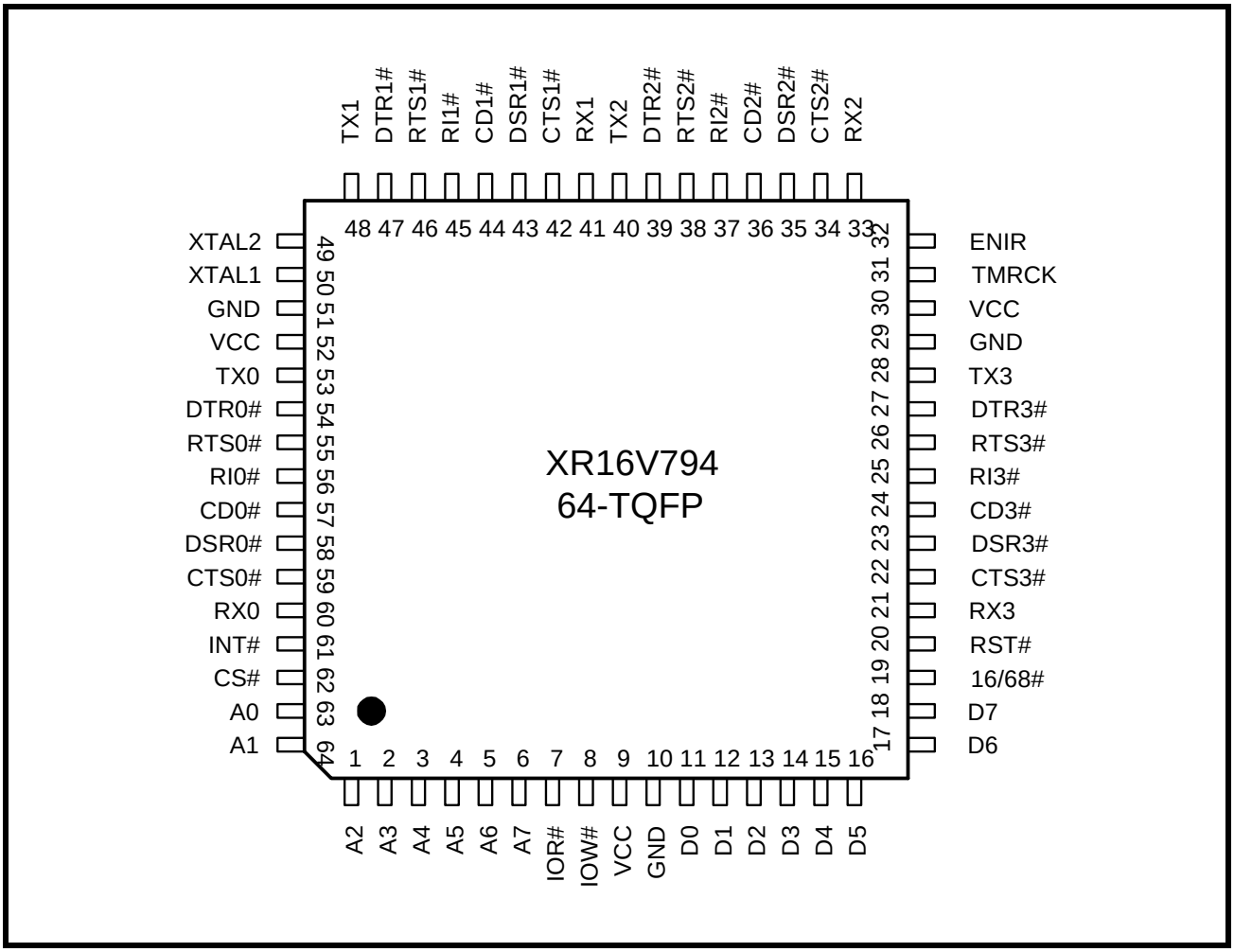


FIGURE 2. PIN OUT OF THE DEVICE



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR16V794IV	64-Lead LQFP	-40°C to +85°C	Active

PIN DESCRIPTIONS

NAME	PIN #	TYPE	DESCRIPTION
DATA BUS INTERFACE			
A7-A0	6-1,64,63	I	Address data lines [7:0]. A0:A3 selects individual UART's 16 configuration registers, A4:A6 selects UART channel 0 to 3, and A7 selects the global device configuration registers
D7:D0	18-11	IO	Data bus lines [7:0] (bidirectional).
IOR#	7	I	When 16/68# pin is HIGH, it selects Intel bus interface and this input is read strobe (active low). The falling edge instigates an internal read cycle and retrieves the data byte from an internal register pointed by the address lines [A7:A0], puts it on the data bus to allow the host processor to read it on the leading edge. When 16/68# pin is LOW, it selects Motorola bus interface and this input should be connected to VCC.
IOW# (R/W#)	8	I	When 16/68# pin is HIGH, it selects Intel bus interface and this input becomes write strobe (active low). The falling edge instigates the internal write cycle and the leading edge transfers the data byte on the data bus to an internal register pointed by the address lines. When 16/68# pin is LOW, it selects Motorola bus interface and this input becomes read (logic 1) and write (logic 0) signal.
CS#	62	I	When 16/68# pin is HIGH, this input is chip select (active low) to enable the XR16V794 device. When 16/68# pin is LOW, this input becomes the read and write strobe (active low) for the Motorola bus interface.
INT#	61	OD	Global interrupt output from XR16V794 (open drain, active low). This output requires an external pull-up resistor (47K-100K ohms) to operate properly. It may be shared with other devices in the system to form a single interrupt line to the host processor and have the software driver polls each device for the interrupt status.
MODEM OR SERIAL I/O INTERFACE			
TX0	53	O	UART channel 0 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX0	60	I	UART channel 0 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via FCTR bit-4. If this bit is a logic 0, a LOW on the RXD input is considered a mark and if this bit is a logic 1, a HIGH on the RXD input is considered a space.
RTS0#	55	O	UART channel 0 Request to Send or general purpose output (active low). This port must be asserted prior using for one of two functions: 1) auto RTS flow control, see EFR bit-6, MCR bits-1 & 2, FCTR bits 0-3 and IER bit-6 2) Auto RS485 half-duplex direction control, see FCTR bit-5, MCR bit-2 and MSR bits 4-7.
CTS0#	59	I	UART channel 0 Clear to Send or general purpose input (active low). It can be used for auto CTS flow control, see EFR bit-7, MCR bit-2 and IER bit-7.

NAME	PIN #	TYPE	DESCRIPTION
DTR0#	54	O	UART channel 0 Data Terminal Ready or general purpose output (active low). This port must be asserted prior using for one of two functions: 1) auto DTR flow control, see EFR bit-6, FCTR bits-0 to 3, MCR bits-0 & 2, and IER bit-6 2) Auto RS485 half-duplex direction control, see FCTR bit-5, MCR bit-2 and MSR bit 4-7.
DSR0#	58	I	UART channel 0 Data Set Ready or general purpose input (active low). It can be used for auto DSR flow control, see EFR bit-7, MCR bit-2 and IER bit-7.
CD0#	57	I	UART channel 0 Carrier Detect or general purpose input (active low).
RI0#	56	I	UART channel 0 Ring Indicator or general purpose input (active low).
TX1	48	O	UART channel 1 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX1	41	I	UART channel 1 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via FCTR bit-4. If this bit is a logic 0, a LOW on the RXD input is considered a mark and if this bit is a logic 1, a HIGH on the RXD input is considered a space.
RTS1#	46	O	UART channel 1 Request to Send or general purpose output (active low). See description of RTS0# pin.
CTS1#	42	I	UART channel 1 Clear to Send or general purpose input (active low). See description of CTS0# pin.
DTR1#	47	O	UART channel 1 Data Terminal Ready or general purpose output (active low). See description of DTS0# pin.
DSR1#	43	I	UART channel 1 Data Set Ready or general purpose input (active low). See description of DSR0# pin.
CD1#	44	I	UART channel 1 Carrier Detect or general purpose input (active low).
RI1#	45	I	UART channel 1 Ring Indicator or general purpose input (active low).
TX2	40	O	UART channel 2 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX2	33	I	UART channel 2 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via FCTR bit-4. If this bit is a logic 0, a LOW on the RXD input is considered a mark and if this bit is a logic 1, a HIGH on the RXD input is considered a space.
RTS2#	38	O	UART channel 2 Request to Send or general purpose output (active low). See description of RTS0# pin.
CTS2#	34	I	UART channel 2 Clear to Send or general purpose input (active low). See description of CTS0# pin.
DTR2#	39	O	UART channel 2 Data Terminal Ready or general purpose output (active low). See description of DTS0# pin.
DSR2#	35	I	UART channel 2 Data Set Ready or general purpose input (active low). See description of DSR0# pin.
CD2#	36	I	UART channel 2 Carrier Detect or general purpose input (active low).
RI2#	37	I	UART channel 2 Ring Indicator or general purpose intput (active low).

NAME	PIN #	TYPE	DESCRIPTION
TX3	28	O	UART channel 3 Transmit Data or infrared transmit data. Normal TXD output idles HIGH while infrared TXD output idles LOW.
RX3	21	I	UART channel 3 Receive Data or infrared receive data. Normal RXD input idles HIGH while infrared RXD input idles LOW. In the infrared mode, the polarity of the incoming RXD signal can be selected via FCTR bit-4. If this bit is a logic 0, a LOW on the RXD input is considered a mark and if this bit is a logic 1, a HIGH on the RXD input is considered a space.
RTS3#	26	O	UART channel 3 Request to Send or general purpose output (active low). See description of RTS0# pin.
CTS3#	22	I	UART channel 3 Clear to Send or general purpose input (active low).d. See description of CTS0# pin.
DTR3#	27	O	UART channel 3 Data Terminal Ready or general purpose output (active low). See description of DTS0# pin.
DSR3#	23	I	UART channel 3 Data Set Ready or general purpose input (active low). See description of DSR0# pin.
CD3#	24	I	UART channel 3 Carrier Detect or general purpose input (active low).
RI3#	25	I	UART channel 3 Ring Indicator or general purpose input (active low).
ANCILLARY SIGNALS			
XTAL1	50	I	Crystal or external clock input. Caution: this input is not 5V tolerant.
XTAL2	49	O	Crystal or buffered clock output.
TMRCK	31	I	16-bit timer/counter external clock input.
ENIR	32	I	Infrared mode enable (active high). This pin is sampled during power up, following a hardware reset (RST#) or soft-reset (register RESET). It can be used to start up all 4 UARTs in the infrared mode. The sampled logic state is transferred to MCR bit-6 in the UART.
RST#	20	I	Reset (active low). The configuration and UART registers are reset to default values, see **Table 19**.
16/68#	19	I	Intel or Motorola data bus interface select. HIGH selects Intel bus interface and LOW selects Motorola interface. This input affects the functionality of IOR#, IOW# and CS# pins.
VCC	9,30,52		+2.25V to 3.6V supply with 5V tolerant serial (modem) inputs.
GND	10,29,51		Power supply common, ground.

NOTE: *Pin type: I=Input, O=Output, IO= Input/output, OD=Output Open Drain.*

1.0 DESCRIPTION

The XR16V794 (794) integrates the functions of 4 enhanced 16550 UARTs, a general purpose 16-bit timer/counter and an on-chip oscillator. The device configuration registers include a set of four consecutive interrupt source registers that provides interrupt-status for all 4 UARTs, timer/counter and a sleep wake up indicator. Each UART channel has its own 16550 UART compatible configuration register set for individual channel control, status, and data transfer. Additionally, each UART channel has 64-byte of transmit and receive FIFOs, automatic RTS/CTS or DTR/DSR hardware flow control with hysteresis control, automatic Xon/Xoff and special character software flow control, programmable transmit and receive FIFO trigger levels, FIFO level counters, infrared encoder and decoder (IrDA ver. 1.0), programmable baud rate generator with a prescaler of divide by 1 or 4, and data rate up to 8Mbps with 8X sampling clock or 4Mbps with 16X sampling clock. The XR16V794 is a 2.25-3.6V device with 5 volt tolerant inputs (except XTAL1).

2.0 FUNCTIONAL DESCRIPTIONS

2.1 Device Reset

2.1.1 Hardware Reset

The RST# input resets the internal registers and the serial interface outputs in all 4 channels to their default state (see **Table 19**). A LOW pulse of longer than 40 ns duration will be required to activate the reset function in the device.

2.1.2 Software Reset

The internal registers of each UART can be reset by writing to the RESET register in the Device Configuration Registers. For more details, see the RESET register description on **page 24**.

2.2 UART Channel Selection

A LOW on the chip select pin, CS#, allows the user to select one of the UART channels to configure, send transmit data and/or unload receive data to/from the UART. When address line A7 = 0, address lines A6:A4 are used to select one of the eight channels. See **Table 1** below for UART channel selection.

TABLE 1: UART CHANNEL SELECTION

A7	A6	A5	A4	FUNCTION
0	0	0	0	Channel 0 Selected
0	0	0	1	Channel 1 Selected
0	0	1	0	Channel 2 Selected
0	0	1	1	Channel 3 Selected

2.3 Simultaneous Write to All Channels

During a write cycle, the setting of the Device Configuration register REGB (**See Table 8**) bit-0 to a logic 1 will override the channel selection of address A6:A4 and allow a simultaneous write to all 4 UART channels when any channel is written to. This functional capability allow the registers in all 4 UART channels to be modified concurrently, saving individual channel initialization time. Caution should be considered, however, when using this capability. Any in-process serial data transfer may be disrupted by changing an active channel's mode. Also, REGB bit-0 should be reset to a logic 0 before attempting to read from the UART.

2.4 INT# Ouput

The INT# interrupt output changes according to the operating mode and enhanced features setup. **Table 2 and 3** summarize the operating behavior for the transmitter and receiver.

TABLE 2: INT# PIN OPERATION FOR TRANSMITTER

Auto RS485 Mode	FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
NO	HIGH = a byte in THR LOW = THR empty	HIGH = FIFO above trigger level LOW = FIFO below trigger level or FIFO empty
YES	HIGH = a byte in THR LOW = transmitter empty	HIGH = FIFO above trigger level LOW = FIFO below trigger level or transmitter empty

TABLE 3: INT# PIN OPERATION FOR RECEIVER

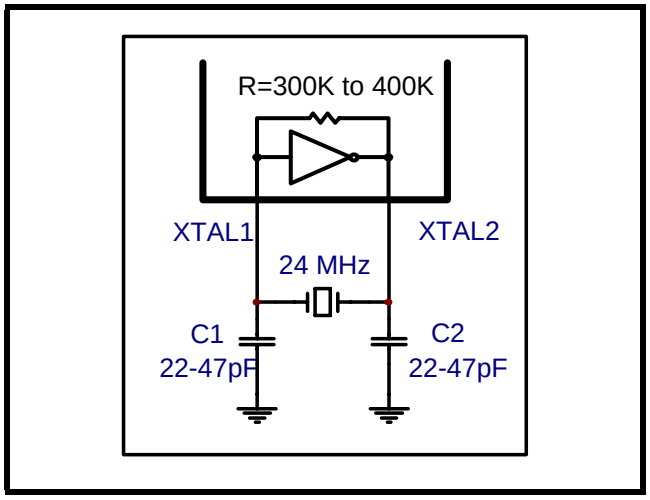
FCR BIT-0 = 0 (FIFO DISABLED)	FCR BIT-0 = 1 (FIFO ENABLED)
HIGH = no data LOW = 1 byte	HIGH = FIFO below trigger level LOW = FIFO above trigger level

2.5 CRYSTAL OSCILLATOR / BUFFER

The 794 includes an on-chip oscillator. The crystal oscillator provides the system clock to the Baud Rate Generators (BRG) in each of the 4 UARTs, the 16-bit general purpose timer/counter and internal logics. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. For programming details, see **"Section 2.6, Programmable Baud Rate Generator with Fractional Divisor" on page 8**.

The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant, fundamental frequency with 10-22 pF capacitance load, ESR of 20-120 ohms and 100ppm frequency tolerance) connected externally between the XTAL1 and XTAL2 pins (see **Figure 3**). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal 4 baud rate generators for standard or custom rates. The typical oscillator connections are shown in **Figure 3**. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

FIGURE 3. TYPICAL OSCILLATOR CONNECTIONS



2.6 Programmable Baud Rate Generator with Fractional Divisor

Each UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter and receiver. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The output of the prescaler clocks to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (216 - 0.0625) in increments of 0.0625 (1/16) to obtain a 16X or 8X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL, DLM and DLD registers) defaults to the value of '1' (DLL = 0x01, DLM = 0x00 and DLD = 0x00) upon reset. Therefore, the BRG must be programmed during initialization to the operating data rate. The DLL and DLM registers provide the integer part of the divisor and the DLD register provides the fractional part of the dvisior. Only the four lower bits of the DLD are implemented and they are used to select a value from 0 (for setting 0000) to 0.9375 or 15/16 (for setting 1111). Programming the Baud Rate Generator Registers DLL, DLM and DLD provides the capability for selecting the operating data rate. **Table 4** shows the standard data rates available with a 24MHz crystal or external clock at 16X clock rate. If the pre-scaler is used (MCR bit-7 = 1), the output data rate will be 4 times less than that shown in **Table 4**. At 8X sampling rate, these data rates would double. Also, when using 8X sampling mode, please note that the bit-time will have a jitter (+/- 1/16) whenever the DLD is non-zero and is an odd number. When using a non-standard data rate crystal or external clock, the divisor value can be calculated with the following equation(s):

Required Divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16), **WITH 8XMODE [7:0] IS 0**
Required Divisor (decimal) = (XTAL1 clock frequency / prescaler / (serial data rate x 8), **WITH 8XMODE [7:0] IS 1**

The closest divisor that is obtainable in the 794 can be calculated using the following formula:

ROUND((Required Divisor - TRUNC(Required Divisor))*16)/16 + TRUNC(Required Divisor), where

DLM = TRUNC(Required Divisor) >> 8
DLL = TRUNC(Required Divisor) & 0xFF
DLD = ROUND((Required Divisor-TRUNC(Required Divisor))*16)

In the formulas above, please note that:

TRUNC (N) = Integer Part of N. For example, TRUNC (5.6) = 5.

ROUND (N) = N rounded towards the closest integer. For example, ROUND (7.3) = 7 and ROUND (9.9) = 10.

A >> B indicates right shifting the value 'A' by 'B' number of bits. For example, 0x78A3 >> 8 = 0x0078.

FIGURE 4. BAUD RATE GENERATOR

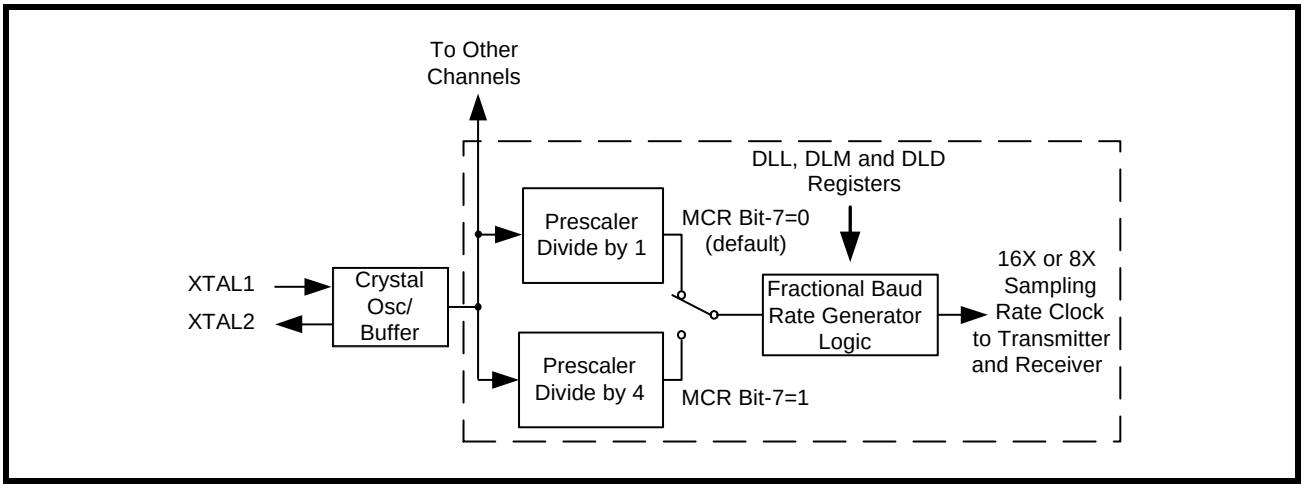


TABLE 4: TYPICAL DATA RATES WITH A 24 MHZ CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING

Required Output Data Rate	DIVISOR FOR 16x Clock (Decimal)	DIVISOR OBTAINABLE IN 794	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DLD PROGRAM VALUE (HEX))	DATA ERROR RATE (%)
400	3750	3750	E	A6	0	0
2400	625	625	2	71	0	0
4800	312.5	312 8/16	1	38	8	0
9600	156.25	156 4/16	0	9C	4	0
10000	150	150	0	96	0	0
19200	78.125	78 2/16	0	4E	2	0
25000	60	60	0	3C	0	0
28800	52.0833	52 1/16	0	34	1	0.04
38400	39.0625	39 1/16	0	27	1	0
50000	30	30	0	1E	0	0
57600	26.0417	26 1/16	0	1A	1	0.08
75000	20	20	0	14	0	0
100000	15	15	0	F	0	0
115200	13.0208	13	0	D	0	0.16
153600	9.7656	9 12/16	0	9	C	0.16
200000	7.5	7 8/16	0	7	8	0
225000	6.6667	6 11/16	0	6	B	0.31
230400	6.5104	6 8/16	0	6	8	0.16
250000	6	6	0	6	0	0
300000	5	5	0	5	0	0
400000	3.75	3 12/16	0	3	C	0
460800	3.2552	3 4/16	0	3	4	0.16
500000	3	3	0	3	0	0
750000	2	2	0	2	0	0
921600	1.6276	1 10/16	0	1	A	0.16
1000000	1.5	1 8/16	0	1	8	0

2.7 Transmitter

The transmitter section comprises of an 8-bit Transmit Shift Register (TSR) and 64 bytes of FIFO which includes a byte-wide Transmit Holding Register (THR). TSR shifts out every data bit with the 16X or 8X (if 8X sampling is selected via the **8XMODE Register**) internal clock. A bit time is 16 (or 8) clock periods. The transmitter sends the start-bit followed by the number of data bits, inserts the proper parity-bit if enabled, and adds the stop-bit(s). The status of the FIFO and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

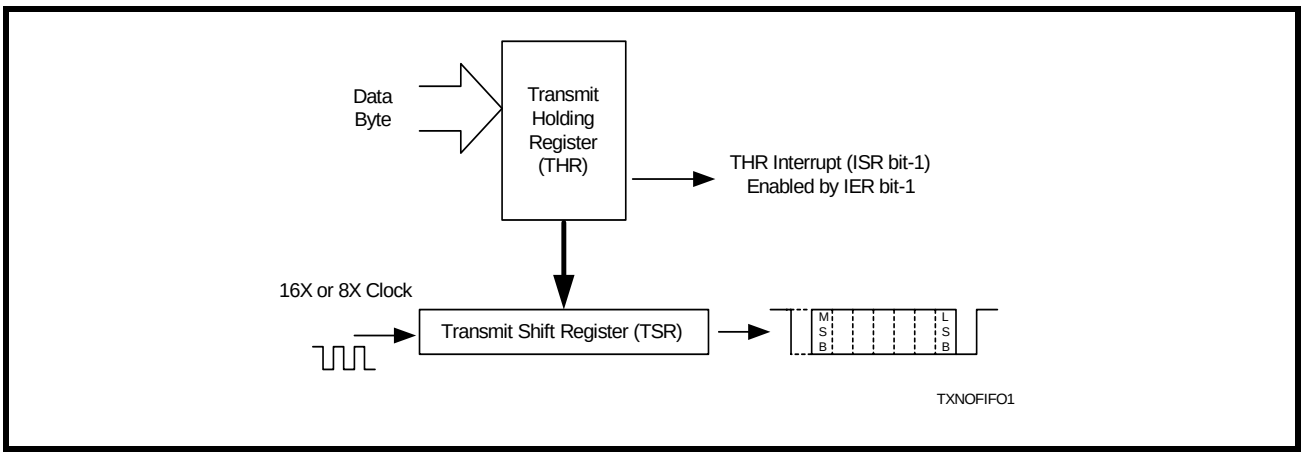
2.7.1 Transmit Holding Register (THR) - Write Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (Bit-0) becomes first data bit to go out. The THR is the input register to the transmit FIFO of 64 bytes when FIFO operation is enabled by FCR bit-0. Every time a write operation is made to the THR, the FIFO data pointer is automatically bumped to the next sequential data location.

2.7.2 Transmitter Operation in non-FIFO Mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

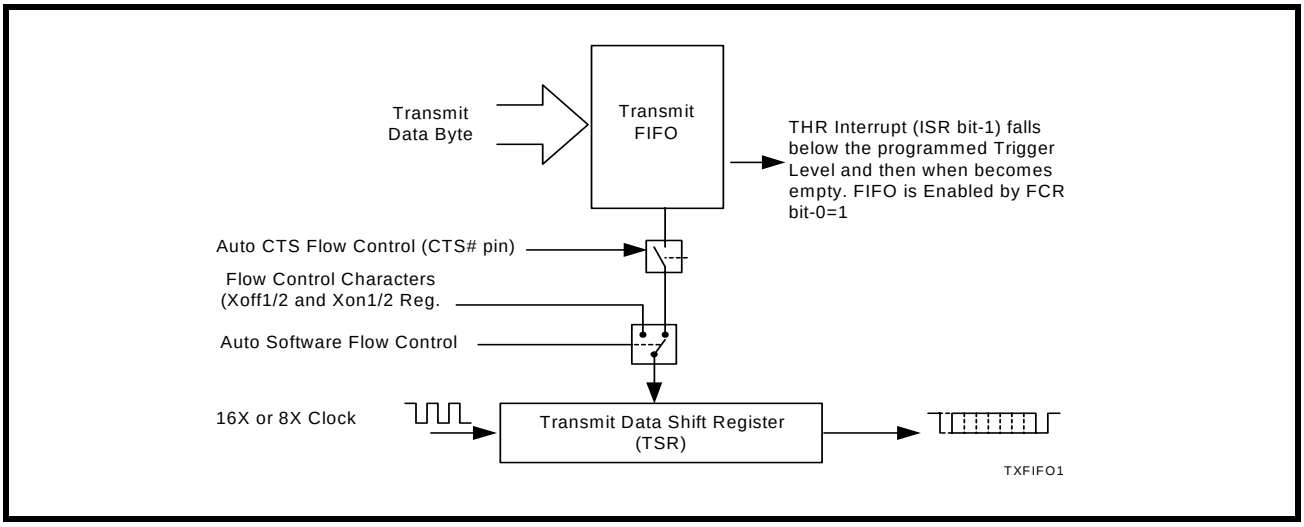
FIGURE 5. TRANSMITTER OPERATION IN NON-FIFO MODE



2.7.3 Transmitter Operation in FIFO Mode

The host may fill the transmit FIFO with up to 64 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The THR empty flag can generate a transmit empty interrupt (ISR bit-1) when the amount of data in the FIFO falls below its programmed trigger level. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR/FIFO becomes empty.

FIGURE 6. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



2.8 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and 64 bytes of FIFO which includes a byte-wide Receive Holding Register (RHR). The RSR uses the 16X (or the 8X) clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting the number of 16X (or 8X) clocks. After 8 (or 4) clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 2-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error tags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out interrupt when data is not received for 4 word lengths as defined by LCR[1:0] plus 12 bits time. This is equivalent to 3.7-4.6 character times. The RHR interrupt is enabled by IER bit-0.

2.8.1 Receive Holding Register (RHR) - Read-Only

The Receive Holding Register is an 8-bit register that holds a receive data byte from the Receive Shift Register. It provides the receive data interface to the host processor. The RHR register is part of the receive FIFO of 64 bytes by 11-bits wide, the 3 extra bits are for the 3 error tags to be reported in LSR register. When the FIFO is enabled by FCR bit-0, the RHR contains the first data character received by the FIFO. After the RHR is read, the next character byte is loaded into the RHR and the errors associated with the current data byte are immediately updated in the LSR bits 2-4.

FIGURE 7. RECEIVER OPERATION IN NON-FIFO MODE

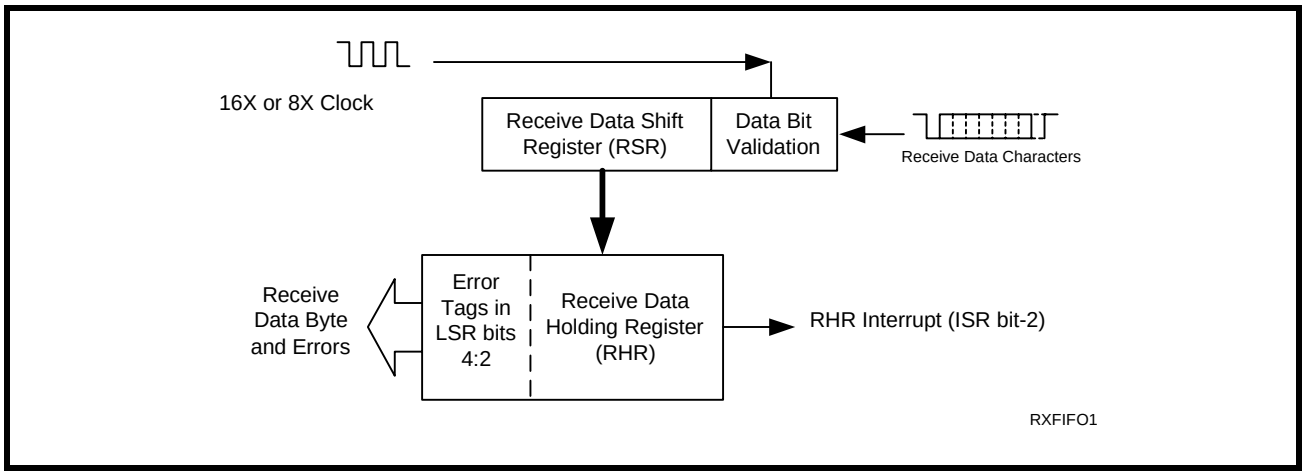
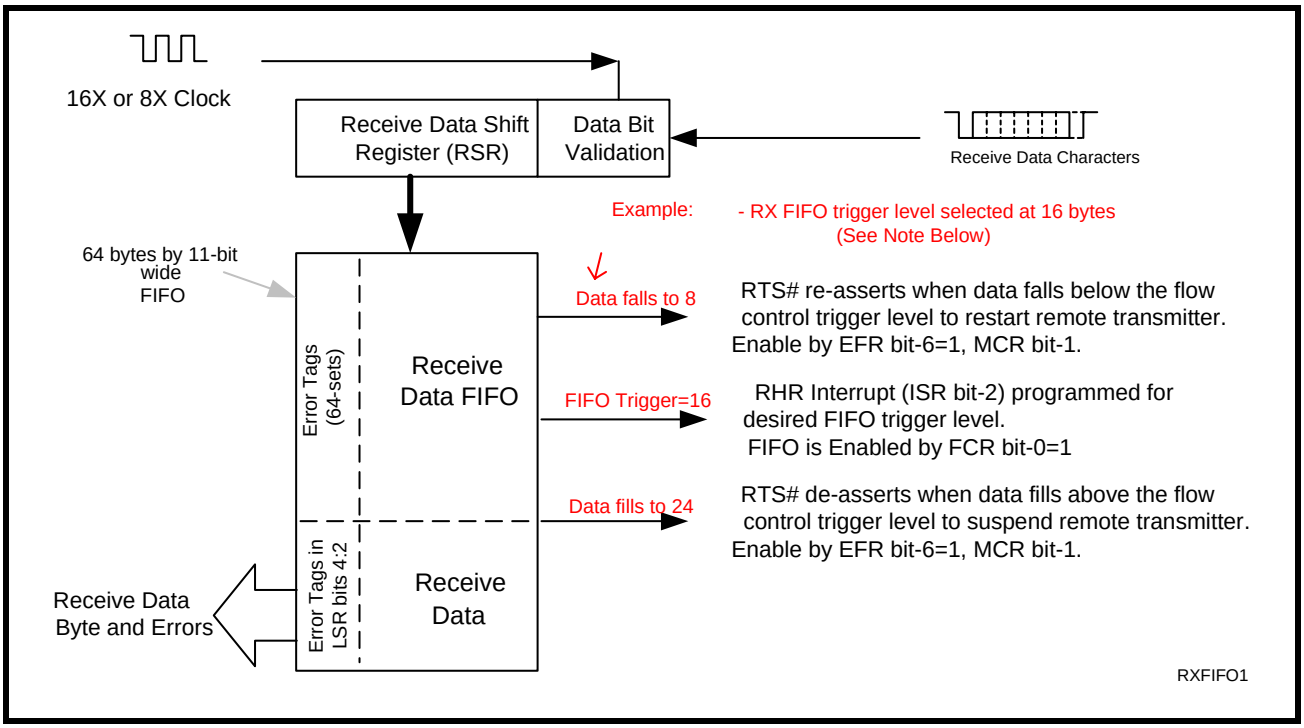


FIGURE 8. RECEIVER OPERATION IN FIFO AND AUTO RTS FLOW CONTROL MODE



NOTE: *Table-B selected as Trigger Table for* **Figure 8** *(see* **Table 14***).*

2.9 THR and RHR Register Locations

The THR and RHR register addresses for channel 0 to channel 7 are shown in **Table 5** below. The THR and RHR for channels 0 to 7 are located at address 0x00, 0x10, 0x20, 0x30, 0x40, 0x50, 0x60 and 0x70 respectively. Transmit data byte is loaded to the THR when writing to that address and receive data is unloaded from the RHR register when reading that address. Both THR and RHR registers are 16C550 compatible in 8-bit format, so each bus operation can only write or read in bytes..

TABLE 5: TRANSMIT AND RECEIVE HOLDING REGISTER LOCATIONS, 16C550 COMPATIBLE

THR and RHR Address Locations For CH0 to CH3 (16C550 Compatible)

CH0	0x00	Write THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH0	0x00	Read RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH1	0x10	Write THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH1	0x10	Read RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH2	0x20	Write THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH2	0x20	Read RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH3	0x30	Write THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH3	0x30	Read RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0

784THRRHR1

2.10 Auto RTS/DTR Hardware Flow Control Operation

Automatic RTS/DTR flow control is used to prevent data overrun to the **local** receiver FIFO. The RTS#/DTR# output pin is used to request remote unit to suspend/resume data transmission. The flow control features are individually selected to fit specific application requirement (see **Figure 9**):

- Select RTS (and CTS) or DTR (and DSR) through MCR bit-2.
- Enable auto RTS/DTR flow control using EFR bit-6.
- The auto RTS or auto DTR function must be started by asserting the RTS# or DTR# output pin (MCR bit-1 or bit-0 to a logic 1, respectively) after it is enabled.
- If using programmable RX FIFO trigger levels, hysteresis levels can be selected via FCTR bits 3-0.

With the Auto RTS function enabled, the RTS# output pin will not be de-asserted (HIGH) when the receive FIFO reaches the programmed trigger level, but will be de-asserted when the FIFO reaches the next trigger level for Trigger Tables A-C (**See Table 14**). The RTS# output pin will be asserted (LOW) again after the FIFO is unloaded to the next trigger level below the programmed trigger level.

For Trigger Table D (or programmable trigger levels), the RTS# output pin is de-asserted when the the RX FIFO level reaches the RX trigger level plus the hysteresis level and is asserted when the RX FIFO level falls below the RX trigger level minus the hysteresis level.

However, even under these conditions, the 794 will continue to accept data until the receive FIFO is full if the remote UART transmitter continues to send data.

- If used, enable RTS/DTR interrupt through IER bit-6 (after setting EFR bit-4). The UART issues an interrupt when the RTS#/DTR# pin makes a transition: ISR bit-5 will be set to 1.

2.10.1 Auto CTS/DSR Flow Control

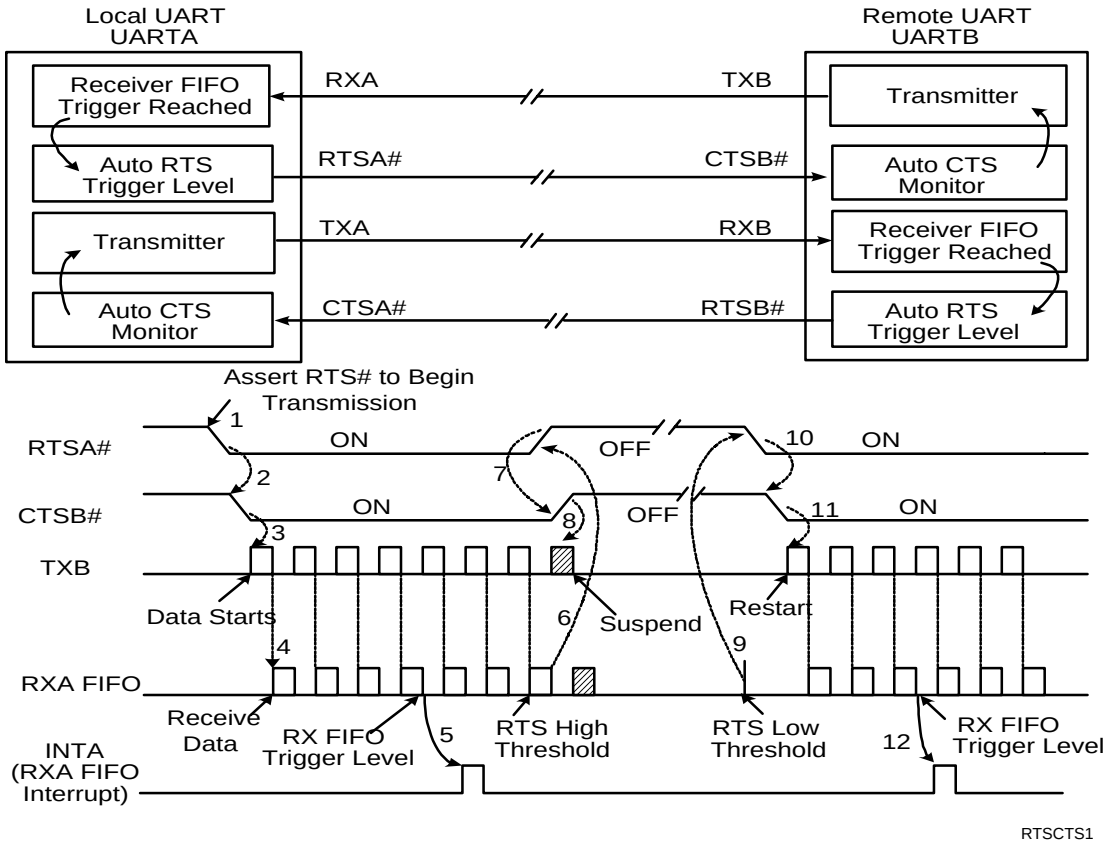
Automatic CTS/DSR flow control is used to prevent data overrun to the remote receiver FIFO. The CTS/DSR pin is monitored to suspend/restart local transmitter. The flow control features are individually selected to fit specific application requirement (see **Figure 9**):

- Select CTS (and RTS) or DSR (and DTR) through MCR bit-2.
- Enable auto CTS/DSR flow control using EFR bit-7.

With the Auto CTS or Auto DTR function enabled, the UART will suspend transmission as soon as the stop bit of the character in the Transmit Shift Register has been shifted out. Transmission is resumed after the CTS#/DTR# input is re-asserted (LOW), indicating more data may be sent.

- If used, enable CTS/DSR interrupt through IER bit-7 (after setting EFR bit-4). The UART issues an interrupt when the CTS#/DSR# pin makes a transition: ISR bit-5 will be set to a logic 1, and UART will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS#/DSR# input returns LOW, indicating more data may be sent.

FIGURE 9. AUTO RTS/DTR AND CTS/DSR FLOW CONTROL OPERATION



The local UART (UARTA) starts data transfer by asserting RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

2.11 Auto Xon/Xoff (Software) Flow Control

When software flow control is enabled (**See Table 18**), the 794 compares one or two sequential receive data characters with the programmed Xon-1,2 or Xoff-1,2 character value(s). If receive character(s) (RX) match the programmed Xoff-1,2 value(s), the 794 will halt transmission (TX) as soon as the current character has completed transmission. When a match occurs, the Xoff (if enabled via IER bit-5) flag will be set and the interrupt output pin will be activated. Following a suspension due to a match of the Xoff character(s), the 794 will monitor the receive data stream for a match to the Xon-1,2 character(s). If a match is found, the 794 will resume operation and clear the flags (ISR bit-4).

Reset initially sets the contents of the Xon1, Xon2, Xoff1 and Xoff2 flow control registers to '0'. Following reset, any desired Xon/Xoff value can be used for software flow control. Different conditions can be set to detect Xon/Xoff characters (**See Table 18**) and suspend/resume transmissions. When double 8-bit Xon/Xoff characters are selected, the 794 compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the user accessible RX data buffer or FIFO.

In the event that the receive buffer is overfilling and flow control needs to be executed, the 794 automatically sends an Xoff message (when enabled) via the serial TX output to the remote modem. The 794 sends the Xoff-1,2 characters two character times (= time taken to send two characters at the programmed baud rate) after the receive FIFO crosses the programmed trigger level (for all trigger tables A-D). To clear this condition, the 794 will transmit the programmed Xon-1,2 characters as soon as receive FIFO is less than one trigger level below the programmed trigger level (for Trigger Tables A, B, and C) or when receive FIFO is less than the trigger level minus the hysteresis value (for Trigger Table D). This hysteresis value is the same as the Auto RTS/DTR Hysteresis value in Table 17. Table 6 below explains this when Trigger Table-B (See Table 14) is selected.

TABLE 6: AUTO XON/XOFF (SOFTWARE) FLOW CONTROL

RX TRIGGER LEVEL	INT PIN ACTIVATION	XOFF CHARACTER(S) SENT (CHARACTERS IN RX FIFO)	XON CHARACTER(S) SENT (CHARACTERS IN RX FIFO)
8	8	8*	0
16	16	16*	8
24	24	24*	16
28	28	28*	24

** After the trigger level is reached, an xoff character is sent after a short span of time (= time required to send 2 characters); for example, after 2.083ms has elapsed for 9600 baud and 10-bit word length setting.*

2.12 Special Character Detect

A special character detect feature is provided to detect an 8-bit character when bit-5 is set in the Enhanced Feature Register (EFR). When this character (Xoff2) is detected, it will be placed in the FIFO along with normal incoming RX data. The 794 compares each incoming receive character with Xoff-2 data. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of special character. Although the Internal Register Table shows Xon, Xoff Registers with 8 bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register (LCR) bits 0-1 defines the number of character bits, i.e., either 5 bits, 6 bits, 7 bits, or 8 bits. The word length selected by LCR bits 0-1 also determines the number of bits that will be used for the special character comparison. Bit-0 in the Xon, Xoff Registers corresponds to the LSB bit for the receive character.

2.13 Auto RS485 Half-duplex Control

The auto RS485 half-duplex direction control changes the behavior of the transmitter when enabled by FCTR bit-5. It asserts RTS# or DTR# (LOW) after a specified delay indicated in MSR[7:4] following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote station's response. The delay optimizes the time needed for the last transmission to reach the farthest station on a long cable network before switching off the line driver. This delay prevents undesirable line signal disturbance that causes signal degradation. When the host is ready to transmit next polling data packet again, it only has to load data bytes to the transmit FIFO. The transmitter automatically de-asserts RTS# or DTR# output (HIGH) prior to sending the data. The auto RS485 half-duplex direction control also changes the transmitter empty interrupt to TSR empty instead of THR empty.

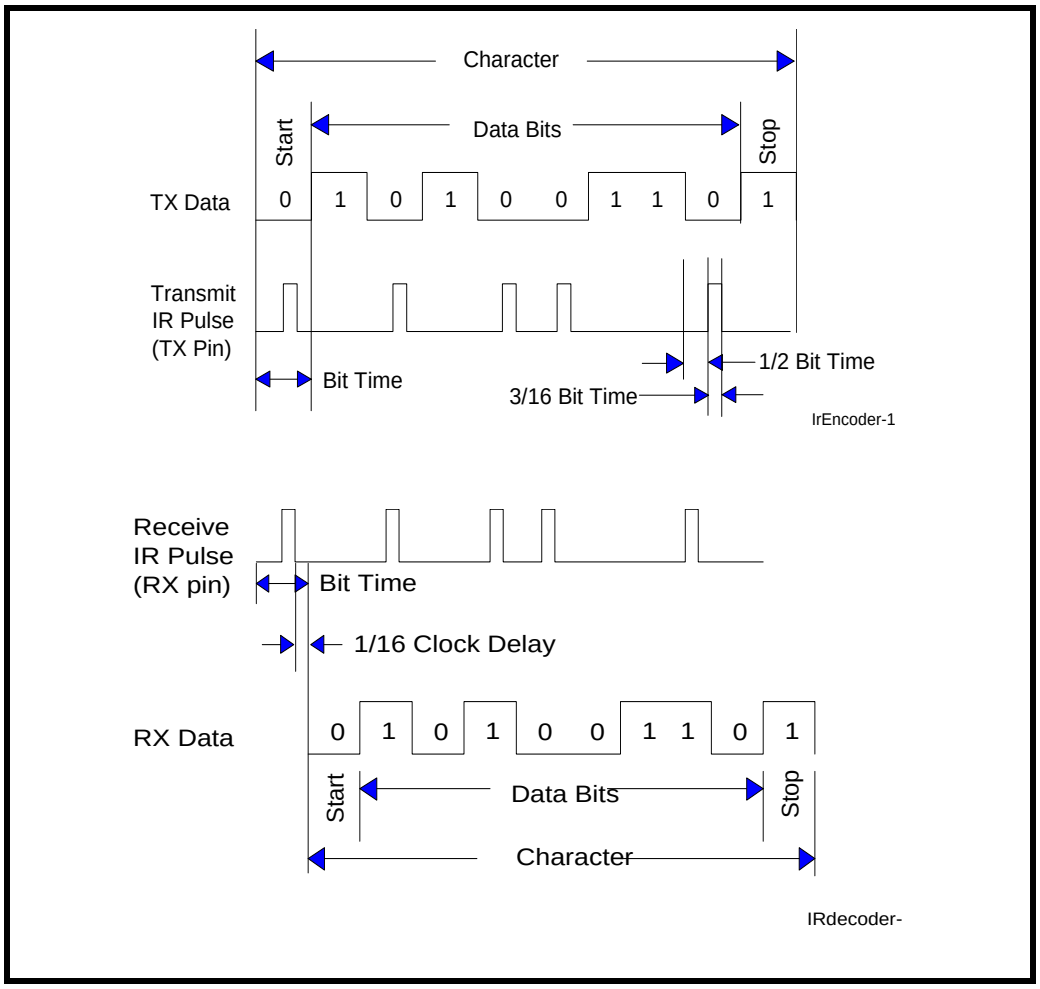
2.14 Infrared Mode

Each UART in the 794 includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The input pin ENIR conveniently activates all 4 UART channels to start up in the infrared mode. Note that the ENIR pin is sampled when the RST# input is de-asserted. This global control pin enables the MCR bit-6 function in every UART channel register. After power up or a reset, the software can overwrite MCR bit-6 if so desired. ENIR and MCR bit-6 also disable the receiver while the transmitter is sending data. This prevents echoed data from reaching the receiver. The global activation ENIR pin prevents the infrared emitter from turning on and drawing large amount of current while the system is starting up. When the infrared feature is enabled, the transmit data outputs, TX[7:0], would idle at logic zero level. Likewise, the RX [7:0] inputs assume an idle level of logic zero.

The infrared encoder sends out a 3/16 of a bit wide HIGH-pulse for each “0” bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See **Figure 10** below.

The infrared decoder receives the input pulse from the infrared sensing diode on RX pin. Each time it senses a light pulse, it returns a logic zero to the data bit stream. The decoder also accepts (when FCTR bit-4 = 1) an inverted IR-encoded input signal. This option supports active LOW instead of normal active HIGH pulse from some infrared modules on the market.

FIGURE 10. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



2.15 Sleep Mode with Auto Wake-Up

The 794 supports low voltage system designs, hence, a sleep mode is included to reduce its power consumption when the chip is not actively used.

All of these conditions must be satisfied for the 794 to enter sleep mode:

- no interrupts pending for all 4 channels of the 794 (ISR bit-0 = 1)
- SLEEP register = 0xFF
- modem inputs are not toggling (MSR bits 0-3 = 0)
- RX input pin of all 4 channels are idling HIGH

The 794 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The 794 resumes normal operation by any of the following:

- a receive data start bit transition (HIGH to LOW)
- a data byte is loaded to the transmitter, THR or FIFO
- a change of logic state on any of the modem or general purpose serial inputs: CTS#, DSR#, CD#, RI#

If the 794 is awakened by any one of the above conditions, it will generate an interrupt. If the interrupt for the event that woke up the 794 is not enabled, then a special wake-up interrupt occurs where reading the interrupt status register will return a "no interrupt" indication. For example, there is a change of state on the CTS# input that wakes up the 794, but the MSR interrupt is not enabled. Reading the interrupt status register will return a value indicating that there are no pending interrupts and will clear the wake-up interrupt.

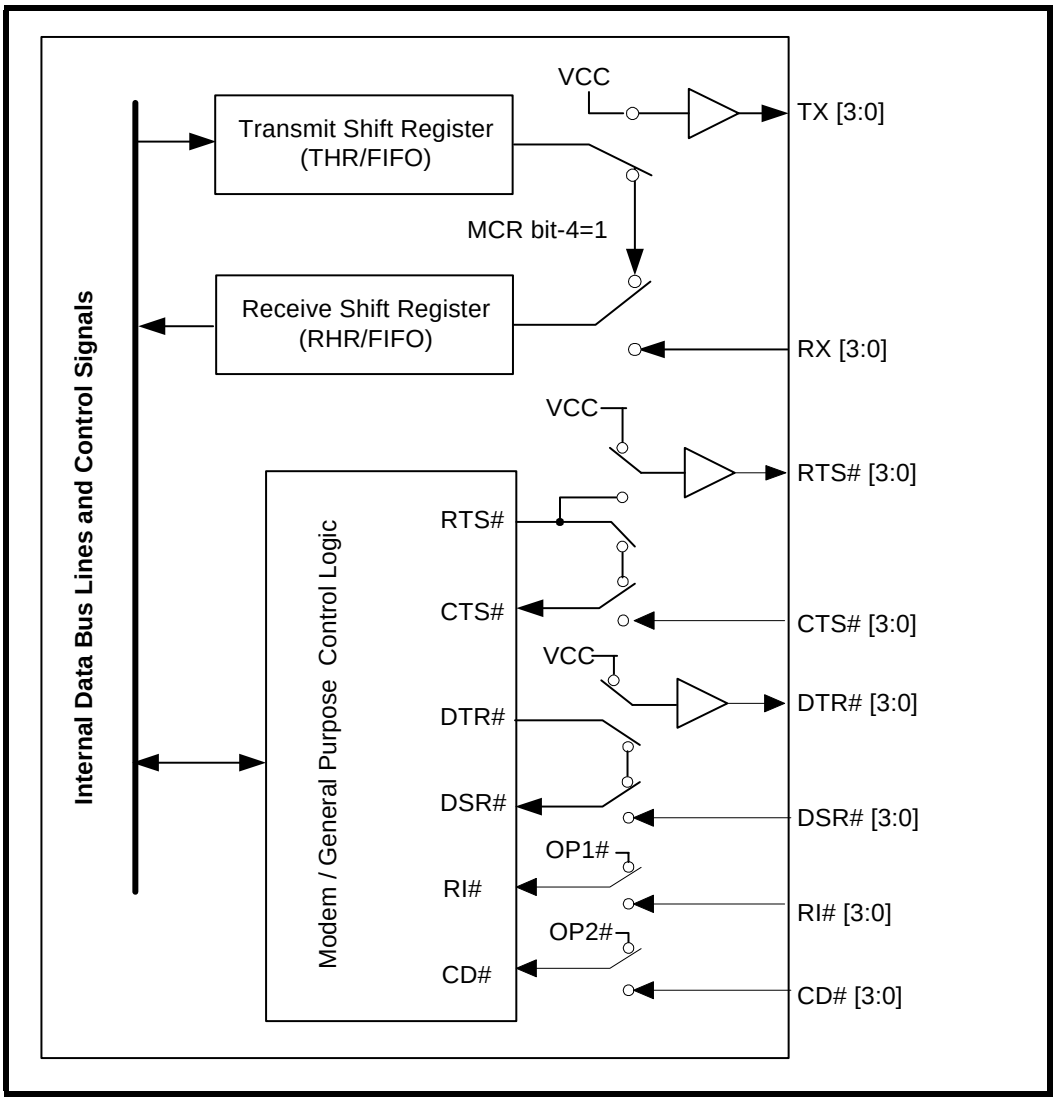
The 794 will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the 794 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending in any channel. The 794 will stay in the sleep mode of operation until it is disabled by setting SLEEP = 0x00.

A word of caution: owing to the starting up delay of the crystal oscillator after waking up from sleep mode, the first few receive characters may be lost. The number of characters lost during the restart also depends on your operating data rate. More characters are lost when operating at higher data rate.

2.16 Internal Loopback

Each UART channel provides an internal loopback capability for system diagnostic purposes. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 11 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX pin is held at HIGH or mark condition while RTS# and DTR# are de-asserted (HIGH), and CTS#, DSR# CD# and RI# inputs are ignored.

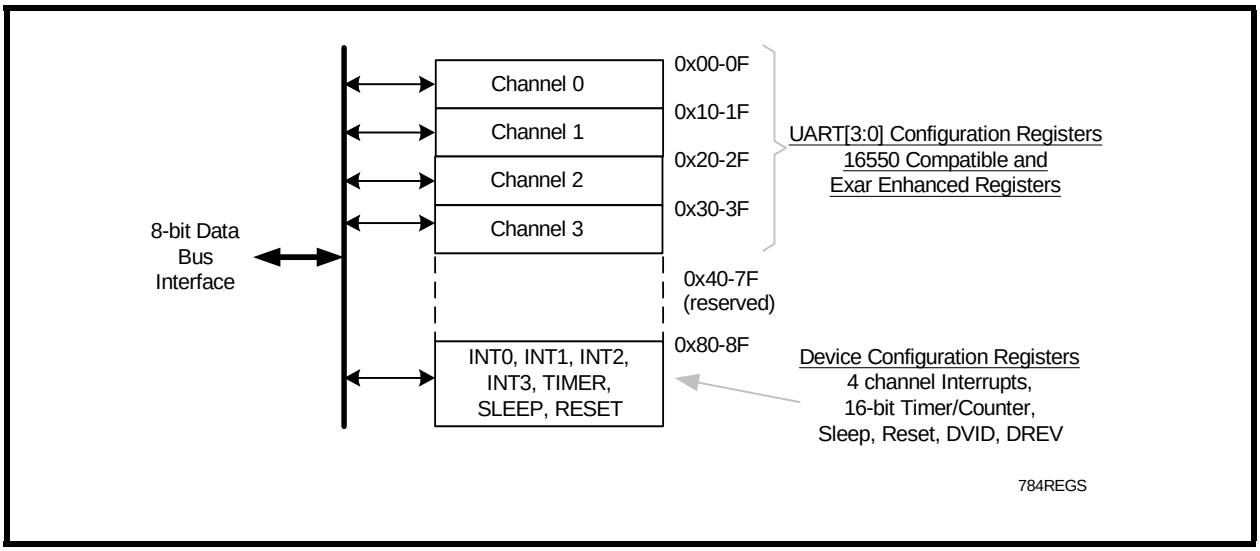
FIGURE 11. INTERNAL LOOP BACK



3.0 XR16V794 REGISTERS

The XR16V794 octal UART register set consists of the Device Configuration Registers that are accessible directly from the data bus for programming general operating conditions of the UARTs and monitoring the status of various functions. These functions include all 4 channel UART's interrupt control and status, 16-bit general purpose timer control and status, sleep mode, soft-reset, and device identification and revision. Also, each UART channel has its own set of internal UART Configuration Registers for its own operation control, status reporting and data transfer. These registers are mapped into a 256-byte of the data memory address space. The following paragraphs describe all the registers in detail.

FIGURE 12. THE XR16V794 REGISTERS



3.1 DEVICE CONFIGURATION REGISTER SET

The device configuration registers are directly accessible from the bus. This provides easy programming of general operating parameters to the 794 UART and for monitoring the status of various functions. The device configuration registers are mapped onto address 0x80-8F as shown on the register map in **Table 8** and **Figure 12**. These registers provide global controls and status of all 4 channel UARTs that include interrupt status, 16-bit general purpose timer control and status, 8X or 16X sampling clock, sleep mode control, soft-reset control, simultaneous UART initialization, and device identification and revision.

TABLE 7: XR16V794 REGISTER SETS

ADDRESS [A7:A0]	UART CHANNEL SPACE	REFERENCE	COMMENT
0x00 - 0x0F	UART channel 0 Registers	(**Table 11** & **12**)	
0x10 - 0x1F	UART channel 1 Registers	(**Table 11** & **12**)	
0x20 - 0x2F	UART channel 2 Registers	(**Table 11** & **12**)	
0x30 - 0x3F	UART channel 3 Registers	(**Table 11** & **12**)	First 8 registers are 16550 compatible
0x40 - 0x7F	None		Reserved
0x80 - 0x8F	Device Configuration Registers	(**Table 8**)	Interrupt registers and global controls

TABLE 8: DEVICE CONFIGURATION REGISTERS

ADDRESS [A7:A0]	READ/ WRITE	REGISTER	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x80	R	INT Source	Reserved	Reserved	Reserved	Reserved	UART 3	UART 2	UART 1	UART 0
0x81	R	INT 1	UART 2 bit 1	source bit 0	UART 1 bit 2	interrupt bit 1	source bit 0	UART 0 bit 2	interrupt bit 1	source bit 0
0x82	R	INT 2	Reserved	Reserved	Reserved	Reserved	UART 3 bit 2	interrupt bit 1	source bit 0	UART 2 bit 2
0x83	R	INT 3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x84	R/W	TIMER CTRL	0	0	0	0	clock source	function select	start timer	enable timer INT
0x85	R	TIMER	0	0	0	0	0	0	0	0
0x86	R/W	TIMER LSB	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x87	R/W	TIMER MSB	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x88	R/W	8X MODE	UART 7	UART 6	UART 5	UART 4	UART 3	UART 2	UART 1	UART 0
0x89	R	REGA	0	0	0	0	0	0	0	0
0x8A	W	RESET	Reserved	Reserved	Reserved	Reserved	Reset UART 3	Reset UART 2	Reset UART 1	Reset UART 0
0x8B	R/W	SLEEP	Reserved	Reserved	Reserved	Reserved	Enable sleep UART 3	Enable sleep UART 2	Enable sleep UART 1	Enable sleep UART 0
0x8C	R	DREV	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x8D	R	DVID	0	1	0	0	0	1	0	0
0x8E	R/W	REGB	0	0	0	0	0	0	0	write to all UARTs

3.1.1 The Global Interrupt Source Registers

The XR16V794 has a global interrupt source register set that consists of 4 consecutive registers [INT0, INT1, INT2 and INT3]. The four registers are in the device configuration register address space.

INT3 [0x00]	INT2 [0x00]	INT1 [0x00]	INT0 [0x00]

All four registers default to logic zero (as indicated in square braces) for no interrupt pending. All 4 channel interrupts are enabled or disabled in each channel's IER register. INT0 shows individual status for each channel while INT1, INT2 and INT3 show the details of the source of each channel's interrupt with its unique 3-bit encoding. **Figure 13** shows the 4 interrupt registers in sequence for clarity. The 16-bit timer and sleep wake-up interrupts are masked in the device configuration registers, TIMERCNTL and SLEEP. An interrupt is generated (if enabled) by the 794 when awakened from sleep if all 4 channels were placed in the sleep mode previously.

Each bit gives an indication of the channel that has requested for service. For example, bit-0 represents channel 0 and bit-3 indicates channel 3. Logic one indicates the channel N [3:0] has called for service. Bits 4 to 7 are reserved and remains at logic zero. The interrupt bit clears after reading the appropriate register of the interrupting UART channel register (ISR, LSR and MSR). **SEE "INTERRUPT CLEARING:" ON PAGE 30.** for interrupt clearing details.

3.1.1.1 INT0 Channel Interrupt Indicator:

INT0 Register
Individual UART Channel Interrupt Status

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Rsvd	Rsvd	Rsvd	Rsvd	Ch-3	Ch-2	Ch-1	Ch-0

3.1.1.2 INT1, INT2 and INT3 Interrupt Source Locator

INT3, INT2 and INT1 provide a 24-bit (3 bits per channel) encoded interrupt indicator. **Table 9** shows the 3 bit encoding and their priority order. The 16-bit Timer time-out interrupt will show up only as a channel 0 interrupt. For other channels, interrupt 7 is reserved.

FIGURE 13. THE GLOBAL INTERRUPT REGISTERS, INT0, INT1, INT2 AND INT3

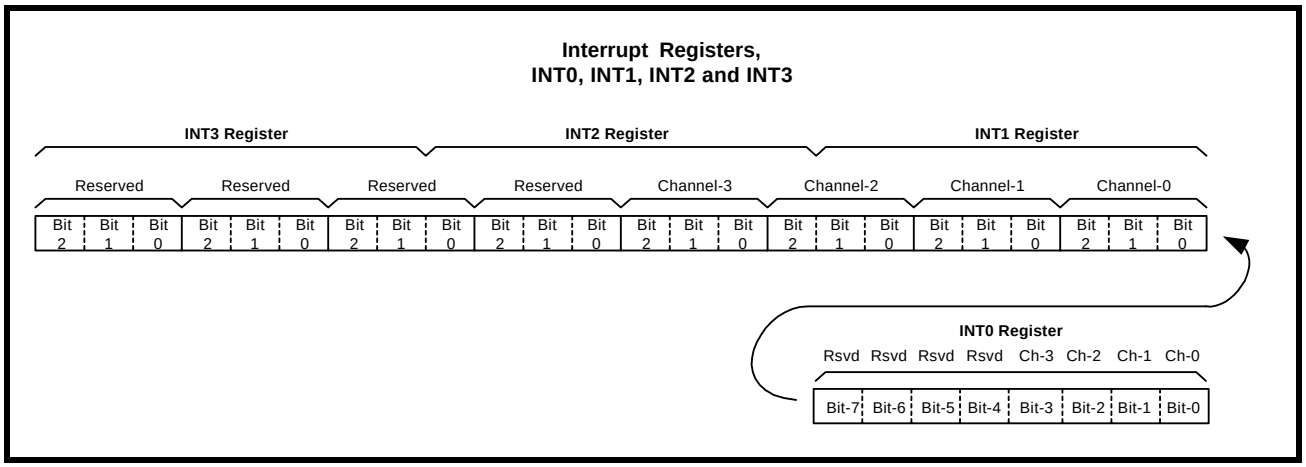


TABLE 9: UART CHANNEL [7:0] INTERRUPT SOURCE ENCODING AND CLEARING

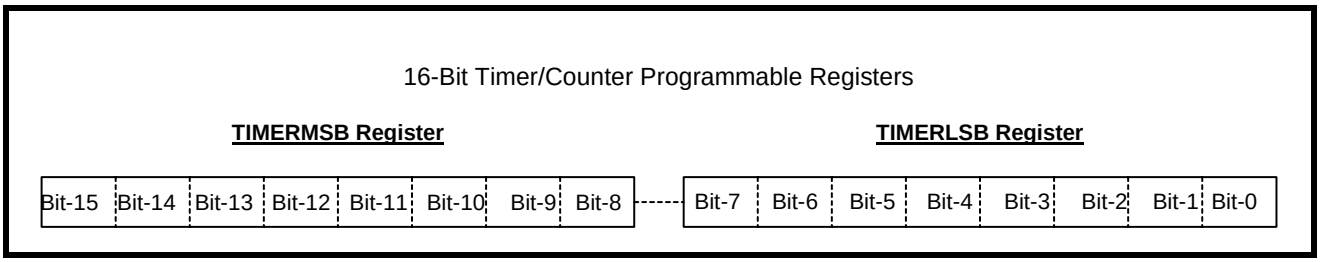
PRIORITY	Bit 2	Bit 1	Bit 0	INTERRUPT SOURCE(S) AND CLEARING
x	0	0	0	None (or wake-up indicator)
1	0	0	1	RXRDY & RX Line Status (logic OR of LSR[4:1]). RXRDY INT clears by reading data in the RX FIFO until it falls below the trigger level; RX Line Status INT cleared after reading LSR register.
2	0	1	0	RXRDY Time-out: Cleared same way as RXRDY INT.
3	0	1	1	TXRDY, THR or TSR (auto RS485 mode) empty, clears after reading ISR register.
4	1	0	0	MSR, RTS/CTS or DTR/DSR delta or Xoff/Xon or special character detected. The first two clears after reading MSR register; Xoff/Xon or special char. detect INT clears after reading ISR register.
5	1	0	1	Reserved.
6	1	1	0	Reserved.
7	1	1	1	TIMER Time-out, shows up as a channel 0 INT. It clears after reading the TIMERCNTL register. Reserved in other channels.

3.1.2 General Purpose 16-bit Timer/Counter [TIMERMSB, TIMELSB, TIMER, TIMECNTL] (DEFAULT 0xXX-XX-00-00)

The 794 includes a 16-bit general purpose timer/counter. Its clock source may be selected from internal crystal oscillator or externally on pin TMRCK. The timer can be set to be a single-shot for a one-time event or re-triggerable for a periodic signal. An interrupt may be generated when the timer times out and will show up as a Channel 0 interrupt (see **Table 9**). It is controlled through 4 configuration registers [TIMERCNTL, TIMER, TIMELSB, TIMERMSB]. These registers provide start/stop and re-triggerable or one-shot operation (see **Table 10** below). The time-out output of the Timer can be set to generate an interrupt for system or event alarm.

3.1.2.1 TIMERMSB [7:0] and TIMERLSB [7:0]

TIMERMSB and TIMERLSB form a 16-bit value. The least-significant bit of the timer is being bit-0 of the TIMERLSB with most-significant-bit being bit-7 in TIMERMSB. Notice that these registers do not hold the current counter value when read. Default value is zero (timer disabled) upon powerup and reset.



3.1.2.2 TIMER [7:0] Reserved

3.1.2.3 TIMERCNTL [7:0] Register

The bits 3:0 of this register are used to issue commands. The commands are self-clearing, so reading this register does not show the last written command. Reading this register returns a value of 0x01 when there is a Timer interrupt pending and 0x00 at all other times.

TABLE 10: TIMER CONTROL COMMANDS

TIMERCNTL [7:4]	Reserved
TIMERCNTL [3:0]	These bits are used to invoke a series of commands that control the function of the Timer/Counter. The commands 1011 to 1111 are reserved. 0001: Enable Timer Interrupt 0010: Disable Timer Interrupt 0011: Select One-shot mode 0100: Select Re-triggerable mode 0101: Select Internal Crystal Oscillator output as clock source for the Timer 0110: Select External Clock source (through TMRCK pin) for the Timer 0111: Reserved 1000: Reserved 1001: Start Timer 1010: Stop Timer 1011: Reset Timer

TIMER OPERATION

The following paragraphs describe the operation of the 16-bit Timer/Counter. The following conventions will be used in this discussion:

- 'N' is the 16-bit value programmed in the TIMER MSB, LSB registers
- 'N' can take any value from 0x0002 to 0xFFFF.

Timer Interrupt

In the one-shot mode, the Timer will issue an interrupt 'N' clocks after the Timer is started. This is the time when the Timer times-out in the one-shot mode. In the re-triggerable mode, the Timer will keep issuing an interrupt every 'N' clocks. This is shown in **Figure 15**, where the time between successive time-outs (in re-triggereble mode) is 'N' clocks. The Timer interrupt can be cleared by reading the TIMERCNTL register. The TIMERCNTL will read a value of 0x01 when there is an interrupt and a 0x00 at all other times.

FIGURE 14. TIMER/COUNTER CIRCUIT.

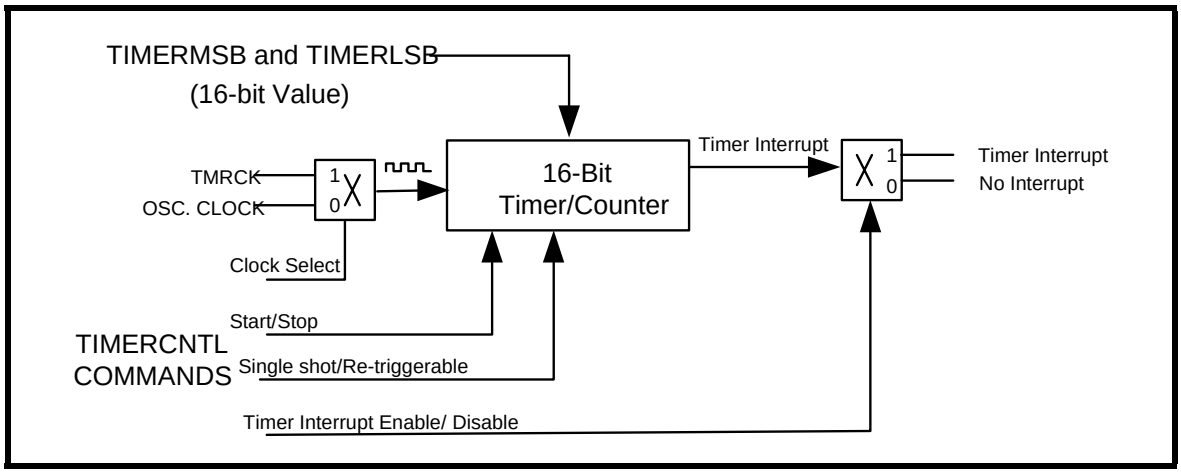
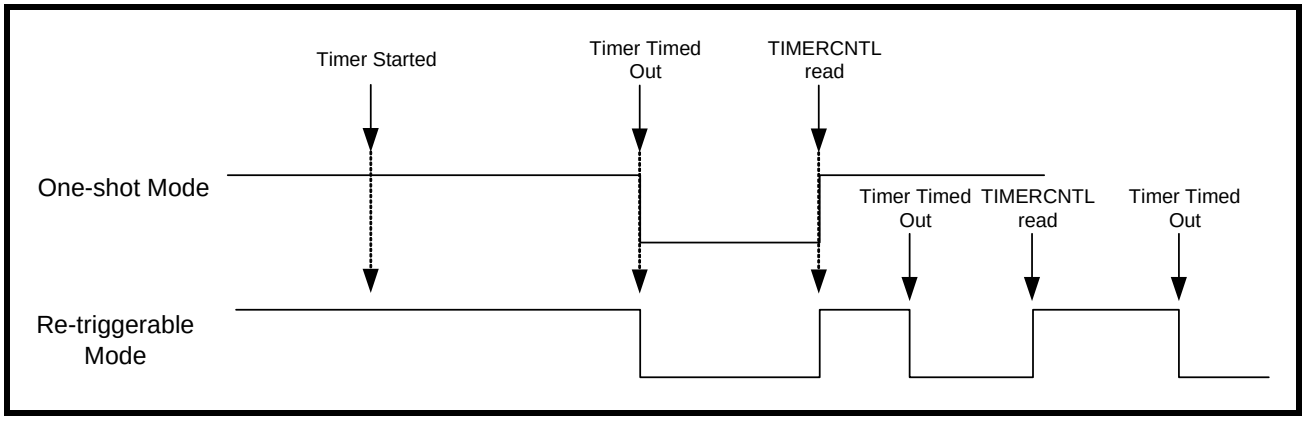


FIGURE 15. INTERRUPT OUTPUT IN ONE-SHOT AND RE-TRIGGERABLE MODES



3.1.3 8XMODE [7:0] (default 0x00)

Each bit selects 8X or 16X sampling rate for that UART channel, bit-0 is channel 0. Logic 0 (default) selects normal 16X sampling with logic one selects 8X sampling rate. Transmit and receive data rates will double by selecting 8X.

8XMODE Register
Individual UART Channel 8X Clock Mode Enable

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Ch-7	Ch-6	Ch-5	Ch-4	Ch-3	Ch-2	Ch-1	Ch-0

3.1.4 REGA [7:0](default 0x00)

Reserved.

3.1.5 RESET [7:0] (default 0x00)

RESET Register
Individual UART Channel Reset Enable

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Ch-7	Ch-6	Ch-5	Ch-4	Ch-3	Ch-2	Ch-1	Ch-0

The 8-bit RESET register provides the software with the ability to reset the UART(s) when there is a need. Each bit is self-resetting after it is written a logic 1 to perform a reset to that channel. All registers in that channel will be reset to the default condition, see **Table 19** for details. As an example, bit-0 =1 resets UART channel 0 with bit-7=1 resets channel 7.

3.1.6 SLEEP [7:0] (default 0x00)

The 8-bit Sleep register enables each UART separately to enter Sleep mode. Sleep mode reduces power consumption when the system needs to put the UART(s) to idle. The UART enters sleep mode when there is no interrupt pending. When all 4 UARTs are put to sleep, the on-chip oscillator shuts off to further conserve power. In this case, the octal UART is awaken by any of the UART channel on from a receive data byte or a change on the serial port. The UART is ready after 32 crystal clocks to ensure full functionality. Also, a special interrupt is generated with an indication of no pending interrupt. Logic 0 (default) and logic 1 disable and enable sleep mode respectively.

SLEEP Register
Individual UART Channel Sleep Enable

Ch-7	Ch-6	Ch-5	Ch-4	Ch-3	Ch-2	Ch-1	Ch-0
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0

3.1.7 Device Identification and Revision

There are 2 internal registers that provide device identification and revision, DVID and DREV registers. The 8-bit content in the DVID register provides device identification. A return value of 0x44 from this register indicates the device is a XR16V794. The DREV register returns a 8-bit value of 0x01 for revision A, 0x02 for revision B and so on. This information is very useful to the software driver for identifying which device it is communicating with and to keep up with revision changes.

3.1.7.1 DVID [7:0] (default 0x48)

Device identification for the type of UART. The Device ID for the V794 is 0x44.

Examples:

XR16V794 = 0x44

XR16L784 = 0x24

3.1.7.2 DREV [7:0] (default (0x01)

Revision number of the XR16V794. A 0x01 represents "revision-A" with 0x02 for rev-B and so forth.

3.1.8 REGB [7:0] (default 0x00)

REGB[0]: Simultaneous write to all 4 UARTs

- Logic 0 = Write to each UART configuration register individually (default).
- Logic 1 = Enable simultaneous write to all 4 UART configuration registers. This can be very useful during device initialization in the power-up and reset routines.

REGB[7:1]

Reserved.

3.2 UART CHANNEL CONFIGURATION REGISTERS

The first 8 registers are 16550 compatible with EXAR enhanced feature registers located on the upper 8 addresses. The 4 sets of UART configuration registers are decoded using address lines A0 to A3 as shown below.

TABLE 11: UART CHANNEL CONFIGURATION REGISTERS.

ADDRESS	REGISTER	READ/WRITE	COMMENTS
A3 A2 A1 A0			
16550 COMPATIBLE			
0 0 0 0	RHR - Receive Holding Reg THR - Transmit Holding Register	Read-only Write-only	LCR[7] = 0
0 0 0 0	DLL - Divisor LSB	Read/Write	LCR[7] = 1
0 0 0 1	DLM - Divisor MSB	Read/Write	LCR[7] = 1
0 0 1 0	DLD - Divisor Fractional Part	Read/Write	LCR[7] = 1
0 0 0 1	IER - Interrupt Enable Reg	Read/Write	LCR[7] = 0
0 0 1 0	ISR - Interrupt Status Reg FCR - FIFO Control Reg	Read-only Write-only	LCR[7] = 0
0 0 1 1	LCR - Line Control Reg	Read/Write	
0 1 0 0	MCR - Modem Control Reg	Read/Write	
0 1 0 1	LSR - Line Status Reg reserved	Read-only Write-only	
0 1 1 0	MSR - Modem Status Reg - Auto RS485 Delay	Read-only Write-only	
0 1 1 1	SPR - Scratch Pad Reg	Read/Write	
ENHANCED REGISTER			
1 0 0 0	FCTR	Read/Write	
1 0 0 1	EFR - Enhanced Function Reg	Read/Write	
1 0 1 0	TXCNT - Transmit FIFO Level Counter TXTRG - Transmit FIFO Trigger Level	Read-only Write-only	
1 0 1 1	RXCNT - Receive FIFO Level Counter RXTRG - Receive FIFO Trigger Level	Read-only Write-only	
1 1 0 0	Xoff-1 - Xoff Character 1 Xchar	Write-only Read-only	Xon,Xoff Rcvd. Flags
1 1 0 1	Xoff-2 - Xoff Character 2 reserved	Write-only Read-only	
1 1 1 0	Xon-1 - Xon Character 1 reserved	Write-only Read-only	
1 1 1 1	Xon-2 - Xon Character 2 reserved	Write-only Read-only	

TABLE 12: UART CHANNEL CONFIGURATION REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED BY EFR BIT-4.

ADDRESS A3-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
0 0 0 0	RHR	R	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
0 0 0 0	THR	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
0 0 0 0	DLL	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1
0 0 0 1	DLM	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1
0 0 1 0	DLD	R/W	0	0	0	0	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1
0 0 0 1	IER	R/W	0/ CTS/ DSR# Int. Enable	0/ RTS/ DTR# Int. Enable	0/ Xon/Xoff/ Sp. Char. Int. Enable	0	Modem Status Int. Enable	RX Line Status Int. Enable	TX Ready Int. Enable	RX Data Int. Enable	LCR[7]=0
0 0 1 0	ISR	R	FIFOs Enable	FIFOs Enable	0/ Delta-Flow Cntl	0/ Xoff/special char	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	LCR[7]=0
0 0 1 0	FCR	W	RX FIFO Trigger	RX FIFO Trigger	0/ TX FIFO Trigger	0/ TX FIFO Trigger	DMA Mode	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	LCR[7]=0
0 0 1 1	LCR	R/W	Divisor Enable	Set TX Break	Set Parity	Even Par-ity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
0 1 0 0	MCR	R/W	0/ BRG Prescaler	0/ IR Enable	0/ XonAny	Internal Loopback Enable	(OP2)[1] TX char Immedi-ate	(OP1)[1] RTS/DTR Flow Sel	RTS# Pin Control	DTR# Pin Control	
0 1 0 1	LSR	R/W	RX FIFO ERROR	Transmit-ter Empty	TX FIFO Empty	RX Break	RX Fram-ing Error	RX Parity Error	RX Over-run	RX Data Ready	
0 1 1 0	MSR	R	CD	RI	DSR	CTS	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
	MSR	W	RS485 DLY-3	RS485 DLY-2	RS485 DLY-1	RS485 DLY-0	Disable TX	Disable RX			
0 1 1 1	SPR	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	User Data
1 0 0 0	FCTR	R/W	TRG Table Bit-1	TRG Table Bit-0	Auto RS485 Enable	Invert IR RX Input	RTS/DTR Hyst Bit-3	RTS/DTR Hyst Bit-2	RTS/DTR Hyst Bit-1	RTS/DTR Hyst Bit-0	
1 0 0 1	EFR	R/W	Auto CTS/DSR Enable	Auto RTS/DTR Enable	Special Char Select	Enable IER [7:5], ISR [5:4], FCR[5:4], MCR[7:5, 3:2] MSR[7:2]	Software Flow Cntl Bit-3	Software Flow Cntl Bit-2	Software Flow Cntl Bit-1	Software Flow Cntl Bit-0	
1 0 1 0	TXCNT	R	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

TABLE 12: UART CHANNEL CONFIGURATION REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED BY EFR BIT-4.

ADDRESS A3-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
1 0 1 0	TXTRG	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1 1	RXCNT	R	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1 1	RXTRG	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 0 0	XCHAR	R	0	0	0	0	TX Xon Indicator	TX Xoff Indicator	Xon Det. Indicator	Xoff Det. Indicator	Self clear after read
1 1 0 0	XOFF1	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 0 1	XOFF2	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1 0	XON1	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1 1	XON2	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

NOTE: *MCR bits 2 and 3 (OP1 and OP2 outputs) are not available in the XR16V794. They are present for 16C550 compatibility during Internal loopback, see* **Figure 11**.

4.0 INTERNAL REGISTER DESCRIPTIONS

4.1 Receive Holding Register (RHR) - Read Only

SEE "RECEIVER" ON PAGE 11..

4.2 Transmit Holding Register (THR) - Write Only

SEE "TRANSMITTER" ON PAGE 9..

4.3 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR) and also encoded in INT (INT0-INT3) register in the Device Configuration Registers.

4.3.1 IER versus Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = a logic 1) and receive interrupts (IER BIT-0 = logic 1) are enabled, the RHR interrupts (see ISR bits 3 and 4) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

4.3.2 IER versus Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1 for FIFO enable; resetting IER bits 3:0 enables the XR16V794 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR (non-FIFO mode) or RX FIFO (FIFO mode).

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BIT 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR (non-FIFO mode) or TX FIFO (FIFO mode) is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

IER[7]: CTS# Input Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the CTS# interrupt (default).
- Logic 1 = Enable the CTS# interrupt. The UART issues an interrupt when CTS# pin makes a transition from LOW to HIGH.

IER[6]: RTS# Output Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the RTS# interrupt (default).
- Logic 1 = Enable the RTS# interrupt. The UART issues an interrupt when RTS# pin makes a transition from LOW to HIGH.

IER[5]: Xoff Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the software flow control, receive Xoff interrupt (default).
- Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

IER[4]: Reserved.

IER[3]: Modem Status Interrupt Enable

The Modem Status Register interrupt is issued whenever any of the delta bits of the MSR register (bits 3:0) is set.

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[2]: Receive Line Status Interrupt Enable

An Overrun error, Framing error, Parity error or detection of a Break character will result in an LSR interrupt. The 794 will issue an LSR interrupt immediately after receiving a character with an error. It will again re-issue the interrupt (if the first one has been cleared by reading the LSR register) when the character with the error is on the top of the FIFO, meaning the next one to be read out of the FIFO.

For example, let's consider an incoming data stream of 0x55, 0xAA, etc and that the character 0xAA has a Parity error associated with it. Let's assume that the character 0x55 has not been read out of the FIFO yet. The 794 will issue an interrupt as soon as the stop bit of the character 0xAA is received. The LSR register will have only the FIFO error bit (bit-7) set and none of the other error bits (Bits 1,2,3 and 4) will be set, since the byte on the top of the FIFO is 0x55 which does not have any errors associated with it. When this byte has been read out, the 794 will issue another LSR interrupt and this time the LSR register will show the Parity bit (bit-2) set.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[1]: TX Ready Interrupt Enable

In non-FIFO mode, a TX interrupt is issued whenever the THR is empty. In the FIFO mode, an interrupt is issued twice: once when the number of bytes in the TX FIFO falls below the programmed trigger level and again when the TX FIFO becomes empty. When autoRS485 mode is enabled (FCTR bit-5 = 1), the second interrupt is delayed until the transmitter (both the TX FIFO and the TX Shift Register) is empty.

- Logic 0 = Disable Transmit Ready Interrupt (default).
- Logic 1 = Enable Transmit Ready Interrupt.

IER[0]: RX Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

4.4 Interrupt Status Register (ISR) - Read Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced, others queue up for next service. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 13, shows the data values (bit 0-5) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

4.4.1 Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4. See IER bit-2 description above.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by a 4-char plus 12 bits delay timer.
- TXRDY is by TX trigger level or TX FIFO empty (or transmitter empty in auto RS-485 control).
- MSR is by any of the MSR bits 0, 1, 2 and 3.
- Receive Xon/Xoff/Special character is by detection of a Xon, Xoff or Special character.
- CTS#/DSR# is when its transmitter toggles the input pin (from LOW to HIGH) during auto CTS/DSR flow control enabled by EFR bit-7 and selection on MCR bit-2.
- RTS#/DTR# is when its receiver toggles the output pin (from LOW to HIGH) during auto RTS/DTR flow control enabled by EFR bit-6 and selection on MCR bit-2.
- Wake-up Indicator is when the UART wakes up from the sleep mode.

4.4.2 Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY interrupt is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out interrupt is cleared by reading RHR.
- TXRDY interrupt is cleared by a read to the ISR register or writing to THR.
- MSR interrupt is cleared by a read to the MSR register.
- Xon or Xoff interrupt is cleared by a read to ISR register.
- Special character interrupt is cleared by a read to ISR or after the next character is received.
- RTS#/DTR# and CTS#/DSR# status change interrupts are cleared by a read to the MSR register.
- Wake-up Indicator is cleared by a read to the INT0 register.

TABLE 13: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS						SOURCE OF THE INTERRUPT
	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY (Received Data Ready)
3	0	0	1	1	0	0	RXRDY (Receive Data Time-out)
4	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
5	0	0	0	0	0	0	MSR (Modem Status Register)
6	0	1	0	0	0	0	RXRDY (Received Xon/Xoff or Special character)
7	1	0	0	0	0	0	CTS#/DSR#, RTS#/DTR# change of state
X	0	0	0	0	0	1	None (default)

ISR[7:6]: FIFO Enable Status

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

ISR[5:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels (See **Table 13**). See **"Section 4.4.1, Interrupt Generation:" on page 30** and **"Section 4.4.2, Interrupt Clearing:" on page 30** for details.

ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending. (default condition)

4.5 FIFO Control Register (FCR) - Write Only

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

FCR[7:6]: Receive FIFO Trigger Select

(logic 0 = default, RX trigger level =1)

The FCTR Bits 5-4 are associated with these 2 bits. These 2 bits are used to set the trigger level for the receive FIFO. The UART will issue a receive interrupt when the number of the characters in the FIFO crosses the trigger level. **Table 14** shows the complete selections. Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side.

FCR[5:4]: Transmit FIFO Trigger Select (requires EFR bit-4=1)

(logic 0 = default, TX trigger level = one)

The FCTR Bits 6-7 are associated with these 2 bits by selecting one of the four tables. The 4 user selectable trigger levels in 4 tables are supported for compatibility reasons. These 2 bits set the trigger level for the transmit FIFO interrupt. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. **Table 14** below shows the selections.

FCR[3]: DMA Mode Select

This bit has no effect since TXRDY and RXRDY pins are not available in this device. It is provided for legacy software compatibility.

- Logic 0 = Set DMA to mode 0 (default).
- Logic 1 = Set DMA to mode 1.

FCR[2]: TX FIFO Reset

This bit is only active when FCR bit-0 is active.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is active.

- Logic 0 = No receive FIFO reset (default).
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[0]: TX and RX FIFO Enable

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

TABLE 14: TRANSMIT AND RECEIVE FIFO TRIGGER TABLE AND LEVEL SELECTION

TRIGGER TABLE	FCTR BIT-7	FCTR BIT-6	FCR BIT-7	FCR BIT-6	FCR BIT-5	FCR BIT-4	RECEIVE TRIGGER LEVEL	TRANSMIT TRIGGER LEVEL	COMPATIBILITY
Table-A	0	0			0	0		1 (default)	16C550, 16C2550, 16C2552, 16C554, 16C580, 16L580
			0	0			1 (default)		
			0	1			4		
			1	0			8		
			1	1			14		
Table-B	0	1			0	0		16	16C650A, 16L651
					0	1		8	
					1	0		24	
					1	1		30	
			0	0			8		
			0	1			16		
			1	0			24		
			1	1			28		
Table-C	1	0			0	0		8	16C654
					0	1		16	
					1	0		32	
					1	1		56	
			0	0			8		
			0	1			16		
			1	0			56		
			1	1			60		
Table-D	1	1	X	X	X	X	Programmable via RXTRG register	Programmable via TXTRG register	16L2752, 16L2750, 16C2852, 16C850, 16C854, 16C864

4.6 Line Control Register (LCR) - Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[7]: Baud Rate Divisors Enable

Baud rate generator divisor (DLL, DLM, DLD) enable.

- Logic 0 = Data registers are selected (default).
- Logic 1 = Divisor latch registers (DLL, DLM and DLD) are selected.

LCR[6]: Transmit Break Enable

When enabled the Break control bit causes a break condition to be transmitted (the TX output is forced to a “space’, logic 0, state). This condition remains until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition. (default)
- Logic 1 = Forces the transmitter output (TX) to a “space”, logic 0, for alerting the remote receiver of a line break condition.

LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR BIT-5 = logic 0, parity is not forced (default).
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

TABLE 15: PARITY PROGRAMMING

LCR BIT-5	LCR BIT-4	LCR BIT-3	PARITY SELECTION
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity to mark, “1”
1	1	1	Forced parity to space, “0”

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1’s in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even the number of logic 1’s in the transmitted character. The receiver must be programmed to check the same format.

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See **Table 15** above for parity selection summary.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	WORD LENGTH	STOP BIT LENGTH (BIT TIME(S))
0	5,6,7,8	1 (default)
1	5	1-1/2
1	6,7,8	2

LCR[1:0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	WORD LENGTH
0	0	5 (default)
0	1	6
1	0	7
1	1	8

4.7 Modem Control Register (MCR) - Read/Write

The MCR register is used for controlling the modem interface signals or general purpose inputs/outputs.

MCR[7]: Clock Prescaler Select (requires EFR bit-4=1)

- Logic 0 = Divide by one. The input clock from the crystal or external clock is fed directly to the Programmable Baud Rate Generator without further modification, i.e., divide by one (default).
- Logic 1 = Divide by four. The prescaler divides the input clock from the crystal or external clock by four and feeds it to the Programmable Baud Rate Generator, hence, data rates become one forth.

MCR[6]: Infrared Encoder/Decoder Enable (requires EFR bit-4=1)

The state of this bit depends on the sampled logic level of pin ENIR during power up, following a hardware reset (rising edge of RST# input). Afterward user can override this bit for desired operation.

- Logic 0 = Enable the standard modem receive and transmit character interface.
- Logic 1 = Enable infrared IrDA receive and transmit inputs/outputs. While in this mode, the TX/RX output/input are routed to the infrared encoder/decoder. The data input and output levels will conform to the IrDA infrared interface requirement. As such, while in this mode the infrared TX output will be a logic 0 during idle data conditions. FCTR bit-4 may be selected to invert the RX input signal level going to the decoder for infrared modules that provide rather an inverted output.

MCR[5]: Xon-Any Enable (requires EFR bit-4=1)

- Logic 0 = Disable Xon-Any function (default).
- Logic 1 = Enable Xon-Any function. In this mode any RX character received will enable Xon, resume data transmission.

MCR[4]: Internal Loopback Enable

- Logic 0 = Disable loopback mode (default).
- Logic 1 = Enable local loopback mode, see loopback section and **Figure 11**.

MCR[3]: Send Char Immediate (OP2 in Local Loopback Mode)

This bit is used to transmit a character immediately irrespective of the bytes currently in the transmit FIFO. The data byte must be loaded into the transmit holding register (THR) immediately following the write to this bit (to set it to a '1'). In other words, no other register must be accessed between setting this bit and writing to the THR. The loaded byte will be transmitted ahead of all the bytes in the TX FIFO, immediately after the character currently being shifted out of the transmit shift register is sent out. The existing line parameters (parity, stop bits) will be used when composing the character. This bit is self clearing, therefore, must be set before sending a custom characer each time. Please note that the Transmitter must be enabled for this function (MSR[3] = 0). Also, if software flow control is enabled, the software flow control characters (Xon, Xoff) have higher priority and will get shifted out before the custom byte is transmitted.

- Logic 0 = Send Char Immediate disabled (default).
- Logic 1 = Send Char Immediate enabled.

In Local Loopback Mode (MCR[4] = 1), this bit acts as the legacy OP2 output and controls the CD bit in the MSR register as shown in **Figure 11**. Please make sure that this bit is a '0' when exiting the Local Loopback Mode.

MCR[2]: DTR# or RTS# for Auto Flow Control (OP1 in Local Loopback Mode)

DTR# or RTS# auto hardware flow control select. This bit is in effect only when auto RTS/DTR is enabled by EFR bit-6. DTR# selection is associated with DSR# and RTS# is with CTS#.

- Logic 0 = Uses RTS# and CTS# pins for auto hardware flow control.
- Logic 1 = Uses DTR# and DSR# pins for auto hardware flow control.

In Local Loopback mode (MCR[4] = 1), this bit acts as the legacy OP1 output and controls the RI bit in the MSR register, as shown in **Figure 11**.

MCR[1]: RTS# Output

The RTS# pin may be used for automatic hardware flow control by enabled by EFR bit-6 and MCR bit-2=0. If the modem interface is not used, this output may be used for general purpose.

- Logic 0 = Force RTS# output to a logic 1 (default).
- Logic 1 = Force RTS# output to a logic 0.

MCR[0]: DTR# Output

The DTR# pin may be used for automatic hardware flow control enabled by EFR bit-6 and MCR bit-2=1. If the modem interface is not used, this output may be used for general purpose.

- Logic 0 = Force DTR# output to a logic 1 (default).
- Logic 1 = Force DTR# output to a logic 0.

4.8 Line Status Register (LSR) - Read Only

This register provides the status of data transfers between the UART and the host. If IER bit-2 is set to a logic 1, an LSR interrupt will be generated immediately when any character in the RX FIFO has an error (parity, framing, overrun, break).

LSR[7]: Receive FIFO Data Error Flag

- Logic 0 = No FIFO error (default).
- Logic 1 = An indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there are no more errors in the FIFO.

LSR[6]: Transmitter Empty Flag

This bit is the Transmitter Empty indicator. This bit is set to a logic 1 whenever both the transmit FIFO (or THR, in non-FIFO mode) and the transmit shift register (TSR) are both empty. It is set to logic 0 whenever either the TX FIFO or TSR contains a data character.

LSR[5]: Transmit FIFO Empty Flag

This bit is the Transmit FIFO Empty indicator. This bit indicates that the transmitter is ready to accept a new character for transmission. This bit is set to a logic 1 when the last data byte is transferred from the transmit FIFO to the transmit shift register. The bit is reset to logic 0 as soon as a data byte is loaded into the transmit FIFO. In the non-FIFO mode this bit is set when the transmit holding register (THR) is empty; it is cleared when at a byte is written to the THR.

LSR[4]: Receive Break Flag

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO. The break indication remains until the RX input returns to the idle condition, “mark” or logic 1.

LSR[3]: Receive Data Framing Error Flag

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR.

LSR[2]: Receive Data Parity Error Flag

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The receive character in RHR (top of the FIFO) does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR.

LSR[1]: Receiver Overrun Flag

- Logic 0 = No overrun error (default).
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

LSR[0]: Receive Data Ready Indicator

- Logic 0 = No data in receive holding register or FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

4.9 Modem Status Register (MSR) - Read Only

This register provides the current state of the modem interface signals, or other peripheral device that the UART is connected. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used as general purpose inputs/outputs when they are not used with modem signals.

MSR[7]: CD Input Status

Normally this bit is the complement of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input when the modem interface is not used.

MSR[6]: RI Input Status

Normally this bit is the complement of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

MSR[5]: DSR Input Status

DSR# pin may function as automatic hardware flow control signal input if it is enabled and selected by Auto CTS/DSR bit (EFR bit-6=1) and RTS/DTR flow control select bit (MCR bit-2=1). Auto CTS/DSR flow control allows starting and stopping of local data transmissions based on the modem DSR# signal. A HIGH on the DSR# pin will stop UART transmitter as soon as the current character has finished transmission, and a LOW will resume data transmission. Normally MSR bit-5 is the complement of the DSR# input. However in the loopback mode, this bit is equivalent to the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

MSR[4]: CTS Input Status

CTS# pin may function as automatic hardware flow control signal input if it is enabled and selected by Auto CTS/DSR bit (EFR bit-6=1) and RTS/DTR flow control select bit (MCR bit-2=0). Auto CTS/DSR flow control allows starting and stopping of local data transmissions based on the modem CTS# signal. A HIGH on the CTS# pin will stop UART transmitter as soon as the current character has finished transmission, and a LOW will resume data transmission. Normally MSR bit-4 is the complement of the CTS# input. However in the loopback mode, this bit is equivalent to the RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

MSR[3]: Delta CD# Input Flag

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[2]: Delta RI# Input Flag

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from a logic 0 to a logic 1, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[1]: Delta DSR# Input Flag

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[0]: Delta CTS# Input Flag

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

4.10 Modem Status Register (MSR) - Write Only

The upper four bits 7:4 of this register set the delay in number of bits time for the auto RS485 turn around from transmit to receive.

MSR [7:4]

When Auto RS485 feature is enabled (FCTR bit-5=1) and RTS# output is connected to the enable input of a RS-485 transceiver. These 4 bits select from 0 to 15 bit-time delay after the end of the last stop-bit of the last transmitted character. This delay controls when to change the state of RTS# output. This delay is very useful in long-cable networks. **Table 16** shows the selection. The bits are enabled by EFR bit-4.

TABLE 16: AUTO RS485 HALF-DUPLEX DIRECTION CONTROL DELAY FROM TRANSMIT-TO-RECEIVE

MSR[7]	MSR[6]	MSR[5]	MSR[4]	DELAY IN DATA BIT(S) TIME
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
9	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

MSR [3]: Transmitter Disable

This bit can be used to disable the transmitter by halting the Transmit Shift Register (TSR). When this bit is set to a '1', the bytes already in the FIFO will not be sent out. Also, any more data loaded into the FIFO will stay in the FIFO and will not be sent out. When this bit is set to a '0', the bytes currently in the TX FIFO will be sent out. Please note that setting this bit to a '1' stops any character from going out. Also, this bit must be a '0' for Send Char Immediate function (see MCR[3]).

- Logic 0 = Enable Transmitter (default).
- Logic 1 = Disable Transmitter.

MSR [2]: Receiver Disable

This bit can be used to disable the receiver by halting the Receive Shift Register (RSR). When this bit is set to a '1', the receiver will not receive any more characters until it is enabled again by setting this bit to a '0'. Data currently in the RX FIFO can be read out. Please note that setting this bit to a '1' prevents any character from coming in.

- Logic 0 = Enable Receiver (default).
- Logic 1 = Disable Receiver.

MSR [1:0]: Reserved

4.11 SCRATCH PAD REGISTER (SPR) - Read/Write

This is a 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

4.12 FEATURE CONTROL REGISTER (FCTR) - Read/Write

This register controls the UART enhanced functions that are not available on ST16C554 or ST16C654.

FCTR[7:6]: TX and RX FIFO Trigger Table Select

These 2 bits select the transmit and receive FIFO trigger level table A, B, C or D. When table A, B, or C is selected the auto RTS flow control trigger level is set to "next FIFO trigger level" for compatibility to ST16C550 and ST16C650 series. RTS/DTR# triggers on the next level of the RX FIFO trigger level, in another word, one FIFO level above and one FIFO level below. See in **Table 14** for complete selection with FCR bit 4-5 and FCTR bit 6-7, i.e. if Table C is used on the receiver with RX FIFO trigger level set to 56 bytes, RTS/DTR# output will de-assert at 60 and re-assert at 16.

FCTR[5]: Auto RS485 Enable

Auto RS485 half duplex control enable/disable.

- Logic 0 = Standard ST16C550 mode. Transmitter generates an interrupt when transmit holding register (THR) becomes empty. Transmit Shift Register (TSR) may still be shifting data bit out.
- Logic 1 = Enable Auto RS485 half duplex direction control. RTS# output changes its logic level from HIGH to LOW when finished sending the last stop bit of the last character out of the TSR register. It changes from LOW to HIGH when a data byte is loaded into the THR or transmit FIFO. The change to HIGH occurs prior sending the start-bit. It also changes the transmitter interrupt from transmit holding to transmit shift register (TSR) empty.

FCTR[4]: Infrared RX Input Logic Select

- Logic 0 = Select RX input as active HIGH encoded IrDA data, normal, (default).
- Logic 1 = Select RX input as active LOW encoded IrDA data, inverted.

FCTR [3:0] - Auto RTS/DTR Flow Control Hysteresis Select

These bits select the auto RTS/DTR flow control hysteresis and only valid when TX and RX Trigger Table-D is selected (FCTR bit-6 and 7 are set to logic 1). The RTS/DTR hysteresis is referenced to the RX FIFO trigger level. After reset, these bits are set to logic 0 selecting the next FIFO trigger level for hardware flow control. **Table 17** shows the 16 selectable hysteresis levels.

TABLE 17: 16 SELECTABLE HYSTERESIS LEVELS WHEN TRIGGER TABLE-D IS SELECTED

FCTR BIT-3	FCTR BIT-2	FCTR BIT-1	FCTR BIT-0	RTS/DTR HYSTERESIS (CHARACTERS)
0	0	0	0	0
0	0	0	1	+/- 4
0	0	1	0	+/- 6
0	0	1	1	+/- 8
0	1	0	0	+/- 8
0	1	0	1	+/- 16
0	1	1	0	+/- 24
0	1	1	1	+/- 32
1	1	0	0	+/- 12
1	1	0	1	+/- 20
1	1	1	0	+/- 28
1	1	1	1	+/- 36
1	0	0	0	+/- 40
1	0	0	1	+/- 44
1	0	1	0	+/- 48
1	0	1	1	+/- 52

4.13 Enhanced Feature Register (EFR) - Read/Write

Enhanced features are enabled or disabled using this register. Bits 3:0 provide single or dual consecutive character software flow control selection (see **Table 18**). When the Xon1 and Xon2 and Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential characters. Caution: note that whenever changing the TX or RX flow control bits, always reset all bits back to logic 0 (disable) before programming a new setting.

EFR[7]: Auto CTS Flow Control Enable

Automatic CTS or DSR Flow Control.

- Logic 0 = Automatic CTS/DSR flow control is disabled (default).
- Logic 1 = Enable Automatic CTS/DSR flow control. Transmission stops when CTS/DSR# pin de-asserts (HIGH). Transmission resumes when CTS/DSR# pin is asserted (LOW). The selection for CTS# or DSR# is through MCR bit-2.

EFR[6]: Auto RTS or DTR Flow Control Enable

RTS#/DTR# output may be used for hardware flow control by setting EFR bit-6 to logic 1. When Auto RTS/DTR is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and RTS/DTR# will de-assert (HIGH) at the next upper trigger or selected hysteresis level. RTS/DTR# will re-assert (LOW) when FIFO data falls below the next lower trigger or selected hysteresis level (see FCTR bits 4-7). The RTS# or DTR# output must be asserted (LOW) before the auto RTS/DTR can take effect. The selection for RTS# or DTR# is through MCR bit-2. RTS/DTR# pin will function as a general purpose output when hardware flow control is disabled.

- Logic 0 = Automatic RTS/DTR flow control is disabled (default).
- Logic 1 = Enable Automatic RTS/DTR flow control.

EFR[5]: Special Character Detect Enable

- Logic 0 = Special Character Detect Disabled (default).
- Logic 1 = Special Character Detect Enabled. The UART compares each incoming receive character with data in Xoff-2 register. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of the special character. Bit-0 corresponds with the LSB bit for the receive character. If flow control is set for comparing Xon1, Xoff1 (EFR [1:0]=10) then flow control and special character work normally. However, if flow control is set for comparing Xon2, Xoff2 (EFR[1:0]=01) then flow control works normally, but Xoff2 will not go to the FIFO, and will generate an Xoff interrupt and a special character interrupt.

EFR[4]: Enhanced Function Bits Enable

Enhanced function control bit. This bit enables the enhanced functions in IER bits 7:5, ISR bits 5:4, FCR bits 5:4, MCR bits 7:5, 3:2 and MSR 7:2 bits to be modified. After modifying any enhanced bits, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents legacy software from altering or overwriting the enhanced functions once set. Normally, it is recommended to leave it enabled, logic 1.

- Logic 0 = modification disable/latch enhanced features. IER bits 7:5, ISR bits 5:4, FCR bits 5:4, MCR bits 7:5, 3:2 and MSR 7:2 bits are saved to retain the user settings. After a reset, all these bits are set to a logic 0 to be compatible with ST16C550 mode (default).
- Logic 1 = Enables the enhanced functions. When this bit is set to a logic 1 all enhanced features are enabled.

EFR[3:0]: Software Flow Control Select

Combinations of software flow control can be selected by programming these bits, as shown in **Table 18** below.

TABLE 18: SOFTWARE FLOW CONTROL FUNCTIONS

EFR BIT-3	EFR BIT-2	EFR BIT-1	EFR BIT-0	TRANSMIT AND RECEIVE SOFTWARE FLOW CONTROL
0	0	0	0	No TX and RX flow control (default and reset)
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1 and Xon2, Xoff1 and Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	1	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1 and Xon2, Xoff1 and Xoff2 Receiver compares Xon1 and Xon2, Xoff1 and Xoff2
0	0	1	1	No transmit flow control Receiver compares Xon1 and Xon2, Xoff1 and Xoff2

4.14 TXCNT[7:0]: Transmit FIFO Level Counter - Read Only

Transmit FIFO level byte count from 0x00 (zero) to 0x40 (64). This 8-bit register gives an indication of the number of characters in the transmit FIFO. The FIFO level Byte count register is read only. The user can take advantage of the FIFO level byte counter for faster data loading to the transmit FIFO, which reduces CPU bandwidth requirements.

4.15 TXTRG [7:0]: Transmit FIFO Trigger Level - Write Only

An 8-bit value written to this register sets the TX FIFO trigger level from 0x00 (zero) to 0x40 (64). The TX FIFO trigger level generates an interrupt whenever the data level in the transmit FIFO falls below this preset trigger level.

4.16 RXCNT[7:0]: Receive FIFO Level Counter - Read Only

Receive FIFO level byte count from 0x00 (zero) to 0x40 (64). It gives an indication of the number of characters in the receive FIFO. The FIFO level byte count register is read only. The user can take advantage of the FIFO level byte counter for faster data unloading from the receiver FIFO, which reduces CPU bandwidth requirements.

4.17 RXTRG[7:0]: Receive FIFO Trigger Level - Write Only

An 8-bit value written to this register, sets the RX FIFO trigger level from 0x00 (zero) to 0x40 (64). The RX FIFO trigger level generates an interrupt whenever the receive FIFO level rises to this preset trigger level.

4.18 XOFF1, XOFF2, XON1 AND XON2 REGISTERS, WRITE ONLY

These registers are used to program the Xoff1, Xoff2, Xon1 and Xon2 control characters respectively.

4.19 XCHAR REGISTER, READ ONLY

This register gives the status of the last sent control character (xon or xoff) and the last received control character (xon or xoff). This register will be reset to 0x00 if, at anytime, the Software Flow Control is disabled.

XCHAR [7:4] : Reserved

XCHAR [3]: Transmit Xon Indicator

If the last transmitted control character was a xon character or characters (xon1, xon2), this bit will be set to a logic 1. This bit will clear after the read.

XCHAR [2]: Transmit Xoff Indicator

If the last transmitted control character was a xoff character or characters (xoff1, xoff2), this bit will be set to a logic 1. This bit will clear after the read.

XCHAR [1]: Xon Detect Indicator

If the last received control character was a xon character or characters (xon1, xon2), this bit will be set to a logic 1. This bit will clear after the read.

XCHAR [0]: Xoff Detect Indicator

If the last received control character was a xoff character or characters (xoff1, xoff2), this bit will be set to a logic 1. This bit will clear after the read.

TABLE 19: UART RESET CONDITIONS

REGISTERS	RESET STATE
DLL	Bits 7-0 = 0x01
DLM	Bits 7-0 = 0x00
DLD	Bits 7-0 = 0x00
RHR	Bits 7-0 = 0xXX
THR	Bits 7-0 = 0xXX
IER	Bits 7-0 = 0x00
FCR	Bits 7-0 = 0x00
ISR	Bits 7-0 = 0x01
LCR	Bits 7-0 = 0x00
MCR	Bits 7-0 = 0x00
LSR	Bits 7-0 = 0x60
MSR	Bits 3-0 = logic 0 Bits 7-4 = logic levels of the inputs
SPR	Bits 7-0 = 0xFF
FCTR	Bits 7-0 = 0x00
EFR	Bits 7-0 = 0x00
TFCNT	Bits 7-0 = 0x00
TFTRG	Bits 7-0 = 0x00
RFCNT	Bits 7-0 = 0x00
RFTRG	Bits 7-0 = 0x00
XCHAR	Bits 7-0 = 0x00
XON1	Bits 7-0 = 0x00
XON2	Bits 7-0 = 0x00
XOFF1	Bits 7-0 = 0x00
XOFF2	Bits 7-0 = 0x00

I/O SIGNALS	RESET STATE
TX[ch-3:0]	HIGH
IRTX[ch-3:0]	LOW
RTS#[ch-3:0]	HIGH
DTR#[ch-3:0]	HIGH

ABSOLUTE MAXIMUM RATINGS

Power Supply Range	4 Volts
Voltage at Any Pin	-0.5 to 4V
Operating Temperature	-40^{o} to +85^{o} C
Storage Temperature	-65^{o} to +150^{o} C
Package Dissipation	500 mW
Thermal Resistance (10x10x1.4mm 64-LQFP)	θ-ja = 70°C/W , θ-jc = 14°C/W

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS

TA=0^{o} to 70^{o}C (-40^{o} to +85^{o}C for industrial grade package), Vcc is 2.25V to 3.6V

SYMBOL	PARAMETER	2.5V MIN	2.5V MAX	3.3V MIN	3.3 MAX	UNITS	CONDITIONS
V_{ILCK}	Clock input low level	-0.3	0.6	-0.3	0.6	V	
V_{IHCK}	Clock input high level	1.8	4	2.4	6	V	
V_{IL}	Input Low Voltage	-0.3	0.5	-0.3	0.7	V	
V_{IH}	Input High Voltage	1.8		2.0		V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 6mA
V_{OH}	Output High Voltage	1.8		2.4		V V	I_{OH} = -6mA I_{OH} = -3mA
I_{IL}	Input Low Leakage Current		-10		-10	uA	
I_{IH}	Input High Leakage Current		10		10	uA	
C_{IN}	Input Pin Capacitance		5		5	pF	
I_{CC}	Power Supply Current		5		5	mA	EXT Clock=2MHz A7-A0 at GND, all inputs at VCC or GND and outputs unloaded
I_{SLEEP}	Sleep Current		60		60	uA	All UARTs asleep. A7-A0 at GND, all inputs at VCC or GND and outputs unloaded.

AC ELECTRICAL CHARACTERISTICS

TA=0^{o} to 70^{o}C (-40^{o} to $+85^{o}$C for industrial grade package), Vcc is 2.25V to 3.6V, 70 pF Load where applicable

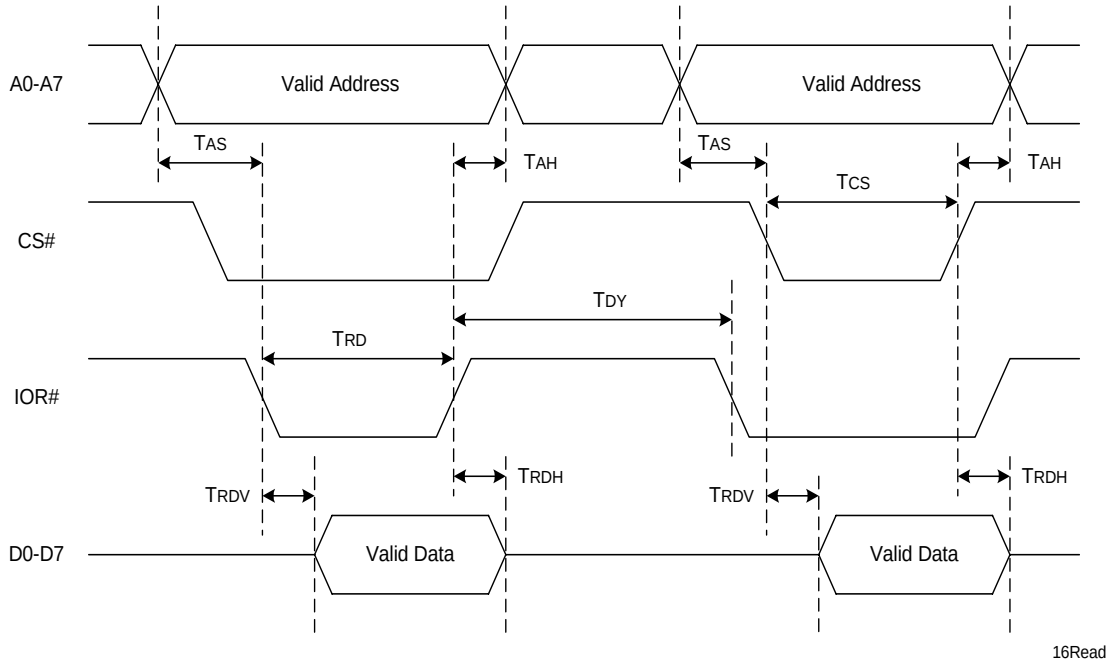
SYMBOL	PARAMETER	2.5V MIN	2.5V MAX	3.3V MIN	3.3V MAX	UNITS
T_{C1},T_{C2}	Clock Pulse Period	10		7		ns
T_{OSC}	Crystal Frequency		24		24	MHz
T_{ECK}	External Clock Frequency		50		64	MHz
T_{AS}	Address Setup (16 Mode)	3		3		ns
T_{AH}	Address Hold (16 Mode)	3		3		ns
T_{CS}	Chip Select Width (16 Mode)	25		25		ns
T_{DY}	Delay between CS# Active Cycles (16 Mode)	25		25		ns
T_{RD}	Read Strobe Width (16 Mode)	25		25		ns
T_{WR}	Write Strobe Width (16 Mode)	20		20		ns
T_{RDV}	Read Data Valid (16 Mode)		20		20	ns
T_{WDS}	Write Data Setup (16 Mode)	10		10		ns
T_{RDH}	Read Data Hold (16 Mode)		15		15	ns
T_{WDH}	Write Data Hold (16 Mode)	7		7		ns
T_{ADS}	Address Setup (68 Mode)	3		3		ns
T_{ADH}	Address Hold (68 Mode)	3		3		ns
T_{RWS}	R/W# Setup to CS# (68 Mode)	3		3		ns
T_{RDA}	Read Data Access (68 mode)	20		20		ns
T_{RDH}	Read Data Hold (68 mode)		15		15	ns
T_{WDS}	Write Data Setup (68 mode)	10		10		ns
T_{WDH}	Write Data Hold (68 Mode)	7		7		ns
T_{RWH}	CS# De-asserted to R/W# De-asserted (68 Mode)	1		1		ns
T_{CSL}	CS# Width (68 Mode)	25		25		ns
T_{CSD}	CS# Cycle Delay (68 Mode)	25		25		ns
T_{WDO}	Delay from IOW# to Modem Output		50		50	ns
T_{MOD}	Delay to set Interrupt from Modem Input		50		50	ns
T_{RSI}	Delay To Reset Interrupt From IOR#		50		50	ns
T_{SSI}	Delay From Stop To Set Interrupt		1		1	Bclk
T_{RRI}	Delay From IOR# To Reset Interrupt		45		45	ns

AC ELECTRICAL CHARACTERISTICS

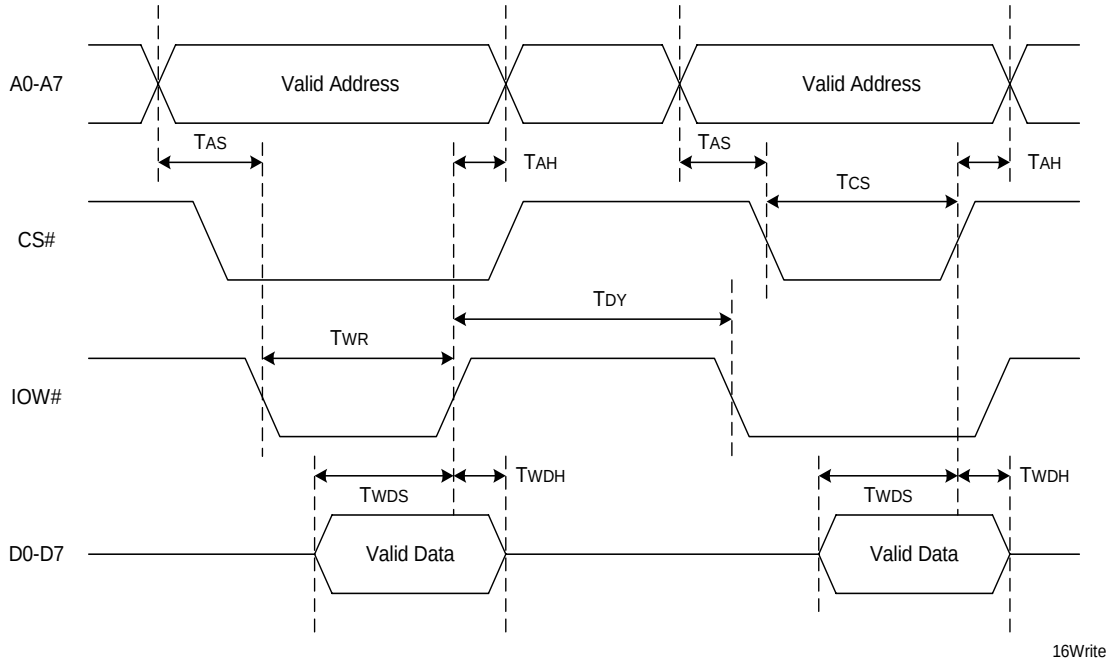
TA=0^{o} to 70^{o}C (-40^{o} to +85^{o}C for industrial grade package), Vcc is 2.25V to 3.6V, 70 pF Load where applicable

SYMBOL	PARAMETER	2.5V MIN	2.5V MAX	3.3V MIN	3.3V MAX	UNITS
T_{SI}	Delay From Stop To Interrupt		45		45	ns
T_{WRI}	Delay From IOW# To Reset Interrupt		45		45	ns
T_{RST}	Reset Pulse	40		40		ns
Bclk	Baud Clock	16X or 8X of data rate				Hz

FIGURE 16. 16 MODE (INTEL) DATA BUS READ AND WRITE TIMING

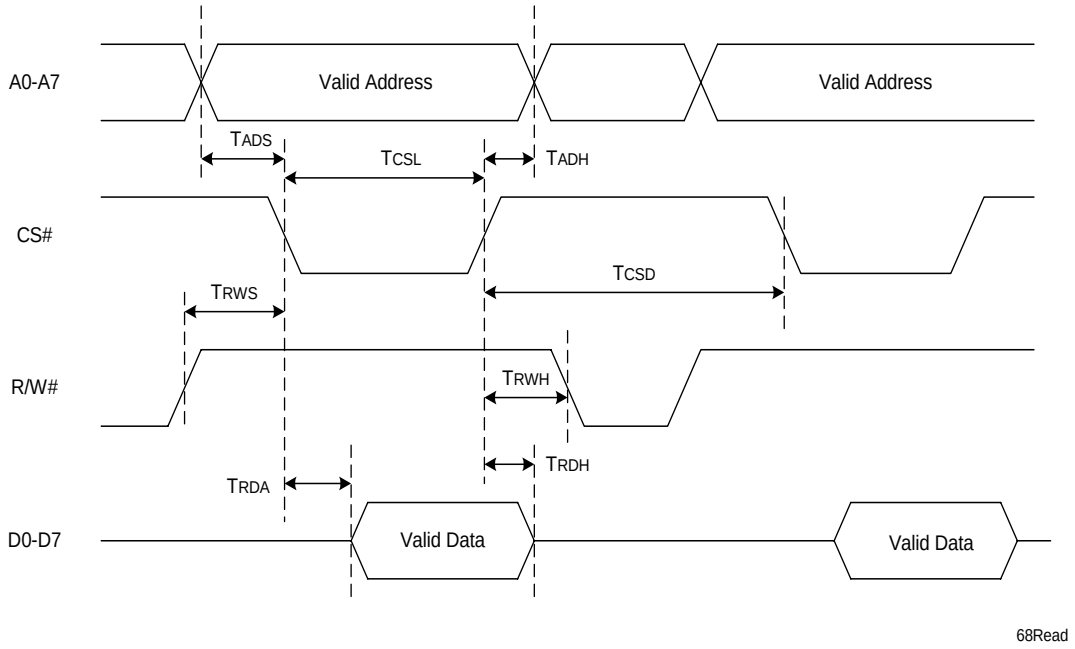


16 Mode (Intel) Data Bus Read Timing

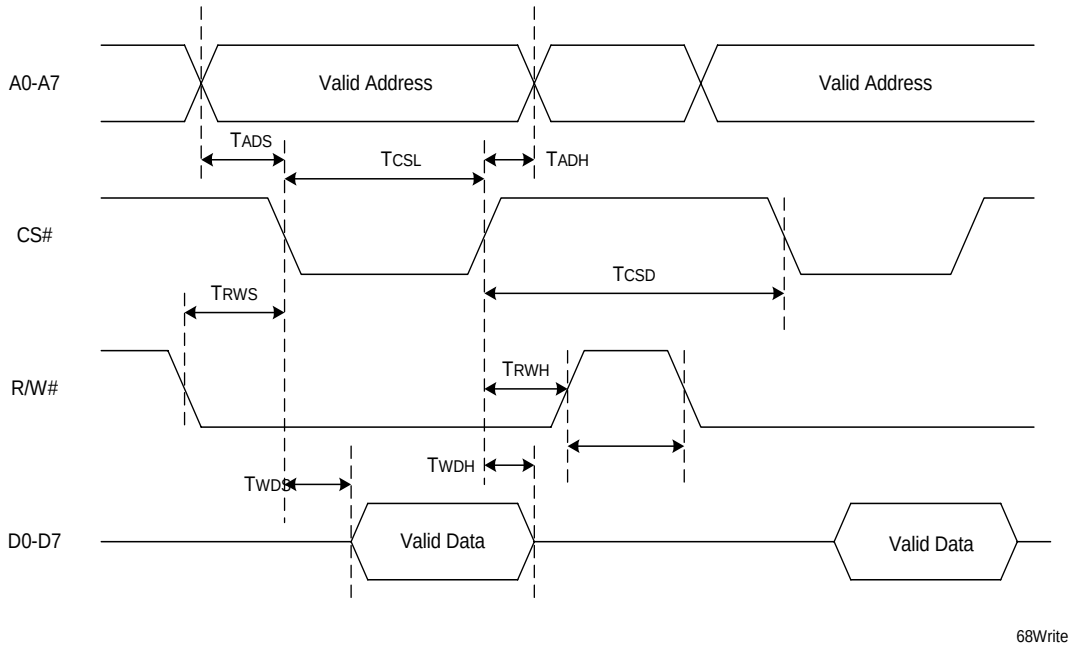


16 Mode (Intel) Data Bus Write Timing

FIGURE 17. 68 MODE (MOTOROLA) DATA BUS READ AND WRITE TIMING



68 Mode (Motorola) Data Bus Read Timing



68 Mode (Motorola) Data Bus Write Timing

FIGURE 18. MODEM INPUT/OUTPUT TIMING

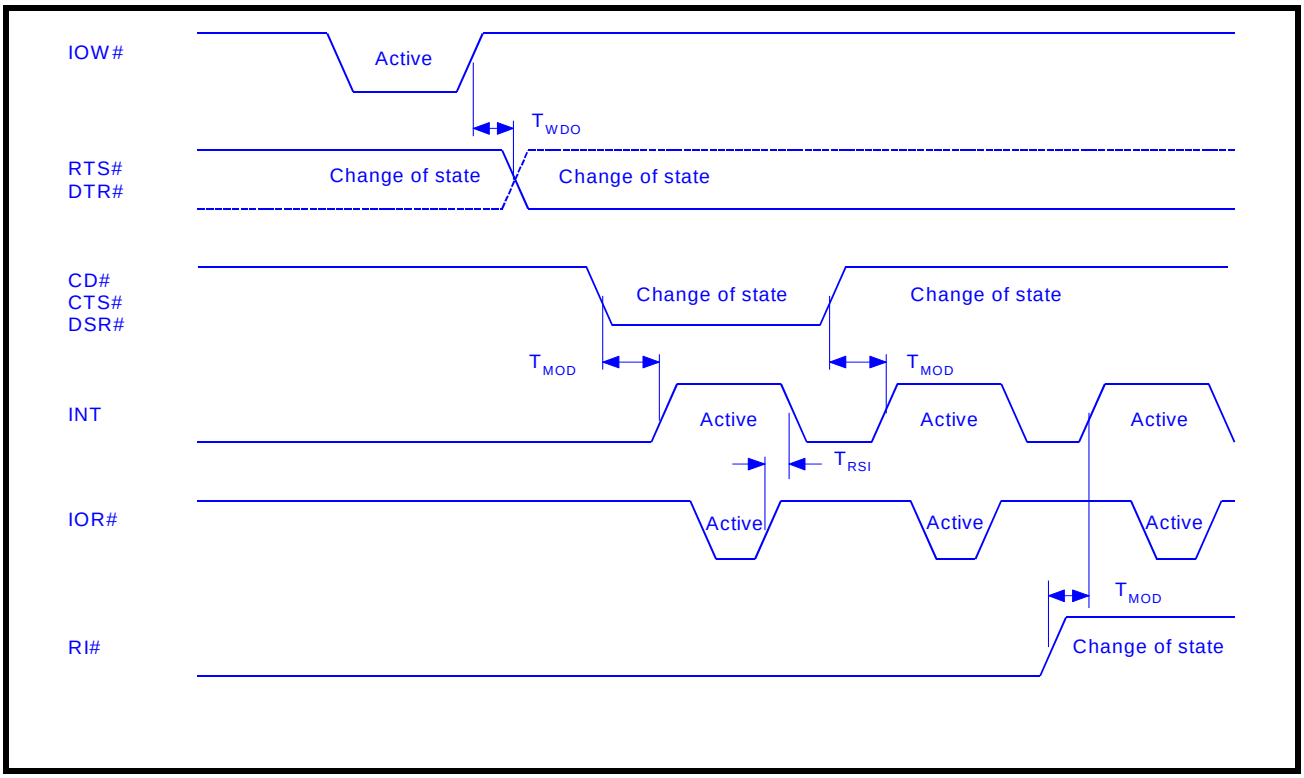


FIGURE 19. RECEIVE INTERRUPT TIMING [NON-FIFO MODE]

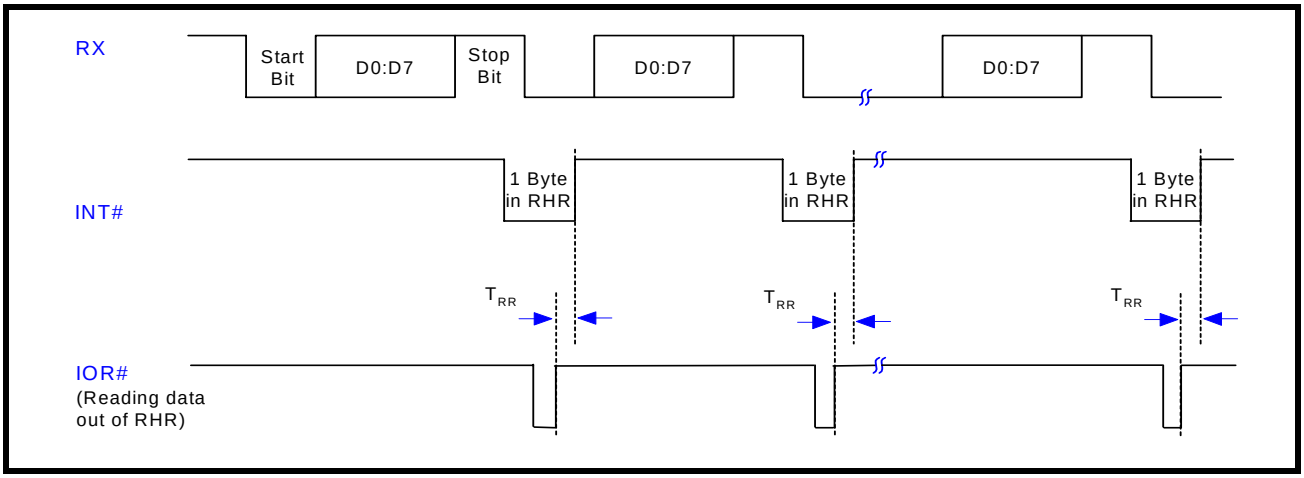


FIGURE 20. TRANSMIT INTERRUPT TIMING [NON-FIFO MODE]

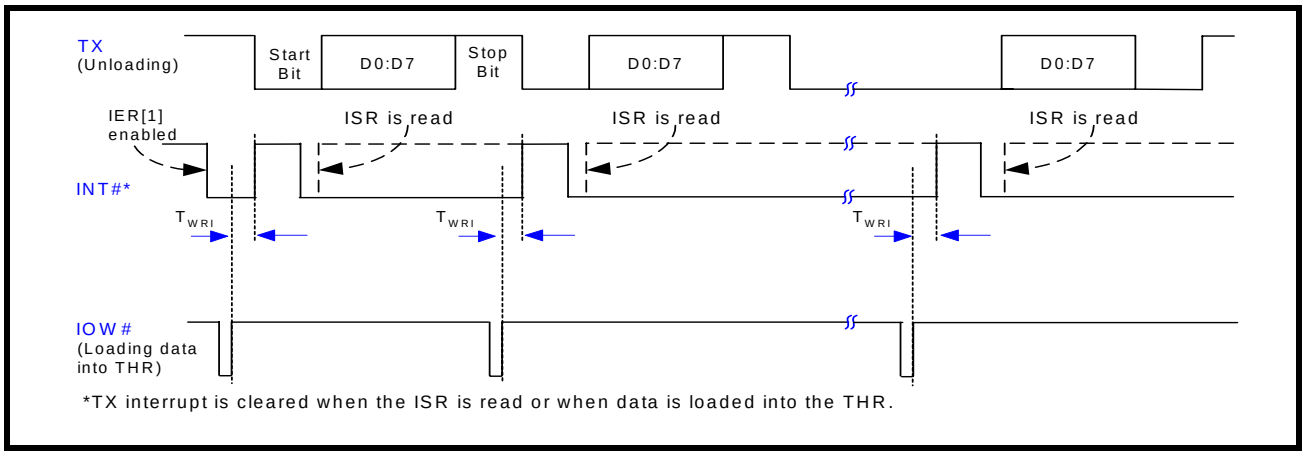


FIGURE 21. RECEIVE INTERRUPT TIMING [FIFO MODE]

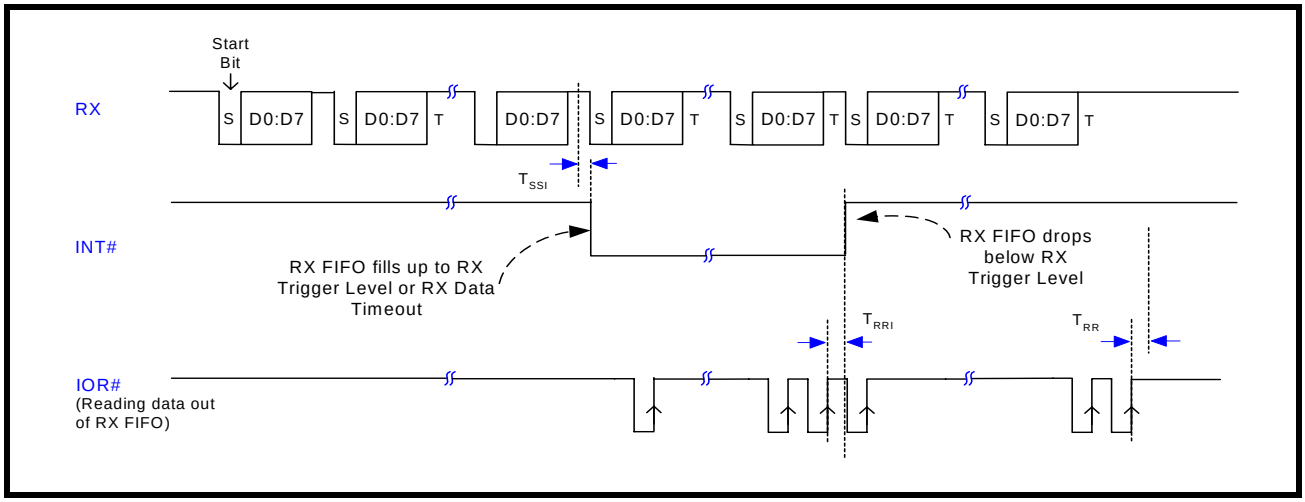
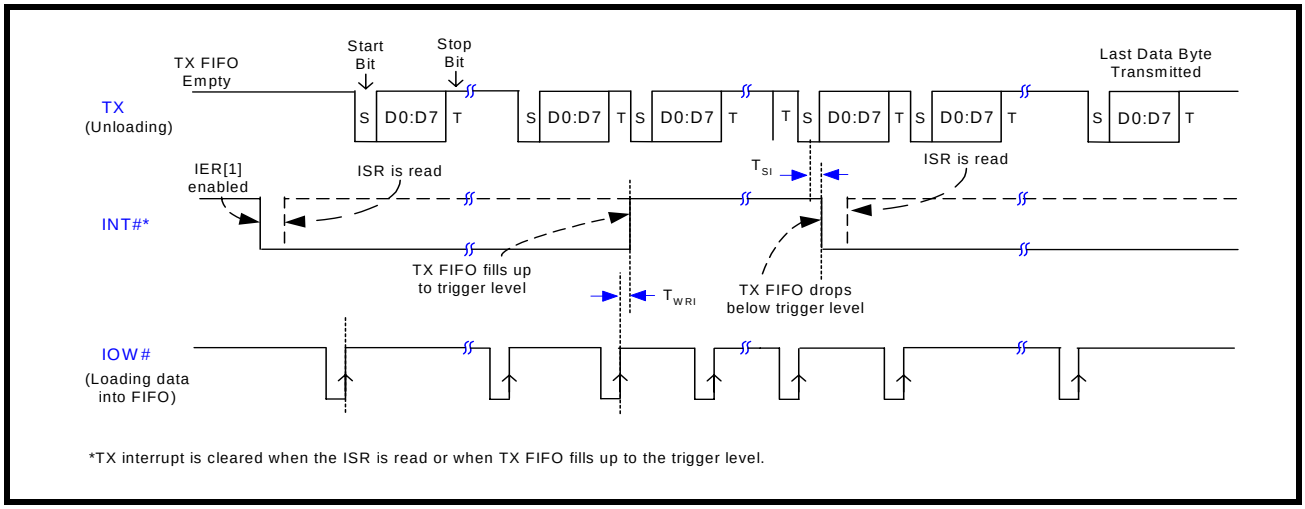
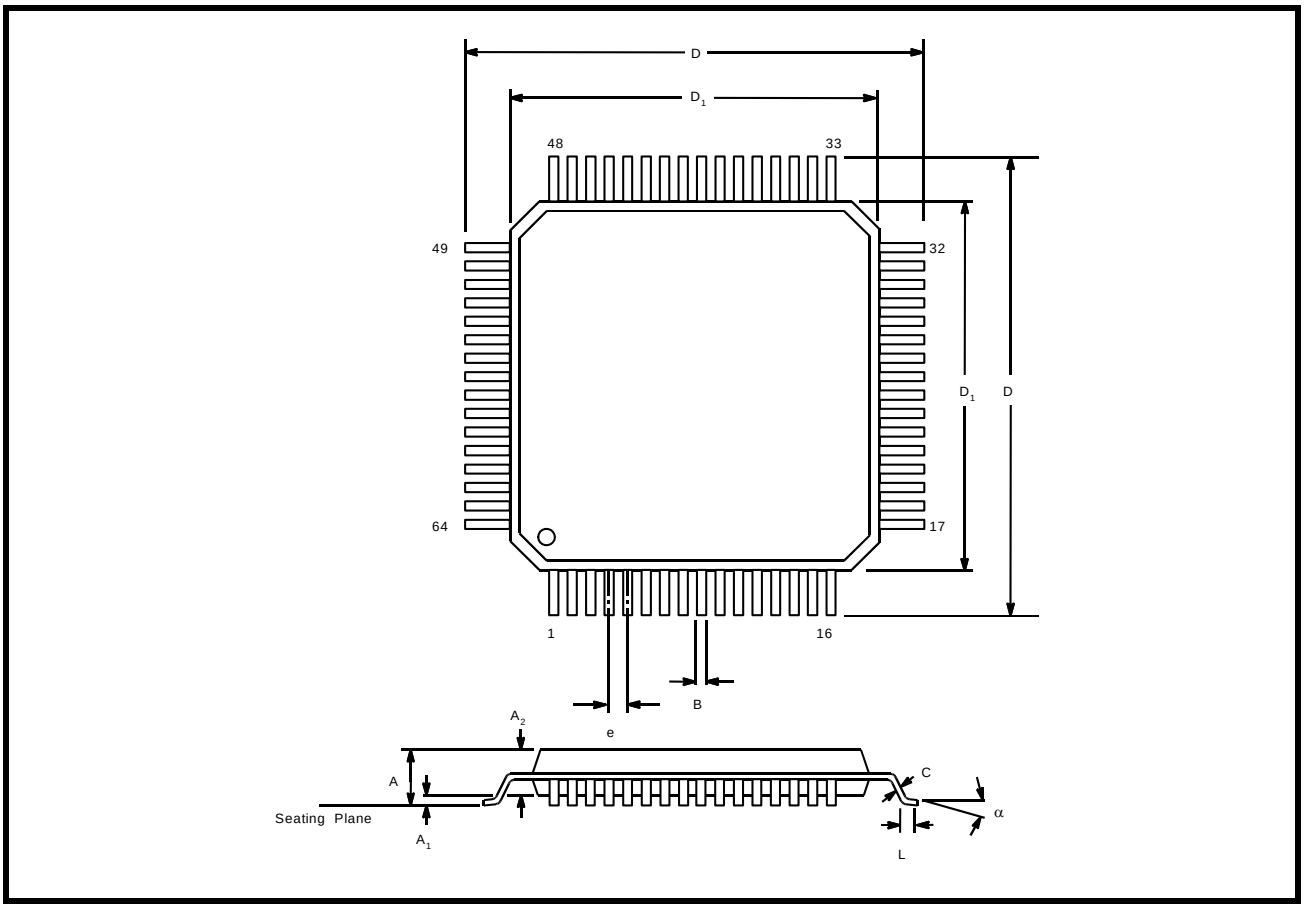


FIGURE 22. TRANSMIT INTERRUPT TIMING [FIFO MODE]



PACKAGE DIMENSIONS

64 LEAD LOW-PROFILE QUAD FLAT PACK (10 x 10 x 1.4 mm LQFP)



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.465	0.480	11.80	12.20
D1	0.390	0.398	9.90	10.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

REVISION HISTORY

REVISION	DATE	DESCRIPTION
A1.0.0	June 2005	Advanced Datasheet.
A1.0.1	March 2006	Updated the 1.4mm-thick Quad Flat Pack package description from "TQFP" to "LQFP" to be consistent with JEDEC and Industry norms.
P1.0.0	October 2006	Preliminary Datasheet.
1.0.0	May 2007	Final Datasheet.
1.0.1	July 2008	Corrected description of Xon/Xoff/Special character interrupt.

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