LM7480x-Q1 Ideal Diode Controller with Load Dump Protection

ADVANCE INFORMATION

1 Features

- AEC-Q100 Qualified with the following results
  - Device temperature grade 1: –40°C to +125°C Ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- 3-V to 65-V Input range
- Reverse input protection down to –65 V
- Drives external back-to-back N-Channel MOSFETs in common drain and common source configurations
- Ideal diode operation with 10.5-mV A to C forward voltage drop regulation
- Fast response to reverse current blocking: < 0.6µs
- 20-mA peak gate (DGATE) turnon current
- 1.5-A Peak DGATE turnoff current
- Adjustable over-voltage protection
- Low 3 µA shutdown current (EN=Low)
- Meets automotive ISO7637 transient requirements with a suitable TVS diode
- Available in space saving 12-Pin WSON package

2 Applications

- Automotive battery protection
  - ADAS domain controller
  - Camera ECU
  - Head Unit
  - USB HUBs
- Active ORing for redundant power

3 Description

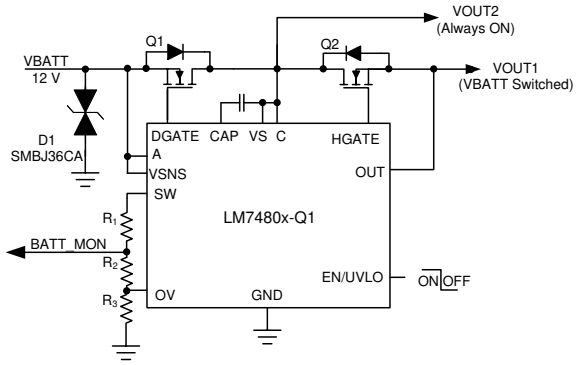
The LM7480x-Q1 ideal diode controller drives and controls external back to back N-Channel MOSFETs to emulate an ideal diode rectifier with power path ON/OFF control and over voltage protection. The wide input supply of 3V to 65V allows protection and control of 12-V and 24-V automotive battery powered ECUs. The device can withstand and protect the loads from negative supply voltages down to –65 V. An integrated ideal diode controller (DGATE) drives the first MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. With a second MOSFET in the power path the device allows load disconnect (ON/OFF control) and over voltage protection using HGATE control. The device features an adjustable over voltage cut-off protection feature. The LM7480x-Q1 controller can drive the external MOSFETs in Common Drain and Common Source configurations. With Common Drain configuration of the power MOSFETs, the mid-point can be utilized for OR-ing designs using an another ideal diode. The LM7480x-Q1 has a maximum voltage rating of 65-V. The loads can be protected from extended over voltage transients like 200-V Unsuppressed Load Dumps in 24-V Battery systems by configuring the device with external MOSFETs in Common Source topology.

Table 1. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM74800-Q1, LM74801-Q1,	WSON (12)	3.0 mm x 3.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Ideal Diode with Switched Output



Ideal Diode with 200-V Load Dump Protection

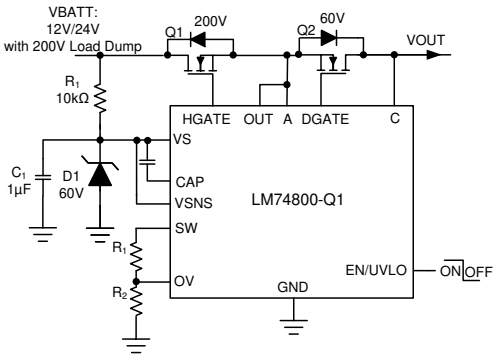


Table of Contents

ADVANCE INFORMATION

4 Revision History

Changes from Original (April 22 2020) to Revision *2 **Page**

- Changed second paragraph of Application Information ... 13

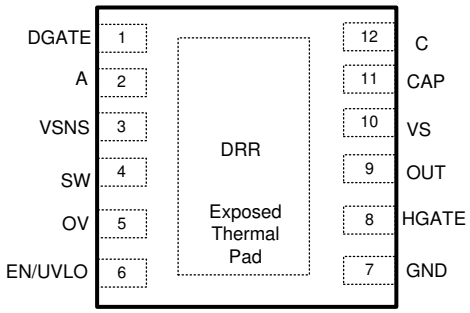
DATE	REVISION	NOTES
May 2020	A is APL/AI	2nd Advance Information release.
April 2020	*	Advance Information release.

5 Device Comparison Table

	LM74800-Q1	LM74801-Q1
Reverse Current Blocking	$V_{(A-C)}$ linear regulation and comparator	$V_{(A-C)}$ comparator only

6 Pin Configuration and Functions

WSON
12-Pin DRR
Transparent Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	LM7480x-Q1		
	DRR-12 (WSON)		
DGATE	1	O	Diode Controller Gate Drive Output. Connect to the GATE of the external MOSFETAnode of the ideal diode.
A	2	I	Anode of the ideal diode. Connect to the source of the external MOSFET
VSNS	3	I	Voltage sensing input.
SW	4	I	Voltage sensing disconnect switch terminal. VSNS and SW are internally connected through a switch. Use SW as the top connection of the battery sensing or OV resistor ladder network. When EN/UVLO is pulled low, the switch is OFF disconnecting the resistor ladder from the battery line thereby cutting off the leakage current. If the internal disconnect switch between VSNS and SW is not used then short them together and connect to VS pin.
OV	5	I	Adjustable over voltage threshold input. Connect a resistor ladder across SW to OV terminal. When the voltage at OVP exceeds the over voltage cut-off threshold then the HGATE is pulled low turning OFF the HSFET. HGATE turns ON when the sense voltage goes below the OVP falling threshold.
EN/UVLO	6	I	EN/UVLO Input. Connect to VS pin for always ON operation. Can be driven externally from a micro controller I/O. Pulling it low below 0.6V enters the device in low Iq shutdown mode. For UVLO, connect an external resistor ladder to EN/UVLO to GND.
GND	7	G	Connect to the system ground plane.
HGATE	8	O	GATE driver output for the HSFET. Connect to the GATE of the external FET
OUT	9	I	Connect to the output rail (external MOSFET source).
VS	10	I	Input power supply to the IC. Connect VS to middle point of the common drain back to back MOSFET configuration. Connect a 100nF capacitor across VS and GND pins.
CAP	11	O	Charge pump output. Connect a 100nF capacitor across CAP and VS pins.
C	12	I	Cathode of the ideal diode. Connect to the drain of the external MOSFET
RTN	Thermal Pad	—	Leave exposed pad floating. Do Not connect to GND plane.

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	A to GND	–65	70	V
	VS to GND	–1	70	V
	EN/UVLO, C, SNS, SW, OV, OUT to GND, $V_{(A)} > 0$ V	–0.3	70	V
	EN/UVLO, C, SNS, SW, OV, OUT to GND, $V_{(A)} \leq 0$ V	$V_{(A)}$	$(70 + V_{(A)})$	V
	RTN to GND	–65	0.3	V
	OUT to VS	–65	16.5	V
Output Pins	CAP to VS	–0.3	15	V
	CAP to A	–0.3	85	V
	DGATE to A	–0.3	15	V
	HGATE to OUT	–0.3	15	V
Output to Input Pins	C to A	–5	85	V
Operating junction temperature, T_j(2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (DGATE, OV, and C)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	A to GND	–60		65	V
Input Pins	VS to GND			65	V
Input Pins	EN/UVLO to GND			65	V
External Capacitance	A to GND, VS to GND, CAP to A	0.1			µF
External MOSFET max VGS rating	DGATE to A and HGATE to OUT	15			V
Tj	Operating Junction temperature(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

ADVANCE INFORMATION

7.4 Thermal Information

THERMAL METRIC(1)		LM7480x-Q1 DRR (WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)} = V_{(C)} = V_{(OUT)} = V_{(VS)}$ = 12 V, $V_{(CAP)} – V_{(S)}$ = 15 V, $V_{(AC)}$ = 20 mV, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(VS)}$	Operating input voltage		3		65	V
$V_{(VS\_PORR)}$	VS POR threshold, rising			2.72	2.85	V
$V_{(VS\_PORF)}$	VS POR threshold, falling		1.9	2.08	2.3	V
$I_{(SHDN)}$	SHDN current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 0 V		3	5	µA
$I_{(Q)}$	Total System Quiescent current, $I_{(GND)}$	$V_{(EN/UVLO)}$ = 2 V		428		µA
$I_{(REV)}$	Leakage current during Reverse Polarity, $I_{(GND)}$, $I_{(OUT)}$	0 V < $V_{(A)}$ < – 65V			110	µA
ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT						
$V_{(UVLOR)}$	EN/UVLO threshold voltage, rising		1.194	1.237	1.267	V
$V_{(UVLOF)}$	EN/UVLO threshold voltage, falling		1.11	1.128	1.169	V
$V_{(ENF)}$	EN/UVLO threshold voltage for low Iq shutdown, falling		0.3	0.67		V
$V_{(ENhys)}$	Enable Hysteresis			66		mV
$I_{(EN/UVLO)}$		0 V < $V_{(EN/UVLO)}$ < 65 V			1	µA
OVER VOLTAGE PROTECTION AND BATTERY SENSING (VSNS, SW, OV) INPUT						
$R_{(SW)}$	Battery sensing disconnect switch resistance		10	24		Ω
$V_{(OVR)}$	Overvoltage threshold input, risIng		1.194	1.233	1.267	V
$V_{(OVF)}$	Overvoltage threshold input, falling		1.11	1.123	1.169	V
$I_{(OV)}$	OV Input leakage current	0 V < $V_{(OV)}$ < 65 V			1	µA
CHARGE PUMP (CAP)						
$I_{(CAP)}$	Charge Pump/DGATE Driver Supply current	$V_{(CAP)} – V_{(A)}$ = 7 V, 6 V< $V_{(VS)}$ < 65 V	0.6			mA
VCAP – VS	Charge Pump Turn ON voltage			12.2		V
	Charge Pump Turnoff voltage			13.2	13.9	V
	Charge Pump UVLO voltage threshold, rising			6.7		V
	Charge Pump UVLO voltage threshold, falling			5.5		V
IDEAL DIODE (A, C, DGATE)						
$V_{(AC\_REG)}$	Regulated Forward V_A–V_C Threshold	LM74800-Q1 Only		10.5		mV
$V_{(AC\_FWD)}$	V_A–V_C threshold for reverse to forward conduction			175		mV

ADVANCE INFORMATION

Electrical Characteristics (continued)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)} = V_{(C)} = V_{(OUT)} = V_{(VS)}$ = 12 V, $V_{(CAP)} – V_{(S)}$ = 15 V, $V_{(AC)}$ = 20 mV, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(AC\_REV)}$	V_A–V_C Threshold for Fast Reverse Current Blocking			–4.5		mV
$V_{(DGATE)}$- $V_{(A)}$	Gate Drive Voltage	3 V < V_S < 65 V	7	10	13	V
$I_{(DGATE)}$	Peak Gate Source current	$V_A – V_C$ = 100 mV, $V_{DGATE} – V_A$ = 1 V		20		mA
	Peak Gate Sink current	$V_A – V_C$ = –12 mV, $V_{DGATE} – V_A$ = 11 V		1500		mA
	Regulation sink current	$V_A – V_C$ = 0 V, $V_{DGATE} – V_A$, LM74800-Q1 Only	10			µA
I_C	Cathode leakage Current	V_A = 0 V, V_C = 12 V		10		µA
		V_A = –14 V, V_C = 12 V		10		µA
HIGH SIDE CONTROLLER (HGATE, OUT)						
$V_{(HGATE)} – V_{(OUT)}$	Gate Drive Voltage	3 V < $V_{(VS)}$ < 65 V	7		14.5	V
$I_{(HGATE)}$	Source Current	3 V < $V_{(VS)}$ < 65 V		53		µA
$I_{(HGATE)}$	Sink Current	$V_{(OV)}$ > $V_{(OVR)}$		260		mA

7.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)} = V_{(C)} = V_{(OUT)} = V_{(VS)}$ = 12 V, $V_{(CAP)} – V_{(S)}$ = 15 V, $V_{(AC)}$ = 20 mV, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN/UVLO)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DGATE\_OFF(dly)}$	DGATE Turnoff Delay during reverse voltage detection	$V_A – V_C$ = +30 mV to – 100 mV to $V_{(DGATE–A)}$ < 1 V, $C_{(DGATE–A)}$ = 10 nF		0.66		µs
$t_{DGATE\_ON(dly)}$	DGATE Turnon Delay during forward voltage detection	$V_A – V_C$ = –20 mV to +700 mV to $V_{(DGATE–A)}$ > 5 V, $C_{(DGATE–A)}$ = 10 nF		2		µs
$t_{EN(dly)\_DGATE}$	DGATE Turnon Delay during EN/UVLO	EN/UVLO ↑ to $V_{(DGATE–A)}$ > 5 V, $C_{(DGATE–A)}$ = 10 nF		185		µs
$t_{EN(deg)\_DGATE}$	Deglitch time	EN/UVLO ↓ to DGATE ↓		5.8		µs
$t_{EN(deg)\_HGATE}$	Deglitch time	EN/UVLO ↓ to HGATE ↓		5.6		µs
$t_{OVP(deg)\_HGATE}$	Deglitch time	OV ↑ to HGATE ↓		3		µs
	Deglitch time	OV ↓ to HGATE ↑		6		µs

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The LM7480x-Q1 ideal diode controller drives and controls external back to back N-Channel MOSFETs to emulate an ideal diode rectifier with power path ON/OFF control, inrush current limiting and over voltage protection. The wide input supply of 3V to 65V allows protection and control of 12-V and 24-V automotive battery powered ECUs. The device can withstand and protect the loads from negative supply voltages down to –65 V. An integrated ideal diode controller (DGATE) drives the first MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. A strong charge pump with 20mA peak GATE source current driver stage and short turn ON and turn OFF delay times ensures fast transient response ensuring robust performance during automotive testing such as ISO16750 or LV124 where an ECU is subjected to AC superimpose input signals. With a second MOSFET in the power path the device allows load disconnect (ON/OFF control) and over voltage protection using HGATE control. The device features an adjustable over voltage cut-off protection feature using a programming resistor across SW and OVP terminal.

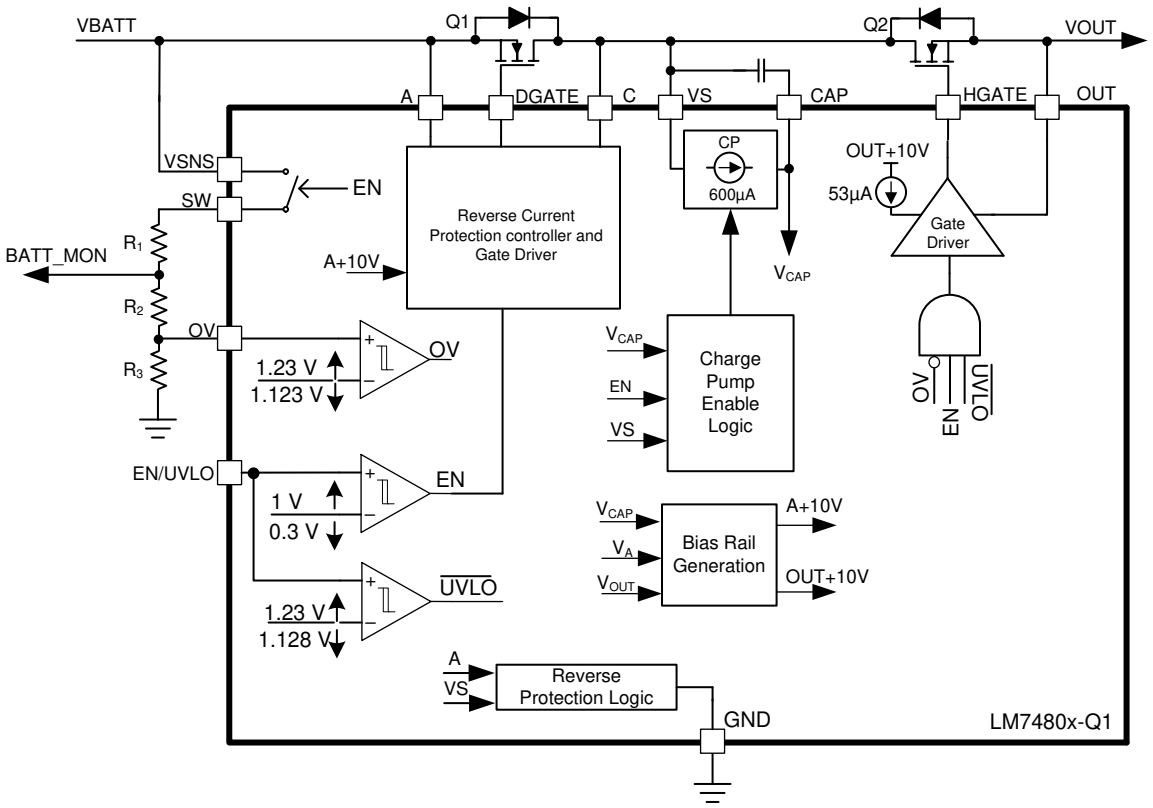
The LM7480x-Q1 controller can drive the external MOSFETs in Common Drain and Common Source configurations. With Common Drain configuration of the power MOSFETs, the mid-point can be utilized for OR-ing designs using an another ideal diode. The LM7480x-Q1 has a maximum voltage rating of 65-V. The loads can be protected from extended over voltage transients like 200-V Unsuppressed Load Dumps in 24-V Battery systems by configuring the device with external MOSFETs in Common Source topology.

The LM74800-Q1 controls the DGATE of the MOSFET to regulate the forward voltage drop at 10.5-mV. The linear regulation scheme in these devices enables graceful control of the GATE voltage and turns off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. The LM74801-Q1 features a comparator based scheme to turn ON/OFF the MOSFET GATE.

The device features enable control. With the enable pin low during the standby mode, both the external MOSFETs and controller is off and draws a very low 3-μA of current. The high voltage rating of LM7480x-Q1 helps to simplify the system designs for automotive ISO7637 protection. The LM74800-Q1 is also suitable for ORing applications

ADVANCE INFORMATION

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Charge Pump (CAP)

The charge pump supplies the voltage necessary to drive the external N-channel MOSFETs. An external charge pump capacitor is placed between CAP and VS pins to provide energy to turn on the external MOSFET. In order for the charge pump to supply current to the external capacitor, the Vs voltage must be above $V_{(VSPOR\_R)}$ threshold and EN/UVLO pin voltage must be above the specified input high threshold, $V_{(EN\_R)}$. The charge pump supply current for LM74800-Q1 and LM74801-Q1 is 600µA. If EN/UVLO pin is pulled low below 0.67V (typ), then the charge pump remains disabled reducing the total Iq current to less than 3µA

8.3.2 Dual Gate control (DGATE, HGATE)

The LM7480x-Q1 feature two separate gate control and driver outputs to drive back to back N-channel MOSFETs.

8.3.2.1 Reverse Battery Protection (A, C, DGATE)

A, C, DGATE comprises of Ideal Diode stage. Connect the Source of the external MOSFET to A, Drain to C and Gate to DGATE. The LM7480x-Q1 has integrated reverse input protection down to –65V.

ADVANCE INFORMATION

Feature Description (continued)

In LM74800-Q1 the voltage drop across the MOSFET is continuously monitored between the A and C pins, and the DGATE to A voltage is adjusted as needed to regulate the forward voltage drop at 10.5 mV (typ). This closed loop regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. This scheme ensures robust performance during slow input voltage ramp down tests. Along with the linear regulation amplifier scheme, the LM74800-Q1 also integrates a fast reverse voltage comparator. When the voltage drop across A and C reaches $V_{AC(REV)}$ threshold then the DGATE goes low within 0.6-µs (typ). This fast reverse voltage comparator scheme ensures robust performance during fast input voltage ramp down tests such as input micro-shorts. The external MOSFET is turned ON back when the voltage across A and C hits $V_{AC(FWD)}$ threshold within 2-µs (typ).

In LM74801-Q1, reverse current blocking is by fast reverse voltage comparator only. When the voltage drop across A and C reaches $V_{AC(REV)}$ threshold then the DGATE goes low within 0.6-µs (typ). This fast reverse voltage comparator scheme ensures robust performance during fast input voltage ramp down tests such as input micro-shorts. The external MOSFET is turned ON back when the voltage across A and C hits $V_{AC(FWD)}$ threshold within 2-µs (typ).

For Ideal Diode only designs, connect LM7480x-Q1 as shown in Figure 1

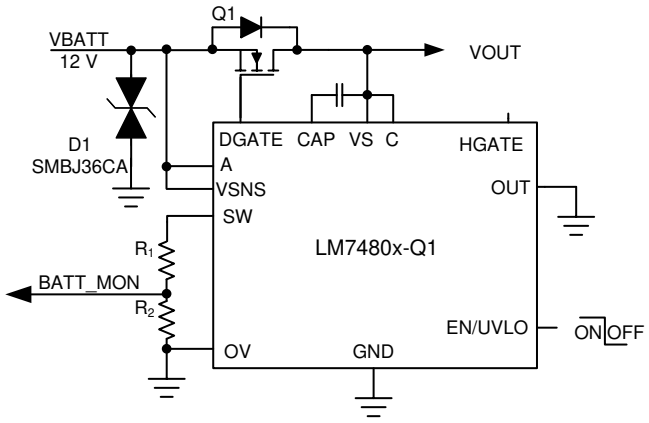


Figure 1. Configuring LM7480x-Q1 for Ideal Diode Only

8.3.3 Load disconnect switch control (HGATE, OUT)

HGATE and OUT comprises of Load disconnect switch control stage. Connect the Source of the external MOSFET to OUT and Gate to HGATE. Connect C_{dVdT} capacitor and R_1 as shown in Figure 2.

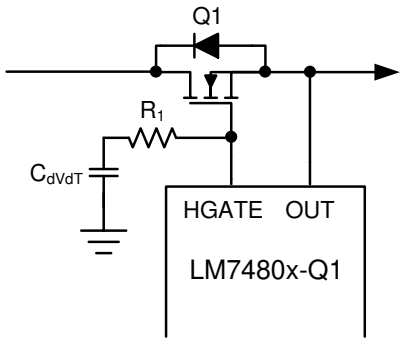


Figure 2. Inrush Current Limiting

The C_{dVdT} capacitor is required for slowing down the HGATE voltage ramp during power up for inrush current limiting. Use Equation 1 to calculate C_{dVdT} capacitance value .

ADVANCE INFORMATION

Feature Description (continued)

$$C_{dVdT} = \frac{I_{HGATE\_DRV}}{I_{INRUSH}} xC_{OUT} \quad (1)$$

where I_{HATE_DRV} is 53-µA (typ), I_{INRUSH} is the inrush current and C_{OUT} is the output load capacitance. An extra resistor, R_1, in series with the C_{dVdT} capacitor improves the turn off time.

8.3.4 Over Voltage Protection and Battery Voltage sensing (VSNS, SW, OV)

Connect a resistor ladder as shown in Figure 3 for Over voltage threshold programming.

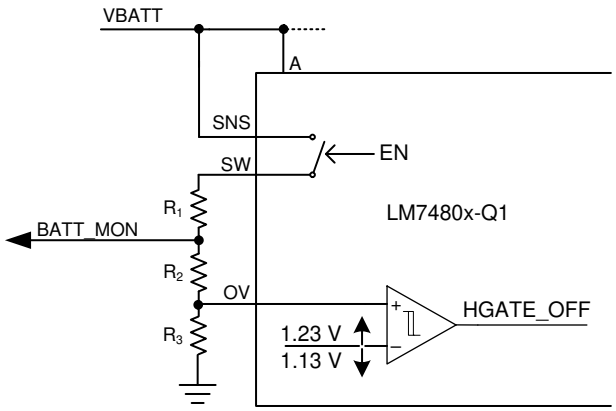


Figure 3. Programming Over Voltage Threshold and Battery Sensing

A disconnect switch is integrated between VSNS and SW pins. This switch is turned OFF when EN/UVLO pin is pulled low. This helps to reduce the leakage current through the resistor divider network during system shutdown state (IGN_OFF state).

8.3.5 Low Iq shutdown and Under Voltage Lockout (EN/UVLO)

The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN/UVLO pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in Charge Pump section. If EN/UVLO pin voltage is less than the input low threshold < 0.6V, the charge pump and both the gate drivers (DGATE and HGATE) are disabled placing the LM7480x-Q1 in shutdown mode. If EN/UVLO is at 1.13V<$V_{EN/UVLO}$<0.6V then only HGATE is disabled disconnecting the load from the supply, DGATE remains ON. The EN/UVLO pin can withstand a maximum voltage of 65V. For always ON operation connect EN/UVLO pin to A.

ADVANCE INFORMATION

8.4 Application Examples

8.4.1 Redundant Supply OR-ing with Inrush Current Limiting, Over-Voltage Protection and ON/OFF control

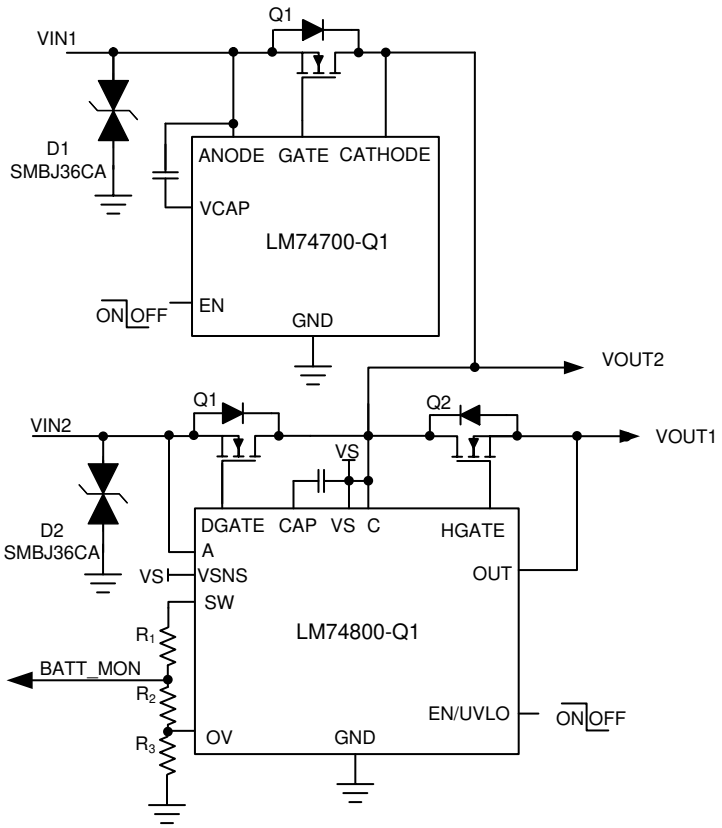


Figure 4. Redundant Supply OR-ing with Over Voltage Protection and ON/OFF control

Figure 4 shows the implementation of Dual OR-ing with Inrush Current Limiting, Over Voltage Protection and power path ON/OFF control. The input side SMBJ36CA TVS across the ideal diodes is required for ISO7637 Pulse 1 transient suppression to limit the input voltage within the device max voltage rating of -65V.

R1 and R2 are the programming resistors for over voltage protection (OVP) threshold. When the voltage at OVP pin exceeds OVP cut-off reference threshold then the HGATE driver turns OFF the FET Q3, disconnecting the power path and protecting the downstream load. HGATE goes high once the OVP pin voltage goes below the OVP falling hysteresis threshold. Use 0.1µF to 1µF capacitor across VS to CAP pins of the LM7480x-Q1. This is the charge pump capacitor and acts as the supply for both the DGATE and HGATE driver stages. The DGATE driver of the LM7480x-Q1 is equipped with 20-mA peak source current and 1.5A peak sink current capability resulting in fast and efficient transient responses during the ISO16750 or LV124 short interruptions as well as AC superimpose testing.

Pull EN low during the sleep/standby mode. With EN low, both the DGATE and HGATE drivers are pulled low turning OFF both the power FETs. VOUT1 gets disconnected from the VBATT rail reducing the system I_Q. VOUT2 is gets power through the body diode of the MOSFET Q2 and this supply can be utilized for always ON loads. The LM7480x-Q1 draws a 3µA current during this mode.

ADVANCE INFORMATION

Application Examples (continued)

8.4.2 Ideal Diode with Unsuppressed Load dump Protection

An extended over voltage protection support above 65V can be achieved by configuring the device with external back to back MOSFETs in common source topology as shown in Figure 5. Place a resistor R1 and a zener clamp across VS pin to GND to limit the voltage below 65V. The load gets protected from over voltages transients like un-suppressed load dumps with the help of over voltage protection feature. Use R2 and R3 for setting the over voltage protection threshold. When voltage at OV pin exceeds the set OV threshold then the HGATE turns OFF. This results in power path disconnection between input and output.

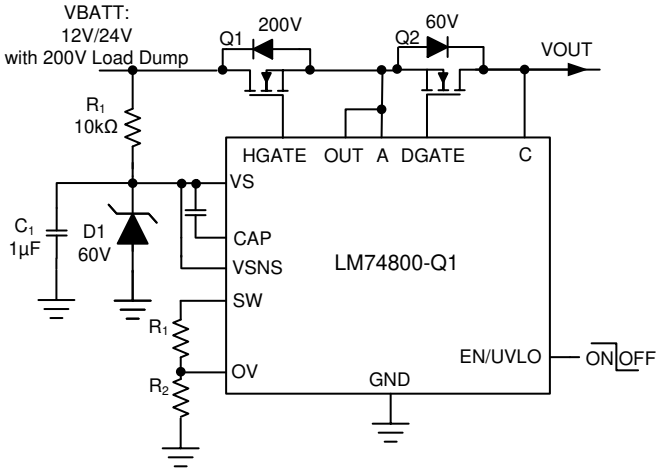


Figure 5. Ideal Diode with 200V Un-supressed Load dump protection

ADVANCE INFORMATION

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

LM74800-Q1 controls two N-channel power MOSFETs with DGATE used to control diode MOSFET to emulate an ideal diode and HGATE controlling second MOSFET for power path cut-off when disabled or during an over voltage protection. HGATE controlled MOSFET can be used to clamp the output during over voltage or load dump conditions. LM74800-Q1 can be placed into low quiescent current mode using EN/UVLO, where both DGATE and HGATE are turned OFF.

The device has a separate supply input pin (Vs). The charge pump is derived from this supply input. With the separate supply input provision and separate GATE control architecture, the LM74800-Q1 device offers flexibility in system design architectures and enables circuit design with various power path control topologies like common drain, common source, ORing and Power MUXing. With these various topologies, the system designers can design the front-end power system to meet various system design requirements. For more information, see the *Six System Architectures With Robust Reverse Battery Protection Using an Ideal Diode Controller* Application Report.

9.2 Typical 12V Reverse Battery Protection Application

A typical application circuit of LM74800-Q1 configured in **common-drain topology** to provide reverse battery protection with over voltage protection is shown in Figure 6.

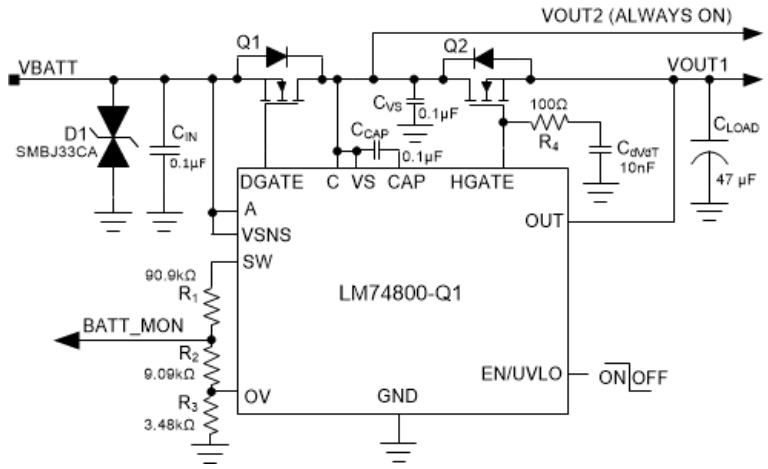


Figure 6. Typical Application Circuit - 12V Reverse Battery Protection and Over Voltage Protection

9.2.1 Design Requirements for 12V Battery Protection

The system design requirements are listed in .

Table 2. Design Parameters - 12V reverse battery protection and over voltage protection

DESIGN PARAMETER	EXAMPLE VALUE
Operating Input Voltage Range	12V battery, 12V nominal with 3.2V Cold Crank and 35V Load Dump
Output Power	50 W
Output Current Range	4A Nominal, 5A maximum
Input Capacitance	0.1µF minimum

ADVANCE INFORMATION

Typical 12V Reverse Battery Protection Application (continued)

Table 2. Design Parameters - 12V reverse battery protection and over voltage protection (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Output Capacitance	0.1µF minimum, (optional 220µF for E-10 functional class A performance)
Over Voltage Cut-off	37.0V, output cut-off >37.0V
AC Super Imposed Test	2V Peak-Peak 30KHz, extendable to 6V Peak-Peak 30KHz
Automotive Transient Immunity Compliance	ISO 7637-2, ISO 16750-2 and LV124
Battery Monitor Ratio	8:1

9.2.2 Automotive Reverse Battery Protection

LM74800-Q1 gate drive output DGATE controls MOSFET Q1 to provide reverse battery protection and true reverse current blocking functionality. This enables LM74800-Q1 to provide comprehensive immunity to various automotive transient tests on 12V battery or 24V battery as per ISO 7637-2 and ISO 16750-2 standard as well as other automotive OEM standards. HGATE controls MOSFET Q2 to turn off the power path during input over voltage condition. Resistor network R1, R2 and R3 connected to OV and SW can be configured for over voltage protection and also for battery monitoring under normal operating conditions as well as reverse battery conditions. Bi-directional TVS D1 clamps the automotive transient input voltages on the 12V battery, both positive and negative transients, to voltage levels safe for MOSFET Q1 and LM74800-Q1.

Fast reverse current blocking response and quick reverse recovery enables LM74800-Q1 to turn ON/OFF MOSFET Q1 during AC super imposed input specified by ISO 16750-2 and LV124 E-06 and provide active rectification of the AC input superimposed on DC battery voltage. Fast reverse current blocking response of LM74800-Q1 helps to turn off MOSFET Q1 during negative transients inputs such as -150V 2ms Pulse 1 specified in ISO 7637-2 and input micro short conditions such as LV124 E-10 test.

9.2.2.1 Input Transient Protection: ISO 7637-2 Pulse 1

ISO 7637-2 Pulse 1 specifies negative transient immunity of electronic modules connected in parallel with an inductive load when the battery is disconnected. A typical pulse 1 specified in ISO 7637-2 starts with battery disconnection where supply voltage collapses to 0 V followed by -150V 2ms applied with a source impedance of 10Ω at a slew rate of 1µs on the supply input. LM74800-Q1 blocks reverse current and prevents the output voltage from swinging negative, protecting the rest of the electronic circuits from damage due to negative transient voltage. MOSFET Q1 is quickly turned off within 0.5µs by fast reverse comparator of LM74800-Q1. A single bi-directional TVS is required at the input to clamp the negative transient pulse within the operating maximum voltage across cathode to anode of 85V and does not violate the MOSFET Q1 drain-source breakdown voltage rating.

ISO 7637-2 Pulse 1 performance of LM74800-Q1 is shown in Figure 7.

ADVANCE INFORMATION

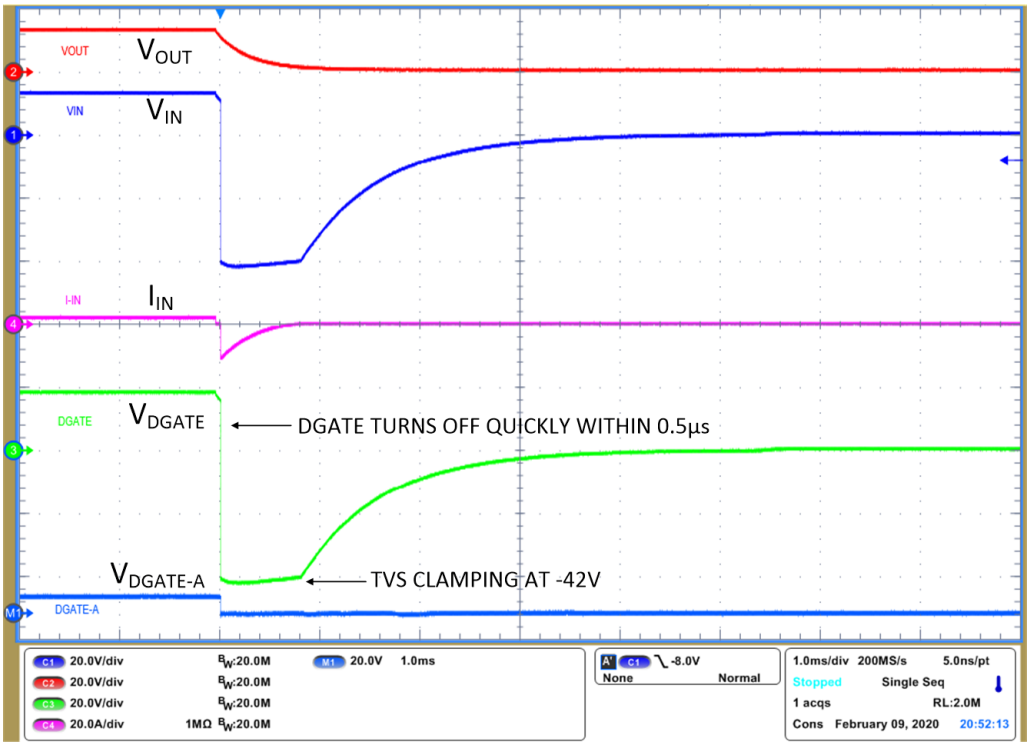


Figure 7. ISO 7637-2 Pulse 1

9.2.2.2 AC Super Imposed Input Rectification: ISO 16750-2 and LV124 E-06

Alternators are used to power the automotive electrical system and charge the battery during normal runtime of the vehicle. Rectified alternator output contains residual AC ripple voltage superimposed on the DC battery voltage due to various reasons which includes engine speed variation, regulator duty cycle with field switching ON/OFF and electrical load variations. On a 12V battery supply, alternator output voltage is regulated by a voltage regulator between 14.5 V to 12.5V by controlling the field current of alternator's rotor. All electronic modules are tested for proper operation with superimposed AC ripple on the DC battery voltage. AC super imposed test specified in ISO 16750-2 and LV124 E-06 requires AC ripple of 2V Peak-Peak on a 13.5 V DC battery voltage, swept from 15Hz to 30KHz. LM74800-Q1 rectifies the AC superimposed voltage by turning the MOSFET Q1 OFF quickly to cut-off reverse current and turning the MOSFET Q1 ON quickly during forward conduction. Active rectification of 2V peak-peak 5KHz AC input by LM74800-Q1 is shown in Figure 8. Fast turn off and quick turn ON of the MOSFET reduces power dissipation in the MOSFET Q1 and active rectification reduces power dissipation in the output hold-up capacitor's ESR by half. Active rectification of 2V peak-peak 30KHz AC input is shown in Figure 9.

ADVANCE INFORMATION

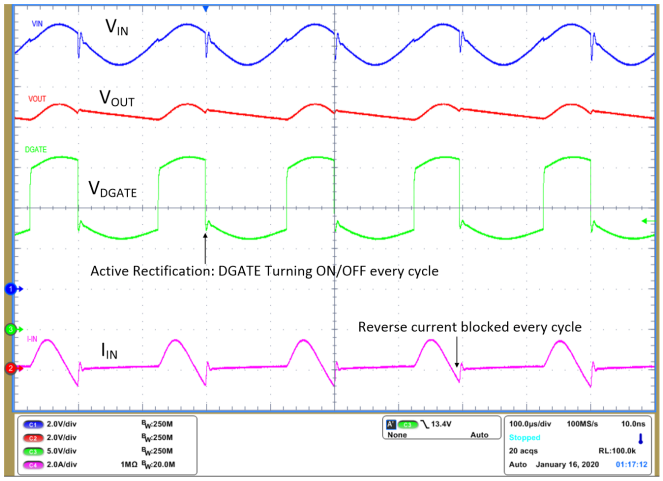


Figure 8. AC Super Imposed Test - 2V Peak-Peak 5KHz

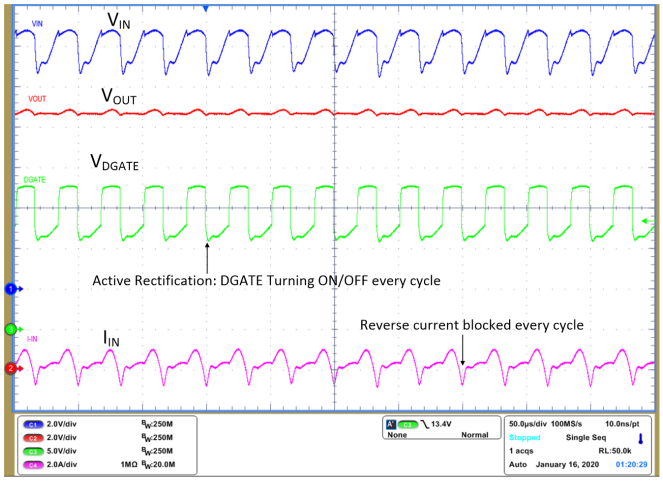


Figure 9. AC Super Imposed Test - 2V Peak-Peak 30KHz

9.2.2.3 Input Micro-Short Protection: LV124 E-10

E-10 test specified in LV124 standard checks for immunity of electronic modules to short interruptions in power supply input due to contact issues or relay bounce. During this test (case 2), micro-short is applied on the input for a duration as low as 10µs to several ms. For a functional pass status A, electronic modules are required to run uninterrupted during the E-10 test (case 2) with 100µs duration. Dual-Gate drive architecture of LM74800-Q1 - DGATE and HGATE - enables to achieve a functional pass status A with optimum hold up capacitance on the output when compared to a single gate drive controller. When input micro-short is applied for 100µs, LM74800-Q1 quickly turns off MOSFET Q1 by shorting DGATE to ANODE (source of MOSFET) within 0.5µs to prevent the output from discharging and the HGATE remains ON keeping MOSFET Q2 ON, enabling fast recovery after the input short is removed.

Performance of LM74800-Q1 during E10 input power supply interruption test case 2 is shown in Figure 10. After the input short is removed, input voltage recovers and MOSFET Q1 is turned back ON within 130µs. Note that dual-gate drive topology allows MOSFET Q2 to remain ON during the test and helps in restoring the input power faster. Output voltage remains unperturbed during the entire duration, achieving functional status A.

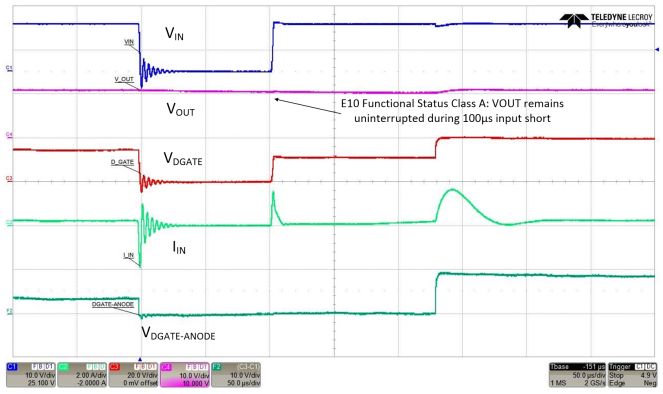


Figure 10. Input Micro-Short - LV124 E10 TC 2 100µs

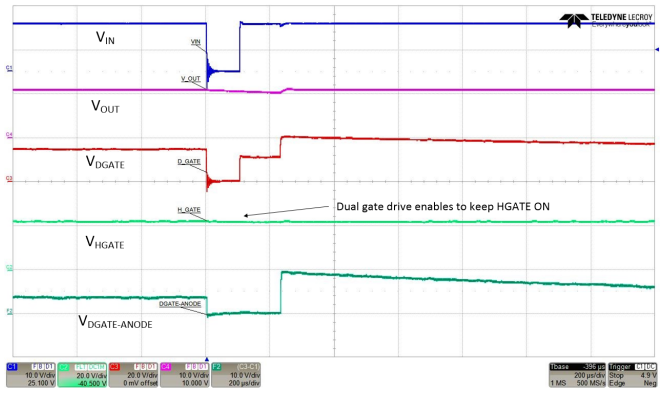


Figure 11. Input Micro-Short - LV124 E10 TC 2 100µs with HGATE

ADVANCE INFORMATION

9.2.3 Detailed Design Procedure

9.2.3.1 Design Considerations

Table 2 summarizes the design parameters that must be known for designing an automotive reverse battery protection circuit with over voltage cut-off. During power up, inrush current through MOSFET Q2 needs to be limited so that the MOSFET operates well within its SOA. Maximum load current, maximum ambient temperature and thermal properties of the PCB determine the R_{DSON} of the MOSFET Q2 and maximum operating voltage determines the voltage rating of the MOSFET Q2. Selection of MOSFET Q2 is determined mainly by the maximum operating load current, maximum ambient temperature, maximum frequency of AC super imposed voltage ripple and ISO 7637-2 pulse 1 requirements. Over voltage threshold is decided based on the rating of downstream DC/DC converter or other components after the reverse battery protection circuit. A single bi-directional TVS or two back-back uni-directional TVS are required to clamp input transients to a safe operating level for the MOSFETs Q1, Q2 and LM74800-Q1.

9.2.3.2 Charge Pump Capacitance VCAP

Minimum required capacitance for charge pump VCAP is based on input capacitance of the MOSFET Q1, $C_{ISS(MOSFET_Q1)}$and input capactiance of Q2 $C_{ISS(MOSFET)}$.

Charge Pump VCAP: Minimum 0.1 µF is required; recommended value of VCAP (µF) ≥ 10 x ($C_{ISS(MOSFET\_Q1)}$ + $C_{ISS(MOSFET\_Q2)}$) (µF)

9.2.3.3 Input and Output Capacitance

A minimum input capacitance C_{IN} of 0.1 µF and output capacitance C_{OUT} of 0.1 µF is recommended.

9.2.3.4 Hold-up Capacitance

Usually bulk capacitors are placed on the output due to various reasons such as uninterrupted operation during power interruption or micro-short at the input, hold-up requirements for doing a memory dump before turning of the module and filtering requirements as well. This design considers minimum bulk capacitors requirements for meeting functional status "A" during LV124 E10 test case 2 100 µs input interruption. To achieve functional pass status A, acceptable voltage droop in the output of LM74800-Q1 is based on the UVLO settings of downstream DC-DC converters. For this design, 2.5V drop in output voltage for 100 µs is considered and the minimum hold-up capacitance required is calculated by

$$C_{HOLD\_UP\_MIN} = \frac{I_{LOAD\_MAX}}{dV_{OUT}} x 100\mu s \tag{2}$$

Minimum hold-up capacitance required for 2.5V drop in 100 µs is 200 µF. Note that the typical application circuit shows the hold-up capacitor as optional because not all designs require hold-up capacitance.

9.2.3.5 Over Voltage Protection and Battery Monitor

Resistors R_1, R_2 and R_3 connected in series are used to program the over voltage threshold and battery monitor ratio. The resistor values required for setting the over voltage threshold V_{OV} to 37.0 V and battery monitor ratio V_{BATT_MON} : V_{BATT} to 1:8 are calculated by solving Equation 3 and Equation 3.

$$V_{OVR} = \frac{R_3}{R_1 + R_2 + R_3} x V_{OV} \tag{3}$$

$$V_{BAT\_MON} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} x V_{BATT} \tag{4}$$

For minimizing the input current drawn from the battery through resistors R_1, R_2 and R_3, it recommended to use higher value of resistance. Using high value resistors will add error in the calculations because the current through the resistors at higher value will become comparable to the leakage current into the OV pin. Maximum leakage current into the OV pin is 1 µA and choosing (R_1 + R_2 + R_3) < 120 kΩ ensures current through resistors is 100 times greater than leakage through OV pin.

ADVANCE INFORMATION

Based on the device electrical characteristics, V_{OVR} is 1.233V V and battery monitor ratio (V_{BATT_MON} / V_{BATT}) is designed for a ratio of 1/8. To limit (R_1 + R_2 + R_3) < 120 kΩ, select (R_1 + R_2) = 100 kΩ. Solving Equation 3 gives R_3 = 3.45 kΩ. Solving Equation 4 for R2 using (R_1 + R_2) = 100 kΩ and R_3 = 3.45 kΩ, gives R_2 = 9.48 kΩ and R_1 = 90.52 kΩ.

Standard 1% resistor values closest to the calculated resistor values are R1 = 90.9kΩ, R2 = 9.09kΩ and R3 = 3.48kΩ.

9.2.4 MOSFET Selection: Blocking MOSFET Q1

For selecting the blocking MOSFET Q1, important electrical parameters are the maximum continuous drain current I_D, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, the maximum source current through body diode and the drain-to-source ON resistance R_{DSON}.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include all the automotive transient events and any anticipated fault conditions. It is recommended to use MOSFETs with V_{DS} voltage rating of 60-V along with a single bidirectional TVS or a V_{DS} rating 40-V maximum rating along with two unidirectional TVS connected back-back at the input.

The maximum V_{GS} LM74800-Q1 can drive is 14 V, so a MOSFET with 15-V minimum V_{GS} rating should be selected. If a MOSFET with <15-V V_{GS} rating is selected, a zener diode can be used to clamp V_{GS} to safe level, but this would result in increased I_Q current.

During startup, inrush current flows through the body diode to charge the bulk hold-up capacitors at the output. The maximum source current through the body diode must be higher than the inrush current.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ may not be beneficial always. Higher $R_{DS(ON)}$ will provide increased voltage information to LM74800-Q1's reverse comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. It is recommended to operate the MOSFET in regulated conduction mode during nominal load conditions and select $R_{DS(ON)}$ such that at nominal operating current, forward voltage drop V_{DS} is close to 8-mV regulation point and not more than 50 mV. As a guideline, it is suggested to choose (8 mV / $I_{Load(Nominal)}$) ≤ $R_{DS(ON)}$ ≤ (50 mV / $I_{Load(Nominal)}$).

For active rectification of AC super imposed ripple on the battery supply voltage, gate-source charge Q_{GS} of Q1 must be selected to meet the required AC ripple frequency. Maximum gate-source charge Q_{GS} (at 4.5V V_{GS}) for active rectification every cycle is

$$Q_{GS\_MAX} = \frac{600\mu A}{F_{AC\_RIPPLE}} \quad (5)$$

where 600 µA is minimum charge pump current at 7V V_{DGATE}-V_A, F_{AC_RIPPLE} is frequency of the AC ripple superimposed on the battery and Q_{GS_MAX} is the Q_{GS} value specified in manufacturer datasheet at 6V V_{GS}. For active rectification at F_{AC_RIPPLE} = 30KHz, Q_{GS_MAX} = 20nC.

Based on the design requirements, preferred MOSFET ratings are:

- 60-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ at 4-A nominal current: (8 mV / 4A) ≤ $R_{DS(ON)}$ ≤ (50 mV / 4A) = 2.0 mΩ ≤ $R_{DS(ON)}$ ≤ 12.5 mΩ.

BUK7Y4R8-60E MOSFET is selected to meet the 12-V reverse battery protection design requirements and its ratings are:

- 60-V $V_{DS(MAX)}$ and ±20-V $V_{GS(MAX)}$
- $R_{DS(ON)}$ 5.0-mΩ typical at 5-V V_{GS} and 2.9-mΩ rated at 10-V V_{GS}
- MOSFET Q_{GS} 17.4 nC

Thermal resistance of the MOSFET should be considered against the expected maximum power dissipation in the MOSFET to ensure that the junction temperature (T_J) is well controlled.

ADVANCE INFORMATION

9.2.5 MOSFET Selection: Hot-Swap MOSFET Q2

The V_{DS} rating of the MOSFET Q2 should be sufficient to handle the maximum system voltage along with the input transient voltage. For this 12V design, transient over voltage events are during suppressed load dump 35 V 400 ms and ISO 7637-2 pulse 2A 50V for 50 µs. Further, ISO 7637-2 Pulse 3B is a very fast repetitive pulse of 100 V 100 ns that is usually absorbed by the input and output ceramic capacitors and the maximum voltage on the 12 V battery can be limited to < 40V the minimum recommended input capacitance of 0.1 µF. The 50 V SO 7637-2 Pulse 2A can also be absorbed by input and output capacitors and its amplitude could be reduced to 40V peak by placing sufficient amount of capacitance at input and output. However for this 12V design, maximum system voltage is 50V and a 60V V_{DS} rated MOSFET is selected.

The VGS rating of the MOSFET Q2 should be higher than that maximum HGATE-OUT voltage 15V.

Inrush current through the MOSFET during input hot-plug into the 12V battery is determined by output capacitance. External capacitor on HGATE, C_{DVDT} is used to limit the inrush current during input hot-plug or startup. The value of inrush current determined by Equation 1 need to be selected to ensure that the MOSFET Q2 is operating well within its safe operating area (SOA). To limit inrush current to 250mA, value of C_{DVDT} is 10.43 nF, closest standard value of 10.0 nF is chosen.

Duration of inrush current is calculated by

$$dT_{INRUSH} = \frac{12}{I_{INRUSH}} xC_{OUT} \tag{6}$$

Calculated inrush current duration is 2.36 ms with 250 mA inrush current.

MOSFET BUK7Y4R8-60E having 60 V V_{DS} and ±20 V V_{GS} rating is selected for Q2. Power dissipation during inrush is well within the MOSFET's safe operating area (SOA).

9.2.6 TVS Selection

A 600W SMBJ TVS such as SMBJ33CA is recommended for input transient clamping and protection. For detailed explanation on TVS selection for 12V battery systems, refer to TVS selection for 12V Battery Systems.

9.2.7 Application Curves

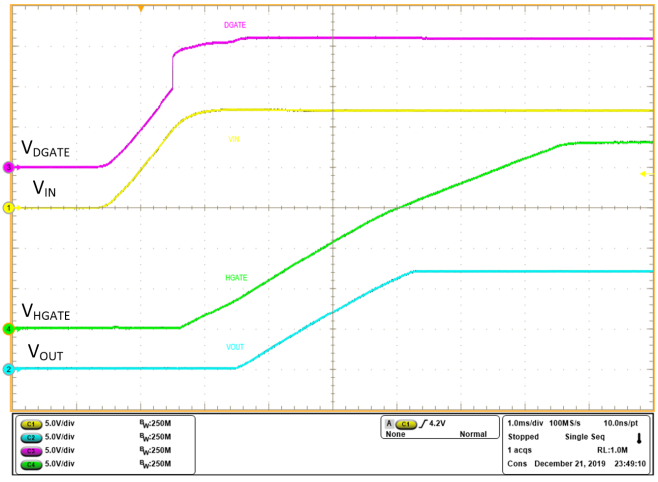


Figure 12. Startup 12V with EN Pulled to VIN

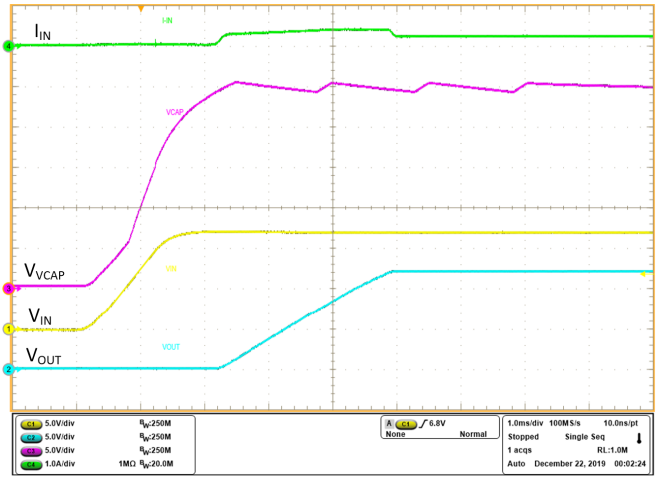


Figure 13. Startup 12V showing Charge Pump VCAP

ADVANCE INFORMATION

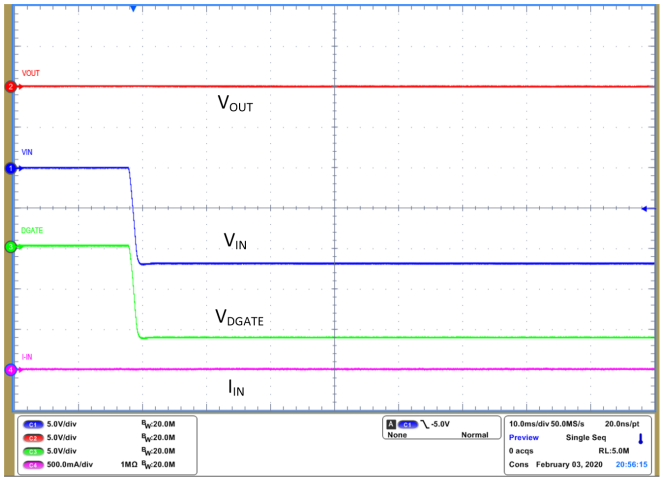


Figure 14. Reverse Input Voltage -14 V

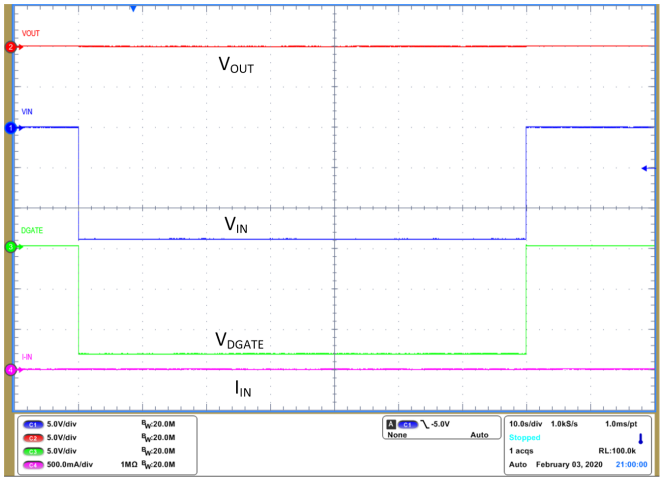


Figure 15. Reverse Input Voltage -14 V for 60 s

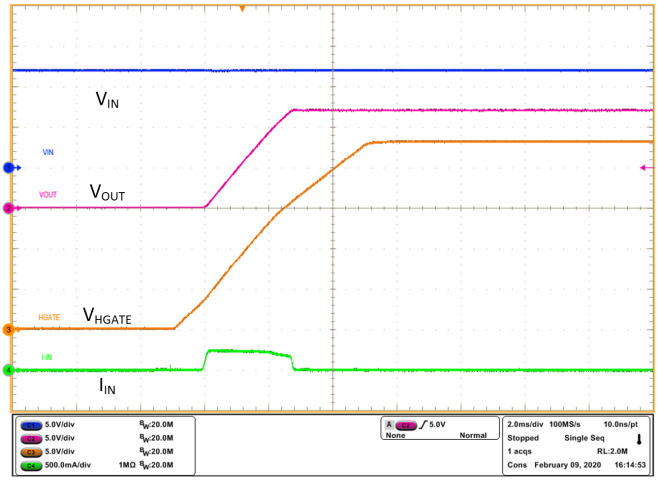


Figure 16. Inrush Current with no load at output

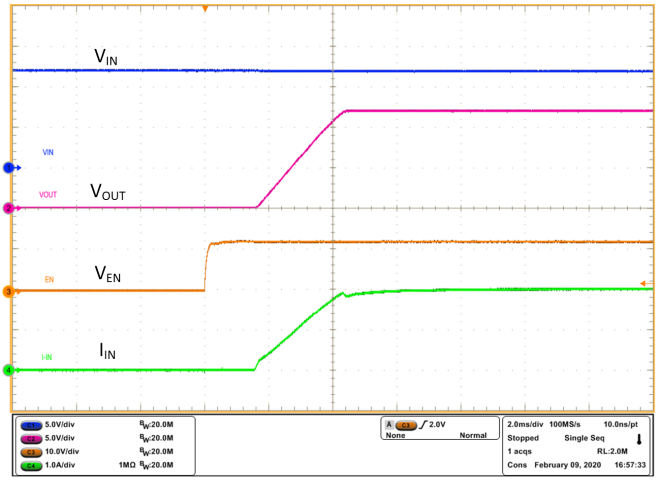


Figure 17. Inrush current with 6Ω load

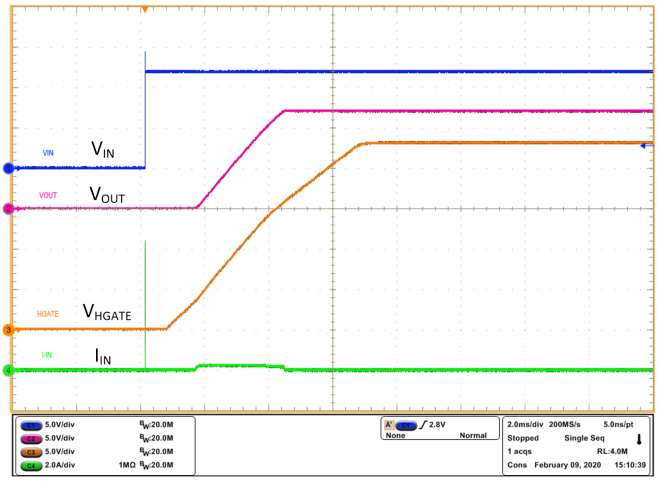


Figure 18. Hot-Plug into 12V

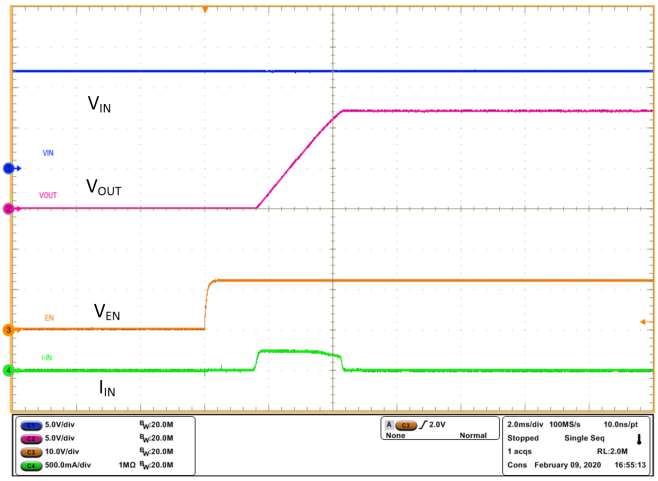


Figure 19. Output Turn ON with Enable

ADVANCE INFORMATION

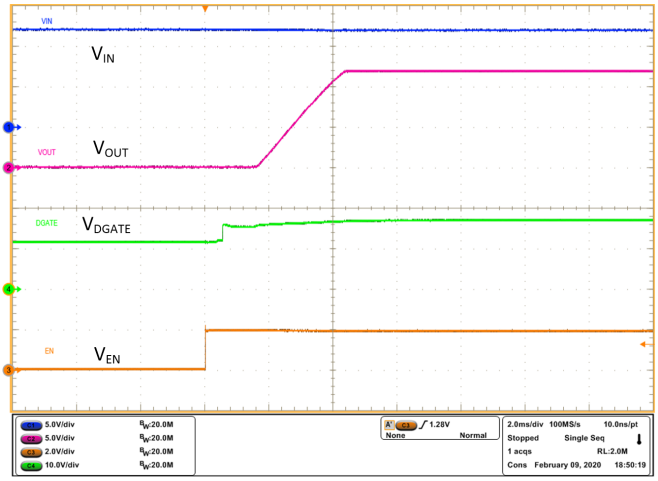


Figure 20. DGATE Turn ON with Enable

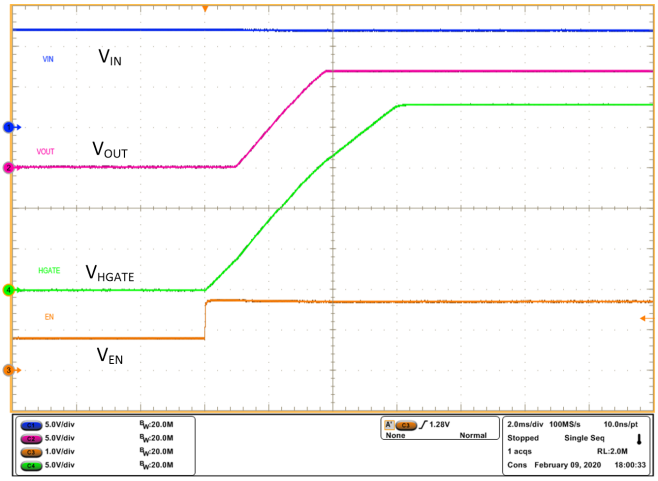


Figure 21. Turn ON with VCAP ON - EN rising from 0.8V

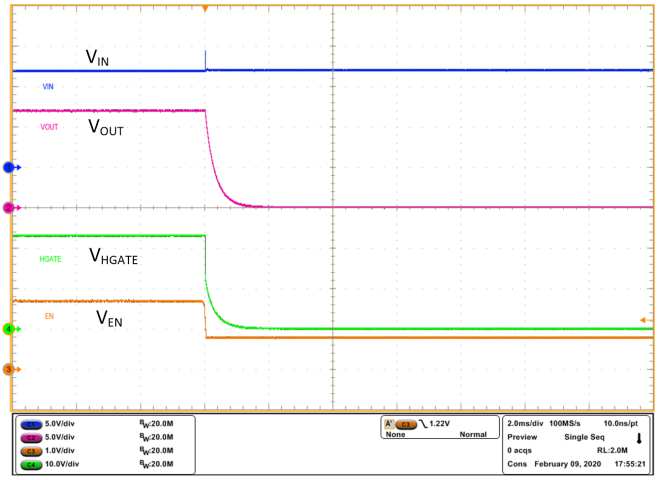


Figure 22. Turn OFF with Enable Control

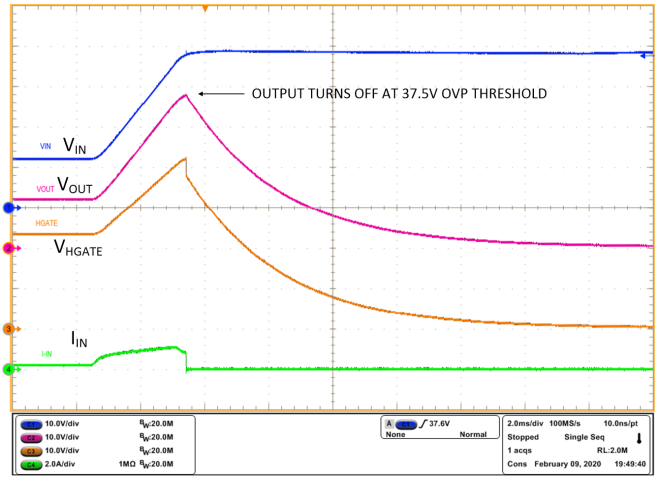


Figure 23. Over Voltage Protection

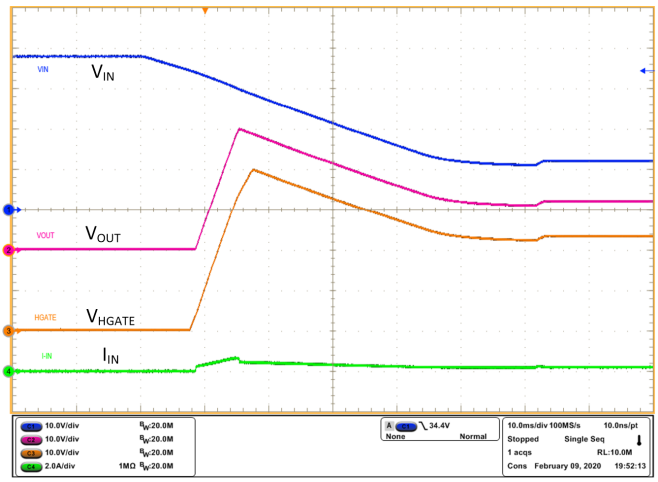


Figure 24. Over Voltage Recovery

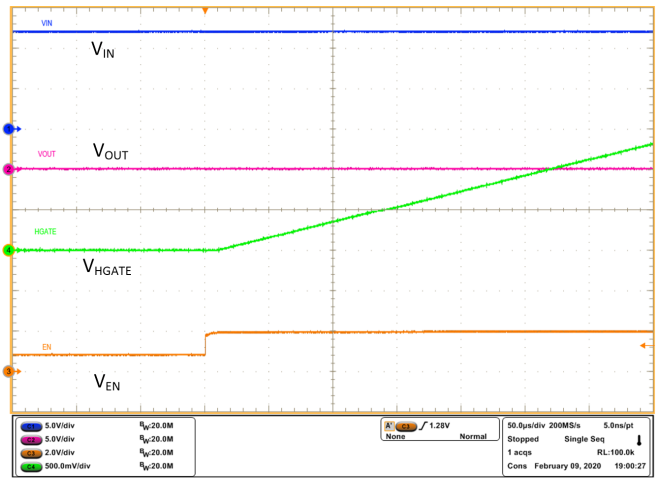


Figure 25. Turn ON delay - HGATE

ADVANCE INFORMATION

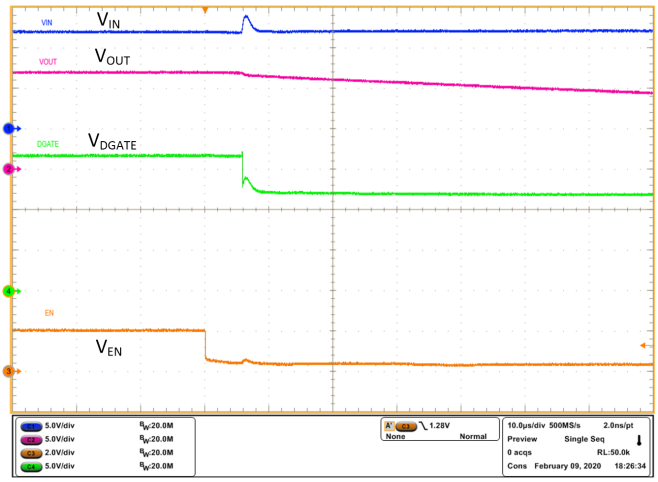


Figure 26. Turn OFF delay - DGATE

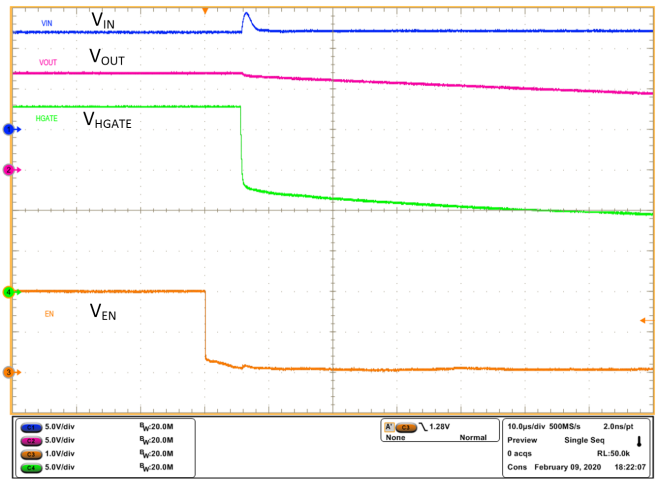


Figure 27. Turn OFF delay - HGATE

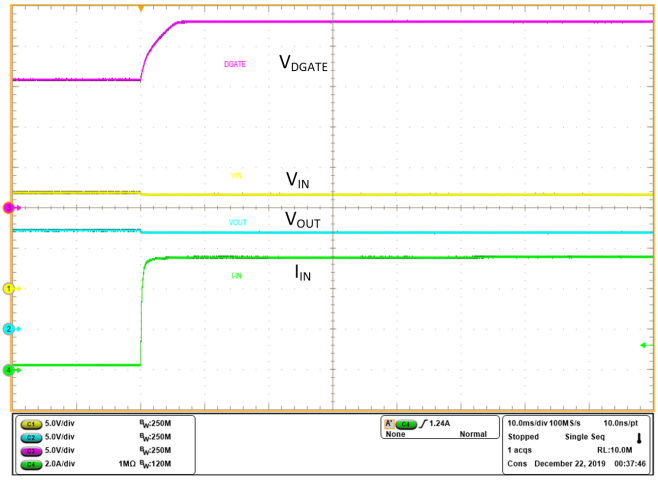


Figure 28. Load Transient 100mA to 5A

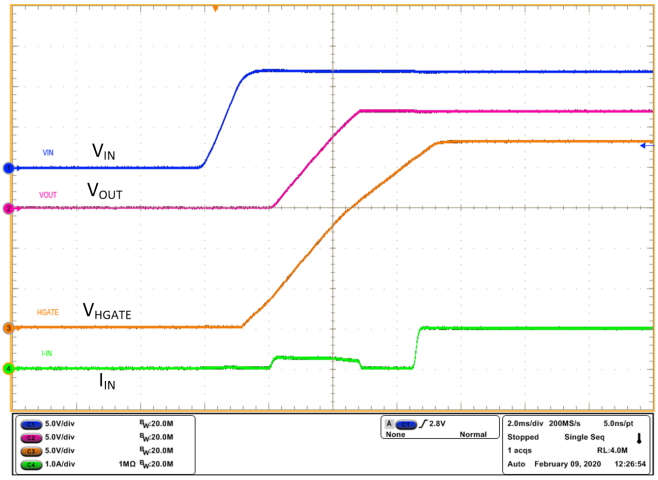


Figure 29. Startup 1A Load 1ms after output powers up

ADVANCE INFORMATION

9.3 200V Unsuppressed Load Dump Protection Application

Independent gate drive topology of LM74800-Q1 enables to configure the LM74800-Q1 in to provide unsuppressed load dump or surge protection along with reverse battery protection. LM74800-Q1 configured in **common-source topology** to provide 200V unsuppressed load dump protection with reverse battery protection is Figure 30.

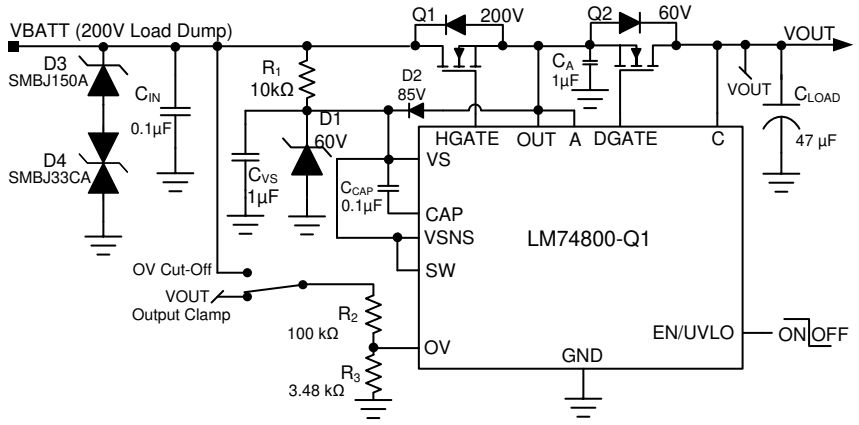


Figure 30. Typical Application Circuit - 200V unsuppressed load dump protection with reverse battery protection

9.3.1 Design Requirements for 200V Unsuppressed Load Dump Protection

Table 3. Design Parameters - 24V unsuppressed load dump protection

DESIGN PARAMETER	EXAMPLE VALUE
Operating Input Voltage Range	24V battery, 6V during cold crank 200V Unsuppressed Load Dump
Output Voltage	6V during Cold Crank and 37.0V during Load Dump
Output Power	25 W
Output Current Range	2A Nominal, 2.5A Peak
Input Capacitance	0.1µF minimum
Output Capacitance	0.1µF minimum, 220µF typical hold-up capacitance
Over Voltage Cut-Off Threshold	37.0V
Over Voltage Clamp	Output clamped between 34.5V and 37.5V
Automotive Transient Immunity Compliance	ISO 7637-2 and ISO 16750-2 including 200V unsuppressed load dump Pulse 5A and -600V 50Ω ISO-7637 Pulse 1

9.3.2 Design Procedure

Load dump transients occurs on loads connected to the alternator when a discharged battery is disconnected from alternator while it is still generating charging current. Load dump amplitude and duration depends on alternator speed and field current into the rotor. The pulse shape and parameter are specified in ISO 7637-2 5A where a 200V pulse lasts maximum 350 ms on 24V battery system. Circuit topology and MOSFET ratings are important when designing a 200V unsuppressed load dump protection circuit using LM74800-Q1. Dual gate drive enables LM74800-Q1 to be configured in common source topology in Figure 30 where MOSFET Q1 is used to turn off or clamp output voltage to acceptable safe level and protect the MOSFET Q2 and LM74800-Q1 from 200V. Note that only the V_S pin is exposed to 200V through a 10 kΩ resistor. A 60V rated zener diode is used to clamp and protect the V_S pin. Rest of the circuit is not exposed to higher voltage as the MOSFET Q1 can either be turned off completely or output voltage clamped to safe level. MOSFET Q1 selection, input TVS selection and MOSFET Q2 selection for ISO 7637-2 and ISO 16750-2 compliance are discussed in this section.

ADVANCE INFORMATION

9.3.2.1 Charge Pump Capacitance VCAP

Minimum required capacitance for charge pump VCAP is based on input capacitance of the MOSFET Q1, $C_{ISS(MOSFET_Q1)}$and input capactiance of Q2 $C_{ISS(MOSFET\_Q2)}$.

Charge Pump VCAP: Minimum 0.1 µF is required; recommended value of VCAP (µF) ≥ 10 x ($C_{ISS(MOSFET\_Q1)}$ + $C_{ISS(MOSFET\_Q2)}$) (µF)

9.3.2.2 Input and output capacitance

A minimum input capacitance C_{IN} of 0.1 µF and output capacitance C_{OUT} of 0.1 µF is recommended.

9.3.2.3 V_S Capacitance, Resistor and Zener Clamp

Minimum of 1 µF C_{VS} capacitance is required. During 200V load dump, resistor R_1 and zener diode D_1 are used to protect VS pin from exceeding the maximum ratings by clamping V_{VS} to 60V. Choosing R_1 = 10 kΩ, the peak power dissipated in zener diode D1 = 60V * (200V-60V)/10kΩ = 0.840W of peak power dissipation. SMA package diode such as BZG03B62-M can handle 840mW peak power dissipation. Peak power dissipated in R1 = $(200V-60V)^2$ / 10kΩ = 1.96W. One 10kΩ resistor in 1210 package with 0.5W DC power rating and 200V rating can withstand 200 Load Dump for 350 ms.

9.3.2.4 Over Voltage Protection and Output Clamp

Resistors R_2 and R_3 connected in series is used to program the over voltage threshold. Connecting R2 to VBATT provides over voltage cut-off and switching the connection to VOUT provides over voltage clamp. The resistor values required for setting the over voltage threshold V_{OV} to 37.0 V is calculated by solving Equation 7.

$$V_{OVR} = \frac{R_3}{R_2 + R_3} x V_{OV} \tag{7}$$

For minimizing the input current drawn from the battery through resistors R_2 and R_3, it recommended to use higher value of resistance. Using high value resistors will add error in the calculations because the current through the resistors at higher value will become comparable to the leakage current into the OV pin. Maximum leakage current into the OV pin is 1 µA and choosing (R_2 + R_3) < 120 kΩ ensures current through resistors is 100 times greater than leakage through OV pin.

Based on the device electrical characteristics, V_{OVR} is 1.233V V. To limit (R_2 + R_3) < 120 kΩ, select (R_2) = 100 kΩ. Solving Equation 7 gives R_3 = 3.45 kΩ.

Closest standard 1% resistor values are R2 = 100kΩ and R3 = 3.48kΩ.

9.3.2.5 MOSFET Q1 Selection

The V_{DS} rating of the MOSFET Q1 should be minimum 200V for a output cutoff design where output can reach 0 V while the load dump transient is present and should be a minimum of 164.5V when output is clamped to 37V (±1.5V). The V_{GS} rating is based on HGATE-OUT maximum voltage of 15V. A 20V V_{GS} rated MOSFET is recommended.

Power dissipation on MOSFET Q1 on a design where output is clamped is critical and SOA characteristics of the MOSFET need to be considered with sufficient design margin for reliable operation.

9.3.2.6 Input TVS selection

Two TVS diodes D3 and D4 are required at the input. The breakdown voltage of TVS in the positive side should be higher than the maximum system voltage 200V. On the negative side clamping, diode D4 is used to clamp ISO 7637-2 pulse 1 and its selection is similar to procedure in TVS selection for 24V Battery Systems. SMBJ150A for D3 and SMBJ33CA for D4 are recommended.

9.3.2.7 MOSFET Q2 Selection

Design requirements for selecting Q2 is similar to MOSFET Q1 selection in Table 2 and hence the procedure for selecting MOSFET Q2 is same as outlined in MOSFET Selection: Blocking MOSFET Q1. MOSFET BUK7Y4R8-60E is selected based on the design requirements.

ADVANCE INFORMATION

9.3.3 Application Curves

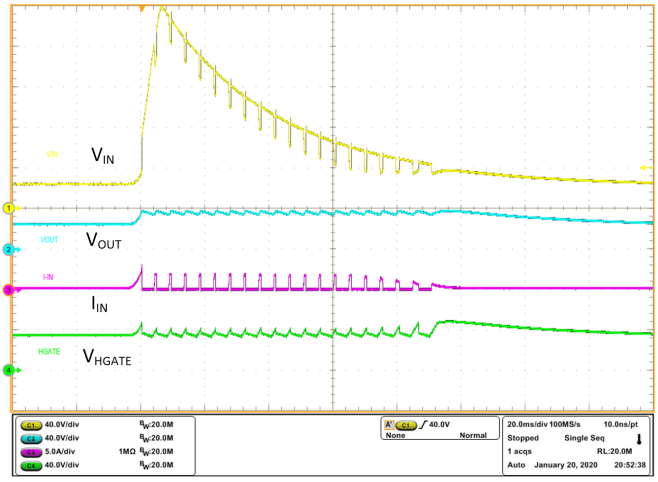


Figure 31. Unsuppressed Load Dump 200V - Output Clamp

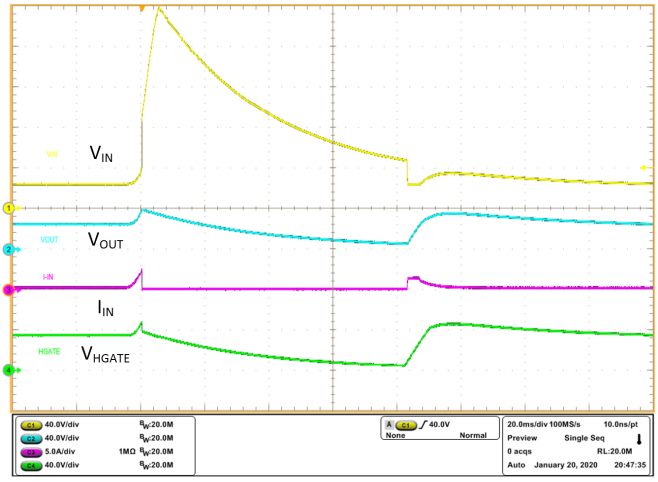


Figure 32. Unsuppressed Load Dump 200V - Output Cut-off

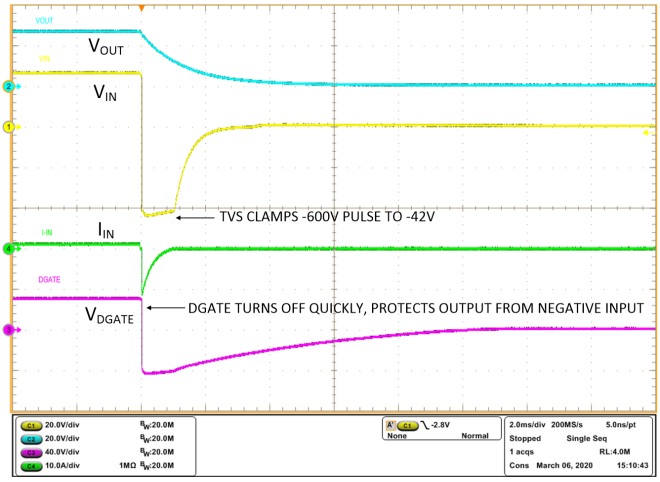


Figure 33. ISO 7637-2 Pulse 1 -600V 50Ω

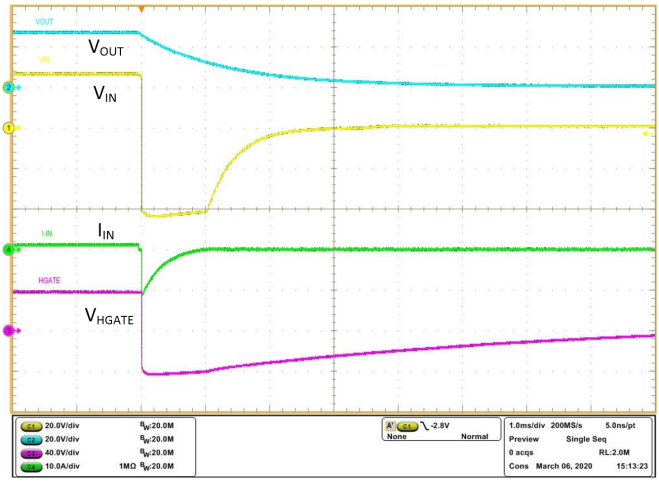


Figure 34. ISO 7637-2 Pulse 1 -600V 50Ω

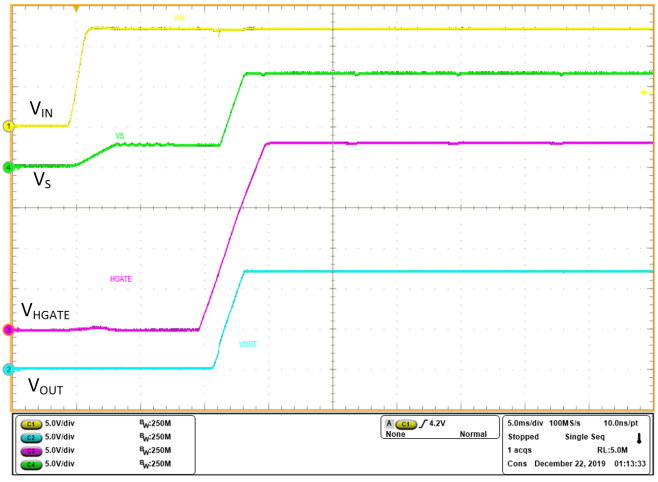


Figure 35. Power up 12V - HGATE and Output

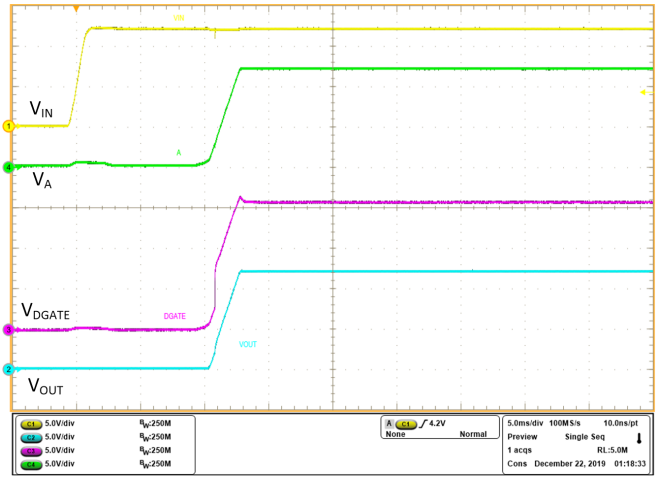


Figure 36. Power up 12V - DGATE and A

ADVANCE INFORMATION

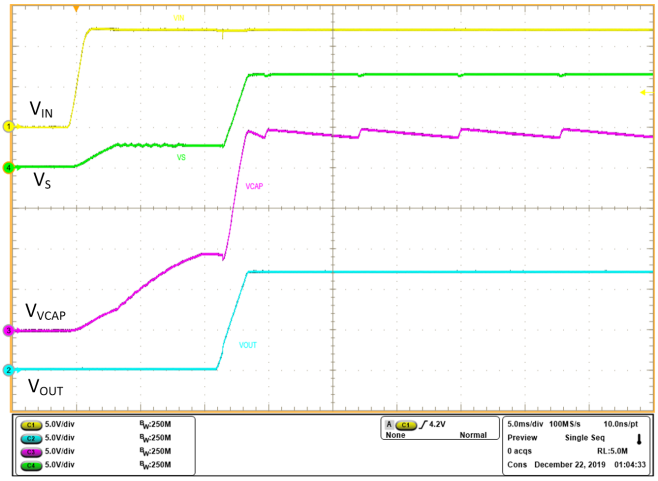


Figure 37. Power up 12V - Charge Pump VCAP

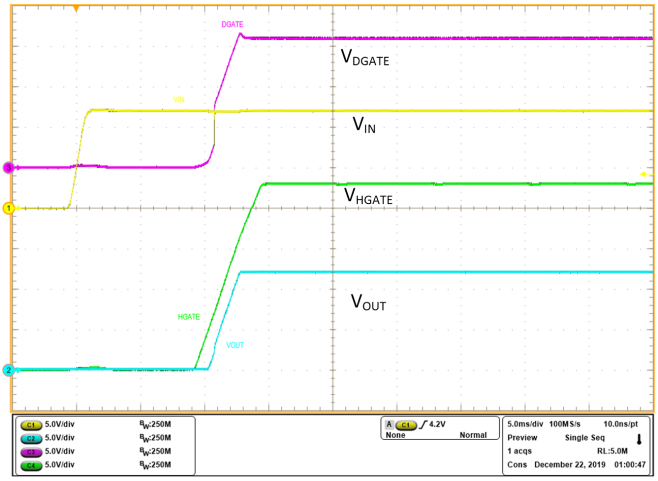


Figure 38. Power up 12V - DGATE and HGATE

9.4 Do's and Don'ts

Leave exposed pad (RTN) of the IC floating. Do not connect it to the GND plane. Connecting RTN to GND disables the Reverse Polarity protection feature.

ADVANCE INFORMATION

10 Power Supply Recommendations

10.1 Transient Protection

When the external MOSFETs turn OFF during the conditions such as over voltage cut-off, reverse current blocking, EN/UVLO causing an interruption of the current flow, the input line inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Use of a Schottky diode across the output and GND to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ to approximately 0.1 µF) to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with Equation 8.

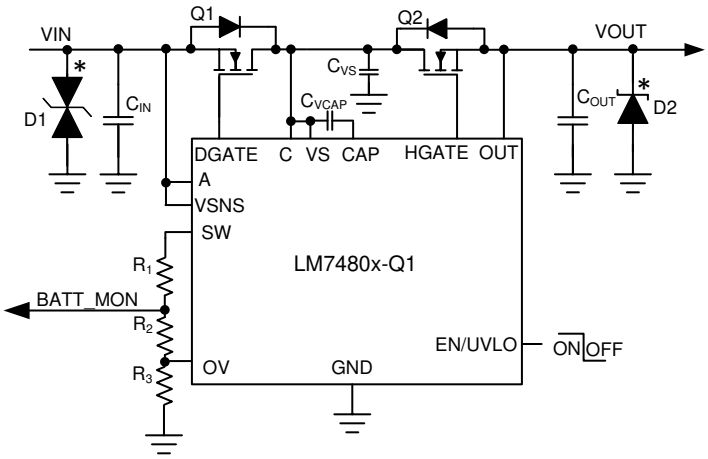
$$V_{spike(Absolute)} = V_{(IN)} + I_{(Load)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (8)$$

where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients can occur during EMC testing such as automotive ISO7637 pulses.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 39



* Optional components needed for suppression of transients

Figure 39. Circuit Implementation with Optional Protection Components for LM7480x-Q1

ADVANCE INFORMATION

10.2 TVS selection for 12V Battery Systems

In selecting the TVS, important specifications are breakdown voltage and clamping voltage. The breakdown voltage of the TVS+ should be higher than 24-V jump start voltage and 35-V suppressed load dump voltage and less than the maximum ratings of LM7480x-Q1 (65 V). The breakdown voltage of TVS- should be beyond than maximum reverse battery voltage –16 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

Clamping voltage is the voltage the TVS diode clamps in high current pulse situations and this voltage is much higher than the breakdown voltage. In the case of an ISO 7637-2 pulse 1, the input voltage goes up to –150 V with a generator impedance of 10 Ω. This translates to 15 A flowing through the TVS - and the voltage across the TVS would be close to its clamping voltage.

The next criterion is that the absolute maximum rating of cathode to anode voltage of the LM7480x-Q1 (85 V) and the maximum V_{DS} rating MOSFET are not exceeded. In the design example, 60-V rated MOSFET is chosen and maximum limit on the cathode to anode voltage is 60 V.

During ISO 7637-2 pulse 1, the anode of LM7480x-Q1 is pulled down by the ISO pulse, clamped by TVS- and the MOSFET Q1 is turned off quickly to prevent reverse current from discharging the bulk output capacitors. When the MOSFET turns off, the cathode to anode voltage seen is equal to (TVS Clamping voltage + Output capacitor voltage). If the maximum voltage on output capacitor is 16-V (maximum battery voltage), then the clamping voltage of the TVS- should not exceed, (60 V – 16) V = –44 V.

The SMBJ33CA TVS diode can be used for 12-V battery protection application. The breakdown voltage of 36.7 V meets the jump start, load dump requirements on the positive side and 16-V reverse battery connection on the negative side. During ISO 7637-2 pulse 1 test, the SMBJ33CA clamps at –44 V with 12 A of peak surge current as shown in and it meets the clamping voltage ≤ 44 V.

SMBJ series of TVS' are rated up to 600 W peak pulse power levels and are sufficient for ISO 7637-2 pulses.

10.3 TVS selection for 24V Battery Systems

For 24-V battery protection application, the TVS and MOSFET in Figure 6 needs to be changed to suit 24-V battery requirements.

The breakdown voltage of the TVS+ should be higher than 48-V jump start voltage, less than the absolute maximum ratings of anode and enable pin of LM7480x-Q1 (70 V) and should withstand 65-V suppressed load dump. The breakdown voltage of TVS- should be lower than maximum reverse battery voltage –32 V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

During ISO 7637-2 pulse 1, the input voltage goes up to –600 V with a generator impedance of 50 Ω. This translates to 12-A flowing through the TVS-. The clamping voltage of the TVS- cannot be same as that of 12-V battery protection circuit. Because during the ISO 7637-2 pulse, the Anode to Cathode voltage seen is equal to (-TVS Clamping voltage + Output capacitor voltage). For 24-V battery application, the maximum battery voltage is 32 V, then the clamping voltage of the TVS- should not exceed, 85 V – 32 V = 53 V.

Single bi-directional TVS cannot be used for 24-V battery protection because breakdown voltage for TVS+ ≥ 65V, maximum clamping voltage is ≤ 53 V and the clamping voltage cannot be less than the breakdown voltage. Two un-directional TVS connected back-back needs to be used at the input. For positive side TVS+, SMBJ58A with the breakdown voltage of 64.4-V (minimum), 67.8 (typical) is recommended. For the negative side TVS-, SMBJ28A with breakdown voltage close to 32-V (to withstand maximum reverse battery voltage –32 V) and maximum clamping voltage of 42.1 V is recommended.

For 24-V battery protection, a 75-V rated MOSFET is recommended to be used along with SMBJ28A and SMBJ58A connected back-back at the input.

10.4 Application Limitations

This section highlights some limitations in the application which were identified during bench evaluation of the existing LM7480x-Q1 silicon on the evaluation module (EVM)

ADVANCE INFORMATION

Application Limitations (continued)

10.4.1 Reverse Current Blocking Threshold ($V_{(AC\_REV)}$)

The $V_{(AC\_REV)}$ threshold is measured at – 2 mV (typical) in the current IC versus the target value of – 4.5 mV (typical). With – 2 mV (typical) value, statistically the threshold can hit > 0 mV which can result in unstable operation.

- A design fix will be included in the final release of the IC

ADVANCE INFORMATION

11 Layout

11.1 Layout Example

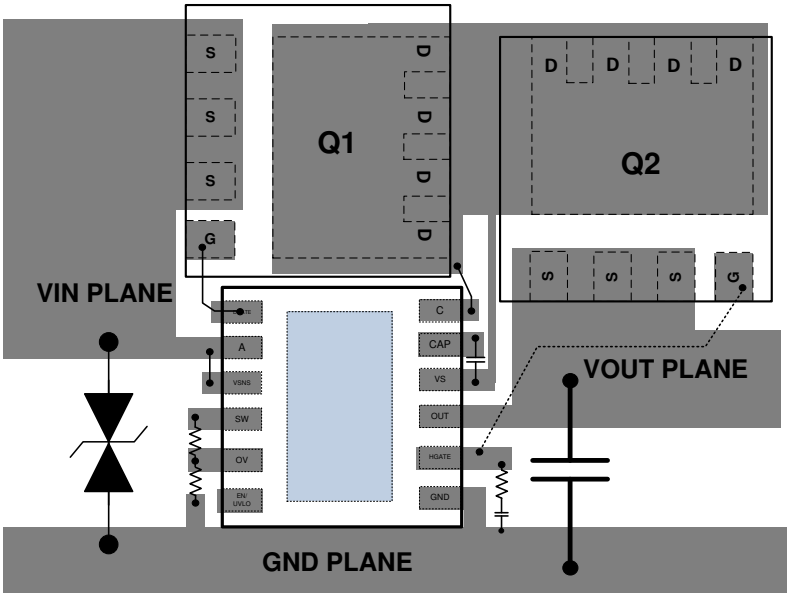


Figure 40. PCB Layout Example for Common Drain Configuration

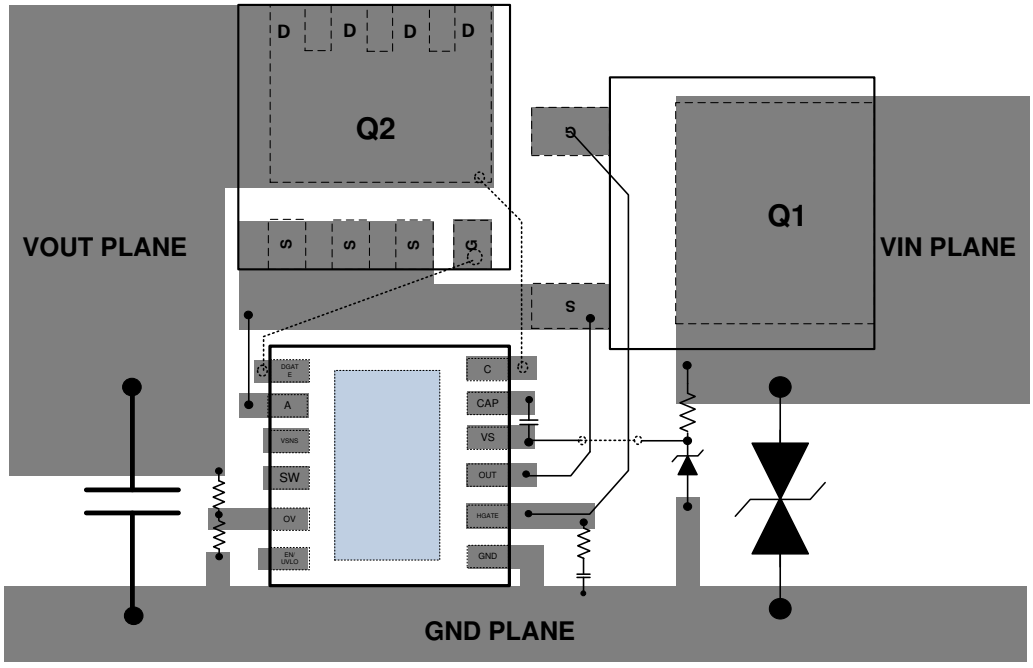


Figure 41. PCB Layout Example for Common Source Configuration

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
PLM74800QDRRRQ1	PREVIEW	WSON	DRR	12	3000	Green (RoHS & no Sb/Br)	NiPdAu	Level-2- 260°C-1 YEAR	–40 to 125	P74800
PLM74801QDRRRQ1	PREVIEW	WSON	DRR	12	3000	Green (RoHS & no Sb/Br)	NiPdAu	Level-2- 260°C-1 YEAR	–40 to 125	P74801

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

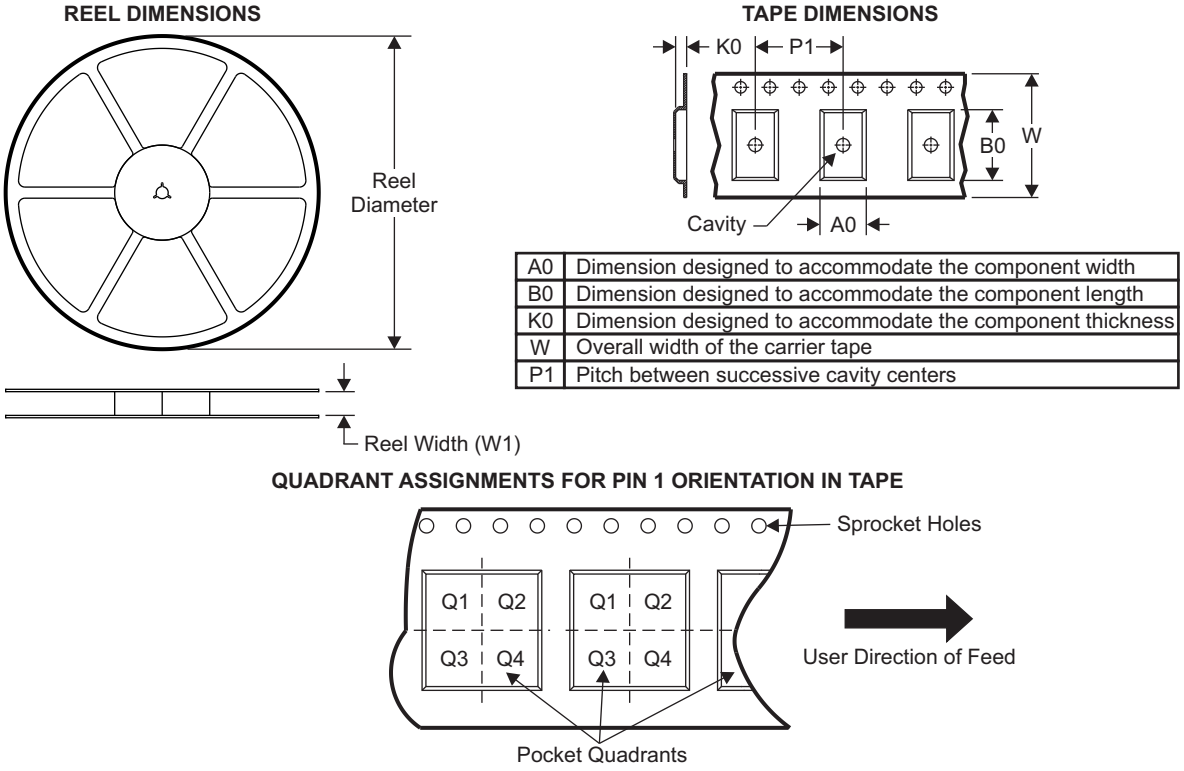
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

ADVANCE INFORMATION

13.1.2 Tape and Reel Information



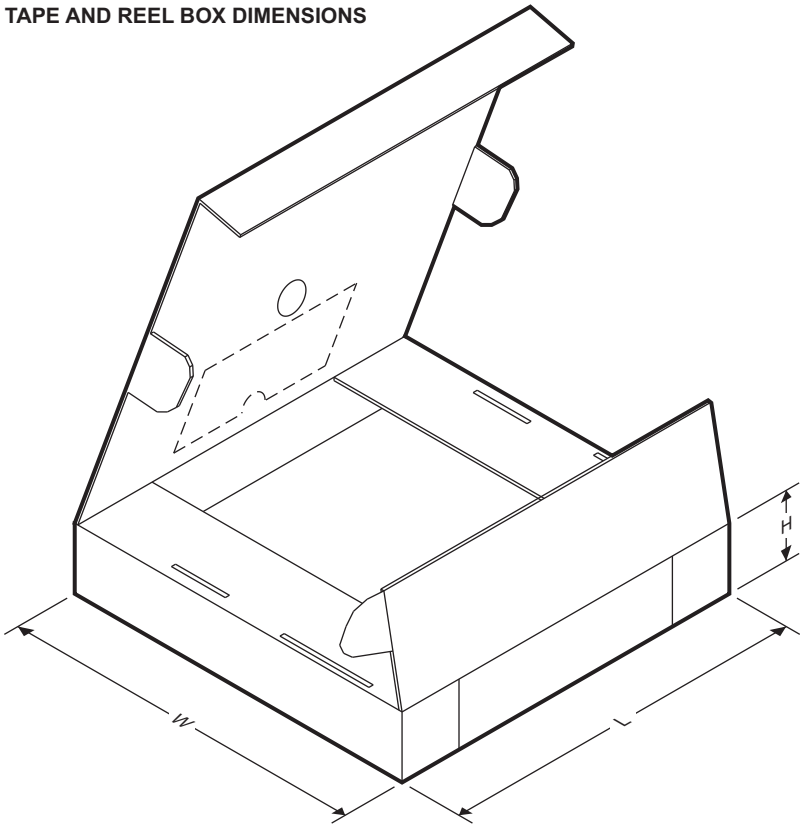
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PLM74800QDRRRQ1	WSON	DRR	12	3000	300	12.4	3.3	3.3	1.1	8	12	3
PLM74801QDRRRQ1	WSON	DRR	12	3000	300	12.4	3.3	3.3	1.1	8	12	3

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



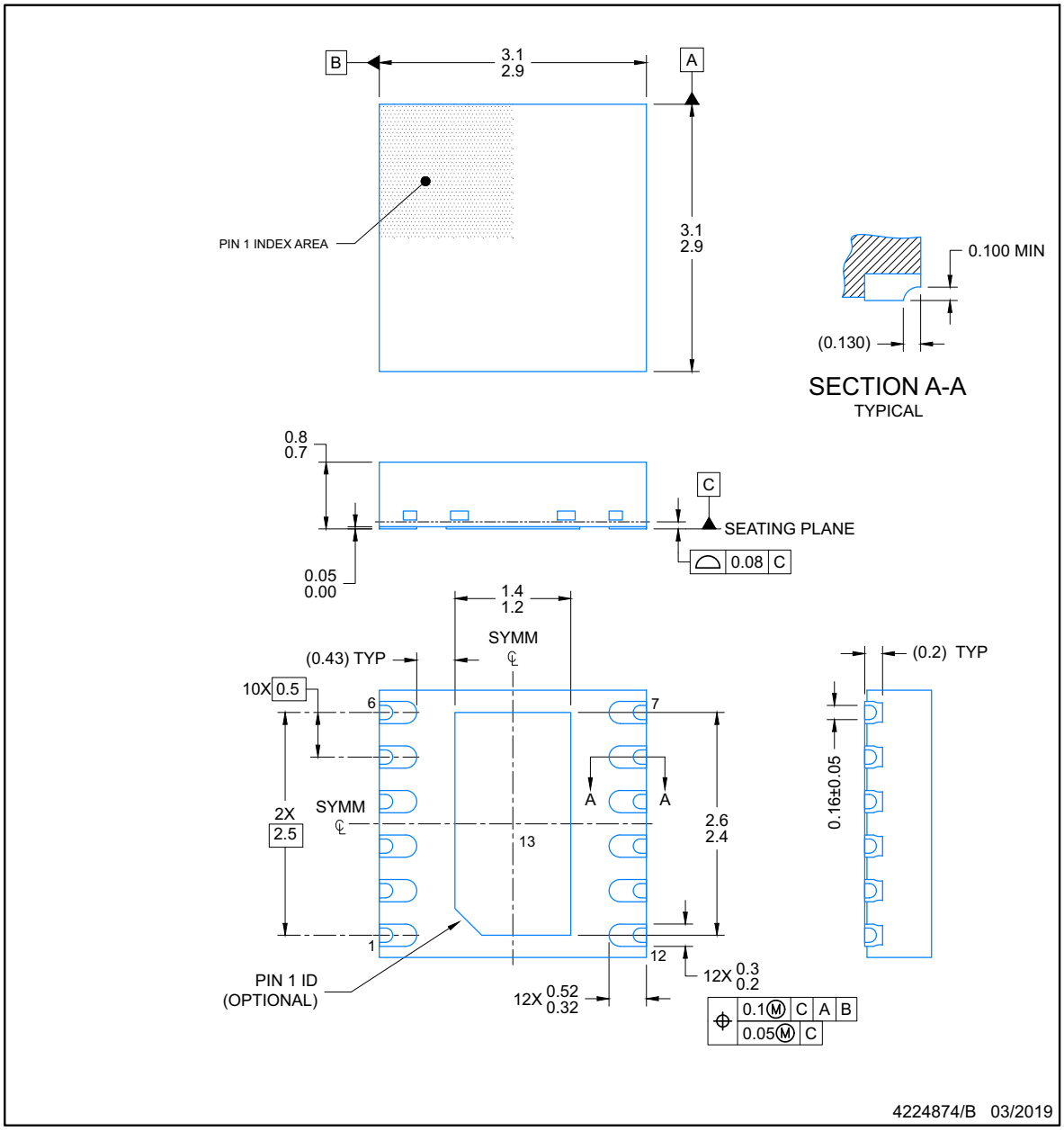
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PLM74800QDRRRQ1	WSON	DRR	12	3000	367	367	35
PLM74801QDRRRQ1	WSON	DRR	12	3000	367	367	35

PACKAGE OUTLINE

DRR0012E

WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

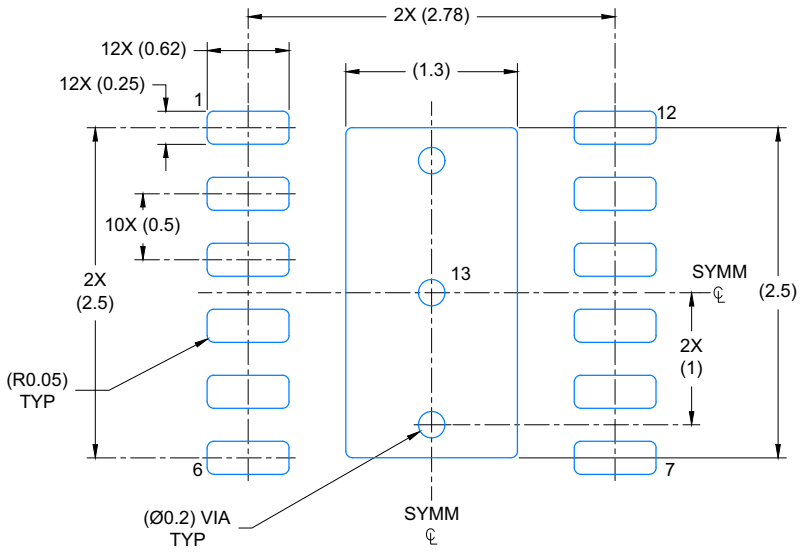
ADVANCE INFORMATION

ADVANCE INFORMATION

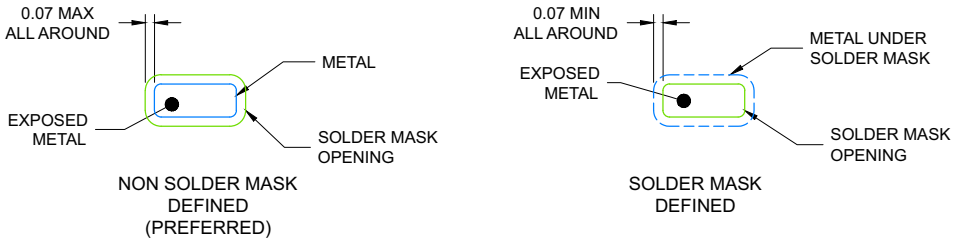
EXAMPLE BOARD LAYOUT

DRR0012E — **WSON - 0.8 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224874/B 03/2019

NOTES: (continued)

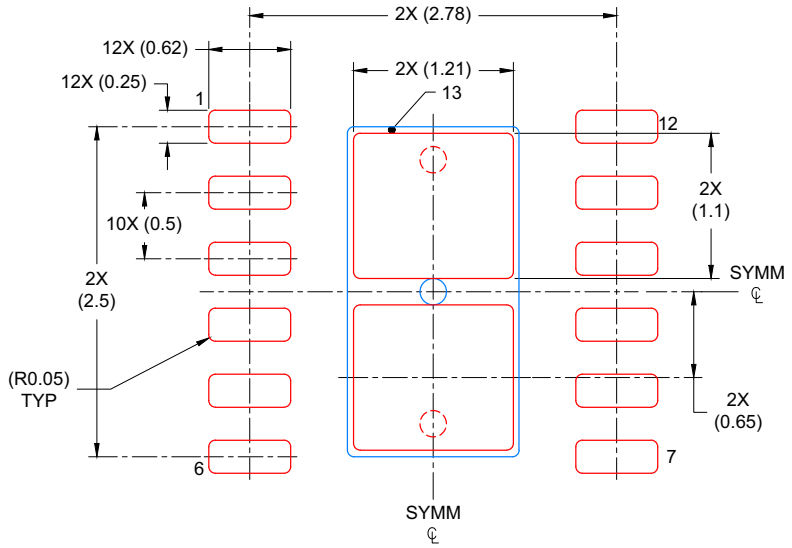
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRR0012E

WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED COVERAGE BY AREA
SCALE: 20X

4224874/B 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74800QDRRRQ1	PREVIEW	SON	DRR	12	3000	TBD	Call TI	Call TI	-40 to 125		
LM74801QDRRRQ1	PREVIEW	SON	DRR	12	3000	TBD	Call TI	Call TI	-40 to 125		
PLM74800QDRRRQ1	ACTIVE	SON	DRR	12	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PLM74801QDRRRQ1	ACTIVE	SON	DRR	12	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

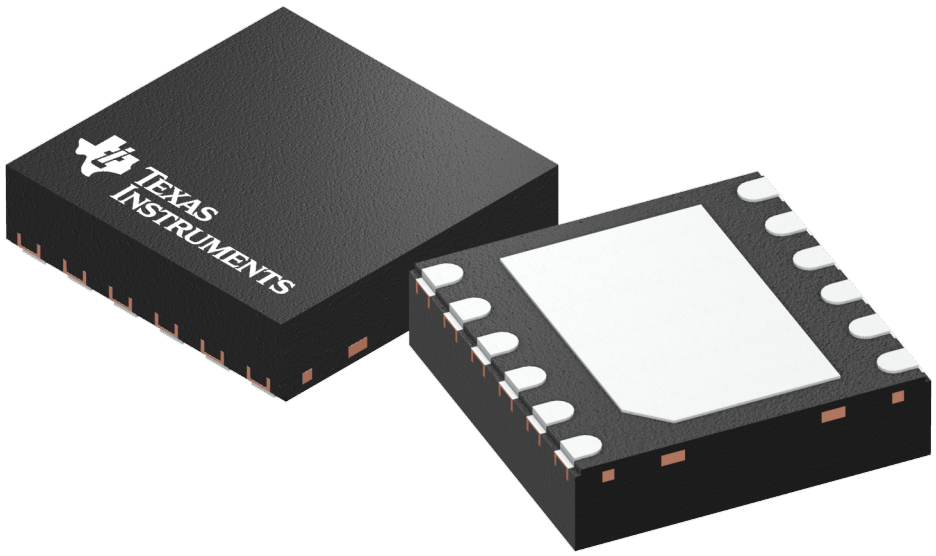
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

DRR 12 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4223490/A

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265