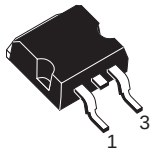
STB75NH02L

N-CHANNEL 24V - 0.0062Ω -75A - D²PAK
STripFET™ III POWER MOSFET

TARGET DATA

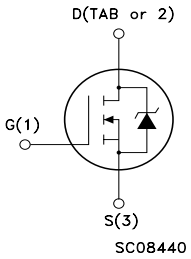
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STB75NH02L	24V	< 0.008Ω	75A

- TYPICAL $R_{DS}(on)$ = 0.0062Ω @ 10 V
- TYPICAL $R_{DS}(on)$ = 0.008Ω @ 5 V
- $R_{DS(ON)}$ * Q_g INDUSTRY's BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- SURFACE-MOUNTING D²PAK (TO-263) POWER PACKAGE IN TUBE (NO SUFFIX) OR IN TAPE & REEL (SUFFIX "T4")



D²PAK
TO-263
(Suffix "T4")

INTERNAL SCHEMATIC DIAGRAM



DESCRIPTION

The **STB75NH02L** utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB75NH02LT4	B75NH02L	D²PAK	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{spike}(1)	Drain-source Voltage Rating	30	V
V_{DS}	Drain-source Voltage (V_{GS} = 0)	24	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	24	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuous) at T_C = 25°C	75	A
I_D	Drain Current (continuous) at T_C = 100°C	53	A
I_{DM} (5)	Drain Current (pulsed)	300	A
P_{TOT}	Total Dissipation at T_C = 25°C	85	W
	Derating Factor	1	W/°C
E_{AS} (2)	Single Pulse Avalanche Energy	TBD	mJ
T_{stg}	Storage Temperature	-55 to 175	°C
T_j	Max. Operating Junction Temperature		

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T_l	Maximum Lead Temperature for Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 25 mA, V_{GS} = 0	24			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = 20V			1	µA
		V_{DS} = 20V, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V, I_D = 30 A		0.0062	0.008	Ω
		V_{GS} = 5 V, I_D = 30 A		0.008	0.014	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)
DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (3)	Forward Transconductance	V_{DS} = 15 V , I_D = 30 A		TBD		S
C_{iss}	Input Capacitance	V_{DS} = 15 V, f = 1 MHz, V_{GS} = 0		2000		pF
C_{oss}	Output Capacitance			420		pF
C_{rss}	Reverse Transfer Capacitance			210		pF
R_g	Gate Input Resistance	f= 1 MHz Gate DC Bias= 0 Test Signal Level= 20 mV Open Drain		1		Ω

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 10 V, I_D = 37.5 A R_G = 4.7Ω V_{GS} = 10 V (see test circuit, Figure 3)		TBD TBD		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 10 V, I_D =75 A, V_{GS} = 10 V		35 TBD TBD	47	nC nC nC
Q_{oss} (4)	Output Charge	V_{DS} = 16 V, V_{GS} = 0		TBD		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off-Delay Time Fall Time	V_{DD} = 10 V, I_D = 37.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see test circuit, Figure 3)		TBD TBD		ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				75	A
I_{SDM} (1)	Source-drain Current (pulsed)				300	A
V_{SD} (3)	Forward On Voltage	I_{SD} = 37.5 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 75 A, di/dt = 100A/µs, V_{DD} = 15V, T_j = 150°C (see test circuit, Figure 5)		TBD TBD TBD		ns nC A

1. Garanted when external R_g = 4.7 Ω and $t_f < t_f$ max
2. Starting T_j = 25°C, I_D = 25A, V_{DD} = 15V
3. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
4. $Q_{oss} = C_{oss}*\Delta V_{in}$, $C_{oss} = C_{gd}+C_{ds}$. See Appendix A
5. Pulse width limited by safe operating area

Fig. 1: Unclamped Inductive Load Test Circuit

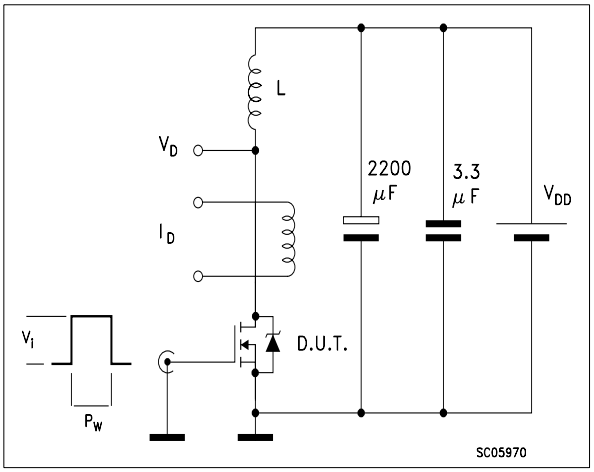


Fig. 2: Unclamped Inductive Waveform

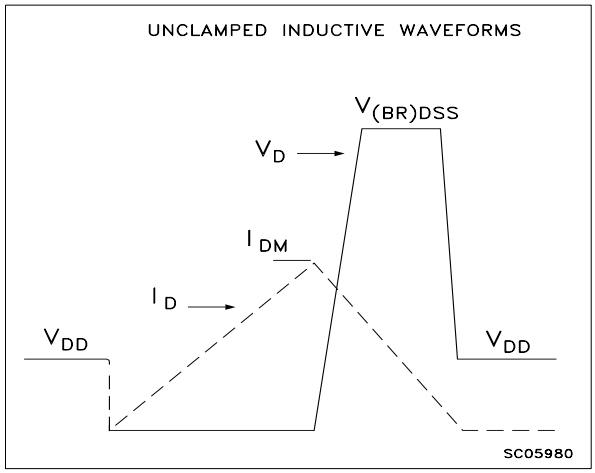


Fig. 3: Switching Times Test Circuit For Resistive Load

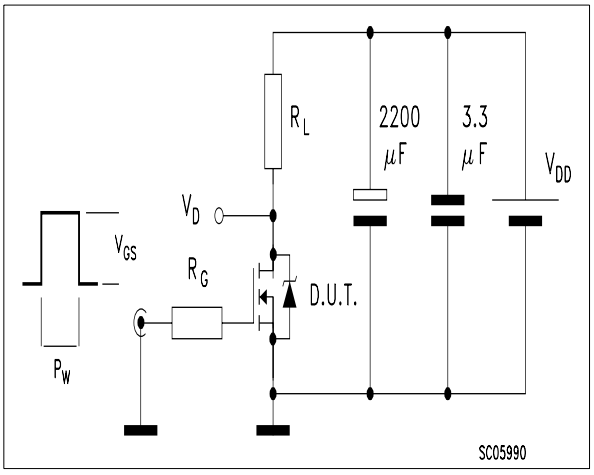


Fig. 4: Gate Charge test Circuit

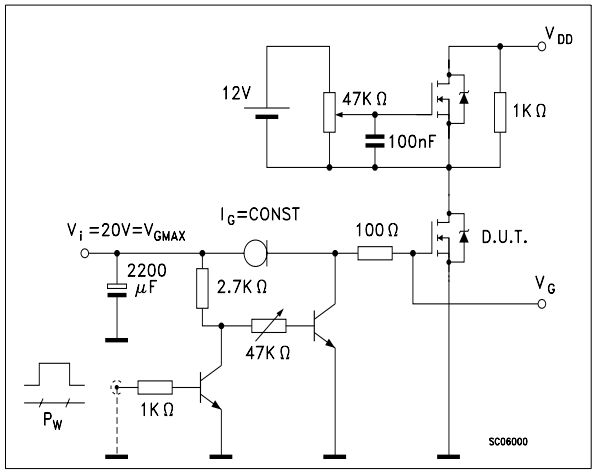
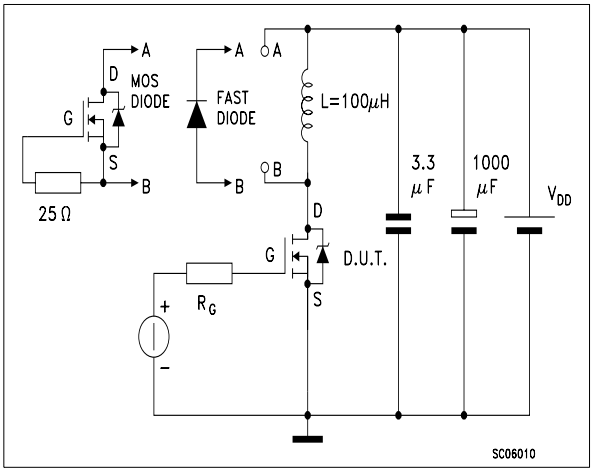
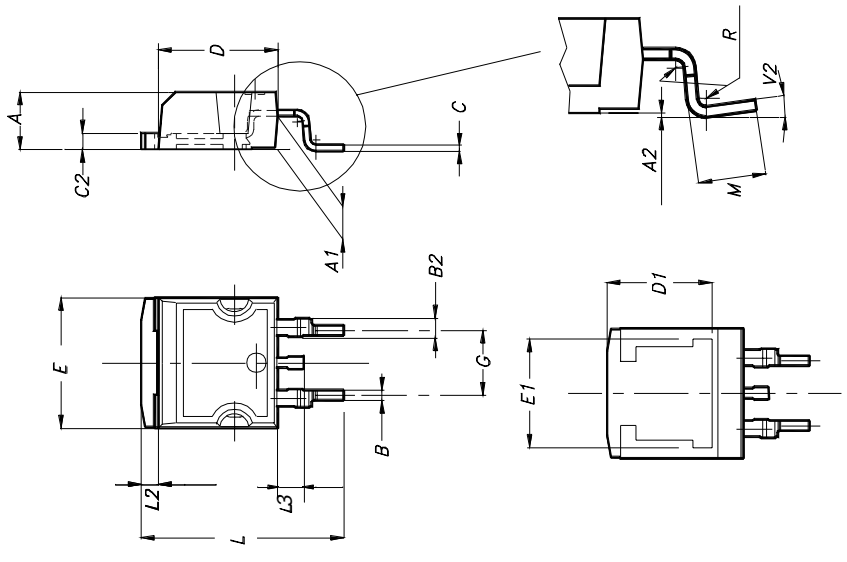


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

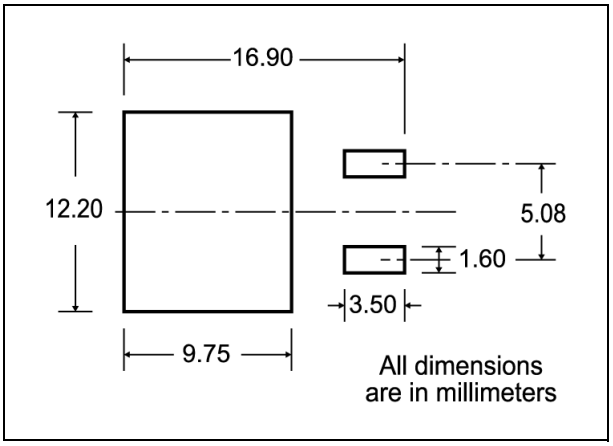


D²PAK MECHANICAL DATA

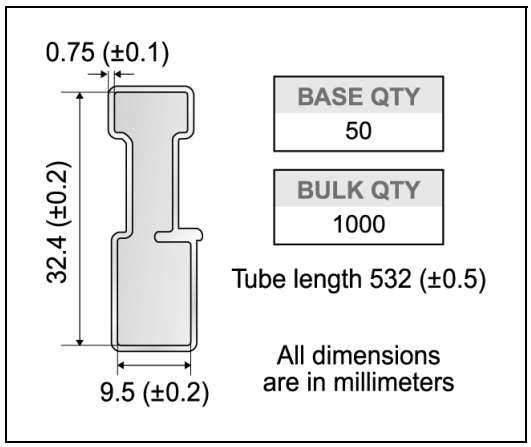
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0º		8º			



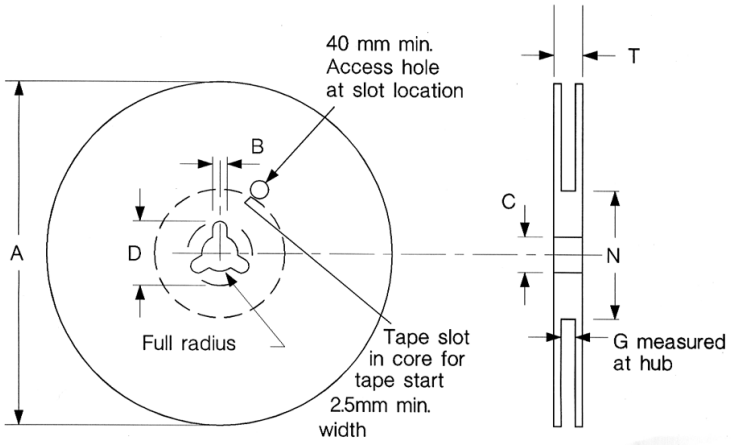
D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*



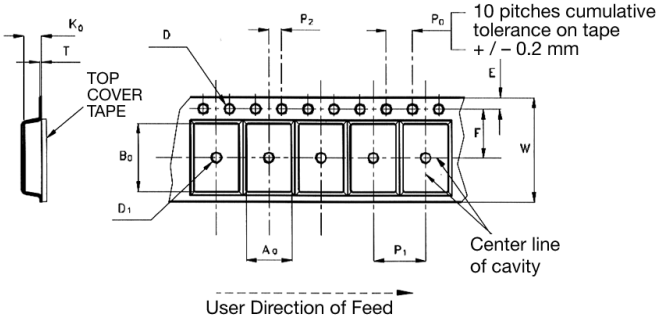
REEL MECHANICAL DATA

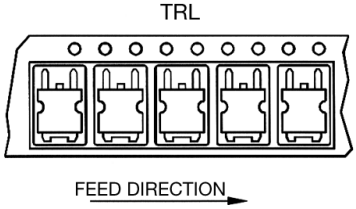
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

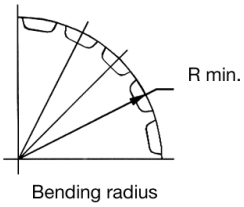
BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956





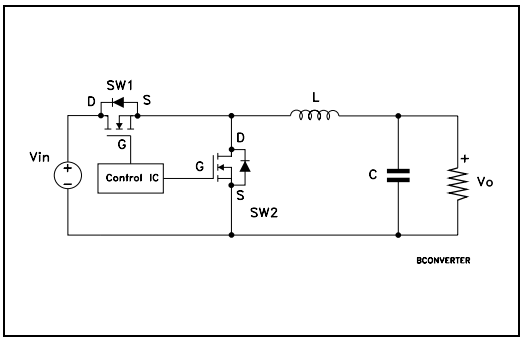


* on sales type

Appendix A: Buck Converter Power Losses Estimation

DESCRIPTION

The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.



The low side (SW2) device requires:

- Very low RDS(on) to reduce conduction losses
- Small Q_{gls} to reduce the gate charge losses
- Small C_{oss} to reduce losses due to output capaci tance
- Small Q_{rr} to reduce losses on SW1 during its turn-on
- The C_{gd}/C_{gs} ratio lower than V_{th}/V_{GG} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon

The high side (SW1) device requires:

- Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Q_g to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses

		High Side Switch (SW1)	Low Side Switch (SW2)
$P_{conduction}$		$R_{DS(on)SW1}*I_L^2*\delta$	$R_{DS(on)SW2}*I_L^2*(1-\delta)$
$P_{switching}$		$V_{in}*(Q_{gsth(SW1)}+Q_{gd(SW1)})*f*\frac{I_L}{I_g}$	Zero Voltage Switching
P_{diode}	Recovery	Not Applicable	[1] $V_{in}*Q_{rr(SW2)}*f$
	Conduction	Not Applicable	$V_{f(SW2)}*I_L*t_{deadtime}*f$
$P_{gate(Q_g)}$		$Q_{g(SW1)}*V_{gg}*f$	$\mathbf{Q_{gls(SW2)}*V_{gg}*f}$
P_{Qoss}		$\frac{V_{in}*Q_{oss(SW1)}*f}{2}$	$\frac{V_{in}*Q_{oss(SW2)}*f}{2}$

Parameter	Meaning
δ	Duty-Cycle
Q_{gsth}	Post Threshold Gate Charge
Q_{gls}	Third Quadrant Gate Charge
Pconduction	On State Losses
Pswitching	On-off Transition Losses
Pdiode	Conduction and Reverse Recovery Diode Losses
Pdiode	Gate Drive Losses
P_{Qoss}	Output Capacitance Losses

[1] Dissipated by SW1 during turn-on

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