RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 102 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 720 to 960 MHz.

900 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 48 Vdc, I_{DQA} = 750 mA, V_{GSB} = 0.8 Vdc, P_{out} = 102 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
920 MHz	18.7	53.5	7.2	–29.5
940 MHz	18.9	54.0	7.0	–29.2
960 MHz	18.5	53.4	6.8	–28.8

700 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 46 Vdc, I_{DQA} = 300 mA, V_{GSB} = 2.3 Vdc, P_{out} = 81 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

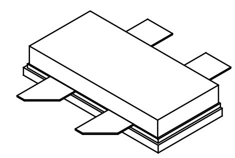
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	P3dB (dBm)	ACPR (dBc)
758 MHz	18.3	56.1	7.9	57.4	–29.7
780 MHz	18.7	55.8	8.0	57.5	–31.0
803 MHz	18.8	55.5	8.0	57.5	–33.0

Features

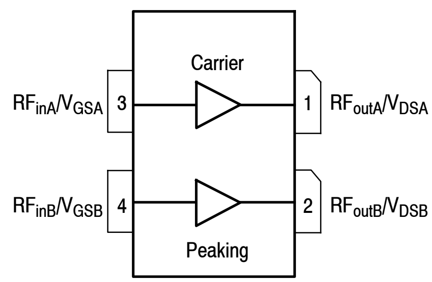
- Advanced high performance in-package Doherty
- Greater negative gate-source voltage range for improved Class C operation
- Designed for digital predistortion error correction systems

A2V09H400-04S

720–960 MHz, 102 W AVG., 48 V AIRFAST RF POWER LDMOS TRANSISTOR



NI-780S-4L



(Top View)

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +105	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	55, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range [1,2]	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value [2,3]	Unit
Thermal Resistance, Junction to Case Case Temperature 81°C, 107 W Avg., W-CDMA, 48 Vdc, I_{DQA} = 750 mA, V_{GSB} = 0.8 Vdc, 940 MHz	$R_{\theta JC}$	0.51	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	2
Charge Device Model (per JS-002-2014)	C3

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics [4]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 105 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 55 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics — Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 137 μAdc)	$V_{GS(th)}$	1.3	1.7	2.3	Vdc
Gate Quiescent Voltage (V_{DD} = 48 Vdc, I_D = 750 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.0	2.4	2.8	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.4 Adc)	$V_{DS(on)}$	0.1	0.2	0.4	Vdc
On Characteristics — Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 211 μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.1 Adc)	$V_{DS(on)}$	0.1	0.2	0.5	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
4. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1] (In NXP Doherty Production Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 750 mA, V_{GSB} = 0.8 Vdc, P_{out} = 102 W Avg., f = 920 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	18.0	18.7	21.0	dB
Drain Efficiency	η_D	48.5	53.5	—	%
P_{out} @ 3 dB Compression Point, CW	P3dB	55.4	56.9	—	dBm
Adjacent Channel Power Ratio	ACPR	—	–29.5	–27.5	dBc
Wideband Ruggedness (In NXP Doherty Production Test Fixture, 50 ohm system) I_{DQA} = 750 mA, V_{GSB} = 0.8 Vdc, f = 940 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR					
ISBW of 400 MHz at 55 Vdc, 239 W Avg. Modulated Output Power (5 dB Input Overdrive from 107 W Avg. Modulated Output Power)	No Device Degradation				
Typical Performance (In NXP Doherty Production Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 750 mA, V_{GSB} = 0.8 Vdc, 920–960 MHz Bandwidth					
P_{out} @ 3 dB Compression Point [2]	P3dB	—	512	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 920–960 MHz frequency range)	Φ	—	–16	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	80	—	MHz
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 102 W Avg.	G_F	—	0.6	—	dB
Gain Variation over Temperature (–40°C to +85°C)	ΔG	—	0.031	—	dB/°C
Output Power Variation over Temperature (–40°C to +85°C)	ΔP1dB	—	0.009	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A2V09H400-04SR3	R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel	NI-780S-4L

1. Part internally input matched.
2. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

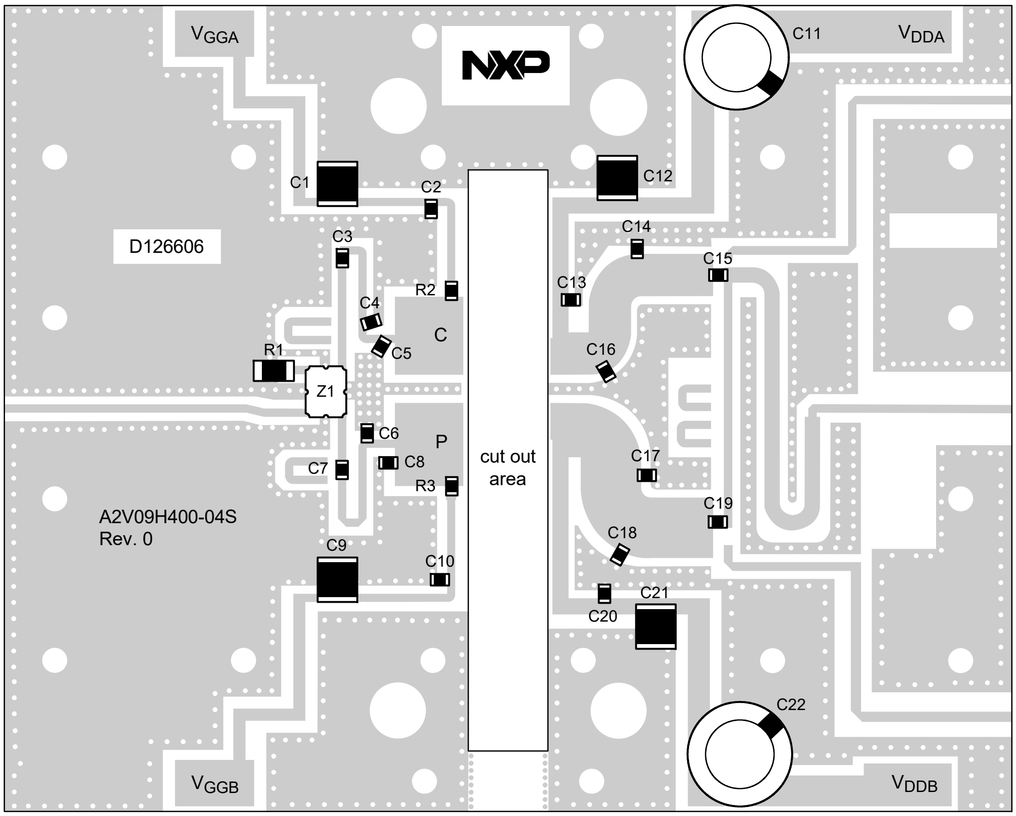


Figure 2. A2V09H400-04S Test Circuit Component Layout

Table 6. A2V09H400-04S Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C9, C12, C21	10 μF Chip Capacitor	C5750X7S2A106M230KB	TDK
C2, C3, C7, C10, C13, C20	47 pF Chip Capacitor	600F470JT250XT	ATC
C4, C8	3.3 pF Chip Capacitor	600F3R3BT250XT	ATC
C5	5.6 pF Chip Capacitor	600F5R6BT250XT	ATC
C6	6.2 pF Chip Capacitor	600F6R2BT250XT	ATC
C11, C22	470 μF, 100 V Electrolytic Capacitor	MCGPR100V477M16X32	Multicomp
C14	11 pF Chip Capacitor	600F110JT250XT	ATC
C15	10 pF Chip Capacitor	600F100JT250XT	ATC
C16	12 pF Chip Capacitor	600F120JT250XT	ATC
C17	7.5 pF Chip Capacitor	600F7R5JT250XT	ATC
C18	3.9 pF Chip Capacitor	600F3R9BT250XT	ATC
C19	5.1 pF Chip Capacitor	600F5R1BT250XT	ATC
R1	50 Ω, 10 W Termination Chip Resistor	C10A50Z4	Anaren
R2, R3	4.75 Ω, 1/4 W Chip Resistor	CRCW12064R75FKEA	Vishay
Z1	800–1000 MHz, 90°, 2 dB Asymmetric Coupler	CMX09Q02	RN2 Technologies
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D126606	MTL

P3dB LOAD PULL PERFORMANCE, CARRIER — 758–821 MHz

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQA} = 750 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	η_D (%)	AM/PM (°)
758	3.20 – j1.77	3.30 + j2.10	2.80 – j0.20	18.4	54.8	62.7	–14
790	2.80 – j2.10	3.00 + j2.50	2.70 – j0.30	18.5	54.7	60.8	–15
803	2.50 – j2.50	2.90 + j2.60	2.80 – j0.20	18.5	54.7	61.2	–15
821	3.30 – j2.30	2.90 + j2.80	2.40 + j0.20	18.9	54.6	60.6	–15

(1) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQA} = 750 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

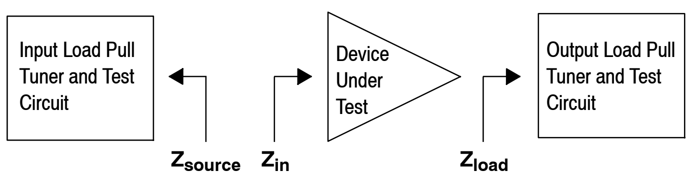
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	η_D (%)	AM/PM (°)
758	3.20 – j1.77	3.04 + j2.10	2.60 + j1.70	20.2	53.9	73.3	–20
790	2.80 – j2.10	2.70 + j2.50	2.70 + j1.70	20.8	53.2	71.6	–24
803	2.50 – j2.50	2.60 + j2.60	2.50 + j2.10	21.1	53.0	72.0	–26
821	3.30 – j2.30	2.60 + j2.80	2.30 + j2.20	21.1	53.1	71.3	–24

(1) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P3dB LOAD PULL PERFORMANCE, PEAKING — 758–821 MHz

Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQB} = 1000 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power				
			P3dB				
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	η_D (%)	AM/PM (°)
758	1.90 – j4.10	1.90 + j3.80	1.90 – j1.02	18.1	56.5	60.8	–15
790	2.10 – j4.30	1.90 + j4.20	2.00 – j0.70	18.5	56.3	62.2	–16
803	1.90 – j4.40	1.90 + j4.40	1.60 – j0.60	18.1	56.5	59.3	–17
821	2.10 – j4.40	2.00 + j4.70	1.70 – j0.40	18.3	56.4	59.8	–18

(1) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 10. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQB} = 1000 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

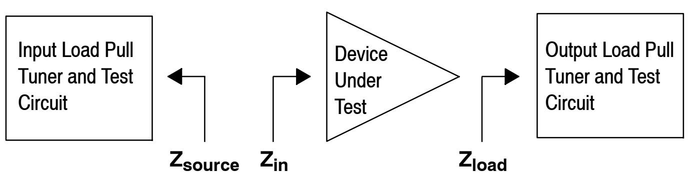
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency				
			P3dB				
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	η_D (%)	AM/PM (°)
758	1.90 – j4.10	1.80 + j3.80	2.10 + j0.90	20.4	54.9	72.2	–22
790	2.10 – j4.30	1.73 + j4.10	2.00 + j0.41	20.2	55.2	69.3	–22
803	1.90 – j4.40	1.70 + j4.30	1.80 + j0.60	20.3	55.0	70.7	–25
821	2.10 – j4.40	1.80 + j4.50	1.60 + j0.70	20.3	55.1	69.8	–25

(1) Load impedance for optimum P3dB efficiency.

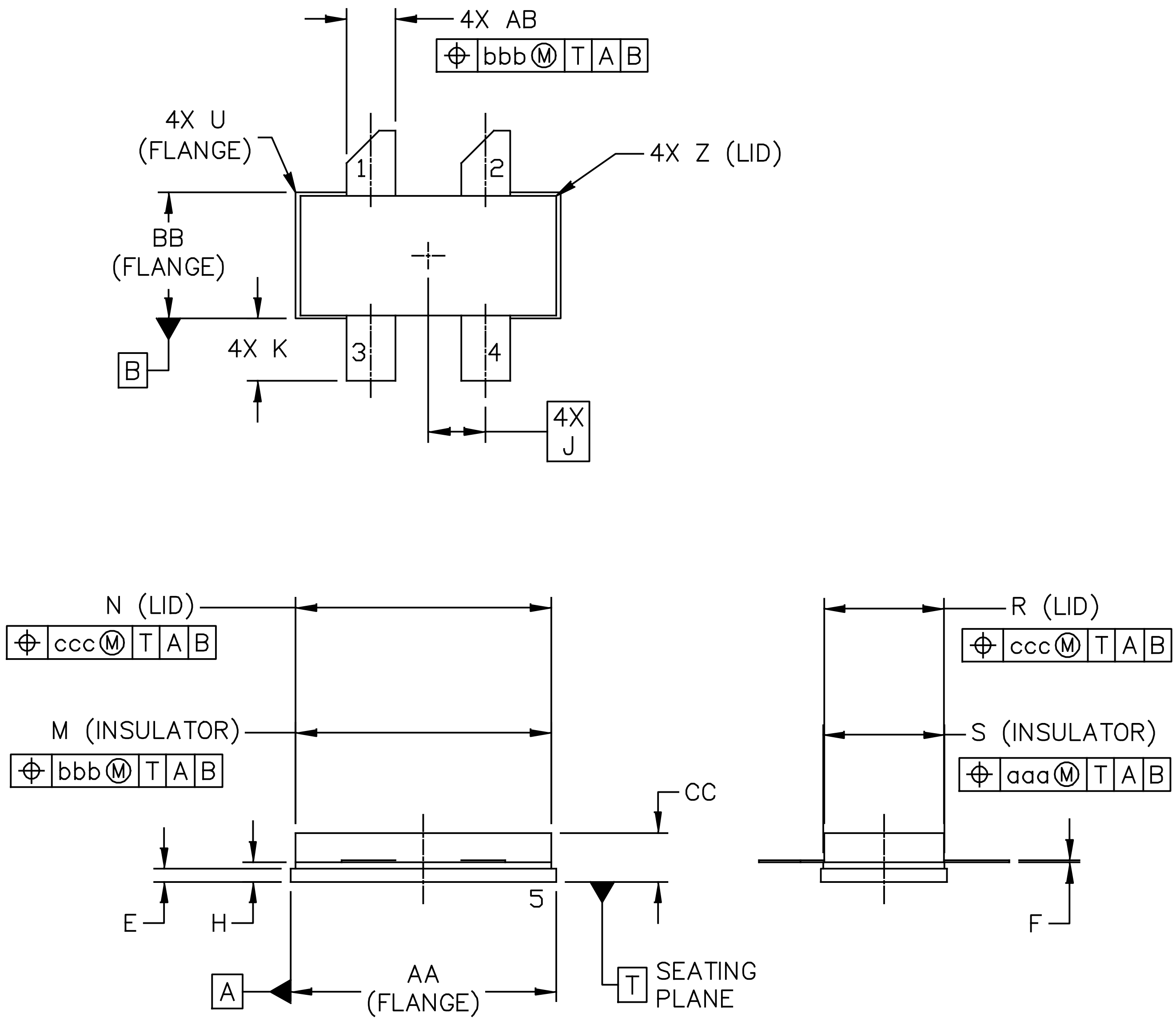
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



PACKAGE DIMENSIONS



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NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

2. CONTROLLING DIMENSION: INCH.

3. DELETED

4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM FLANGE TO CLEAR EPOXY FLOW OUT PARALLEL TO DATUM B.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	.805	.815	20.45	20.70	U		.040		1.02
BB	.382	.388	9.70	9.86	Z		.030		0.76
CC	.125	.170	3.18	4.32	AB	.145	.155	3.68 –	3.94
E	.035	.045	0.89	1.14					
F	.003	.006	0.08	0.15	aaa	.005		0.127	
H	.057	.067	1.45	1.70	bbb	.010		0.254	
J	.175 BSC		4.44 BSC		ccc	.015		0.381	
K	.170	.210	4.32	5.33					
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
R	.365	.375	9.27	9.53					
S	.365	.375	9.27	9.52					

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1908: Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- Electromigration MTTF Calculator
- .s2p File

Development Tools

- Printed Circuit Boards

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2019	• Initial release of data sheet
1	Jan. 2021	• Added 700 MHz performance table with corresponding measured data, p. 1
2	Feb. 2021	• Tables 7–10, Load Pull Performance: added Carrier Side and Peaking Side load pull performance tables showing P3dB performance across the 758–821 MHz band, pp. 5–6

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