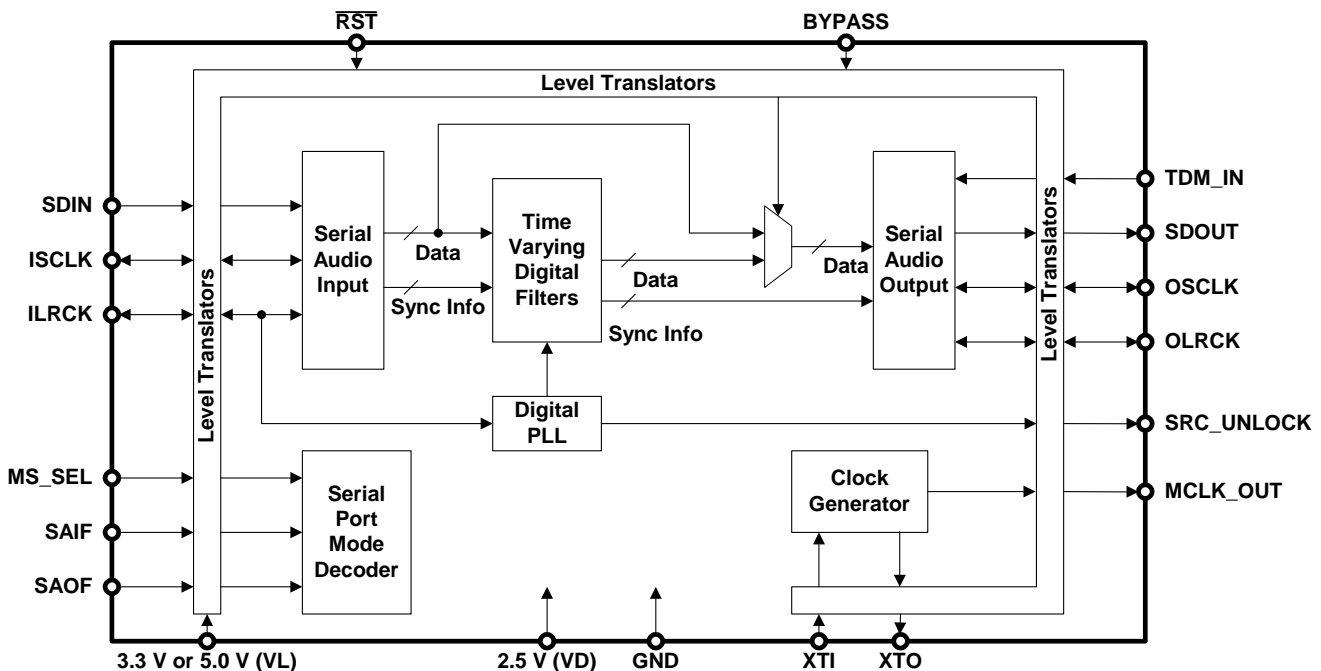


32-bit, 192 kHz Asynchronous Sample Rate Converter

Features

- 175 dB Dynamic Range
- -140 dB THD+N
- No Programming Required
- No External Master Clock Required
- Supports Sample Rates up to 211 kHz
- Input/Output Sample Rate Ratios from 7.5:1 to 1:8
- Master Clock Support for $128 \times f_s$, $256 \times f_s$, $384 \times f_s$, and $512 \times f_s$ (Master Mode)
- 16, 20, 24, or 32-bit Data I/O
- 32-bit Internal Signal Processing
- Dither Automatically Applied and Scaled to Output Resolution
- Flexible 3-Wire Serial Digital Audio Input and Output Ports
- Master and Slave Modes for Both Input and Output
- Bypass Mode
- Time Division Multiplexing (TDM) Mode
- Attenuates Clock Jitter
- Multiple Part Outputs are Phase Matched
- Linear Phase FIR Filter
- Automatic Soft Mute/Unmute
- +2.5 V Digital Supply (VD)
- +3.3 V or 5.0 V Digital Interface (VL)
- Space Saving 20-pin TSSOP and QFN Packages



Preliminary Product Information

This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

General Description

The CS8421 is a 32-bit, high performance, monolithic CMOS stereo asynchronous sample rate converter.

Digital audio inputs and outputs can be 32, 24, 20, or 16-bits. Input and output data can be completely asynchronous, synchronous to an external data clock, or the part can operate without any external clock by using an integrated oscillator.

Audio data is input and output through configurable 3-wire input/output ports. The CS8421 does not require any software control via a control port.

Target applications include digital recording systems (DVD-R/RW, CD-R/RW, PVR, DAT, MD, and VTR), digital mixing consoles, high quality D/A, effects processors, computer audio systems, and automotive audio systems.

The part is available in space saving 20-pin TSSOP and QFN packages and supports sample rates up to 211 kHz.

ORDERING INFORMATION

Product	Description	Package	Pb-Free	Temp Range	Container	Order#
CS8421	32-bit Asynchronous Sample Rate Converter	TSSOP	YES	-10° to +70°C	Rail	CS8421-CZZ
CS8421	32-bit Asynchronous Sample Rate Converter	TSSOP	YES	-10° to +70°C	Tape and Reel	CS8421-CZZR
CS8421	32-bit Asynchronous Sample Rate Converter	QFN	YES	-10° to +70°C	Rail	CS8421-CNZ
CS8421	32-bit Asynchronous Sample Rate Converter	QFN	YES	-10° to +70°C	Tape and Reel	CS8421-CNZR
CS8421	32-bit Asynchronous Sample Rate Converter	TSSOP	YES	-40° to +85°C	Rail	CS8421-DZZ
CS8421	32-bit Asynchronous Sample Rate Converter	TSSOP	YES	-40° to +85°C	Tape and Reel	CS8421-DZZR
CDB8421	Evaluation Board for CS8421	-	-	-	-	CDB8421

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1. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and $T_A = 25^\circ\text{C}$.)

SPECIFIED OPERATING CONDITIONS (GND = 0 V, all voltages with respect to 0 V)

Parameter	Symbol	Min	Nominal	Max	Units	
Power Supply Voltage	VD	2.38	2.5	2.62	V	
	VL	3.14	3.3 or 5.0	5.25	V	
Ambient Operating Temperature:	'-CZ'	T_A	-10	-	+70	$^\circ\text{C}$
	'-CNZ'		-10	-	+70	$^\circ\text{C}$
	'-DZ'		-40	-	+85	$^\circ\text{C}$

ABSOLUTE MAXIMUM RATINGS (GND = 0 V; all voltages with respect to 0 V. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	VD	-0.3	3.5	V
	VL	-0.3	6.0	V
Input Current, Any Pin Except Supplies (Note 1)	I_{in}	-	± 10	mA
Input Voltage	V_{in}	-0.3	VL+0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	+125	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65	+150	$^\circ\text{C}$

- Notes:
1. Transient currents of up to 100 mA will not cause SCR latch-up.
 2. Numbers separated by a colon indicate input and output sample rates. For example, 48 kHz:96 kHz indicates that $F_{si} = 48 \text{ kHz}$ and $F_{so} = 96 \text{ kHz}$.

PERFORMANCE SPECIFICATIONS (XTI/XTO = 27 MHz; Input signal = 1.000 kHz, 0 dBFS, Measurement Bandwidth = 20 to Fso/2 Hz, and Word Width = 32-Bits, unless otherwise stated.)

Parameter		Min	Typ	Max	Units
Resolution		16	-	32	bits
Sample Rate with XTI = 27.000 MHz	Slave	7.2	-	207	kHz
	Master	53	-	211	kHz
Sample Rate with other XTI clocks	Slave	XTI/3750	-	XTI/130	kHz
	Master	XTI/512	-	XTI/128	kHz
Sample Rate with ring oscillator (XTI to GND or VL, XTO floating)		12	-	96	kHz
Sample Rate Ratio - Upsampling		-	-	1:8	
Sample Rate Ratio - Downsampling		-	-	7.5:1	
Interchannel Gain Mismatch		-	0.0	-	dB
Interchannel Phase Deviation		-	0.0	-	Degrees
Peak Idle Channel Noise Component (32-bit operation)		-	-	-192	dBFS
Dynamic Range (20 Hz to Fso/2, 1 kHz, -60 dBFS Input)					
44.1 kHz:48 kHz	A-Weighted	-	180	-	dB
	Unweighted	-	177	-	dB
44.1 kHz:192 kHz	A-Weighted	-	175	-	dB
	Unweighted	-	172	-	dB
48 kHz:44.1 kHz	A-Weighted	-	180	-	dB
	Unweighted	-	177	-	dB
48 kHz:96 kHz	A-Weighted	-	179	-	dB
	Unweighted	-	176	-	dB
96 kHz:48 kHz	A-Weighted	-	176	-	dB
	Unweighted	-	173	-	dB
192 kHz:32 kHz	A-Weighted	-	175	-	dB
	Unweighted	-	172	-	dB
Total Harmonic Distortion + Noise (20 Hz to Fso/2, 1 kHz, 0 dBFS Input)					
32 kHz:48 kHz		-	-161	-	dB
44.1 kHz:48 kHz		-	-171	-	dB
44.1 kHz:192 kHz		-	-130	-	dB
48 kHz:44.1 kHz		-	-160	-	dB
48 kHz:96 kHz		-	-148	-	dB
96 kHz:48 kHz		-	-168	-	dB
192 kHz:32 kHz		-	-173	-	dB

DIGITAL FILTER CHARACTERISTICS

Parameter	Min	Typ	Max	Units
Passband (Upsampling or Downsampling)	-	-	0.4535*Fso	Hz
Passband Ripple	-	-	±0.007	dB
Stopband	0.5465*Fso	-	-	Hz
Stopband Attenuation	125	-	-	dB
Group Delay	(Note 3)			ms

Notes: 3. The equation for the group delay through the sample rate converter is $(56.581 / F_{si}) + (55.658 / F_{so})$. For example, if the input sample rate is 192 kHz and the output sample rate is 96 kHz, the group delay through the sample rate converter is $(56.581/192,000) + (55.658/96,000) = .875$ milliseconds.

DC ELECTRICAL CHARACTERISTICS (GND = 0 V; all voltages with respect to 0 V.)

Parameters	Symbol	Min	Typ	Max	Units
Power-down Mode (Note 4)					
Supply Current in power down (Oscillator attached to XTI-XTO)	VD	-	50	-	μA
	VL = 3.3 V	-	100	-	μA
	VL = 5.0 V	-	200	-	μA
Supply Current in power down (Crystal attached to XTI-XTO)	VD	-	99.9	-	μA
	VL = 3.3 V	-	1.34	-	mA
	VL = 5.0 V	-	3.54	-	mA
Normal Operation (Note 5)					
Supply Current at 48 kHz F _{si} and F _{so} (Oscillator attached to XTI-XTO)	VD	-	23.1	-	mA
	VL = 3.3 V	-	2.17	-	mA
	VL = 5.0 V	-	3.42	-	mA
Supply Current at 192 kHz F _{si} and F _{so} (Oscillator attached to XTI-XTO)	VD	-	78.7	-	mA
	VL = 3.3 V	-	7.7	-	mA
	VL = 5.0 V	-	12.49	-	mA
Supply Current at 48 kHz F _{si} and F _{so} (Crystal attached to XTI-XTO)	VD	-	23.1	-	mA
	VL = 3.3 V	-	2.92	-	mA
	VL = 5.0 V	-	6.02	-	mA
Supply Current at 192 kHz F _{si} and F _{so} (Crystal attached to XTI-XTO)	VD	-	78.7	-	mA
	VL = 3.3 V	-	3.037	-	mA
	VL = 5.0 V	-	6.25	-	mA

- Notes: 4. Power Down Mode is defined as $\overline{RST} = \text{LOW}$ with all clocks and data lines held static, except when a crystal is attached across XTI-XTO, in which case the crystal will begin oscillating.
5. Normal operation is defined as $\overline{RST} = \text{HI}$.

DIGITAL INPUT CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	I _{in}	-	-	±10	μA
Input Capacitance	I _{in}	-	8	-	pF
Input Hysteresis		-	250	-	mV

DIGITAL INTERFACE SPECIFICATIONS (GND = 0 V; all voltages with respect to 0 V.)

Parameters	Symbol	Min	Max	Units
High-Level Output Voltage, except MCLK_OUT and SDOOUT (I _{OH} =-4 mA)	V _{OH}	0.77xVL	-	V
Low-Level Output Voltage, except MCLK_OUT and SDOOUT (I _{OL} =4 mA)	V _{OL}	-	.6	V
High-Level Output Voltage, MCLK_OUT (I _{OH} =-6 mA)	V _{OH}	0.77xVL	-	V
Low-Level Output Voltage, MCLK_OUT (I _{OL} =6 mA)	V _{OL}	-	.6	V
High-Level Output Voltage, SDOOUT (I _{OH} =-8 mA)	V _{OH}	0.77xVL	-	V
Low-Level Output Voltage, SDOOUT (I _{OL} =8 mA)	V _{OL}	-	.6	V
High-Level Input Voltage	V _{IH}	0.55xVL	VL+0.3	V
Low-Level Input Voltage	V _{IL}	-0.3	0.8	V

SWITCHING SPECIFICATIONS

(Inputs: Logic 0 = 0 V, Logic 1 = VL; C_L = 20 pF)

Parameters	Symbol	Min	Max	Units
RST pin Low Pulse Width (Note 6)		1	-	ms
XTI Frequency (Note 7)	Crystal	16.384	27.000	MHz
	Digital Clock Source	1.024	27.000	MHz
XTI Pulse Width High/Low		14.8	-	ns
MCLK_OUT Duty Cycle		45	55	%
Slave Mode				
I/OSCLK Frequency		-	24.576	MHz
OLRCK High Time (Note 8)	t _{lrckh}	326	-	ns
I/OSCLK High Time	t _{sckh}	9	-	ns
I/OSCLK Low Time	t _{sckl}	9	-	ns
I/OLRCK Edge to I/OSCLK Rising	t _{lcks}	6	-	ns
OLRCK Rising Edge to OSCLK Rising Edge (TDM)	t _{fss}	5	-	ns
I/OSCLK Rising Edge to I/OLRCK Edge	t _{lckd}	5	-	ns
OSCLK Rising Edge to OLRCK Falling Edge (TDM)	t _{fsh}	5	-	ns
OSCLK Falling Edge/OLRCK Edge to SDOUT Output Valid	t _{dpd}	-	18	ns
SDIN/TDM_IN Setup Time Before I/OSCLK Rising Edge	t _{ds}	3	-	ns
SDIN/TDM_IN Hold Time After I/OSCLK Rising Edge	t _{dh}	5	-	ns

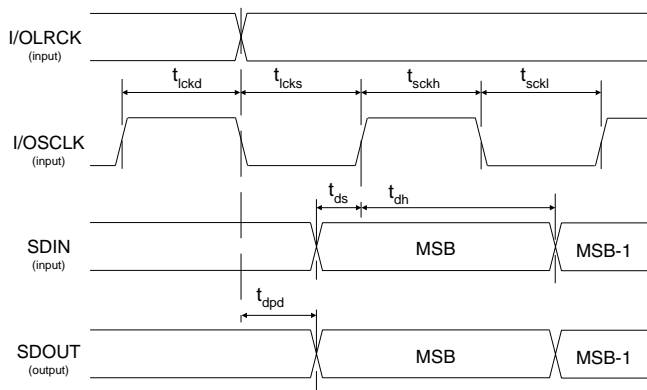


Figure 1. Non-TDM Slave Mode Timing

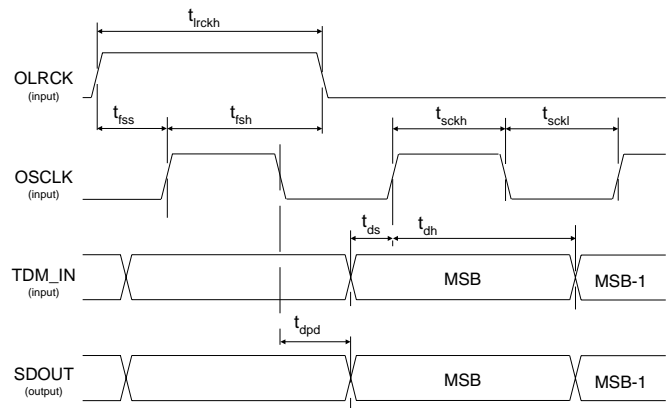
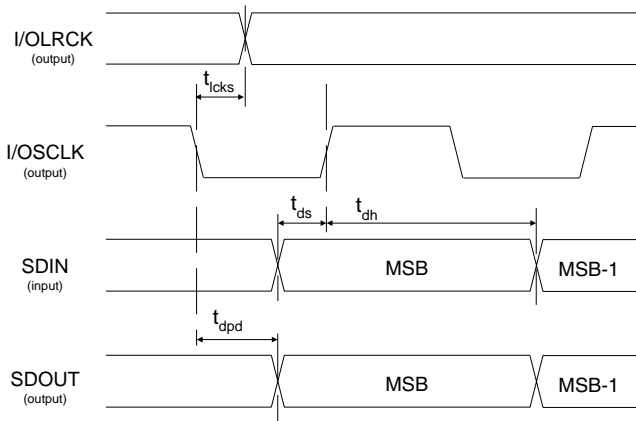
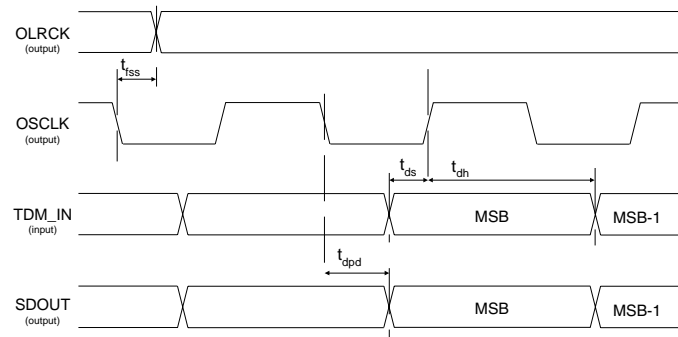


Figure 2. TDM Slave Mode Timing

Parameters	Symbol	Min	Max	Units
Master Mode (Note 9)				
I/OSCLK Frequency (non-TDM)		64*Fsi/o		MHz
OSCLK Frequency (TDM)		256*Fso		MHz
I/OLRCK Duty Cycle		45	55	%
I/OSCLK Duty Cycle		45	55	%
I/OSCLK Falling Edge to I/OLRCK Edge	t_{lcks}	-	5	ns
OSCLK Falling Edge to OLRCK Edge (TDM)	t_{fss}	-	5	ns
OSCLK Falling Edge to SDOUT Output Valid	t_{dpd}	-	7	ns
SDIN/TDM_IN Setup Time Before I/OSCLK Rising Edge	t_{ds}	3	-	ns
SDIN/TDM_IN Hold Time After I/OSCLK Rising Edge	t_{dh}	5	-	ns

- Notes:
- After powering up the CS8421, \overline{RST} should be held low until the power supplies and clocks are settled.
 - The maximum possible sample rate is $XTI/128$.
 - OLRCK must remain high for at least 8 OSCLK periods in TDM mode.
 - Only the input or the output serial port can be set as master at a given time.


Figure 3. Non-TDM Master Mode Timing

Figure 4. TDM Master Mode Timing

2. TYPICAL CONNECTION DIAGRAMS

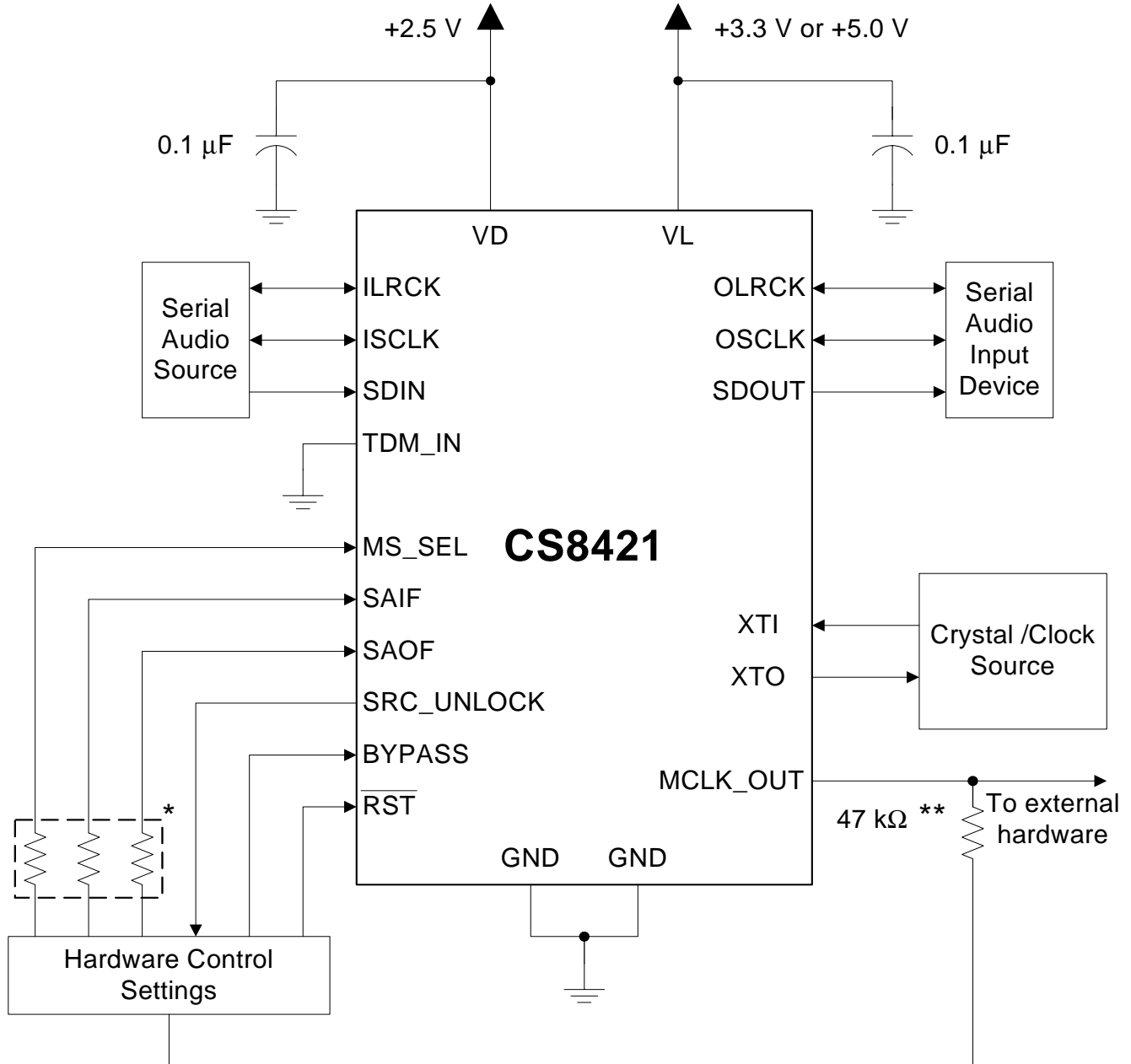


Figure 5. Typical Connection Diagram, Master and Slave Modes

* The connection (VL or GND) and value of these three resistors determines the mode of operation for the input and output serial ports as described in Table 1, "Serial Audio Port Master/Slave and Clock Ratio Select Startup Options (MS_SEL)", Table 2, "Serial Audio Input Port Startup Options (SAIF)", and Table 3, "Serial Audio Output Port Startup Options (SAOF)", all on page 13.

** MCLK_OUT pin should be pulled high through a 47 kΩ resistor if an MCLK output is not needed.

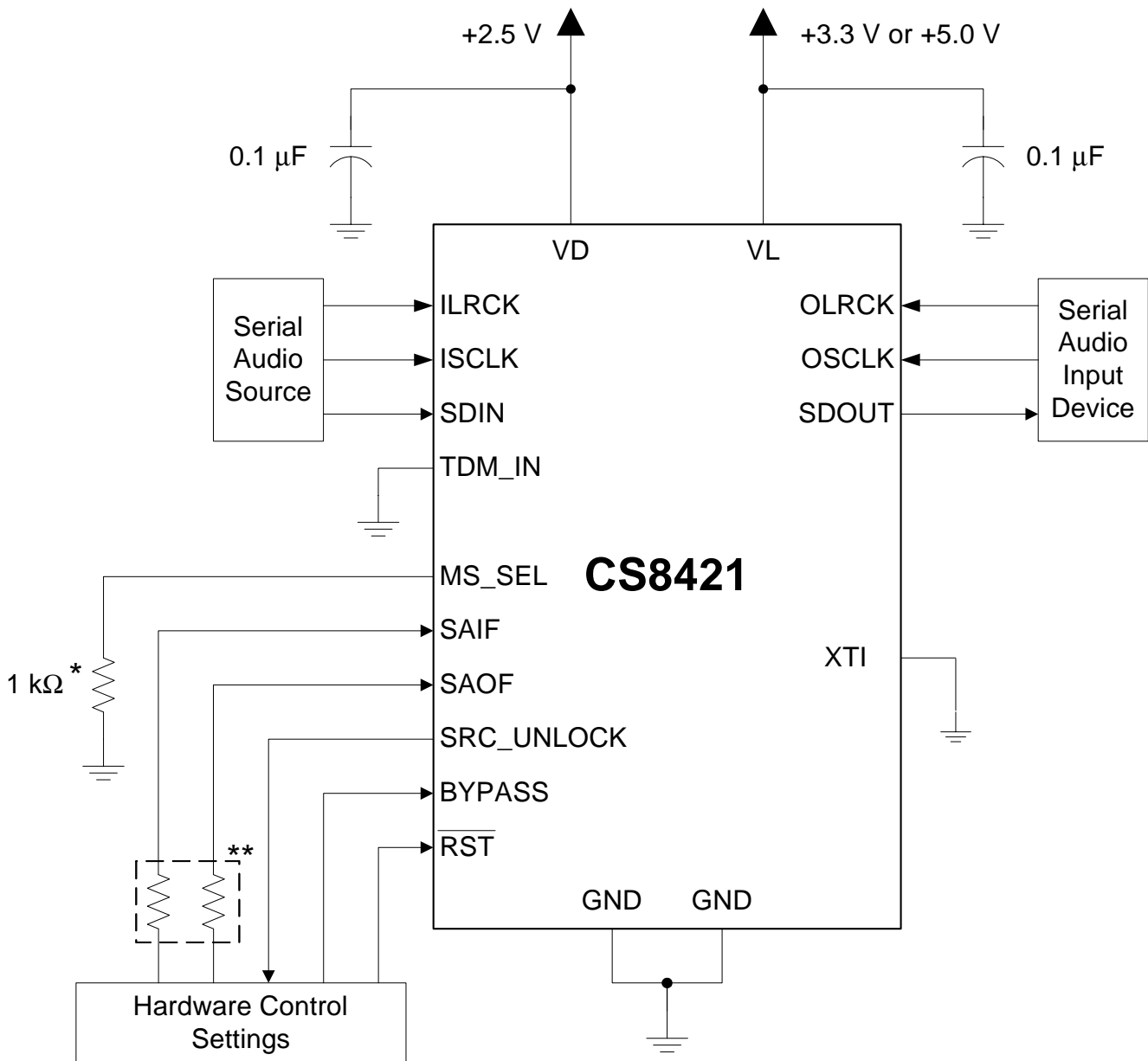


Figure 6. Typical Connection Diagram, No External Master Clock

* When no external master clock is supplied to the part, both input and output must be set to salve mode for the part to operate properly. This is done by connecting the MS_SEL pin to ground through a resistance of 0Ω to $1\text{ k}\Omega \pm 1\%$ as stated in Table 1, "Serial Audio Port Master/Slave and Clock Ratio Select Startup Options (MS_SEL)," on page 13

** The connection (VL or GND) and value of these two resistors determines the mode of operation for the input and output serial ports as described in Table 1, "Serial Audio Port Master/Slave and Clock Ratio Select Startup Options (MS_SEL)", Table 2, "Serial Audio Input Port Startup Options (SAIF)", and Table 3, "Serial Audio Output Port Startup Options (SAOF)", all on page 13.

3. GENERAL DESCRIPTION

The CS8421 is a 32-bit, high performance, monolithic CMOS stereo asynchronous sample rate converter. The digital audio data is input and output through configurable 3-wire serial ports. The digital audio input/output ports offer Left Justified, Right Justified, and I²S serial audio formats. The CS8421 also supports a TDM mode which allows multiple channels of digital audio data on one serial line. A bypass mode allows the data to be passed directly to the output port without sample rate conversion.

The CS8421 does not require a control port interface, helping to speed design time by not requiring the user to develop software to configure the part. Pins that are sensed after reset allow the part to be configured. See “Reset, Power Down, and Start-up” on page 32.

Target applications include digital recording systems (DVD-R/RW, CD-R/RW, PVR, DAT, MD, and VTR), digital mixing consoles, high quality D/A, effects processors and computer audio systems.

Figure 5 and Figure 6 show the supply and external connections to the CS8421.

4. THREE-WIRE SERIAL INPUT/OUTPUT AUDIO PORT

A 3-wire serial audio input/output port is provided. The interface format should be chosen to suit the attached device through the MS_SEL, SAIF, and SAOF pins. Table 1, Table 2, and Table 3 show the pin functions and their corresponding settings. The following parameters are adjustable:

- Master or slave.
- Master clock (MCLK) ratios of $128 \cdot F_{si/o}$, $256 \cdot F_{si/o}$, $384 \cdot F_{si/o}$, and $512 \cdot F_{si/o}$ (Master mode).
- Audio data resolution of 16, 20, 24, or 32-bits.
- Left or right justification of the data relative to left/right clock (LRCK) as well as I²S.

Figure 7, Figure 8, and Figure 9 show the input/output formats available.

In master mode, the left/right clock and the serial bit clock are outputs, derived from the XTI input pin master clock.

In slave mode, the left/right clock and the serial bit clock are inputs and may be asynchronous to the XTI master clock. The left/right clock should be continuous, but the duty cycle can be less than 50% if enough serial clocks are present in each phase to clock all of the data bits.

ISCLK is always set to $64 \cdot F_{si}$ when the input is set to master. In normal operation, OSCLK is set to $64 \cdot F_{so}$. In TDM slave mode, OSCLK must operate at $N \cdot 64 \cdot F_{so}$, where N is the number of CS8421's connected together. In TDM master mode, OSCLK is set to $256 \cdot F_{so}$

5. MODE SELECTION

The CS8421 uses the resistors attached to the MS_SEL, SAIF, and SAOF pins to determine the modes of operation. After reset the resistor value and condition (VL or GND) are sensed. This operation will take approximately 4 μ s to complete. The SRC_UNLOCK pin will remain high and the SDOUT pin will be muted until the mode detection sequence has completed. After this, if all clocks are stable, SRC_UNLOCK will be brought low when audio output is valid and normal operation will occur. Table 1, Table 2, and Table 3 show the pin functions and their corresponding settings. If the 1.0 k Ω option is selected for MS_SEL, SAIF, or SAOF, the resistor connected to that pin may be replaced by a direct connection to VL or GND as appropriate.

The resistor attached to each mode selection pin should be placed physically close to the CS8421. The end of the resistor not connected to the mode selection pins should be connected as close as possible to VL and GND to minimize noise. Table 1, Table 2, and Table 3 show the pin functions and their corresponding settings.

MS_SEL pin	Input M/S	Output M/S
1.0 kΩ ± 1% to GND	Slave	Slave
1.96 kΩ ± 1% to GND	Slave	Master (128 x Fso)
4.02 kΩ ± 1% to GND	Slave	Master (256 x Fso)
8.06 kΩ ± 1% to GND	Slave	Master (384 x Fso)
16.2 kΩ ± 1% to GND	Slave	Master (512 x Fso)
1.0 kΩ ± 1% to VL	Master (128 x Fsi)	Slave
1.96 kΩ ± 1% to VL	Master (256 x Fsi)	Slave
4.02 kΩ ± 1% to VL	Master (384 x Fsi)	Slave
8.06 kΩ ± 1% to VL	Master (512 x Fsi)	Slave

Table 1. Serial Audio Port Master/Slave and Clock Ratio Select Startup Options (MS_SEL)

SAIF pin	Input Port Configuration
1.0 kΩ ± 1% to GND	I ² S up to 32-bit data
1.96 kΩ ± 1% to GND	Left Justified up to 32-bit data
4.02 kΩ ± 1% to GND	Right Justified 16-bit data
1.0 kΩ ± 1% to VL	Right Justified 20-bit data
1.96 kΩ ± 1% to VL	Right Justified 24-bit data
4.02 kΩ ± 1% to VL	Right Justified 32-bit data

Table 2. Serial Audio Input Port Startup Options (SAIF)

SAOF pin	Output Port Configuration
1.0 kΩ ± 1% to GND	I ² S 16-bit data
1.96 kΩ ± 1% to GND	I ² S 20-bit data
4.02 kΩ ± 1% to GND	I ² S 24-bit data
8.06 kΩ ± 1% to GND	I ² S 32-bit data
16.2 kΩ ± 1% to GND	Left Justified 16-bit data
32.4 kΩ ± 1% to GND	Left Justified 20-bit data
63.4 kΩ ± 1% to GND	Left Justified 24-bit data
127.0 kΩ ± 1% to GND	Left Justified 32-bit data
1.0 kΩ ± 1% to VL	Right Justified 16-bit data
1.96 kΩ ± 1% to VL	Right Justified 20-bit data
4.02 kΩ ± 1% to VL	Right Justified 24-bit data
8.06 kΩ ± 1% to VL	Right Justified 32-bit data
16.2 kΩ ± 1% to VL	TDM Mode 16-bit data
32.4 kΩ ± 1% to VL	TDM Mode 20-bit data
63.4 kΩ ± 1% to VL	TDM Mode 24-bit data
127.0 kΩ ± 1% to VL	TDM Mode 32-bit data

Table 3. Serial Audio Output Port Startup Options (SAOF)

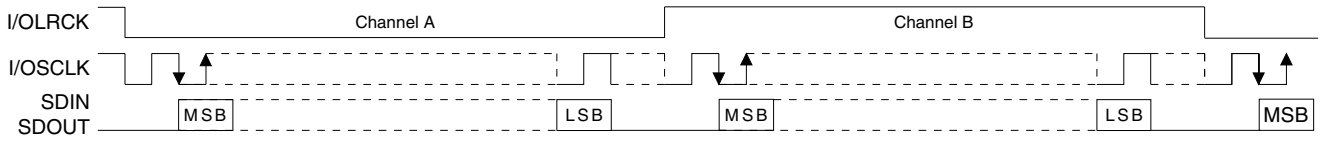


Figure 7. Serial Audio Interface Format - I²S

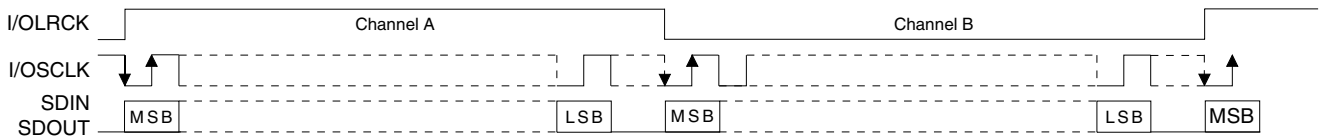


Figure 8. Serial Audio Interface Format - Left Justified

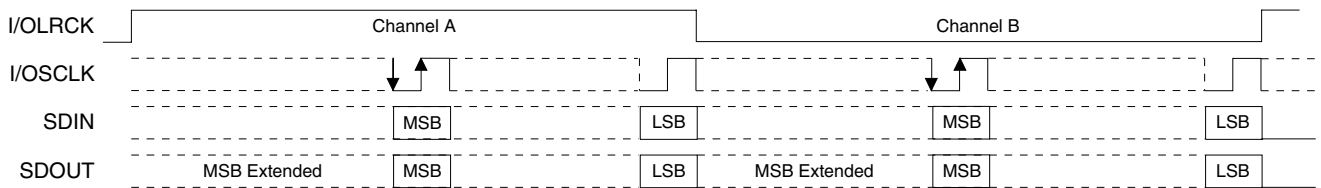


Figure 9. Serial Audio Interface Format - Right Justified

6. SAMPLE RATE CONVERTER (SRC)

Multirate digital signal processing techniques are used to conceptually upsample the incoming data to a very high rate and then downsample to the outgoing rate. The internal data path is 32-bits wide even if a lower bit depth is selected at the output. The filtering is designed so that a full input audio bandwidth of 20 kHz is preserved if the input sample and output sample rates are greater than or equal to 44.1 kHz. When the output sample rate becomes less than the input sample rate, the input is automatically band limited to avoid aliasing products in the output. Careful design ensures minimum ripple and distortion products are added to the incoming signal. The SRC also determines the ratio between the incoming and outgoing sample rates, and sets the filter corner frequencies appropriately. Any jitter in the incoming signal has little impact on the dynamic performance of the rate converter and has no influence on the output clock.

6.1 Clocking

In order to ensure proper operation of the CS8421, the clock or crystal attached to XTI must simultaneously satisfy the requirements of LRCK for both the input and output as follows:

- If the input is set to master, $F_{si} \leq XTI/128$ and $F_{so} \leq XTI/130$.
- If the output is set to master, $F_{so} \leq XTI/128$ and $F_{si} \leq XTI/130$.
- If both input and output are set to slave, $XTI \geq 130 * [\text{minimum}(F_{si}, F_{so})]$, $XTI/F_{si} < 3750$, and $XTI/F_{so} < 3750$.

6.2 Data Resolution and Dither

When using the serial audio input port in left justified and I²S modes all input data is treated as 32-bits wide. Any truncation that has been done prior to the CS8421 to less than 32-bits should have been done using an appropriate dithering process. If the serial audio input port is in right justified mode, the input data will be truncated to the bit depth set by SAIF pin setting. If the SAIF bit depth is set to 16, 20, or 24-bits, and the input data is 32-bits wide, then truncation distortion will occur. Similarly, in any serial audio input port mode, if an inadequate number of bit clocks are entered (i.e. 16 clocks instead of 20 clocks), then the input words will be truncated, causing truncation distortion at low levels. In summary, there is no dithering mechanism on the input side of the CS8421, and care must be taken to ensure that no truncation occurs. Dithering is used internally where appropriate inside the SRC block.

The output side of the SRC can be set to 16, 20, 24, or 32-bits. Dithering is applied and is automatically scaled to the selected output word length. This dither is not correlated between left and right channels.

6.3 SRC Locking and Varispeed

The SRC calculates the ratio between the input sample rate and the output sample rate, and uses this information to set up various parameters inside the SRC block. The SRC takes some time to make this calculation, approximately $4200/F_{so}$ (8.75 ms at F_{so} of 48 kHz).

If F_{si} is changing, as in a varispeed application, the SRC will track the incoming sample rate. During this tracking mode, the SRC will still rate convert the audio data, but at increased distortion levels. Once the incoming sample rate is stable the SRC will return to normal levels of audio quality. The data buffer in the SRC can overflow if the input sample rate changes at greater than 10%/sec.

The SRC_UNLOCK pin is used to indicate when the SRC is not locked. When \overline{RST} is asserted, or if there is a change in F_{si} or F_{so} , SRC_UNLOCK will be set high. The SRC_UNLOCK pin will continue to be high until the SRC has reacquired lock and settled, at which point it will transition low. When the SRC_UNLOCK pin is set low, SDOUT is outputting valid audio data. This can be used to signal a DAC to unmute its output.

6.4 Bypass Mode

When the BYPASS pin is set high, the input data bypasses the sample rate converter and is sent directly to the serial audio output port. No dithering is performed on the output data. This mode is ideal for passing non-audio data through without a sample rate conversion. ILRCK and OLRCK should be the same sample rate and synchronous in this mode.

6.5 Muting

The SDOUT pin is set to all zero output (full mute) immediately after the $\overline{\text{RST}}$ pin is set high. When the output from the SRC becomes valid, though the SRC may not have reached full performance, SDOUT is unmuted over a period of approximately 4096 OLRCK cycles (soft unmuted). When the output becomes invalid, depending on the condition, SDOUT is either immediately set to all zero output (hard muted) or SDOUT is muted over a period of approximately 4096 OLRCK cycles until it reaches full mute (soft muted). The SRC will soft mute SDOUT if there is an illegal ratio between ILRCK and the XTI master clock. Conditions that will cause the SRC to hard mute SDOUT include removing OLRCK, the $\overline{\text{RST}}$ pin being set low, or illegal ratios between OLRCK and the XTI master clock. After all invalid states have been cleared, the SRC will soft unmute SDOUT.

6.6 Group Delay and Phase Matching Between Multiple CS8421 Parts

The equation for the group delay through the sample rate converter is shown in “Digital Filter Characteristics” on page 6. This phase delay is equal across multiple parts. Therefore, when multiple parts operate at the same Fsi and Fso and use a common XTI/XTO clock, their output data is phase matched.

6.7 Master Clock

The CS8421 uses the clock signal supplied through XTI as its master clock (MCLK). MCLK can be supplied from a digital clock source, a crystal oscillator, or a fundamental mode crystal. Figure 10 shows the typical connection diagram for using a fundamental mode crystal. Please refer to the crystal manufacturer's specifications for the external capacitor recommendations. If XTO is not used, such as with a digital clock source or crystal oscillator, XTO should be left unconnected or pulled low through a 47 k Ω resistor to GND.

If either serial audio port is set as master, MCLK will be used to supply the sub-clocks to the master SCLK and LRCK. In this case MCLK will be synchronous to the master serial audio port. If both serial audio ports are set as slave, MCLK can be asynchronous to either or both ports. If the user needs to change the clock source to XTI while the CS8421 is still powered on and running, a RESET must be issued once the XTI clock source is present and valid to ensure proper operation.

When both serial ports are configured as slave and operating at sample rates less than 96 kHz, the CS8421 has the ability to operate without a master clock input through XTI. This benefits the design by not requiring extra external clock components (lowering production cost) and not requiring a master clock to be routed to the CS8421, resulting in lowered noise contribution in the system. In this mode, an internal oscillator provides the clock to run all of the internal logic. To enable the internal oscillator simply tie XTI to GND or VL. In this mode, XTO should be left unconnected.

The CS8421 can also provide a buffered MCLK output through the MCLK_OUT pin. This pin can be used to supply MCLK to other system components that operate synchronously to MCLK. If MCLK_OUT is not needed, the output of the pin can be disabled by pulling the pin high through a 47 k Ω resistor to VL. MCLK_OUT is also disabled when using the internal oscillator mode. The MCLK_OUT pin will be set low when disabled by using the internal oscillator mode.

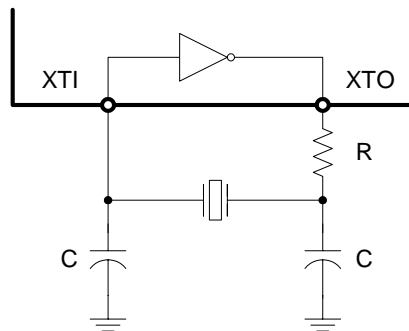


Figure 10. Typical Connection Diagram for Crystal Circuit

6.8 Time Division Multiplexing (TDM) Mode

TDM mode allows several CS8421 to be serially connected together allowing their corresponding SDOUT data to be multiplexed onto one line for input into a DSP or other TDM capable multichannel device.

The CS8421 can operate in two TDM modes. The first mode consists of all of the CS8421's output ports set to slave as shown in Figure 13. The second mode consists of one CS8421 output port set to master and the remaining CS8421's output ports set to slave as shown in Figure 14.

The TDM_IN pin is used to input the data while the SDOUT pin is used to output the data. The first CS8421 in the chain should have its TDM_IN set to GND. Data is transmitted from SDOUT most significant bit first on the first OSCLK after an OLRCK transition and is valid on the rising edge of OSCLK.

In TDM slave mode, the number of channels that can be multiplexed to one serial data line depends on the output sampling rate. For slave mode, OSCLK must operate at $N \cdot 64 \cdot F_{so}$, where N is the number of CS8421's connected together. The maximum allowable OSCLK frequency is 24.576 MHz, so for $F_{so} = 48$ kHz, $N = 8$ (16 channels of serial audio data).

In TDM master mode, OSCLK operates at $256 \cdot F_{so}$, which is equivalent to $N = 4$, so a maximum of 8 channels of digital audio can be multiplexed together. Note that for TDM master mode, MCLK must be at least $256 \cdot F_{so}$, where $F_{so} \leq 96$ kHz. OLRCK identifies the start of a new frame. Each time slot is 32-bits wide, with the valid data sample left justified within the time slot. Valid data lengths are 16, 20, 24 or 32-bits. Figure 11 and Figure 12 show the interface format for master and slave TDM modes.

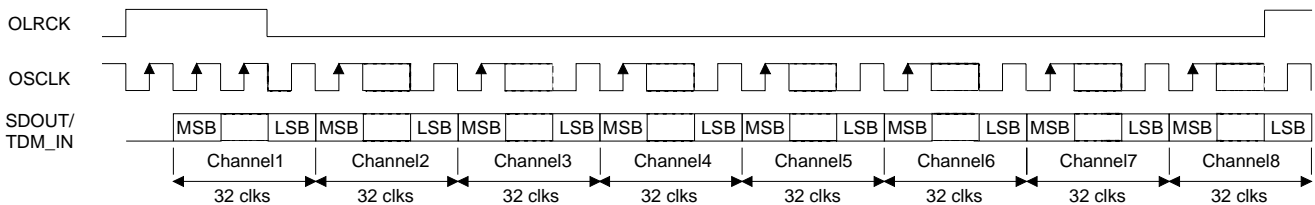


Figure 11. TDM Slave Mode Timing Diagram

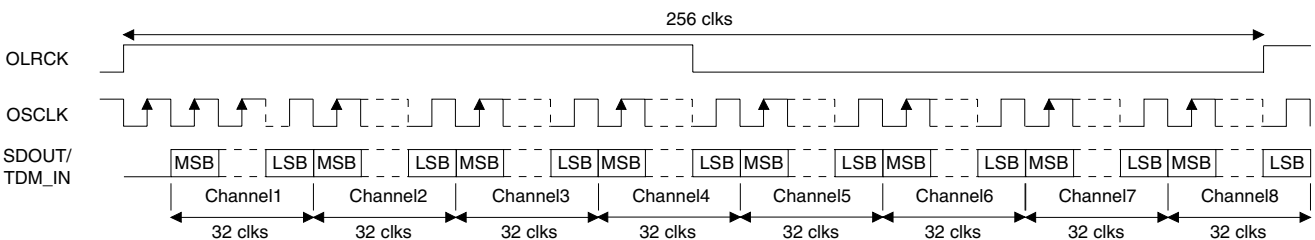


Figure 12. TDM Master Mode Timing Diagram

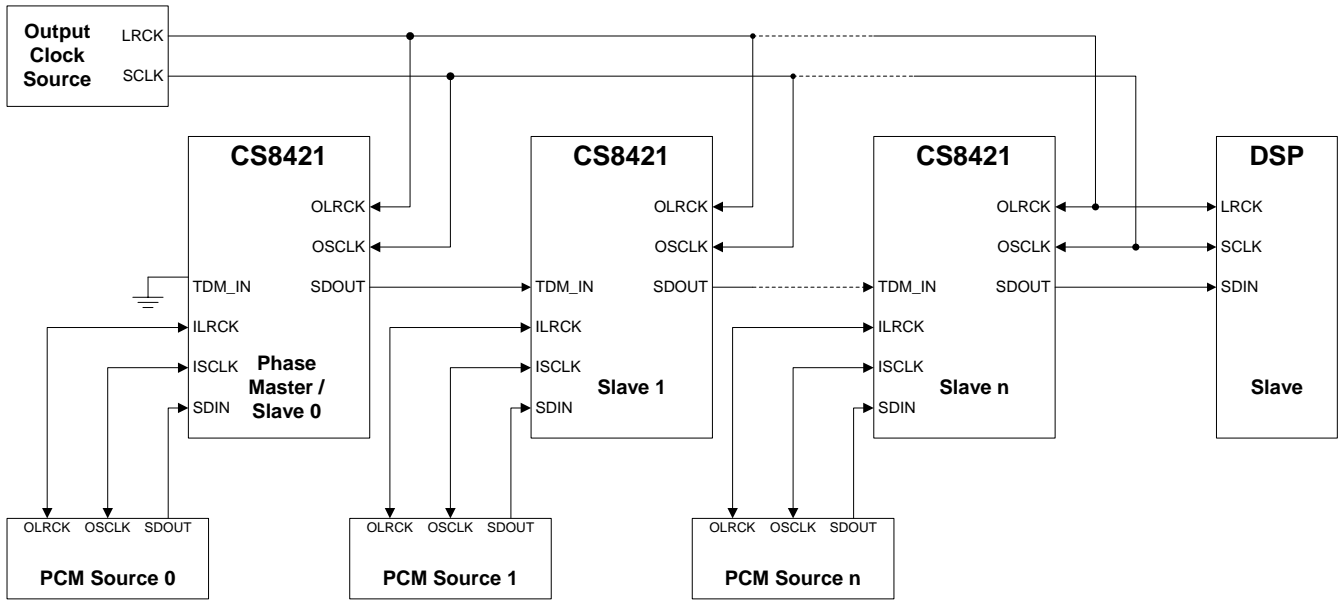


Figure 13. TDM Mode Configuration (All CS8421 outputs are slave)

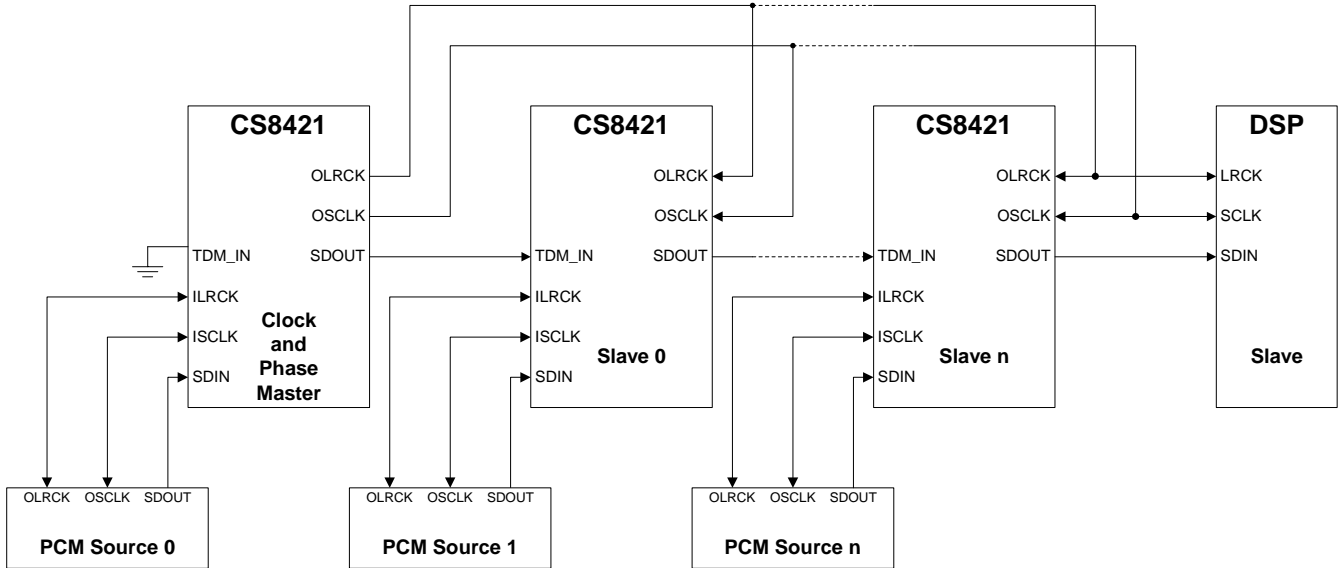
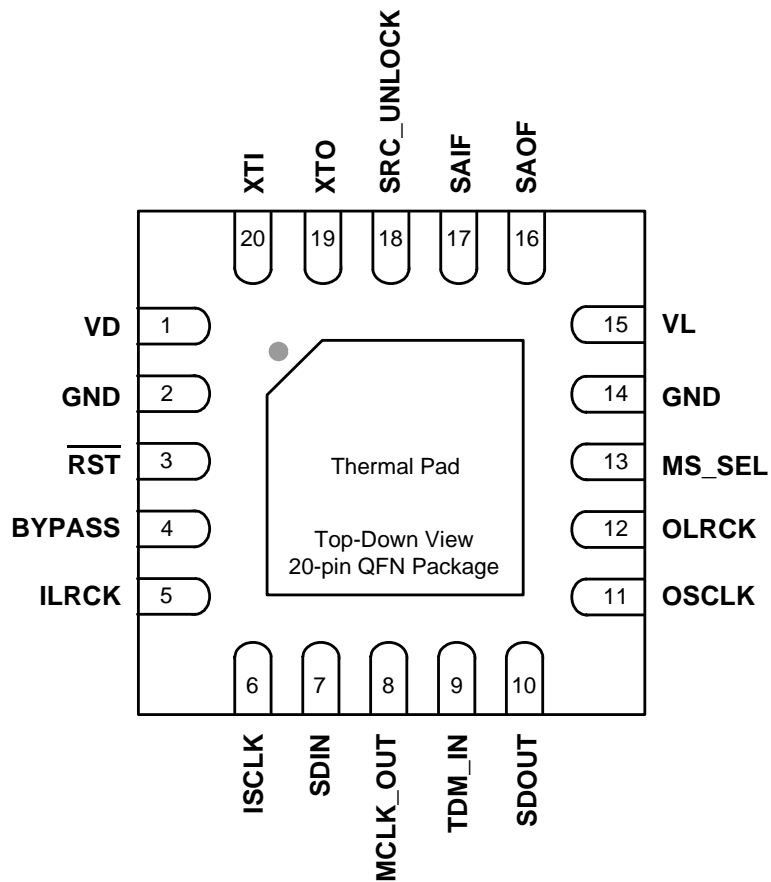
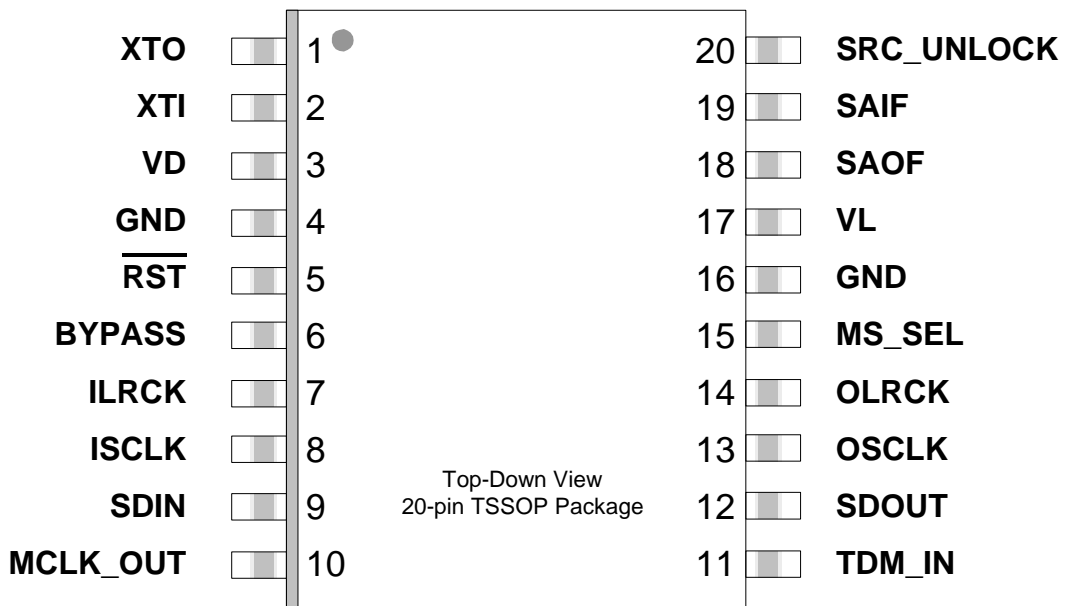


Figure 14. TDM Mode Configuration (First CS8421 output is master, all others are slave)

7. PIN DESCRIPTIONS


7.1 TSSOP PIN DESCRIPTIONS

	PIN	
XTO	1	Crystal Out (Output) - Crystal output for Master clock. See “Master Clock” on page 17.
XTI	2	Crystal/Oscillator In (Input) - Crystal or digital clock input for Master clock. See “Master Clock” on page 17.
VD	3	Digital Power (Input) - Digital core power supply. Typically +2.5 V.
GND	4	Ground (Input) - Ground for I/O and core logic.
$\overline{\text{RST}}$	5	Reset (Input) - When $\overline{\text{RST}}$ is low the CS8421 enters a low power mode and all internal states are reset. On initial power up $\overline{\text{RST}}$ must be held low until the power supply is stable and all input clocks are stable in frequency and phase.
BYPASS	6	Sample Rate Converter Bypass (Input) - When BYPASS is high, the sample rate converter will be bypassed and any data input through the serial audio input port will be directly output on the serial audio output port. When Bypass is low the sample rate converter will operate normally.
ILRCK	7	Serial Audio Input Left/Right Clock (Input/Output) - Word rate clock for the audio data on the SDIN pin.
ISCLK	8	Serial Audio Bit Clock (Input/Output) - Serial bit clock for audio data on the SDIN pin.
SDIN	9	Serial Audio Input Data Port (Input) - Audio data serial input pin.
MCLK_OUT	10	Master Clock Output (Output) - Buffered and level shifted output for Master clock. If MCLK_OUT is not required, this pin should be pulled high through a 47 k Ω resistor to turn the output off. See “Master Clock” on page 17.
TDM_IN	11	Serial Audio TDM Input (Input) - Time Division Multiplexing serial audio data input. Grounded when not used. See “Time Division Multiplexing (TDM) Mode” on page 18
SDOUT	12	Serial Audio Output Data Port (Output) - Audio data serial output pin. Optionally this pin may be pulled low through a 47 k Ω resistor, but should not be pulled high.
OSCLK	13	Serial Audio Bit Clock (Input/Output) - Serial bit clock for audio data on the SDOUT pin.
OLRCK	14	Serial Audio Input Left/Right Clock (Input/Output) - Word rate clock for the audio data on the SDOUT pin.
MS_SEL	15	Master/Slave Select (Input) - Used to select Master or Slave for the input and output serial audio ports at startup and reset. See Table 1 on page 13 for format settings.
GND	16	Ground (Input) - Ground for I/O and core logic.
VL	17	Logic Power (Input) - Input/Output power supply. Typically +3.3 V or +5.0 V.
SAOF	18	Serial Audio Output Format Select (Input) - Used to select the serial audio output format at startup and reset. See Table 3 on page 13 for format settings.
SAIF	19	Serial Audio Input Format Select (Input) - Used to select the serial audio input format at startup and reset. See Table 2 on page 13 for format settings.
SRC_UNLOCK	20	SRC Unlock Indicator (Output) - Indicates when the SRC is unlocked. See “SRC Locking and Varispeed” on page 15.

Table 4. TSSOP Pin Descriptions

7.2 QFN PIN DESCRIPTIONS

	PIN	
VD	1	Digital Power (Input) - Digital core power supply. Typically +2.5 V.
GND	2	Ground (Input) - Ground for I/O and core logic.
RST	3	Reset (Input) - When $\overline{\text{RST}}$ is low the CS8421 enters a low power mode and all internal states are reset. On initial power up $\overline{\text{RST}}$ must be held low until the power supply is stable and all input clocks are stable in frequency and phase.
BYPASS	4	Sample Rate Converter Bypass (Input) - When BYPASS is high, the sample rate converter will be bypassed and any data input through the serial audio input port will be directly output on the serial audio output port. When Bypass is low the sample rate converter will operate normally.
ILRCK	5	Serial Audio Input Left/Right Clock (Input/Output) - Word rate clock for the audio data on the SDIN pin.
ISCLK	6	Serial Audio Bit Clock (Input/Output) - Serial bit clock for audio data on the SDIN pin.
SDIN	7	Serial Audio Input Data Port (Input) - Audio data serial input pin.
MCLK_OUT	8	Master Clock Output (Output) - Buffered and level shifted output for Master clock. If MCLK_OUT is not required, this pin should be pulled high through a 47 k Ω resistor to turn the output off. See "Master Clock" on page 17.
TDM_IN	9	Serial Audio TDM Input (Input) - Time Division Multiplexing serial audio data input. Grounded when not used. See "Time Division Multiplexing (TDM) Mode" on page 18
SDOUT	10	Serial Audio Output Data Port (Output) - Audio data serial output pin. Optionally this pin may be pulled low through a 47 k Ω resistor, but should not be pulled high.
OSCLK	11	Serial Audio Bit Clock (Input/Output) - Serial bit clock for audio data on the SDOUT pin.
OLRCK	12	Serial Audio Input Left/Right Clock (Input/Output) - Word rate clock for the audio data on the SDOUT pin.
MS_SEL	13	Master/Slave Select (Input) - Used to select Master or Slave for the input and output serial audio ports at startup and reset. See Table 1 on page 13 for format settings.
GND	14	Ground (Input) - Ground for I/O and core logic.
VL	15	Logic Power (Input) - Input/Output power supply. Typically +3.3 V or +5.0 V.
SAOF	16	Serial Audio Output Format Select (Input) - Used to select the serial audio output format at startup and reset. See Table 3 on page 13 for format settings.
SAIF	17	Serial Audio Input Format Select (Input) - Used to select the serial audio input format at startup and reset. See Table 2 on page 13 for format settings.
SRC_UNLOCK	18	SRC Unlock Indicator (Output) - Indicates when the SRC is unlocked. See "SRC Locking and Varispeed" on page 15.
XTO	19	Crystal Out (Output) - Crystal output for Master clock. See "Master Clock" on page 17.
XTI	20	Crystal/Oscillator In (Input) - Crystal or digital clock input for Master clock. See "Master Clock" on page 17.
THERMAL PAD	-	Thermal Pad - Thermal relief pad for optimized heat dissipation.

Table 5. QFN Pin Descriptions

8. PERFORMANCE PLOTS

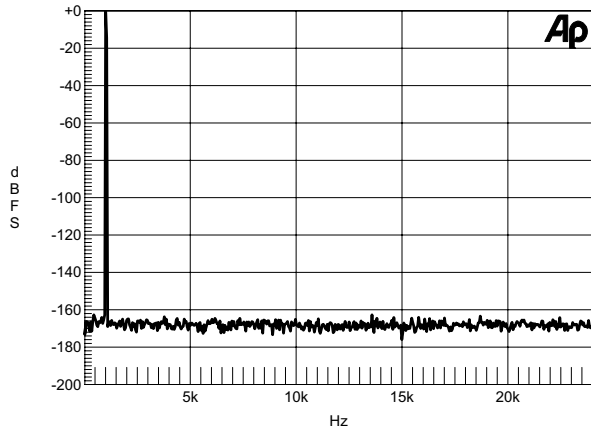


Figure 15a. Wideband FFT Plot (16k Points) 0 dBFS 1 kHz Tone, 48 kHz:48 kHz

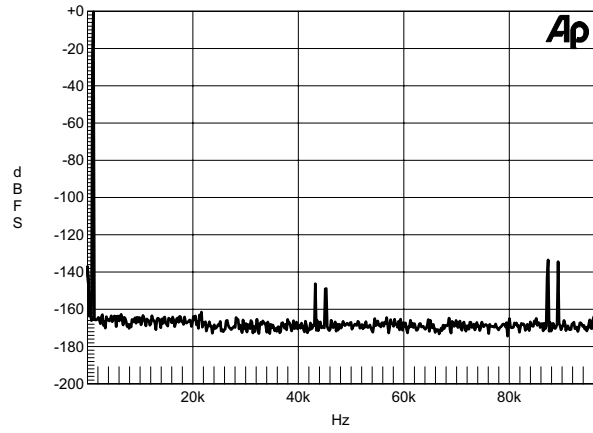


Figure 15b. Wideband FFT Plot (16k Points) 0 dBFS 1 kHz Tone, 44.1 kHz:192 kHz

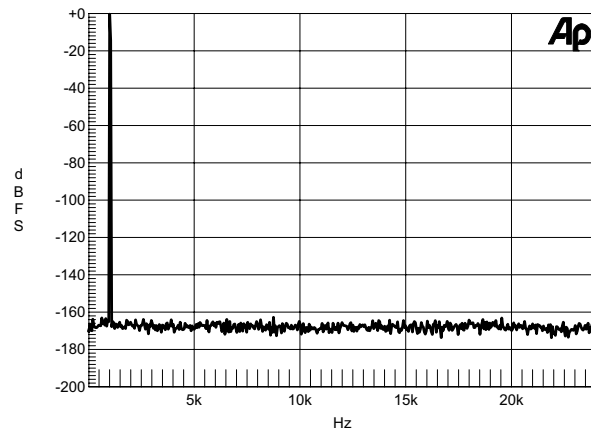


Figure 16a. Wideband FFT Plot (16k Points) 0 dBFS 1 kHz Tone, 44.1 kHz:48 kHz

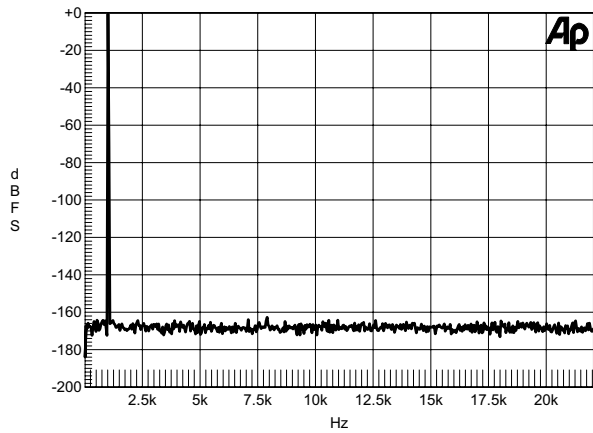


Figure 16b. Wideband FFT Plot (16k Points) 0 dBFS 1 kHz Tone, 48 kHz:44.1 kHz

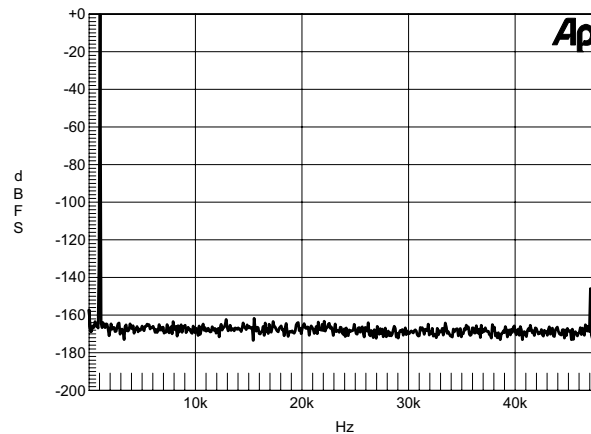


Figure 17a. Wideband FFT Plot (1Fsi6k Points) 0 dBFS 1 kHz Tone, 48 kHz:96 kHz

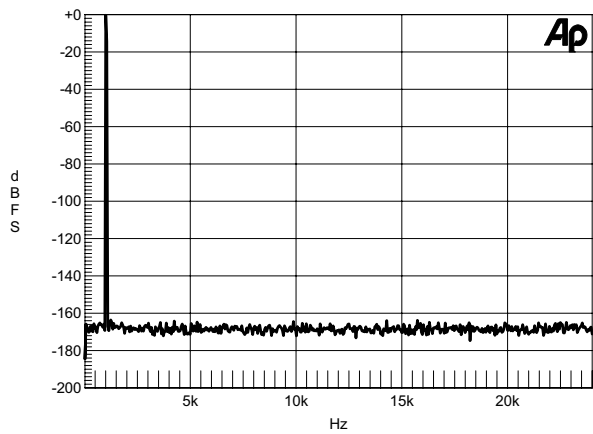


Figure 17b. Wideband FFT Plot (16k Points) 0 dBFS 1 kHz Tone, 96 kHz:48 kHz

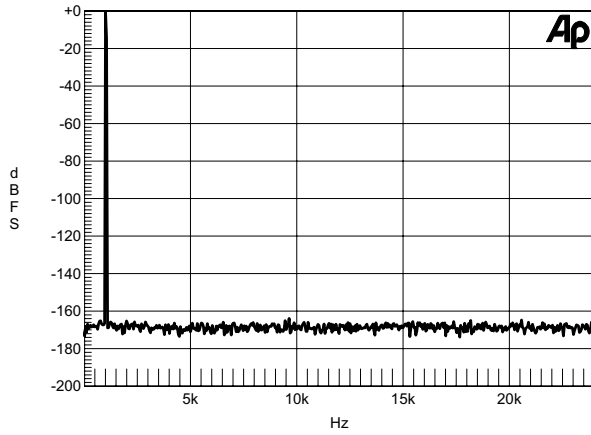


Figure 18a. Wideband FFT Plot (16k Points) 0 dBFS 1 kHz Tone, 192 kHz:48 kHz

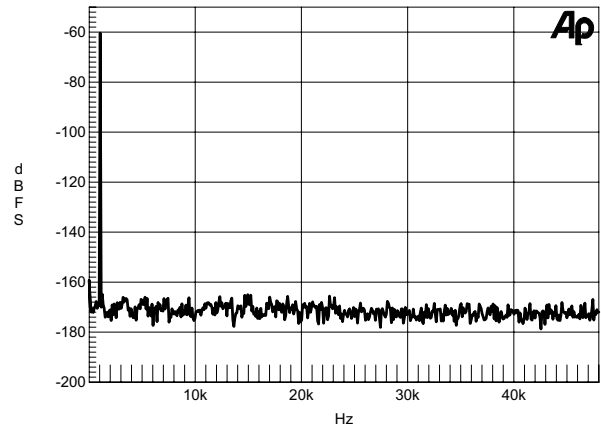


Figure 18b. Wideband FFT Plot (16k Points) -60 dBFS 1 kHz Tone, 48 kHz:96 kHz

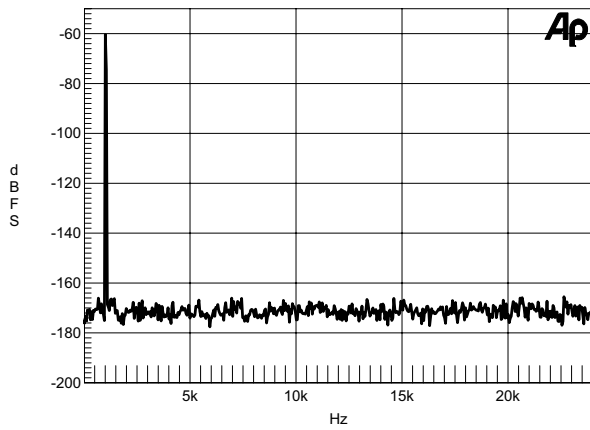


Figure 19a. Wideband FFT Plot (16k Points) -60 dBFS 1 kHz Tone, 48 kHz:48 kHz

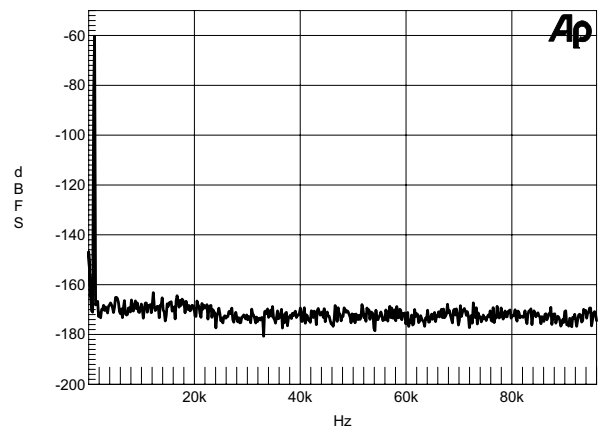


Figure 19b. Wideband FFT Plot (16k Points) -60 dBFS 1 kHz Tone, 44.1 kHz:192 kHz

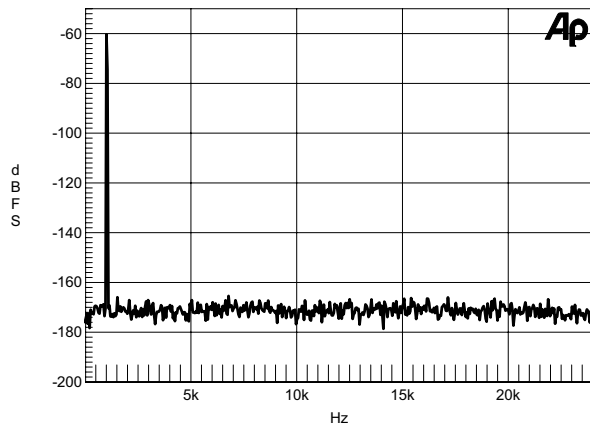


Figure 20a. Wideband FFT Plot (16k Points) -60 dBFS 1 kHz Tone, 44.1 kHz:48 kHz

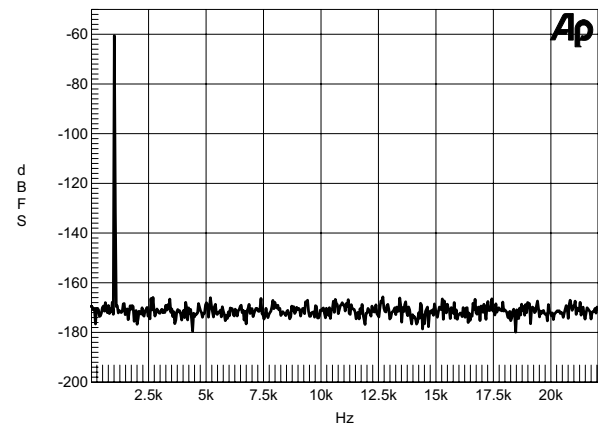


Figure 20b. Wideband FFT Plot (16k Points) -60 dBFS 1 kHz Tone, 48 kHz:44.1 kHz

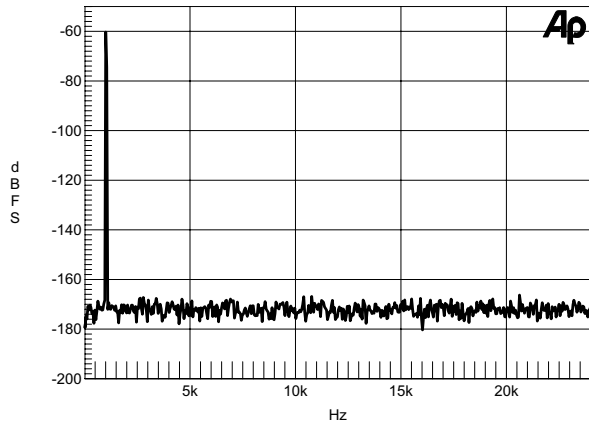


Figure 21b. Wideband FFT Plot (16k Points) -60 dBFS 1 kHz Tone, 96 kHz:48 kHz

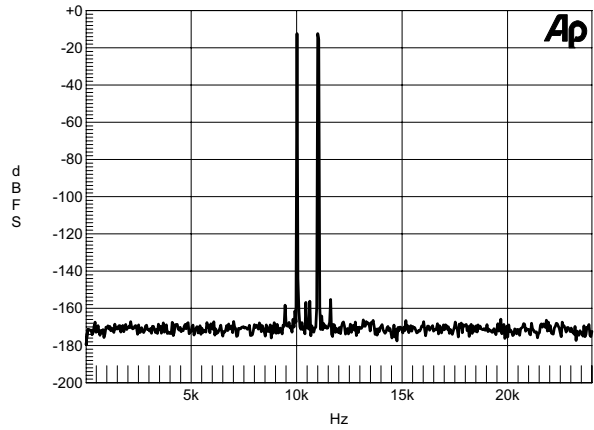


Figure 21b. IMD, 10 kHz and 11 kHz -7 dBFS, 96 kHz:48 kHz

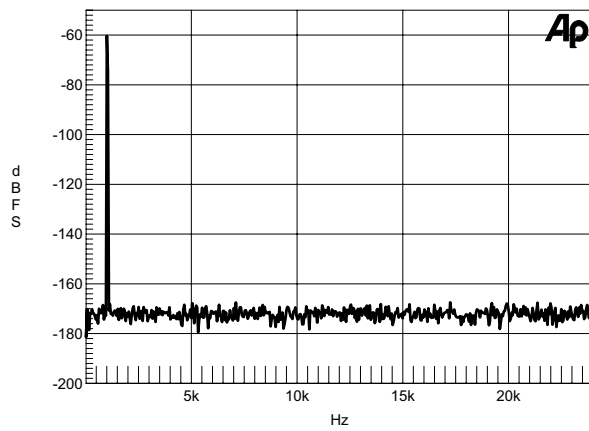


Figure 22a. Wideband FFT Plot (16k Points) -60 dBFS 1 kHz Tone, 192 kHz:48 kHz

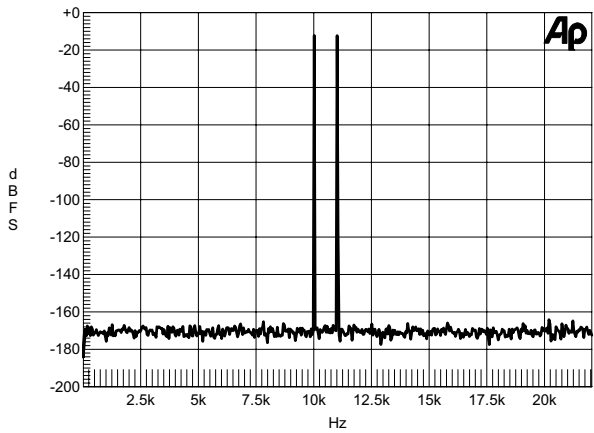


Figure 22b. IMD, 10 kHz and 11 kHz -7 dBFS, 48 kHz:44.1 kHz

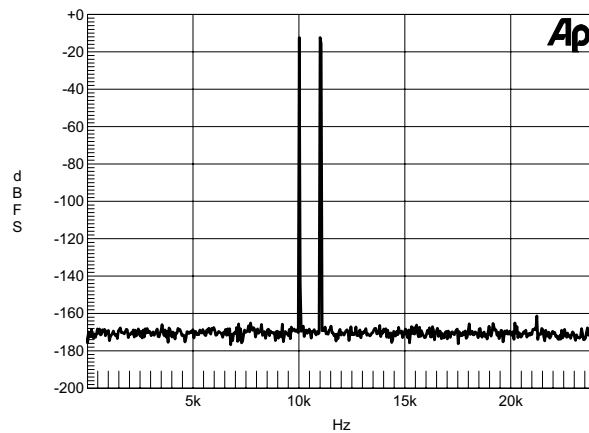


Figure 23a. IMD, 10 kHz and 11 kHz -7 dBFS, 44.1 kHz:48 kHz

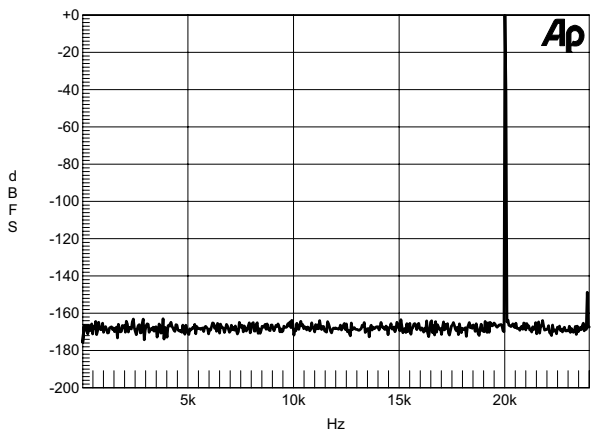


Figure 23b. Wideband FFT Plot (16k Points) 0 dBFS 20 kHz Tone, 44.1 kHz:48 kHz

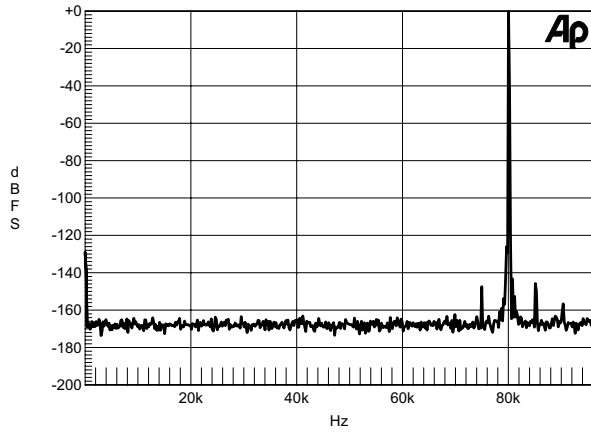


Figure 24a. Wideband FFT Plot (16k Points) 0 dBFS 80 kHz Tone, 192 kHz:192 kHz

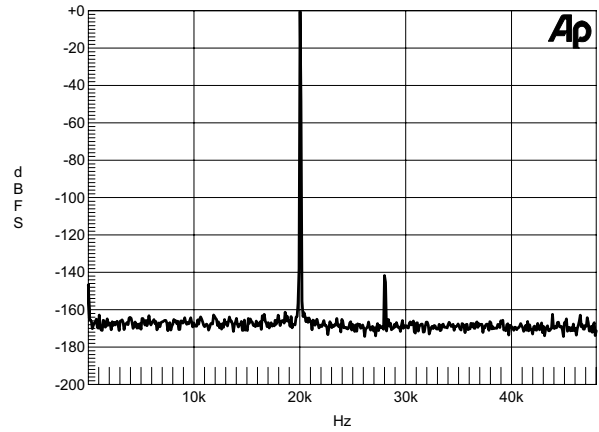


Figure 24b. Wideband FFT Plot (16k Points) 0 dBFS 20 kHz Tone, 48 kHz:96 kHz

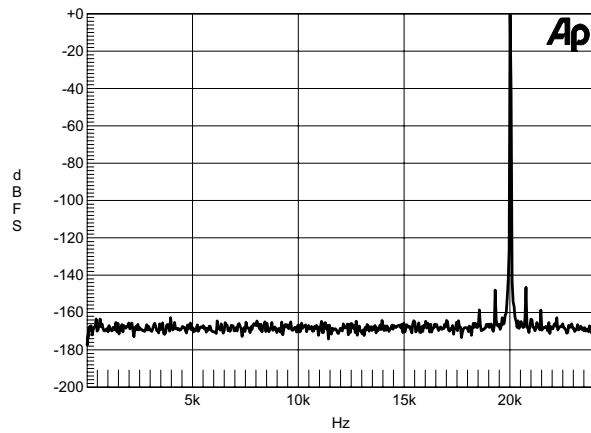


Figure 25a. Wideband FFT Plot (16k Points) 0 dBFS 20 kHz Tone, 48 kHz:48 kHz

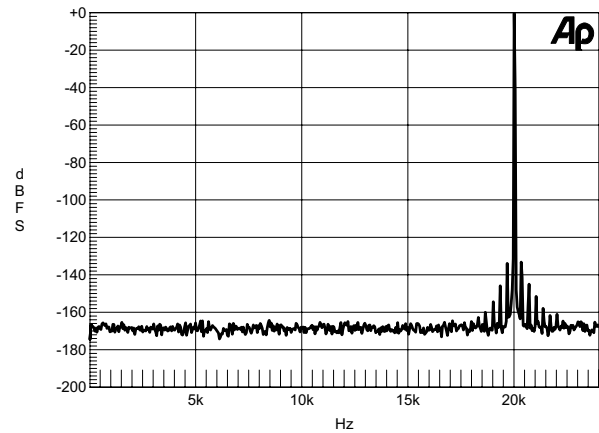


Figure 25b. Wideband FFT Plot (16k Points) 0 dBFS 20 kHz Tone, 96 kHz:48 kHz

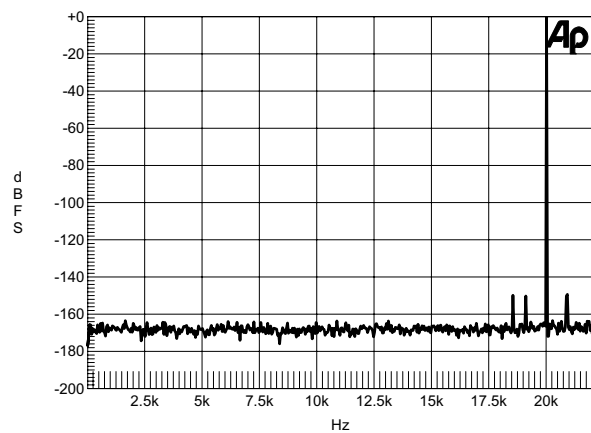


Figure 26a. Wideband FFT Plot (16k Points) 0 dBFS 20 kHz Tone, 48 kHz:44.1 kHz

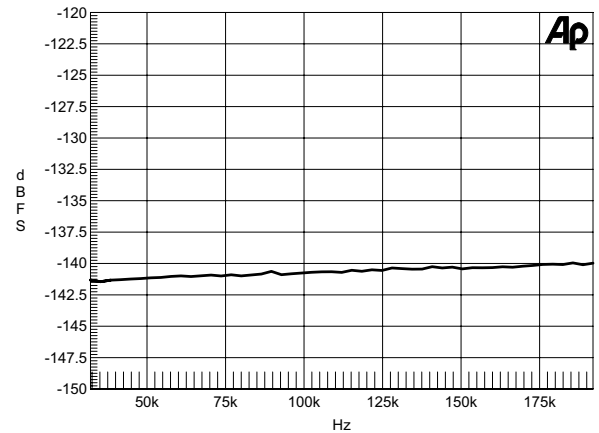


Figure 26b. THD+N vs. Output Sample Rate, 0 dBFS 1 kHz Tone, Fsi = 192 kHz

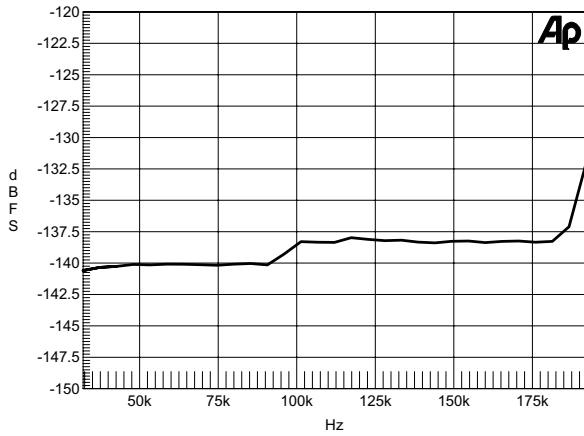


Figure 27a. THD+N vs. Output Sample Rate, 0 dBFS 1 kHz Tone, Fsi = 48 kHz

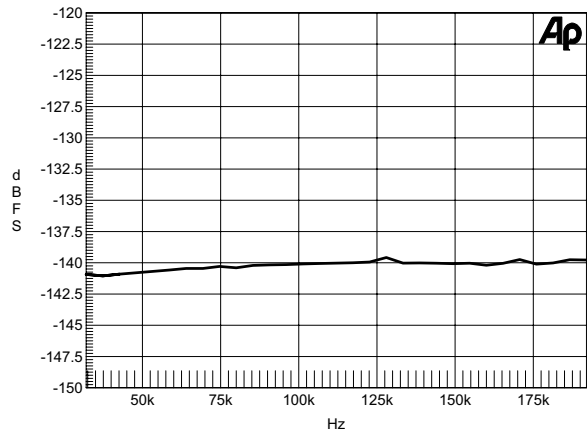


Figure 27b. THD+N vs. Output Sample Rate, 0 dBFS 1 kHz Tone, Fsi = 96 kHz

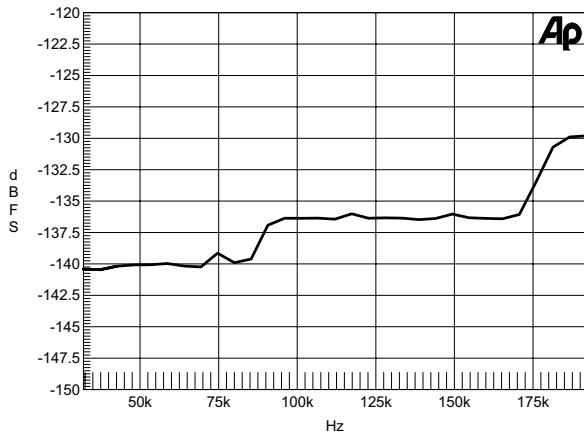


Figure 28a. THD+N vs. Output Sample Rate, 0 dBFS 1 kHz Tone, Fsi = 44.1 kHz

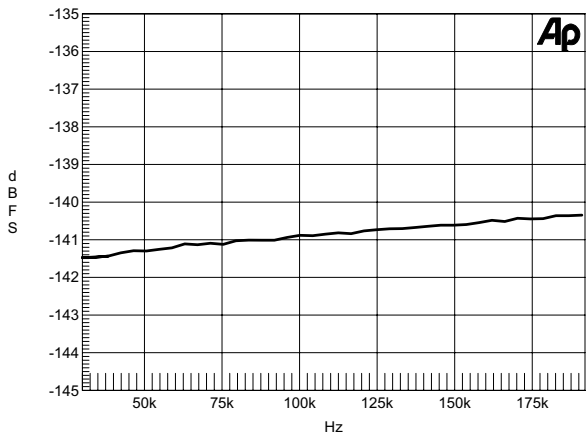


Figure 28b. Dynamic Range vs. Output Sample Rate, -60 dBFS 1 kHz Tone, Fsi = 192 kHz

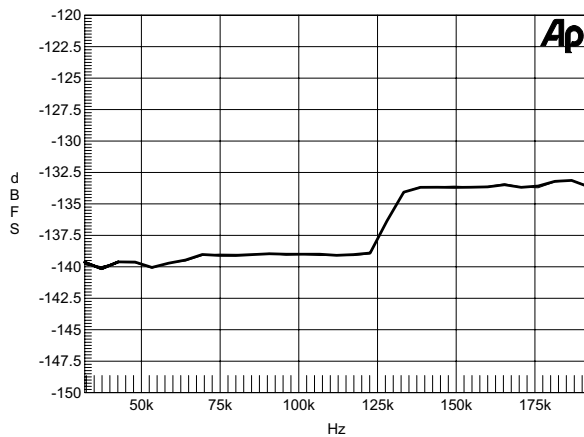


Figure 29a. THD+N vs. Output Sample Rate, 0 dBFS 1 kHz Tone, Fsi = 32 kHz

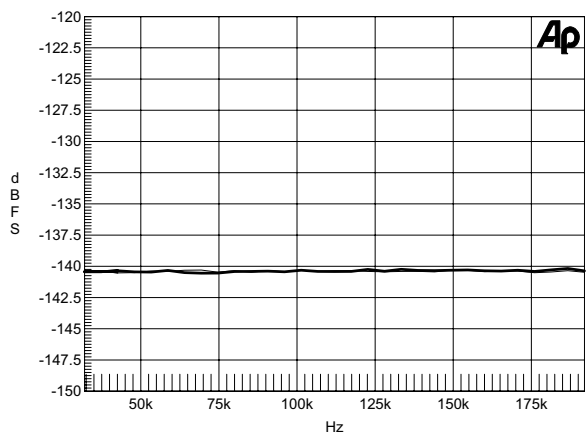


Figure 29b. Dynamic Range vs. Output Sample Rate, -60 dBFS 1 kHz Tone, Fsi = 32 kHz

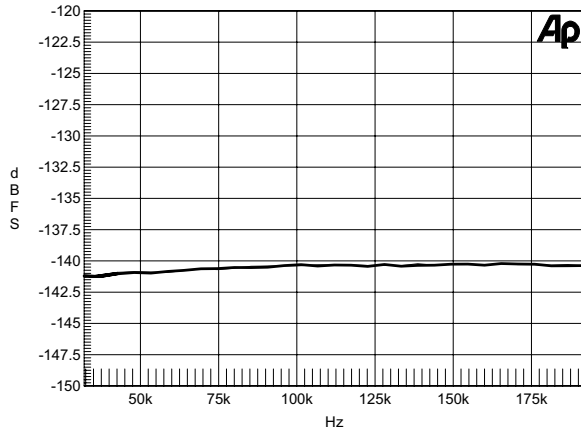


Figure 30a. Dynamic Range vs. Output Sample Rate, -60 dBFS 1 kHz Tone, Fsi = 96 kHz

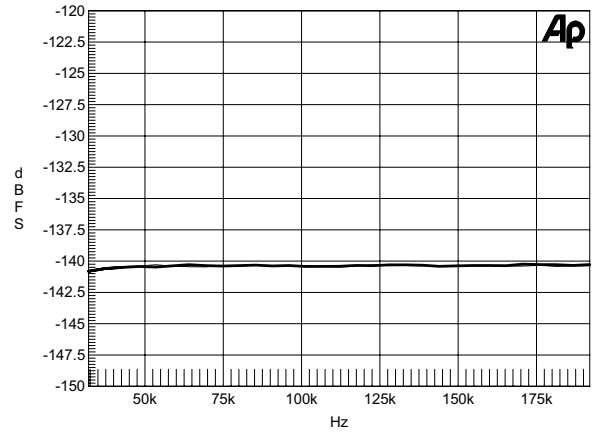


Figure 30b. Dynamic Range vs. Output Sample Rate, -60 dBFS 1 kHz Tone, Fsi = 44.1 kHz

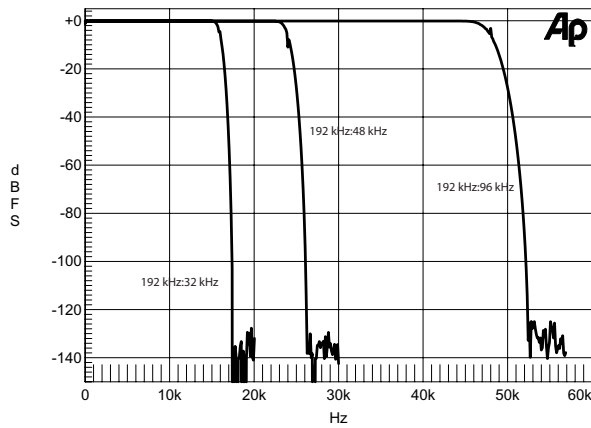


Figure 31a. Frequency Response with 0 dBFS Input

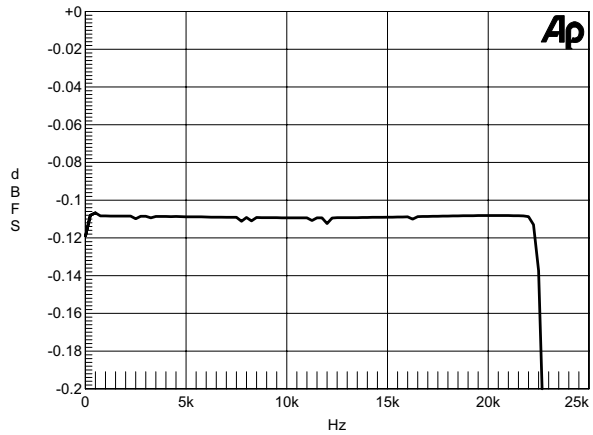


Figure 31b. Passband Ripple, 192 kHz:48 kHz

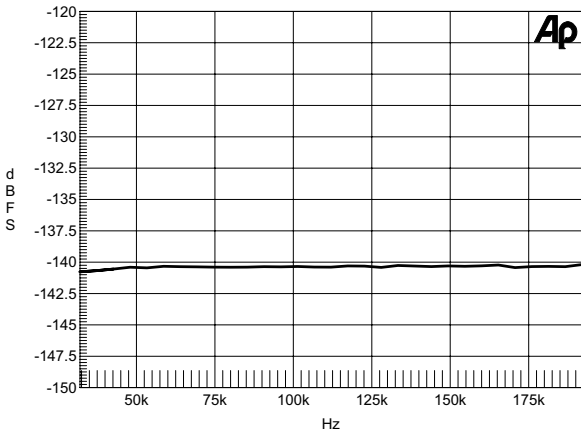


Figure 32a. Dynamic Range vs. Output Sample Rate, -60 dBFS 1 kHz Tone, Fsi = 48 kHz

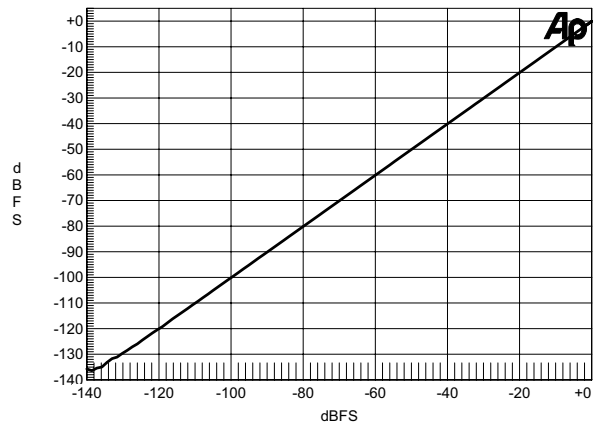


Figure 32b. Linearity Error, 0 to -140 dBFS Input, 200 Hz Tone, 48 kHz:48 kHz

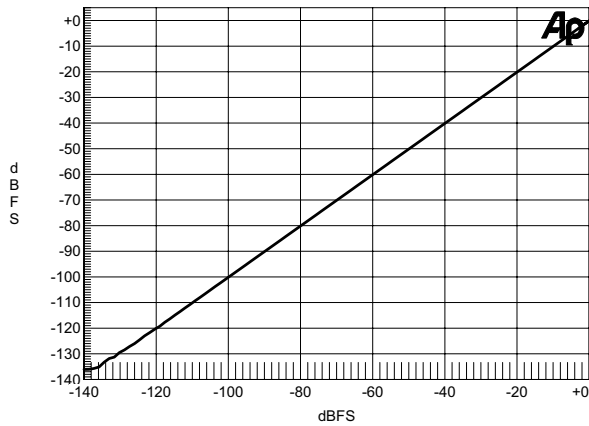


Figure 33a. Linearity Error, 0 to -140 dBFS Input, 200 Hz Tone, 48 kHz:44.1 kHz

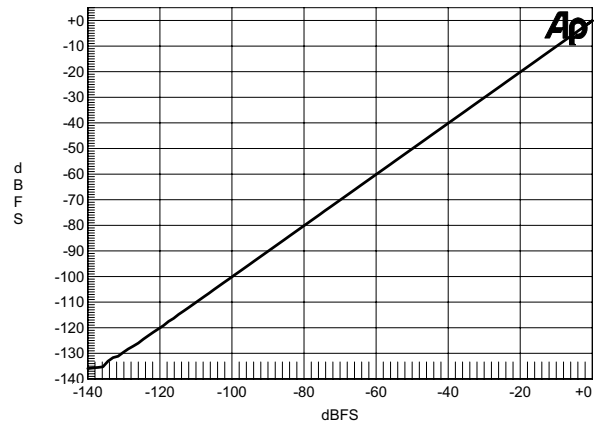


Figure 33b. Linearity Error, 0 to -140 dBFS Input, 200 Hz Tone, 48 kHz:96 kHz

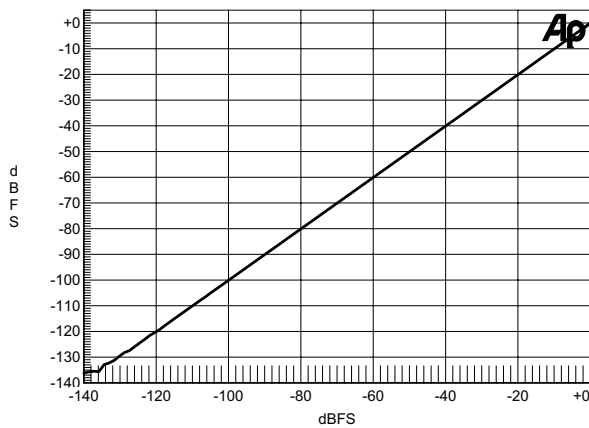


Figure 34a. Linearity Error, 0 to -140 dBFS Input, 200 Hz Tone, 96 kHz:48 kHz

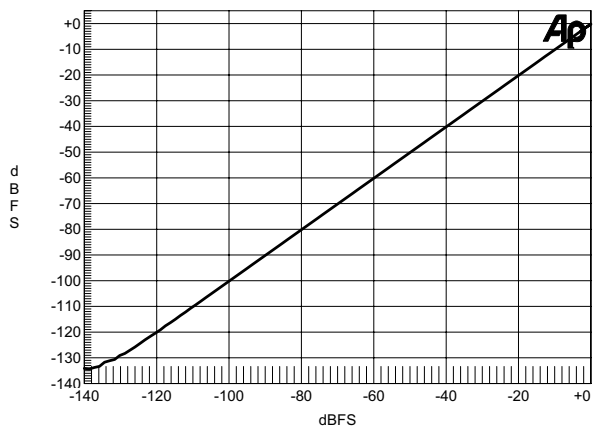


Figure 34b. Linearity Error, 0 to -140 dBFS Input, 200 Hz Tone, 44.1 kHz:192 kHz

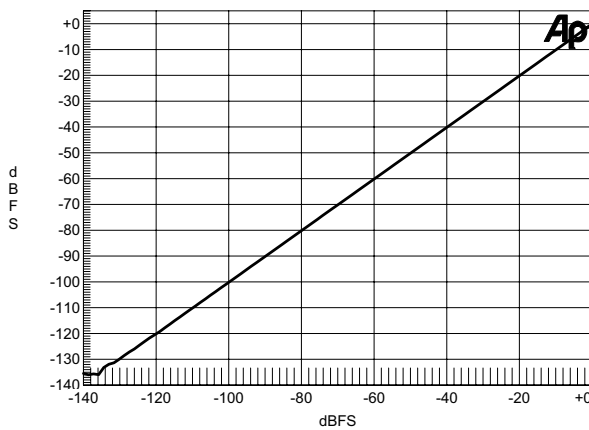


Figure 35a. Linearity Error, 0 to -140 dBFS Input, 200 Hz Tone, 44.1 kHz:48 kHz

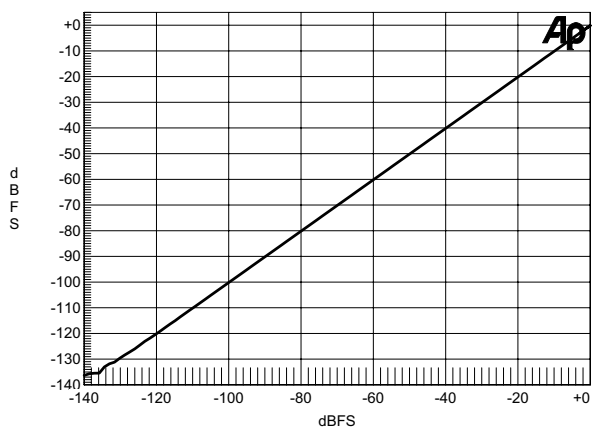


Figure 35b. Linearity Error, 0 to -140 dBFS Input, 200 Hz Tone, 192 kHz:44.1 kHz

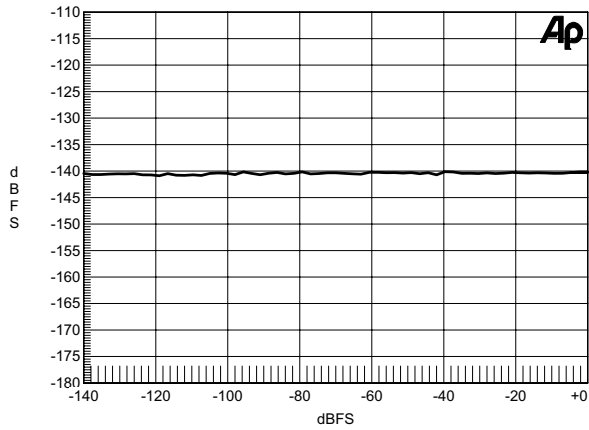


Figure 36a. THD+N vs. Input Amplitude, 1 kHz Tone, 48 kHz:44.1 kHz

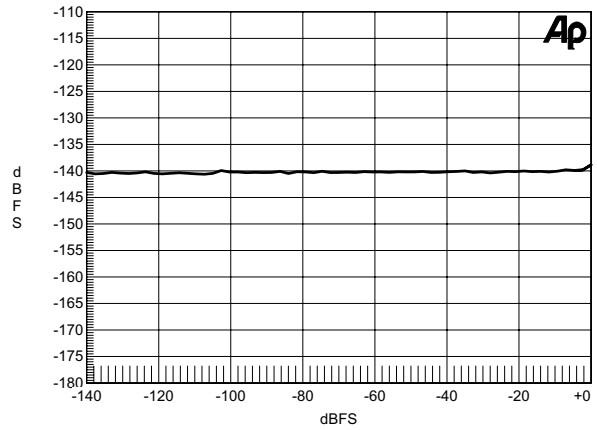


Figure 36b. THD+N vs. Input Amplitude, 1 kHz Tone, 48 kHz:96 kHz

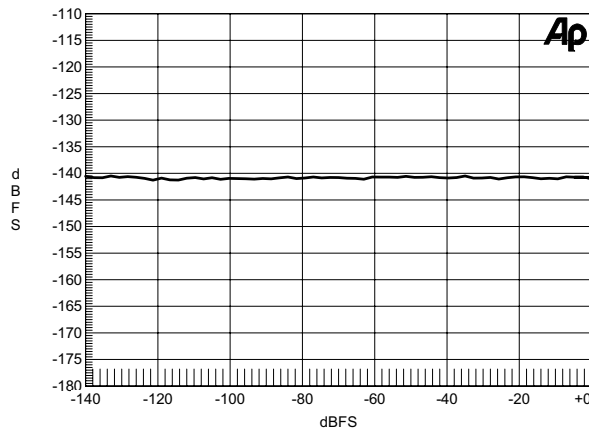


Figure 37a. THD+N vs. Input Amplitude, 1 kHz Tone, 96 kHz:48 kHz

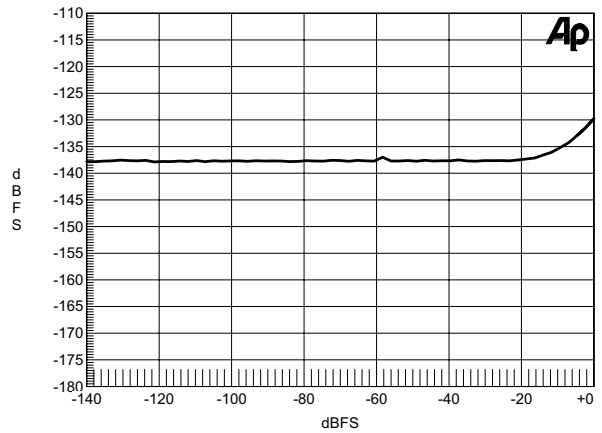


Figure 37b. THD+N vs. Input Amplitude, 1 kHz Tone, 44.1 kHz:192 kHz

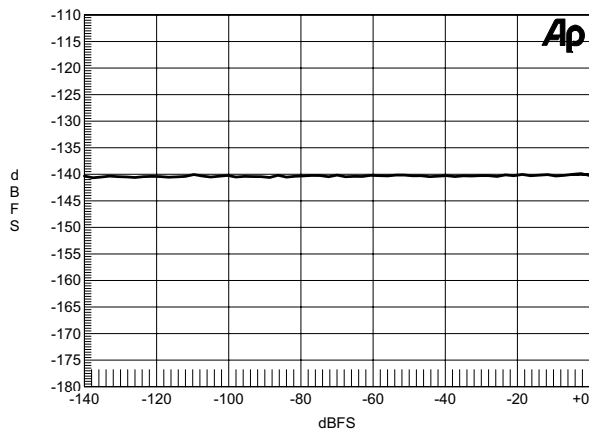


Figure 38a. THD+N vs. Input Amplitude, 1 kHz Tone, 44.1 kHz:48 kHz

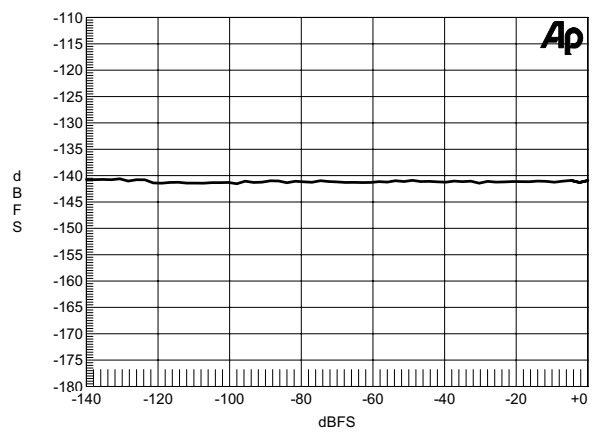
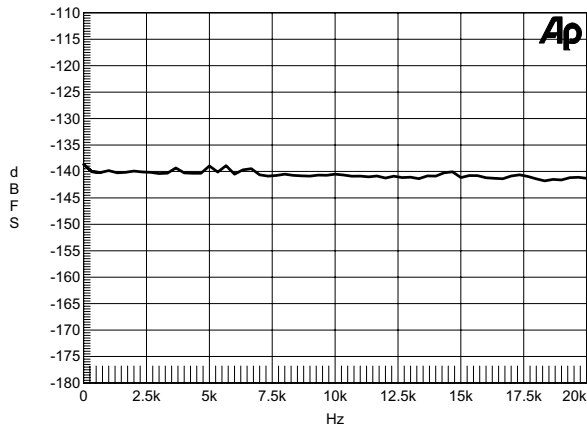
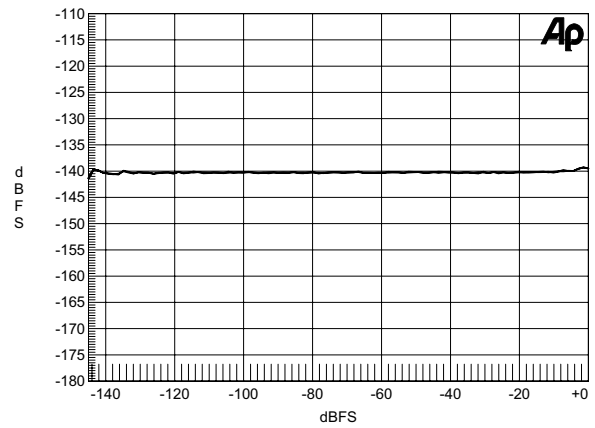
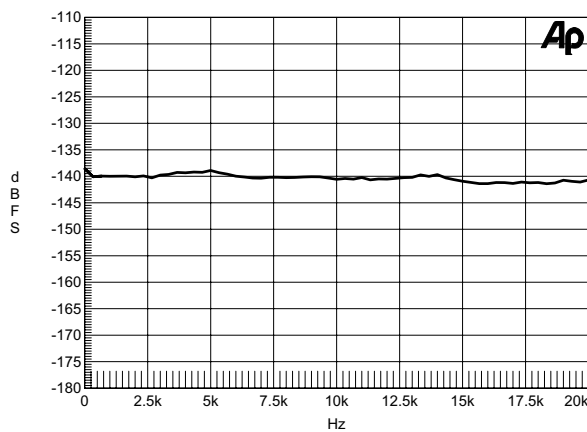
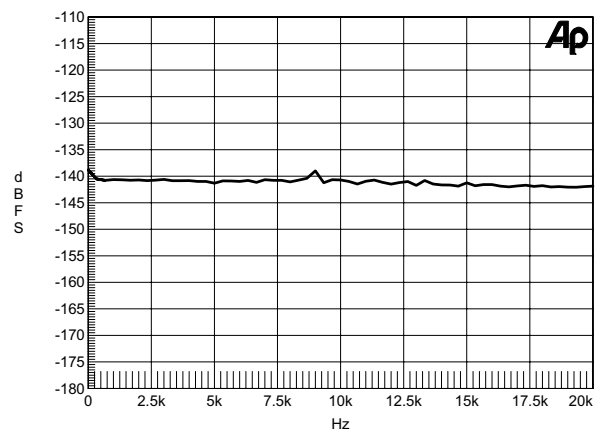


Figure 38b. THD+N vs. Input Amplitude, 1 kHz Tone, 192 kHz:48 kHz


Figure 39a. THD+N vs. Frequency Input, 0 dBFS, 48 kHz:44.1 kHz

Figure 39b. THD+N vs. Frequency Input, 0 dBFS, 48 kHz:96 kHz

Figure 40a. THD+N vs. Frequency Input, 0 dBFS, 44.1 kHz:48 kHz

Figure 40b. THD+N vs. Frequency Input, 0 dBFS, 96 kHz:48 kHz

All performance plots represent typical performance. Measurements for all performance plots were taken under the following conditions, unless otherwise stated:

- $V_D = 2.5\text{ V}$, $V_L = 3.3\text{ V}$
- Serial Audio Input port set to slave
- Serial Audio Output port set to slave
- Input and output clocks and data are asynchronous
- $XTI/XTO = 27\text{ MHz}$
- Input signal = 1.000 kHz, 0 dBFS
- Measurement Bandwidth = 20 to $(F_{so}/2)$ Hz
- Word Width = 24 Bits

9. APPLICATIONS

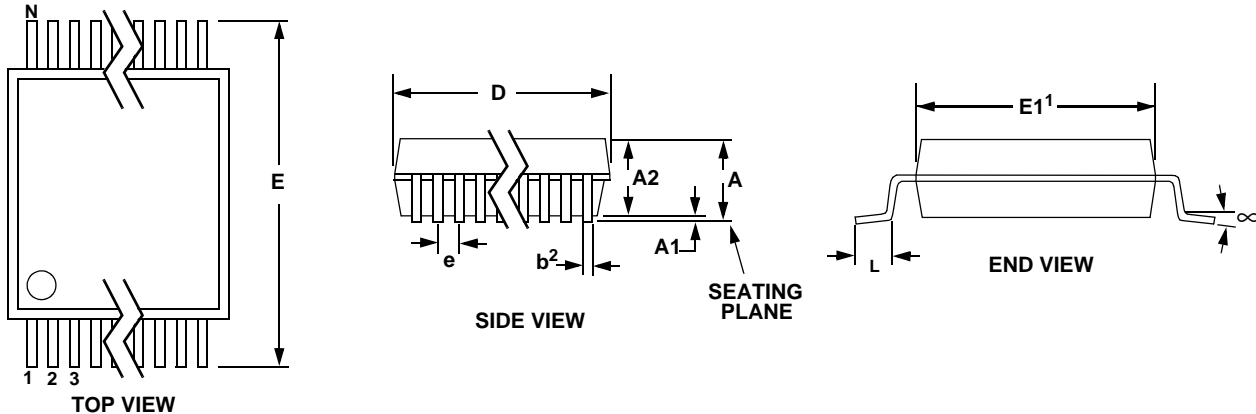
9.1 Reset, Power Down, and Start-up

When $\overline{\text{RST}}$ is low the CS8421 enters a low power mode, all internal states are reset, and the outputs are disabled. After $\overline{\text{RST}}$ transitions from low to high the part senses the resistor value on the configuration pins (MS_SEL, SAIF, and SAOF) and sets the appropriate mode of operation. After the mode has been set (approximately 4 μs) the part is set to normal operation and all outputs are functional.

9.2 Power Supply, Grounding, and PCB layout

The CS8421 operates from a $V_D = +2.5\text{ V}$ and $V_L = +3.3\text{ V}$ or $+5.0\text{ V}$ supply. These supplies may be set independently. Follow normal supply decoupling practices, see Figure 5.

Extensive use of power and ground planes, ground plane fill in unused areas, and surface mount decoupling capacitors are recommended. Decoupling capacitors should be mounted on the same side of the board as the CS8421 to minimize inductance effects and all decoupling capacitors should be as close to the CS8421 as possible. The pin of the configuration resistors not connected to MS_SEL, SAIF, and SAOF should be connected as close as possible to V_L or GND.

10. PACKAGE DIMENSIONS
20L TSSOP (4.4 mm BODY) PACKAGE DRAWING


DIM	INCHES			MILLIMETERS			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.252	0.256	0.259	6.40	6.50	6.60	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	--	0.026	--	--	0.65	
L	0.020	0.024	0.028	0.50	0.60	0.70	
∞	0°	4°	8°	0°	4°	8°	

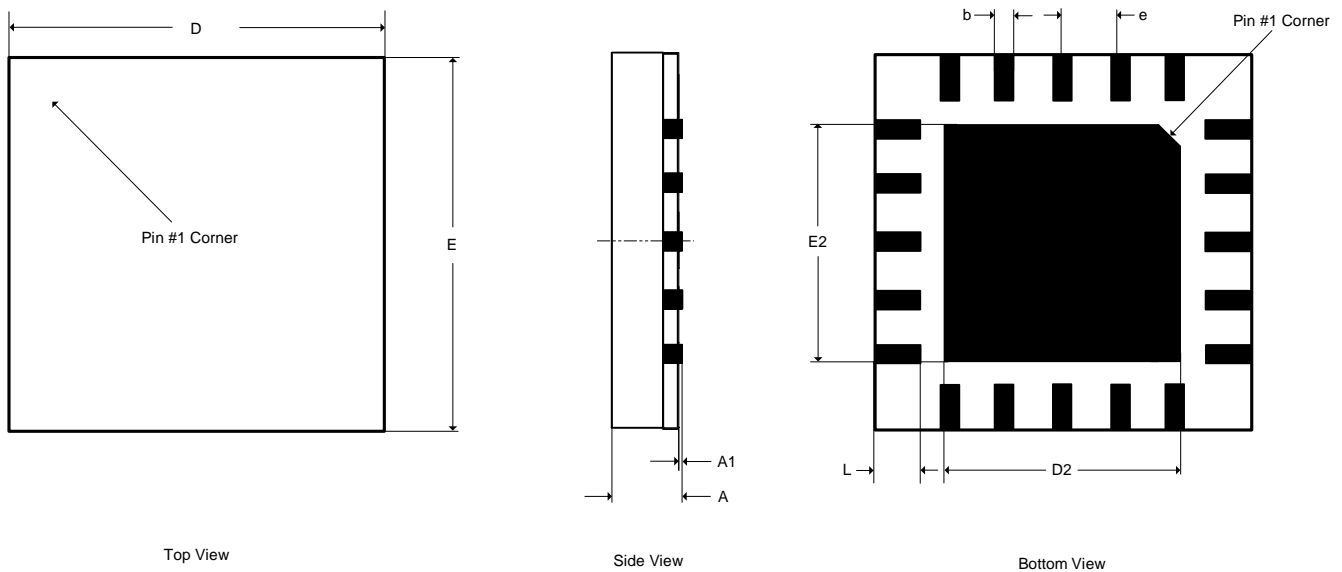
JEDEC #: MO-153

Controlling Dimension is Millimeters.

- Notes:
1. "D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
 2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
 3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

THERMAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Impedance	2 Layer Board	θ_{JA}	-	48	-	°C/Watt
	4 Layer Board		-	38	-	°C/Watt

20-PIN QFN (5 × 5 MM BODY) PACKAGE DRAWING


DIM	INCHES			MILLIMETERS			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.0394	--	--	1.00	1
A1	0.0000	--	0.0020	0.00	--	0.05	1
b	0.0091	0.0110	0.0130	0.23	0.28	0.33	1,2
D	0.1969 BSC			5.00 BSC			1
D2	0.1201	0.1220	0.1240	3.05	3.10	3.15	1
E	0.1969 BSC			5.00 BSC			1
E2	0.1202	0.1221	0.1241	3.05	3.10	3.15	1
e	0.0256 BSC			0.65 BSC			1
L	0.0197	0.0236	0.0276	0.50	0.60	0.70	1

JEDEC #: MO-220

Controlling Dimension is Millimeters.

- Notes: 1. Dimensioning and tolerance per ASME Y 14.5M-1995.
 2. Dimensioning lead width applies to the plated terminal and is measured between 0.23mm and 0.33mm from the terminal tip.

THERMAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Impedance	2 Layer Board	θ_{JA}	-	131	-	°C/Watt
	4 Layer Board		-	38	-	°C/Watt

11. REVISION HISTORY

Release	Date	Changes
A1	July 2004	Initial Advance Release
PP1	January 2005	<ul style="list-style-type: none"> -Updated "Features" on page 1. -Updated "Sample Rate with other XTI clocks" on page 6. -Updated "DC Electrical Characteristics" on page 7. -Updated "Digital Input Characteristics" on page 7. -Updated "Digital Interface Specifications" on page 7 -Updated Figure 5. "Typical Connection Diagram, Master and Slave Modes" on page 10. -Added Figure 6. "Typical Connection Diagram, No External Master Clock" on page 11. -Corrected reference to bypass mode to output only data on page 12. -Added section 6.1, "Clocking" on page 15. -Updated "Master Clock" on page 17. -Updated "Time Division Multiplexing (TDM) Mode" on page 18. -Added Thermal Pad label "Pin Descriptions" on page 20. -Added Thermal Pad pin description to "QFN Pin Descriptions" on page 22. -Updated "Performance Plots" beginning on page 23.

Table 6. Revision History

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com

IMPORTANT NOTICE

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