



## CMOS I<sup>2</sup>C 2-WIRE BUS 4K ELECTRICALLY ERASABLE PROGRAMMABLE ROM 512 X 8 BIT EEPROM

### FEATURES :

- Power Supply Voltage  
Single Vcc for Read and Programming  
(Vcc = 2.7 V to 5.5 V)
- Low Power (Isb = 2µa @ 5.5 V)
- I<sup>2</sup>C Bus, 2-Wire Serial Interface
- Support Byte Write and Page Write (16 Bytes)
- Automatic Page write Operation (maximum 10 ms)  
Internal Control Timer  
Internal Data Latches for 16 Bytes
- High Reliability CMOS Technology with EEPROM Cell  
Endurance : 1,000,000 Cycles  
Data Retention : 100 Years

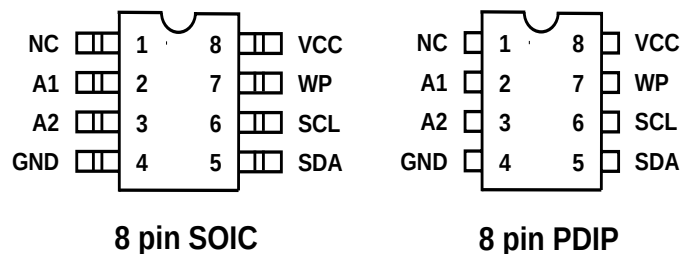
### DESCRIPTION:

The Turbo IC 24C04 is a serial 4K EEPROM fabricated with Turbo's proprietary, high reliability, high performance CMOS technology. Its 4K of memory is organized as 512 x 8 bits. The memory is configured as 32 pages with each page containing 16 bytes. This device offers significant advantages in low power applications.

The Turbo IC 24C04 uses the I<sup>2</sup>C addressing protocol and 2-wire serial interface which includes a bidirectional serial data bus synchronized by a clock. It offers a flexible byte write and a faster 16-byte page write.

The Turbo IC 24C04 is assembled in either a 8-pin PDIP or 8-pin SOIC package. Pin #1 is not connected (NC). Pin #2 is the A1 device address input for the 24C04. Pin #3 is the A2 device address input for the 24C04, such that a total of four 24C04 devices can be connected on a single bus. Pin #4 is the ground (Vss). Pin #5 is the serial data (SDA) pin used for bidirectional transfer of data. Pin #6 is the serial clock (SCL) input pin. Pin #7 is the write protect (WP) pin used to protect hardware data. Pin #8 is the power supply (Vcc) pin.

### PIN DESCRIPTION



### PIN DESCRIPTION

#### DEVICE ADDRESS (A1 & A2)

A1 and A2 are device address inputs that enables a total of four 24C04 devices to connect on a single bus. When the address input pin is left unconnected, it is interpreted as zero.

#### WRITE PROTECT (WP)

When the write protect input is connected to Vcc, the entire memory array is protected against write operations. For normal write operations, the write protect pin should be grounded. When the pin is left unconnected, WP is interpreted as zero.

#### SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data in and out of the Turbo IC 24C04. The pin is an open-drain output. A pullup resistor must be connected from SDA to Vcc.

#### SERIAL CLOCK (SCL)

The SCL input synchronizes the data on the SDA bus. It is used in conjunction with SDA to define the start and stop conditions. It is also used in conjunction with SDA to transfer data to and from the Turbo IC 24C04.



#### DESCRIPTION (Continued):

For a write operation, the master issues a start condition, a device address byte, a memory address byte, and then up to 16 data bytes. The Turbo IC 24C04 acknowledges after each byte transmission. To terminate the transmission, the master issues a stop condition by pulling SDA from low to high while SCL is high.

For a read operation, the master issues a start condition and a device address byte. The Turbo IC 24C04 acknowledges, and then transmits a data byte, which is accessed from the EEPROM memory. The master acknowledges, indicating that it requires more data bytes. The Turbo IC 24C04 transmits more data bytes, with the memory address counter automatically incrementing for each data byte, until the master does not acknowledge, indicating that it is terminating the transmission. The master then issues a stop condition.

#### DEVICE OPERATION:

##### BIDIRECTIONAL BUS PROTOCOL:

The Turbo IC 24C04 follows the I<sup>2</sup>C bus protocol. The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving device as a receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates the data transfers, and provides the clock for both transmit and receive operations. The Turbo IC 24C04 acts as a slave device in all applications. Either the master or the slave can take control of the SDA bus, depending on the requirement of the protocol.

##### ACKNOWLEDGE:

All data is serially transmitted in bytes (8 bits) on the SDA bus. The acknowledge protocol is used as a handshake signal to indicate successful transmission of a byte of data. The bus transmitter, either the master or the slave (Turbo IC 24C04), releases the bus after sending a byte of data on the SDA bus. The receiver pulls the SDA bus low during the ninth clock cycle to acknowledge the successful transmission of a byte of data. If the SDA is not pulled low during the ninth clock cycle, the Turbo IC 24C04 terminates the data transmission and goes into standby mode.

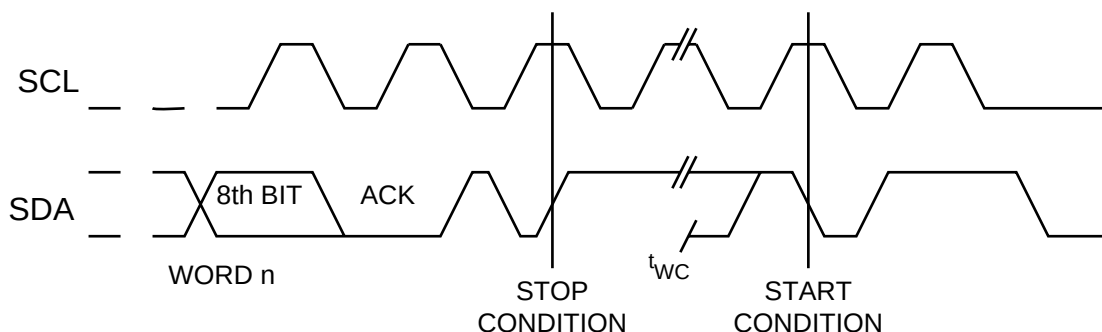
##### START/STOP CONDITION AND DATA TRANSITIONS:

While SCL clock is high, a high to low transition on the SDA bus is recognized as a START condition which precedes any read or write operation. While SCL clock is high, a low to high transition on the SDA bus is recognized as a STOP condition which terminates the communication and places the Turbo IC 24C04 into standby mode. All other data transitions on the SDA bus must occur while SCL clock is low to ensure proper operation.

For the write operation, the Turbo IC 24C04 acknowledges after the device address byte, acknowledges after the memory address byte, and acknowledges after each subsequent data byte.

For the read operation, the Turbo IC 24C04 acknowledges after the device address byte. Then the Turbo IC 24C04 transmits each subsequent data byte, and the master acknowledges after each data byte transfer, indicating that it requires more data bytes. The Turbo IC 24C04 monitors the SDA bus for the acknowledge. To terminate the transmission, the master does not acknowledge, and then sends a stop condition.

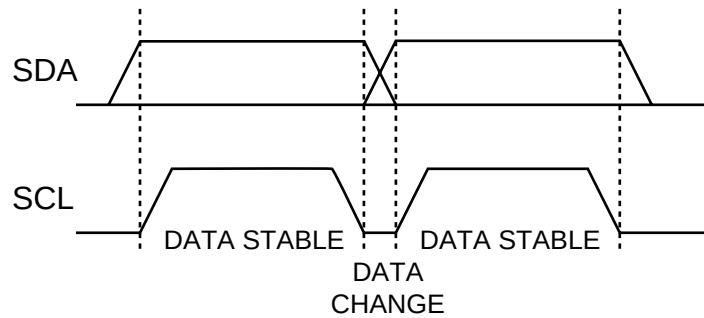
#### Write Cycle Timing



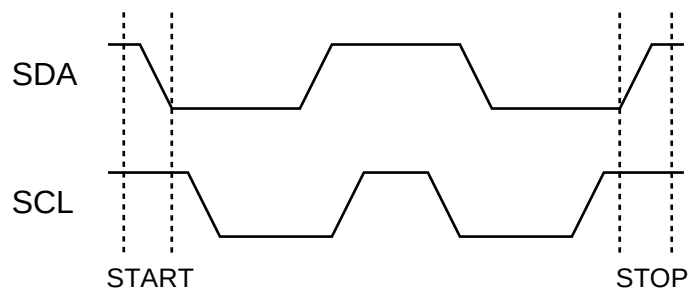
Note: The write cycle time  $t_{wc}$  is the time from a valid stop condition of a write sequence to the end of the internal clear / write cycle.



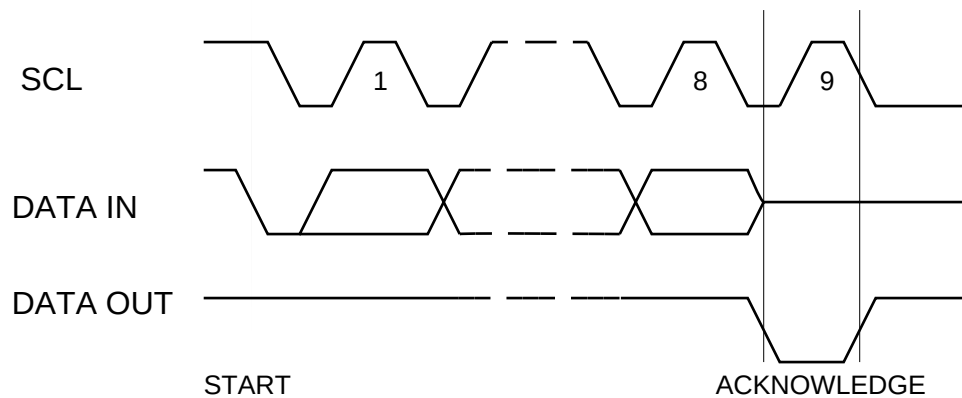
**Data Valid**



**Start and Stop Definition**



**Output Acknowledge**





#### DEVICE ADDRESSING:

Following the start condition, the master will issue a device address byte consisting of 1010 (A2) (A1) (B8) (R/W) to access the selected Turbo IC 24C04 for a read or write operation. A1 and A2 are the device address select bits which have to match the A1 and A2 pin inputs on the 24C04 device. The B[8] bit is the most significant bit of the memory address. The (R/W) bit is a high (1) for read and low (0) for write.

#### DATA INPUT DURING WRITE OPERATION:

During the write operation, the Turbo IC 24C04 latches the SDA bus signal on the rising edge of the SCL clock.

#### DATA OUTPUT DURING READ OPERATION:

During the read operation, the Turbo IC 24C04 serially shifts the data onto the SDA bus on the falling edge of the SCL clock.

#### MEMORY ADDRESSING:

The memory address is sent by the master in the form of 2 bytes. Device address A2 and memory address bits B[8], are included in the device address byte. The remaining memory address bits B[7:0] are included in the second byte. The memory address byte can only be sent as part of a write operation.

#### BYTE WRITE OPERATION:

The master initiates the byte write operation by issuing a start condition, followed by the device address byte 1010 (A2) (A1) (B8) 0, followed by the memory address byte, followed by one data byte, followed by an acknowledge, then a stop condition. After each byte transfer, the Turbo IC 24C04 acknowledges the successful data transmission by pulling the SDA bus low. The stop condition starts the internal EEPROM write cycle, and all inputs are disabled until the completion of the write cycle.

#### PAGE WRITE OPERATION:

The master initiates the page write operation by issuing a start condition, followed by the device address byte 1010 (A2) (A1) (B8) 0, followed by the memory address byte, followed by up to 16 data bytes, followed by an acknowledge, then a stop condition. After each byte transfer, the Turbo IC 24C04 acknowledges the successful data transmission by pulling SDA low. After each data byte transfer, the memory address counter is automatically incremented by one. The stop condition starts the internal EEPROM write cycle only if the stop condition occurs in the clock cycle immediately following the acknowledge (10th clock cycle). All inputs are disabled until the completion of the write cycle.

#### POLLING ACKNOWLEDGE:

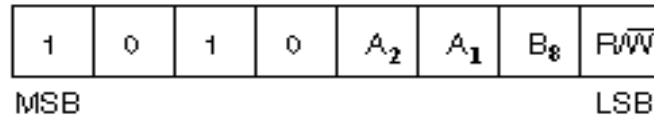
During the internal write cycle of a write operation in the Turbo IC 24C04, the completion of the write cycle can be detected by polling acknowledge. The master starts acknowledge polling by issuing a start condition, then followed by the device address byte 1010 (A2) (A1) (B8) 0. If the internal write cycle is finished, the Turbo IC 24C04 acknowledges by pulling the SDA bus low. If the internal write cycle is still ongoing, the Turbo IC 24C04 does not acknowledge because its inputs are disabled. Therefore, the device will not respond to any command. By using polling acknowledge, the system delay for write operations can be reduced. Otherwise, the system needs to wait for the maximum internal write cycle time, tWC, given in the spec.

#### POWER ON RESET:

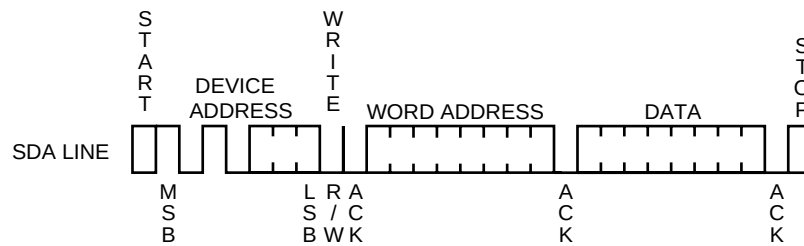
The Turbo IC 24C04 has a Power On Reset circuit (POR) to prevent data corruption and accidental write operations during power up. On power up, the internal reset signal is on and the Turbo IC 24C04 will not respond to any command until the VCC voltage has reached the POR threshold value.



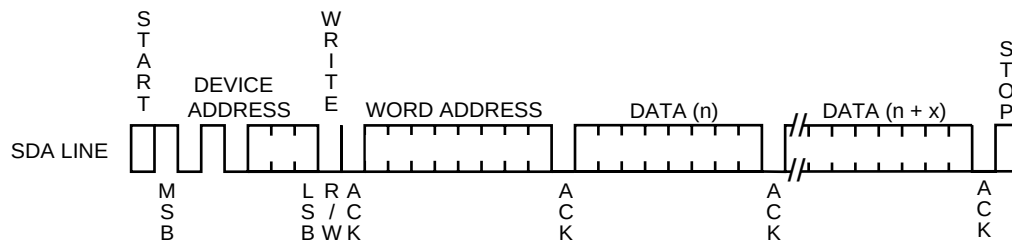
### Device Address



### Byte Write



### Page Write





#### CURRENT ADDRESS READ:

The internal memory address counter of the Turbo IC 24C04 contains the last memory address accessed during the previous read or write operation, incremented by one. To start the current address read operation, the master issues a start condition, followed by the device address byte 1010 (A2) (A1) (B8) 1. The Turbo IC 24C04 responds with an acknowledge by pulling the SDA bus low, and then serially shifts out the data byte accessed from memory at the location corresponding to the memory address counter. The master does not acknowledge, then sends a stop condition to terminate the read operation. It is noted that the memory address counter is incremented by one after the data byte is shifted out.

#### RANDOM ADDRESS READ:

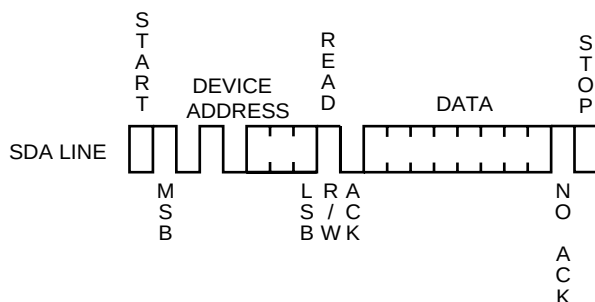
The master starts with a dummy write operation (one with no data bytes) to load the internal memory address counter by first issuing a start condition, followed by the device address byte 1010 (A2) (A1) (B8) 0, followed by the memory address bytes. Following the acknowledge from the Turbo IC 24C04, the master starts the current read operation by issuing a start condition, followed by the device address byte 1010 (A2) (A1) (B8) 1. The Turbo IC 24C04 responds with

an acknowledge by pulling the SDA bus low, and then serially shifts out the data byte accessed from memory at the location corresponding to the memory address counter. The master does not acknowledge, then sends a stop condition to terminate the read operation. It is noted that the memory address counter is incremented by one after the data byte is shifted out.

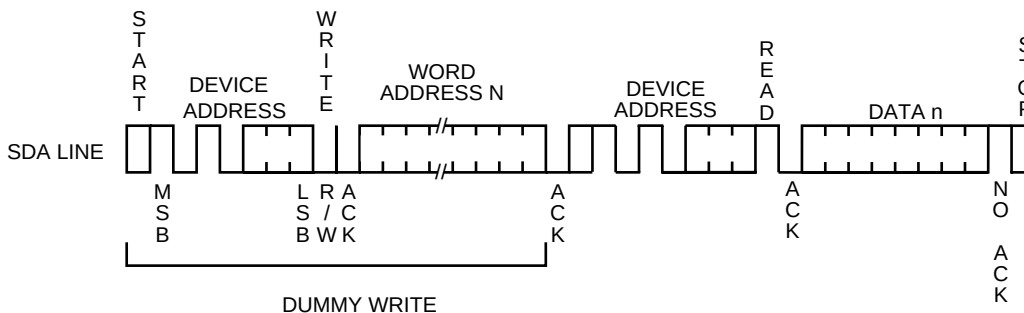
#### SEQUENTIAL READ:

The sequential read is initiated by either a current address read or random address read. After the Turbo IC 24C04 serially shifts out the first data byte, the master acknowledges by pulling the SDA bus low, indicating that it requires additional data bytes. After the data byte is shifted out, the Turbo IC 24C04 increments the memory address counter by one. Then the Turbo IC 24C04 shifts out the next data byte. The sequential reads continues for as long as the master keeps acknowledging. When the memory address counter is at the last memory location, the counter will 'roll-over' when incremented by one to the first location in memory (address zero). The master terminates the sequential read operation by not acknowledging, then sends a stop condition.

#### Current Address Read

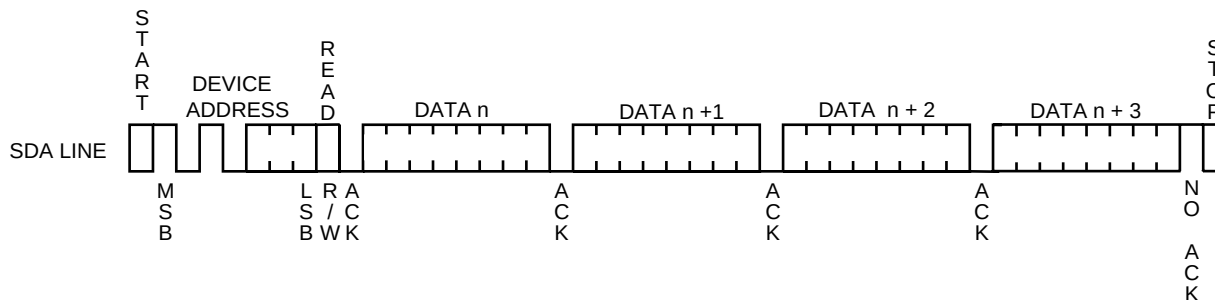


#### Random Read





#### Sequential Read



#### ABSOLUTE MAXIMUM RATINGS

##### TEMPERATURE

Storage: -65° C to 150° C  
Under Bias: -55° C to 125° C

##### ALL INPUT OR OUTPUT VOLTAGES

with respect to Vss +6 V to -0.3 V

\* "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### RECOMMENDED OPERATING CONDITIONS

Temperature Range: Commercial: 0° C to 70° C  
Industrial: -40° C to 85° C  
Military: -55° C to 125° C

Vcc Supply Voltage: 2.7 to 5.5 Volts

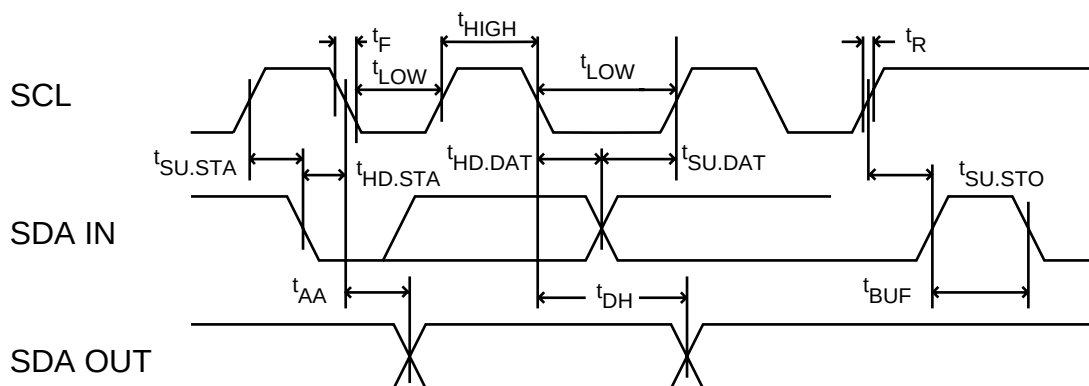
Endurance: 100,000 Cycles/Byte (Typical)  
Data Retention: 100 Years

#### D.C. CHARACTERISTICS

| Symbol           | Parameter              | Condition           | Min     | Max     | Units |
|------------------|------------------------|---------------------|---------|---------|-------|
| I <sub>cc1</sub> | Active Vcc Current     | READ at 100 KHZ     |         | 1.0     | MA    |
| I <sub>cc2</sub> | Active Vcc Current     | WRITE at 100 KHZ    |         | 3.0     | MA    |
| I <sub>sb1</sub> | Standby Current        | Vcc = 4.5 v         |         | 2.0     | uA    |
|                  |                        | Vcc = 5.5 v         |         | 2.0     | uA    |
| I <sub>il</sub>  | Input Leakage Current  | Vin=Vcc Max         |         | 3       | uA    |
| I <sub>ol</sub>  | Output Leakage Current |                     |         | 3       | uA    |
| V <sub>il</sub>  | Input Low Voltage      |                     | -1.0    | 0.8     | V     |
| V <sub>ih</sub>  | Input High Voltage     |                     | Vccx0.7 | Vcc+0.5 | V     |
| V <sub>ol1</sub> | Output Low             | Vcc=4.5v Iol=2.1 mA |         | 0.4     | V     |



#### Bus Timing



#### A.C. CHARACTERISTICS

| Symbol              | Parameter                  | 2.7 volt |     | 5.5 volt |     | Units |
|---------------------|----------------------------|----------|-----|----------|-----|-------|
|                     |                            | Min      | Max | Min      | Max |       |
| SCL                 | SCL Clock Frequency        |          | 100 |          | 400 | KHZ   |
| T                   | Noise Suppression Time (1) |          | 100 |          | 50  | ns    |
| t <sub>LOW</sub>    | Clock Low Period           | 4.7      |     | 1.2      |     | us    |
| t <sub>HIGH</sub>   | Clock High Period          | 4.0      |     | 0.6      |     | us    |
| t <sub>AA</sub>     | SCL Low to SDA Data Out    | 0.1      | 4.5 | 0.1      | 0.9 | us    |
| t <sub>BUF</sub>    | Bus Free to New Start (1)  | 4.7      |     | 1.2      |     | us    |
| t <sub>HD.STA</sub> | Start Hold Time            | 4.0      |     | 0.6      |     | us    |
| t <sub>SU.STA</sub> | Start Set-up Time          | 4.7      |     | 0.6      |     | us    |
| t <sub>HD.DAT</sub> | Data-in Hold Time          | 0        |     | 0        |     | us    |
| t <sub>SU.DAT</sub> | Data-in Set-up Time        | 200      |     | 100      |     | ns    |
| t <sub>R</sub>      | SCL and SDA Rise Time (1)  |          | 1.0 |          | 0.3 | us    |
| t <sub>F</sub>      | SCL and SDA Fall Time (1)  |          | 300 |          | 300 | ns    |
| t <sub>SU.STO</sub> | Stop Set-up Time           | 4.7      |     | 0.6      |     | us    |
| t <sub>DH</sub>     | Data-out Hold Time         | 100      |     | 50       |     | ns    |
| t <sub>WC</sub>     | Write Cycle Time           |          | 10  |          | 10  | ms    |

Note: 1 This parameter is characterized and not 100% tested.

#### TURBO IC PRODUCTS AND DOCUMENTS

1. All documents are subject to change without notice. Please contact Turbo IC for the latest revision of documents.
2. Turbo IC does not assume any responsibility for any damage to the user that may result from accidents or operation under abnormal conditions.
3. Turbo IC does not assume any responsibility for the use of any circuitry other than what embodied in a Turbo IC product. No other circuits, patents, licenses are implied.
4. Turbo IC products are not authorized for use in life support systems or other critical systems where component failure may endanger life. System designers should design with error detection and correction, redundancy and back-up features.

#### Part Numbers & Order Information

