High Efficiency, Low Supply Current, Step-up DC/DC Converter

General Description

The RT9262/A is a compact, high efficient, step-up DC/DC converter with an adaptive current mode PWM control loop, providing a stable and high efficient operation over a wide range of load currents. It operates in both continuous and discontinuous current modes in stable waveforms without external compensation.

The low start-up input voltage below 1V makes RT9262/A suitable for 1 to 4 battery cell applications providing up to 400mA output current. The 550kHz high switching rate minimized the size of external components. Besides, the 17μA low quiescent current together with high efficiency maintains long battery lifetime.

The 1.8V to 5V output voltage is set with 2 external resistors. Both internal 2A switch and driver for driving external power devices (NMOS or NPN) are provided.

A 300mA LDO is included in RT9262 to provide a secondary low noise output as well as an output current stop in the shutdown mode. Similarly, a 1.8V to 5V LDO output voltage can be set with 2 external resistors. For RT9262A, a low battery detector with 0.86V detection voltage is included. RT9262/A are provided in SOP-8 packages.

Features

- **1.0V Low Start-up Input Voltage**
- **High Supply Capability to Deliver 3.3V 100mA with 1V Input Voltage**
- **17μA Quiescent (Switch-off) Supply Current**
- **90% Efficiency**
- **550kHz Fixed Switching Rate**
- **Providing Flexibility for Using Internal and External Power Switches**
- **Built-in 300mA LDO, also for the Zero-Output-Current Shutdown Mode (RT9262)**
- **Boost DC-DC Integrating LDO for Up-Down Regulation (RT9262)**
- **Built-in 0.86V Voltage Detector (RT9262A)**
- **8-Pin SOP Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- PDA
- Portable Instrument
- Wireless Equipment
- DSC
- LCD Back Bias Circuit
- RF-Tags

Ordering Information

RT9262/A □ □

- Package Type
  S : SOP-8
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)
- Include Low Battery Detector
- Include LDO

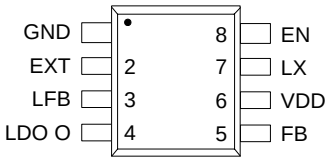
Note :

RichTek Pb-free and Green products are :

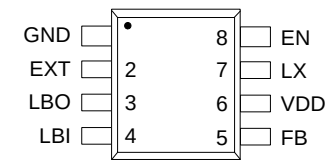
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100%matte tin (Sn) plating.

Pin Configurations

(TOP VIEW)



RT9262CS



RT9262ACS

SOP-8

Typical Application Circuit

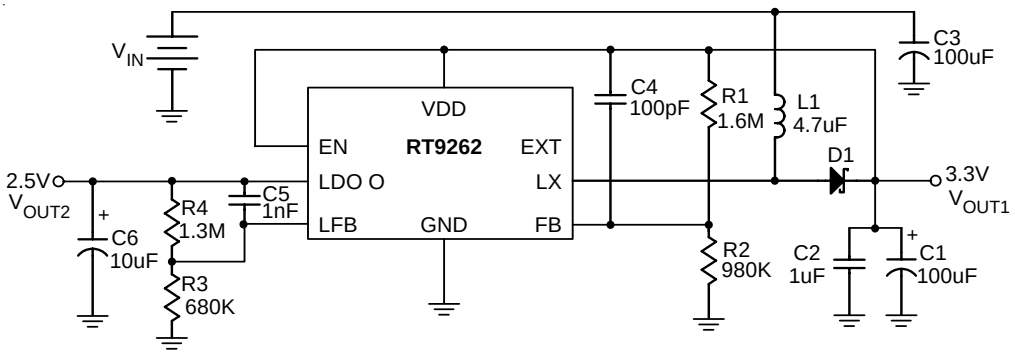


Figure 1. RT9262 Typical Application for Portable Instruments below 400mA

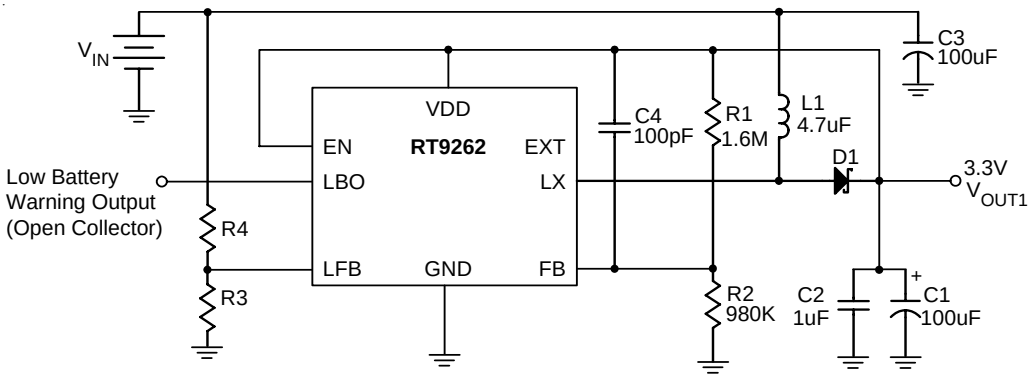


Figure 2. RT9262A Typical Application for Portable Instruments below 400mA

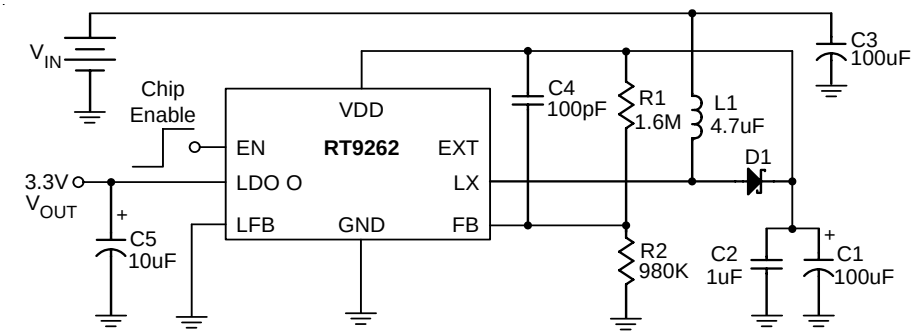


Figure 3. Application Circuit with Zero-Output-Current Shutdown Mode Control

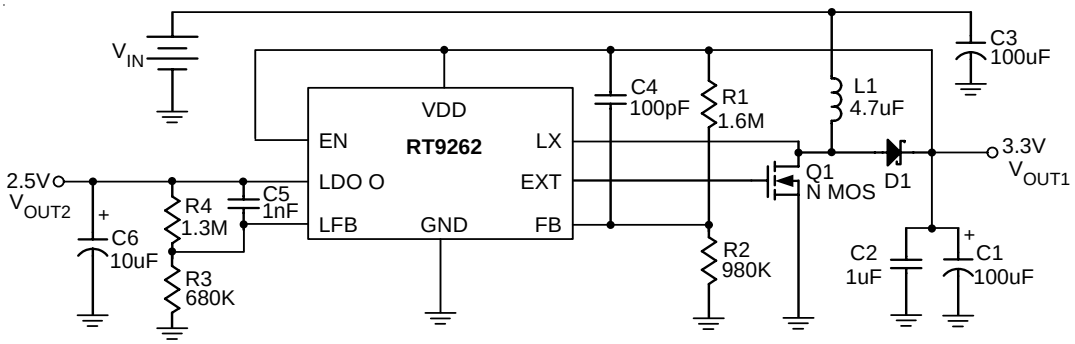


Figure 4. 0.4A ~ 2A Output Current Application

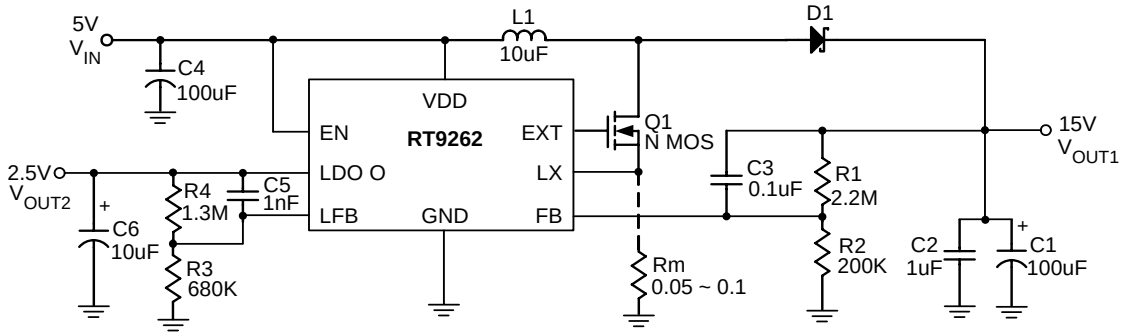
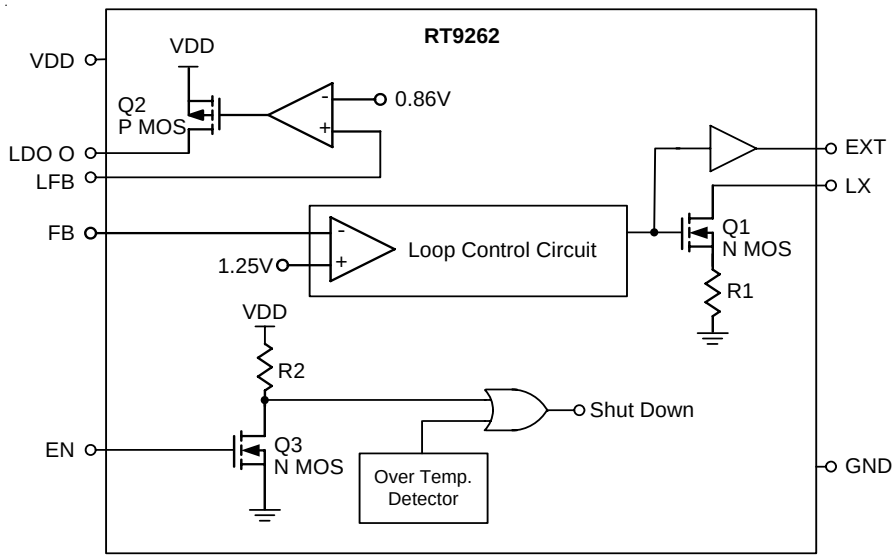


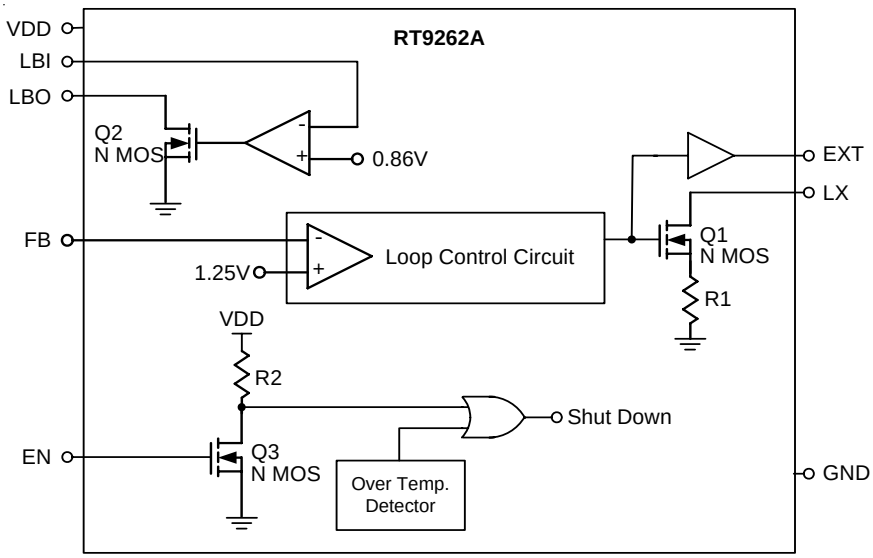
Figure 5. High Voltage Application (Rm should be added when IL > 100mA)

Functional Pin Description

Pin No.		Pin Name	Pin Function
RT9262	RT9262A		
1	1	GND	Ground
2	2	EXT	Output Pin for Driving External NMOS or NPN When driving an NPN, a resistor should be added for limiting base current.
3	--	LFB	Feedback Pin of the Built-in LDO (Internal Vref = 0.86V)
4	--	LDOO	Voltage Output Pin of the Built-in LDO
--	3	LBO	Drain Output Pin of the NMOS of the Built-in Low Voltage Detector This pin will be internally pulled low when the voltage at LBI pin drops to below 0.86V.
--	4	LBI	Input Pin of the Built-in Low Voltage Detector Trip point = 0.86V
5	5	FB	Feedback Input Pin Internal reference voltage for the error amplifier is 1.25V.
6	6	VDD	Input Positive Power Pin of RT9262/A
7	7	LX	Pin for Switching
8	8	EN	Chip Enable Pin (Active High).

Function Block Diagram





Absolute Maximum Ratings

- Supply Voltage ---------- –0.3V to 7V
- LX Pin Switch Voltage ---------- –0.3V to 7V
- LDO Output Voltage ---------- –0.3V to (V_{DD} + 0.3V)
- Other I/O Pin Voltages ---------- –0.3V to (V_{DD} + 0.3V)
- LX Pin Switch Current ---------- 2.5A
- EXT Pin Driver Current ---------- 30mA
- LBO Current ---------- 30mA
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 ---------- 0.625W
- Package Thermal Resistance
  SOP-8, θ_{JA} ---------- 160°C/W
- Operating Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to +150°C

Electrical Characteristics

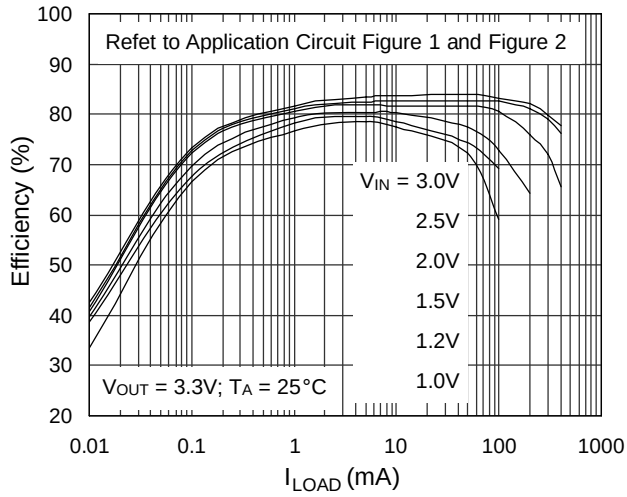
(V_{IN} = 1.5V, VDD set to 3.3V, Load Current = 0, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Start-UP Voltage		V_{ST}	I_L = 1mA	--	0.98	1.05	V
Operating VDD Range		V_{DD}	Start-up to I_{DD1} > 250μA	0.8	--	6.5 *	V
No Load Current I (V_{IN})		$I_{NO\ LOAD}$	V_{IN} = 1.5V, V_{OUT} = 3.3V	--	47	--	μA
Switch-off Current I (VDD)		$I_{SWITCH\ OFF}$	V_{IN} = 6V	--	17	--	μA
Shutdown Current I (V_{IN})		I_{OFF}	EN Pin = 0V, V_{IN} = 4.5V	--	0.1	1	μA
Feedback Reference Voltage		V_{REF}	Close Loop, V_{DD} = 3.3V	1.225	1.25	1.275	V
Feedback Reference Voltage for LDO	RT9262	V_{REF}	Close Loop, V_{DD} = 3.3V	0.843	0.86	0.877	V
LBI Pin Trip Point	RT9262A		V_{DD} = 3.3V	0.843	0.86	0.877	V
Switching Rate		F_S	V_{DD} = 3.3V	--	550	--	kHz
Maximum Duty		D_{MAX}	V_{DD} = 3.3V	--	92	--	%
LX ON Resistance			V_{DD} = 3.3V	--	0.25	--	Ω
Current Limit Setting		I_{LIM}	V_{DD} = 3.3V	--	2	--	A
EXT ON Resistance to VDD			V_{DD} = 3.3V	--	40	--	Ω
EXT ON Resistance to GND			V_{DD} = 3.3V	--	30	--	Ω
Line Regulation		ΔV_{LINE}	V_{IN} = 1.5 to 2.5V, I_L = 1mA	--	10	--	mV/V
Load Regulation		ΔV_{LOAD}	V_{IN} = 2.5V, I_L = 1 to 100mA	--	0.25	--	mV/mA
LDO PMOS ON Resistance	RT9262		V_{DD} = 3.3V	--	1	1.5	Ω
LDO Drop Out Voltage	RT9262	V_{DROP}	V_{DD} = 3.3V, I_L = 100mA	--	70	--	mV
LBO ON Resistance	RT9262A		V_{DD} = 3.3V	--	40	--	Ω
EN Pin Trip Level			V_{DD} = 3.3V	0.2	0.8	1.4	V
Temperature Stability for FB, LFB, LBI		T_S	Guaranteed by Design	--	50	--	ppm/°C
Thermal Shutdown		T_{SD}	Guaranteed by Design	--	165	--	°C
Thermal Shutdown Hysterises		ΔT_{SD}	Guaranteed by Design	--	10	--	°C

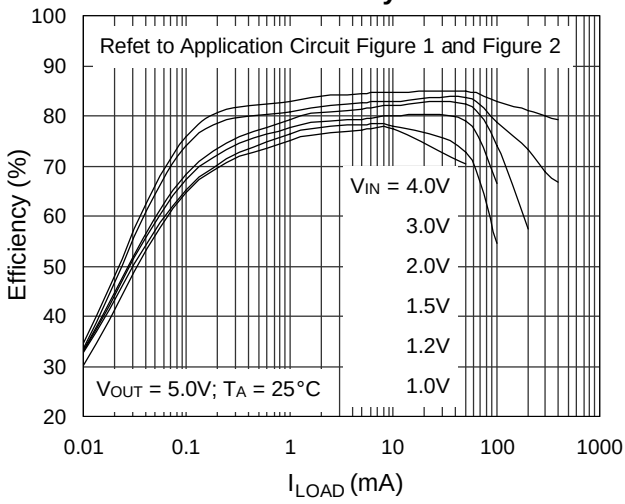
*** Note:** The EN pin shall be tied to VDD pin and inhibit to act the ON/OFF state whenever the VDD pin voltage may reach to 5.5V or above.

Typical Operating Characteristics

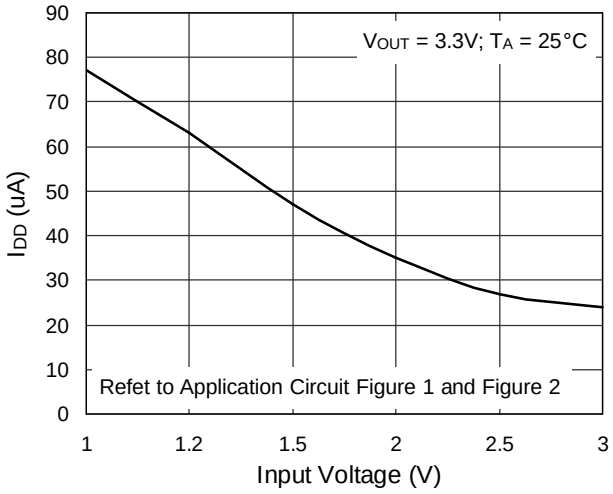
Efficiency



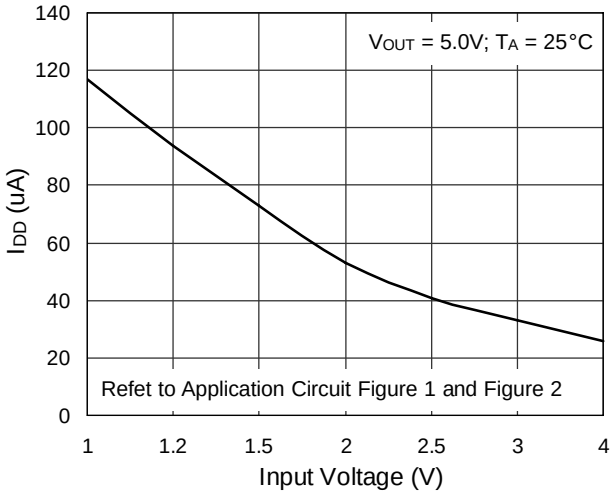
Efficiency



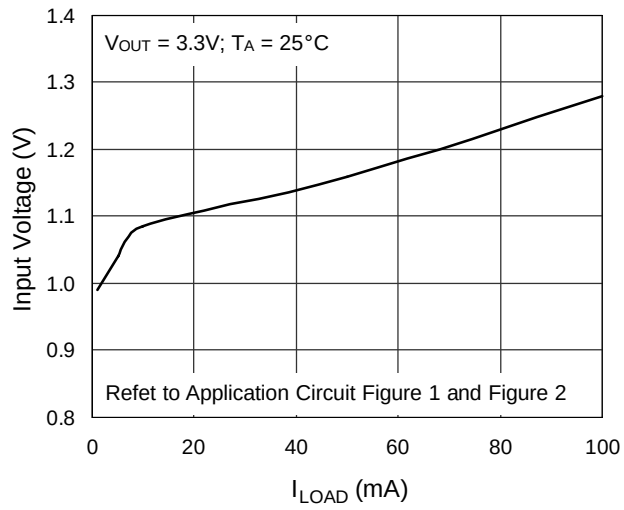
No Load Current



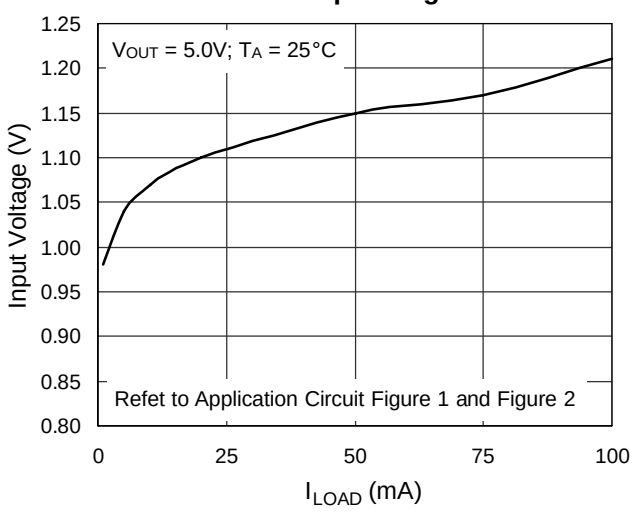
No Load Current



Start Up Voltage



Start Up Voltage



Applications Information

Output Voltage Setting

Referring to application circuits Figure 1 to Figuer 5 the output voltage of the switching regulator (V_{OUT1}) can be set with Equation (1).

The LDO output voltage (V_{OUT2} of RT9262) can be set with Equation (2).

$$V_{OUT1} = (1 + \frac{R1}{R2}) \times 1.25V \quad (1)$$

$$V_{OUT2} = (1 + \frac{R4}{R3}) \times 0.86V \quad (2)$$

And trip point of the low battery detector is 0.86V at LBI pin of RT9262A.

Feedback Loop Design

Referring to application circuits Figure 1 to Figure 5. The selection of R1, R2, R3, and R4 based on the trade-off between quiescent current consumption and interference immunity is stated below:

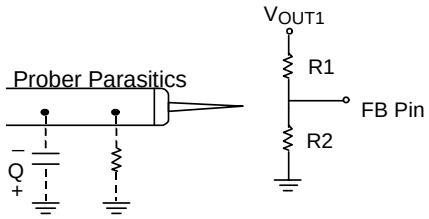
- Follow Equation (1) and Equation (2).
- Higher R reduces the quiescent current (Path current = 1.25V/R2, and 0.86V/R3), however resistors beyond 5MW are not recommended.
- Lower R gives better noise immunity, and is less sensitive to interference, layout parasitics, FB/LFB node leakage, and improper probing to FB/LFB pins.
- A proper value of feed forward capacitor parallel with R1 (or R4) on Figure 1 to Figure 5 can improve the noise immunity of the feedback loops, especially in an improper layout. An empirical suggestion is around 100pF ~ 1nF for feedback resistors of MW, and 10nF~ 0.1µF for feedback resistors of tens to hundreds kΩ.

For applications without standby or suspend modes, lower values of R1 to R4 are preferred. For applications concerning the current consumption in standby or suspend modes, the higher values of R1 to R4 are needed. Such "high impedance feedback loops" are sensitive to any interference, which require careful layout and avoid any interference, e.g. probing to FB/LFB pins.

PRECAUTION 1: Improper probing to FB or LFB pin will cause fluctuation at V_{OUT1} and V_{OUT2}. It may damage RT9262/A and system chips because V_{OUT1} may drastically rise to an over-rated level due to unexpected interference or parasitics being added to FB pin.

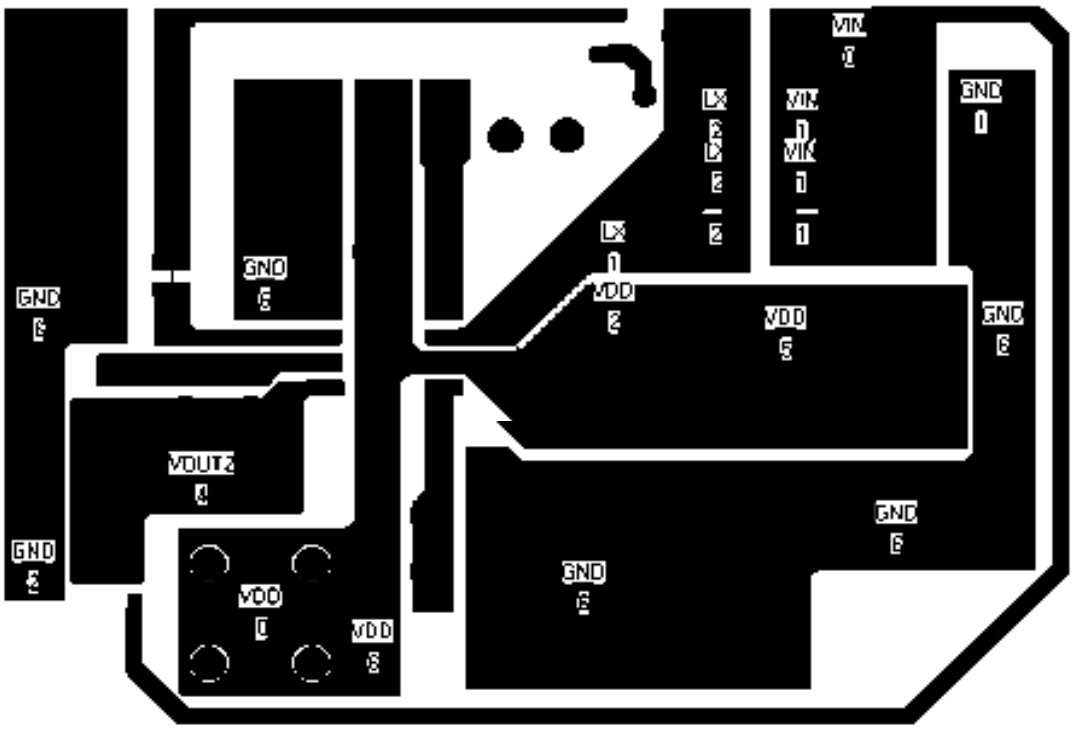
PRECAUTION 2: Disconnecting R1 or short circuit across R2 may also cause similar IC damage as described in precaution 1.

PRECAUTION 3: When large R values were used in feedback loops, any leakage in FB/LFB node may also cause V_{OUT1} and V_{OUT2} voltage fluctuation, and IC damage. To be especially highlight here is when the air moisture frozen and re-melt on the circuit board may cause several mA leakage between IC or component pins. So, when large R values are used in feedback loops, post coating, or some other moisture-preventing processes are recommended.

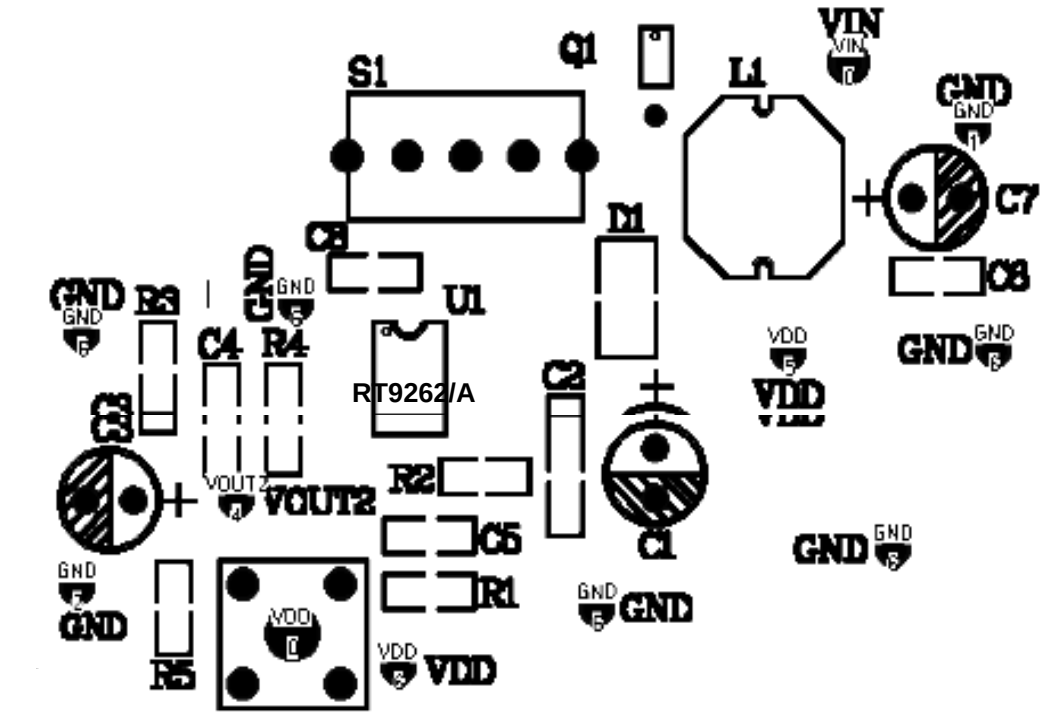


Layout Guide

- A full GND plane without gap break.
- V_{OUT1} to GND noise bypass–Short and wide connection for C2 to Pin1 and Pin6.
- V_{IN} to GND noise bypass - Add a 100µF capacitor close to L1 inductor, when VIN is not an idea voltage source.
- Minimized FB/LFB node copper area and keep far away from noise sources.
- Minimized parasitic capacitance connecting to LX and EXT nodes, which may cause additional switching loss.
- The following diagram is an example of 2-layer board layout for application circuits Figure 1 to Figure 4.

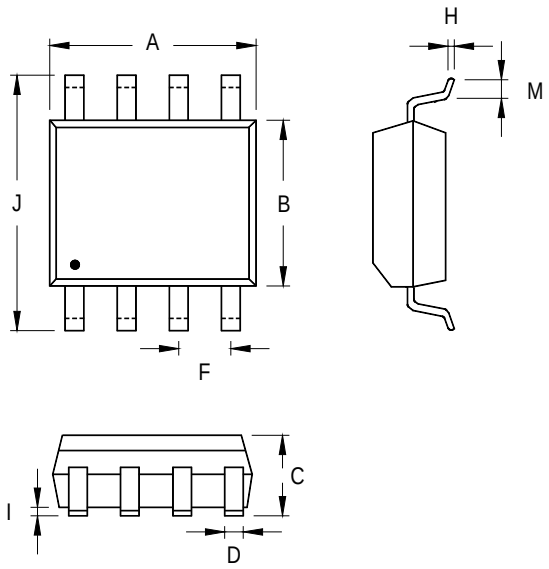


First Layer



Second Layer (Full GND Plane)

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

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