LMR12015/LMR12020 SIMPLE SWITCHER® 20Vin, 1.5A/2A Step-Down Voltage Regulator in WSON-10

Check for Samples: LMR12015, LMR12020

FEATURES

- **Space Saving 3 x 3 x 0.8 mm WSON-10 Package**
- **Input Voltage Range of 3V to 20V**
- **Output Voltage Range of 1V to 18V**
- **LMR12015 and LMR12020 Deliver 1.5A and 2A Maximum Output Current Respectively**
- **2 MHz Switching Frequency**
- **Frequency Synchronization from 1.00 MHz to 2.35 MHz**
- **70 nA Shutdown Current**
- **1% Voltage Reference Accuracy**
- **Peak Current Mode PWM Operation**
- **Thermal Shutdown**
- **Internally Compensated**
- **Internal Soft-Start**
- **WEBENCH® Enabled**

PERFORMANCE BENEFITS

- **Tight Accuracy for Powering Digital ICs**
- **Extremely Easy to Use**
- **Tiny Overall Solution Reduces System Cost**

APPLICATIONS

- **Point-of-Load Conversions from 3.3V, 5V and 12V Rails**
- **Space Constrained Applications**

DESCRIPTION

The LMR12015/20 regulator is a monolithic, high frequency, PWM step-down DC-DC converter in a 10-pin WSON package. It contains all the active functions to provide local DC-DC conversion with fast transient response and accurate regulation in the smallest possible PCB area.

With a minimum of external components the LMR12015/20 is easy to use. The ability to drive 1.5/2A loads respectively, with an internal 150 mΩ NMOS switch results in the best power density available. The control circuitry allows for on-times as low as 65 ns, thus supporting exceptionally high frequency conversion. Switching frequency is internally set to 2 MHz and synchronizable from 1 to 2.35 MHz, which allows the use of extremely small surface mount inductors and chip capacitors. Even though the operating frequency is very high, efficiencies up to 90% are easy to achieve. External shutdown is included featuring an ultra-low shutdown current of 70 nA. The LMR12015/20 utilizes peak current mode control and internal compensation to provide high-performance regulation over a wide range of operating conditions. Additional features include internal soft-start circuitry to reduce inrush current, pulse-by-pulse current limit, thermal shutdown, and output over-voltage protection.

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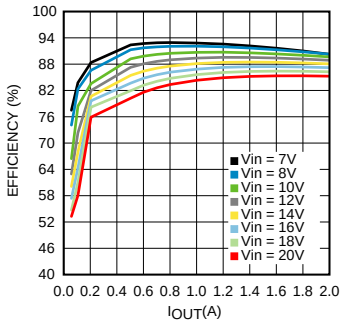
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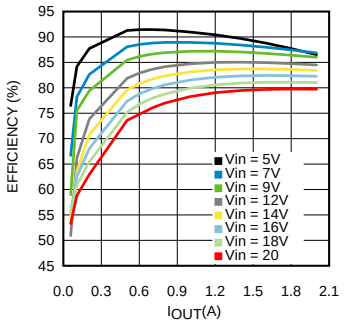
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System Performance

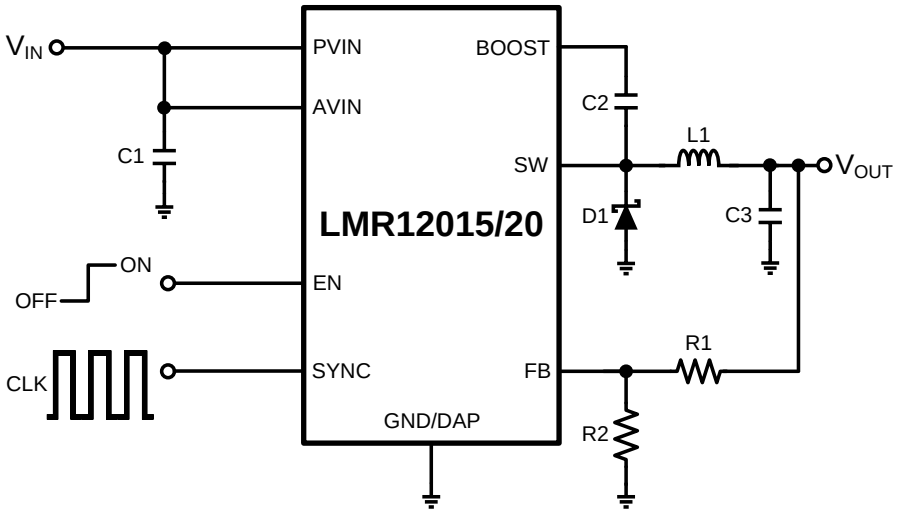
Efficiency vs Load Current
LMR12015/20 V_{OUT} = 5V, f_{sw} = 2 MHz



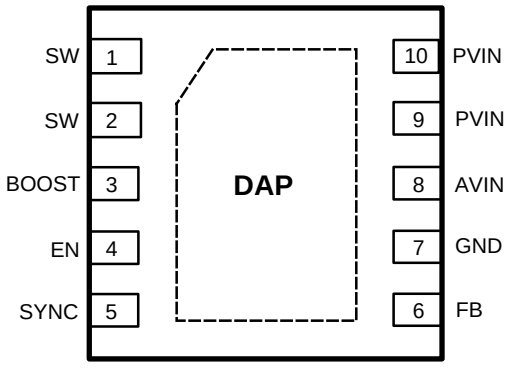
Efficiency vs Load Current
LMR12015/20 V_{OUT} = 3.3V, f_{sw} = 2 MHz



Typical Application Circuit



Connection Diagram



10 - Lead WSON (Top View)
See Package Number DSC

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PIN DESCRIPTIONS

Pin	Name	Function
1,2	SW	Output switch. Connects to the inductor, catch diode, and bootstrap capacitor.
3	BOOST	Boost voltage that drives the internal NMOS control switch. A bootstrap capacitor is connected between the BOOST and SW pins.
4	EN	Enable control input. Logic high enables operation. Do not allow this pin to float or be greater than V_{IN} + 0.3V.
5	SYNC	Frequency synchronization input. Drive this pin with an external clock or pulse train. Ground it to use the internal clock.
6	FB	Feedback pin. Connect FB to the external resistor divider to set output voltage.
7	GND	Signal and Power Ground pin. Place the bottom resistor of the feedback network as close as possible to this pin for accurate regulation.
8	AVIN	Supply voltage for the control circuitry.
9,10	PVIN	Supply voltage for output power stage. Connect a bypass capacitor to this pin.
DAP	GND	Signal / Power Ground and thermal connection. Tie this directly to GND (pin 7). See APPLICATION INFORMATION regarding optimum thermal layout.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

AVIN, PVIN	-0.5V to 24V
SW Voltage	-0.5V to 24V
Boost Voltage	-0.5V to 28V
Boost to SW Voltage	-0.5V to 6.0V
FB Voltage	-0.5V to 3.0V
SYNC Voltage	-0.5V to 6.0V
EN Voltage	-0.5V to (V_{IN} + 0.3V)
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
ESD Susceptibility(3)	2kV
Soldering Information Infrared Reflow (5sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the recommended Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5 kΩ in series with 100 pF.

Operating Ratings(1)

AVIN, PVIN	3V to 20V
SW Voltage	-0.5V to 20V
Boost Voltage	-0.5V to 24V
Boost to SW Voltage	3.0V to 5.5V
Junction Temperature Range	-40°C to +125°C
Thermal Resistance (θ_{JA}) WSON (DSC)(2)	33°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the recommended Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and should not be operated beyond such conditions.
(2) All numbers apply for packages soldered directly onto a 3" x 3" PC board with 2oz. copper on 4 layers in still air.

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Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those in **boldface type** apply over the full **Operating Temperature Range** (T_J = -40°C to 125°C). V_{IN} = 12V, and V_{BOOST} - V_{SW} = 4.3V unless otherwise specified. Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM PARAMETERS						
V_{FB}	Feedback Voltage	T_J = 0°C to 85°C	0.990	1.0	1.010	V
		T_J = -40°C to 125°C	**0.984**	1.0	**1.014**	
$\Delta V_{FB}/\Delta V_{IN}$	Feedback Voltage Line Regulation	V_{IN} = 3V to 20V		0.003		% / V
I_{FB}	Feedback Input Bias Current			20	**100**	nA
OVP	Over Voltage Protection, V_{FB} at which PWM Halts.			1.13		V
UVLO	Undervoltage Lockout	V_{IN} Rising until V_{SW} is Switching	**2.60**	2.75	**2.90**	V
	UVLO Hysteresis	V_{IN} Falling from UVLO	**0.30**	0.47	**0.6**	
SS	Soft Start Time		0.5	1	1.5	ms
I_Q	Quiescent Current, $I_Q = I_{Q_AVIN} + I_{Q_PVIN}$	V_{FB} = 1.1 (not switching)		2.4		mA
	Quiescent Current, $I_Q = I_{Q_AVIN} + I_{Q_PVIN}$	V_{EN} = 0V (shutdown)		70		nA
I_{BOOST}	Boost Pin Current	f_{SW}= 2 MHz		8.2	**10**	mA
		f_{SW}= 1 MHz		4.4	6	
OSCILLATOR						
f_{SW}	Switching Frequency	SYNC = GND	**1.75**	2	**2.3**	MHz
V_{FB_FOLD}	FB Pin Voltage where SYNC input is overridden.			0.53		V
f_{FOLD_MIN}	Frequency Foldback Minimum	V_{FB} = 0V		220	250	kHz
LOGIC INPUTS (EN, SYNC)						
f_{SYNC}	SYNC Frequency Range		1		2.35	MHz
V_{IL}	EN, SYNC Logic low threshold	Logic Falling Edge			0.4	V
V_{IH}	EN, SYNC Logic high threshold	Logic Rising Edge	1.8			
t_{SYNC_HIGH}	SYNC, Time Required above V_{IH} to Ensure a Logical High.		100			ns
t_{SYNC_LOW}	SYNC, Time Required below V_{IL} to Ensure a Logical Low.		100			ns
I_{SYNC}	SYNC Pin Current	V_{SYNC} < 5V		20		nA
I_{EN}	Enable Pin Current	V_{EN} = 3V		6	15	µA
		$V_{IN} = V_{EN}$ = 20V		50	100	
INTERNAL MOSFET						
$R_{DS(ON)}$	Switch ON Resistance			150	**320**	mΩ
I_{CL}	Switch Current Limit	LMR12020	**2.5**		**4.0**	A
		LMR12015	**2.0**		**3.7**	
D_{MAX}	Maximum Duty Cycle	SYNC = GND	**85**	93		%
t_{MIN}	Minimum on time			65		ns
I_{SW}	Switch Leakage Current			40		nA
BOOST LDO						
V_{LDO}	Boost LDO Output Voltage			3.9		V
THERMAL						
T_{SHDN}	Thermal Shutdown Temperature (1)	Junction temperature rising		165		°C
	Thermal Shutdown Hysteresis	Junction temperature hysteresis		15		°C

(1) Thermal shutdown will occur if the junction temperature exceeds 165°C. The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$.

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TYPICAL PERFORMANCE CHARACTERISTICS

All curves taken at V_{IN} = 12V, V_{BOOST} - V_{SW} = 4.3V and T_A = 25°C, unless specified otherwise.

Efficiency vs Load Current
V_{OUT} = 5V, f_{SW} = 2 MHz
Refer to Figure 37

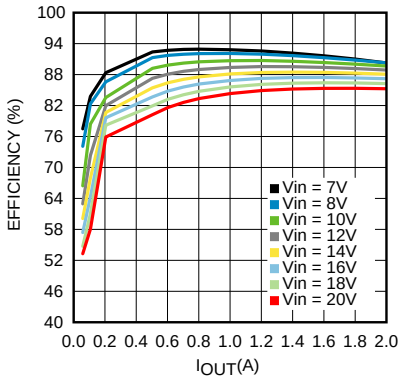


Figure 1.

Load Transient
V_{OUT} = 5V, I_{OUT} = 100 mA - 2A @ slewrate = 2A / µs
Refer to Figure 37

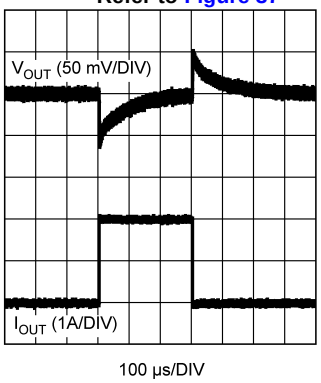


Figure 2.

Efficiency vs Load Current
V_{OUT} = 3.3V, f_{SW} = 2 MHz
Refer to Figure 39

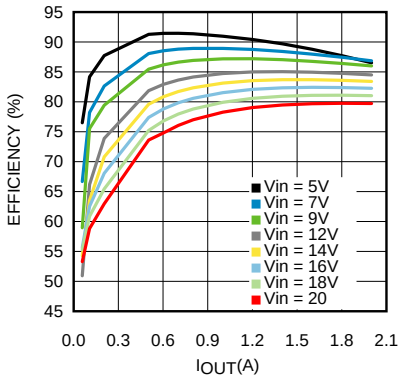


Figure 3.

Load Transient
V_{OUT} = 3.3V, I_{OUT} = 100 mA - 2A @ slewrate = 2A / µs
Refer to Figure 39

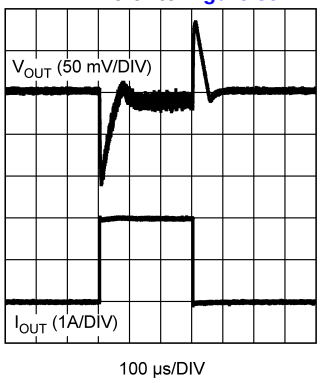


Figure 4.

Efficiency vs Load Current
V_{OUT} = 1.8V, f_{SW} = 2 MHz
Refer to Figure 40

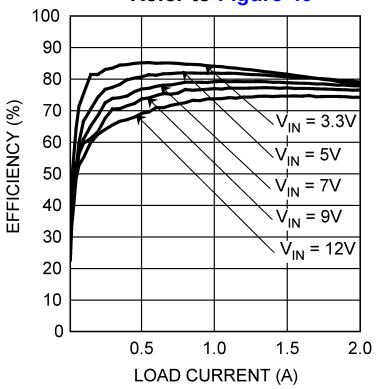


Figure 5.

Load Transient
V_{OUT} = 1.8V, I_{OUT} = 100 mA - 2A @ slewrate = 2A / µs
Refer to Figure 40

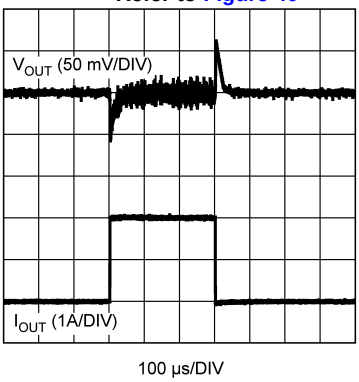


Figure 6.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

All curves taken at V_{IN} = 12V, V_{BOOST} - V_{SW} = 4.3V and T_A = 25°C, unless specified otherwise.

Line Transient
V_{IN} = 10 to 15V, V_{OUT} = 3.3V, no C_{FF}
Refer to Figure 39

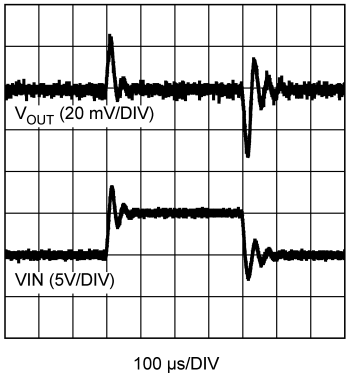


Figure 7.

Line Transient
V_{IN} = 10 to 15V, V_{OUT} = 3.3V
Refer to Figure 38

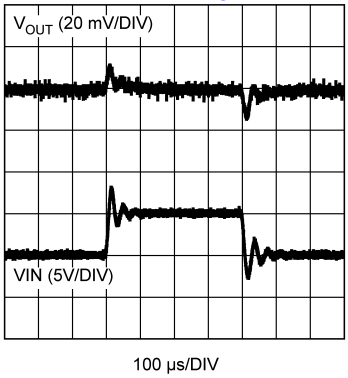


Figure 8.

Short Circuit

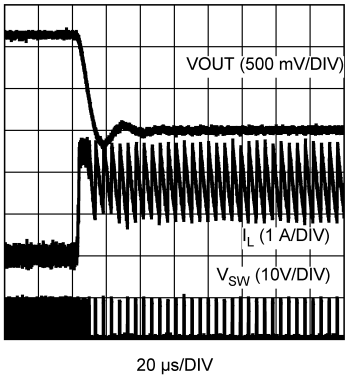


Figure 9.

Short Circuit Release

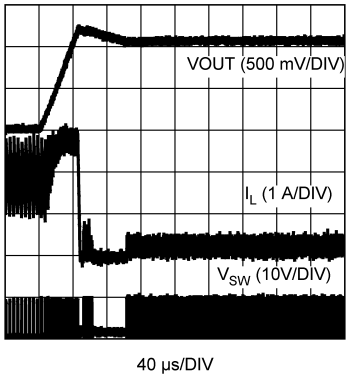


Figure 10.

Soft Start

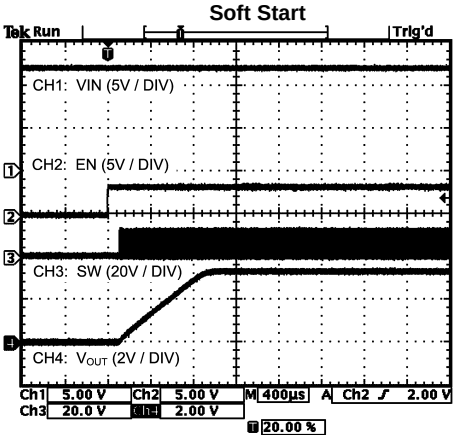


Figure 11.

Soft Start with EN Tied to V_{IN}

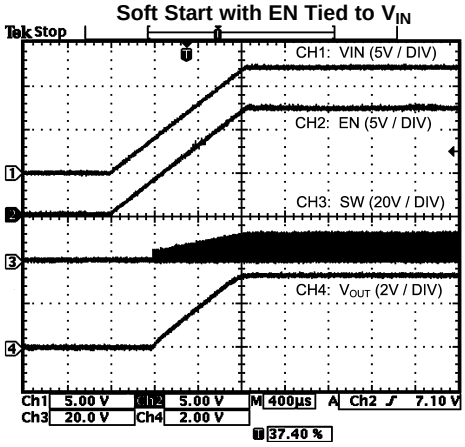


Figure 12.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

All curves taken at V_{IN} = 12V, V_{BOOST} - V_{SW} = 4.3V and T_A = 25°C, unless specified otherwise.

V_{IN} = 12V, V_{OUT} = 5 V, L = 2.2 µH, C_{OUT} = 44 µF Iout =1A

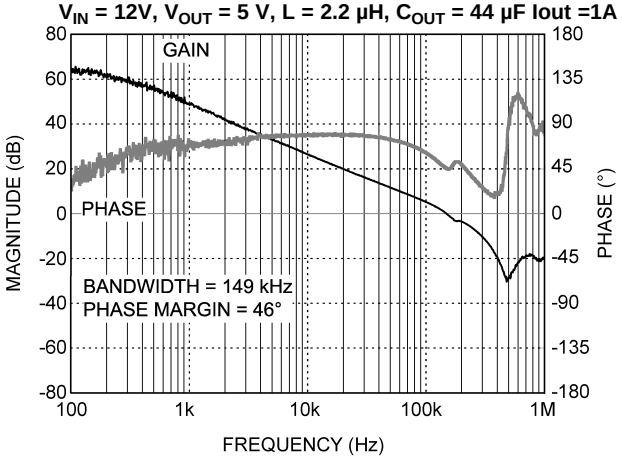


Figure 13.

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5 µH C_{OUT} = 44 µF Iout =1A

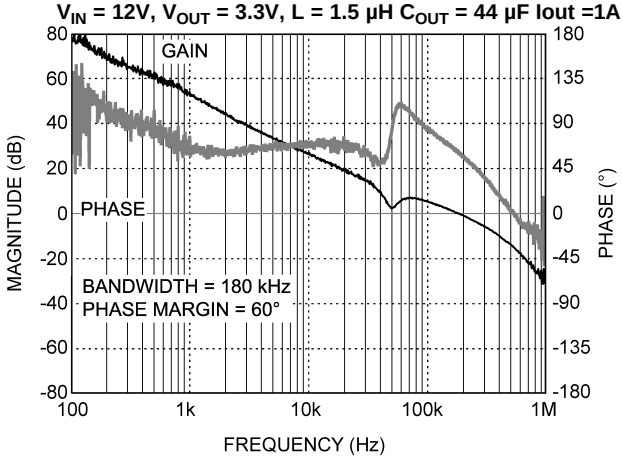


Figure 14.

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1.0 µH C_{OUT} = 44 µF Iout =1A

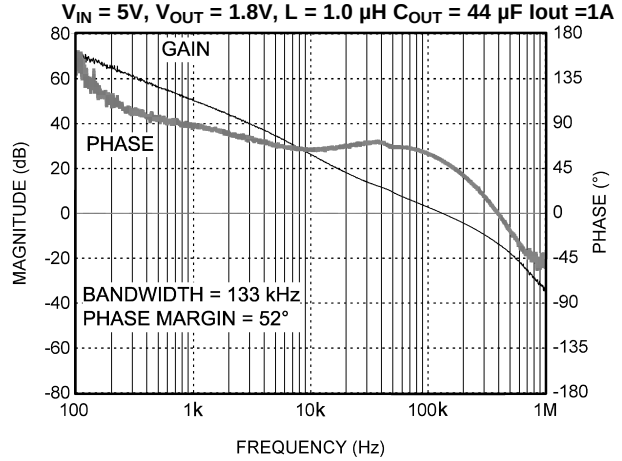


Figure 15.

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.56 µH C_{OUT} = 68 µF Iout =1A

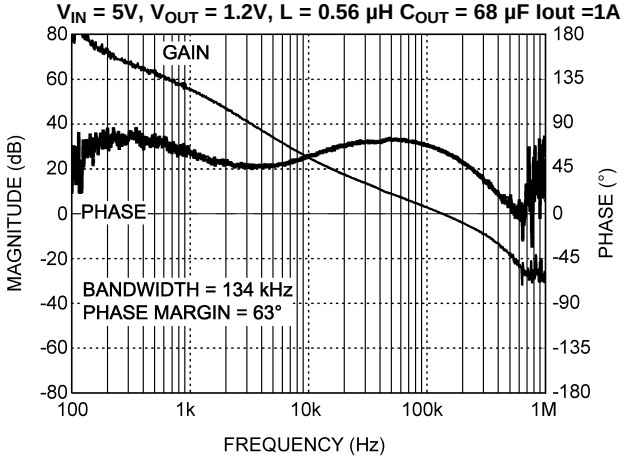


Figure 16.

Sync Functionality

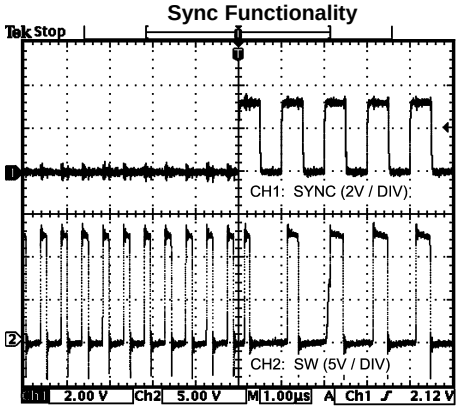


Figure 17.

Loss of Synchronization

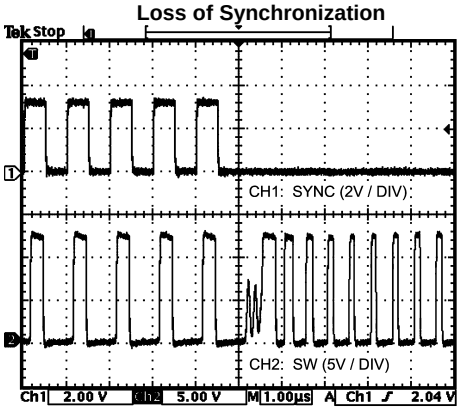


Figure 18.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

All curves taken at V_{IN} = 12V, V_{BOOST} - V_{SW} = 4.3V and T_A = 25°C, unless specified otherwise.

Oscillator Frequency vs Temperature
V_{SYNC} = GND

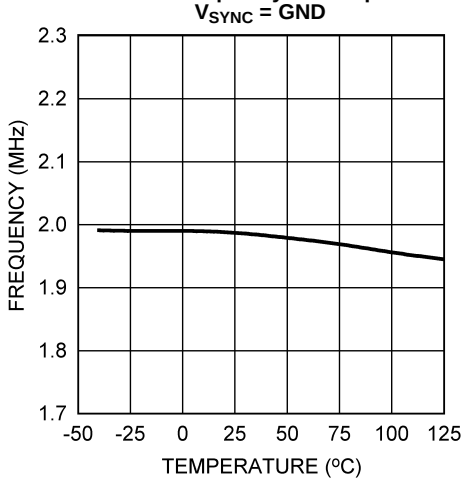


Figure 19.

Oscillator Frequency vs V_{FB}
V_{SYNC} = GND

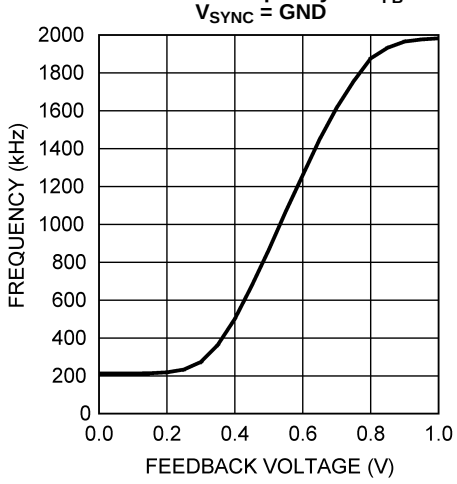


Figure 20.

V_{FB} vs Temperature

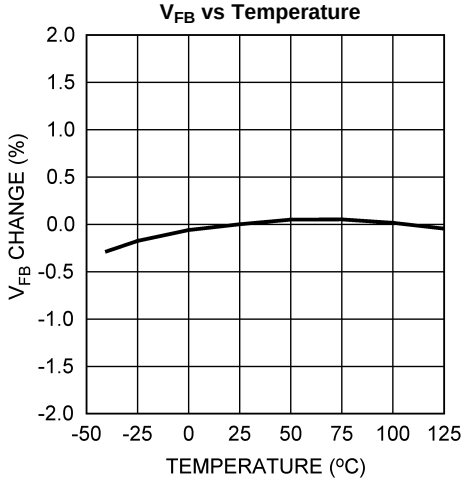


Figure 21.

V_{FB} vs V_{IN}

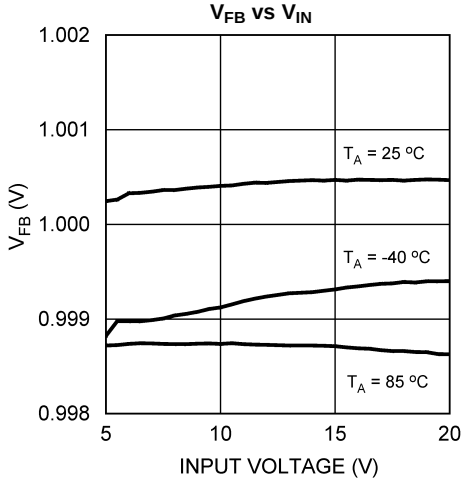


Figure 22.

Current Limit vs Temperature
V_{IN} = 12V

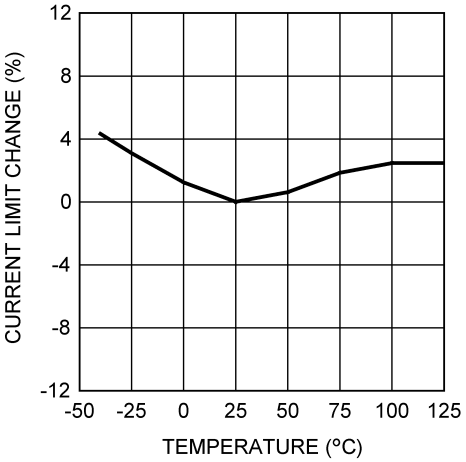


Figure 23.

R_{DSON} vs Temperature

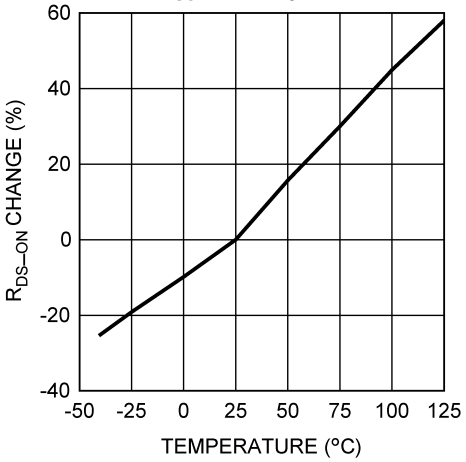


Figure 24.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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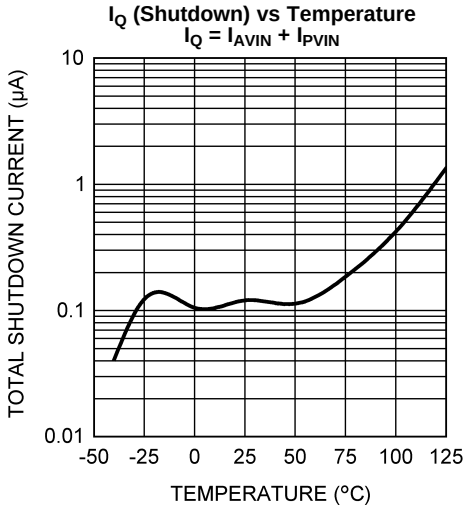


Figure 25.

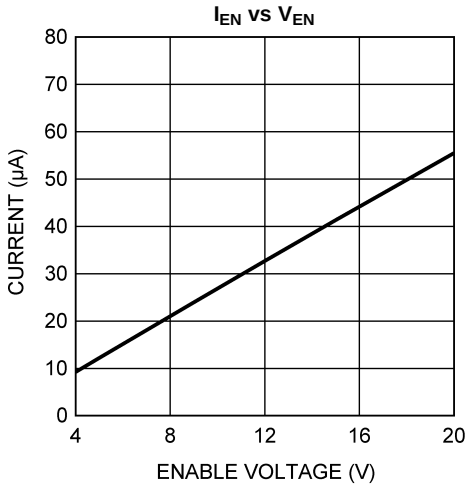
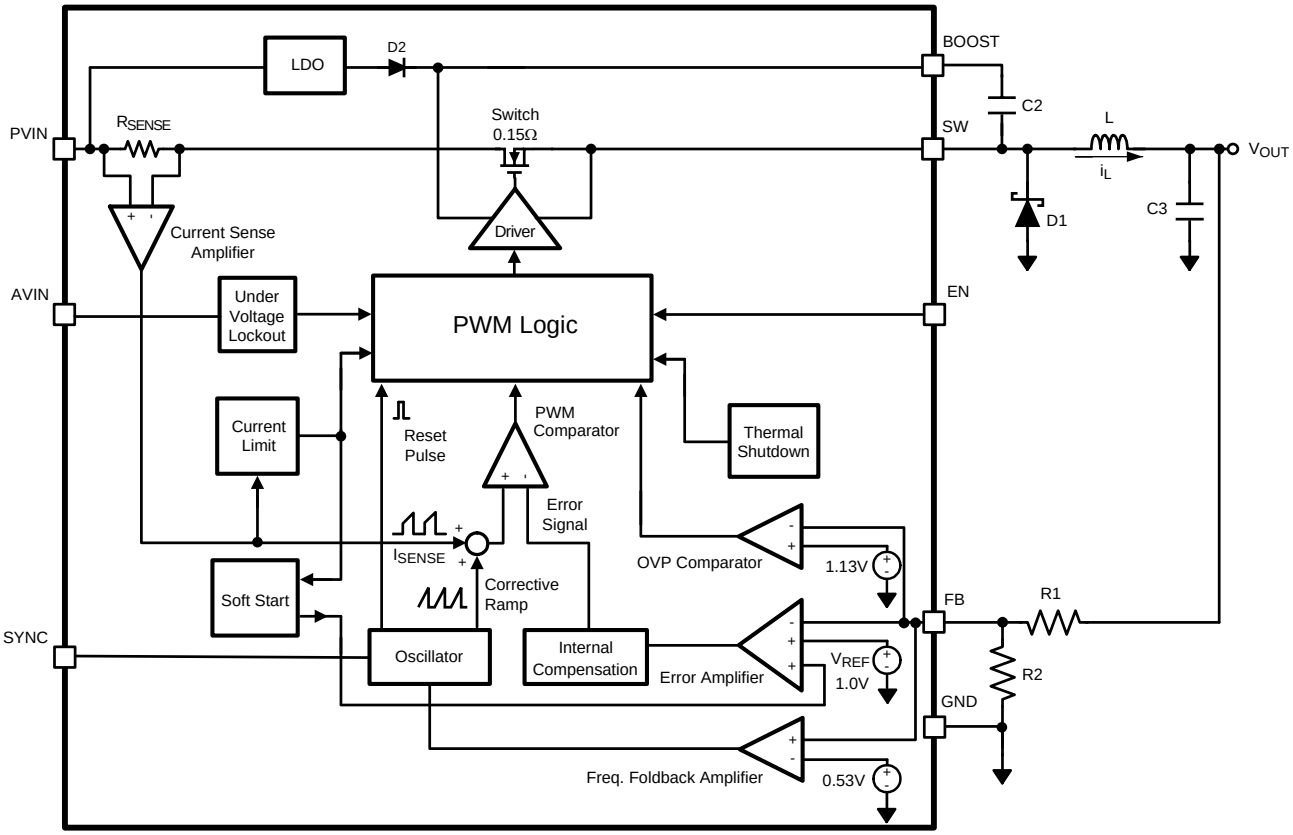


Figure 26.

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Block Diagram



APPLICATION INFORMATION

THEORY OF OPERATION

The LMR12015/20 is a constant-frequency, peak current-mode PWM buck regulator IC that delivers a 1.5 or 2A load current. The regulator has a preset switching frequency of 2 MHz. This high frequency allows the LMR12015/20 to operate with small surface mount capacitors and inductors, resulting in a DC-DC converter that requires a minimum amount of board space. The LMR12015/20 is internally compensated, which reduces design time, and requires few external components.

The following operating description of the LMR12015/20 will refer to the Block Diagram and to the waveforms in Figure 27. The LMR12015/20 supplies a regulated output voltage by switching the internal NMOS switch at a constant frequency and varying the duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal NMOS switch. During this on-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (i_L) increases with a linear slope. The current-sense amplifier measures i_L, which generates an output proportional to the switch current typically called the sense signal. The sense signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage (V_{FB}) and V_{REF}. When the output of the PWM comparator goes high, the switch turns off until the next switching cycle begins. During the switch off-time (t_{OFF}), inductor current discharges through the catch diode D1, which forces the SW pin (V_{SW}) to swing below ground by the forward voltage (V_{D1}) of the catch diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

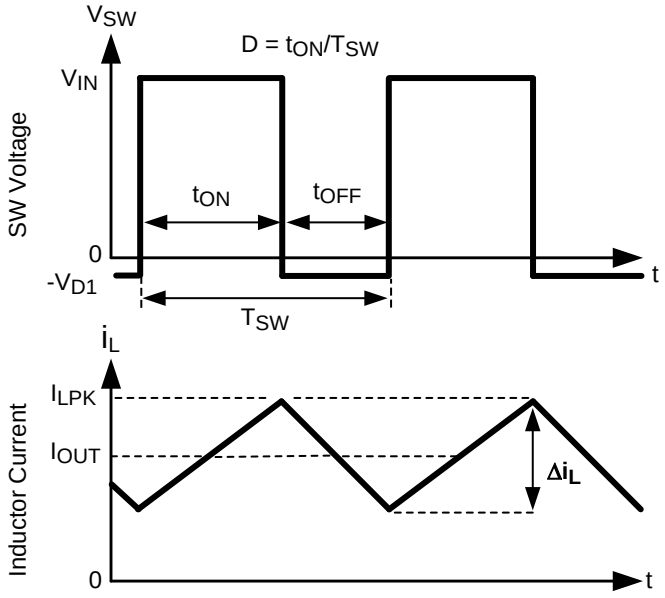


Figure 27. LMR12015/20 Waveforms of SW Pin Voltage and Inductor Current

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BOOST FUNCTION

Capacitor C_2 in Block Diagram, commonly referred to as C_{BOOST}, is used to store a voltage V_{BOOST}. When the LMR12015/20 starts up, an internal LDO charges C_{BOOST} ,via an internal diode, to a voltage sufficient to turn the internal NMOS switch on. The gate drive voltage supplied to the internal NMOS switch is V_{BOOST} - V_{SW}.

During a normal switching cycle, when the internal NMOS control switch is off (t_{OFF}) (refer to Figure 27), V_{BOOST} equals V_{LDO} minus the forward voltage of the internal diode (V_{D2}). At the same time the inductor current (i_L) forward biases the catch diode D1 forcing the SW pin to swing below ground by the forward voltage drop of the catch diode (V_{D1}). Therefore, the voltage stored across C_{BOOST} is

$$V_{BOOST} - V_{SW} = V_{LDO} - V_{D2} + V_{D1} \quad (1)$$

Thus,

$$V_{BOOST} = V_{SW} + V_{LDO} - V_{D2} + V_{D1} \quad (2)$$

When the NMOS switch turns on (t_{ON}), the switch pin rises to

$$V_{SW} = V_{IN} – (R_{DSON} \times I_L), \quad (3)$$

reverse biasing D1, and forcing V_{BOOST} to rise. The voltage at V_{BOOST} is then

$$V_{BOOST} = V_{IN} – (R_{DSON} \times I_L) + V_{LDO} – V_{D2} + V_{D1} \quad (4)$$

which is approximately

$$V_{IN} + V_{LDO} - 0.4V \quad (5)$$

V_{BOOST} has pulled itself up by its "bootstraps", or boosted to a higher voltage.

LOW INPUT VOLTAGE CONSIDERATIONS

When the input voltage is below 5V and the duty cycle is greater than 75 percent, the gate drive voltage developed across C_{BOOST} might not be sufficient for proper operation of the NMOS switch. In this case, C_{BOOST} should be charged via an external Schottky diode attached to a 5V voltage rail, see Figure 28. This ensures that the gate drive voltage is high enough for proper operation of the NMOS switch in the triode region. Maintain V_{BOOST} - V_{SW} less than the 6V absolute maximum rating.

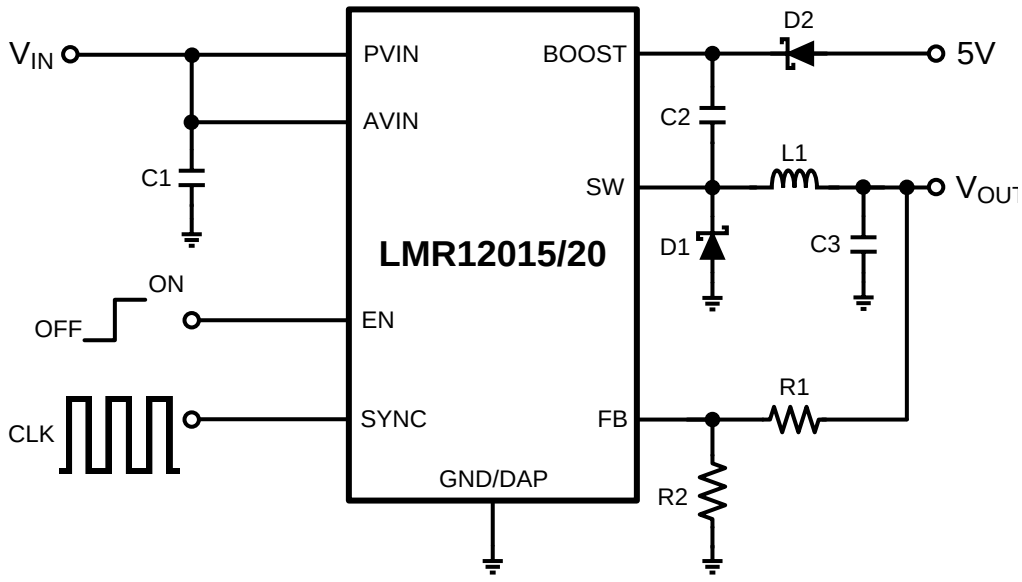


Figure 28. External Diode Charges C_{BOOST}

HIGH OUTPUT VOLTAGE CONSIDERATIONS

When the output voltage is greater than 3.3V, a minimum load current is needed to charge C_{BOOST}, see Figure 29. The minimum load current forward biases the catch diode D1 forcing the SW pin to swing below ground. This allows C_{BOOST} to charge, ensuring that the gate drive voltage is high enough for proper operation. The minimum load current depends on many factors including the inductor value.

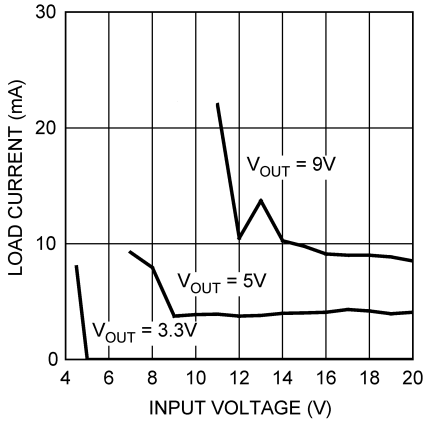


Figure 29. Minimum Load Current for L = 1.5 µH

ENABLE PIN / SHUTDOWN MODE

Connect the EN pin to a voltage source greater than 1.8V to enable operation of the LMR12015/20. Apply a voltage less than 0.4V to put the part into shutdown mode. In shutdown mode the quiescent current drops to typically 70 nA. Switch leakage adds another 40 nA from the input supply. For proper operation, the LMR12015/20 EN pin should never be left floating, and the voltage should never exceed V_{IN} + 0.3V.

The simplest way to enable the operation of the LMR12015/20 is to connect the EN pin to AVIN which allows self start-up of the LMR12015/20 when the input voltage is applied.

When the rise time of V_{IN} is longer than the soft-start time of the LMR12015/20 this method may result in an overshoot in output voltage. In such applications, the EN pin voltage can be controlled by a separate logic signal, or tied to a resistor divider, which reaches 1.8V after V_{IN} is fully established (see Figure 30). This will minimize the potential for output voltage overshoot during a slow V_{IN} ramp condition. Use the lowest value of V_{IN} , seen in your application when calculating the resistor network, to ensure that the 1.8V minimum EN threshold is reached.

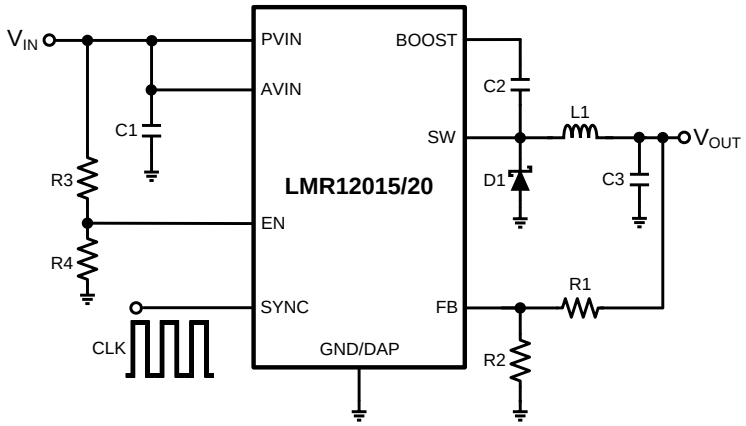


Figure 30. Resistor Divider on EN

$$R3 = \left(\frac{V_{IN}}{1.8} - 1 \right) \times R4 \quad (6)$$

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FREQUENCY SYNCHRONIZATION

The LMR12015/20 switching frequency can be synchronized to an external clock, between 1.00 and 2.35 MHz, applied at the SYNC pin. At the first rising edge applied to the SYNC pin, the internal oscillator is overridden and subsequent positive edges will initiate switching cycles. If the external SYNC signal is lost during operation, the LMR12015/20 will revert to its internal 2 MHz oscillator within 1.5 µs. To disable Frequency Synchronization and utilize the internal 2 MHz oscillator, connect the SYNC pin to GND.

The SYNC pin gives the designer the flexibility to optimize their design. A lower switching frequency can be chosen for higher efficiency. A higher switching frequency can be chosen to keep EMI out of sensitive ranges such as the AM radio band. Synchronization can also be used to eliminate beat frequencies generated by the interaction of multiple switching power converters. Synchronizing multiple switching power converters will result in cleaner power rails.

The selected switching frequency (f_{SYNC}) and the minimum on-time (t_{MIN}) limit the minimum duty cycle (D_{MIN}) of the device.

$$D_{MIN} = t_{MIN} \times f_{SYNC} \quad (7)$$

Operation below D_{MIN} is not reccomended. The LMR12015/20 will skip pulses to keep the output voltage in regulation, and the current limit is not ensured. The switching is in phase but no longer at the same switching frequency as the SYNC signal.

CURRENT LIMIT

The LMR12015/20 use cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 2.0A min (LMR12015) or 2.5A min (LMR12020) , and turns off the switch until the next switching cycle begins.

FREQUENCY FOLDBACK

The LMR12015/20 employs frequency foldback to protect the device from current run-away during output short-circuit. Once the FB pin voltage falls below regulation, the switch frequency will smoothly reduce with the falling FB voltage until the switch frequency reaches 220 kHz (typ). If the device is synchronized to an external clock, synchronization is disabled until the FB pin voltage exceeds 0.53V

SOFT-START

The LMR12015/20 has a fixed internal soft-start of 1 ms (typ). During soft-start, the error amplifier's reference voltage ramps from 0.0 V to its nominal value of 1.0 V in approximately 1 ms. This forces the regulator output to ramp in a controlled fashion, which helps reduce inrush current. Upon soft-start the part will initially be in frequency foldback and the frequency will rise as FB rises. The regulator will gradually rise to 2 MHz. The LMR12015/20 will allow synchronization to an external clock at FB > 0.53V.

OUTPUT OVERVOLTAGE PROTECTION

The overvoltage comparator turns off the internal power NFET when the FB pin voltage exceeds the internal reference voltage by 13% ($V_{FB} > 1.13 * V_{REF}$). With the power NFET turned off the output voltage will decrease toward the regulation level.

UNDERVOLTAGE LOCKOUT

Undervoltage lockout (UVLO) prevents the LMR12015/20 from operating until the input voltage exceeds 2.75V(typ).

The UVLO threshold has approximately 470 mV of hysteresis, so the part will operate until V_{IN} drops below 2.28V(typ). Hysteresis prevents the part from turning off during power up if V_{IN} has finite impedance.

THERMAL SHUTDOWN

Thermal shutdown limits total power dissipation by turning off the internal NMOS switch when the IC junction temperature exceeds 165°C (typ). After thermal shutdown occurs, hysteresis prevents the internal NMOS switch from turning on until the junction temperature drops to approximately 150°C.

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Design Guide

INDUCTOR SELECTION

Inductor selection is critical to the performance of the LMR12015/20. The selection of the inductor affects stability, transient response and efficiency. A key factor in inductor selection is determining the ripple current (Δi_L) (see Figure 27).

The ripple current (Δi_L) is important in many ways.

First, by allowing more ripple current, lower inductance values can be used with a corresponding decrease in physical dimensions and improved transient response. On the other hand, allowing less ripple current will increase the maximum achievable load current and reduce the output voltage ripple (see Output Capacitor section for more details on calculating output voltage ripple). Increasing the maximum load current is achieved by ensuring that the peak inductor current (I_{LPK}) never exceeds the minimum current limit of 2.0A min (LMR12015) or 2.5A min (LMR12020) .

$$I_{LPK} = I_{OUT} + \Delta i_L / 2 \quad (8)$$

Secondly, the slope of the ripple current affects the current control loop. The LMR12015/20 has a fixed slope corrective ramp. When the slope of the current ripple becomes significantly less than the converter's corrective ramp (see Block Diagram), the inductor pole will move from high frequencies to lower frequencies. This negates one advantage that peak current-mode control has over voltage-mode control, which is, a single low frequency pole in the power stage of the converter. This can reduce the phase margin, crossover frequency and potentially cause instability in the converter. Contrarily, when the slope of the ripple current becomes significantly greater than the converter's corrective ramp, resonant peaking can occur in the control loop. This can also cause instability (Sub-Harmonic Oscillation) in the converter. For the power supply designer this means that for lower switching frequencies the current ripple must be increased to keep the inductor pole well above crossover. It also means that for higher switching frequencies the current ripple must be decreased to avoid resonant peaking.

With all these factors, how is the desired ripple current selected? The ripple ratio (r) is defined as the ratio of inductor ripple current (Δi_L) to output current (I_{OUT}), evaluated at maximum load:

$$r = \frac{\Delta i_L}{I_{OUT}} \quad (9)$$

A good compromise between physical size, transient response and efficiency is achieved when we set the ripple ratio between 0.2 and 0.4. The recommended ripple ratio vs. duty cycle shown below (see Figure 31) is based upon this compromise and control loop optimizations. Note that this is just a guideline. Please see Application note AN-1197 SNVA038 for further considerations.

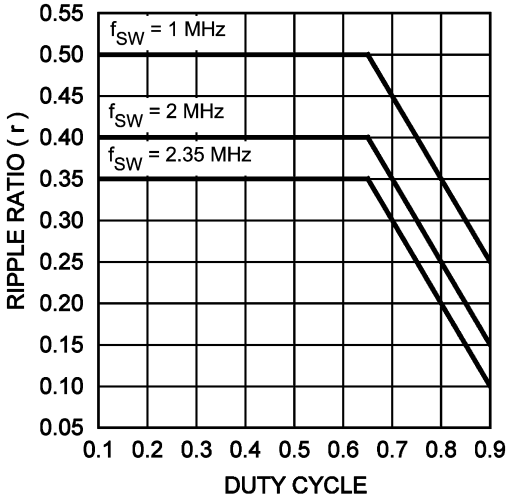


Figure 31. Recommended Ripple Ratio Vs. Duty Cycle

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The Duty Cycle (D) can be approximated quickly using the ratio of output voltage (V_{OUT}) to input voltage (V_{IN}):

$$D = \frac{V_{OUT}}{V_{IN}} \quad (10)$$

The application's lowest input voltage should be used to calculate the ripple ratio. The catch diode forward voltage drop (V_{D1}) and the voltage drop across the internal NFET (V_{DS}) must be included to calculate a more accurate duty cycle. Calculate D by using the following formula:

$$D = \frac{V_{OUT} + V_{D1}}{V_{IN} + V_{D1} - V_{DS}} \quad (11)$$

V_{DS} can be approximated by:

$$V_{DS} = I_{OUT} \times R_{DS(ON)} \quad (12)$$

The diode forward drop (V_{D1}) can range from 0.3V to 0.5V depending on the quality of the diode. The lower V_{D1} is, the higher the operating efficiency of the converter.

Now that the ripple current or ripple ratio is determined, the required inductance is calculated by:

$$L = \frac{V_{OUT} + V_{D1}}{I_{OUT} \times r \times f_{SW}} \times (1-D_{MIN}) \quad (13)$$

where D_{MIN} is the duty cycle calculated with the maximum input voltage, f_{sw} is the switching frequency, and I_{OUT} is the maximum output current of 2A. Using I_{OUT} = 2A will minimize the inductor's physical size.

INDUCTOR CALCULATION EXAMPLE

Operating conditions for the LMR12015/20 are:

$$V_{IN} = 7 - 16V \quad (14)$$

$$f_{SW} = 2\ MHz \quad (15)$$

$$V_{OUT} = 3.3V \quad (16)$$

$$V_{D1} = 0.5V \quad (17)$$

$$I_{OUT} = 2A \quad (18)$$

First the maximum duty cycle is calculated.

$$D_{MAX} = (V_{OUT} + V_{D1}) / (V_{IN} + V_{D1} - V_{DS}) = (3.3V + 0.5V) / (7V + 0.5V - 0.30V) = 0.528 \quad (19)$$

Using Figure 31 gives us a recommended ripple ratio = 0.4.

Now the minimum duty cycle is calculated.

$$D_{MIN} = (V_{OUT} + V_{D1}) / (V_{IN} + V_{D1} - V_{DS}) = (3.3V + 0.5V) / (16V + 0.5V - 0.30V) = 0.235 \quad (20)$$

The inductance can now be calculated.

$$L = (1 - D_{MIN}) \times (V_{OUT} + V_{D1}) / (I_{OUT} \times r \times f_{sw}) = (1 - 0.235) \times (3.3V + .5V) / (2A \times 0.4 \times 2\ MHz) = 1.817\ \mu H \quad (21)$$

This is close to the standard inductance value of 1.8 µH. This leads to a 1% deviation from the recommended ripple ratio, which is now 0.4038.

Finally, we check that the peak current does not reach the minimum current limit of 2.5A.

$$I_{LPK} = I_{OUT} \times (1 + r / 2) = 2A \times (1 + .4038 / 2) = 2.404A \quad (22)$$

The peak current is less than 2.5A, so the DC load specification can be met with this ripple ratio. To design for the LMR12015 simply replace I_{OUT} = 1.5A in the equations for I_{LPK} and see that I_{LPK} does not exceed the LMR12015's current limit of 2.0A (min).

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INDUCTOR MATERIAL SELECTION

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation will result in a sudden reduction in inductance and prevent the regulator from operating correctly. To prevent the inductor from saturating over the entire -40 °C to 125 °C range, pick an inductor with a saturation current higher than the upper limit of I_{CL} listed in the Electrical Characteristics table.

Ferrite core inductors are recommended to reduce AC loss and fringing magnetic flux. The drawback of ferrite core inductors is their quick saturation characteristic. The current limit circuit has a propagation delay and so is oftentimes not fast enough to stop a saturated inductor from going above the current limit. This has the potential to damage the internal switch. To prevent a ferrite core inductor from getting into saturation, the inductor saturation current rating should be higher than the switch current limit I_{CL}. The LMR12015/20 is quite robust in handling short pulses of current that are a few amps above the current limit. Saturation protection is provided by a second current limit which is 30% higher than the cycle by cycle current limit. When the saturation protection is triggered the part will turn off the output switch and attempt to soft-start. (When a compromise has to be made, pick an inductor with a saturation current just above the lower limit of the I_{CL}.) Be sure to validate the short-circuit protection over the intended temperature range.

An inductor's saturation current is usually lower when hot. So consult the inductor vendor if the saturation current rating is only specified at room temperature.

Soft saturation inductors such as the iron powder types can also be used. Such inductors do not saturate suddenly and therefore are safer when there is a severe overload or even shorted output. Their physical sizes are usually smaller than the Ferrite core inductors. The downside is their fringing flux and higher power dissipation due to relatively high AC loss, especially at high frequencies.

INPUT CAPACITOR

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage, RMS current rating, and Equivalent Series Inductance (ESL). The recommended input capacitance is 10 µF, although 4.7 µF works well for input voltages below 6V. The input voltage rating is specifically stated by the capacitor manufacturer. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The input capacitor maximum RMS input current rating (I_{RMS-IN}) must be greater than:

$$I_{RMS-IN} = I_{OUT} \times \sqrt{D \times \left(1 - D + \frac{r^2}{12}\right)} \quad (23)$$

where

- r is the ripple ratio defined earlier
- I_{OUT} is the output current, and
- D is the duty cycle

It can be shown from the above equation that maximum RMS capacitor current occurs when D = 0.5. Always calculate the RMS at the point where the duty cycle, D, is closest to 0.5. The ESL of an input capacitor is usually determined by the effective cross sectional area of the current path. A large leaded capacitor will have high ESL and a 0805 ceramic chip capacitor will have very low ESL. At the operating frequencies of the LMR12015/20, certain capacitors may have an ESL so large that the resulting impedance (2πfL) will be higher than that required to provide stable operation. As a result, surface mount capacitors are strongly recommended. Sanyo POSCAP, Tantalum or Niobium, Panasonic SP or Cornell Dubilier Low ESR are all good choices for input capacitors and have acceptable ESL. Multilayer ceramic capacitors (MLCC) have very low ESL. For MLCCs it is recommended to use X7R or X5R dielectrics. Consult the capacitor manufacturer's datasheet to see how rated capacitance varies over operating conditions.

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OUTPUT CAPACITOR

The output capacitor is selected based upon the desired output ripple and transient response. The LMR12015/20's loop compensation is designed for ceramic capacitors. A minimum of 22 µF is required at 2 MHz (33 uF at 1 MHz) while 47 - 100 µF is recommended for improved transient response and higher phase margin. The output voltage ripple of the converter is:

$$\Delta V_{OUT} = \Delta i_L \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (24)$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple will be approximately sinusoidal and 90° phase shifted from the switching action. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise will couple through parasitic capacitances in the inductor to the output. A ceramic capacitor will bypass this noise while a tantalum will not.

The transient response is determined by the speed of the control loop and the ability of the output capacitor to provide the initial current of a load transient. Capacitance can be increased significantly with little detriment to the regulator stability. However, increasing the capacitance provides dimininshing improvement over 100 uF in most applications, because the bandwidth of the control loop decreases as output capacitance increases. If improved transient performance is required, add a feed forward capacitor. This becomes especially important for higher output voltages where the bandwidth of the LMR12015/20 is lower. See Feed Forward Capacitor and Frequency Synchronization sections.

Check the RMS current rating of the capacitor. The RMS current rating of the capacitor chosen must also meet the following condition:

$$I_{RMS\text{-}OUT} = I_{OUT} \times \frac{r}{\sqrt{12}}$$

where

- I_{OUT} is the output current, and
- r is the ripple ratio. (25)

CATCH DIODE

The catch diode (D1) conducts during the switch off-time. A Schottky diode is recommended for its fast switching times and low forward voltage drop. The catch diode should be chosen so that its current rating is greater than:

$$I_{D1} = I_{OUT} \times (1\text{-}D) \quad (26)$$

The reverse breakdown rating of the diode must be at least the maximum input voltage plus appropriate margin. To improve efficiency choose a Schottky diode with a low forward voltage drop.

BOOST DIODE (OPTIONAL)

For circuits with input voltages V_{IN} < 5V and duty cycles (D) >0.75V. a small-signal Schottky diode is recommended. A good choice is the BAT54 small signal diode. The cathode of the diode is connected to the BOOST pin and the anode to a 5V voltage rail.

BOOST CAPACITOR

A ceramic 0.1 µF capacitor with a voltage rating of at least 6.3V is sufficient. The X7R and X5R MLCCs provide the best performance.

OUTPUT VOLTAGE

The output voltage is set using the following equation where R2 is connected between the FB pin and GND, and R1 is connected between V_{OUT} and the FB pin. A good starting value for R2 is 1 kΩ.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (27)$$

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FEED FORWARD CAPACITOR (OPTIONAL)

A feed forward capacitor C_{FF} can improve the transient response of the converter. Place C_{FF} in parallel with R1. The value of C_{FF} should place a zero in the loop response at, or above, the pole of the output capacitor and R_{LOAD}. The C_{FF} capacitor will increase the crossover frequency of the design, thus a larger minimum output capacitance is required for designs using C_{FF}. C_{FF} should only be used with an output capacitance greater than or equal to 44 uF. Example waveforms of load transient with and without the C_{FF} caps are as shown below.

$$C_{FF} <= \frac{V_{OUT} \times C_{OUT}}{I_{OUT} \times R1} \quad (28)$$

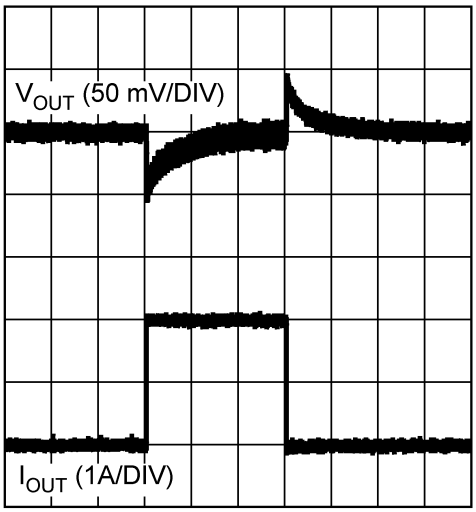


Figure 32. LMR12015/20 Load Transient with C_{FF} cap
V_{OUT} = 3.3V

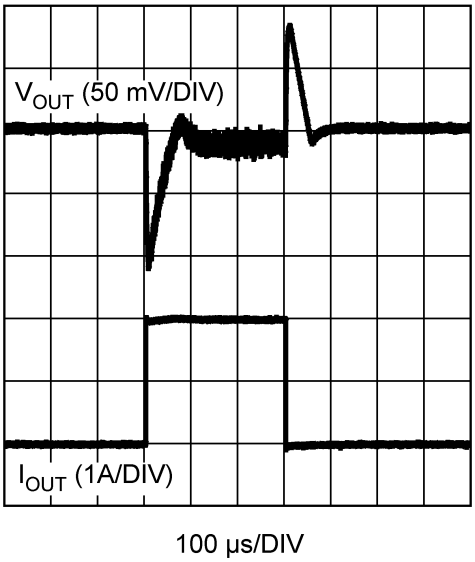


Figure 33. LMR12015/20 Load Transient without C_{FF} cap
V_{OUT} = 3.3V

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Calculating Efficiency, and Junction Temperature

The complete LMR12015/20 DC-DC converter efficiency can be calculated in the following manner.

$$\eta = \frac{P_{OUT}}{P_{IN}} \tag{29}$$

Or

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \tag{30}$$

Calculations for determining the most significant power losses are shown below. Other losses totaling less than 2% are not discussed.

Power loss (P_{LOSS}) is the sum of two basic types of losses in the converter, switching and conduction. Conduction losses usually dominate at higher output loads, where as switching losses remain relatively fixed and dominate at lower output loads. The first step in determining the losses is to calculate the duty cycle (D).

$$D = \frac{V_{OUT} + V_{D1}}{V_{IN} + V_{D1} - V_{DS}} \tag{31}$$

V_{DS} is the voltage drop across the internal NFET when it is on, and is equal to:

$$V_{DS} = I_{OUT} \times R_{DSON} \tag{32}$$

V_D is the forward voltage drop across the Schottky diode. It can be obtained from the Electrical Characteristics section of the schottky diode datasheet. If the voltage drop across the inductor (V_{DCR}) is accounted for, the equation becomes:

$$D = \frac{V_{OUT} + V_{D1} + V_{DCR}}{V_{IN} + V_{D1} - V_{DS}} \tag{33}$$

V_{DCR} usually gives only a minor duty cycle change, and has been omitted in the examples for simplicity.

SCHOTTKY DIODE CONDUCTION LOSSES

The conduction losses in the free-wheeling Schottky diode are calculated as follows:

$$P_{DIODE} = V_{D1} \times I_{OUT} (1-D) \tag{34}$$

Often this is the single most significant power loss in the circuit. Care should be taken to choose a Schottky diode that has a low forward voltage drop.

INDUCTOR CONDUCTION LOSSES

Another significant external power loss is the conduction loss in the output inductor. The equation can be simplified to:

$$P_{IND} = I_{OUT}^2 \times R_{DCR} \tag{35}$$

MOSFET CONDUCTION LOSSES

The LMR12015/20 conduction loss is mainly associated with the internal NFET:

$$P_{COND} = I_{OUT}^2 \times R_{DSON} \times D \tag{36}$$

MOSFET SWITCHING LOSSES

Switching losses are also associated with the internal NFET. They occur during the switch on and off transition periods, where voltages and currents overlap resulting in power loss. The simplest means to determine this loss is to empirically measuring the rise and fall times (10% to 90%) of the switch at the switch node:

$$P_{SWF} = 1/2(V_{IN} \times I_{OUT} \times f_{SW} \times t_{FALL}) \tag{37}$$

$$P_{SWR} = 1/2(V_{IN} \times I_{OUT} \times f_{SW} \times t_{RISE}) \tag{38}$$

$$P_{SW} = P_{SWF} + P_{SWR} \tag{39}$$

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Table 1. Typical Rise and Fall Times vs Input Voltage

V_{IN}	t_{RISE}	t_{FALL}
5V	8ns	8ns
10V	9ns	9ns
15V	10ns	10ns

IC QUIESCENT LOSSES

Another loss is the power required for operation of the internal circuitry:

$$P_Q = I_Q \times V_{IN} \quad (40)$$

I_Q is the quiescent operating current, and is typically around 2.4 mA.

MOSFET DRIVER LOSSES

The other operating power that needs to be calculated is that required to drive the internal NFET:

$$P_{BOOST} = I_{BOOST} \times V_{BOOST} \quad (41)$$

V_{BOOST} is normally between 3VDC and 5VDC. The I_{BOOST} rms current is dependant on switching frequency f_{SW}. I_{BOOST} is approximately 8.2 mA at 2 MHz and 4.4 mA at 1 MHz.

TOTAL POWER LOSSES

Total power losses are:

$$P_{LOSS} = P_{COND} + P_{SWR} + P_{SWF} + P_Q + P_{BOOST} + P_{DIODE} + P_{IND} \quad (42)$$

Losses internal to the LMR12015/20 are:

$$P_{INTERNAL} = P_{COND} + P_{SWR} + P_{SWF} + P_Q + P_{BOOST} \quad (43)$$

EFFICIENCY CALCULATION EXAMPLE

Operating conditions are:

V_{IN} = 12V (44)
f_{SW} = 2 MHz (45)
V_{OUT} = 3.3V (46)
V_{D1} = 0.5V (47)
I_{OUT} = 2A (48)
R_{DCR} = 20 mΩ (49)

Internal Power Losses are:

$P_{COND} = I_{OUT}^2 \times R_{DSON} \times D = 2^2 \times 0.15\Omega \times 0.314 = 188$ mW (50)
$P_{SW} = (V_{IN} \times I_{OUT} \times f_{SW} \times t_{FALL}) = (12V \times 2A \times 2$ MHz $\times 10ns) = 480$ mW (51)
$P_Q = I_Q \times V_{IN} = 2.4$ mA $\times 12V = 29$ mW (52)
$P_{BOOST} = I_{BOOST} \times V_{BOOST} = 8.2$ mA $\times 4.5V = 37$mW (53)
$P_{INTERNAL} = P_{COND} + P_{SW} + P_Q + P_{BOOST} = 733$ mW (54)

Total Power Losses are:

$P_{DIODE} = V_{D1} \times I_{OUT} (1 - D) = 0.5V \times 2 \times (1 - 0.314) = 686$ mW (55)
$P_{IND} = I_{OUT}^2 \times R_{DCR} = 2^2 \times 20$ mΩ $= 80$ mW (56)
$P_{LOSS} = P_{INTERNAL} + P_{DIODE} + P_{IND} = 1.499$ W (57)

The efficiency can now be estimated as:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} = \frac{6.6\ W}{6.6\ W + 1.499\ W} = 81\ \% \quad (58)$$

With this information we can estimate the junction temperature of the LMR12015/20.

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CALCULATING THE LMR12015/20 JUNCTION TEMPERATURE

Thermal Definitions:

T_J = IC junction temperature

T_A = Ambient temperature

$R_{\theta JC}$ = Thermal resistance from IC junction to device case

$R_{\theta JA}$ = Thermal resistance from IC junction to ambient air

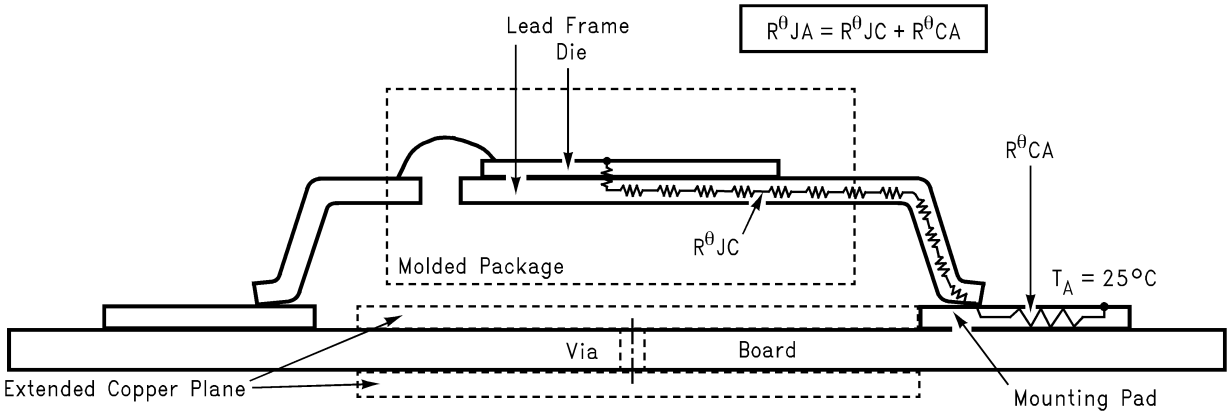


Figure 34. Cross-Sectional View of Integrated Circuit Mounted on a Printed Circuit Board.

Heat in the LMR12015/20 due to internal power dissipation is removed through conduction and/or convection.

Conduction: Heat transfer occurs through cross sectional areas of material. Depending on the material, the transfer of heat can be considered to have poor to good thermal conductivity properties (insulator vs conductor).

Heat Transfer goes as:

Silicon→Lead Frame→PCB (59)

Convection: Heat transfer is by means of airflow. This could be from a fan or natural convection. Natural convection occurs when air currents rise from the hot device to cooler air.

Thermal impedance is defined as:

$$R_\theta = \frac{\Delta T}{\text{Power}} \tag{60}$$

Thermal impedance from the silicon junction to the ambient air is defined as:

$$R_{\theta JA} = \frac{T_J - T_A}{\text{Power}} \tag{61}$$

This impedance can vary depending on the thermal properties of the PCB. This includes PCB size, weight of copper used to route traces , the ground plane, and the number of layers within the PCB. The type and number of thermal vias can also make a large difference in the thermal impedance. Thermal vias are necessary in most applications. They conduct heat from the surface of the PCB to the ground plane. Six to nine thermal vias should be placed under the exposed pad to the ground plane. Placing more than nine thermal vias results in only a small reduction to $R_{\theta JA}$ for the same copper area. These vias should have 8 mil holes to avoid wicking solder away from the DAP. See AN-1187 SNOA401and AN-1520 SNVA183 for more information on package thermal performance.

To predict the silicon junction temperature for a given application, three methods can be used. The first is useful before prototyping and the other two can more accurately predict the junction temperature within the application.

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Method 1:

The first method predicts the junction temperature by extrapolating a best guess $R_{\theta JA}$ from the table or graph. The tables and graph are for natural convection. The internal dissipation can be calculated using the efficiency calculations. This allows the user to make a rough prediction of the junction temperature in their application. Methods two and three can later be used to determine the junction temperature more accurately.

The table below has values of $R_{\theta JA}$ for the WSON package.

Table 2. $R_{\theta JA}$ values for the LLP @ 1 Watt dissipation:

Number of Board Layers	Size of Bottom Layer Copper Connected to DAP	Size of Top Layer Copper Connected to Dap	Number of 8 mil Thermal Vias	$R_{\theta JA}$
2	0.25 in^2	0.05 in^2	8	78 °C/W
2	0.5625 in^2	0.05 in^2	8	65.6 °C/W
2	1 in^2	0.05 in^2	8	58.6 °C/W
2	1.3225 in^2	0.05 in^2	8	50 °C/W
4 (Eval Board)	3.25 in^2	2.25 in^2	15	30.7 °C/W

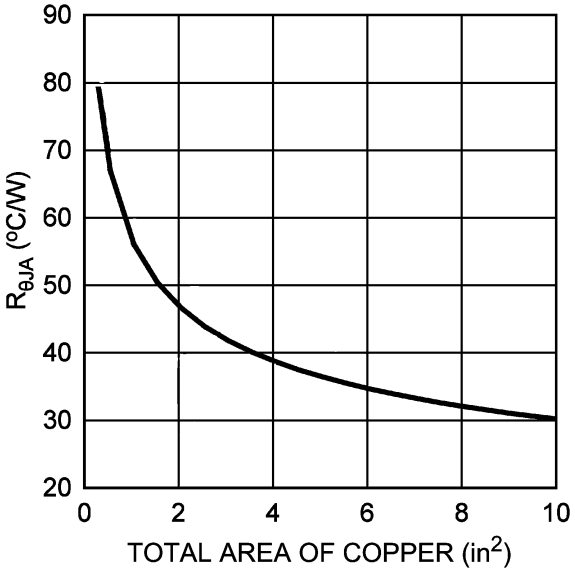


Figure 35. Estimate of Thermal Resistance vs. Ground Copper Area Eight Thermal Vias and Natural Convection

Method 2:

The second method requires the user to know the thermal impedance of the silicon junction to case. ($R_{\theta JC}$) is approximately 9.1°C/W for the WSON. The case temperature should be measured on the bottom of the PCB at a thermal via directly under the DAP of the LMR12015/20. The solder resist should be removed from this area for temperature testing. The reading will be more accurate if it is taken midway between pins 2 and 9, where the NMOS switch is located. Knowing the internal dissipation from the efficiency calculation given previously, and the case temperature (T_C) we have:

$$R_{\theta JC} = \frac{T_J - T_C}{Power} \tag{62}$$

Therefore:

$$T_J = (R_{\theta JC} \times P_{LOSS}) + T_C \tag{63}$$

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PCB Layout Considerations

COMPACT LAYOUT

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. The following guidelines will help the user design a circuit with maximum rejection of outside EMI and minimum generation of unwanted EMI.

Parasitic inductance can be reduced by keeping the power path components close together and keeping the area of the loops small, on which high currents travel. Short, thick traces or copper pours (shapes) are best. In particular, the switch node (where L1, D1, and the SW pin connect) should be just large enough to connect all three components without excessive heating from the current it carries. The LMR12015/20 operates in two distinct cycles (see Figure 27) whose high current paths are shown below in Figure 36:

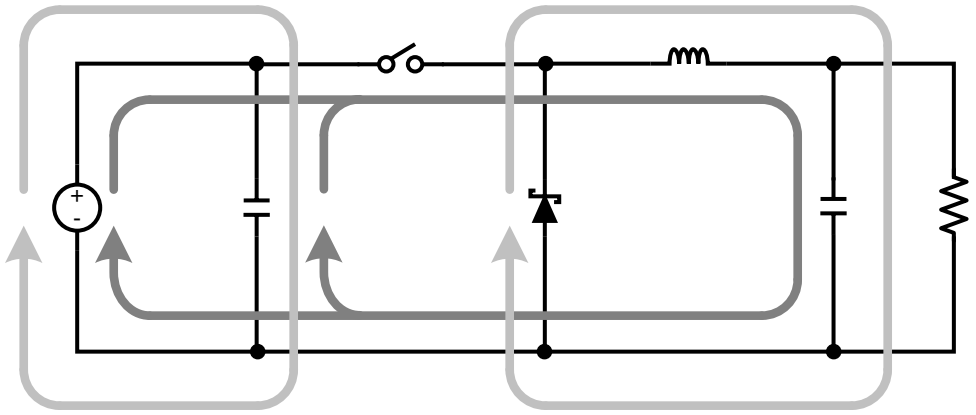


Figure 36. Buck Converter Current Loops

The dark grey, inner loop represents the high current path during the MOSFET on-time. The light grey, outer loop represents the high current path during the off-time.

GROUND PLANE AND SHAPE ROUTING

The diagram of Figure 36 is also useful for analyzing the flow of continuous current vs. the flow of pulsating currents. The circuit paths with current flow during both the on-time and off-time are considered to be continuous current, while those that carry current during the on-time or off-time only are pulsating currents. Preference in routing should be given to the pulsating current paths, as these are the portions of the circuit most likely to emit EMI. The ground plane of a PCB is a conductor and return path, and it is susceptible to noise injection just like any other circuit path. The path between the input source and the input capacitor and the path between the catch diode and the load are examples of continuous current paths. In contrast, the path between the catch diode and the input capacitor carries a large pulsating current. This path should be routed with a short, thick shape, preferably on the component side of the PCB. Multiple vias in parallel should be used right at the pad of the input capacitor to connect the component side shapes to the ground plane. A second pulsating current loop that is often ignored is the gate drive loop formed by the SW and BOOST pins and boost capacitor C_{BOOST}. To minimize this loop and the EMI it generates, keep C_{BOOST} close to the SW and BOOST pins.

FB LOOP

The FB pin is a high-impedance input, and the loop created by R2, the FB pin and ground should be made as small as possible to maximize noise rejection. R2 should therefore be placed as close as possible to the FB and GND pins of the IC.

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PCB SUMMARY

1. Minimize the parasitic inductance by keeping the power path components close together and keeping the area of the high-current loops small.
2. The most important consideration when completing the layout is the close coupling of the GND connections of the C_{IN} capacitor and the catch diode D1. These ground connections should be immediately adjacent, with multiple vias in parallel at the pad of the input capacitor connected to GND. Place C_{IN} and D1 as close to the IC as possible.
3. Next in importance is the location of the GND connection of the C_{OUT} capacitor, which should be near the GND connections of C_{IN} and D1.
4. There should be a continuous ground plane on the copper layer directly beneath the converter. This will reduce parasitic inductance and EMI.
5. The FB pin is a high impedance node and care should be taken to make the FB trace short to avoid noise pickup and inaccurate regulation. The feedback resistors should be placed as close as possible to the IC, with the GND of R2 placed as close as possible to the GND of the IC. The V_{OUT} trace to R1 should be routed away from the inductor and any other traces that are switching.
6. High AC currents flow through the V_{IN}, SW and V_{OUT} traces, so they should be as short and wide as possible. However, making the traces wide increases radiated noise, so the layout designer must make this trade-off. Radiated noise can be decreased by choosing a shielded inductor.

The remaining components should also be placed as close as possible to the IC. Please see Application Note AN-2279 SNVU191 for further considerations and the LMR12015/20 eval board as an example of a four-layer layout.

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LMR12015/20 Circuit Examples

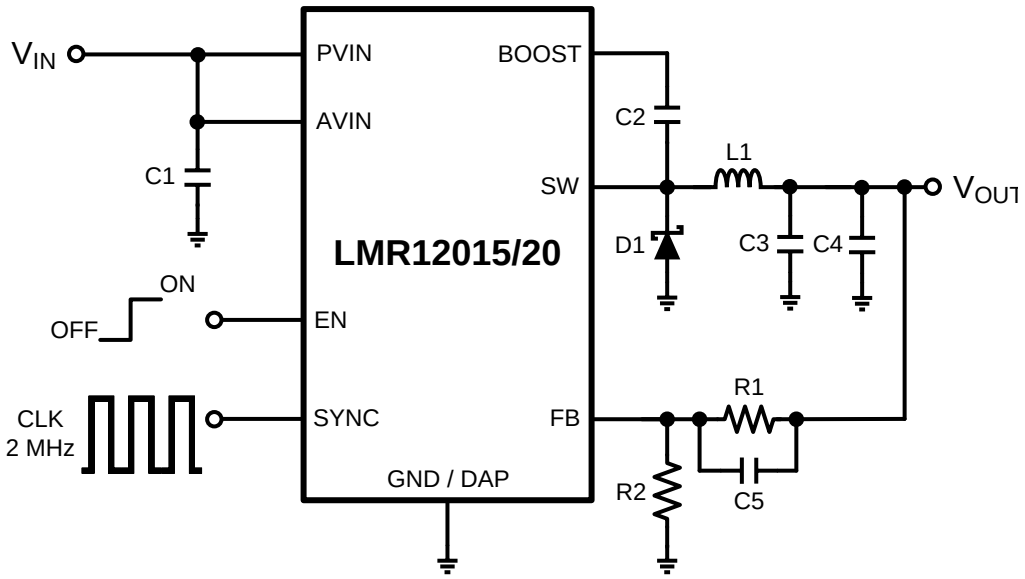


Figure 37. V_{IN} = 7 - 20V, V_{OUT} = 5V, f_{SW} = 2 MHz, I_{OUT} = Full Load with C_{FF}

Table 3. Bill of Materials for Figure 37

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	1.5 or 2A Buck Regulator	LMR12015/20	Texas Instruments
C_{PVIN}	C1	10 µF	C1210C106K8PACTU	Kemet
C_{BOOST}	C2	0.1 µF	C0603X104K4RACTU	Kemet
C_{OUT}	C3	22 µF	GRM32ER71C226KE18L	MuRata
C_{OUT}	C4	22 µF	GRM32ER71C226KE18L	MuRata
C_{FF}	C5	0.18 µF	0603ZC184KAT2A	AVX
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS06	Toshiba
Inductor	L1	3.3 µH	7447789003	Wurth
Feedback Resistor	R1	4.02 kΩ	CRCW06034K02FKEA	Vishay
Feedback Resistor	R2	1.02 kΩ	CRCW06031K02FKEA	Vishay

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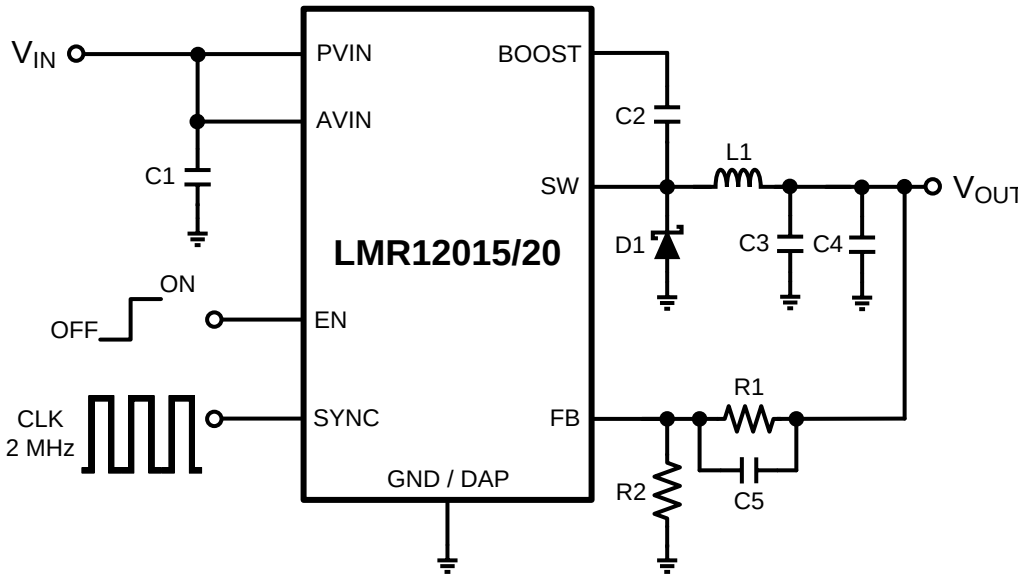


Figure 38. V_{IN} = 5 - 20V, V_{OUT} = 3.3V, f_{SW} = 2 MHz, I_{OUT} = Full Load with C_{FF}

Table 4. Bill of Materials for Figure 38

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	1.5 or 2A Buck Regulator	LMR12015/20	Texas Instruments
C_{PVIN}	C1	10 µF	C1210C106K8PACTU	Kemet
C_{BOOST}	C2	0.1 µF	C0603X104K4RACTU	Kemet
C_{OUT}	C3	22 µF	GRM32ER71C226KE18L	MuRata
C_{OUT}	C4	22 µF	GRM32ER71C226KE18L	MuRata
C_{FF}	C5	0.18 µF	0603ZC184KAT2A	AVX
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS06	Toshiba
Inductor	L1	3.3 µH	7447789003	Wurth
Feedback Resistor	R1	2.32 kΩ	CRCW06032K32FKEA	Vishay
Feedback Resistor	R2	1.02 kΩ	CRCW06031K02FKEA	Vishay

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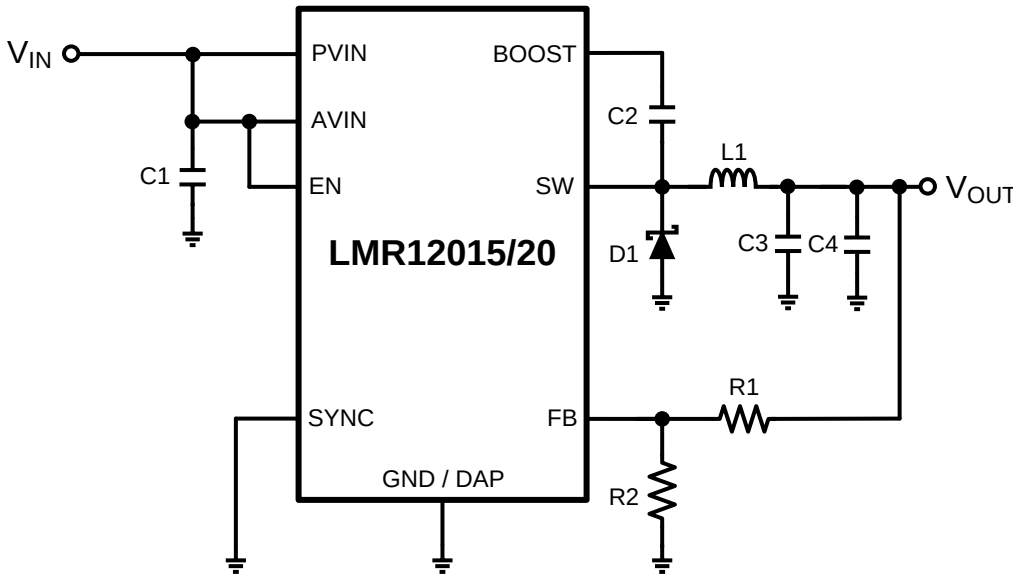


Figure 39. V_{IN} = 5 - 20V, V_{OUT} = 3.3V, f_{SW} = 2 MHz, I_{OUT} = Full Load without C_{FF}

Table 5. Bill of Materials for Figure 39

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	1.5 or 2A Buck Regulator	LMR12015/20	Texas Instruments
C_{PVIN}	C1	10 µF	C1210C106K8PACTU	Kemet
C_{BOOST}	C2	0.1 µF	C0603X104K4RACTU	Kemet
C_{OUT}	C3	22 µF	GRM32ER71C226KE18L	MuRata
C_{OUT}	C4	22 µF	GRM32ER71C226KE18L	MuRata
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS06	Toshiba
Inductor	L1	3.3 µH	7447789003	Sumida
Feedback Resistor	R1	2.32 kΩ	CRCW06032K32FKEA	Vishay
Feedback Resistor	R2	1.02 kΩ	CRCW06031K02FKEA	Vishay

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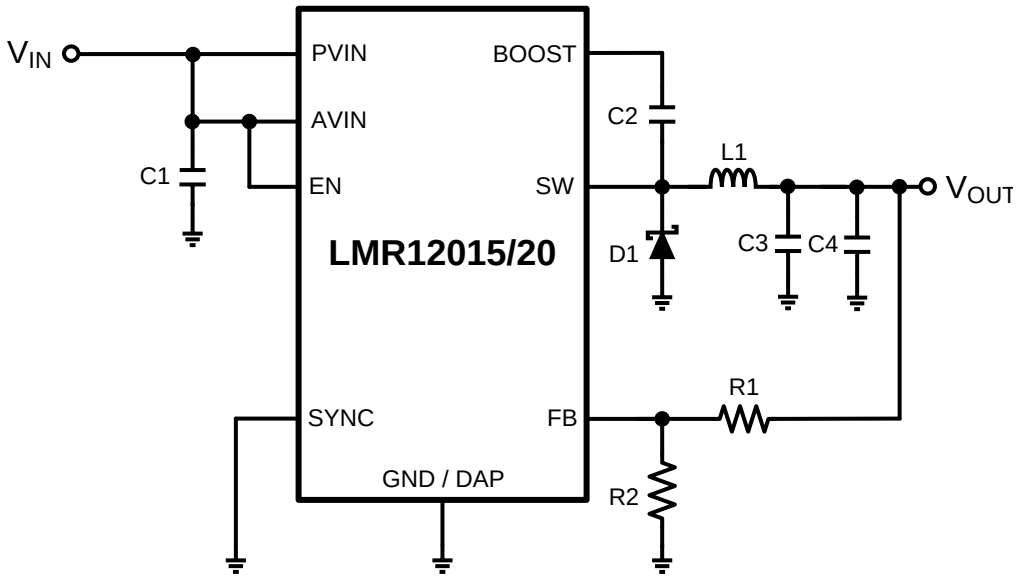


Figure 40. V_{IN} = 3.3 - 16V, V_{OUT} = 1.8V, f_{SW} = 2 MHz, I_{OUT} = Full Load

Table 6. Bill of Materials for Figure 40

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	1.5 or 2A Buck Regulator	LMR12015/20	Texas Instruments
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	22 µF	C3225X7R1C226K	TDK
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS06	Toshiba
Inductor	L1	1.0 µH	CDRH5D18BHPNP	Sumida
Feedback Resistor	R1	12 kΩ	CRCW060312K0FKEA	Vishay
Feedback Resistor	R2	15 kΩ	CRCW060315K0FKEA	Vishay

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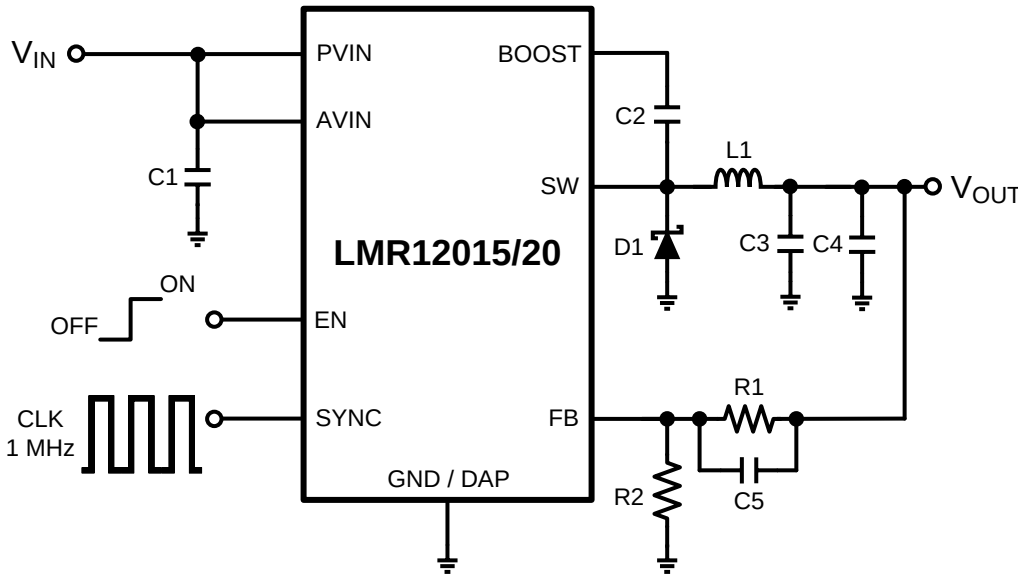


Figure 41. V_{IN} = 3.3 - 16V, V_{OUT} = 1.8V, f_{SW} = 1 MHz, I_{OUT} = Full Load

Table 7. Bill of Materials for Figure 41

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	1.5 or 2A Buck Regulator	LMR12015/20	Texas Instruments
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	22 uF	C3225X7R1C226K	TDK
C_{OUT}	C4	22 uF	C3225X7R1C226K	TDK
C_{FF}	C5	3.9 nF	GRM188R71H392KA01D	Murata
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS06	Toshiba
Inductor	L1	1.8 µH	CDRH5D18BHPNP	Sumida
Feedback Resistor	R1	12 kΩ	CRCW060312K0FKEA	Vishay
Feedback Resistor	R2	15 kΩ	CRCW060315K0FKEA	Vishay

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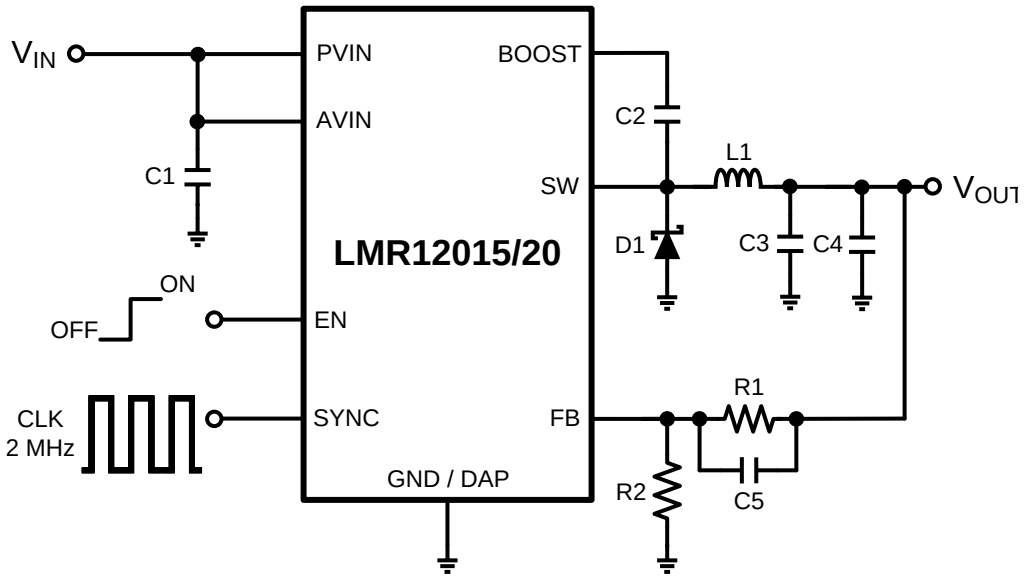


Figure 42. V_{IN} = 3.3 - 9V, V_{OUT} = 1.2V, f_{SW} = 2 MHz, I_{OUT} = Full Load

Table 8. Bill of Materials for Figure 42

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	1.5 or 2A Buck Regulator	LMR12015/20	Texas Instruments
C_{PVIN}	C1	10 µF	GRM32DR71E106KA12L	Murata
C_{BOOST}	C2	0.1 µF	GRM188R71C104KA01D	Murata
C_{OUT}	C3	47 µF	GRM32ER61A476KE20L	Murata
C_{OUT}	C4	22 µF	C3225X7R1C226K	TDK
C_{FF}	C5	NOT MOUNTED		
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS06	Toshiba
Inductor	L1	0.56 µH	CDRH2D18/HPNP	Sumida
Feedback Resistor	R1	1.02 kΩ	CRCW06031K02FKEA	Vishay
Feedback Resistor	R2	5.10 kΩ	CRCW06035K10FKEA	Vishay

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REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	32

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMR12015XSD/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L285B	Samples
LMR12015XSDX/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L285B	Samples
LMR12020XSD/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L284B	Samples
LMR12020XSDX/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L284B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

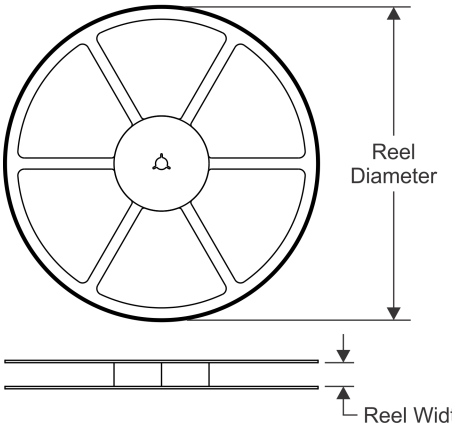
(4) Only one of markings shown within the brackets will appear on the physical device.

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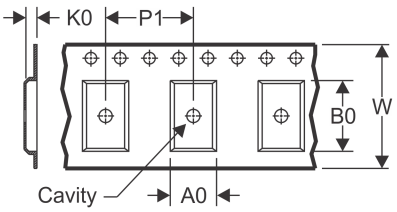
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

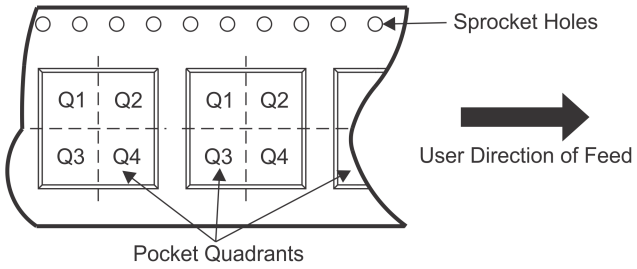


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

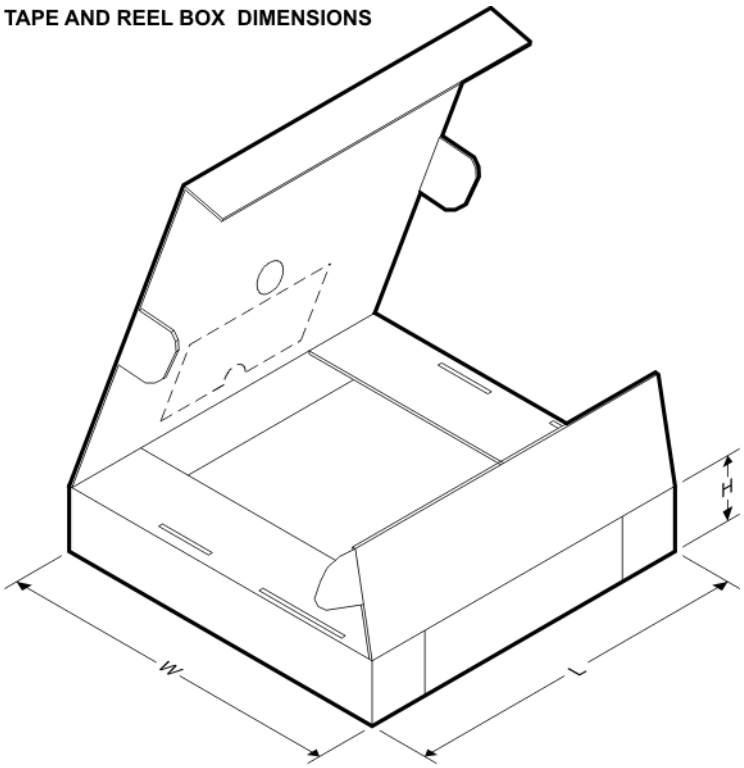
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR12015XSD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR12015XSDX/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR12020XSD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMR12020XSDX/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

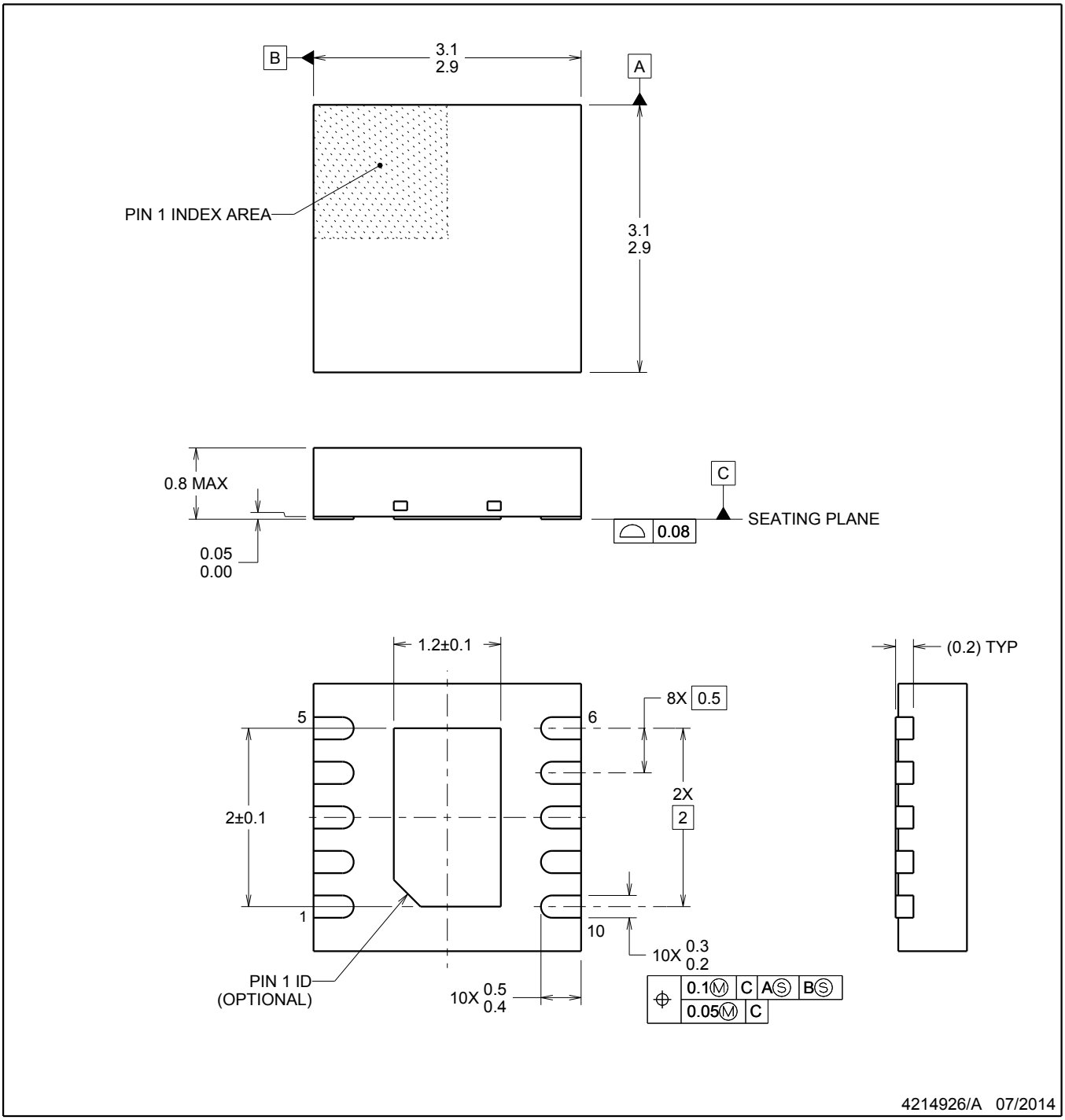
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR12015XSD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LMR12015XSDX/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0
LMR12020XSD/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LMR12020XSDX/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0

PACKAGE OUTLINE

DSC0010B

WSON - 0.8 mm max height

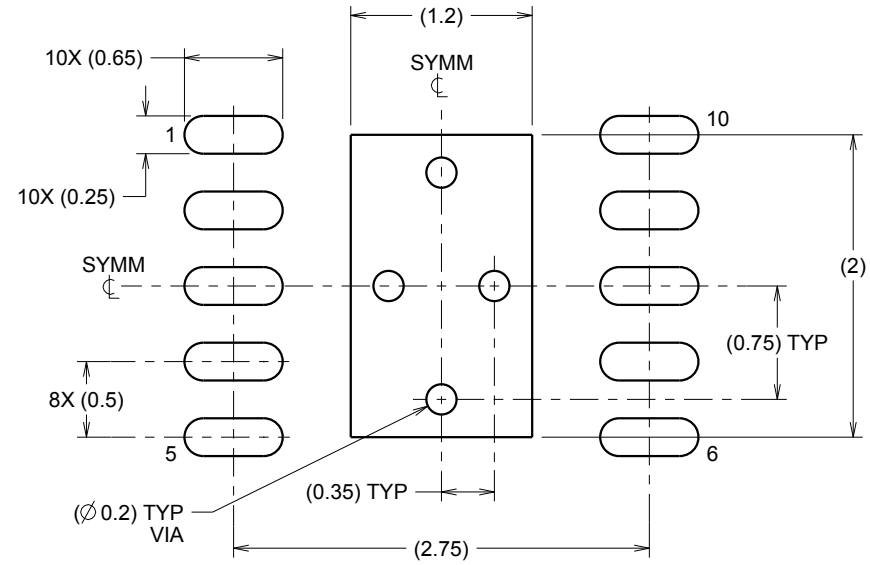
PLASTIC SMALL OUTLINE - NO LEAD



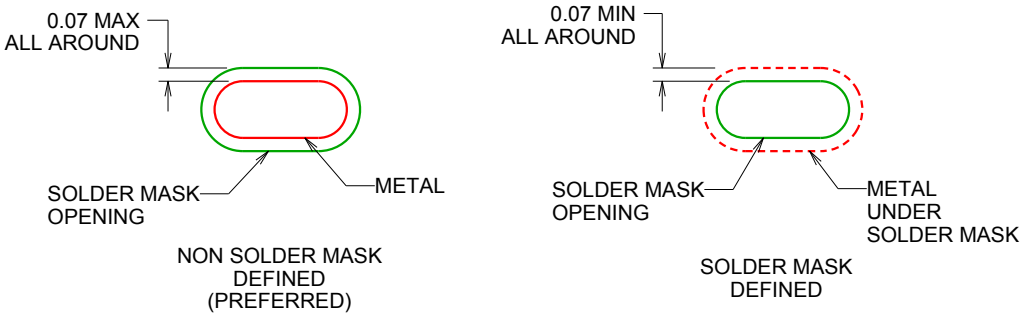
4214926/A 07/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4214926/A 07/2014

NOTES: (continued)

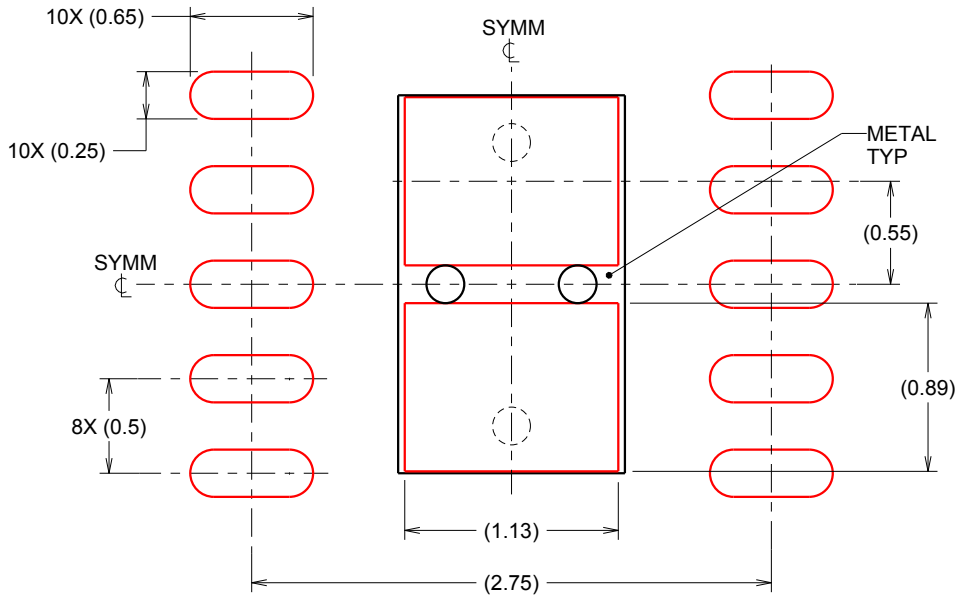
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSC0010B

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4214926/A 07/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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