

Z8 Encore!® Motor Control Series

Z8 Encore!® Z8FMC16 MCU

Programming Specification

PRS000502-1005

PRELIMINARY

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Flash Memory Programming Overview

The Z8 Encore!® Z8FMC16 Motor Control features a Flash program memory selections of 8KB or 16KB. By using Flash memory, you have the ability to easily update the code. The Z8 Encore!® features an on-chip Flash controller that typically manages the timing of Flash control signals for programming, page erase, and mass erase operations. The Flash controller can also be bypassed to allow direct control of Flash signals via the general purpose input/output (GPIO) pins. Flash memory can be programmed faster by controlling the Flash memory signals directly. Bypassing the Flash controller is beneficial when programming a large number of devices, and is most likely to be used by third party vendors who are developing the multi-site gang programmers.

Bypassing the Flash Controller

Flash controller bypass mode is enabled by writing the following three bytes of instruction to the on-chip debugger (OCD) via the DBG interface:

1. **80H** - This instruction initiates auto-baud calculation of the DBG interface data and clock rate.
2. **F0H** - OCD writes testmode register command.
3. **04H** - Data to be written to the testmode register. This data enables the Flash controller bypass mode.

Flash Memory Control Signals

Depending on the size (number of bytes) available in the Flash memory, the Flash memory uses fourty two signals for its direct interfacing.

- 16 signals for the address lines.
- 8 signals for data input.
- 8 signals for data output.
- 10 signals for control operations.

The Flash memory control signals are listed and described in Table 1

Table 1. Flash Memory Control Signals

Signal	Direction	Description
XADDR[9:0]	I	X address input selects a row. XADDR[9:0] corresponds to the upper 10 bits of the program memory address space (PROGMEM[15:6]). For Z8 Encore!® devices with less than 64KB of program memory, the unused upper address bits must be set to 0.
YADDR[5:0]	I	Y address input selects one byte within a row. YADDR[5:0] corresponds to the lower 6 bits of the program memory address space (PROGMEM[5:0]).
DIN[7:0]	I	Data input.
DOUT[7:0]	O	Data output.
XE	I	X address enable.
YE	I	Y address enable.
SE	I	Sense amplifier enable.
OE	I	Output enable.
ERASE	I	Erase enable. This signal is used to select erase operations.
MAS1	I	Mass erase select. This signal is used to distinguish between page erase and mass erase operations.
PROG	I	Program enable. This signal is used to select a program operation.
NVSTR	I	Non-volatile store enable. This signal is used during page erase, mass erase, and programming operations.
TMR	I	This signal should be set to 1 during all operations.
IFREN	I	Information area select.

Flash Memory Operations

When bypassing the Flash controller, all Flash memory operations (read, program, page erase, and mass erase) are available. The mode of operation is set by the Flash memory control signals as described in Table 2.

The selection of the Flash main memory or the Flash information area depends on the IFREN signal as described in Table 3.

Table 2. Flash Mode Truth Table

Mode	XE	YE	SE	OE	PROG	ERASE	MAS1	NVSTR	TMR	IFREN
Read	H	H	H	H	L	L	L	L	H	L/H[1]
Program	H	H	L	L	H	L	L	H	H	L/H[1]
Page Erase	H	L	L	L	L	H	L	H	H	L/H[1]
Mass Erase	H	L	L	L	L	H	H	H	H	L/H[1]

See Table 3 for IFREN signal operation information.

Table 3. IFREN Signal Truth Table

Mode	IFREN = 1	IFREN = 0
Read	Read Information Area	Read Main Memory
Program	Program Information Area	Program Main Memory
Page Erase	Page Erase Information Area	Page Erase Main Memory
Mass Erase	Mass Erase Information Area	Mass Erase Main Memory

Flash Bypass Mode Register Structure

For using Flash controller bypass mode for all package sizes, the signals must be registered internally. This allows all data access to occur through pin PWM2L and Port A [6:0]. Three other pins (PWM2H, PWM1L, and PWM1H), selects one of the input data registers or the data output register as shown in Table 4.

Table 4. Control Registers in Flash Bypass Mode

	Register Select [PWM2H, PWM1L, PWM1H]						
	000	**001**	**010**	**011**	**100**	**101**	**110-111**
Input/Output	**Input**	**Input**	**Input**	**Input**	**Input**	**Output**	**Input**
PWM2L	XADDR[9]	XADDR[1]	DIN[7]	XE	TMR	DOUT[7]	NOP
Port A6	XADDR[8]	XADDR[0]	DIN[6]	YE	IFREN	DOUT[6]	NOP
Port A5	XADDR[7]	YADDR[5]	DIN[5]	SE	NOP	DOUT[5]	NOP
Port A4	XADDR[6]	YADDR[4]	DIN[4]	OE	NOP	DOUT[4]	NOP
Port A3	XADDR[5]	YADDR[3]	DIN[3]	ERASE	NOP	DOUT[3]	NOP
Port A2	XADDR[4]	YADDR[2]	DIN[2]	PROG	NOP	DOUT[2]	NOP
Port A1	XADDR[3]	YADDR[1]	DIN[1]	MAS1	NOP	DOUT[1]	NOP
Port A0	XADDR[2]	YADDR[0]	DIN[0]	NVSTR	NOP	DOUT[0]	NOP

Flash Bypass Mode Register Structure

Figure 1 illustrates the multiplexed register structure that allows access to all Flash memory signals through GPIO ports.

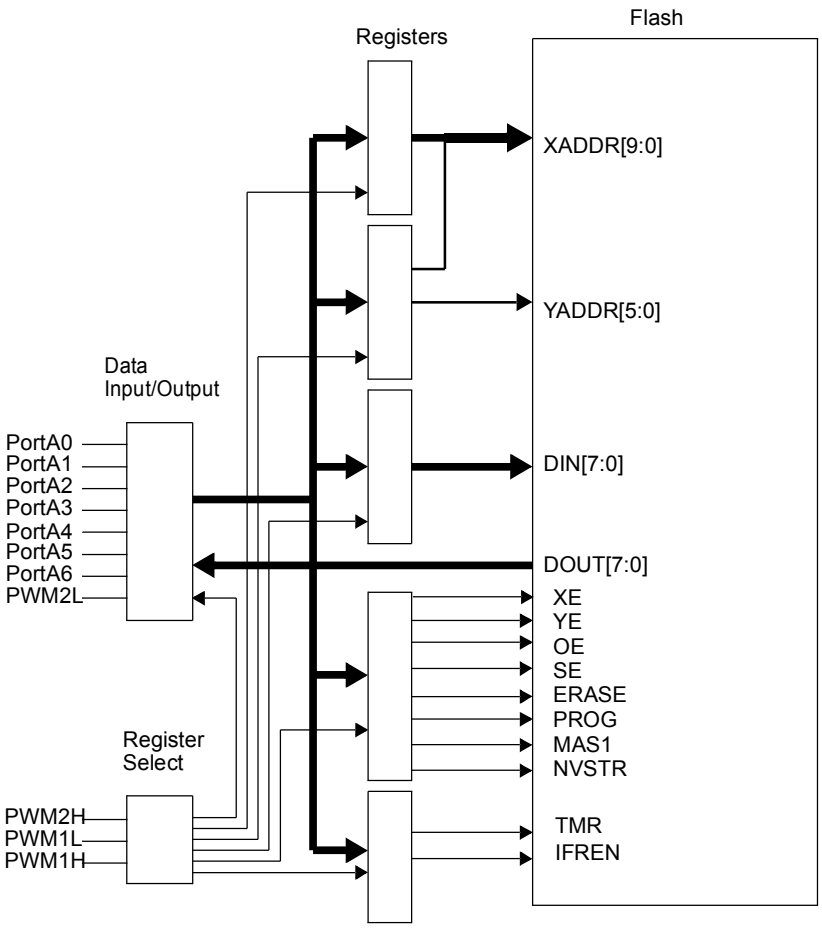


Figure 1. Flash Bypass Mode Register Structure

Bypass Mode Register Read Timing

Figure 2 illustrates the timing of a read operation using the Flash controller bypass mode registers. While reading data, output data is latched into the output register on the first

clock edge. The data is read during the next clock period. Mode selector comprises of the following pins: PWM2H, PWM1L, and PWM1H.

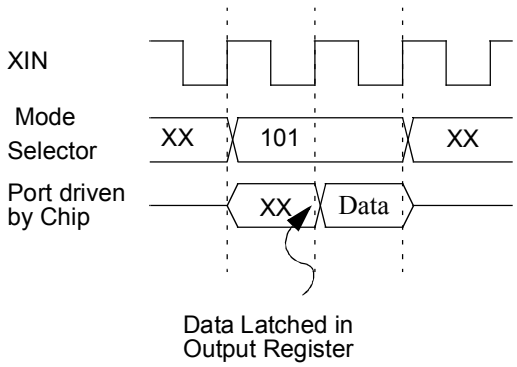


Figure 2. Bypass Mode Register Read Timing

Bypass Mode Register Write Timing

Figure 3 illustrates the timing of a write operation using the Flash controller bypass mode registers. When writing data into the registers, the data is latched on the rising edge of XIN.

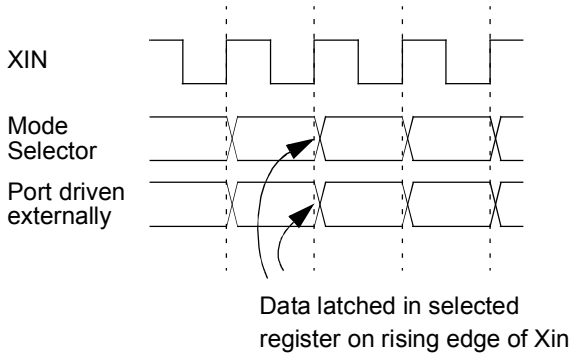


Figure 3. Bypass Mode Register Write Timing

Flash Row Programming

The Flash memory can be programmed either as a single byte at a time or as a row of bytes at a time. Multi-byte row programming allows programming of a full row of Flash memory without incurring all of the programming setup and recovery time for each byte. During row programming, the Flash memory's PROG and NVSTR signals are

continuously asserted until all bytes in a row are programmed. This allows the row to be programmed faster than if these signals are deasserted after programming each byte.

During row programming, you must ensure that the cumulative programming high voltage period does not exceed the specification limits for a row.

Flash Memory Timing

Table 5 and Figures 4 through Figure 7 provides the detailed timing information on accessing the Flash memory in Flash controller bypass mode.

Table 5. Flash Memory Timing Parameters

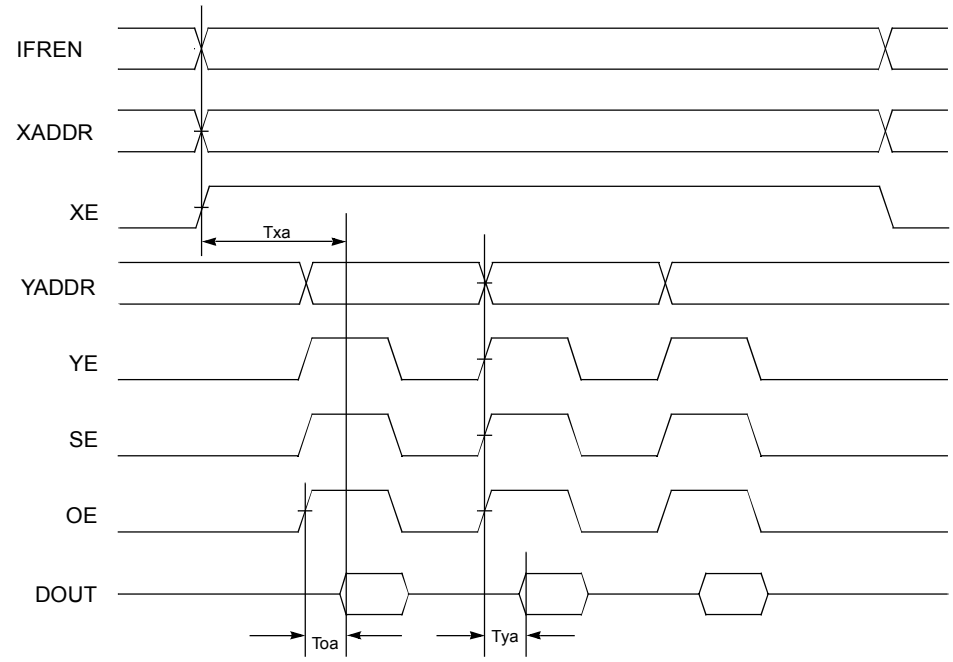
Parameter	Symbol	Min.	Max.	Unit
X address access time	Txa	-	40	ns
Y address access time	Tya	-	40	ns
OE access time	Toa	-	4	ns
PROG/ERASE to NVSTR setup time	Tnvs	5	-	µs
NVSTR hold time	Tnvh	5	-	µs
NVSTR hold time (Mass Erase)	Tnvh1	100	-	µs
NVSTR to program setup time	Tpgs	10	-	µs
Program hold time	Tpgh	20	-	ns
Byte program time	Tprog	30	60	µs
Address / Data setup time	Tads	20	-	ns
Address / Data hold time	Tadh	20	-	ns
Recovery time	Trcv	1	-	µs
Cumulative program high voltage period[1]	Thv	-	12	ms
Erase time	Terase	10	-	ms
Mass Erase time	Tme	200	-	ms

[1]Thv is the cumulative high voltage programming time for a single row before the next erase.

Caution: The same address (byte) cannot be programmed more than twice before the next erase.

Flash Read Timing

Figure 4 illustrates the timing of a read operation from the Flash memory.

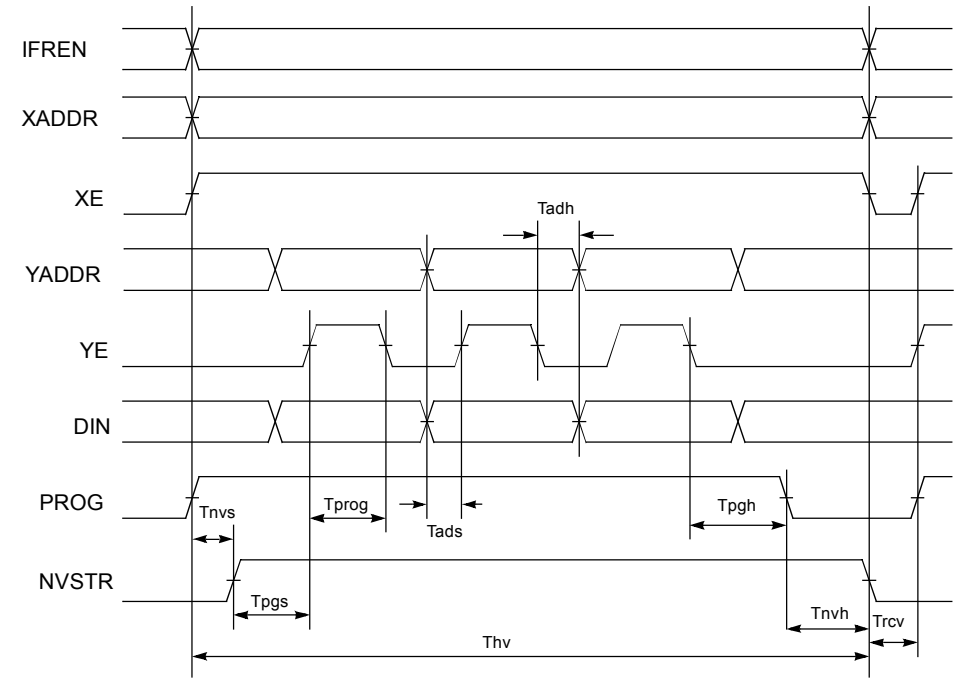


ERASE = 0, MAS1 = 0, NVSTR = 0, TMR = 1

Figure 4. Flash Read Timing

Flash Program Timing

Figure 5 illustrates the Flash programming operation for three bytes on a single row. The XADDR is unchanged while PROG and NVSTR are high, but the YADDR changes three times to identify three different bytes in a single row.

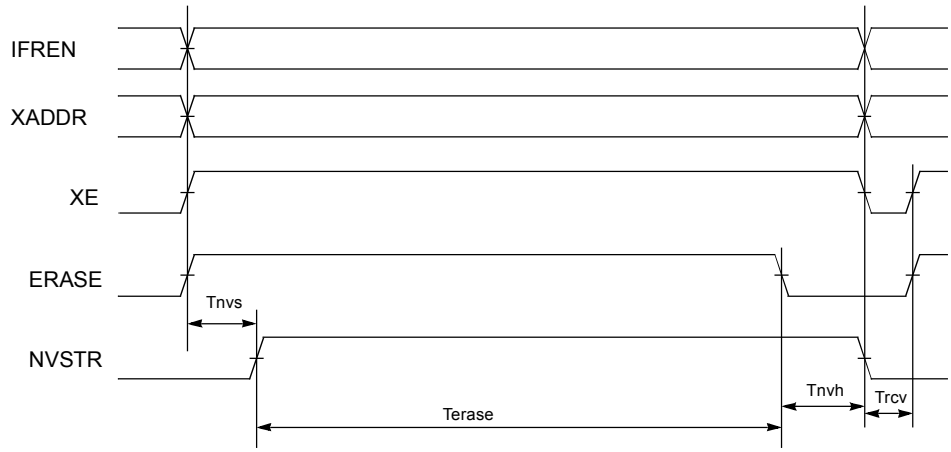


SE = 0, OE = 0, ERASE = 0, MAS1 = 0, TMR = 1

Figure 5. Flash Byte Program Timing

Flash Page Erase Timing

Figure 6 illustrates the timing of a Flash page erase operation.

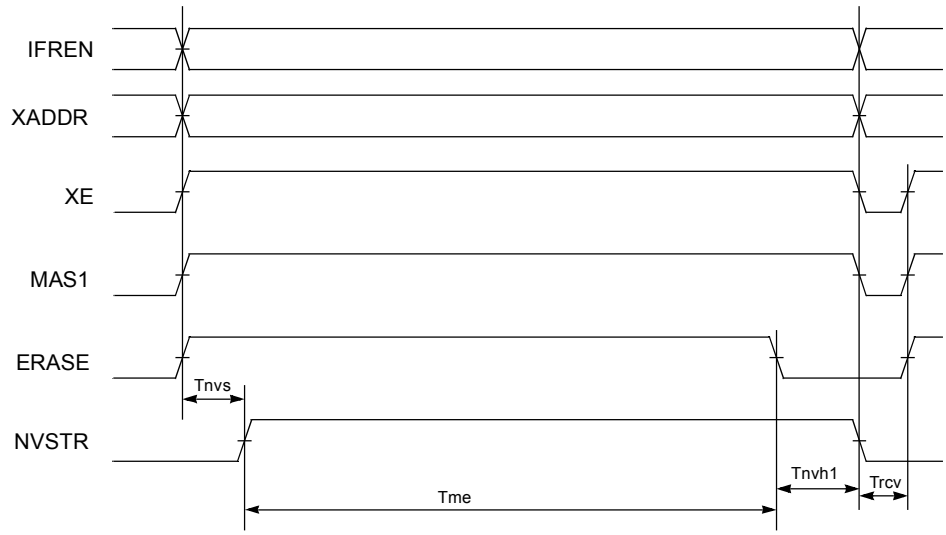


YE = 0, SE = 0, OE = 0, PROG = 0, MAS1 = 0, TMR = 1

Figure 6. Flash Page Erase Timing

Flash Mass Erase Timing

Figure 7 illustrates the timing of a Flash mass erase operation.With IFREN driven high (1), the mass erase operation will erase both the main memory and the information area. With IFREN driven low (0), the mass erase operation will erase only the main memory.



YE = 0, SE = 0, OE = 0, PROG = 0, TMR = 1

Figure 7. Flash Mass Erase Timing

Z8FMC16100 Flash Programming Flowchart

Figure 8 illustrates an example flowchart for read and write operations.

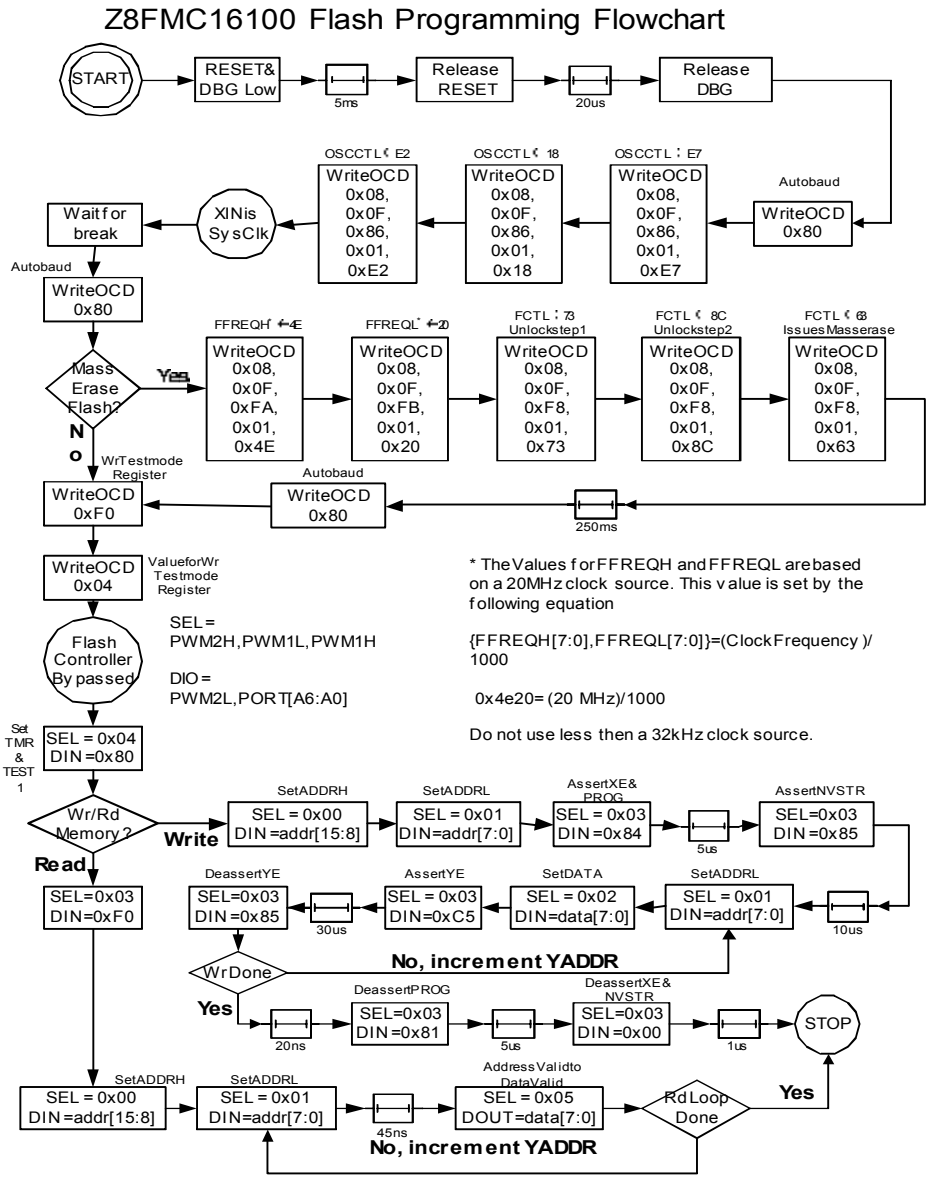


Figure 8. Z8FMC16100 Flash Gang Programming Flow